AN1161
APPLICATION NOTE

Power-up, Reset and Brown-out considerations when using Flash memories

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INTRODUCTION

Many designs do not consider all of the problems associated with power-up, reset and brown-out situations. Most semiconductors are designed to be able to cope with these situations as well as possible, and Flash memory is no exception.

This application note gives some insight into how the Flash memory works internally and highlights how these might affect the operation of your designs under marginal V_{CC} circumstances. Designers of battery powered products should take particular notice of some of the points in this application note.

ADDRESS TRANSITION DETECTION

Before discussing how the Flash behaves during power-up, reset and brown-outs it is important to understand how a read is initiated in the Flash. The external bus on Flash memories is asynchronous. During read operations Chip Enable ($\overline{E}$) and Output Enable ($\overline{G}$) can be left low and address changes will generate new data on the data bus after the t_{AVQV} access time.

Reading the memory array consumes quite a lot of the total power required by the Flash memory. In order to achieve shorter access times, more power is required. Many memories make use of a synchronous internal read cycle with the following steps:

1. Address Transition Detection circuitry detects a change on the address bus and initiates a new synchronous read cycle. Chip Enable low transitions also initiate a new synchronous read cycle.
2. Address decoding selects the correct cells in the memory array.
3. Sense Amplifiers read the state in the cells.
4. Output latches hold the data on the Data Bus and the rest of the memory returns to Standby mode.

Address Transition Detection allows access to the memory array to be faster per unit power consumed. It can also cause some problems that are not obvious for an asynchronous part. Firstly, if the address transition is not detected then the output does not change and secondly if the Sense Amplifiers do not read the correct value, waiting longer will not change the value on the output. These problems rarely, if ever, occur.

POWER-UP

During power-up the rise of V_{CC} is monitored. A synchronous read cycle is not generated until the voltage level is sufficiently high for the memory to operate correctly. This way the memory can start from a reset with Chip Enable tied low, Reset tied High and no address transition before the first read operation; the correct data will be read once the memory is ready.

Older Flash memory parts (prior to 'A' and 'B' revisions) could have problems when accessed after power-up if V_{CC} took longer than 1us to rise. For these parts it was necessary to generate a Chip Enable low signal, an address transition or a reset pulse when V_{CC} was in the operating region, otherwise the output latch could hold invalid data. Most systems do this anyway.

RESET

For parts with Reset pins it is recommended, though not essential, to connect the system reset to the Reset pin. As long as the system reset cannot be in the Not Reset state when V_{CC} is invalid, the Flash will always respond correctly.

BROWN-OUT

A brown-out is when the voltage temporarily drops below the operating voltage level and then recovers. Brown-outs can occur for many reasons. They are hard to detect, particularly when they occur for 20ns or less. Decoupling capacitors remove short glitches; a 0.1µF ceramic capacitor only drops 0.2V/µs when 20mA is being drawn from it. Battery powered products can produce longer brown-outs, particularly when the batteries are running out. If the voltage level drops too far then the internal reset circuitry will reset the Flash once the voltage level recovers to the operating level. However, at some voltages the internal reset is not triggered but the Sense Amplifiers and internal logic are not guaranteed to work correctly.

There are two ways that the Flash can produce an incorrect value during a brown-out. Firstly the address transition detection circuitry does not detect the address transition and secondly the Sense Amplifiers do not read the correct value from the memory array. The value on the output of the Flash will not recover when the voltage recovers to the correct level. A new read operation is required to read the correct data.

Most battery powered applications make use of watchdogs that monitor the voltage levels and reset the system when the voltage drops below a fixed level. Failure during brown-out operations can be avoided by using a watchdog.

CONCLUSION

Flash memories from STMicroelectronics always respond correctly during power-up. Even so, using reset is recommended on parts that have a reset pin. Designers should take care to avoid brown-outs, which can cause the data bus to have invalid data on it when the voltage returns to the operating voltage level.

If you have any questions or suggestion concerning the matters raised in this document please send them to the following electronic mail address:

ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number.