AN1322
APPLICATION NOTE

MIGRATING AN APPLICATION FROM ST7263 REV.B TO ST7263B

by Microcontroller Applications Division

INTRODUCTION

This application note provides information on migrating existing ST7263 Rev. B based applications to the new ST7263B. This document:

– describes the different steps required to upgrade your design environment so as to support the ST7263B,

– lists the device differences that must be taken into account when porting device firmware.

1 DEVICES INVOLVED

– ST72631L4M1/XXX
– ST72T631L4M1
– ST72631K4B1/XXX
– ST72T631K4B1
– ST72632L2M1/XXX
– ST72T632L2M1
– ST72632K2B1/XXX
– ST72T632K2B1
– ST72633L1M1/XXX
– ST72T633L1M1
– ST72633K1B1/XXX
– ST72T633K1B1
– ST72E631K4D1

Note: XXX is the name of the ROM code.

2 DEVELOPMENT TOOLS

Table 1. Development Tool Ordering Information

Device	Emulator	EPROM Programming Board (EPB)
ST7263 Rev. B	ST7263-EMU2	ST7263-EPB
ST7263B	ST7MDTU3-EMU2B	ST7MDTU3-EPB2

If you already have the ST7263-EMU2 emulator, you do not need to order the new emulator. Simply contact our sale office for further information.

3 HARDWARE CHANGES

For a summary of hardware modifications, please refer to Table 2.

3.1 PULL UP VALUE ON RESET PIN

The value of the weak pull-up resistor for the RESET pin changes from 30 kΩ for the ST7263 Rev. B to 100 kΩ for the ST7263B.

3.2 POWER SUPPLY

In ST7263 Rev.B, the operating power supply is between 4.0 V and 6.0 V, while for the ST7263B, the operating supply is as follows:

– 4.0 V to 5.5 V (with USB or Emulator)
– 3.0 V to 5.5 V (when USB is disabled).

3.3 LOW VOLTAGE DETECTOR (LVD)

The LVD generates a Reset when V_{DD} is:

– below 3.80 V for ST7263B (3.75 V for ST7263 Rev. B) when V_{DD} is rising,
– below 3.65 V for ST7263B (3.50 V for ST7263 Rev.B) when V_{DD} is falling.

3.4 INPUT HIGH LEVEL VOLTAGE (VIH)

The V_{IH} value changes from 0.7 x V_{DD} in the ST7263 Rev. B to 0.8 x V_{DD} for the ST7263B.

Table 2. Hardware Comparison Chart

	ST7263 Rev. B	ST7263B
RESET Pull-up Value	30 kΩ	100 kΩ
Power Supply	4.0 to 6.0 V	4.0 to 5.5 V (with USB or Emulator) 3.0 to 5.5 V (when USB is disabled)
LVD Reset Generation	3.75 V when V_{DD} is rising	3.80 V when V_{DD} is rising
	3.50 V when V_{DD} is falling	3.65 V when V_{DD} is falling
V_{IH} Minimum Value	0.7 x V_{DD}	0.8 x V_{DD}

Please refer to the corresponding datasheet for all electrical characteristics.

4 SOFTWARE PORTING

4.1 DEVICE CONFIGURATION

The ST7263B device features an option byte that provides two new optional functions:

– Watchdog hardware selection,

– Read out protection.

This option byte allows the device to be configured independently of the application software. The option byte is also used to control certain functions that were previously managed in the Miscellaneous register (MISCR) in the ST7263 Rev.B:

– 24 or 12 MHz oscillator selection function that provides an internal frequency of either 2, 4 or 8 MHz while maintaining a 6 MHz frequency for the USB

– LVD Reset function that allows the MCU to reset other devices.

Moreover, a new bit, the Slow Mode Select (SMS) bit, is added in the MISCR register and enables an internal divide-by-2 clock divider used to halve the CPU frequency for power saving reasons.

Consequently, the MISCR register of the ST7263 Rev.B and ST7263B are not directly upward compatible and require some software adjustments.

4.1.1 Option Byte Description

Six new configuration options are available as described below.

7							**0**
-	-	WDGSW	WDHALT	LVD	-	OSC24/12	FMP_R

Bit 5 = **WDGSW** *Hardware or Software Watchdog*
This option bit selects the watchdog type.
0: Hardware (watchdog always enabled)
1: Software (watchdog to be enabled by software)

Bit 4 = **WDHALT** *Watchdog and HALT mode*
This option bit determines if a RESET is generated when entering HALT mode while the Watchdog is active.
0: No reset generation when entering HALT mode
1: Reset generation when entering HALT mode.

Bit 3 = **LVD** *Low Voltage Detector selection*
This option bit enables the LVD.
0: LVD Reset enabled
1: LVD Reset disabled

Bit 1 = **OSC24/12** *Quartz Crystal Selection*
This option bit ensures that the USB peripheral is clocked at 6 MHz regardless of the quartz crystal used. The CPU frequency also depends on the context of the MISCR register.
0: 24 MHz oscillator
1: 12 Mhz oscillator

Bit 0 = **FMP_R** *Memory read-out protection*
This option indicates if the user memory is protected against read-out piracy. This protection is based on the read and write protection of the memory in test modes and during In-Application Programming (IAP). If the option bytes are erased when the FMP_R option is selected, the entire user Flash memory will be erased first. As a ROM option, this will be a mask option and not software.
0: Read-out protection enabled
1: Read-out protection disabled

4.1.2 MISCR Register Description

ST7263 Rev. B

7							0
-	-	-	-	LVD	CLKDIV	USBOE	CLKEN

ST7263B

7							0
-	-	-	-	-	SMS	USBOE	MCO

The **LVD** bit has been removed from the MISCR register and added to the option byte. Its behaviour remains unchanged.

The **CLKDIV** bit, which selects either a 12 or 24 MHz quartz crystal, has been removed from the Miscellaneous register and added to the option byte of the ST7263B. For further information, refer to Section 4.1.1 Option Byte Description.

The **CLKEN** and **MCO** bits still have the same function (PA0 outputs the internal CPU clock signal). Only the name has been changed.

The **SMS** bit used for Slow Mode Selection is now available in the Miscellaneous register. If the SMS bit is equal to 1, the CPU frequency is divided by 2.

The following section provides two different tables summarizing how the option byte and miscellaneous register must be programmed in order to be compatible with existing applications based on the ST7263 Rev.B.

4.1.3 Option Byte and Miscellaneous Register Programming

Table 3. ST7263B Configuration for ST7263 Rev.B Upward Compatibility

ST7263 Rev. B Configuration		Equivalent ST7263B Configuration					
LVD (MISCR)	CLKDIV (MISCR)	SMS (MISCR)	Option Byte				
			WDGSW	LVD	OSC24/12	WDHALT	FMP_R
0	0	0	1	0	0	0	1
0	1	0	1	0	1	0	1
1	0	0	1	1	0	0	1
1	1	0	1	1	1	0	1

Table 4. Internal Frequency Configuration

Quartz	OSC24/12 Option Byte (Bit 1)	Slow Mode MISCR (Bit 2)	F_{CPU}	F_{USB}
24 MHz	0	0	8 MHz	6 MHz
24 MHz	0	1	4 MHz	6 MHz
12 MHz	1	0	4 MHz	6 MHz
12 MHz	1	1	2 MHz	6 MHz

4.2 PERIPHERALS

The I²C and USB peripherals are fully software compatible as long as the application software has been recompiled with an updated register map.

4.2.1 Serial Communications Interface (SCI) (Not upward compatible)

Certain new features such as the power down and parity generation/check functions have been added and are controlled by bits that were unused on the ST7263 Rev. B. As long as the following 5 bits are set to 0 on the ST7263 Rev.B software, they are directly upward compatible when recompiled with an updated register map.

The new parity management feature in the ST7263B requires the following configuration in both Transmission and Reception modes:

In the SCICR1 register,

– Bit 5 = **SCID** *SCI Disabled*
When this bit is set, the SCI cell is disabled and power consumption is reduced.

– Bit 2 = **PCE** *Parity Control Enable*
Select the hardware parity control. In transmission, parity is inserted at the MSB position, and parity is checked in Reception mode.

– Bit 1 = **PS** *Parity Selection*
Even (0) or Odd (1)

– Bit 0 = **PIE** *Parity Interrupt Enable*
Generates an interrupt when a parity error is detected.

In the SCISR register,

– Bit 0 = **PE** *Parity Error detection*
This flag is set when a parity error is detected in Reception mode.

The baud rate value selection has also been changed. In the new version, all transmission and reception rates are multiplied by two.

Consequently, the contents of the Baud Rate (SCIBRR) register for the ST7263B must be updated to match certain ST7263 Rev.B rates.

For example, to obtain the same baud rate (1200 baud), the SCP[1:0] and SCT[2:0] bits in the SCIBRR register must be configured as follows:

Table 5. Baud Rate Register Comparison Chart

ST7263 Rev. B		**ST7263B**	
SCP[1:0]	SCT[2:0]	SCP[1:0]	SCT[2:0]
11	100	11	101

4.2.2 Timer (Upward compatible)

The 16-bit timer of the ST7263B has been modified to solve certain issues related to PWM and One Pulse modes.

4.2.2.1 PWM Mode

To prevent uncontrolled states from being output in PWM mode, a double buffering on the output compare registers (2x16 bits) is implemented in the ST7263B.

Any new values written in the four OC1R and OC2R registers are taken into account only at the end of the PWM period (OC2 event) to prevent spikes from occurring on the PWM output.

4.2.2.2 One Pulse Mode

One Pulse mode has been improved in the ST7263B version to increase efficiency. When the ICAP1 event is detected (on the falling or rising edge), the IC1R register is loaded with the value of the counter, which is then reset to FFFCh. The rest of the sequence remains unchanged.

4.3 REGISTER MAP

A new line must be inserted in the Register Map corresponding to the FLASH Control and Status Register (FCSR).

Address: 0037h
Read/Write
Reset Value: 0000 0000 (00h)

7							0
0	0	0	0	0	0	0	0

This register is reserved for use by the Programming Tool software. It controls the FLASH programming and erasing operations. For details on customizing FLASH programming methods and In-Circuit Testing, refer to the ST7 FLASH Programming and ICC Reference Manual.

Table 6. Interrupt Vector Addresses

Vector Address	ST7263 Rev.B	ST7263B
FFEE - FFEF	--	USB interrupt vector
FFF0 - FFF1	USB interrupt vector	SCI interrupt vector
FFF2 - FFF3	SCI interrupt vector	I²C interrupt vector
FFF4 - FFF5	I²C interrupt vector	Timer interrupt vector
FFF6 - FFF7	Timer interrupt vector	IT1 to IT8 interrupt vector
FFF8 - FFF9	IT1 to IT8 interrupt vector	USB end suspend mode interrupt vector
FFFA - FFFB	USB End Suspend mode interrupt vector	FLASH Start Programming interrupt vector
FFFC - FFFD	TRAP interrupt	TRAP interrupt
FFFE - FFFF	RESET vector	RESET vector

4.3.1 RAM

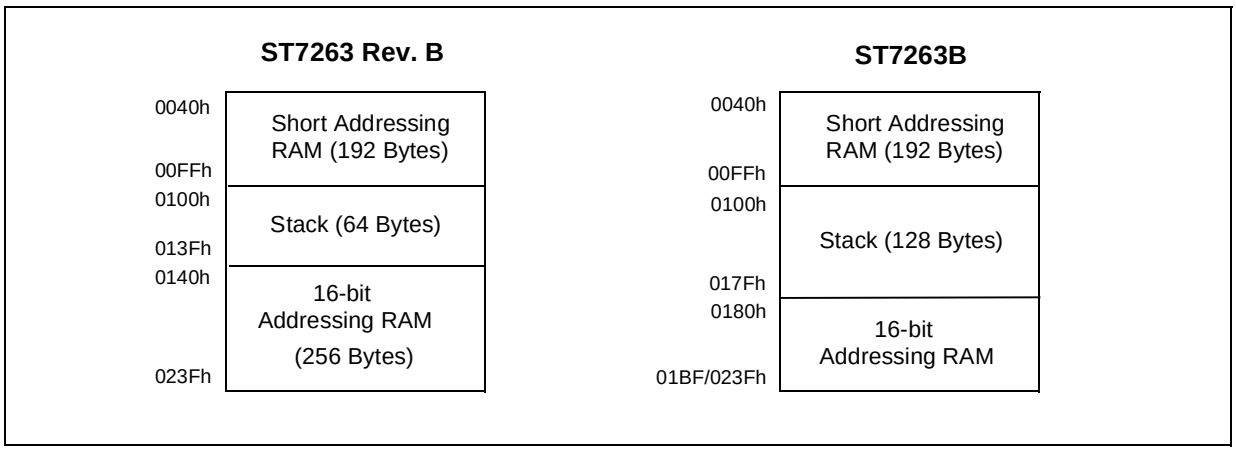
In the ST7263 Rev. B, the DATA RAM is up to 512 bytes with 64-byte stacks. In the ST7263B version, the DATA RAM is 512 bytes with 128-byte stacks. Therefore, the stack address is also changed:

– In ST7263 Rev.B, the stack is from 0100h to 013Fh
– In ST7263B, the stack is from 0100h to 017Fh

In the same way, 16-bit addressing RAM size is reduced:

– In ST7263 Rev.B, the 16-bit addressing RAM is from 0140h to 023Fh
– In ST7263B, the 16-bit addressing RAM is from 0180h to 023Fh

Figure 1. RAM Memory Map



* Program memory and RAM sizes are product dependent. See specific datasheet for more information.

5 FEATURE COMPARISON CHART

	ST7263 rev.B	ST7263B
Package	CSDIP32W, PSDIP32, SO34	SDIP32, SO34, CQFP64
Program Memory	4K, 8K or16K (OTP or ROM)	4K, 8 K (Flash or ROM) or 16K (Flash)
RAM	256 bytes for 4K and 8K 512 bytes for 16K with 64-byte stack	384 bytes for 4K and 8K 512 bytes for 16K with 128-byte stack
Register Map	64 bytes	64 bytes (Minor changes)
I/Os	19 pins	19 pins (Unchanged)
12/24 MHz Oscillator	Selected in Miscellaneous register	Selected in Option Byte
MISCR Register	Yes	Not upward compatibility
Watchdog	Yes	Yes (Unchanged)
16-bit Timer	Yes	Yes (Minor change in PWM and One Shot modes)
I²C	Yes	Yes (Unchanged)
SCI	Yes	New features, not upward compatible
ADC	Yes	Yes (Unchanged)
LVD	Selected in Miscellaneous register	Selected in Option Byte
USB	Yes	Yes (Unchanged)
Power Supply	4.0 V to 6.0 V	4.0 V to 5.5 V
RESET	RESET Pad pull-up is 30 kΩ	RESET Pad pull-up is 100 kΩ
Interrupt Vector Map	FFF0 - FFFF	FFEE - FFFE (due to Flash IT insertion)

For more detailed information, please refer to the ST7263B Datasheet.

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