Features

- **High Performance ULC Family Suitable for Latest CPLDs and FPGAs**
- **From 82 K Gates up to 1575 K Gates Supported**
- **From 62 Kbit to 1195 Kbit DPRAM**
- **Compatible with Xilinx or Altera Latest FPGA's**
- **Pin-counts to Over 976 pins**
- **VDD 1.8V +/- 0.15V for core: 1.8, 2.5, 3.3V for Periphery**
- **Any Pin–out Matched**
- **Full Range of Packages: DIP, SOIC, LCC/PLCC, PQFP/TQFP, BGA, PGA/PPGA**
- **Available in Commercial and Industrial Grades**
- **0.18 µm Drawn CMOS, 5 and 6 Metal Layers**
- **Library Optimised for Synthesis, Floor Plan & Testability Generation (ATPG)**
- **High System Frequency Skew Control**
  - **Clock Tree Synthesis Software**
- **Power on Reset**
- **Standard 2, 4, 6, 8,10, 12 and 16mA I/Os**
- **CMOS/TTL/PCI Interface LVCMOS, LVTTL, GTL, HSTL, LVDS Interfaces**
- **High Noise & EMC Immunity**
  - **I/O with Slew Rate Control**
  - **Internal Decoupling**
  - **Signal Filtering between Periphery & Core**
- **Thick Oxide Matrices Allowing Interface with 2.5V and 3.3V Environments**

Description

The ATU18 series of ULCs is well suited for conversion of latest CPLDs and FPGAs. We can support within one ULC from 62 Kbits to 1195 Kbits DPRAM and from 82 Kgates to 1575 Kgates. Typically, ULC die size is 50% smaller than the equivalent FPGA die size. DPRAM blocks are compatible with Xilinx or Altera FPGA blocks at metal level.

Devices are implemented in high–performance CMOS technology with 0.18µm (drawn) channel lengths, and are capable of supporting flip–flop toggle rates of 180 MHz at 1.8 V, and input to output delays as fast as 100ps at 1.8V. The architecture of the ATU18 series allows for efficient conversion of latest CPLD and FPGA device types with higher IO count. A compact RAM cell, along with the large number of available gates allows the implementation of RAM in FPGA architectures that support this feature, as well as JTAG boundary–scan and scan–path testing.

Conversion to the ATU18 series of ULC can provide a significant reduction in operating power when compared to the original PLD or FPGA. This is especially true when compared to many PLD and CPLD architecture devices, which typically consume 100mA or more even when not being clocked. The ATU18 series has a very low standby consumption of less than 0.3nA/gate typically commercial temperature. Operating consumption is a strict function of clock frequency, which typically results in a power reduction of 50% to 90% depending on the device being compared.

0.18 µm ULC Series with Embedded DPRAM

ATU18

Rev. 4318A–ULC–01/04

The ATU18 series provides several options for output buffers, including a variety of drive levels up to 16mA. Schmitt trigger inputs are also an option. A number of techniques are used for improved noise immunity and reduced EMC emissions, including: several independent power supply busses and internal decoupling for isolation; slew rate limited outputs are also available if required.

The ATU18 series is designed to allow conversion of high performance 1.8V devices. Support of mixed supply conversions is also possible, allowing optimal trade–offs between speed and power consumption.

Array Organization

Table 1. Matrices

Part Number	Max Pads	KGates	DPRAM Kbits	PLL
UIJ700	700	1575	1195	4
UIJ600	600	1157	878	4
UIJ540	540	937	711	4
UIJ484	484	753	571	4
UIJ432	432	600	455	4
UIJ388	388	484	367	4
UIJ352	352	398	303	4
UIJ304	304	297	225	2
UIJ256	256	210	160	2
UIJ228	228	167	127	2
UIJ208	208	139	105	2
UIJ160	160	82	62	2

Note: All arrays with internal POR and optional multiplier blocks

Architecture

The basic element of the ATU18 family is called a cell. One cell can typically implement between one to four FPGA gates. Cells are located contiguously throughout the core of the device, with routing resources provided in three to four metal layers above the cells. Some cell blockage does occur due to routing, and utilization will be significantly greater with three metal routing than two. The sizes listed in the Product Outline are estimated usable amounts using three metal layers. I/O cells are provided at each pad, and may be configured as inputs, outputs, I/Os, V_{DD} or V_{SS} as required to match any FPGA or PLD pinout.

In order to improve noise immunity within the device, separate V_{DD} and V_{SS} busses are provided for the internal cells and the I/O cells.

I/O Buffer Interfacing

I/O Flexibility

All I/O buffers may be configured as input, output, bi-directional, oscillator or supply. A level translator could be located close to each buffer.

I/O Options

Inputs

Each input can be programmed as TTL, CMOS, or Schmitt Trigger, with or without a pull up or pull down resistor.

Fast Output Buffer

Fast output buffers are able to source or sink 2 to 16mA at 3.3V according to the chosen option. 32mA achievable, using 2 pads.

Slew Rate Controlled Output Buffer

In this mode, the p– and n–output transistors commands are delayed, so that they are never set “ON” simultaneously, resulting in a low switching current and low noise. These buffers are dedicated to very high load drive.

Power Supply and Noise Protection

In order to improve the noise immunity of the ATU18 core matrix, several mechanisms have been implemented inside the ATU18 arrays. Two types of protection have been added: one to limit the I/O buffer switching noise and the other to protect the I/O buffers against the switching noise coming from the matrix.

The speed and density of the ATU18 technology cause large switching current spikes, for example when:

- 16 high current output buffers switch simultaneously, or
- 10% of the 700 000 gates are switching within a window of 1ns.

Sharp edges and high currents cause some parasitic elements in the packaging to become significant. In this frequency range, the package inductance and series resistance should be taken into account. It is known that an inductor slows down the setting time of the current and causes voltage drops on the power supply lines. These drops can affect the behavior of the circuit itself or disturb the external application (ground bounce).

I/O Buffers Switching Protection

Three features are implemented to limit the noise generated by the switching current:

- The power supplies of the input and output buffers are separated.
- The rise and fall times of the output buffers can be controlled by an internal regulator.
- A design rule concerning the number of buffers connected on the same power supply line has been imposed.

Matrix Switching Current Protection

This noise disturbance is caused by a large number of gates switching simultaneously. To allow this without impacting the functionality of the circuit, three new features have been added:

- Decoupling capacitors are integrated directly on the silicon to reduce the power supply drop.
- A power supply network has been implemented in the matrix. This solution reduces the number of parasitic elements such as inductance and resistance and constitutes an artificial V_{DD} and Ground plane. One mesh of the network supplies approximately 150 cells.
- A low pass filter has been added between the matrix and the input to the output buffer. This limits the transmission of the noise coming from the ground or the V_{DD} supply of the matrix to the external world via the output buffers.

Electrical Characteristics

Absolute Maximum Ratings*

Operating Temperature	
Commercial	0° to 70°C
Industrial	-40° to 85°C
Max Supply Core Voltage (V_{DD})	1.95 V
Max Supply Periphery Voltage (V_{CC})	3.6V
3.3V Tolerant/Compliant V_{CC}	+0.3V
Storage Temperature	-65° to 150°C
Operating Ambient Temperature	-55° to 125°C

*NOTICE: Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

This value is based on the maximum allowable die temperature and the thermal resistance of the package.

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