High-Performance MIPS® System Controller for Communications Applications
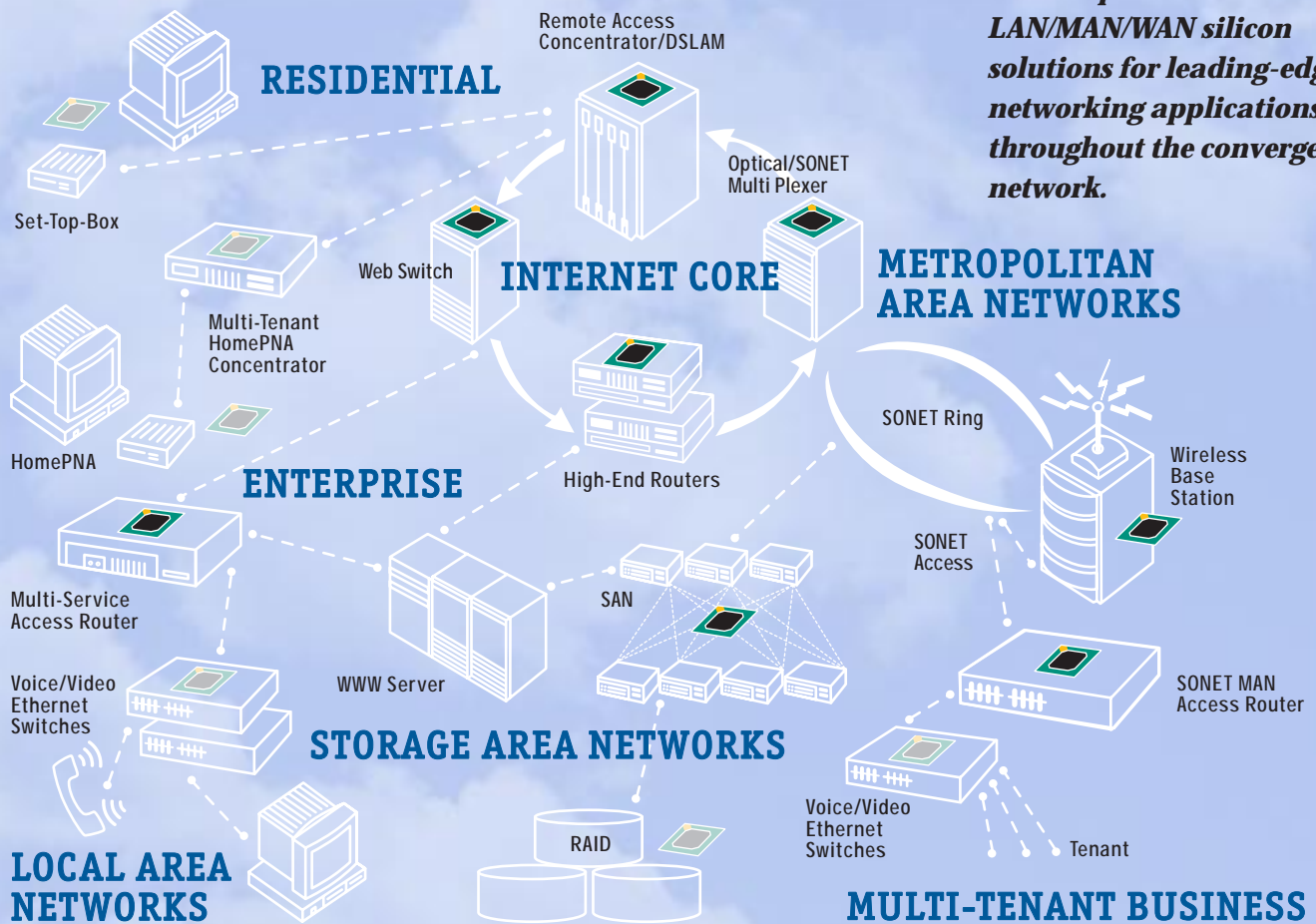
The Discovery™ GT-64240 provides a breakthrough in MIPS®-based communications systems architecture, setting a new standard for performance and integration.

Galileo
TECHNOLOGY
A Division of Marvell™
Discovery™
GT-64240

Discovery™

NETWORK APPLICATIONS

Marvell provides advanced LAN/MAN/WAN silicon solutions for leading-edge networking applications throughout the converged network.

RESIDENTIAL

Remote Access Concentrator/DSLAM

Optical/SONET Multi Plexer

Set-Top-Box

Web Switch

INTERNET CORE

METROPOLITAN AREA NETWORKS

Multi-Tenant HomePNA Concentrator

SONET Ring

HomePNA

ENTERPRISE

High-End Routers

Wireless Base Station

SONET Access

Multi-Service Access Router

SAN

Voice/Video Ethernet Switches

WWW Server

SONET MAN Access Router

STORAGE AREA NETWORKS

Voice/Video Ethernet Switches

LOCAL AREA NETWORKS

RAID

Tenant

MULTI-TENANT BUSINESS

Marvell's highly integrated communications systems on silicon simplifies designs, reduces development risks and costs, and substantially improves time-to-market for manufacturers of data communications and telecommunications equipment. Marvell's semiconductor chips are highly-integrated, scalable, programmable, and flexible to meet the demands of technologically sophisticated network applications.

Discovery™ GT-64240 Controller Application Solutions

Additional Marvell Application Solutions

MARVELL PRODUCT FAMILIES

| Family	Number of Products	Feature Summary
High-Performance System Controllers for MIPS® and PowerPC®–Based Systems	13	*Integrated CPU interface with PCI, memory and peripheral controllers*
Discovery™ Family of High-Performance System Controllers for Communications Applications	6	*Integrated system controllers with LAN, WAN, and peripheral interface ports*
Horizon™ WAN Communications Controllers for MIPS and PowerPC–Based Communications Systems	3	*Multi-channel T1/E1, T3/E3 WAN interfaces, 10/100 Ethernet ports, integrated system and communications peripherals*
GalNet®-II, GalNet-2+ Switched Ethernet Controllers	24	*Scalable 10/100 and Gigabit Ethernet switch family for advanced workgroup and chassis applications*
GalNet®-3 Layer 3/4/5 Converged Voice/Video/Data Network Switch Processors	7	*Scalable 10/100 and Gigabit Ethernet routing switch family for converged enterprise LAN and MAN applications*

The Industry's Most Powerful System Controller

TYPICAL COMMUNICATIONS SYSTEM ARCHITECTURE

Innovative Architecture for Communications Applications Delivers Superior Performance

A highly integrated solution, the Discovery™ GT-64240 is a full-featured system controller that combines high-performance system and communications peripherals on a single chip. The GT-64240 is ideally suited for next-generation communications systems designed to meet ever increasing system performance needs. Typical applications for the GT-64240 include core and edge routers, web switches, optical network hardware, load balancing and traffic management systems, wireless base stations, VPN gateways, and storage gateways.
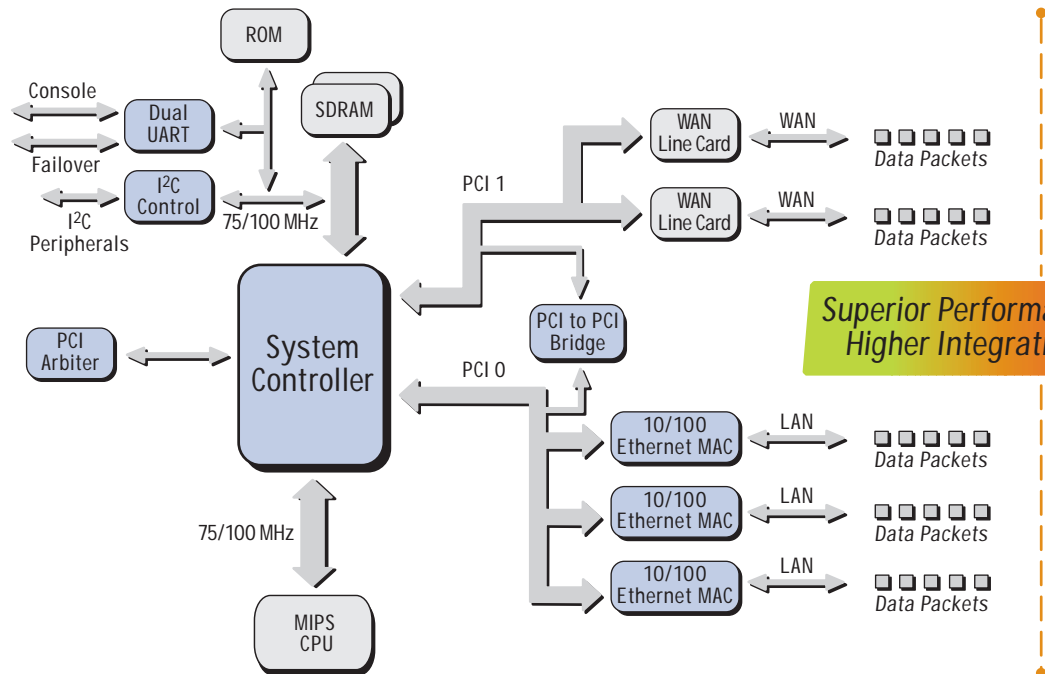
Innovative Architecture and High-Speed Interfaces Deliver Superior Performance

The Discovery™ GT-64240 supports industry standard MIPS® processors, including PMC-Sierra's™ RM7000x, RM527x, RM526x as well as other R4xxx and R5000 processors. Both traditional SysAD and the extended PMC-Sierra's MIPS RM7000x bus protocols are supported. An on-chip SDRAM memory controller with a 72-bit wide (64-bit with 8-bit ECC), 100 MHz interface enables high speed data transactions between memory, processor and PCI peripherals.

Advanced Crossbar Fabric

The Discovery GT-64240 architecture employs a high-speed crossbar fabric to enable non-blocking concurrent transactions between the CPU, PCI, LAN, WAN, and memory, greatly enhancing overall system performance.

The internal crossbar fabric provides an aggregate throughput of 76 Gbps to deliver unprecedented performance for next-generation communications equipment.

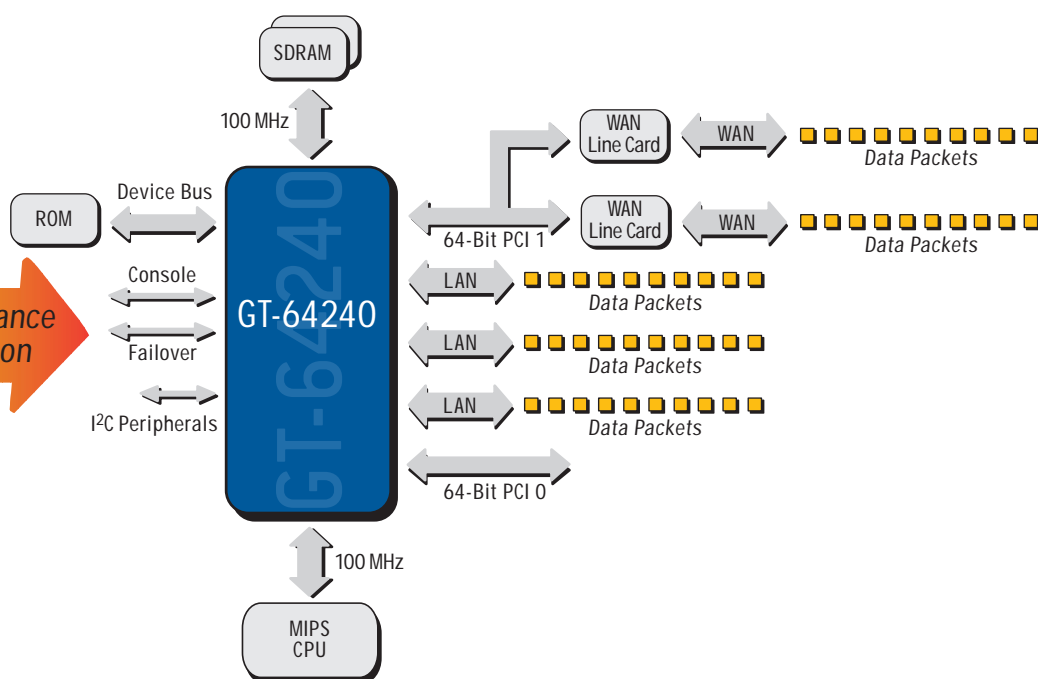### High Integration Reduces Design Time and Board Space Requirements

The Discovery GT-64240 integrates system peripherals necessary to build a high performance MIPS system: PCI bridge and arbiter, interrupt controller, eight channel DMA engine, I²C controller, timers, multi-channel device bus interface, and a 72-bit SDRAM memory controller. In addition, three 10/100 Ethernet controllers and two Multi-Protocol Serial Controllers (MPSCs) are integrated for communications applications. The MPSCs can be used as UARTs if needed.

Ideal for Communications Applications

Three 10/100 Mbps full-duplex Ethernet

DISCOVERY™ GT-64240 BASED ARCHITECTURE

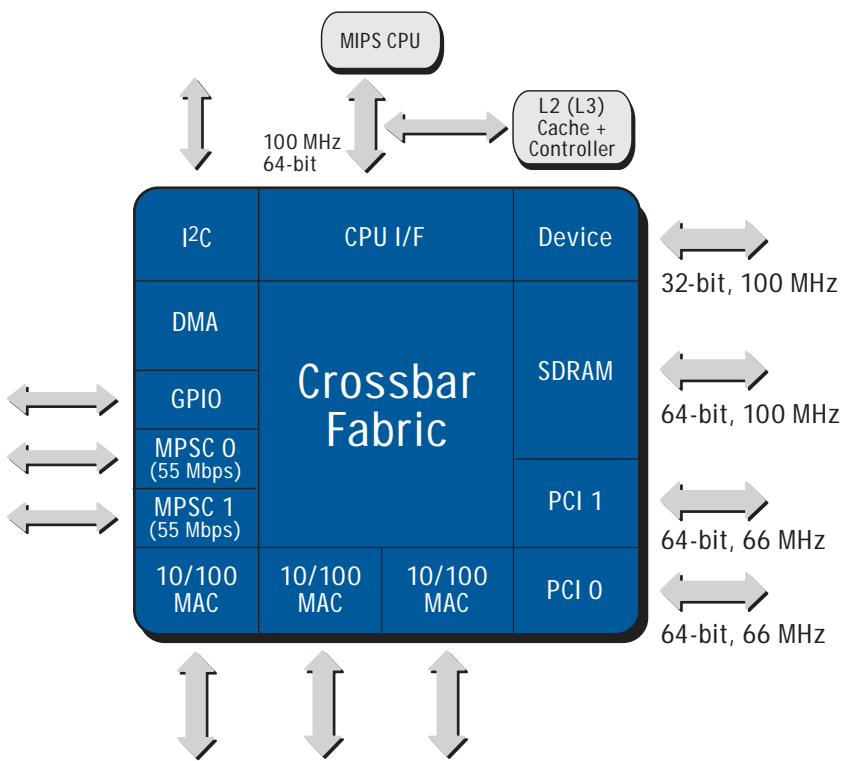**Integrated Crossbar Maximizes System Bandwidth**

The Discovery™ GT-64240 chip combines an advanced high-performance crossbar architecture with Marvell's market-leading system controller technology to deliver unprecedented performance. With an aggregate throughput of 76 Gbps, the GT-64240's crossbar fabric supports non-blocking concurrent transactions among peripherals at full bus speeds.

Discovery EV-64240 Development Platform

· System-level development platform supporting the PMC-Sierra RM7000A MIPS CPU

· Wind River VxWorks® Board Support Package available

· Four 32/64-bit PCI expansion board slots

· Three 10/100 Mbps Ethernet ports

· Two serial ports (UART, LVDS, and V.35 PHY modules available)

· Supports 72-bit SDRAM DIMMs (up to 2 GB)

ports on the Discovery GT-64240 are fully compliant with IEEE 802.3/802.3u standards and integrate MAC functionality with a dual speed MII/RMII interface. The GT-64240 supports Auto-Negotiation of port speed (10 or 100 Mbps) and communications mode (half or full-duplex) through the PHY. Up to 8K MAC addresses can be up filtered with on-chip logic allowing a packet to be discarded at the MAC level before precious bandwidth is wasted on storing and analyzing the packet by the CPU.

The GT-64240 has Quality of Service (QoS) features to enable flow classification based on packet content. Each GT-64240 Ethernet MAC includes two transmit and four receive priority queues. Data can be queued based on MAC addresses, 802.1p tags or IP header Type of Service (ToS) fields. As the packet classification is done in hardware by the GT-64240 at the MAC level, CPU processing

bandwidth is saved for other critical application functions. The GT-64240 supports several packet-based WAN interfaces including ISDN, frame relay, unchannelized T1/T3, xDSL (HDSL2, SDSL), HSSI, and more. Two on-chip MPSCs support UART, HDLC, BISYNC, and Transparent protocols, and can be configured as simple debug/console ports if needed.

Flexible PCI Architecture

The Discovery GT-64240 can be configured to support two independent 64-bit/32-bit PCI interfaces. Each PCI interface can operate at up to 66 MHz with zero wait states. The PCI units can act either as a master, initiating a PCI-bus transaction or as a slave, responding to PCI-bus transactions. The PCI-to-PCI transaction bridging and PCI arbitration logic are integrated to optimize system performance and simplify board design.

High Integration
Reduces Design Time

DISCOVERY™ GT-64240 BLOCK DIAGRAM

MIPS CPU

L2 (L3) Cache + Controller

100 MHz 64-bit

I²C	CPU I/F	Device
DMA	Crossbar Fabric	SDRAM
GPIO		
MPSC 0 (55 Mbps)		PCI 1
MPSC 1 (55 Mbps)		
10/100 MAC	10/100 MAC	10/100 MAC	PCI 0

32-bit, 100 MHz

64-bit, 100 MHz

64-bit, 66 MHz

64-bit, 66 MHz

DISCOVERY DEVELOPMENT PLATFORM

FEATURE HIGHLIGHTS:

Discovery™ GT-64240 Features

- High-Performance 64-Bit MIPS CPU Interface

- 64-Bit SDRAM Controller

- Integrated System Peripherals

- Eight Independent Direct Memory Access (IDMA) Channels

- Three 10/100 Mbps Fast Ethernet MACs

- Two Multi-Protocol Serial Controllers

- Dual 32/64-Bit, 66 MHz PCI 2.2 Interfaces

- Supports Full-Duplex OC-48 Data Rates

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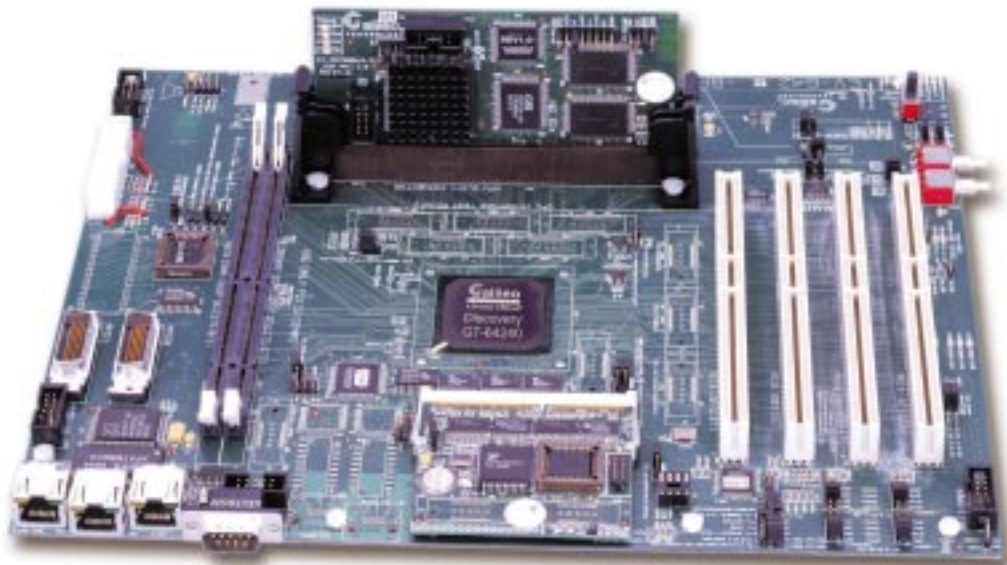
Family	CPU Interface	Frequency	SDRAM Support	Device Support	I/O Support	Package	Voltage
GT-64240	R5K/R7K MIPS® 64-Bit SysAD	100 MHz	4 GB 64-Bit, 100 MHz SDRAM	32-Bit, 100 MHz 5 Chip Selects	2x64-Bit 66 MHz PCI 3 X Fast Ethernet 2 X MPSC (HDLC)	665 BGA	1.8V Core 2.5/3.3V I/O

Discovery™

High-Performance Controller for MIPS-Based Communications Systems
- 64-bit 100 MHz CPU bus interface
- 72-bit (64-bit with 8-bit ECC) 100 MHz SDRAM controller
- Dual 32/64-bit 66 MHz PCI interfaces
- Advanced internal crossbar fabric
- 32-bit 100 MHz peripheral device bus interface

Integrated Systems Peripherals
- Interrupt controller
- 8 channel DMA controller
- Device bus controller
- PCI arbiter
- Master/slave I^{2}C controller
- SDRAM controller
- Timers

Advanced Communications Unit
- Three 10/100 Ethernet controllers with packet filtering and priority queuing
- Two Multi-Protocol Serial Controllers (MPSCs)

64-Bit MIPS CPU Bus Interface
- PMC-Sierra RM526X, RM527X, RM7000x and other MIPS R4xxx, R5000 processor support
- Traditional SysAD and PMC-Sierra RM7000x (extended bus protocols)
- 100 MHz CPU bus frequency (2.5V or 3.3V configuration)
- Supports PMC-Sierra RM7000x splitread transactions with out-of-order completion

High-Performance SDRAM Controller
- 100 MHz memory interface
- 4 GB address space
- Supports 2-way and 4-way bank interleaving
- Supports up to 16 open pages

Data Integrity Support Between CPU, PCI and DRAM Interfaces
- ECC on 64-bit wide SDRAM
- Parity support on CPU and PCI buses
- Full error reporting including error counters

32/64-Bit, 66 MHz PCI 2.2 Interface
- Dual PCI interface
- 32 or 64-Bit, 66 MHz PCI interface
- Transaction bridging between PCI interfaces
- Supports PCI delayed read transactions

Advanced 0.18u Process
- 1.8V core
- 2.5V/3.3V CPU interface
- 3.3V I/O
- 5V tolerant PCI interface
- 100 MHz speed

665 PBGA Package