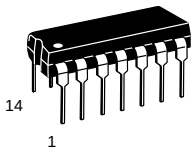
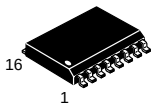
MC145436A

Advance Information

Low-Power Dual Tone Multiple Frequency Receiver



P SUFFIX
PLASTIC DIP
CASE 646



DW SUFFIX
SOG PACKAGE
CASE 751G

ORDERING INFORMATION

MC145436AP	Plastic DIP
MC145436ADW	SOG Package

The MC145436A is a low–power and improved input sensitivity version of the MC14LC5436.

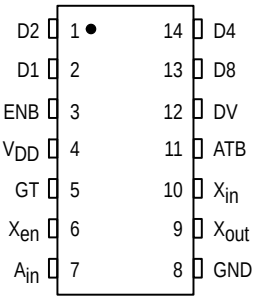
The MC145436A is a silicon gate CMOS LSI device containing the filter and decoder for detection of a pair of tones conforming to the DTMF standard with outputs in hexadecimal. Switched capacitor filter technology is used together with digital circuitry for the timing control and output circuits. The MC145436A provides excellent power line noise and dial tone rejection and is suitable for applications in central office equipment, PABX, and keyphone systems, remote control equipment and consumer telephony products.

The MC145436A offers the following performance features:

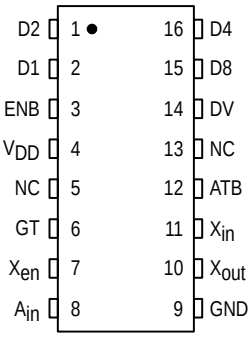
- Single + 5 V Power Supply
- Detects All 16 Standard Digits
- Uses Inexpensive 3.58 MHz Crystal
- Provides Guard Time Controls to Improve Speech Immunity
- Output in 4–Bit Hexadecimal Code
- Built–In 60 Hz and Dial Tone Rejection
- Pin Compatible with SSI–204, MC145436, and MC14LC5436
- Functional and Applicational Compatible with MC145436 and MC14LC5436

PIN ASSIGNMENTS

PDIP



SOG

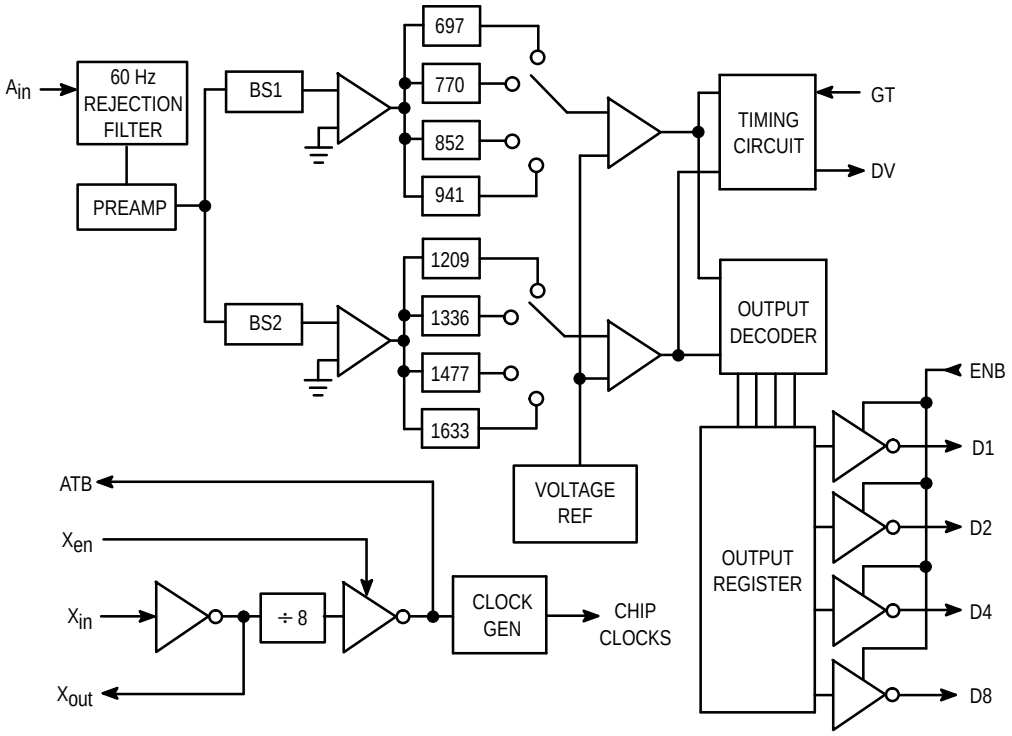


NC = NO CONNECTION

REV 1
1/96

MOTOROLA

BLOCK DIAGRAM



MAXIMUM RATINGS (Voltages Referenced to GND Unless Otherwise Noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 6.0	V
Input Voltage, Any Pin Except A_{in}	V_{in}	– 0.5 to V_{DD} + 0.5	V
Input Voltage, A_{in}	V_{in}	V_{DD} – 10 to V_{DD} + 0.5	V
DC Current Drain per Pin	I	± 10	mA
Power Dissipation	P_D	100	mW
Operating Temperature Range	T_A	– 40 to + 85	°C
Storage Temperature Range	T_{stg}	– 65 to + 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages to this high impedance circuit.

For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are tied to and appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

ELECTRICAL CHARACTERISTICS

(All Polarities Referenced to V_{SS} = 0 V, V_{DD} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

Parameter		Symbol	Min	Typ	Max	Unit
DC Supply Voltage		V_{DD}	4.5	5	5.5	V
Supply Current (f_{CLK} = 3.58 MHz)		I_{DD}	—	5	8	mA
Input Current	GT ENB, X_{in}, X_{en}	I_{in}	— —	— —	450 ± 1	µA
Input Voltage Low	ENB, GT, X_{en}	V_{IL}	—	—	1.5	V
Input Voltage High	ENB, GT, X_{en}	V_{IH}	3.5	—	—	V
I_{out} Data and DV Pins: V_{out} = 4.5 V (Source)		I_{OH}	800	—	—	µA
I_{out} Data and DV Pins: V_{out} = 0.4 V (Sink)		I_{OL}	1.0	—	—	mA
Input Impedance	A_{in}	R_{in}	90	100	—	kΩ
Fanout	ATB	F_{out}	—	—	10	
Input Capacitance	X_{en}, ENB	C_{in}	—	6	—	pF

ANALOG CHARACTERISTICS (V_{DD} = 5.0 V ± 10%, T_A = – 40 to + 85°C, Unless Otherwise Noted)

Parameter	Min	Typ	Max	Unit
Signal Level for Detection (A_{in})	– 35	—	– 2	dBm
Twist = High Tone/Low Tone	– 10	—	10	dB
Frequency Detect Bandwidth	± (1.5 + 2 Hz)	± 2.5	± 3.5	% f_O
60 Hz Tolerance	—	—	0.8	Vrms
Dial Tone Tolerance (Note 1) (Dial Tone 330 + 440)	—	—	0	dB
Noise Tolerance (Notes 1 and 2)	—	—	– 12	dB
Power Supply Noise (Wide Band)	—	—	10	mV p–p
Talk Off (Mitel Tape #CM7290)	—	2	—	Hits

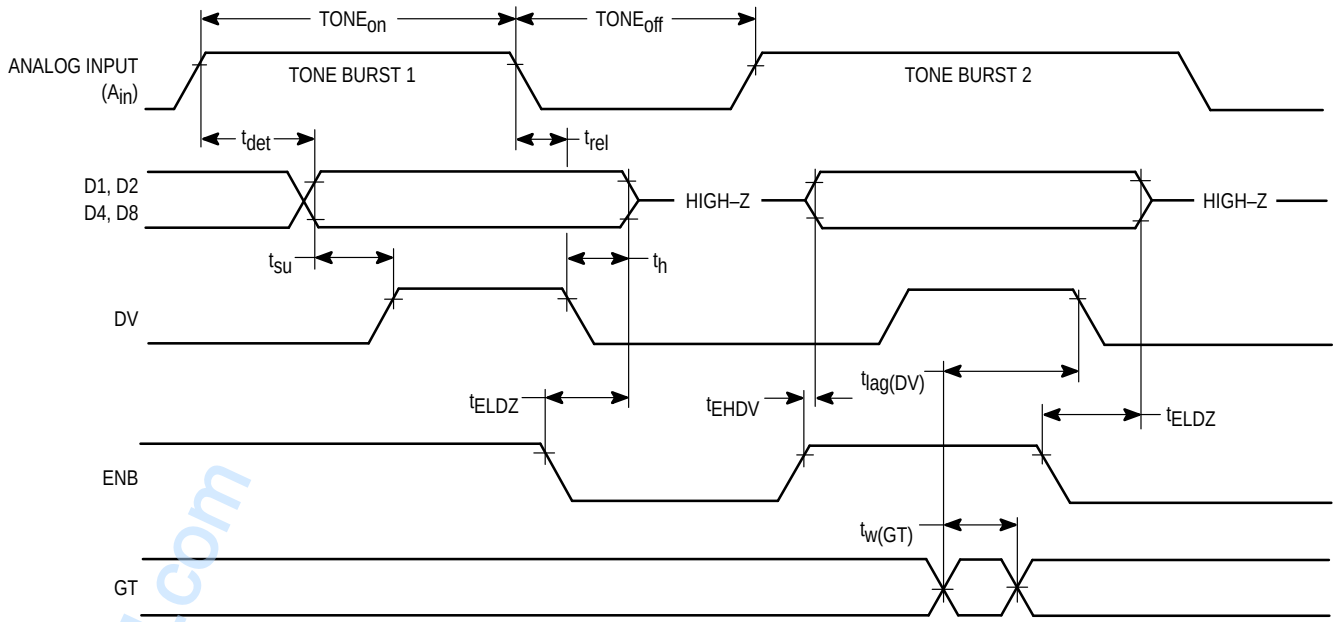
NOTES:
1. Referenced to lower amplitude tone.
2. Bandwidth limited (0 to 3.4 kHz) Gaussian Noise.

AC CHARACTERISTICS (V_{DD} = 5.0 V ± 10%, T_A = – 40 to + 85°C)

Characteristic		Symbol	Min	Typ	Max	Unit
Tone On Time	For Detection For Rejection	$TONE_{on}$	40 —	— —	— 20	ms
Pause Time	For Detection For Rejection	$TONE_{off}$	40 —	— —	— 20	ms
Detect Time	GT = 0 GT = 1	t_{det}	22 32	— —	40 50	ms
Release Time	GT = 0 GT = 1	t_{rel}	28 18	— —	40 30	ms
Data Setup Time		t_{su}	7	—	—	µs
Data Hold Time		t_h	4.2	4.6	5	ms
Pulse Width	GT	$t_{w(GT)}$	18	—	—	µs
DV Reset Lag Time		$t_{lag(DV)}$	—	—	5	ms
ENB High to Output DV*		t_{EHDV}	—	120	500	ns
ENB Low to Output High–Z*		t_{ELDZ}	—	110	300	ns

* Data out: C_L = 35 pF ‖ R_L = 500 Ω.

TIMING DIAGRAM



PIN DESCRIPTIONS

V_{DD}
Positive Power Supply (PDIP, SOG — Pin 4)

The digital supply pin, which is connected to the positive side of the power supply.

V_{SS}
Ground (PDIP — Pin 8, SOG — Pin 9)

Ground return pin is typically connected to the system ground.

D1, D2, D4, D8
Data Output (PDIP — Pins 2, 1, 14, 13; SOG — Pins 2, 1, 16, 15)

These digital outputs provide the hexadecimal codes corresponding to the detected digit. The digital outputs become valid after a tone pair has been detected and are cleared when a valid pause is timed. See Table 1 for hexadecimal codes.These output pins are high impedance when the enable pin is at logic 0.

ENB
Enable (PDIP, SOG — Pin 3)

Outputs D1, D2, D4, D8 are enabled when ENB is at a logic 1, and high impedance (disabled) when ENB is at a logic 0.

GT
Guard Time (PDIP — Pin 5, SOG — Pin 6)

The guard time control input provides two sets of detected time and release time, both within the allowed ranges of tone on and tone off (see Figure 1). A longer tone detect time rejects signals too short to be considered valid. With GT = 1, talk off performance is improved, since it reduces the probability that tones simulated by speech will maintain signal conditions long enough to be accepted. In addition, a shorter release time reduces the probability that a pause simulated by an interrupt in speech will be detected as a valid pause. On the other hand, a shorter tone detect time with a long release time would be appropriate for an extremely noisy environment where fast acquisition time and immunity to dropouts would be required. In general, the tone signal time generated by a telephone is 100 ms, nominal, followed by a pause of about 100 ms. A high–to–low or low–to–high transition on the GT pin resets the internal logic and the MC145436A is immediately ready to accept a new tone input. If left open, this pin is internally pulled to ground.

Table 1. Hexadecimal Codes

Digit	Output Code			
	D8	D4	D2	D1
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	1	0	1	0
*	1	0	1	1
#	1	1	0	0
A	1	1	0	1
B	1	1	1	0
C	1	1	1	1
D	0	0	0	0

X_{en}
Oscillator Enable (PDIP — Pin 6, SOG — Pin 7)

A logic 1 on X_{en} enables the on–chip crystal oscillator. When using alternate time base from the ATB pin, X_{en} should be tied to V_{SS}.

A_{in}
Analog Input (PDIP — Pin 7, SOG — Pin 8)

This pin accepts the analog input and is internally biased so that the input signal may be ac coupled. The input may be dc coupled so long as it does not exceed the positive supply (see Figure 2).

X_{in}/X_{out}
Oscillator In and Oscillator Out (PDIP — Pins 10, 9; SOG — Pins 11, 10)

These pins connect to an internal crystal oscillator. In operation, a parallel resonant crystal is connected from X_{in} to X_{out}, as well as a 1 MΩ resistor in parallel with the crystal. When using the alternate clock source from ATB, X_{in} should be tied to V_{DD}.

ATB
Alternate Time Base (PDIP — Pin 11, SOG — Pin 12)

This pin serves as a frequency reference when more than one MC145436A is used, so that only one crystal is required for multiple MC145436As. When doing so, all ATB pins should be tied together as shown in Figure 3. When only one MC145436A is used, this pin should be left unconnected. The output frequency of ATB is 447.4 kHz.

DV
Data Valid (PDIP — Pin 12, SOG — Pin 14)

DV signals a detection by going high after a valid tone pair is sensed and decoded at output pins D1, D2, D4, D8. DV remains high until a loss of the current DTMF signal occurs or until a transition in GT occurs.

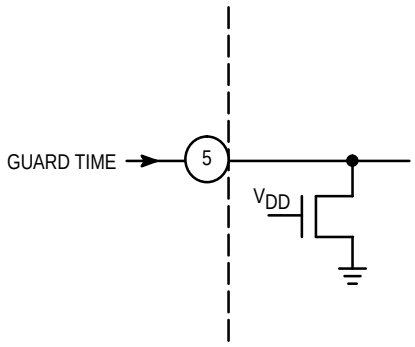


Figure 1. Guard Time

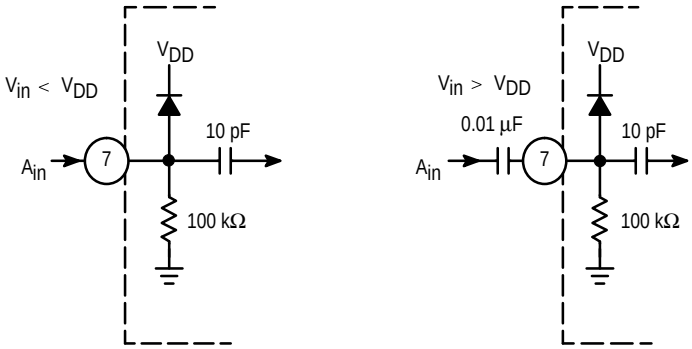


Figure 2. Analog Input (Operational Information Based on PDIP Package)

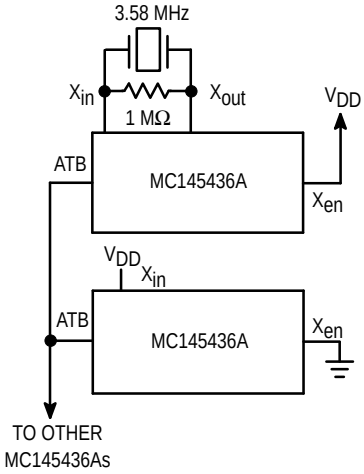


Figure 3. Multiple MC145436As

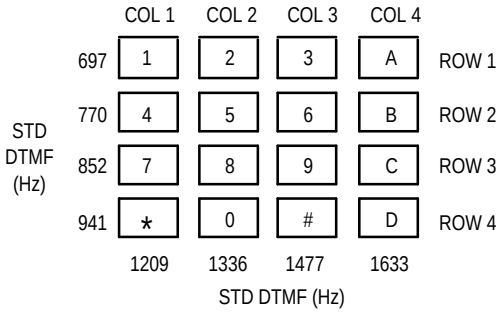
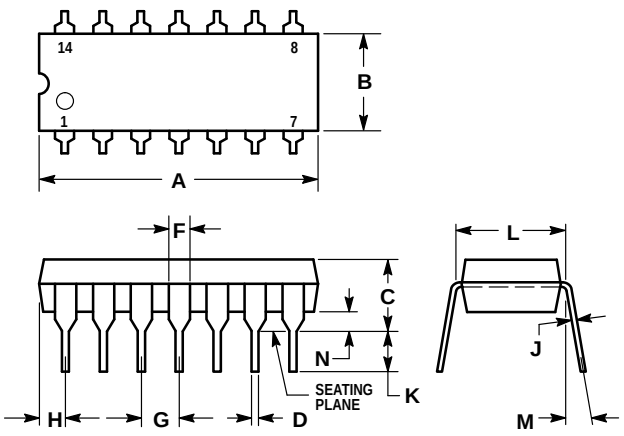


Figure 4. 4 × 4 Keyboard Matrix

PACKAGE DIMENSIONS

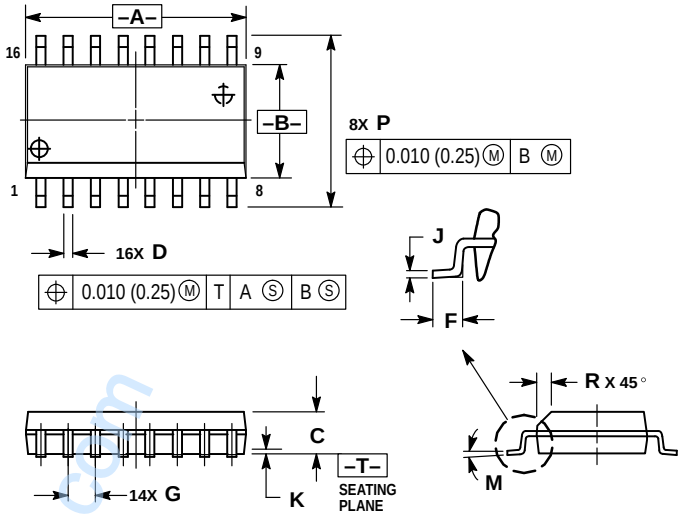
P SUFFIX
PLASTIC DIP
CASE 646–06



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

DW SUFFIX
SOG PACKAGE
CASE 751G–02



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

How to reach us:
USA/EUROPE: Motorola Literature Distribution;
P.O. Box 20912; Phoenix, Arizona 85036. 1–800–441–2447

MFAX: RMFAX0@email.sps.mot.com – TOUCHTONE (602) 244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, Toshikatsu Otsuki,
6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298