PMC-SIERRA

MSP for VoIP Gateways and Phones, Wired and Wireless

GENERAL

The MSP2015 belongs to a full family of Multi-Service Processors designed to meet the performance, QoS and security needs of communications equipment used within the customer premise. The MSP2015 is an ideal solution for VoIP Gateways and wireless IP Phones. As shown below, it includes a MIPS CPU, three 10/100 Ethernet MACs, TDM interface, and a PCI interface.

The MSP2015 provides a new level of price performance for VoIP Gateways and wireless IP phones. Because the MSP2015 eliminates the need for a separate processor, voice processing DSP, and multiple Ethernet MACs, systems can now be built with fewer chips at a very affordable price point.

The MSP2015 has a unique systems architecture that provides wire-speed performance. This architecture includes a powerful MIPS CPU, a 4.25 Gbps bus, 16KB Scratchpad, and intelligent context aware DMA engines. Together, this

results in an extremely cost effective VoIP solution. Integration of 802.11a, b, and g wireless LANs is easily facilitated through the PCI interface.

To reduce time-to-market, PMC-Sierra offers comprehensive support for the MSP2015, including evaluation boards, software, application engineering support, training, and documentation that together accelerate the product development process. In addition, the MSP2015 supports Linux, VxWorks, or custom operating systems.

FEATURES

The MSP2015 Multi-Service Processor offers the following advantages:

- Cost effective VoIP solutions
- Versatile PCI and ELB Buses
- Support for Global IP Sound technology
- 3 10/100 Ethernet MACs
- Flexible GPIo architecture to easily support keypad scan
- High performance systems architecture
- Significant cost reduction through integration of multiple processors and discrete parts on a single chip
- Architecture that scales to voice and data applications
- Easy porting of customer and third party software and protocol stacks

APPLICATIONS

- 1- and 2-port VoIP Gateway,
- Wired and Wireless
- IP Phones, Wired and Wireless
- TDM Ethernet Bridge

BLOCK DIAGRAM
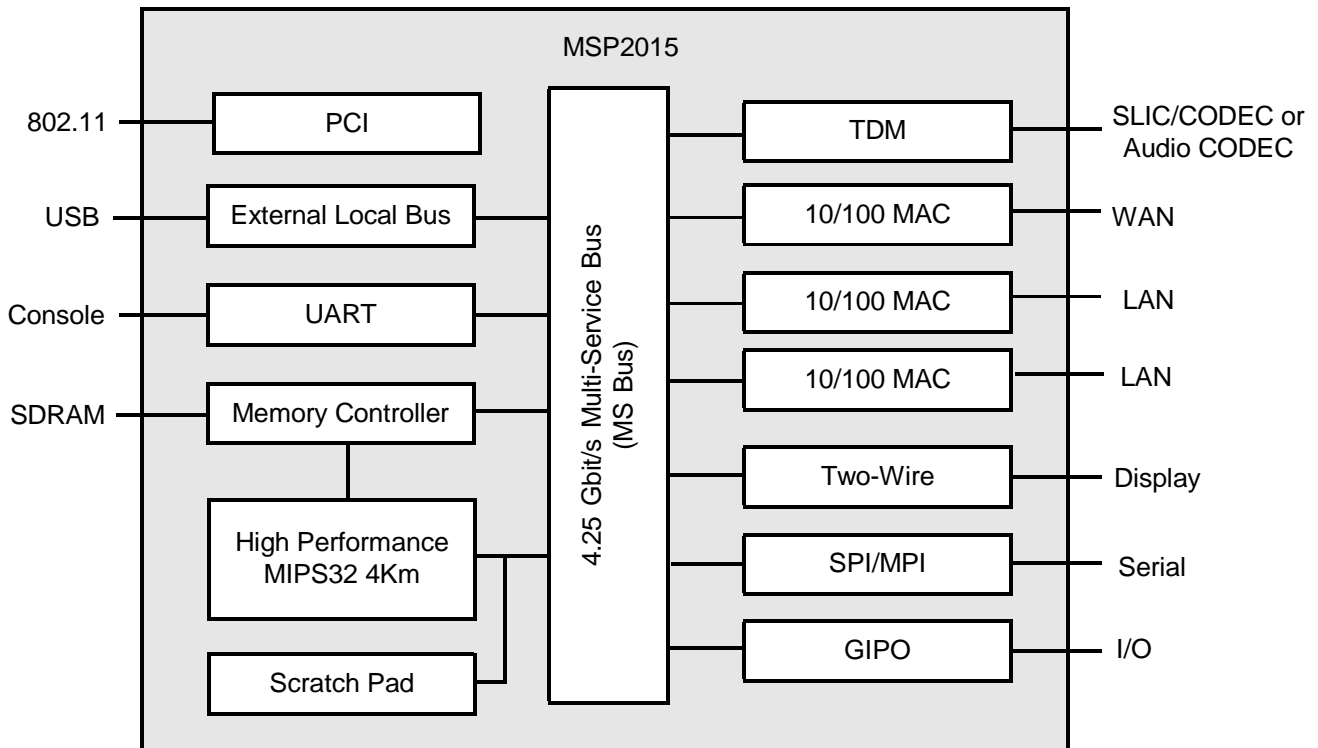
ELECTRICAL
- 276 pin PBGA
- Vcc 3.3V I/O, 1.8V core
- Power consumption 1.3W

SYSTEM PROCESSOR
- High performance MIPS32 4Km processor at:
  - 170 MHz - 1 ch VoIP GW
  - 200 MHz - 2 ch VoIP GW
- 16 KB instruction cache, 16 KB data cache
- 16 KB Scratchpad

ULTRAFAST MULTI-SERVICE BUS (MS BUS)
- Peak bandwidth of 4.25 Gbps
- True parallel processing

LAN INTERFACE
- 3 Independent 10/100 Ethernet MACs
  - MII/RMII
- Supports VLAN tagging

VOICE INTERFACE
- TDM Interface

HIGH PERFORMANCE SYSTEM BUSES
- PCI interface (32-bit, 33 MHz)
  - PCI V2.1 and V2.2 compatible
- Flexible external local bus interface
  - Up to 25 MBps data throughput

SYSTEM CONTROL
- Four interrupt inputs
- 55 GPIOs
- MIPS timer, 2 system timers, and watchdog timer
- Block copy engine

MISCELLANEOUS INTERFACES
- 2 UARTs
- SPI/MPI
- Two-wire serial

MEMORY CONTROLLER
- Glueless interface to 256 MB of SDRAM
- Glueless interface to 32 MB of flash

SOFTWARE
- APIs: MACs, VoIP, and Block Copy
- Board support package

DEVELOPMENT TOOLS
- Support for Linux and VxWorks
- Evaluation boards
- Third party tool chains

THIRD PARTY SUPPORT
- Voice Processing
  - GIPS - Global IP Sound - NetEq
  - RADVISION - H.323, SIP, MGCP
- EJTAG Debuggers
  - EPI - MAJIC probe
  - WindRiver - visionICE II

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