

Siliconix

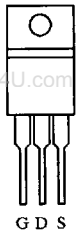
N-Channel Enhancement-Mode Transistor

175°C Maximum Junction Temperature

Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.014	60 ^a

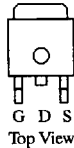
TO-220AB



Top View

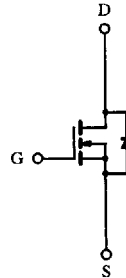
SUP60N06-14

TO-263



Top View

SUB60N06-14



N-Channel MOSFET

Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ($T_J = 175^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	60 ^a
		$T_C = 100^\circ\text{C}$	42
Pulsed Drain Current	I_{DM}	240	A
Avalanche Current	I_{AR}	60	
Repetitive Avalanche Energy ^b	E_{AR}	180	mJ
Power Dissipation	P_D	$T_C = 25^\circ\text{C}$ (TO-220AB and TO-263)	100
		$T_A = 25^\circ\text{C}$ (TO-263) ^c	3.7
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Junction-to-Ambient	R_{thJA}	PCB Mount (TO-263) ^c	40
		Free Air (TO-220AB)	80
Junction-to-Case	R_{thJC}	1.5	$^\circ\text{C/W}$

Notes:

- Package limited.
- Duty cycle $\leq 1\%$.
- When mounted on 1" square PCB (FR-4 material).

(05/16/94)

Advance Information

6-161

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Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_{DS} = 1\ \text{mA}$	2.0	3.0	4.0	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}$			25	μA
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			250	
		$V_{DS} = 48\text{ V}, V_{GS} = 0\text{ V}, T_J = 175^\circ\text{C}$			500	
On-State Drain Current ^b	$I_{D(on)}$	$V_{DS} = 5\text{ V}, V_{GS} = 10\text{ V}$	60			A
Drain-Source On-State Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$			0.014	Ω
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 125^\circ\text{C}$			0.023	
		$V_{GS} = 10\text{ V}, I_D = 30\text{ A}, T_J = 175^\circ\text{C}$			0.028	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		TBD		S
Dynamic^a						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		TBD		pF
Output Capacitance	C_{oss}			TBD		
Reversen Transfer Capacitance	C_{rss}			TBD		
Total Gate Charge ^c	Q_g	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 60\text{ A}$		TBD	130	nC
Gate-Source Charge ^c	Q_{gs}			TBD		
Gate-Drain Charge ^c	Q_{gd}			TBD		
Turn-On Delay Time ^c	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 0.47\ \Omega$ $I_D = 60\text{ A}, V_{GEN} = 10\text{ V}, R_G = 2.5\ \Omega$		TBD	30	ns
Rise Time ^c	t_r			TBD	180	
Turn-Off Delay Time ^c	$t_{d(off)}$			TBD	100	
Fall Time ^c	t_f			TBD	50	
Source-Drain Diode Ratings and Characteristics ($T_C = 25^\circ\text{C}$)^a						
Continuous Current	I_s				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage ^b	V_{SD}	$I_F = 60\text{ A}, V_{GS} = 0\text{ V}$			1.8	V
Reverse Recovery Time	t_{rr}	$I_F = 60\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		TBD		ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			TBD		A
Reverse Recovery Charge	Q_{rr}			TBD		μC

Notes:

- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- c. Independent of operating temperature.