

# HN27C101AP/AFP/ATT Series

## HN27C301AP/AFP Series

### 131072-word X 8-bit CMOS One Time Electrically Programmable ROM

The HN27C101AP/AFP/ATT series are 131072-word X 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C101AP/AFP/ATT, HN27C301AP /AFP series are in the "1" state (output high).

Data is introduced by selectively programming "0" into the desired bit location. This device is packaged in 32-pin plastic package, therefore, this device cannot be rewritten and erased.

The packages of the HN27C101ATT series are surface mount thin and small outline packages. They are suitable for hand-held equipment such as a memory card.

### Features

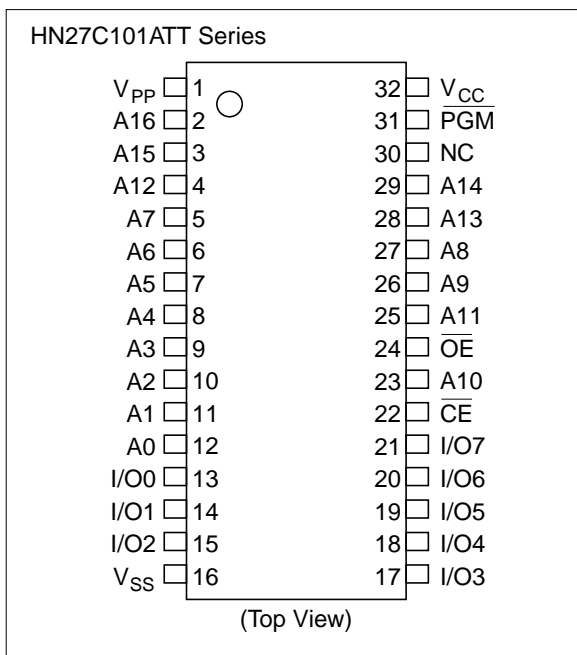
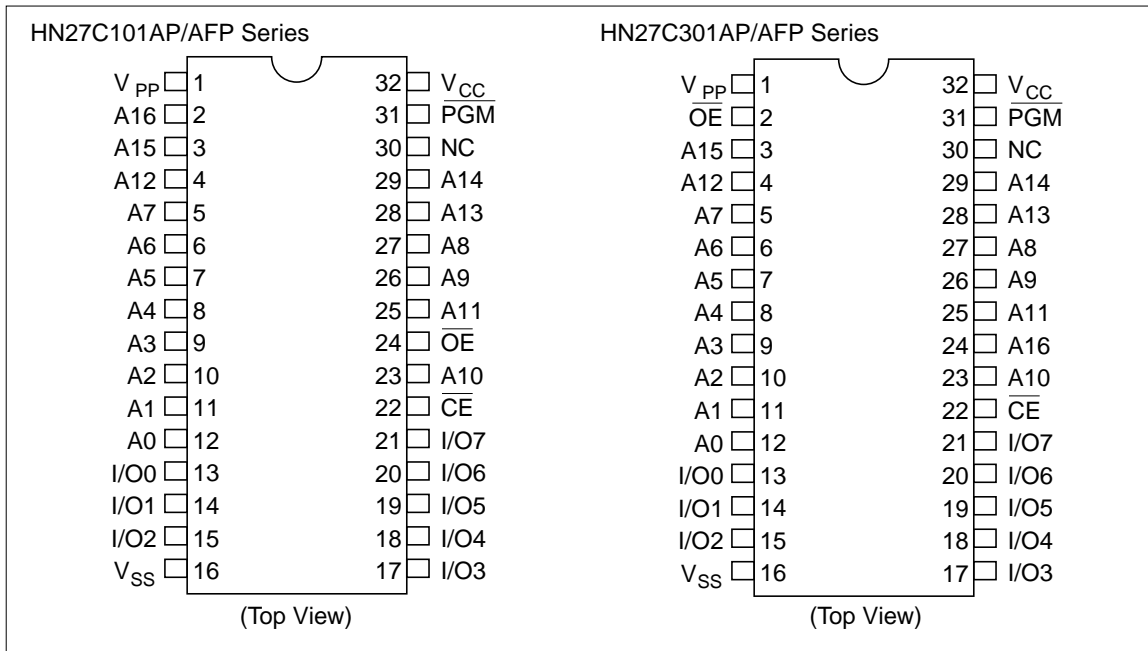
- Single power supply: +5 V  $\pm$  10%
- Fast high-reliability programming mode and fast high-reliability page programming mode
  - Programming voltage: +12.5 V DC
  - Fast high-reliability page programming: 14 sec typ
- High speed inputs and outputs TTL compatible during both read and program modes
- Low power dissipation: 50 mW/MHz typ (active)  
5  $\mu$ W typ (standby)
- Pin arrangement: 32-pin JEDEC standard except HN27C301A series replaceable 32 pin Mask ROM (HN27C301AP/AFP Series)
- Package
  - Surface mount thin and small outline package (TSOP) type II: HN27C101ATT series
- Device identifier mode: manufacturer code and device code
- Fully compatible with HN27C101P/FP, 301P/FP series

### Ordering Information

| Type No.       | Access time | Package                                     |
|----------------|-------------|---|
| HN27C101AP-12  | 120 ns      | 600-mil<br>32-pin<br>plastic DIP<br>(DP-32) |
| HN27C101AP-15  | 150 ns      |   |
| HN27C101AP-20  | 200 ns      |   |
| HN27C101AP-25  | 250 ns      |   |
| HN27C301AP-12  | 120 ns      |   |
| HN27C301AP-15  | 150 ns      |   |
| HN27C301AP-20  | 200 ns      |   |
| HN27C301AP-25  | 250 ns      |   |
| HN27C101AFP-12 | 120 ns      | 32-pin plastic<br>SOP<br>(FP-32D)           |
| HN27C101AFP-15 | 150 ns      |   |
| HN27C101AFP-20 | 200 ns      |   |
| HN27C101AFP-25 | 250 ns      |   |
| HN27C301AFP-12 | 120 ns      |   |
| HN27C301AFP-15 | 150 ns      |   |
| HN27C301AFP-20 | 200 ns      |   |
| HN27C301AFP-25 | 250 ns      |   |
| HN27C101ATT-12 | 120 ns      | 32-pin plastic<br>TSOP-(II)<br>(TTP-32D)    |
| HN27C101ATT-15 | 150ns       |   |

# HN27C101AP/AFP/ATT, HN27C301AP/AFP Series

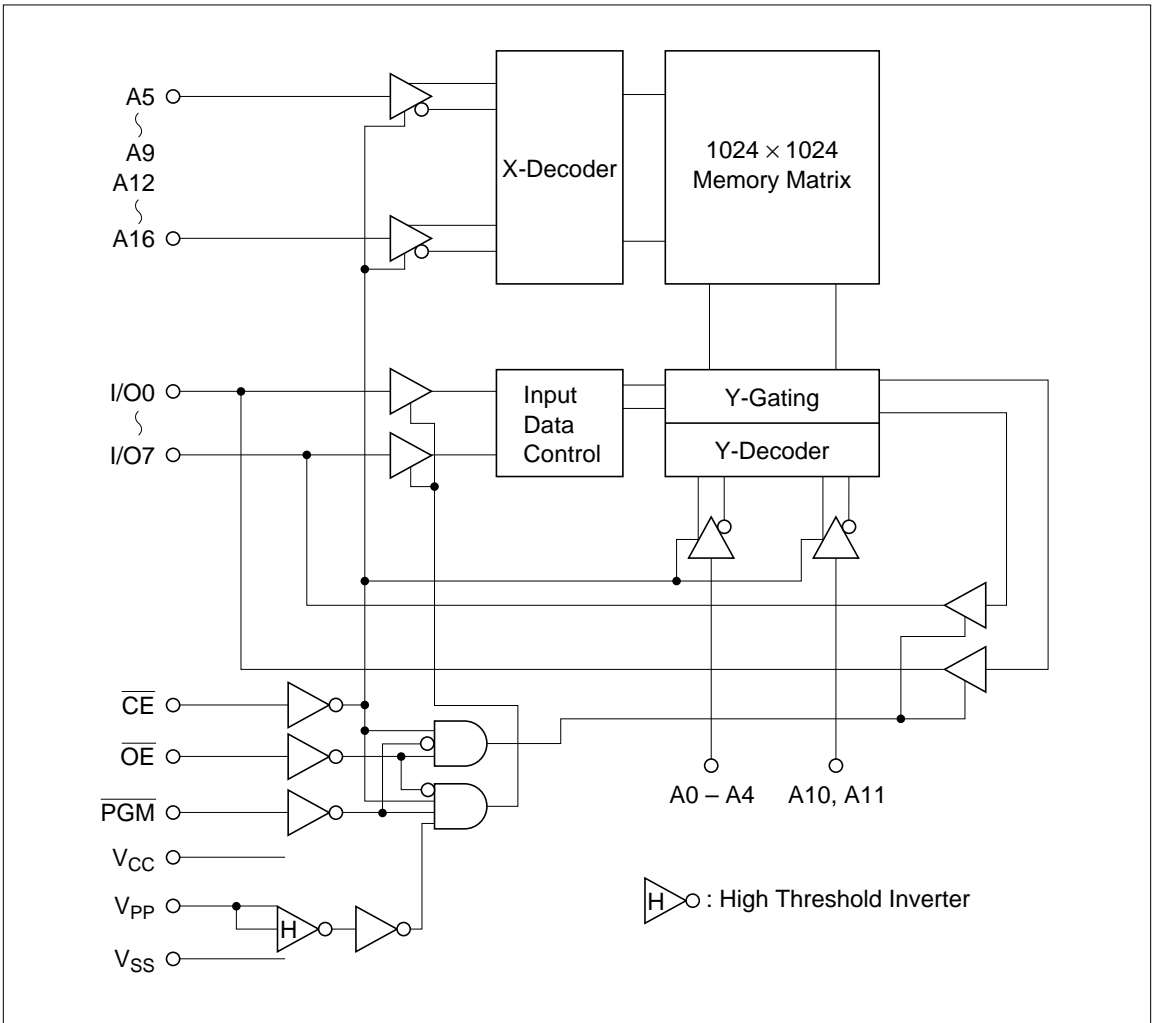
## Pin Arrangement



## Pin Description

| Pin name         | Function                 |
|------------------|--------------------------|
| A0 – A16         | Address                  |
| I/O0 – I/O7      | Input/output             |
| $\overline{CE}$  | Chip enable              |
| $\overline{OE}$  | Output enable            |
| $V_{CC}$         | Power supply             |
| $V_{PP}$         | Programming power supply |
| $V_{SS}$         | Ground                   |
| $\overline{PGM}$ | Programming enable       |
| NC               | No connection            |

Block Diagram



## HN27C101AP/AFP/ATT, HN27C301AP/AFP Series

### Mode Selection

| Mode            | $\overline{CE}$ | $\overline{OE}$ | $\overline{PGM}$ | A9             | V <sub>PP</sub> | V <sub>CC</sub> | I/O                |
|-----------------|-----------------|-----------------|------------------|----------------|-----------------|-----------------|--------------------|
| HN27C101A       | (22)            | (24)            | (31)             | (26)           | (1)             | (32)            | (13 – 15, 17 – 21) |
| HN27C301A       | (22)            | (2)             | (31)             | (26)           | (1)             | (32)            | (13 – 15, 17 – 21) |
| Read            | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub>  | X              | V <sub>CC</sub> | V <sub>CC</sub> | Dout               |
| Output disable  | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IH</sub>  | X              | V <sub>CC</sub> | V <sub>CC</sub> | High-Z             |
| Standby         | V <sub>IH</sub> | X               | X                | X              | V <sub>CC</sub> | V <sub>CC</sub> | High-Z             |
| Program         | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub>  | X              | V <sub>PP</sub> | V <sub>CC</sub> | Din                |
| Program verify  | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub>  | X              | V <sub>PP</sub> | V <sub>CC</sub> | Dout               |
| Page data latch | V <sub>IH</sub> | V <sub>IL</sub> | V <sub>IH</sub>  | X              | V <sub>PP</sub> | V <sub>CC</sub> | Din                |
| Page program    | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IL</sub>  | X              | V <sub>PP</sub> | V <sub>CC</sub> | High-Z             |
| Program inhibit | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IL</sub>  | X              | V <sub>PP</sub> | V <sub>CC</sub> | High-Z             |
|                 | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IH</sub>  |                |                 |                 |                    |
|                 | V <sub>IH</sub> | V <sub>IL</sub> | V <sub>IL</sub>  |                |                 |                 |                    |
|                 | V <sub>IH</sub> | V <sub>IH</sub> | V <sub>IH</sub>  |                |                 |                 |                    |
| Identifier      | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub>  | V <sub>H</sub> | V <sub>CC</sub> | V <sub>CC</sub> | Code               |

- Notes: 1. X: Don't care  
2. V<sub>H</sub>: 12.0 V ± 0.5 V

### Absolute Maximum Ratings

| Parameter                            | Symbol                             | Value           | Unit |
|--------------------------------------|------------------------------------|-----------------|------|
| A11 input and output voltages*1      | V <sub>in</sub> , V <sub>out</sub> | -0.6*2 to +7.0  | V    |
| A9 input voltage*1                   | V <sub>ID</sub>                    | -0.6*2 to +13.5 | V    |
| V <sub>PP</sub> voltage*1            | V <sub>PP</sub>                    | -0.6 to +13.5   | V    |
| V <sub>CC</sub> voltage*1            | V <sub>CC</sub>                    | -0.6 to +7.0    | V    |
| Operating temperature range          | T <sub>opr</sub>                   | 0 to +70        | °C   |
| Storage temperature range            | T <sub>stg</sub>                   | -55 to +125     | °C   |
| Storage temperature range under bias | T <sub>bias</sub>                  | -10 to +80      | °C   |

- Notes: 1. Relative to V<sub>SS</sub>  
2. V<sub>in</sub>, V<sub>out</sub> and V<sub>ID</sub> min = -1.0 V for pulse width ≤ 50 ns

## HN27C101AP/AFP/ATT, HN27C301AP/AFP Series

**Capacitance** ( $T_a = 25^\circ\text{C}$ ,  $f = 1\text{ MHz}$ )

| Parameter          | Symbol    | Min | Typ | Max | Unit | Test conditions        |
|--------------------|-----------|-----|-----|-----|------|------------------------|
| Input capacitance  | $C_{in}$  | —   | —   | 10  | pF   | $V_{in} = 0\text{ V}$  |
| Output capacitance | $C_{out}$ | —   | —   | 15  | pF   | $V_{out} = 0\text{ V}$ |

### Read Operation

**DC Characteristics** ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{PP} = V_{CC}$ ,  $T_a = 0\text{ to }+70^\circ\text{C}$ )

| Parameter                  | Symbol    | Min            | Typ | Max                 | Unit          | Test conditions                                    |
|----------------------------|-----------|----------------|-----|---------------------|---------------|--|
| Input leakage current      | $I_{LI}$  | —              | —   | 2                   | $\mu\text{A}$ | $V_{in} = 0\text{ V to }V_{CC}$                    |
| Output leakage current     | $I_{LO}$  | —              | —   | 2                   | $\mu\text{A}$ | $V_{out} = 0\text{ V to }V_{CC}$                   |
| $V_{PP}$ current           | $I_{PP1}$ | —              | 1   | 20                  | $\mu\text{A}$ | $V_{PP} = 5.5\text{ V}$                            |
| Standby $V_{CC}$ current   | $I_{SB1}$ | —              | —   | 1                   | mA            | $\overline{CE} = V_{IH}$                           |
|                            | $I_{SB2}$ | —              | 1   | 20                  | mA            | $\overline{CE} = V_{CC} \pm 0.3\text{ V}$          |
| Operating $V_{CC}$ current | $I_{CC1}$ | —              | —   | 30                  | mA            | $\overline{CE} = V_{IL}$ , $I_{out} = 0\text{ mA}$ |
|                            | $I_{CC2}$ | —              | —   | 30                  | mA            | $f = 5\text{ MHz}$ , $I_{out} = 0\text{ mA}$       |
|                            |           | —              | —   | 45                  | mA            | $f = 8.4\text{ MHz}$ , $I_{out} = 0\text{ mA}$     |
| Input low voltage          | $V_{IL}$  | $-0.3^{*1}$    | —   | 0.8                 | V             |  |
| Input high voltage         | $V_{IH}$  | 2.2            | —   | $V_{CC} + 1.0^{*2}$ | V             |  |
| Output low voltage         | $V_{OL}$  | —              | —   | 0.45                | V             | $I_{OL} = 2.1\text{ mA}$                           |
| Output high voltage        | $V_{OH}$  | 2.4            | —   | —                   | V             | $I_{OH} = -1\text{ mA}$                            |
|                            |           | $V_{CC} - 0.7$ | —   | —                   | V             | $I_{OH} = -0.1\text{ mA}$                          |

- Notes: 1.  $V_{IL}$  min =  $-1.0\text{ V}$  for pulse width  $\leq 50\text{ ns}$ .  
 2.  $V_{IH}$  max =  $V_{CC} + 1.5\text{ V}$  for pulse width  $\leq 20\text{ ns}$ .  
 If  $V_{IH}$  is over the specified maximum value, read operation cannot be guaranteed.

# HN27C101AP/AFP/ATT, HN27C301AP/AFP Series

AC Characteristics ( $V_{CC} = 5\text{ V} \pm 10\%$ ,  $V_{PP} = V_{CC}$ ,  $T_a = 0\text{ to }+70^\circ\text{C}$ )

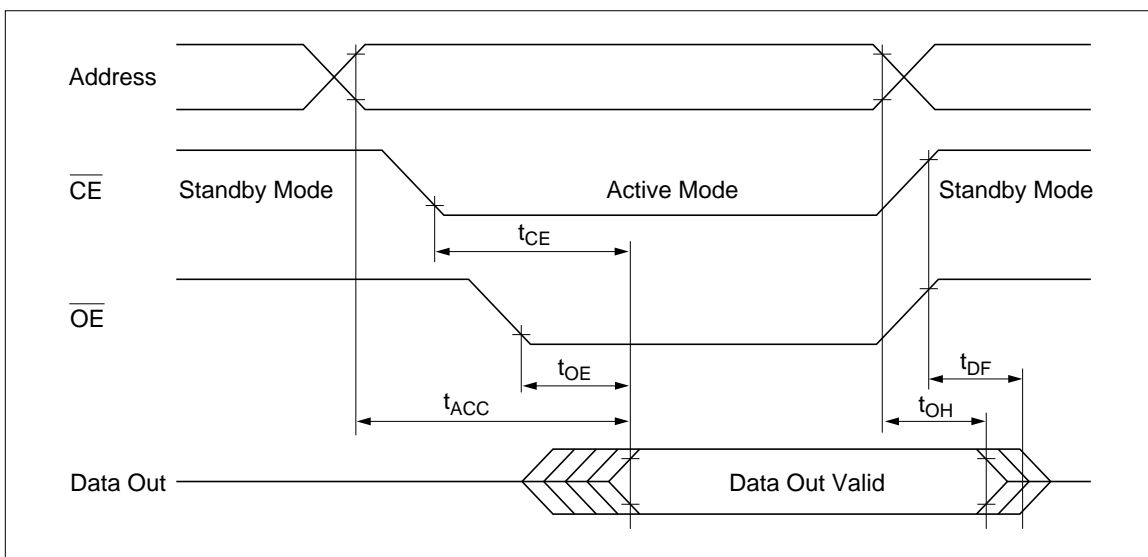
## Test condition

- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times:  $\leq 20\text{ ns}$
- Output load: 1 TTL Gate +100 pF
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V  
Outputs; 0.8 V and 2.0 V

| Parameter                            | Symbol    | HN27C101AP<br>/AFP/ATT<br>HN27C301AP/AFP |     |     |     | HN27C101AP/AFP<br>HN27C301AP/AFP |     |     |     | Unit | Test conditions                          |
|--------------------------------------|-----------|--|-----|-----|-----|----------------------------------|-----|-----|-----|------|--|
|                                      |           | -12                                      |     | -15 |     | -20                              |     | -25 |     |      |  |
|                                      |           | Min                                      | Max | Min | Max | Min                              | Max | Min | Max |      |  |
| Address to output delay              | $t_{ACC}$ | —  | 120 | —   | 150 | —                                | 200 | —   | 250 | ns   | $\overline{CE} = \overline{OE} = V_{IL}$ |
| $\overline{CE}$ to output delay      | $t_{CE}$  | —  | 120 | —   | 150 | —                                | 200 | —   | 250 | ns   | $\overline{OE} = V_{IL}$                 |
| $\overline{OE}$ to output delay      | $t_{OE}$  | —  | 60  | —   | 70  | —                                | 70  | —   | 100 | ns   | $\overline{CE} = V_{IL}$                 |
| $\overline{OE}$ high to output float | $t_{DF}$  | 0  | 50  | 0   | 50  | 0                                | 50  | 0   | 60  | ns   | $\overline{CE} = V_{IL}$                 |
| Address to output hold               | $t_{OH}$  | 0  | —   | 0   | —   | 0                                | —   | 0   | —   | ns   | $\overline{CE} = \overline{OE} = V_{IL}$ |

Note:  $t_{DF}$  is defined as the time at which the output achieves the open circuit condition and data is no longer driven.

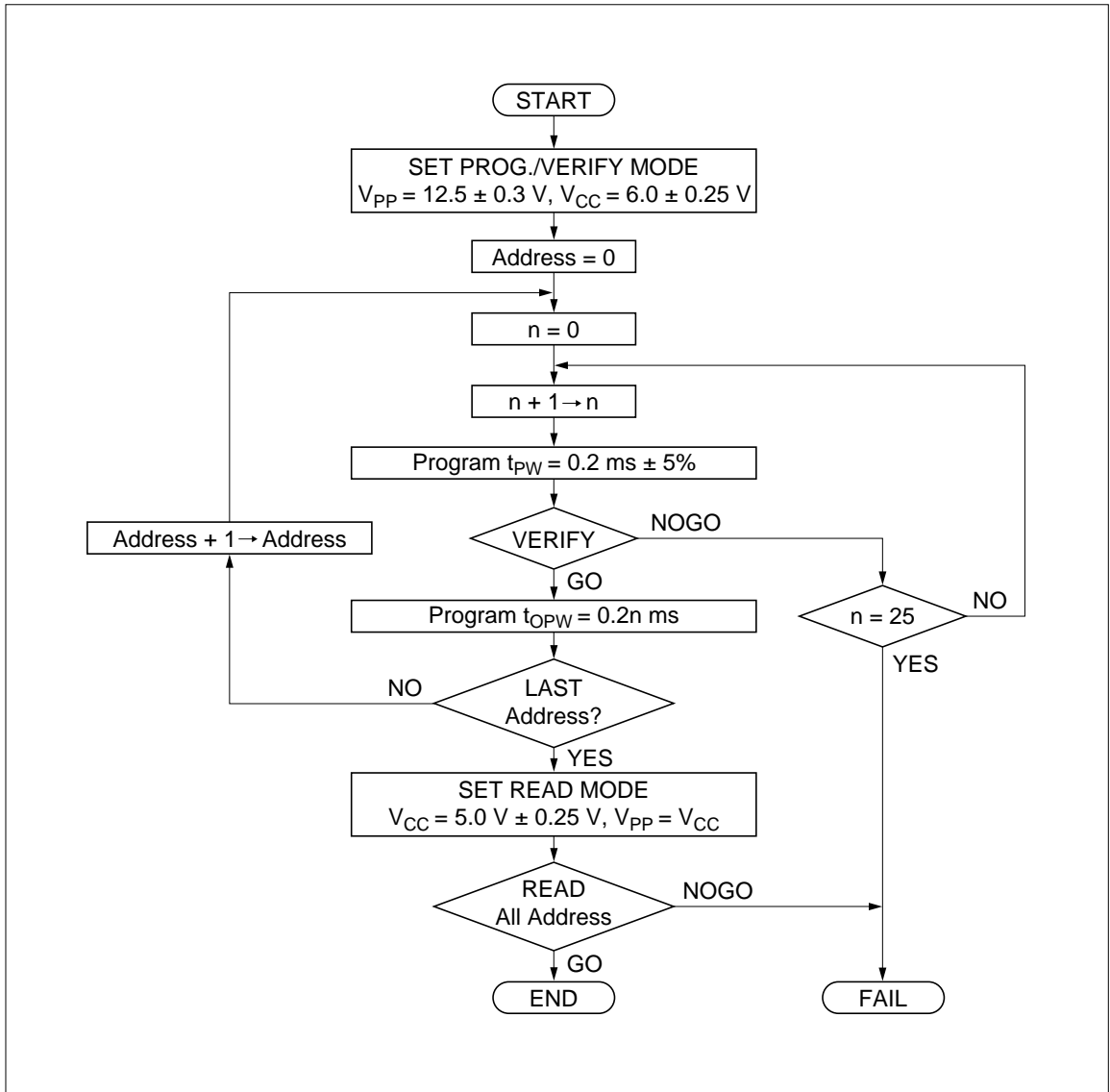
## Read Timing Waveform



## Fast High-Reliability Programming

This device can be applied the programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming

time without any voltage stress to the device nor deterioration in reliability of programmed data.



**Fast High-Reliability Programming Flowchart**

## HN27C101AP/AFP/ATT, HN27C301AP/AFP Series

DC Characteristics ( $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ ,  $V_{CC} = 6\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ )

| Parameter                         | Symbol   | Min         | Typ | Max                 | Unit          | Test conditions                           |
|-----------------------------------|----------|-------------|-----|---------------------|---------------|---|
| Input leakage current             | $I_{LI}$ | —           | —   | 2                   | $\mu\text{A}$ | $V_{in} = 0\text{ V to } V_{CC}$          |
| $V_{PP}$ supply current           | $I_{PP}$ | —           | —   | 40                  | $\text{mA}$   | $\overline{CE} = \overline{PGM} = V_{IL}$ |
| Operating $V_{CC}$ current        | $I_{CC}$ | —           | —   | 30                  | $\text{mA}$   |   |
| Input low level                   | $V_{IL}$ | $-0.1^{*5}$ | —   | 0.8                 | $\text{V}$    |   |
| Input high level                  | $V_{IH}$ | 2.2         | —   | $V_{CC} + 0.5^{*6}$ | $\text{V}$    |   |
| Output low voltage during verify  | $V_{OL}$ | —           | —   | 0.45                | $\text{V}$    | $I_{OL} = 2.1\text{ mA}$                  |
| Output high voltage during verify | $V_{OH}$ | 2.4         | —   | —                   | $\text{V}$    | $I_{OH} = -400\ \mu\text{A}$              |

- Notes:
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
  2.  $V_{PP}$  must not exceed 13.5 V including overshoot.
  3. An influence may be had upon device reliability if the device is installed or removed while  $V_{PP} = 12.5\text{ V}$ .
  4. Do not alter  $V_{PP}$  either  $V_{IL}$  to 12.5 V or 12.5 V to  $V_{IL}$  when  $\overline{CE} = \text{Low}$ .
  5.  $V_{IL}$  min =  $-0.6\text{ V}$  for pulse width  $\leq 20\text{ ns}$ .
  6. If  $V_{IH}$  is over the specified maximum value, programming operation cannot be guaranteed.



## HN27C101AP/AFP/ATT, HN27C301AP/AFP Series

**AC Characteristics** ( $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ ,  $V_{CC} = 6\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ )

### Test condition

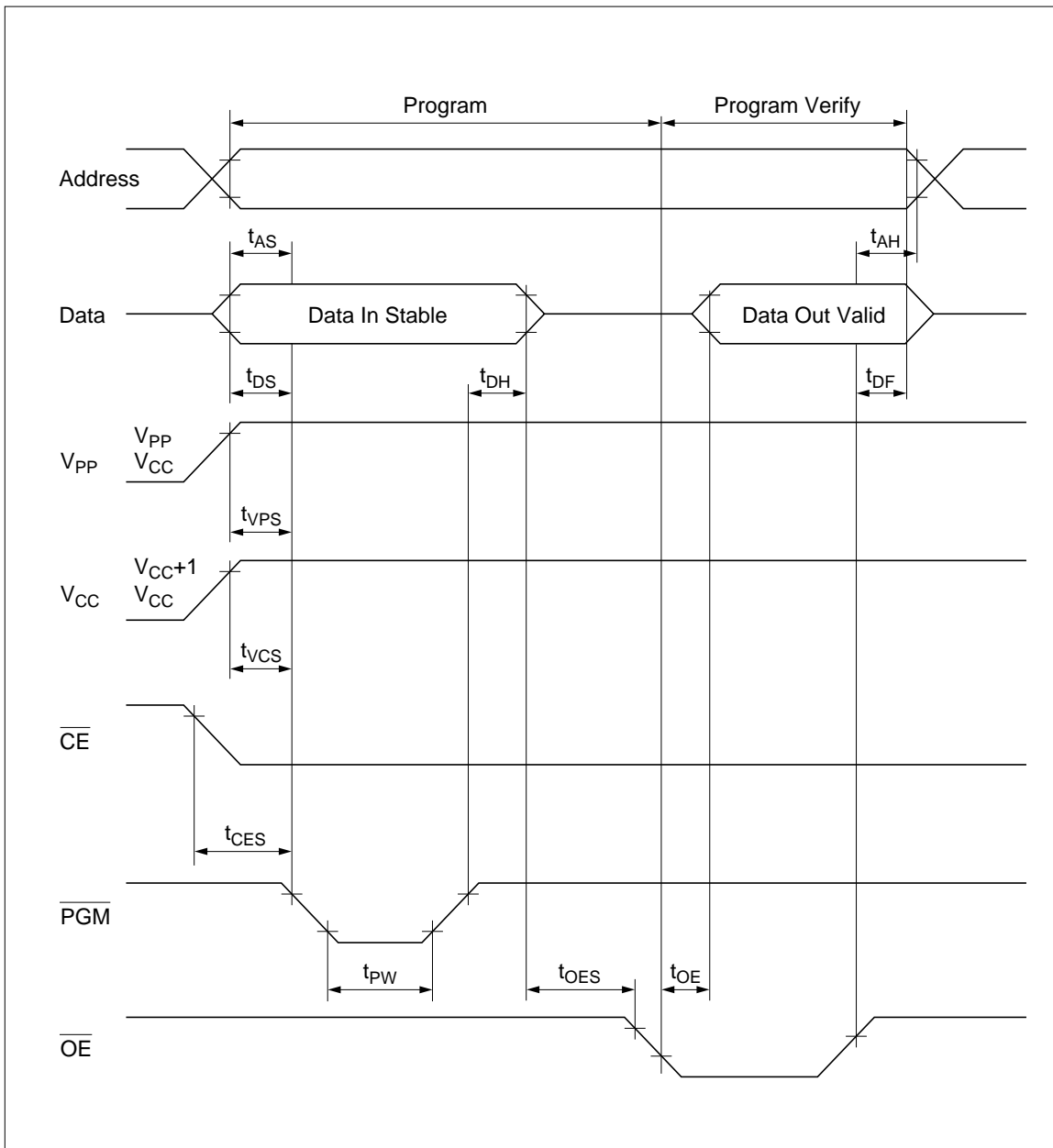
- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times:  $\leq 20\text{ ns}$
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V  
Outputs; 0.8 V and 2.0 V

| Parameter  | Symbol         | Min  | Typ | Max  | Unit          | Test conditions |
|--|----------------|------|-----|------|---------------|-----------------|
| Address setup time                               | $t_{AS}$       | 2    | —   | —    | $\mu\text{s}$ |                 |
| $\overline{OE}$ setup time                       | $t_{OES}$      | 2    | —   | —    | $\mu\text{s}$ |                 |
| Data setup time                                  | $t_{DS}$       | 2    | —   | —    | $\mu\text{s}$ |                 |
| Address hold time                                | $t_{AH}$       | 0    | —   | —    | $\mu\text{s}$ |                 |
| Data hold time                                   | $t_{DH}$       | 2    | —   | —    | $\mu\text{s}$ |                 |
| $\overline{OE}$ to output float delay            | $t_{DF}^{*1}$  | 0    | —   | 130  | ns            |                 |
| $V_{PP}$ setup time                              | $t_{VPS}$      | 2    | —   | —    | $\mu\text{s}$ |                 |
| $V_{CC}$ setup time                              | $t_{VCS}$      | 2    | —   | —    | $\mu\text{s}$ |                 |
| $\overline{PGM}$ initial programming pulse width | $t_{PW}$       | 0.19 | 0.2 | 0.21 | ms            |                 |
| $\overline{PGM}$ overprogramming pulse width     | $t_{OPW}^{*2}$ | 0.19 | —   | 5.25 | ms            |                 |
| $\overline{CE}$ setup time                       | $t_{CES}$      | 2    | —   | —    | $\mu\text{s}$ |                 |
| Data valid from $\overline{OE}$                  | $t_{OE}$       | 0    | —   | 150  | ns            |                 |

- Notes: 1.  $t_{DF}$  is defined as the time at which the output achieves the open circuit condition and data is no longer driven.  
2. Refer to the programming flowchart for  $t_{OPW}$ .

# HN27C101AP/AFP/ATT, HN27C301AP/AFP Series

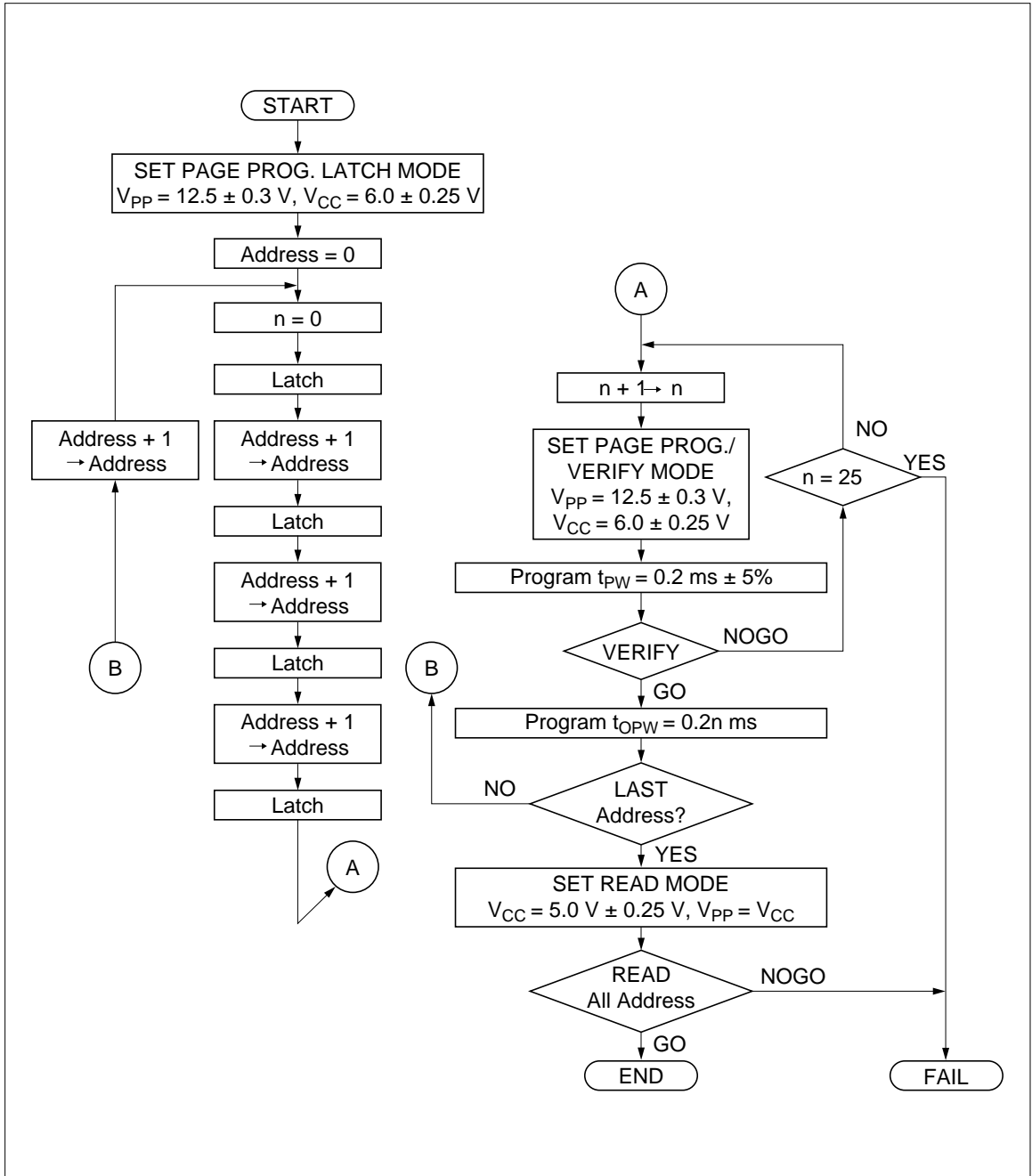
## Fast High-Reliability Programming Timing Waveform



## Fast High-Reliability Page Programming

This device can be applied the high performance page programming algorithm shown in following flowchart. This algorithm allows to obtain faster

programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



**Fast High-Reliability Page Programming Flowchart**

## HN27C101AP/AFP/ATT, HN27C301AP/AFP Series

DC Characteristics ( $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ ,  $V_{CC} = 6\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ )

| Parameter                         | Symbol   | Min         | Typ | Max                 | Unit          | Test conditions  |
|-----------------------------------|----------|-------------|-----|---------------------|---------------|--|
| Input leakage current             | $I_{LI}$ | —           | —   | 2                   | $\mu\text{A}$ | $V_{in} = 0\text{ V to } V_{CC}$                             |
| $V_{PP}$ supply current           | $I_{PP}$ | —           | —   | 50                  | $\text{mA}$   | $\overline{CE} = \overline{OE} = V_{IH}$ ,<br>$PGM = V_{IL}$ |
| Operating $V_{CC}$ current        | $I_{CC}$ | —           | —   | 30                  | $\text{mA}$   |  |
| Input low level                   | $V_{IL}$ | $-0.1^{*5}$ | —   | 0.8                 | $\text{V}$    |  |
| Input high level                  | $V_{IH}$ | 2.2         | —   | $V_{CC} + 0.5^{*6}$ | $\text{V}$    |  |
| Output low voltage during verify  | $V_{OL}$ | —           | —   | 0.45                | $\text{V}$    | $I_{OL} = 2.1\text{ mA}$                                     |
| Output high voltage during verify | $V_{OH}$ | 2.4         | —   | —                   | $\text{V}$    | $I_{OH} = -400\ \mu\text{A}$                                 |

- Notes:
1.  $V_{CC}$  must be applied simultaneously or before  $V_{PP}$  and removed simultaneously or after  $V_{PP}$ .
  2.  $V_{PP}$  must not exceed 13.5 V including overshoot.
  3. An influence may be had upon device reliability if the device is installed or removed while  $V_{PP} = 12.5\text{ V}$ .
  4. Do not alter  $V_{PP}$  either  $V_{IL}$  to 12.5 V or 12.5 V to  $V_{IL}$  when  $\overline{CE} = \text{Low}$ .
  5.  $V_{IL}$  min =  $-0.6\text{ V}$  for pulse width  $\leq 20\text{ ns}$
  6. If  $V_{IH}$  is over the specified maximum value, programming operation cannot be guaranteed.

## HN27C101AP/AFP/ATT, HN27C301AP/AFP Series

**AC Characteristics** ( $T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$ ,  $V_{CC} = 6\text{ V} \pm 0.25\text{ V}$ ,  $V_{PP} = 12.5\text{ V} \pm 0.3\text{ V}$ )

### Test condition

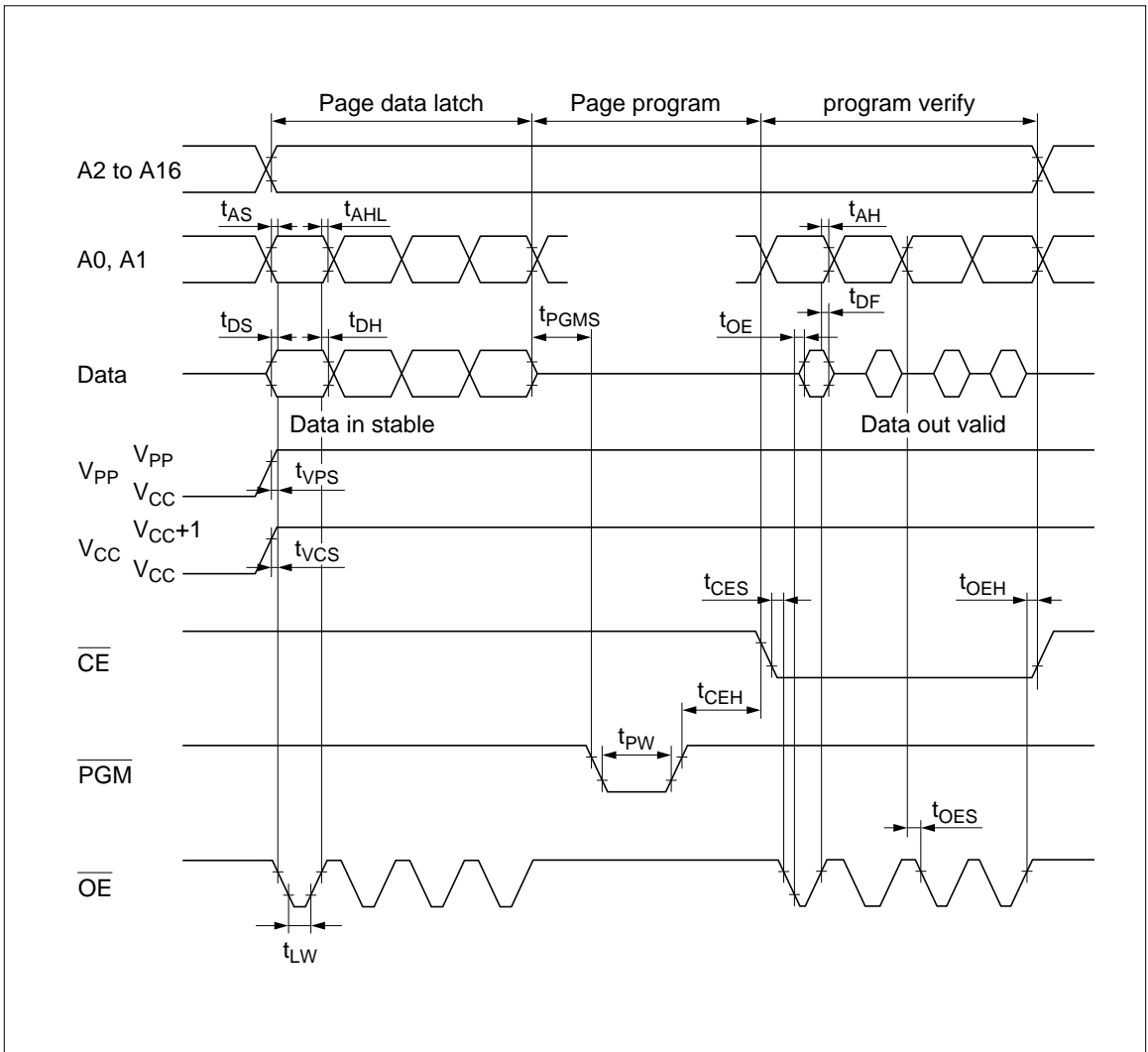
- Input pulse levels: 0.45 V to 2.4 V
- Input rise and fall times:  $\leq 20\text{ ns}$
- Reference levels for measuring timing: Inputs; 0.8 V and 2.0 V  
Outputs; 0.8 V and 2.0 V

| Parameter  | Symbol         | Min  | Typ | Max  | Unit          |
|--|----------------|------|-----|------|---------------|
| Address setup time                               | $t_{AS}$       | 2    | —   | —    | $\mu\text{s}$ |
| $\overline{OE}$ setup time                       | $t_{OES}$      | 2    | —   | —    | $\mu\text{s}$ |
| Data setup time                                  | $t_{DS}$       | 2    | —   | —    | $\mu\text{s}$ |
| Address hold time                                | $t_{AH}$       | 0    | —   | —    | $\mu\text{s}$ |
|  | $t_{AHL}$      | 2    | —   | —    | $\mu\text{s}$ |
| Data hold time                                   | $t_{DH}$       | 2    | —   | —    | $\mu\text{s}$ |
| $\overline{OE}$ to output float delay            | $t_{DF}^{*1}$  | 0    | —   | 130  | ns            |
| $V_{PP}$ setup time                              | $t_{VPS}$      | 2    | —   | —    | $\mu\text{s}$ |
| $V_{CC}$ setup time                              | $t_{VCS}$      | 2    | —   | —    | $\mu\text{s}$ |
| $\overline{PGM}$ initial programming pulse width | $t_{PW}$       | 0.19 | 0.2 | 0.21 | ms            |
| $\overline{PGM}$ overprogramming pulse width     | $t_{OPW}^{*2}$ | 0.19 | —   | 5.25 | ms            |
| $\overline{CE}$ setup time                       | $t_{CES}$      | 2    | —   | —    | $\mu\text{s}$ |
| Data valid from $\overline{OE}$                  | $t_{OE}$       | 0    | —   | 150  | ns            |
| $\overline{OE}$ pulse width during data latch    | $t_{LW}$       | 1    | —   | —    | $\mu\text{s}$ |
| $\overline{PGM}$ setup time                      | $t_{PGMS}$     | 2    | —   | —    | $\mu\text{s}$ |
| $\overline{CE}$ hold time                        | $t_{CEH}$      | 2    | —   | —    | $\mu\text{s}$ |
| $\overline{OE}$ hold time                        | $t_{OEH}$      | 2    | —   | —    | $\mu\text{s}$ |

- Notes: 1.  $t_{DF}$  is defined as the time at which the output achieves the open circuit condition and data is no longer driven.  
2. Refer to the programming flowchart for  $t_{OPW}$ .

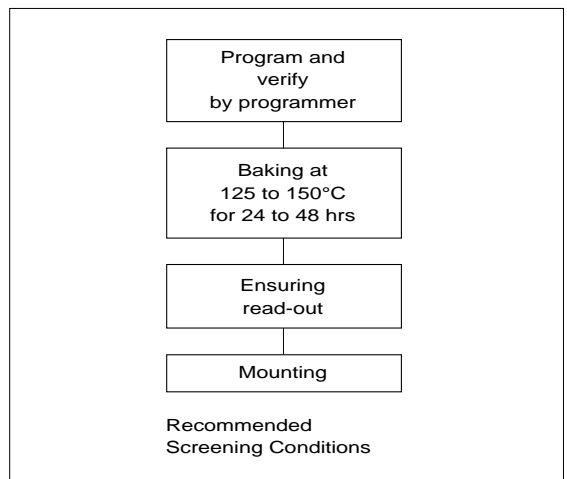
# HN27C101AP/AFP/ATT, HN27C301AP/AFP Series

## Fast High-Reliability Page Programming Timing Waveform



### Recommended Screening Conditions

Before mounting, please make the screening (baking without bias) shown in the right.



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## HN27C101AP/AFP/ATT, HN27C301AP/AFP Series

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### Mode Description

#### Device Identifier Mode

The device identifier mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of OTPROM. By this

mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

#### HN27C101AP/AFP/ATT Identifier Code

| Identifier        | A0<br>(12)      | A9<br>(26)     | I/O7<br>(21) | I/O6<br>(20) | I/O5<br>(19) | I/O4<br>(18) | I/O3<br>(17) | I/O2<br>(15) | I/O1<br>(14) | I/O0<br>(13) | Hex<br>Data |
|-------------------|-----------------|----------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|-------------|
| Manufacturer code | V <sub>IL</sub> | V <sub>H</sub> | 0            | 0            | 0            | 0            | 0            | 1            | 1            | 1            | 07          |
| Device code       | V <sub>IH</sub> | V <sub>H</sub> | 0            | 0            | 1            | 1            | 1            | 0            | 0            | 0            | 38          |

#### HN27C301AP/AFP Identifier Code

| Identifier        | A0<br>(12)      | A9<br>(26)     | I/O7<br>(21) | I/O6<br>(20) | I/O5<br>(19) | I/O4<br>(18) | I/O3<br>(17) | I/O2<br>(15) | I/O1<br>(14) | I/O0<br>(13) | Hex<br>Data |
|-------------------|-----------------|----------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|-------------|
| Manufacturer code | V <sub>IL</sub> | V <sub>H</sub> | 0            | 0            | 0            | 0            | 0            | 1            | 1            | 1            | 07          |
| Device code       | V <sub>IH</sub> | V <sub>H</sub> | 1            | 0            | 1            | 1            | 1            | 0            | 0            | 1            | B9          |

- Notes: 1.  $V_H = 12.0\text{ V} \pm 0.5\text{ V}$   
2. A1 – A8, A10 – A16,  $\overline{\text{CE}}$ ,  $\overline{\text{OE}} = V_{IL}$ ,  $\overline{\text{PGM}} = V_{IH}$

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