

ZABG6002
LOW POWER 6 STAGE FET LNA AND MIXER BIAS CONTROLLER

Summary

The ZABG6002 is a programmable low power depletion mode FET bias and mixer controller intended primarily for satellite Low Noise Blocks (LNBs). Designed to provide system flexibility the ZABG6002 can be programmed to bias six low noise amplifier (LNA) stages or four LNA and two active mixer stages, allowing the ZABG6002 to be used in several system designs. Combining advanced IC process and packaging techniques, the ZABG6002 operates with minimal current over a wide supply voltage. The small package and reduced component count minimizes the PCB area whilst enhancing overall LNB reliability.

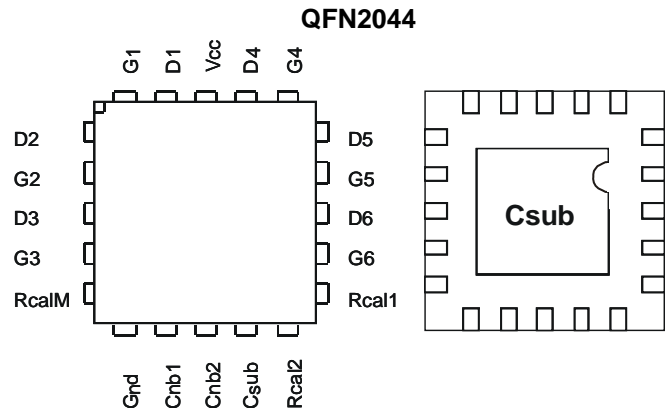
Features

- Six stage FET bias controller, two configurable as mixer stages
- Operating range of 3.0V to 8.0V
- Amplifier FET drain voltages set at 2.0V, mixer drain voltage set at 0.25V
- Amplifier FET drain current selectable from 0 to 15mA, mixer current from 0 to 7.5mA
- Switchable FET's for power management
- FET drain voltages and currents held stable over temperature and V_{CC} variations
- FETs protected against overstress during power-up and power-down.
- Internal negative supply generator allowing single supply operation (available for external use)
- Low quiescent supply current, 1.6mA typical
- Low external component count

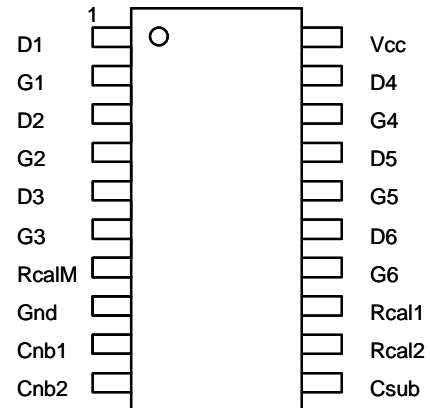
Applications

- Twin LNB's
- Quad LNB's
- US LNB's
- Microwave links
- PMR and Cellular telephone systems

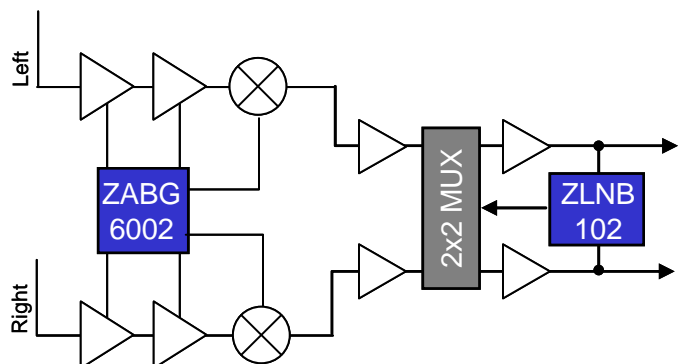
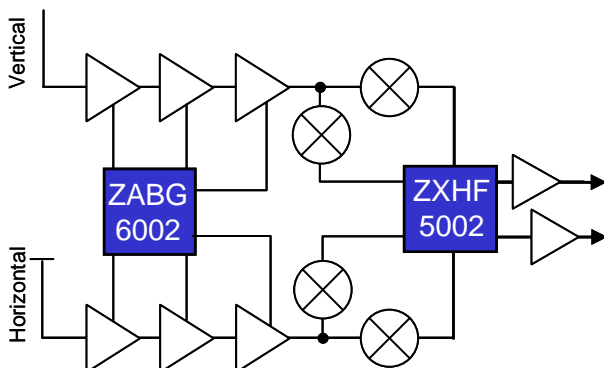
Pin Assignments



QSOP20



Twin LNB System Diagrams



Device Description

The ZABG series of devices are designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBS with a minimum of external components whilst operating from a minimal voltage supply and using minimal current.

The ZABG6002 has six FET bias stages that can be user programmed to provide either a two plus four arrangement of amplifier FET stages or a two plus two arrangement of amplifier FET stages along with two active mixer FET stages. Programming of the FET bias stage arrangement and the operating currents of each FET group is achieved by resistors connected to the Rcal1, Rcal2 and RcalM pins, allowing input FETs to be biased for optimum noise, amplifier FETs for optimum gain and mixer FETs (if used) for optimum conversion gain. Amplifier FETs can be operated at currents in the range 0 to 15mA and mixer FETs in the range 0.5 to 7.5mA.

Drain voltages of amplifier stages are set at 2.0V and mixer stages at 0.3V. The drain supplies are current limited to approximately 5% above the operating currents set by their associated Rcal resistors.

As an additional feature the Rcal pins can also be used as logic inputs to disable pairs of FETs as part of a power management scheme or simply an alternative to LNA switching. Driven to a logic high (>3.0V), the inputs disable their associated FET bias stages by switching gate feeds to -2.5V and drain feeds open circuit.

Depletion mode FETs require a negative voltage bias supply when operated in grounded source circuits. The ZABG6002 includes an integrated low noise switched capacitor DC-DC converter generating a regulated output of -2.5V to allow single supply operation. To aid efficiency and 3.3V systems the ZABG6002 has been design to used with supply rails of 3.3V to 8V

It is possible to use less than the devices full complement of FET bias controls, unused drain and gate connections can be left open circuit without affecting operation of the remaining bias circuits.

To protect the external FETs the circuits have been designed to ensure that, under any conditions including power up/down transients, the gate drive from the bias circuits cannot exceed -3V. Additionally each stage has its own individual current limiter. Furthermore if the negative rail experiences a fault condition, such as overload or short circuit, the drain supply to the FETs will shut down avoiding excessive current flow.

The ZABG6002 is available in the 20 pin 4mm x 4mm QFN or QSOP20 package.

Device operating temperature is -40°C to 85°C to suit a wide range of environmental conditions.

Maximum Ratings

| Parameter | Rating | Unit |
|-----------------------------|-------------|------|
| Supply Voltage | -0.6 to +10 | V |
| Supply Current | 100 | mA |
| Power Dissipation | 600 | mW |
| Operating Temperature Range | -40 to +85 | °C |
| Storage Temperature Range | -40 to 150 | °C |

Electrical Characteristics Measured at $T_{AMB} = 25^{\circ}\text{C}$, $V_{CC} = 3.3\text{V}$ (Note 1), $R_{CAL1} = R_{CAL2} = 36\text{K}$ (setting $I_{D1/2/4/5}$ to 10mA), $R_{CALM} = 68\text{K}$ (setting $I_{D3/6}$ to 5mA) unless otherwise stated

| Parameter | Conditions | Symbol | Min. | Typ. | Max. | Unit |
|-------------------------|--|---------------|------|-------|------|------|
| Operating Voltage Range | | V_{CC} | 3.0 | | 8.0 | V |
| Supply Current | $I_{D1-6} = 0$ | I_{CC} | | 1.6 | 4.0 | mA |
| | $I_{D1-6} = 10\text{mA}$, no R_{CALM} | $I_{CC(L)}$ | | 62 | 64 | mA |
| Substrate Voltage | $I_{CSUB} = 0$ | V_{CSUB} | -3.0 | -2.65 | -2.0 | V |
| | $I_{CSUB} = -200\mu\text{A}$ | $V_{CSUB(L)}$ | | -2.55 | -2.0 | V |
| Oscillator Frequency | | F_{OSC} | 150 | 260 | 600 | kHz |

Gate Characteristics

Gate (G1 to G6, resistor R_{CALM} not present)

| | | | | | | |
|---------------------------------|---|--------------|------|------|------|---------------|
| Current Range | | I_G | -100 | | +500 | μA |
| Voltage Low | $I_D = 12\text{mA}$, $I_G = -10\mu\text{A}$ | $V_{G(L)}$ | -3.0 | -2.5 | -2.0 | V |
| Voltage High | $I_D = 8\text{mA}$, $I_G = 0$ | $V_{G(H)}$ | 0 | 0.7 | 1.0 | V |
| Voltage Disabled ^(*) | $I_D = 0$, $I_G = -10\mu\text{A}$, $V_{RCAL1-2} = 3.0\text{V}$ | $V_{G(DIS)}$ | -3.0 | -2.5 | -2.0 | V |

Gate (G3 and G6, resistor R_{CALM} present)

| | | | | | | |
|---------------------------------|---|--------------|------|------|------|---------------|
| Current Range | | I_G | -100 | | +500 | μA |
| Voltage Low | $I_D = 6\text{mA}$, $I_G = -10\mu\text{A}$ | $V_{G(L)}$ | -3.0 | -2.5 | -2.0 | V |
| Voltage High | $I_D = 4\text{mA}$, $I_G = 0$ | $V_{G(H)}$ | 0 | 0.7 | 1.0 | V |
| Voltage Disabled ^(*) | $I_D = 0$, $I_G = -10\mu\text{A}$, $V_{RCAL2} = V_{RCALM} 3.0\text{V}$ | $V_{G(DIS)}$ | -3.0 | -2.5 | -2.0 | V |

Drain Characteristics

Drain (D1 to D6, resistor R_{CALM} not present)

| | | | | | | |
|---------------------------------|--------------------------------------|--------------|-----|-----|-----|---------------|
| Current Range | | I_D | 0 | | 15 | mA |
| Current Operating | Standard Application Circuit | $I_{D(OP)}$ | 8 | 10 | 12 | mA |
| Current Disabled ^(*) | $V_D = 0$, $V_{RCAL} = 3.0\text{V}$ | $I_{D(DIS)}$ | | | 10 | μA |
| Voltage Operating | $I_D = 10\text{mA}$ | $V_{D(OP)}$ | 1.8 | 2.0 | 2.2 | V |

Electrical Characteristics (Cont.) Measured at $T_{AMB} = 25^{\circ}\text{C}$, $V_{CC} = 3.3\text{V}$ (Note 1), $R_{CAL1} = R_{CAL2} = 36\text{K}$ (setting $I_{D1/2/4/5}$ to 10mA), $R_{CALM} = 68\text{K}$ (setting $I_{D3/6}$ to 5mA) unless otherwise stated

| Parameter | Conditions | Symbol | Min. | Typ. | Max. | Unit |
|--|---|---------------|------|------|------|------|
| Drain Characteristics | | | | | | |
| Drain (D3 and D6, resistor R_{CALM} present) | | | | | | |
| Current Range | | I_{DM} | 0.5 | | 7.5 | mA |
| Current Operating | Standard Application Circuit | $I_{DM(OP)}$ | 4 | 5 | 6 | mA |
| Current Disabled ^(*) | $V_D = 0$, $V_{RCAL} = 3.0\text{V}$, R_{CALM} not present | $I_{DM(DIS)}$ | | | 10 | uA |
| Voltage Operating | $I_D = 5\text{mA}$ | $V_{DM(OP)}$ | 0.25 | 0.3 | 0.35 | V |

| $R_{CAL}(1 \text{ and } 2)$ | | | | | | |
|---|--------------------------|-----------------|-----|-----|-----|----|
| Disable Threshold ^(*) | | $V_{RCAL(DIS)}$ | 1.8 | 2.7 | 3.0 | V |
| Input Current | $V_{RCAL} = 3.0\text{V}$ | $I_{RCAL(DIS)}$ | | 1.7 | 10 | uA |

| R_{CALM} | | | | | | |
|----------------------------------|--|-----------------|------|------|------|----------|
| Disable Threshold ^(*) | | $R_{CALM(DIS)}$ | 1.5M | 3.3M | 5.0M | Ω |
| R_{CALM} Range | | R_{CALM} | 39k | | 390k | Ω |

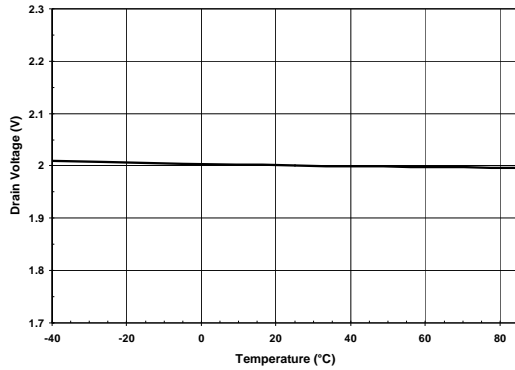
| Voltage and Temperature dependence (R_{CALM} not present) | | | | | | |
|---|---|----------------|--|------|--|--------|
| ΔI_D vs V_{CC} | $V_{CC} = 3.3$ to 8.0V | dI_D/dV_{CC} | | 1.2 | | %/V |
| ΔI_D vs T_{OP} | $T_{OP} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | dI_D/dT_{OP} | | 0.05 | | %/°C |
| ΔV_D vs V_{CC} | $V_{CC} = 3.3$ to 8.0V | dV_D/dV_{CC} | | 0.05 | | %/V |
| ΔV_D vs T_{OP} | $T_{OP} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ | dV_D/dT_{OP} | | 50 | | ppm/°C |

| Output Noise | | | | | | |
|---------------------|---|----------------|--|--|-------|--------|
| Drain Voltage | $C_{GATE-GND} = 10\text{nF}$, $C_{DRAIN-GND} = 10\text{nF}$ | $V_{D(NOISE)}$ | | | 0.02 | Vpk-pk |
| Gate Voltage | $C_{GATE-GND} = 10\text{nF}$, $C_{DRAIN-GND} = 10\text{nF}$ | $V_{G(NOISE)}$ | | | 0.005 | Vpk-pk |

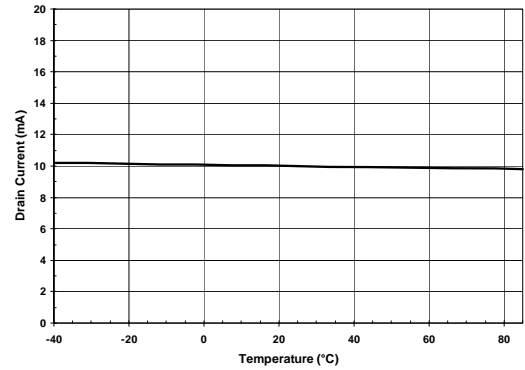
- Notes:
- To disable FET stages 3 and 6, pin R_{CAL2} must be set to 3V or above and pin R_{CALM} should be open circuit. See applications section for further information.
 - The characteristics are measured using up to three external reference resistors, R_{CAL1} , R_{CAL2} and R_{CALM} , wired from pins $R_{CAL1/2/M}$ to ground. Resistor R_{CAL1} sets the drain current of FETs 1 and 4. If R_{CALM} is not present, resistor R_{CAL2} sets the drain currents of FETs 2, 3, 5 and 6. If R_{CALM} is present, resistor R_{CAL2} sets the drain currents of FETs 2 and 5 and R_{CALM} sets the drain currents of FETs 3 and 6.
 - The negative bias voltages are generated on-chip using an internal oscillator. Two external capacitors, C_{NB} and C_{SUB} of value 47nF are required for this purpose.
 - The QFN2044 exposed pad must either be connected to C_{SUB} or left open circuit.
 - Noise voltage measurements are made with FETs and gate and drain capacitors of value 10nF in place. Noise voltages are not measured in production.
 - ESD sensitive, handling precautions are recommended.

Typical Characteristics Measured at $T_{AMB} = 25^{\circ}C$, $V_{CC} = 3.3V$, $R_{CAL1} = R_{CAL2} = 36K$ (setting I_D to 10mA), $R_{CALM} = 68K$ (setting $I_{D3/6}$ to 5mA) unless otherwise stated

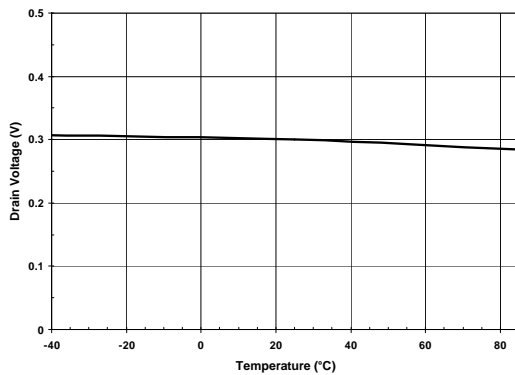
ZABG6002 Drain Voltage (D1 - D6) vs Temperature



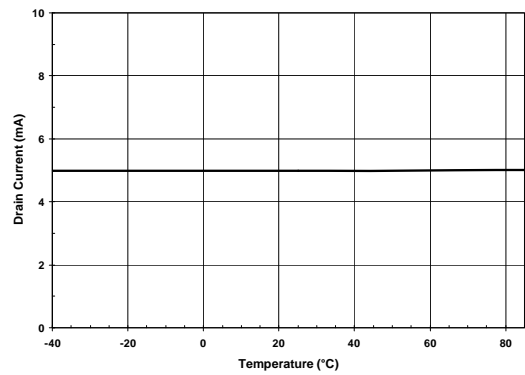
ZABG6002 Drain Current (D1 - D6) vs Temperature



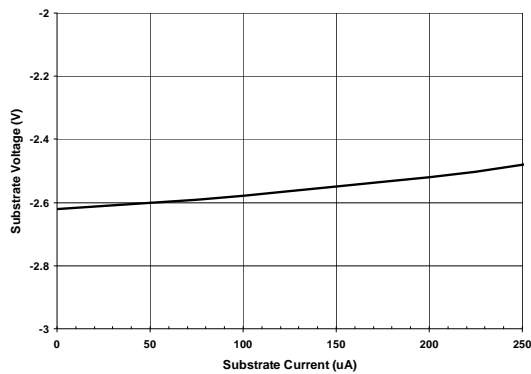
ZABG6002 Drain Voltage (D3 & D6 only) vs Temperature



ZABG6002 Drain Current (D3 & D6 only) vs Temperature

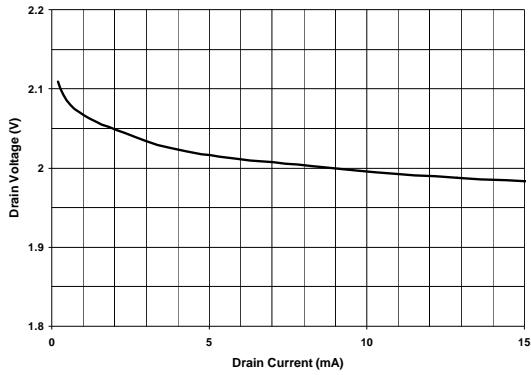


ZABG6002 Substrate Voltage vs Substrate Current

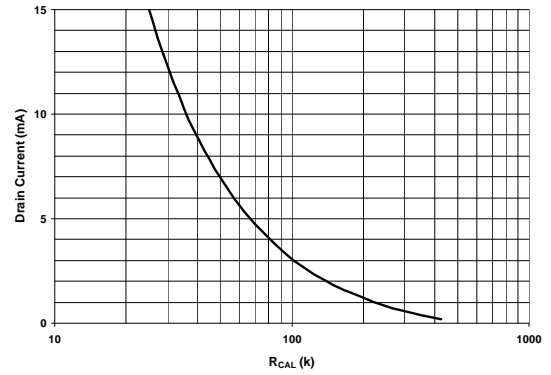


Typical Characteristics (Cont.) Measured at $T_{AMB} = 25^{\circ}C$, $V_{CC} = 3.3V$, $R_{CAL1} = R_{CAL2} = 36K$ (setting I_D to 10mA), $R_{CALM} = 68K$ (setting $I_{D3/6}$ to 5mA) unless otherwise stated

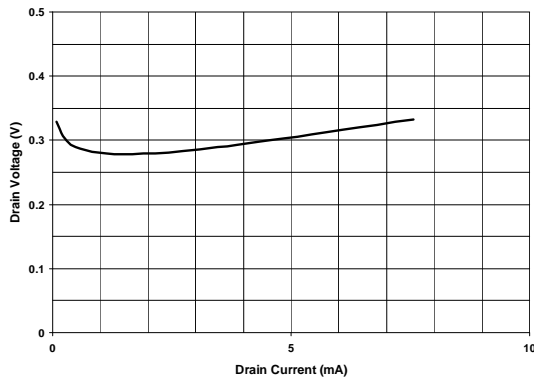
ZABG6002 Drain Voltage vs Drain Current (D1-D6)



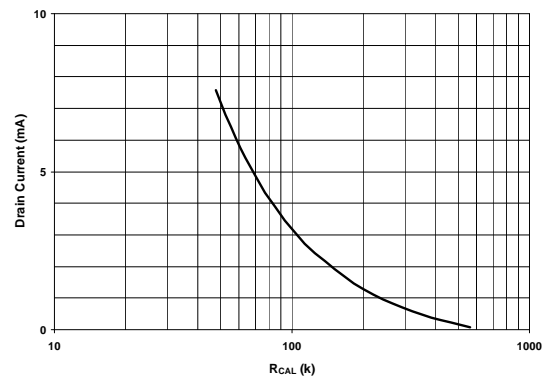
ZABG6002 Drain Current vs R_{CAL}



ZABG6002 Drain Voltage vs Drain Current (D3 & D6 only)



ZABG6002 Drain Current vs R_{CALM}



Application Information

The ZABG6002 is a flexible device and can be set up in a number of ways.

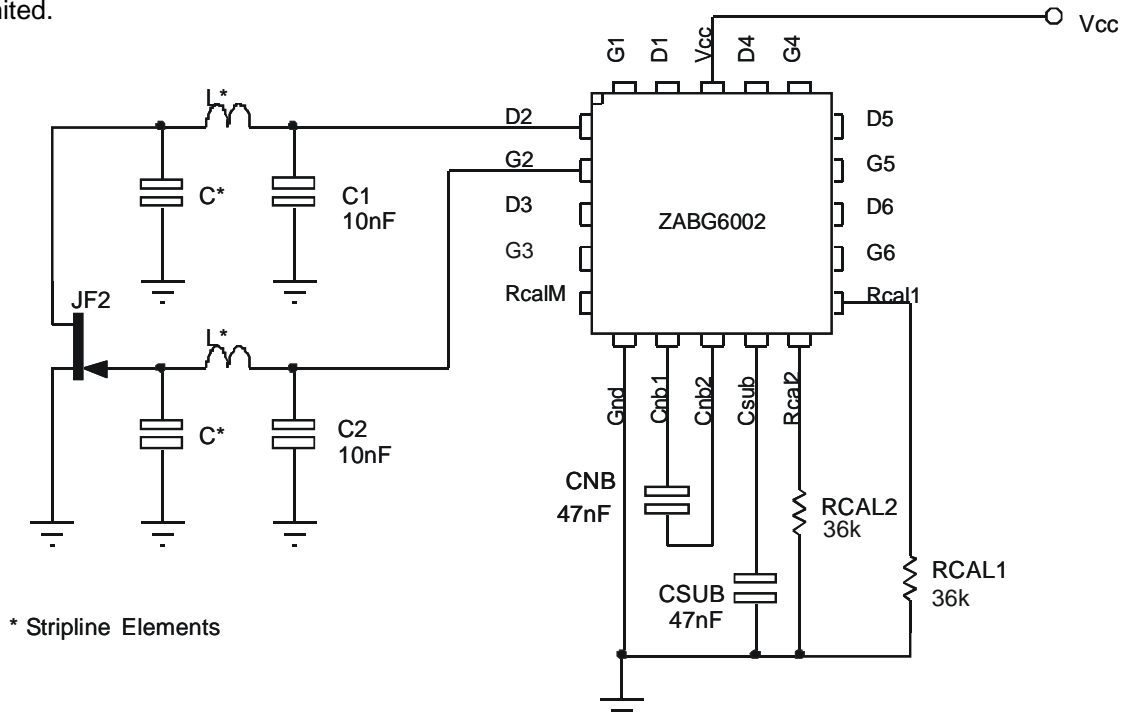
1. 6 LNA stages to provide standard bias to the GaAs or HEMT FET's
2. 4 LNA stages to provide standard bias to the GaAs or HEMT FET's plus 2 active mixer stages
3. Power down FET groups for LNA switching or power saving.

The truth table below shows the function of these features.

| R _{cal} Pin Resistor Termination | | | FET Stage | | | | | |
|---|-------------------|-------------------|----------------|--------|----------------|--------|----------------------|--------|
| R _{cal1} | R _{cal2} | R _{calM} | 1st LNA Stages | | 2nd LNA Stages | | 3rd LNA/Mixer Stages | |
| | | | Bias 1 | Bias 4 | Bias 2 | Bias 5 | Bias 3 | Bias 6 |
| Gnd | Gnd | Open | On | On | On | On | On | On |
| Gnd | Gnd | Gnd | On | On | On | On | Mixer | Mixer |
| Gnd | 3V | Open | On | On | Off | Off | Off | Off |
| Gnd | 3V | Gnd | On | On | Off | Off | Mixer | Mixer |
| 3V | Gnd | Open | Off | Off | On | On | On | On |
| 3V | Gnd | Gnd | Off | Off | On | On | Mixer | Mixer |
| 3V | 3V | Open | Off | Off | Off | Off | Off | Off |
| 3V | 3V | Gnd | Off | Off | Off | Off | Mixer | Mixer |

ZABG6002 in 6 LNA mode

Below is a partial applications circuit for the ZABG6002 showing all external components needed for biasing one of the six FET stages available as a normal LNA bias. Each bias stage is provided with a gate and drain pin. The drain pin provides a regulated 2.0V supply that includes a drain current monitor. The drain current taken by the external FET is compared with a user selected level, generating a signal that adjusts the gate voltage of the FET to obtain the required drain current. If for any reason, an attempt is made to draw more than the user set drain current from the drain pin, the drain voltage will be reduced to ensure excess current is not taken. The gate pin drivers are also current limited.

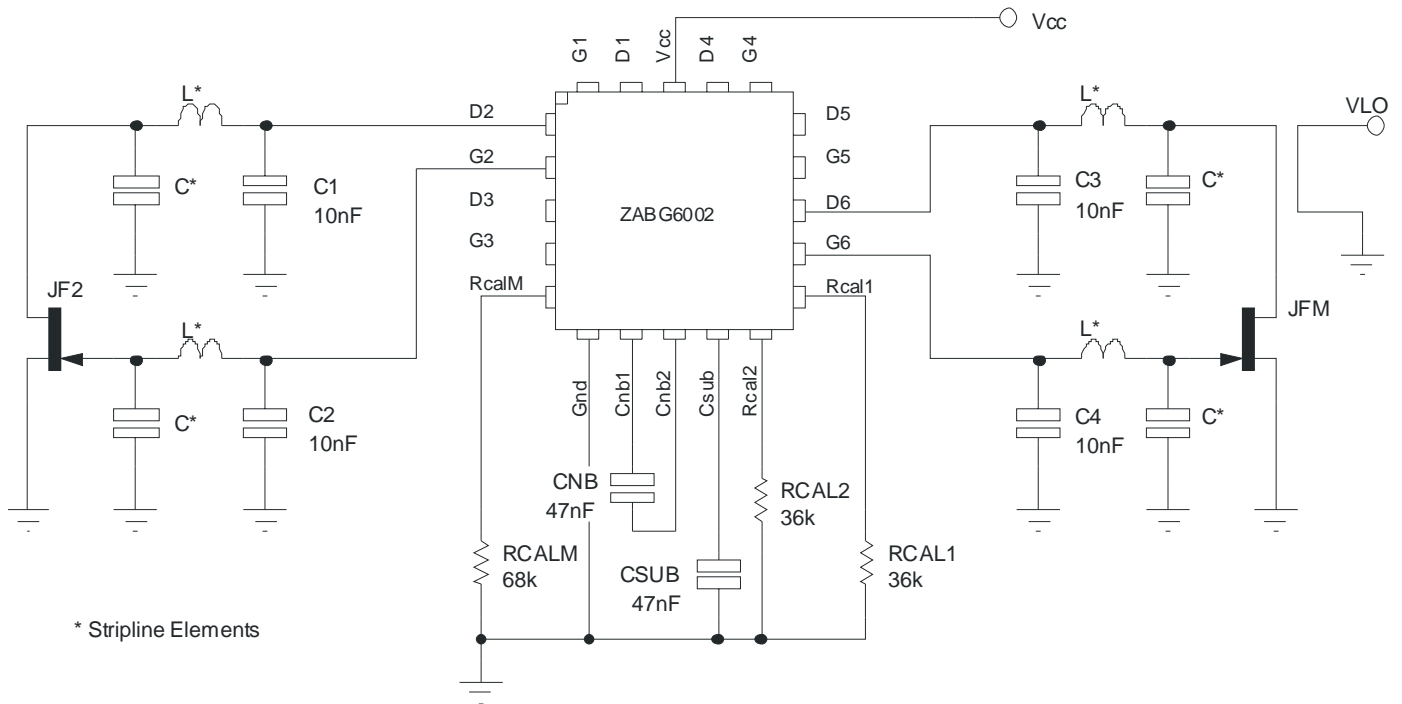


The bias stages are split up into two groups, with the drain current of each group set by an external R_{cal} resistor. R_{cal1} sets the drain currents of stages 1 and 4, whilst R_{cal2} sets the drain currents of stages 2,3,5 and 6.

This allows the optimization of drain currents for differing tasks such as input stages where noise can be critical and later amplifier stages where gain may be more important. A graph showing the relationship between the value of R_{CAL} and I_D is provided in the Typical Characteristics section of this datasheet. To ensure that the mixer function is disabled the R_{CALM} pin should be left open circuit.

ZABG6002 in 4 LNA and 2 active mixer mode

Below is a partial applications circuit for the ZABG6002 showing all external components needed for biasing one of the four FET stages available for LNA bias and one of the two mixer bias stages. Each LNA bias stage is provided with a gate and drain pin. The drain pin provides a regulated 2.0V supply that includes a drain current monitor. Each mixer bias stage is provided with a gate and drain pin. The drain pin provides a regulated 0.3V supply that includes a drain current monitor but optimized to the requirements of an active mixer. The drain current taken by the external FET (LNA and Mixer) is compared with a user selected level, generating a signal that adjusts the gate voltage of the FET to obtain the required drain current. If for any reason, an attempt is made to draw more than the user set drain current from the drain pin, the drain voltage will be reduced to ensure excess current is not taken. The gate pin drivers are also current limited.



The bias stages are split up into three groups, with the drain current of each group set by an external R_{CAL} resistor. R_{CAL1} sets the LNA drain currents of stages 1 and 4 and R_{CAL2} sets the drain currents of LNA stages 2 and 5. R_{CALM} sets the mixer drain currents of stages 3 and 6. This allows the optimization of drain currents for differing tasks such as input stages where noise can be critical and later amplifier stages where gain may be more important. A graph showing the relationship between the value of R_{CAL} and I_D is provided in the Typical Characteristics section of this datasheet.

General Operation

In both modes the R_{CAL} 1 and R_{CAL} 2 pins can also be used as logic inputs. If set to a logic high state ($>3.0V$), the associated FET bias stages programmed for LNA use (2V drains) are disabled by driving gate pins to $-2.5V$ and switching drain pins open-circuit. This feature can be used as part of a power management system that turns off any unwanted stages in a multi input receiver.

The ZABG6002 includes a switched capacitor DC-DC converter that is used to generate the negative supply required to bias depletion mode FETs used in common source circuit configuration as shown above. This converter uses two external capacitors, C_{NB} the charge transfer capacitor and C_{SUB} the output reservoir capacitor. The circuit provides a regulated $-2.5V$ supply both for gate driver use and for external use if required (for extra discrete bias stages, mixer bias, local oscillator bias etc.). The $-2.5V$ supply is available from the C_{SUB} pin.

If any bias stages are not required, their gate and drain pins may be left open circuit. If all bias stages associated with an R_{CAL} resistor are not required, then this resistor may be omitted.

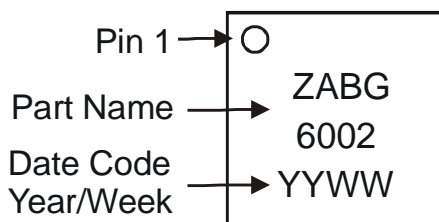
It must be noted that the exposed pad of the QFN package must be either left floating or connected to C_{sub} .

Ordering Information

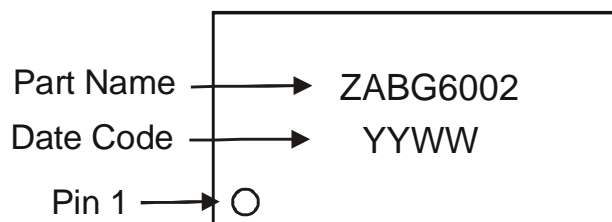
| Device | Package | Reel size (inches) | Tape width (mm) | Quantity per reel |
|----------------|---------|--------------------|-----------------|-------------------|
| ZABG6002JB20TC | QFN2044 | 13 | 12 | 3,000 |
| ZABG6002Q20TC | QSOP20 | 13 | 16 | 2,500 |

Marking Information

QFN2044

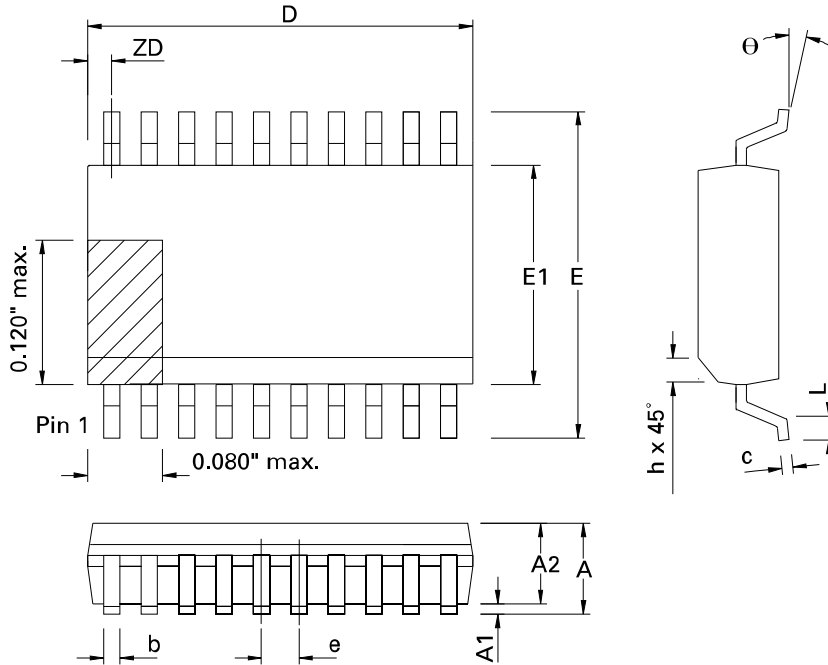


QSOP20



Package Outline Dimensions

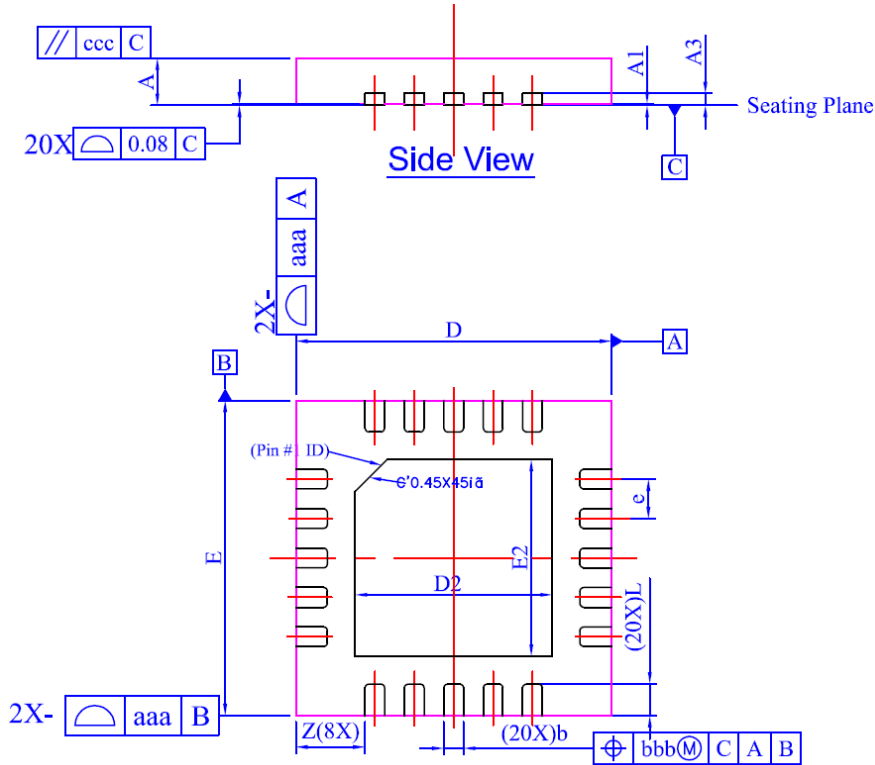
QSOP20



| DIM | Millimeters | | Inches | |
|----------|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.35 | 1.75 | 0.053 | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A2 | 1.25 | 1.50 | 0.049 | 0.059 |
| D | 8.56 | 8.74 | 0.337 | 0.344 |
| ZD | 0.058 REF | | 1.47 REF | |
| b | 0.20 | 0.30 | 0.008 | 0.012 |
| c | 0.18 | 0.25 | 0.007 | 0.010 |
| e | 0.64 BSC | | 0.025 BSC | |
| E | 5.79 | 6.20 | 0.228 | 0.244 |
| E1 | 3.81 | 3.99 | 0.150 | 0.157 |
| L | 0.41 | 1.27 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |
| h | 0.25 | 0.50 | 0.010 | 0.020 |

Package Outline Dimensions (Cont.)

QFN2044



| DIM | Min. | Max. | Typ. |
|-----|------|------|-------|
| D | 3.95 | 4.05 | 4.00 |
| E | 3.95 | 4.05 | 4.00 |
| D2 | 2.40 | 2.60 | 2.50 |
| E2 | 2.40 | 2.60 | 2.50 |
| A | 0.57 | 0.63 | 0.60 |
| A1 | 0 | 0.05 | 0.02 |
| A3 | — | — | 0.15 |
| b | 0.20 | 0.30 | 0.25 |
| L | 0.35 | 0.45 | 0.40 |
| e | — | — | 0.50 |
| z | — | — | 0.875 |
| aaa | 0.25 | | |
| bbb | 0.10 | | |
| ccc | 0.10 | | |

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel. Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

Copyright © 2010, Diodes Incorporated

www.diodes.com