CHESEN ELECTRONICS CORP.

CSC0100P

CSC0100P

USB and PS/2 Combo Peripheral OTP Controller

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Revision History

Revision No.	History	Date	Remark
0.10	Preliminary issue	July 22, 2003	
0.20	Revise EEPROM programming	Jan. 18, 2004	
0.30	Fixed IRQII & IRQEII register address error	July 20, 2004	
1.00	- Amend program user guide - Initial release	July 28, 2004	

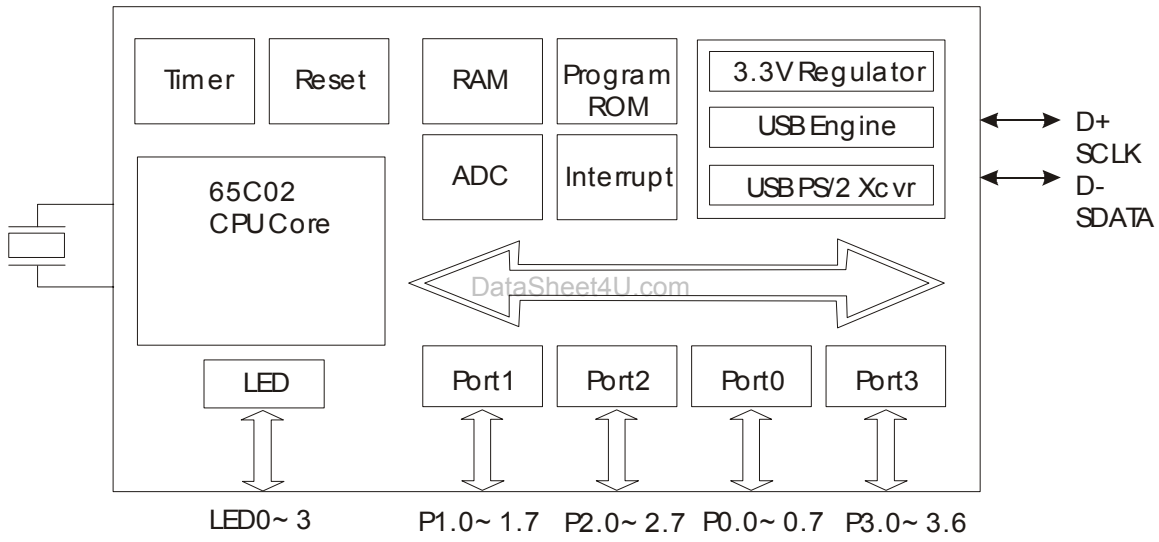
Features

- Low cost solution for low speed USB or PS/2 peripheral, such as keyboard, mice, joystick and others
- Built-in 65C02 8 Bit CPU
  - 6MHz external ceramic resonator
  - 3MHz internal CPU clock
  - 256 bytes RAM
  - 8K x 8 EPROM
  - Auto configure to operate as USB or PS/2 interface
- USB specification compliance:
  - Conforms to USB specification, version 1.1
  - Conforms to USB HID specification, version 1.1
  - Supports 1 low speed device address and 3 endpoints
  - 8 bytes FIFO for each endpoint
  - Integrated USB transceiver
  - Build in 3.3V regulator
- IO ports
  - 31 general purpose I/O pins
  - Port0, 1, 2 are 8 bit I/O with each pin supports high impedance or 20K ohm internal pull up
  - Maskable interrupt on Port2 pins with option programmable pull low
  - Port3 is 7 bit I/O with each pin supports high impedance or 20K ohm internal pull up, 4 of which support programmable interrupt function
  - 4 dedicated LED pins for direct LED driving capability
  - D+ D- can be used as general purpose I/O with programmable interrupt function, 5K ohm pull up while disable USB
- Built-in power-on reset.
- One 8 bits timer
- 8 channels 12 bits analog-to-digital converter switch with Port1
- Available package LQFP-44

Product Overview

The CSC0100P is an 8-bit 65C02 core CPU based USB microcontroller with electrically one-time programmable (OTP) read only memory (EPROM). It features 31 general purpose I/O (GPIO) pins to support USB, PS/2 interface and other applications. These I/O are grouped into 4 ports (Port0 to 3) with high impedance, internal pull up, interrupt mechanism and Schmitt trigger features for various peripheral application requirements. And the 4 dedicated LED output direct connect the LED components with high current drive capability.

Block Diagram



Pin Assignment

CSC0100P-L44

L44 Pin #	NAME	IN/OUT	DESCRIPTION
1	P31	I/O	Port 3 Bit 1
2	P32/INT0	I/O	Port 3 Bit 2 / External interrupt 0
3	P33/INT1	I/O	Port 3 Bit 3 / External interrupt 1
4	P34/INT2	I/O	Port 3 Bit 4 / External interrupt 2
5	P35/INT3	I/O	Port 3 Bit 5 / External interrupt 3
6	P36	I/O	Port 3 Bit 6 Input
7	VPP	P	Programming voltage supply; ground for normal operation
8	P00	I/O	Port 0 Bit 0
9	P01	I/O	Port 0 Bit 1
10	P02	I/O	Port 0 Bit 2
11	P03	I/O	Port 0 Bit 3
12	P04	I/O	Port 0 Bit 4
13	P05	I/O	Port 0 Bit 5
14	P06	I/O	Port 0 Bit 6
15	P07	I/O	Port 0 Bit 7
16	P10 / AD0	I/O[*1]	Port 1 Bit 0 / ADC channel 0
17	P11 / AD1	I/O[*1]	Port 1 Bit 1 / ADC channel 1
18	P12 / AD2	I/O[*1]	Port 1 Bit 2 / ADC channel 2
19	P13 / AD3	I/O[*1]	Port 1 Bit 3 / ADC channel 3
20	P14 / AD4	I/O[*1]	Port 1 Bit 4 / ADC channel 4
21	P15 / AD5	I/O[*1]	Port 1 Bit 5 / ADC channel 5
22	P16 / AD6	I/O[*1]	Port 1 Bit 6 / ADC channel 6
23	P17 / AD7	I/O[*1]	Port 1 Bit 7 / ADC channel 7
24	P20	I/O	Port 2 Bit 0
25	P21	I/O	Port 2 Bit 1
26	P22	I/O	Port 2 Bit 2
27	P23	I/O	Port 2 Bit 3
28	P24	I/O	Port 2 Bit 4
29	P25	I/O	Port 2 Bit 5
30	P26	I/O	Port 2 Bit 6
31	P27	I/O	Port 2 Bit 7
32	LED0	OUT	LED Output Bit 0
33	LED1	OUT	LED Output Bit 1
34	LED2	OUT	LED Output Bit 2
35	LED3	OUT	LED Output Bit 3
36	SELPAD	IN	GPIO Schmitt Trigger input mode select
37	P5V	P	Power supply
38	OSCO	OUT	Crystal/Ceramic resonator out
39	OSCI	IN	Crystal/Ceramic resonator in
40	PADGND	P	Ground
41	USB3V3	P	Power 3.3V
42	D+ / SCLK	I/O	USB data+ / PS/2 SCLK data
43	D- / SDATA	I/O	USB data- / PS/2 SDATA
44	P30	I/O	Port 3 Bit 0 + Schmitt trigger Input

[*1]: Input mode while used as ADC channel (for 8K ROM version only)

CPU and Memory

CPU

The CPU core of CSC0100P is an 8-bit 65C02 running with 3MHz frequency.

ROM

CSC0100P builds in **8K bytes** program memory EPROM with address from **E000H to FFFFH**. The **FFFAH** and **FFFBH** are non-mask interrupt (NMI) vector address, the **FFFCH** and **FFFDH** are CPU reset vector address, and **FFFEH** and **FFFFH** are maskable interrupt vector address。

RAM

CSC0100P builds in **256 bytes** RAM for user data and stack. The address of SRAM is from **80H** to **17FH**. The stack register has to set to **7FH** in the beginning of user program, and then the stack pointer will point to address **17FH**.

Memory Map

$0000 $0033	System Register	
	Unused	
$0080 $00FF	RAM	
$0100 $017F	RAM	
	Unused	
$E000	EPROM	
$FFFA	NMI-L	NMI Vector
$FFFB	NMI-H	
$FFFC	RESET-L	RESET Vector
$FFFD	RESET-H	
$FFFE	IRQ-L	IRQ Vector
$FFFF	IRQ-H	

System Register

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$00	Function IRQ Status I IRQI	00H	R		INT3	INT2	P2INT	4ms	INT1	INT0	TMR
			W								
$01	Function IRQ Clear I IRQCLRI	00H	R								
			W		CINT3	CINT2	CP2INT	C4ms	CINT1	CINT0	CTMR
$02	IRQ Enable I IRQEI	00H	R	EWDT	EINT3	EINT2	EP2INT	E4ms	EINT1	EINT0	ETMR
			W								
$03	IRQ USB Status IRQUSB	00H	R	SUSP	STUP			IN2	IN1	OT0	IN0
			W								
$04	IRQ USB Clear IRQUSBCLR	00H	R								
			W	CSUSP	CSTUP			CIN2	CIN1	COT0	CIN0
$05	IRQ USB Enable IRQUSBE	00H	R	ESUSP	ESTUP			EIN2	EIN1	EOT0	EIN0
			W								
$06	Timer Register TIMER	00H	R								
			W	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0
$07	Timer Control TCON	01H	R	TEST	TESTQ						
			W								ETIMER
$08	Timer Mode TMOD	00H	R						TMD2	TMD1	TMD0
			W								
$09	Port 0 Data PORT0	FFH	R	P07	P06	P05	P04	P03	P02	P01	P00
			W								
$0A	Port 1 Data PORT1	FFH	R	P17	P16	P15	P14	P13	P12	P11	P10
			W								
$0B	Port 2 Data PORT2	FFH	R	P27	P26	P25	P24	P23	P22	P21	P20
			W								
$0C	Port 3 Data PORT3	1FH	R		P36	P35	P34	P33	P32	P31	P30
			W								
$0D	LED	FFH	R					LED3	LED 2	LED 1	LED0
			W								
$0E	Clear Watch Dog CLRWDT	00H	R								
			W	0	1	0	1	0	1	0	1
$0F	Mode Flag MODE_FG	02H	R							POF	SUSF
			W								
$10	USB Address UADD	00H	R		UADD6	UADD5	UADD4	UADD3	UADD2	UADD1	UADD0
			W								
$11	Device Feature Control DFC	21H	R	x	x	PS2EN	x	RESUME	0	x	VCPI
			W								
$12	TXDAT0	XXH	R								
			W	T0B7	T0B6	T0B5	T0B4	T0B3	T0B2	T0B1	T0B0
$13	TXCNT0	XXH	R								
			W					C0B3	C0B2	C0B1	C0B0
$14	TXFLG0	00H	R								
			W						T0SEQC	STL0	T0FULL
$15	RXDAT0	XXH	R	R0B7	R0B6	R0B5	R0B4	R0B3	R0B2	R0B1	R0B0
			W								
$16	RXCNT0	XXH	R					X0B3	X0B2	X0B1	X0B0
			W								
$17	RXFLG0	00H	R								
			W							RSTL0	R0FULL
$18	TXDAT1	XXH	R								
			W	T1B7	T1B6	T1B5	T1B4	T1B3	T1B2	T1B1	T1B0

$19	TXCNT1	XXH	R								
			W					C1B3	C1B2	C1B1	C1B0
$1A	TXFLG1	00H	R					T1EPE	T1SEQC	STL1	T1FULL
			W								
$1B	TXDAT2	XXH	R								
			W	T2B7	T2B6	T2B5	T2B4	T2B3	T2B2	T2B1	T2B0
$1C	TXCNT2	XXH	R								
			W					C2B3	C2B2	C2B1	C2B0
$1D	TXFLG2	00H	R					T2EPE	T2SEQC	STL2	T2FULL
			W								
$1E	SUSLO	00H	R								
			W	0	1	0	1	0	1	0	1
$1F	SUSHI	00H	R								
			W	1	0	1	0	1	0	1	0
$20	ADC Status/Control ADSCR	20H	R	ADACT		CKS2	CKS1	CKS0	CH2	CH1	CH0
			W		ADON						
$21	ADC Data ADDRH	00H	R	ADDR11	ADDR10	ADDR9	ADDR8	ADDR7	ADDR6	ADDR5	ADDR4
			W								
$22	ADC Data ADDRL	00H	R					ADDR3	ADDR2	ADDR1	ADDR0
			W								
$23	Port1 Control P1CON	00H	R	P1CON7	P1CON6	P1CON5	P1CON4	P1CON3	P1CON2	P1CON1	P1CON0
			W								
$24	INT_CFGI	00H	R		I1EDGE	I1_POL1	I1_POL0		I0EDGE	I0_POL1	I0_POL0
			W								
$25	INT_CFGII	00H	R		I3EDGE	I3_POL1	I3_POL0		I2EDGE	I2_POL1	I2_POL0
			W								
$26	INT_CFGIII	00H	R		NEDGE	N_POL1	N_POL0		PEDGE	P_POL1	P_POL0
			W								
$27	Function IRQ Status II IRQII		R							USBN	USBP
			W								
$28	IRQ Enable II IRQEII	00H	R							EUSBN	EUSBP
			W								
$29	Function IRQ Clear II IRQCLRII	00H	R								
			W							CUSBN	CUSBP
$2A	Port0 Control P0CON	00H	R	P0CON7	P0CON6	P0CON5	P0CON4	P0CON3	P0CON2	P0CON1	P0CON0
			W								
$2B	Port2 Control P2CON	00H	R	P2CON7	P2CON6	P2CON5	P2CON4	P2CON3	P2CON2	P2CON1	P2CON0
			W								
$2C	Port3 Control P3CON	00H	R	P3CON7	P3CON6	P3CON5	P3CON4	P3CON3	P3CON2	P3CON1	P3CON0
			W								
$2D	USB Control USBCON	30H	R			NCON	PCON				
			W								
$2E	Port2 Pull_Low Control	08H	R								
			W								
$2F	ANAPOWER	00H	R					vrefsel	adclevel	X	X
			W								
$30	WakeTimer	00H	R	EN	waketm	0	0	0	0	S1	S0
			W								
$31	Port1 ADC Control	00H	R	P1_A7	P1_A6	P1_A5	P1_A4	P1_A3	P1_A2	P1_A1	P1_A0
			W								
$32	DPLUS I/O Control	00H	R								DPIO
			W								
$33	DMINUS I/O Control	00H	R								DMIO
			W								

Power On Reset

CSC0100P builds in power on reset circuitry which will de-assert a 5ms pulse for resetting the system. User also can connect reset signal from the RESETB pin for external resetting control.

Clock and Timer

The system clock is coming from the external crystal or ceramic resonator with 6MHz frequency. This frequency will divide internal by 2 to generate 3MHz for CPU.
The system has an 8 bits timer. The clock source is system clock divided by Timer Mode Register value. Every time when the timer is enable and the Timer Register value down count to zero, it will generate a timer interrupt to the system when ETMR=1.

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$06	Timer Register TIMER	00H	R								
			W	TM7	TM6	TM5	TM4	TM3	TM2	TM1	TM0

TM7 ~ TM0: Timer value
00000000: 0
00000001: 1
00000010: 2
11111110: 254
11111111: 255

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$07	Timer Control TCON	01H	R	X	X						
			W								ETIMER

ETIMER: Enable timer
0: Enable
1: Disable

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$08	Timer Mode TMOD	00H	R W						TMD2	TMD1	TMD0

TMD2, TMD1, TMD0: Timer clock source

TMD2	TMD1	TMD0	Clock Source	Min. Count	Max.. Count
0	0	0	System / 16	2.66us	682.66 us
0	0	1	System / 32	5.32 us	1.36ms
0	1	0	System / 64	10.64 us	2.72 ms
0	1	1	System / 128	21.28 us	5.44 ms
1	0	0	System / 256	42.56 us	10.89 ms
1	0	1	System / 512	85.12 us	21.79 ms
1	1	0	System / 1024	170.24 us	43.58 ms
1	1	1	System / 2048	340.48 us	87.16 ms

Interrupt

The CSC0100P has the following interrupt sources.

1. External IO interrupt
   Programmable level, edge or bi-edge trigger interrupt from P3.2 (INT0), P3.3 (INT1), P3.4 (INT2), P3.5 (INT3), D+ (USBP) or D- (USBN).
2. Timer interrupt
   Interrupt source comes from the timer overflow.
3. 4ms interrupt
   Interrupt source comes from every 4ms.
4. Port2 interrupt
   Interrupt will generate when any bit of Port2 is “0”.
5. OT0 interrupt
   Interrupt source when USB endpoint 0 received data.
6. IN0, IN1, IN2 interrupt
   Interrupt source when Host ready to receive USB data
7. STUP interrupt
   Interrupt source when USB endpoint 0 received SETUP TOKEN.
8. SUSP interrupt
   Interrupt source when USB bus idles for more than 3ms.

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$00	Function IRQ Status I IRQI	00H	R		INT3	INT2	P2INT	4ms	INT1	INT0	TMR
			W								
$01	Function IRQ Clear I IRQCLRI	00H	R								
			W		CINT3	CINT2	CP2INT	C4ms	CINT1	CINT0	CTMR

TMR: Timer interrupt status
0: No timer interrupt
1: 1 timer interrupt is pending

INT0: External P3.2 interrupt status
0: No external I/O interrupt
1: 1 external I/O interrupt is pending

INT1: External P3.3 interrupt status
0: No external interrupt
1: 1 external interrupt is pending

4ms: 4ms interrupt status
0: 4ms not coming
1: Reach 4ms and interrupt is pending

P2INT: Port2 interrupt status
0: None of the bit in Port2 is “0”
1: At least one bit in Port2 is “0”

INT2: External P3.4 interrupt status
0: No external I/O interrupt
1: 1 external I/O interrupt is pending

INT3: External P3.5 interrupt status
0: No external interrupt
1: 1 external interrupt is pending

CTMR: Clear timer interrupt
0: No function
1: Clear timer interrupt

CINT0: Clear external P3.2 interrupt
0: No function
1: Clear external P3.2 interrupt

CINT1: Clear external P3.3 interrupt
0: No function
1: Clear external P3.3 interrupt

C4ms: Clear 4ms interrupt
0: No function
1: Clear 4ms interrupt

CP2INT: Clear Port2 interrupt
0: No function
1: Clear Port2 interrupt

CINT2: Clear external P3.4 interrupt
0: No function
1: Clear external P3.4 interrupt

CINT3: Clear external P3.5 interrupt
0: No function
1: Clear external P3.5 interrupt

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$27	Function IRQ Status II IRQII	00H	R							USBN	USBP
			W								
$29	Function IRQ Clear II IRQCLRII	00H	R								
			W							CUSBN	CUSBP

USBP: External D+ interrupt status
- 0: No external I/O interrupt
- 1: 1 external I/O interrupt is pending

USBN: External D- interrupt status
- 0: No external I/O interrupt
- 1: 1 external I/O interrupt is pending

CUSBP: Clear external D+ interrupt
- 0: No function
- 1: Clear external D+ interrupt

CUSBN: Clear external D- interrupt
- 0: No function
- 1: Clear external D- interrupt

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$02	IRQ Enable I IRQEI	00H	R	EWDT	EINT3	EINT2	EP2INT	E4ms	EINT1	EINT0	ETMR
			W								

ETMR: Enable timer interrupt
- 0: No function
- 1: Enable timer interrupt

EINT0: Enable external P3.2 interrupt
- 0: No function
- 1: Enable external P3.2 interrupt

EINT1: Enable external P3.3 interrupt
- 0: No function
- 1: Enable external P3.3 interrupt

E4ms: Enable 4ms interrupt
- 0: No function
- 1: Enable 4ms interrupt

EP2INT: Enable Port2 interrupt
- 0: No function
- 1: Enable Port2 interrupt

EINT2: Enable external P3.4 interrupt
0: No function
1: Enable external P3.4 interrupt

EINT3: Enable external P3.5 interrupt
0: No function
1: Enable external P3.5 interrupt

EWDT: Enable watchdog function
0: Enable watchdog function
1: Disable

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$28	IRQ Enable II IRQEII	00H	R							EUSBN	EUSBP
			W								

*Function available disable USB device (USBEN="0")

EUSBP: Enable external D+ interrupt
0: No function
1: Enable external D+ interrupt

EUSBN: Enable external D- interrupt
0: No function
1: Enable external D- interrupt

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$03	IRQ USB Status IRQUSB	00H	R	SUSP	STUP			IN2	IN1	OT0	IN0
			W								

IN0: USB endpoint 0 host receiving ready interrupt status
0: No USB IN0 interrupt
1: One IN0 interrupt is pending

OT0: USB endpoint 0 receiving data interrupt status
0: No USB OT0 interrupt
1: 1 OT0 interrupt is pending

IN1: USB endpoint 1 host receiving ready interrupt status
0: No USB IN0 interrupt
1: One IN0 interrupt is pending

IN2: USB endpoint 2 host receiving ready interrupt status
0: No USB IN2 interrupt
1: One IN2 interrupt is pending

STUP: USB endpoint 0 host receiving SETUP TOKEN interrupt status
0: No USB SETUP TOKEN interrupt
1: One USB SETUP TOKEN interrupt is pending

SUSP: USB SUSPEND interrupt status
0: No USB SUSPEND interrupt
1: One USB SUSPEND interrupt is pending

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$04	IRQ USB Clear IRQUSBCLR	00H	R								
			W	CSUSP	CSTUP			CIN2	CIN1	COT0	CIN0

CIN0: Clear USB endpoint 0 host receiving ready interrupt
0: No function
1: One IN0 interrupt is pending

COT0: Clear USB endpoint 0 receiving data interrupt
0: No function
1: 1 OT0 interrupt is pending

CIN1: Clear USB endpoint 1 host receiving ready interrupt
0: No function
1: One IN0 interrupt is pending

CIN2: Clear USB endpoint 2 host receiving ready interrupt
0: No function
1: One IN2 interrupt is pending

CSTUP: Clear USB endpoint 0 host receiving SETUP TOKEN interrupt
0: No function
1: One USB SETUP TOKEN interrupt is pending

CSUSP: Clear USB SUSPEND interrupt
0: No function
1: One USB SUSPEND interrupt is pending

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$05	IRQ USB Enable IRQUSBE	00H	R/W	ESUSP	ESTUP			EIN2	EIN1	EOT0	EIN0

EIN0: Enable USB endpoint 0 host receiving ready interrupt
0: No function
1: Enable IN0 interrupt

EOT0: Enable USB endpoint 0 receiving data interrupt
0: No function
1: Enable OT0 interrupt

EIN1: Enable USB endpoint 1 host receiving ready interrupt
0: No function
1: Enable IN0 interrupt

EIN2: Enable USB endpoint 2 host receiving ready interrupt
0: No function
1: Enable IN2 interrupt

ESTUP: Enable USB endpoint 0 host receiving SETUP TOKEN interrupt
0: No function
1: Enable USB SETUP TOKEN interrupt

ESUSP: Enable USB SUSPEND interrupt
0: No function
1: Enable USB SUSPEND interrupt

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$24	INT_CFGI	00H	R W		I1EDGE	I1_POL1	I1_POL0		I0EDGE	I0_POL1	I0_POL0

I0EDGE, I0_POL1, I0_POL0: External interrupt level and polarity for INT0

I0EDGE	I0_POL1	I0_POL0	Level	Polarity
0	0	0	Edge trigger	Falling
0	0	1	Edge trigger	Rising
1	0	0	Level trigger	High
1	0	1	Level trigger	Low
0	1	0	Edge trigger	Bi-edge

I1EDGE, I1_POL1, I1_POL0: External interrupt level and polarity for INT1

I1EDGE	I1_POL1	I1_POL0	Level	Polarity
0	0	0	Edge trigger	Falling
0	0	1	Edge trigger	Rising
1	0	0	Level trigger	High
1	0	1	Level trigger	Low
0	1	0	Edge trigger	Bi-edge

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$25	INT_CFGII	00H	R W		I3EDGE	I3_POL1	I3_POL0		I2EDGE	I2_POL1	I2_POL0

I2EDGE, I2_POL1, I2_POL0: External interrupt level and polarity for INT2

I2EDGE	I2_POL1	I2_POL0	Level	Polarity
0	0	0	Edge trigger	Falling
0	0	1	Edge trigger	Rising
1	0	0	Level trigger	High
1	0	1	Level trigger	Low

I3EDGE, I3_POL1, I3_POL0: External interrupt level and polarity for INT3

I3EDGE	I3_POL1	I3_POL0	Level	Polarity
0	0	0	Edge trigger	Falling
0	0	1	Edge trigger	Rising
1	0	0	Level trigger	High
1	0	1	Level trigger	Low

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$26	INT_CFGIII	00H	R/W		NEDGE	N_POL1	N_POL0		PEDGE	P_POL1	P_POL0

PEDGE, P_POL1, P_POL0: External interrupt level and polarity for D+

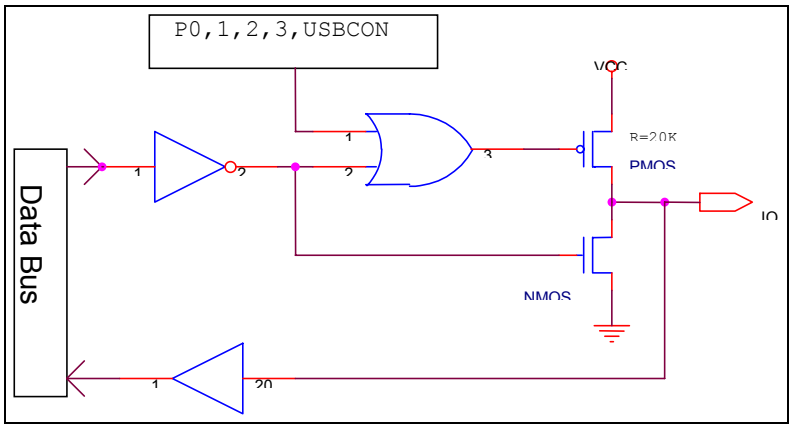
PEDGE	P_POL1	P_POL0	Level	Polarity
0	0	0	Edge trigger	Falling
0	0	1	Edge trigger	Rising
1	0	0	Level trigger	High
1	0	1	Level trigger	Low
0	1	0	Edge trigger	Bi-edge

NEDGE, N_POL1, N_POL0: External interrupt level and polarity for D-

NEDGE	N_POL1	N_POL0	Level	Polarity
0	0	0	Edge trigger	Falling
0	0	1	Edge trigger	Rising
1	0	0	Level trigger	High
1	0	1	Level trigger	Low
0	1	0	Edge trigger	Bi-edge

I/O Port

The CSC0100P has 31 general purpose I/O pins distributed on Port0, Port1, Port2 and Port3. When using the I/O pin as output, just write the corresponding bit to the register. While writing “1” to the corresponding bit first as using this pin as input.
The four LED pins is output only with high current driving capability.



Block Diagram of Port0, 1, 2, 3

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$09	Port 0 Data PORT0	FFH	R W	P07	P06	P05	P04	P03	P02	P01	P00
$0A	Port 1 Data PORT1	FFH	R W	P17	P16	P15	P14	P13	P12	P11	P10
$0B	Port 2 Data PORT2	FFH	R W	P27	P26	P25	P24	P23	P22	P21	P20
$0C	Port 3 Data PORT3	1FH	R W		P36	P35	P34	P33	P32	P31	P30
$0D	LED	FFH	R W					LED3	LED 2	LED 1	LED0
$32	DPLUS I/O Control	00H	R W								DPIO
$33	DMINUS I/O Control	00H	R W								DMIO

Pmn: Corresponding bit for Port0~Port3, where **m** represents for Port number and **n** represents for bit number.

LEDn: Corresponding LED output bit

DPIO: D+ status while disable USB function

DMIO: D- status while disable USB function

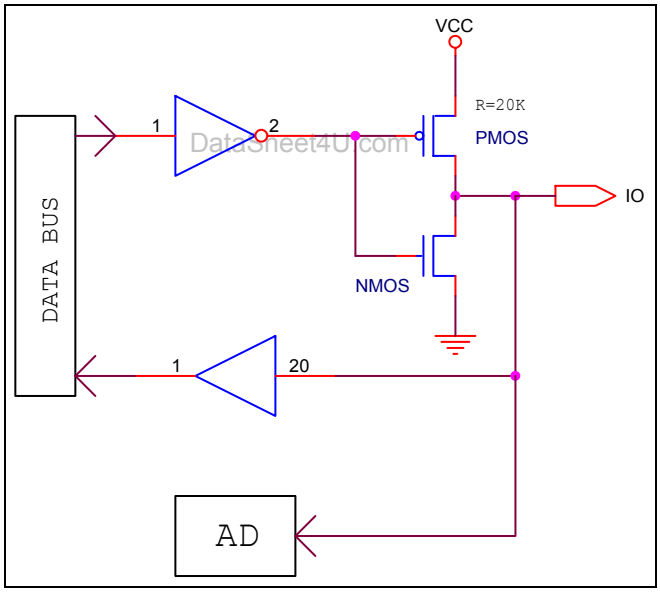
ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$23	Port1 Control P1CON	00H	R/W	P1CON7	P1CON6	P1CON5	P1CON4	P1CON3	P1CON2	P1CON1	P1CON0
$2A	Port0 Control P0CON	00H	R/W	P0CON7	P0CON6	P0CON5	P0CON4	P0CON3	P0CON2	P0CON1	P0CON0
$2B	Port2 Control P2CON	00H	R/W	P2CON7	P2CON6	P2CON5	P2CON4	P2CON3	P2CON2	P2CON1	P2CON0
$2C	Port3 Control P3CON	00H	R/W	P3CON7	P3CON6	P3CON5	P3CON4	P3CON3	P3CON2	P3CON1	P3CON0
$2D	USB Control USBCON	30H	R/W			NCON	PCON				
$2E	Port2 Pull_Low Control	08H	R/W								

P1CONn: Pull up control

0: Internal pull up with 20K ohm resistor

1: No internal pull up

When using the Port1 as analog to digital converter channel, the P1CONn has to set to “1”.



P0CONn: Pull up control

0: Internal pull up with 20K ohm resistor

1: No internal pull up

P2CONn: Pull up control

0: Internal pull up with 20K ohm resistor

1: No internal pull up

P3CONn: Pull up control

0: Internal pull up with 20K ohm resistor

1: No internal pull up

PCON: D+ Pull up control
0: Internal pull up with 5K ohm resistor
1: No internal pull up

NCON: D- Pull up control
0: Internal pull up with 5K ohm resistor
1: No internal pull up

D- D+ and PS/2 Operation

The CSC0100P is optimized to combine USB or PS/2 interface device with following features:
1. The USB D+ and D- line can be used for general purpose I/O or SCLK and SDATA for PS/2.
2. When USB disabled (**VCPI=**"1"), D+ D- pins will be placed in high impedance with pull up disable.
3. The 5K ohm internal pull up on the D+ (SCLK) and D- (SDATA) pins when enable (PCON="0" NCON="0")
4. The state of D+ (SCLK) and D- (SDATA) pins can be read from the DPLUS DMINUS register

Mode of D+ and D-	Procedure
USB	1. Enable USB (**PS2EN="1" && VCPI="0"**) 2. Drive 3.3V voltage output with internal regulator (**VCPI**="0"), 1.5K ohm internal pull up on regulator output and D- pin
PS/2	1. Disable USB (**PS2EN="0" && VCPI="1"**) 2. Drive floating state on internal regulator (**VCPI**="1") 3. Enable PS/2 5K ohm pull up on SCLK, SDATA (**PS2EN**="0") 4. Enable interrupt and read/write status
IO with high impedance	1. Disable USB **(PS2EN="0" && VCPI="1")** 2. Drive floating state on internal regulator (**VCPI**="1") **3.** Disable PS/2 5K ohm pull up on D+, D- **(PCON,NCON ="1")** 4. Read/Write I/O status with **DPLUS DMINUS** register
IO with 5K ohm pull up	1. Disable USB (**PS2EN="0" && VCPI="1")** 2. Drive floating state on internal regulator (**VCPI**="1") 3. Enable PS/2 5K ohm pull up on D+, D- (**PCON, NCON ="0"**) 4. Read/Write I/O status with **DPLUS DMINUS** register

Watch-Dog Timer

The watch-dog resets the system whenever the 150ms internal watch-dog timer run over. Writing 55H to the Clear Watch Dog register at address 0x0E will clear the timer. This is used to prevent the dead lock of program.

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$0E	Clear Watch Dog CLRWDT	00H	R								
			W	0	1	0	1	0	1	0	1

Wake Up Timer

The wake up time can be programmed by configuring the WakeTimer 30H.

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$30	WakeTimer	00H	R/W	EN	waketm	0	0	0	0	S1	S0

S0	S1	Wake up time
0	0	1ms
0	1	2ms
1	0	4ms
1	1	8ms

waketm: State of the wake up timer

0: One wake up state under processing

1: No wake up under processing

EN: Enable wake up timer

0: Disable

1: Enable

Suspend Mode

The CSC0100P supports low power suspend mode. When there is no signal on the USB bus, there is a USB suspend interrupt (SUSP) request occurred. The suspend high / low register (SUSLO SUSHI) are used to place the CSC0100P into the suspend mode. The CSC0100P is placed into the low power state by writing #55H to SUSLO first, writes #AAH to SUSHI after then. The SUSF bit of the mode flag register (MODE_FG) will be set when enters suspend mode.
When the program is running, whether it is active from power on reset or resume reset by distinguishing the POF and SUSF in the mode flag register.

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$0F	Mode Flag MODE_FG	02H	R							POF	SUSF
			W								
$1E	SUSLO	00H	R								
			W	0	1	0	1	0	1	0	1
$1F	SUSHI	00H	R								
			W	1	0	1	0	1	0	1	0

SUSF: Suspend mode flag
0: Non-suspend mode
1: Suspend mode

POF: Power on reset flag
0: Not power on reset
1: Power on reset

USB Device

USB Address Register (UADD): address of USB device

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$10	USB Address UADD	00H	R W		UADD6	UADD5	UADD4	UADD3	UADD2	UADD1	UADD0

UADD6 ~ UADD0: USB address from 1 to 127

Device Feature Control Register (DFC):

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$11	Device Feature Control DFC	21H	R W	X	X	PS2EN	X	RESUME	0	X	VCPI

VCPI:

VCPI	VCP Output
0	D- Pull_up 1.5K to VCP
1	D- No Pull_up 1.5K to VCP

RESUME: When CSC0100P leaves the suspend mode, write this bit to wake up the system by sending a 10 ~ 15ms signal to host.

PS2EN: Disable PS/2 mode manually
0: PS/2 mode
1: USB mode

Transmit Data Register (TXDAT0, TXDAT1, TXDAT2): USB Transmit FIFO Data Register For Endpoint 0/1/2

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$12	TXDAT0	XXH	R								
			W	T0B7	T0B6	T0B5	T0B4	T0B3	T0B2	T0B1	T0B0
$18	TXDAT1	XXH	R								
			W	T1B7	T1B6	T1B5	T1B4	T1B3	T1B2	T1B1	T1B0
$1B	TXDAT2	XXH	R								
			W	T2B7	T2B6	T2B5	T2B4	T2B3	T2B2	T2B1	T2B0

Transmit Byte Count Register (TXCNT0, TXCNT1, TXCNT2): USB FIFO Transmit Byte Count Register For Endpoint 0/1/2

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$13	TXCNT0	XXH	R								
			W					C0B3	C0B2	C0B1	C0B0
$19	TXCNT1	XXH	R								
			W					C1B3	C1B2	C1B1	C1B0
$1C	TXCNT2	XXH	R								
			W					C2B3	C2B2	C2B1	C2B0

CnB3, CnB2, CnB1, CnB0: Transmit byte count from 0 to 8.
The transmit byte count register will increase automatically when every data writes to the transmit data register.
Write 0 to this register force device to send out empty data.

Transmit Flag Register (TXFLG0, TXFLG1, TXFLG2): USB Transmit Flag Register For Endpoint 0/1/2

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$14	TXFLG0	00H	R						T0SEQC	STL0	T0FULL
			W								
$1A	TXFLG1	00H	R					T1EPE	T1SEQC	STL1	T1FULL
			W								
$1D	TXFLG2	00H	R					T2EPE	T2SEQC	STL2	T2FULL
			W								

TnFULL (R): Transmit FIFO full
0: FIFO not full
1: FIFO full

TnFULL (W): Write “1” to start transmission

STLn: Write “1” to tell system the transmit error

TnSEQC:
0: Data transmit from DATA0
1: Data transmit from DATA1

T1EPE: Enable endpoint 1
0: Disable
1: Enable

T2EPE: Enable endpoint 2
0: Disable
1: Enable

Receive Data Register (RXDAT0): USB Receive FIFO Data Register For Endpoint 0

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$15	RXDAT0	XXH	R	R0B7	R0B6	R0B5	R0B4	R0B3	R0B2	R0B1	R0B0
			W								

Receive Byte Count Register: USB FIFO Receive Byte Count Register For Endpoint 0

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$16	RXCNT0	XXH	R					X0B3	X0B2	X0B1	X0B0
			W								

X0B3, X0B2, X0B1, X0B0: Receive byte count from 0 to 8.
The receive byte count register will increase automatically when every data writes to the receive data register.

Receive Flag Register (RXFLG0): USB Receive Flag Register For Endpoint 0

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$17	RXFLG0	00H	R							RSTL0	R0FULL
			W								

R0FULL: Receive FIFO Full
0: Receive FIFO not full
1: Receive FIFO full

RSTL0: Write “1” to tell system the receive error

Analog to Digital Converter

The CSC0100P (8K EPROM only) has 8 channels 12 bits analog to digital converter, the 8-ch analog converting input signals are from P1.0 ~ P1.7. When using P1 as analog input channel, the pull up of the relative bit should be disabled and
Port 1 ADC control should enable.

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$23	Port1 Control P1CON	00H	R W	P1CON7	P1CON6	P1CON5	P1CON4	P1CON3	P1CON2	P1CON1	P1CON0
$31	Port1 ADC Control	00H	R W	P1_A7	P1_A6	P1_A5	P1_A4	P1_A3	P1_A2	P1_A1	P1_A0

P1CONn: Pull up control

0: Internal pull up with 20K ohm resistor

1: No internal pull up

When using the Port1 as analog to digital converter channel, the P1CONn has to set to “1”.

P1_An: Enable port 1 ADC control

0: Disable ADC function

1: Enable ADC function

ADC Status/Control Register (ADSCR):

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$20	ADC Status/Control ADSCR	20H	R W	ADACT	ADON	CKS2	CKS1	CKS0	CH2	CH1	CH0

CH2, CH1, CH0: AD input channel selection

CH2	CH1	CH0	
0	0	0	AD0 (P1.0)
0	0	1	AD1 (P1.1)
0	1	0	AD2 (P1.2)
0	1	1	AD3 (P1.3)
1	0	0	AD4 (P1.4)
1	0	1	AD5 (P1.5)
1	1	0	AD6 (P1.6)
1	1	1	AD7 (P1.7)

CKS2, CKS1, CKS0: ADC conversion time

CKS2	CKS1	CKS0	ADC_CONVERT_TIME
0	0	0	1us
0	0	1	2us
0	1	0	4us
0	1	1	8us
1	0	0	16us
1	0	1	32us
1	1	0	64us
1	1	1	128us

ADON (W): Enable ADC

0: Disable ADC, the P1.0 ~ P1.7 act as general purpose I/O

1: Enable ADC, the P1.0 ~ P1.7 act as analog input channels

ADACT (R): ADC conversion

0: No conversion or conversion not ready

1: Conversion done

ADC Data Register (ADDR):

ADDR	REGISTER	RESET	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$21	ADC Data ADDRH	00H	R	ADDR11	ADDR10	ADDR9	ADDR8	ADDR7	ADDR6	ADDR5	ADDR4
			W								
$22	ADC Data ADDRL	00H	R					ADDR3	ADDR2	ADDR1	ADDR0
			W								
$2F	ANAPOWER	00H	R					vrefsel	adclevel	x	x
			W								

ADDRn (R): 12 bits ADC conversion data

adclevel: Internal reference voltage selection (if vrefsel=0)

0: 3.3V

1: 5.0V

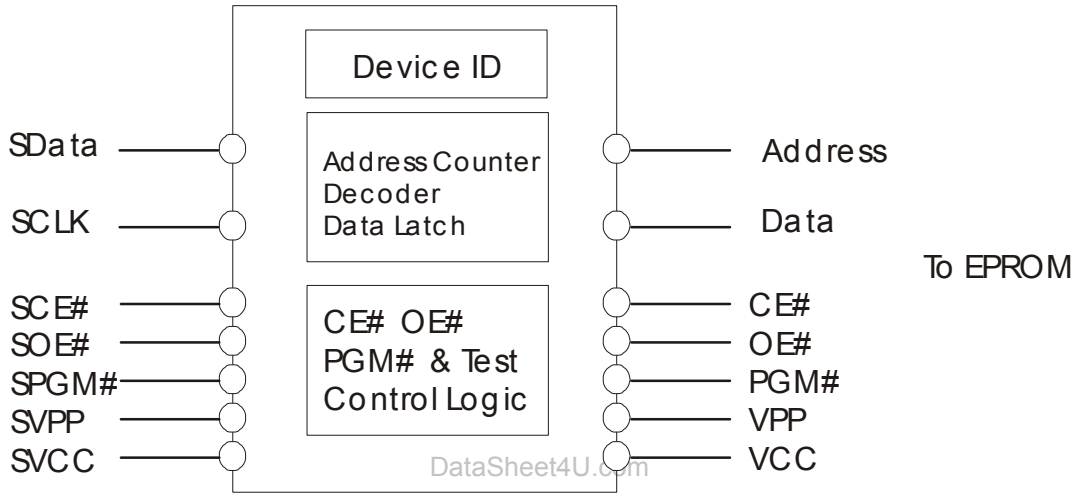
vrefsel: Reference voltage selection

0: Internal

1: External reference voltage from P3.6

Programming of EPROM

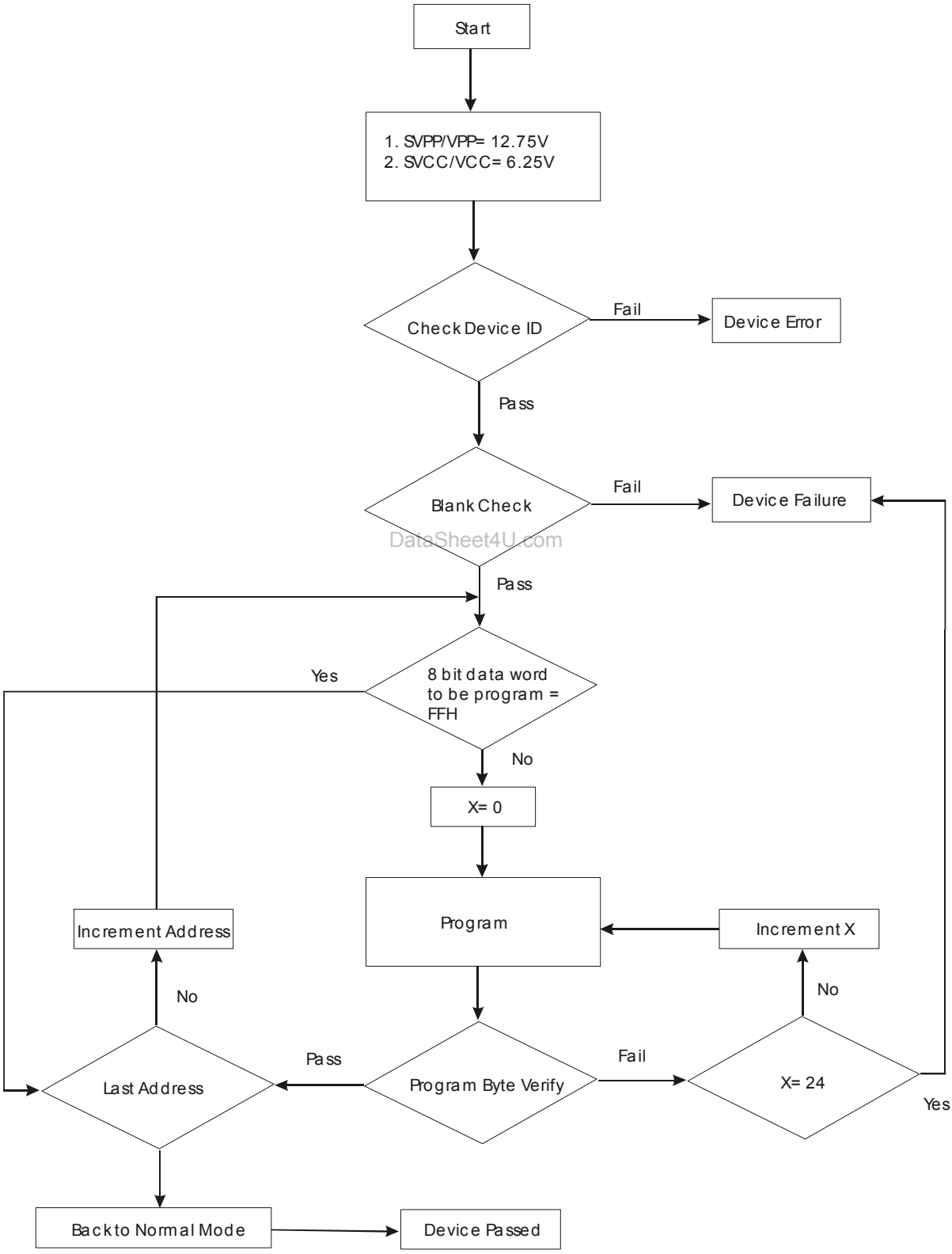
When the CSC0100P is delivered, the chip has all 64K bits in the HIGH state. “ZEROs” are loaded into the CSC0100P relevant bit through the procedure of programming. The programming mode is entered when 12.75V is applied to the VPP pin and 6.25V applied on VCC pin. The rising edge of SCLK shifts a data bit of SDATA to the data latch, data in the data latch can be programmed in 8-bit format to the EPROM directly through the parallel data bus.



Operation Modes

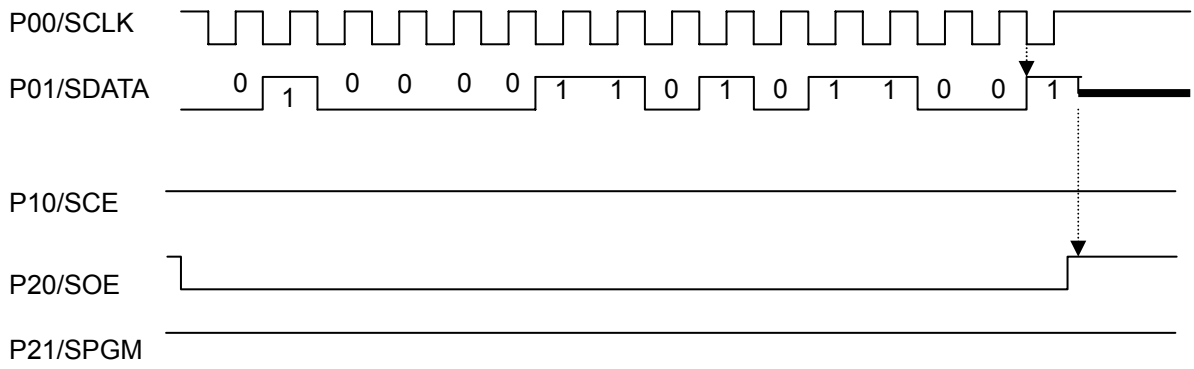
			Serial I/F (SIF)			Parallel I/F (PIF)			
Mode	**SVPP/VPP**	**SVCC/VCC**	**SCE#**	**SOE#**	**SDATA**	**CE#**	**OE#**	**PGM#**	**DATA**
Normal (N)	VCC	VCC	X	X	Hi-Z	V_{IL}	V_{IL}	X	Hi-Z
Program (P)	12.75V	6.25V	V_{IL}	V_{IH}	Shift In	V_{IL}	V_{IH}	V_{IL} t_{PW}	Data Out
Program Verify (PV)	12.75V	6.25V	V_{IL}	V_{IL}	Shift Out	V_{IL}	V_{IL}	V_{IH}	Data In
ID Verify (IDV)	12.75V	6.25V	V_{IH}	V_{IL}	Shift Out	--	--	--	--

Programming Specifications



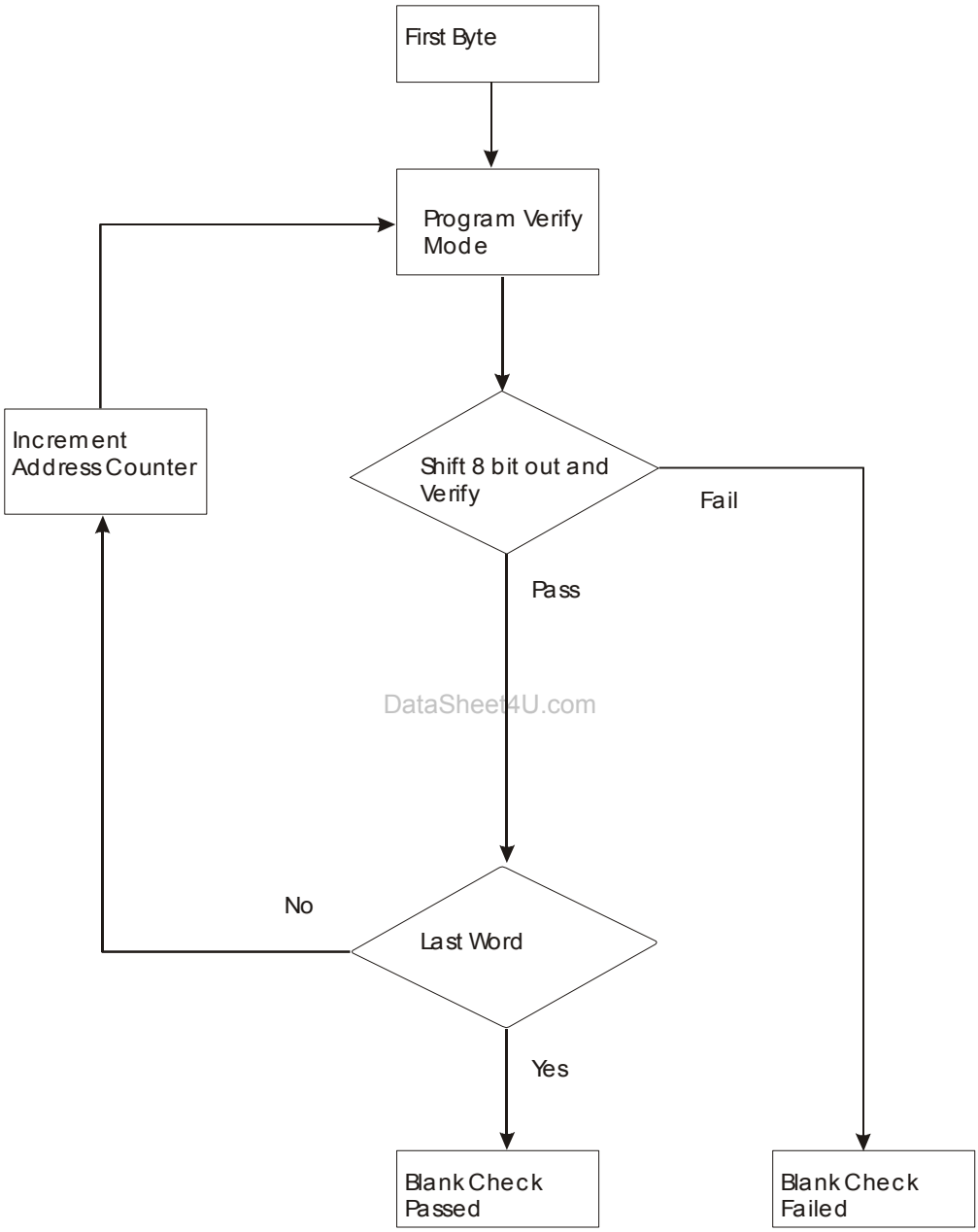
ID Verify

ID Verify (VPP=12.75V VCC=6.25V)



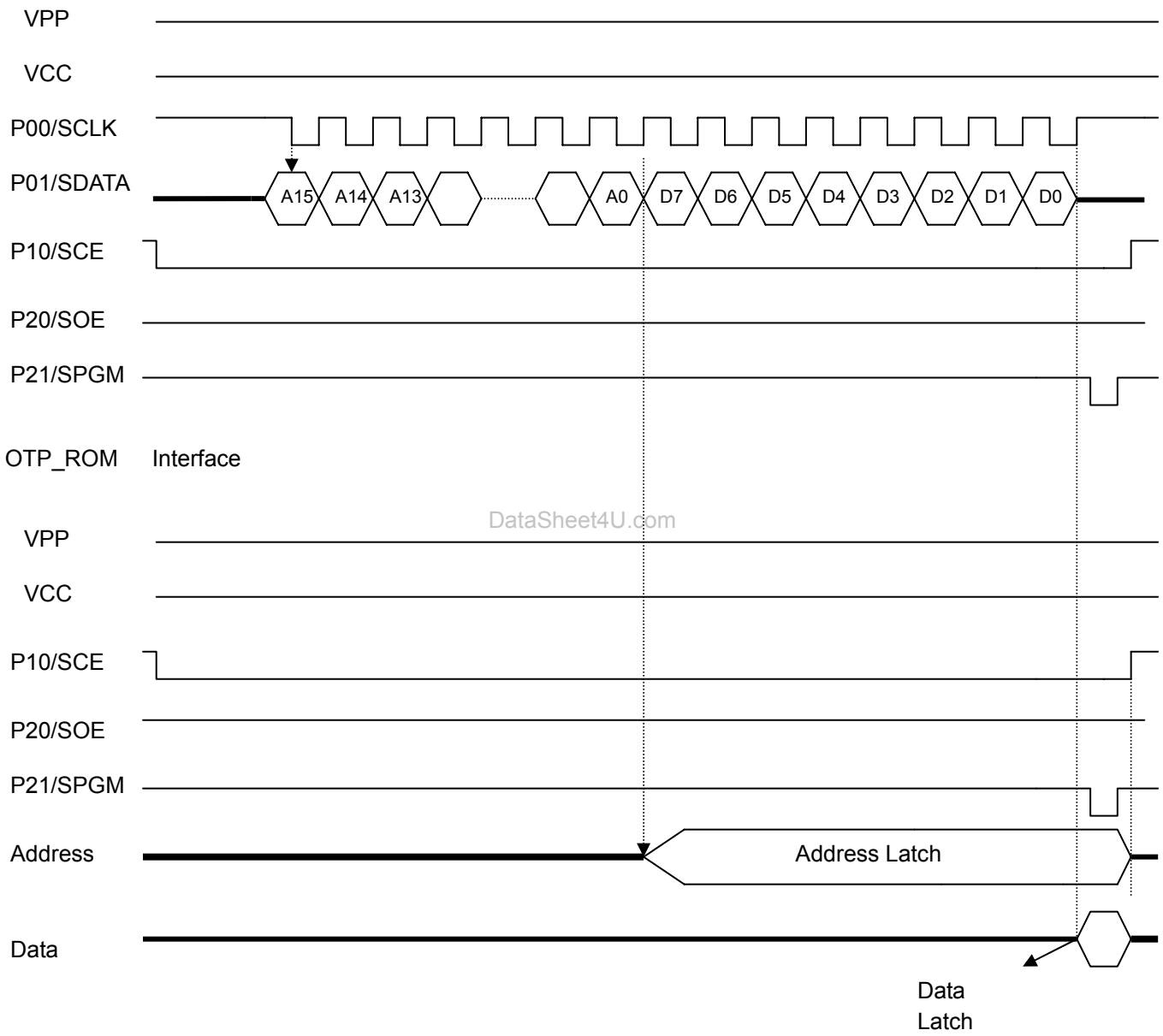
OTP_ROM Interface

Blank Check

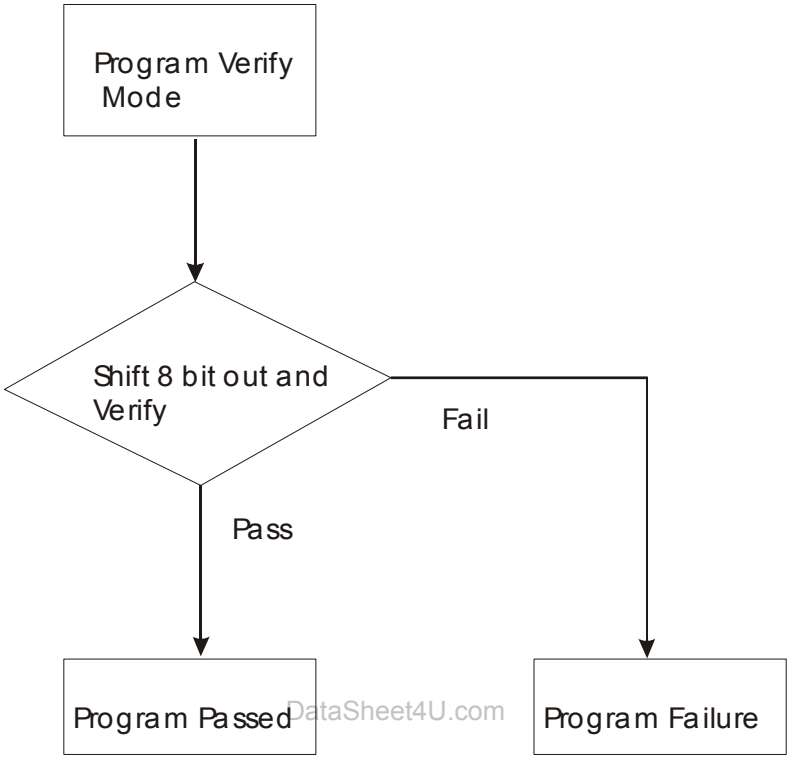


Program

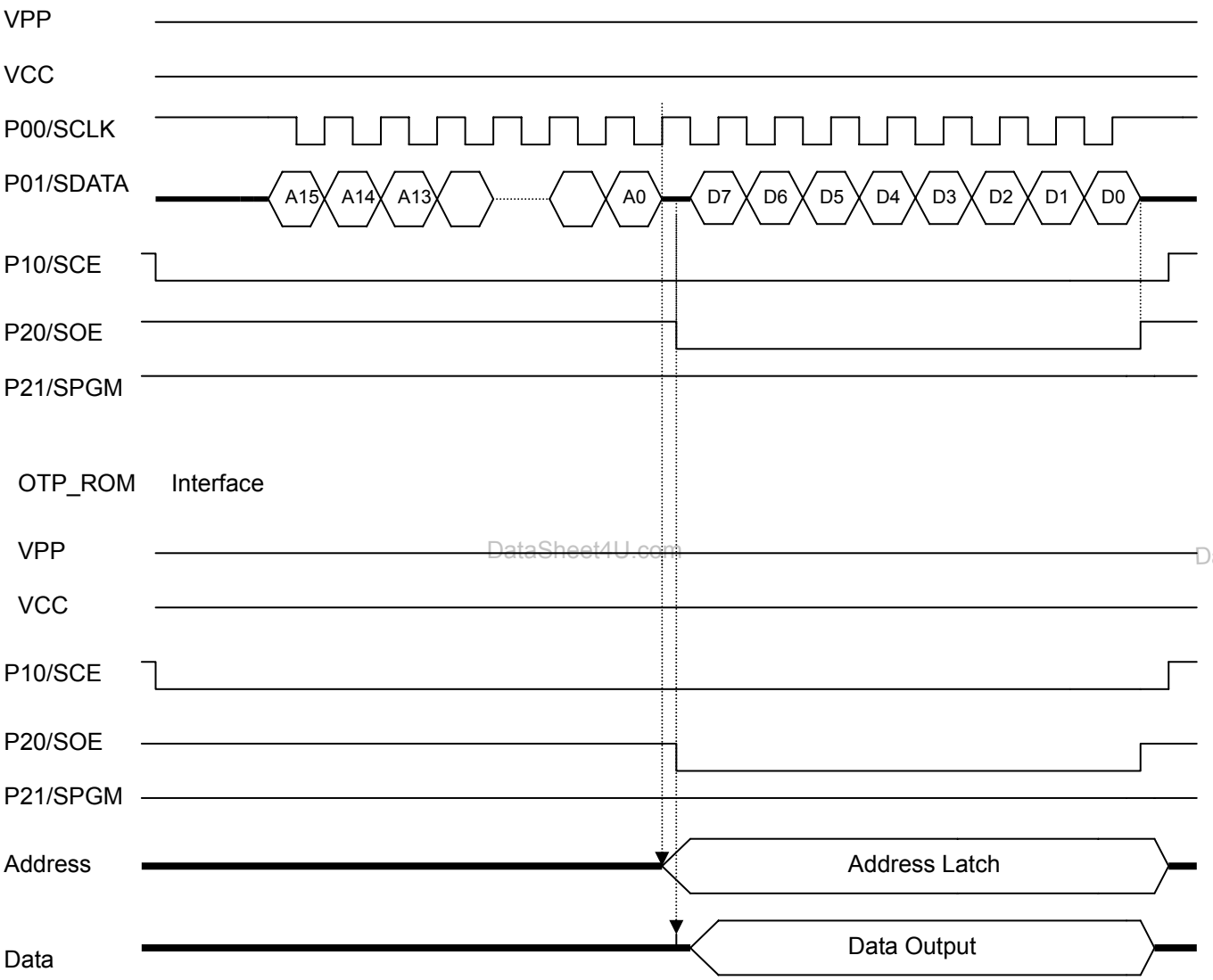
Program (VPP=12.75V VCC=6.25V)



Program Verify



Program Verify (VPP=12.75V VCC=6.25V)



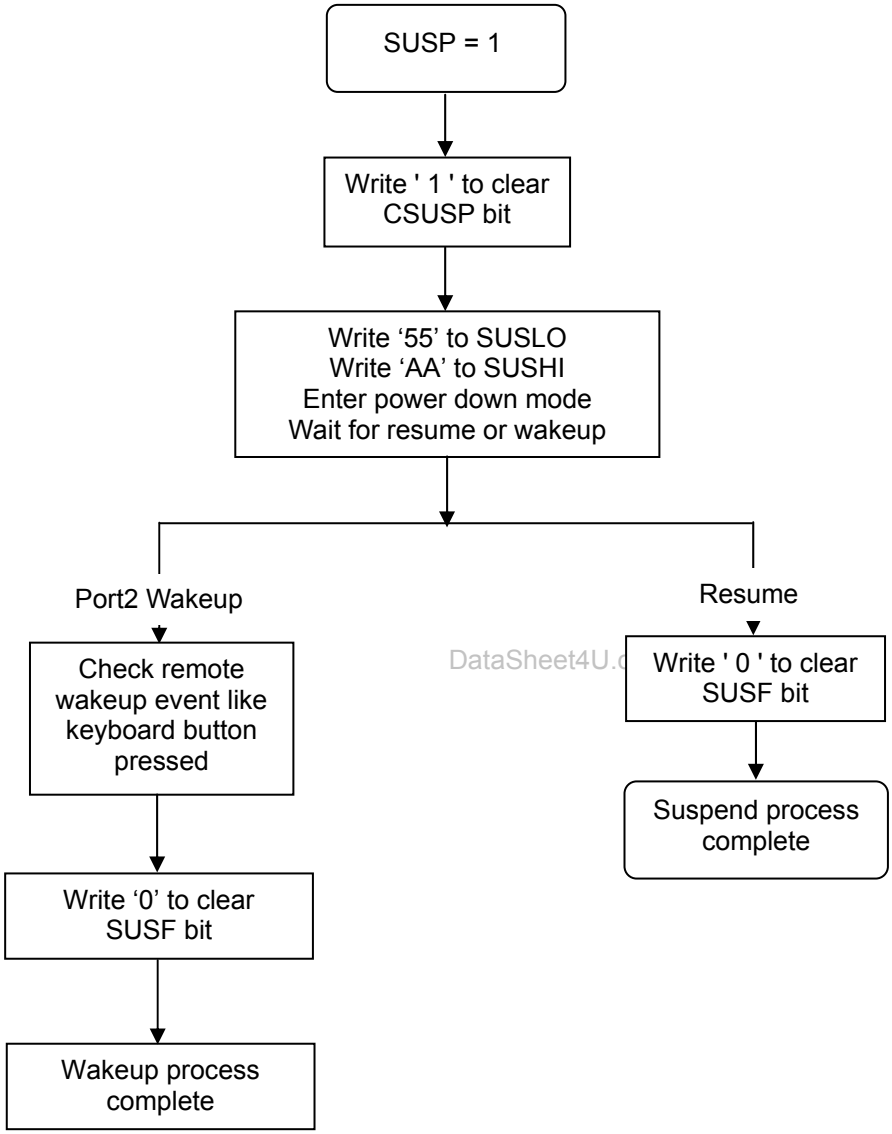
Instruction Set List

Instruction	Description	Instruction	Description
ADC	Add with Carry	LDY	Load index register
AND	Logical AND	LSR	Logical Shift Right
ASL	Arith. Shift Left	LSRA	Logical Shift Right
ASLA	Arith. Shift Left	NOP	No Operation
BBRb	Branch if Bit Reset	ORA	Logical Inclusive OR
BBSb	Branch if Bit Set	PHA	Push Accumulator
BCC	Branch if Carry Clear	PHP	Push status register
BCS	Branch if Carry Set	PHX	Push index register
BEQ	Branch if Equal	PHY	Push index register
BIT	Bit Test	PLA	Pull Accumulator
BMI	Branch if Minus	PLP	Pull status register
BNE	Branch if Not Equal	PLX	Pull index register
BPL	Branch if Plus	PLY	Pull index register
BRA	Branch Always	RMBb	Reset Memory Bit
BRK	Break(-[S]={PC+2,P})	ROL	Rotate Left
BVC	Branch if Overflw Clr	ROLA	Rotate Left Acc.
BVS	Branch if Overflw Set	ROR	Rotate Right
CLC	Clear Carry flag	RORA	Rotate Right Acc.
CLD	Clear Decimal mode	RTI	Return from Interrupt
CLI	Clear Int. disable	RTS	Return from Subr.
CLV	Clear Overflow flag	SBC	Subtract with Carry
CMP	Compare	SEC	Set Carry flag
CPX	Compare index reg.	SED	Set Decimal mode
CPY	Compare index reg.	SEI	Set Interrupt disable
DEC	Decrement	SMBb	Set Memory Bit
DEC A	Decrement Acc.	STA	Store Accumulator
DEX	Decrement index reg.	STX	Store index register
DEY	Decrement index reg.	STY	Store index register
EOR	Logical Exclusive OR	STZ	Store Zero
INC	Increment	TAX	Transfer Accumulator
INC A	Increment Acc.	TAY	Transfer Accumulator
INX	Increment index reg.	TRB	Test and Reset Bits
INY	Increment index reg.	TSB	Test and Set Bits
JMP	Jump	TSX	Transfer Stack ptr
JSR	Jump to Subroutine	TXA	Transfer index reg.
LDA	Load Accumulator	TXS	Transfer index reg.
LDX	Load index register	TYA	Transfer index reg.

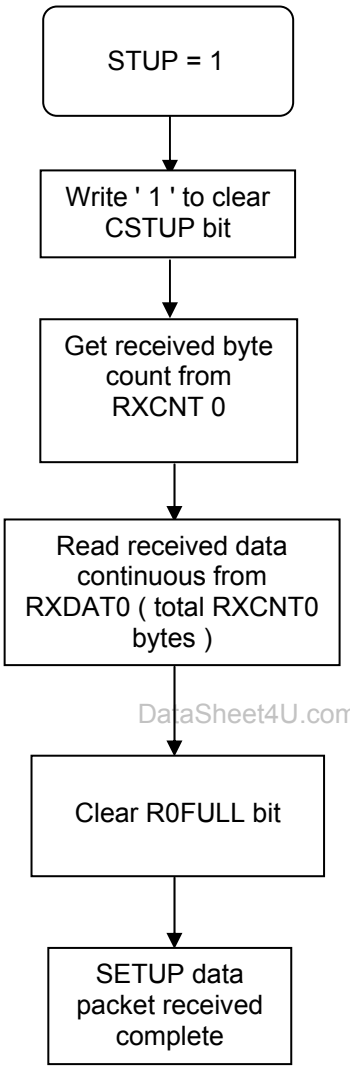
*More detailed specification please refer to 65C02 programming data book.

Firmware Programming Guide

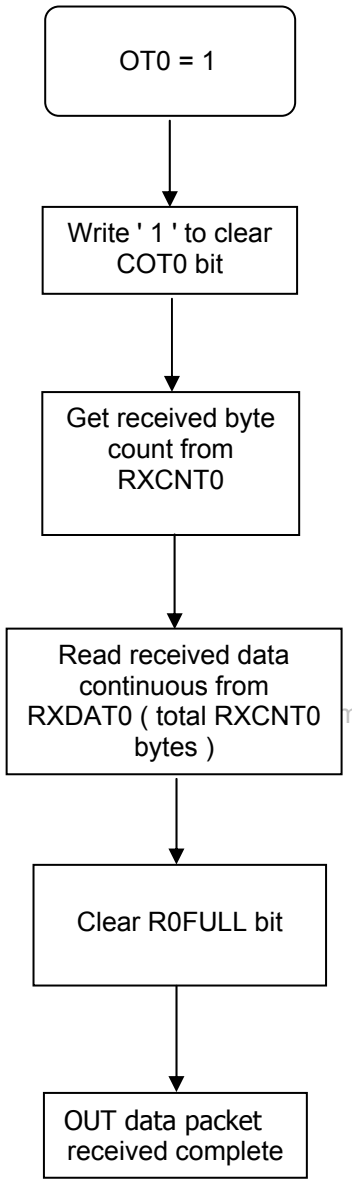
Suspend/Resume/Wakeup



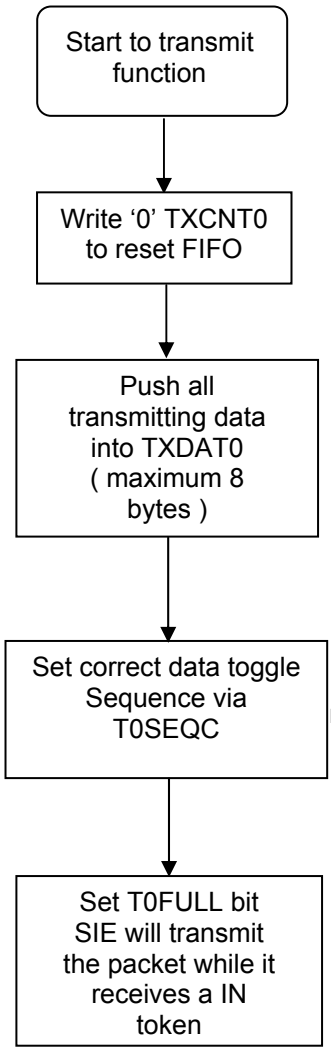
Receive Packet via Setup



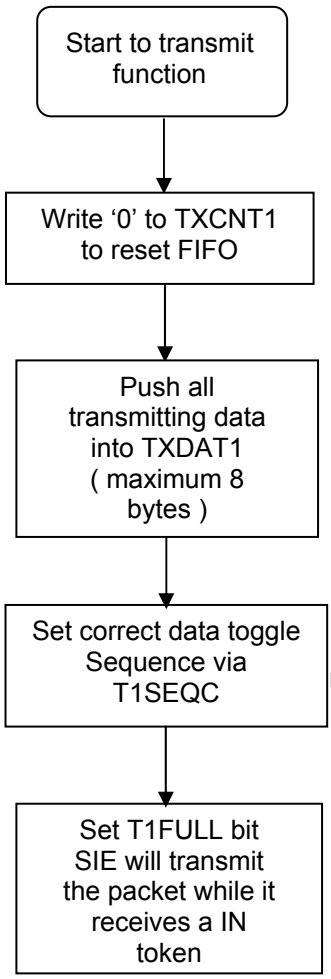
Receive Packet via Endpoint 0



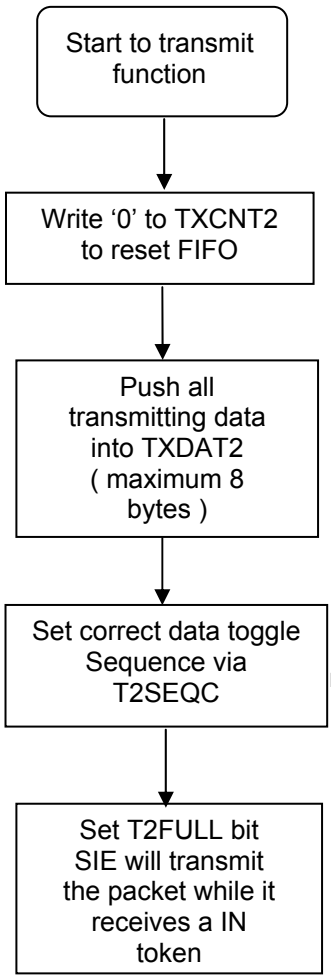
Transmit Packet via Endpoint 0



Transmit Packet via Endpoint 1



Transmit Packet via Endpoint 2



Electrical Characteristics

VDD=5V, GND=0V, TA=25℃, Fosc=6MHz

Parameters	Symbol	Min	Typ	Max	Unit	Conditions
Operating Voltage	Vdd	4.4	5	5.25	V	
Operating Current	Iop			20	mA	No load
Suspend Current	Isp			500	uA	
Input High Voltage	Vih	2			V	
Input Low Voltage	Vil			0.8	V	
Output High Voltage	Voh	2.4			V	
Output Low Voltage	Vol			0.4	V	
LED Sink Current	I led	6	10	14	mA	
Pull-up Resistance	Rup		20K		Ω	
Schmitt Tigger Input High Voltage	Vstih		1.7	2	V	
Schmitt Tigger Input Low Voltage	Vstil	0.8	1.1		V	

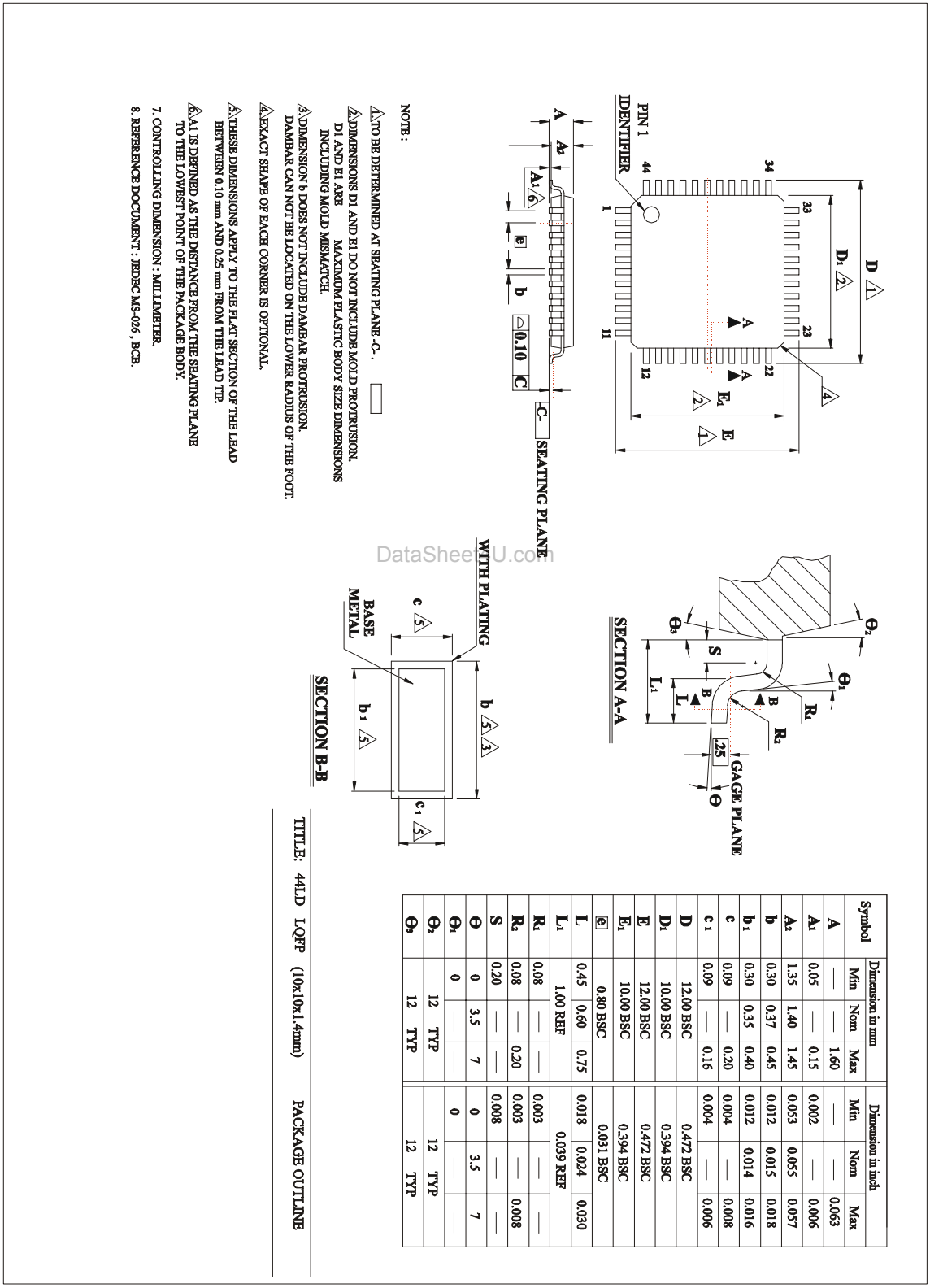
Product Matrix

Part Number	Memory		I/Os		Package Type	Operating Range
	EPROM Size	RAM Size	GPIO	ADC		
CSC0100P-L44	8K Bytes	256 Bytes	31 4 LEDs	8	LQFP-44	Commercial

Part Number	Description
CSC0100P-PG	CSC0100P Programmer

Package Outline

LQFP-44



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.30	0.37	0.45	0.012	0.015	0.018
b1	0.30	0.35	0.40	0.012	0.014	0.016
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	12.00 BSC			0.472 BSC		
D1	10.00 BSC			0.394 BSC		
E	12.00 BSC			0.472 BSC		
E1	10.00 BSC			0.394 BSC		
e	0.80 BSC			0.031 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0	3.5	7	0	3.5	7
θ1	0	—	—	0	—	—
θ2	12 TYP			12 TYP		
θ3	12 TYP			12 TYP		

NOTE :

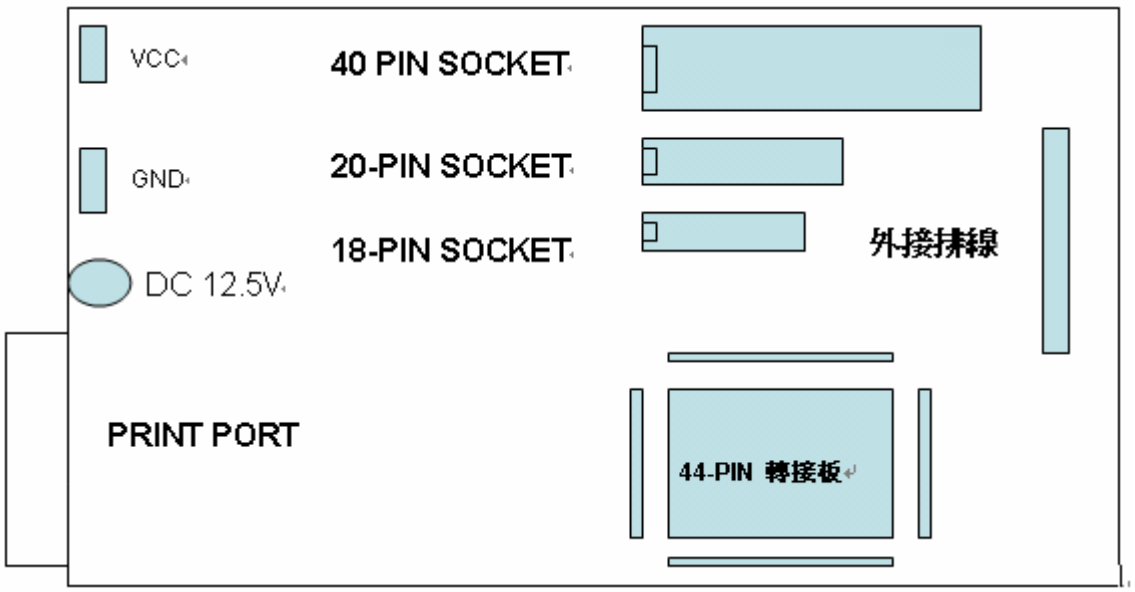
1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026 , BCB.

TITLE: 44LD LQFP (10x10x1.4mm) PACKAGE OUTLINE

Appendix

CSC0100P-PG CSC0100P Programmer Guide

Hardware Description



1. VCC input voltage = 13V ~ 15 V
2. Programmer support 40-pin DIP; 20-pin DIP; 18-pin DIP; 44-pin LQFT and 48-pin LQFP (via the adaptor) IC package type
3. Support flat cable for target board in system programming (The pin definition as indicated in the circuit)

Software Installation and User Guide

1. Boot from Win98 or DOS boot disk (included OTP.exe programmer program)
2. PC BIOS print port sets as EPP mode
3. Execute OTP.EXE, the functions are as below:

[A] **Auto < I&B&P&C>**
Proceed ID verify → Blank verify → Program → Compare
ID verify error or Blank verify error will not proceed Program

[B] **Blank verify**
Check all the EPROM data clear to 0xFF or not

[C] **Compare & display error**
Compare programmed data with the buffer data, will indicated if the data is not the same.

[D] **Display buffer**
Display the buffer data

[I] **ID verify**
Verify the ID data is 0x43H 0x59H or not.

[L] **Load BIN file to buffer**
Load the program .bin file to buffer
***The program file data is located at 0xE000 ~ 0XFFFF, the .bin file needs to move 0x0000 ~ 0x1FFFF to 0xE000 ~ 0XFFFF*

[P] **Program**
Hardware code in buffer burn into IC

[R] **Read**
Read the IC data to buffer memory

[W] **Save buffer to disk**
Save the buffer data to disk

[S] **Security**
As executed, the code on ROM can not read out of it

[Q] **Quit**
Exit the programmer program

Programmer Schematic