SHARP SERVICE MANUAL

CODE: 00ZERA440USME

ELECTRONIC CASH REGISTER

MODEL ER-A440

SRV Key : LKGIM7113RCZZ
PRINTER : DP-730

("U" & "A" version)

CAUTION
EXTREME CAUTION MUST BE TAKEN WHEN SERVICING THIS MACHINE. EVEN THOUGH THE MODE SWITCH IS IN THE OFF POSITION, VOLTAGE IS STILL SUPPLIED TO THE ENTIRE MACHINE.
WHEN WORKING ON THIS MACHINE MAKE SURE THAT THE POWER CORD IS REMOVED FROM THE WALL OUTLET.

CONTENTS

Parts marked with " " is important for maintaining the safety of the set. Be sure to replace these parts with specified ones for maintaining the safety and performance of the set.

SHARP CORPORATION

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The contents are subject to change without notice.

CHAPTER 1. SPECIFICATIONS

1. Appearance/Rating

1) Rating

Power source	AC 120 V ±10% 50/60Hz
Power consumption	Standby: 11.5 W Maximum: 40 W (max.)
Operating temperature	0°C~40°C (32°F~104°F)
Operating humidity	10%~90% (RH)
Physical dimensions, including the drawer	420(W) × 427(D) × 292(H)mm 16.5(W) × 16.8(D) × 11.5(H)in.
Weight	28.7 lbs (13 kg)

2. Keyboard

1) Standard keyboard layout

							PLU/SUB		AUTO 1	AUTO 2	TAX1 SHIFT	TAX2 SHIFT
							5	10	15	20	TAX	FS SHIFT
↑ RECEIOT	↑ JOURNAL	CASH #	CL	7	8	9	4	9	14	19	CONV	FS TEND
PCPT	PRINT	NS	@/ FOR	4	5	6	3	8	13	18	CHK	CH
⊖	#	RA	RFND	1	2	3	2	7	12	17	MDSE SBTL	SBTL
%1	%2	PO	VOID	0	00	•	1	6	11	16	CA/AT	

Fig. 2-1

2) Key top name

① Standard Key Top

KEY TOP	DESCRIPTION
0 to 9,00	Numeric keys
•	Decimal point key
CL	Clear key
@/FOR	Multiplication/split-pricing key
1 to 20	Department 1 to 20 keys
↑R	Receipt Paper Feed key
↑J	Journal Paper Feed key
RCPT	Receipt print & on/off key
#	Non-Add Code key
AUTO 1, 2	Automatically Entry key 1, 2
CASH #	Cashier code entry key
NS	No Sales key
⊖	Discount key
% 1, 2	% key 1, 2
PO 1, 2	Paid Out key
RA	Received on Account key
VOID	Void key
PLU/SUB	PLU/Subdept code entry key
SBTL	Subtotal key
CH	Charge key
CA/AT	Cash/amount tendered
TAX1 SHIFT	TAX1 shift key
TAX2 SHIFT	TAX2 shift key
TAX	Tax key

KEY TOP	DESCRIPTION
PRINT	Validation print key
RFND	Refund key
CONV	Currency conversion key
CHK	Check key
MDSE SBTL	Merchandise subtotal key
FS SHIFT	Food stamp shift key
FS TEND	Food stamp tendered key

② Optional Key Top

KEY TOP	DESCRIPTION
% 3, 4	% key 3, 4
⊖2, 3, 4	Discount key 2, 3, 4
AUTO 3 ~ 10	Automatically entry key 3 ~ 10
CA 2	Cash total 2 key
CH 2 ~ 5	Charge key 2 ~ 5
CR 3, 4	Credit key 3, 4
21 to 50	Department 21 to 50 key
TAX3 SHIFT	TAX3 shift key
TAX4 SHIFT	TAX4 shift key
RA2	Received on account key 2
PO2	Paid out key 2
CONV2 ~ 4	Currency conversion key 2 ~ 4
CHK2	Check key 2
RFND SALE	Refund sales key
BIRTH	Birthday key
1 to 68	Direct price lookup/Subdepartment keys

3. Mode switch

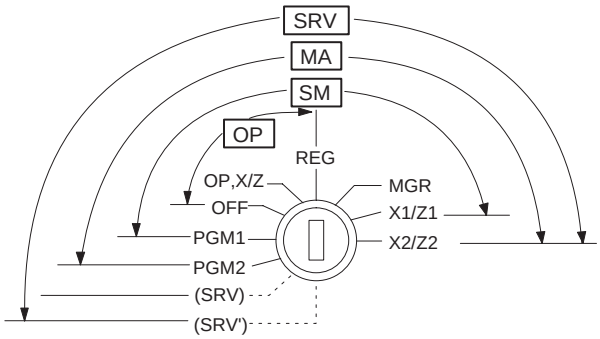


Fig. 3-1

* The key can be removed in the REG or OFF position.
* In the SRV' mode, key inputs are prohibited and no display is made.
* With the key in the off position power is not supplied to the main PWB.

[Functions]

- Function for each key position
- SRV': System reset
- SRV: Service mode (Service programming)
- PGM2: Allows programming of an item that is not changed frequently, in addition to the PGM1 mode programming.
- PGM1: Allows programming of items frequently changed (e.g. department, PLU pricing, and discount rate setting).
- OP, X/Z: Allows X or Z operation by servers or cashiers.
- REG: Allows registrations.
- MGR: Allows the operations, by authorized person such as a manager (e.g. correction after transaction finished or cancellation of entry limits), which are not permitted to ordinary cashiers.
- X1/Z1: Allows reading and resetting of a day's sales total.
- X2/Z2: Allows reading or resetting sales totals in a specified period.
- OFF: Switching off the display to prevent key board entries. (The setting turn off the AC power.)

4. Display

1) Layout

① Operator display

Fig. 4-1

	7 segment display (LED)
No. of positions	10
Color of display	Yellow Green
Character size	14.2 (H) × 8.0 (W) mm

② Customer display (Pop-up display)

Fig. 4-2

	7 segment display (LED)
No. of positions	7
Color of display	Yellow Green
Character size	14.2 (H) × 8.0 (W) mm

Display contents

	Display Position	Description
Amount	1-8	
Minus sign	4-10	–: Floating
Error	10	E
PGM Mode	10	P
VOID Mode	10	u
CA/AT CHK, CR	10	F: Lights up when a registration is finalized by depressing CA/AT, CHK, CR key
SUB TOTAL/ short tender	10	o
Change	10	C: Light up whenever the change due amount appears in the display.
Department	9-10	No zero-suppressed
PLU	5-10	No zero-suppressed
Repeat	8	Endless count, starting from 2.
Decimal point	3-1	TAB
Receipt OFF	9	(–)
Cashier No.	2-3	–xx–: free code
VP compulsory	10	U: Light up when the validation printing is compulsory
Sentinel	10	Light up the decimal point

5. Printer (DP-730)

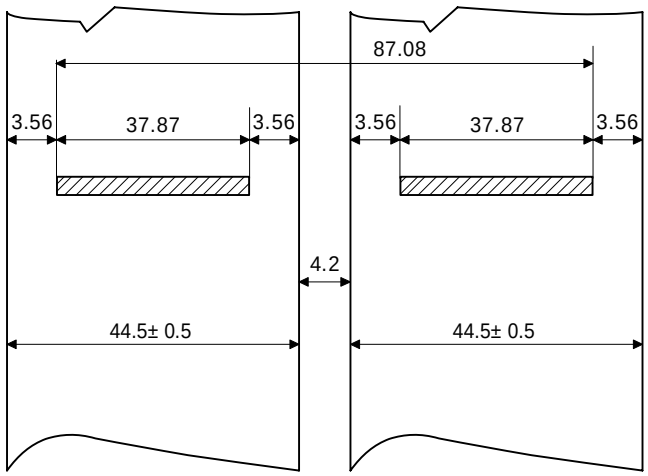
1) Specifications

- Part number: DP-730
- No. of stations: 2
- Printing system: Mechanical serial dot
- Direction of printing: Bidirectional
- Printing capacity: Receipt – 24 characters
  Journal – 24 characters
  Validation – 55 characters (one line only)
- Character size: 1.36 (W) × 2.75 (H) mm at 7 × 7 dots
  Print pitch:
  Column distance 1.59 mm
  Row distance 5.08 mm
- Total number of dots: Receipt – 108 dots/216 positions
  Journal – 108 dots/216 positions
  Validation – 248 dots/495 positions
- Font: 7 × 7 dots (including half dot)
  Space between characters – 1 dot (2 positions)

- Distance between dots: 0.353 mm (H) × 0.353 mm (W)
- Journal near end sensor: Service route option
- Print speed: Approx. 3.0 lines/sec.
- Paper feed speed: Receipt – Approx. 30 lines/sec.
  Journal – Approx. 30 lines/sec.
- Reliability: MCBF – 4 million lines (excluding the print head)
  Head life – 50 million characters (at 4 dots/1 character/ 1 pin)
- Validation form sensor: Not setup

2) Printing area

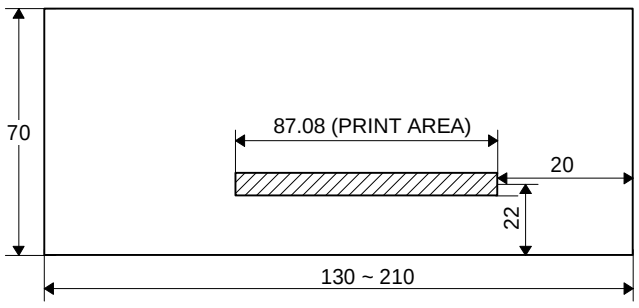
Receipt/journal



Unit : mm

Fig. 5-1

Validation form



Unit : mm

Fig. 5-2

3) Paper

- Paper roll dimensions: 44.5±0.5mm in width, 83mm in diameter
- Paper quality: Journal

  Bond paper (paper thickness: 0.06 to 0.09mm, paper weight: 52.3 to 64g/m^2)

  Validation form
  Thickness: 0.07 to 0.14mm

  Size: 130mm or more (W) × 70mm or more (H)

4) Inking

- Ink supply system: Ink ribbon
- Form: Cartridge/Endless ribbon
- Specification: Material – Nylon
- Ribbon life: Approx. 6 million characters
- Print color: Purple (single color)

5) Logo stamp: None

6) Cutter

- Method: Manual

6. Drawer

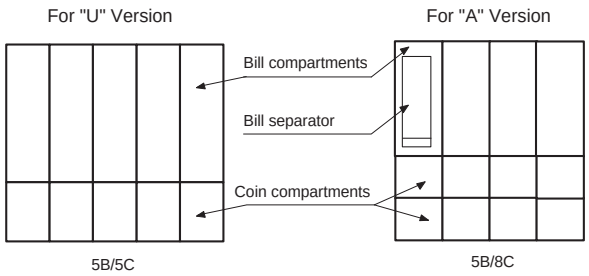
1) Specification

(1) Drawer box and drawer

Model name	SK-423
Size	420 (W) × 427 (L: included lock key) × 112 (H: included rubber leg)
Color	GRAY 368
Material	Metal
Bell	—
Release lever	Standard equipment; Situated at the bottom
Drawer open sensor	Standard equipment

2) Money case

	For "U" version	For "A" version
Separation from the drawer	Allowed	Allowed
Separation of the coin compartments from the money case	Disallowed	Disallowed
Bill separator	—	YES
Number of compartments	5B/5C	4B/8C



3) Lock

Location of the lock	Front	
Method of locking and unlocking	Locking:	Insert the drawer lock key into the lock and turn it 90 degrees counterclockwise.
	Unlocking:	Insert the drawer lock key into the lock and turn it 90 degrees clockwise.
Key No.	SK1-1	

CHAPTER 2. OPTIONS

1. System configuration

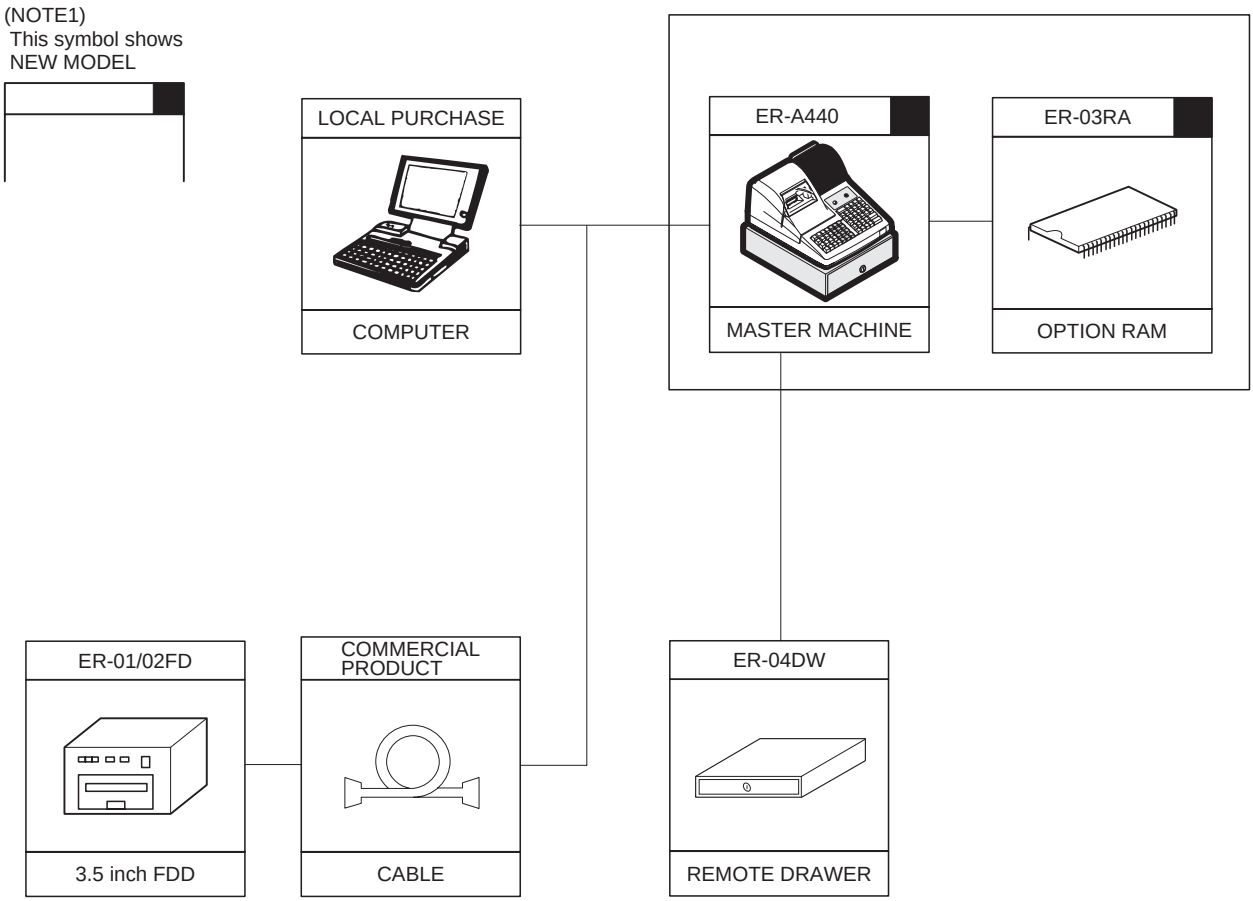


Fig. 1-1

2. Options

No.	NAME	MODEL	DESCRIPTION
1	EXPANSION RAM CHIP	ER-03RA	512K bytes RAM CHIP
2	REMOTE DRAWER	ER-04DW	
3	PRESETS LOADER	ER-01FD/02FD	FD unit
4	KEY TOP KIT	ER-11KT7	1 × 1 KYE TOP UNIT
		ER-12KT7	1 × 2 KYE TOP UNIT
		ER-22KT7	2 × 2 KYE TOP UNIT
		ER-11DK7G	1 × 1 DUMMY KYE KIT
		ER-51DK7G	5 × 1 DUMMY KYE KIT
5	COIN CASE	ER-55CC2	for "U" version
6	COIN CASE	ER-48CC2	for "A" version

3. Service options

No.	NAME	PARTS CODE	PRICE RANK	DESCRIPTION
1	SERVICE KEY	LKGiM7113RCZZ	AF	
2	MODE KEY GRIP COVER	LKGiM7126RCZZ	AL	OP key only
3	DRIP-PROOF KEYBOARD COVER	GCŌVH7126BHZZ	BE	Include the switch cover
4	JOURNAL NEAR END SENSOR	DUNTK3677BH03	BB	
5	TEXT PRESET KEYBOARD COVER	GCŌVB7153BHZZ	BH	

4. Service tools

No.	NAME	PARTS CODE	PRICE RANK	DESCRIPTION
1	RS-232 LOOP BACK CONNECTOR	UKŌG-6705RCZZ	BU	
2	KEY TOP REMOVER	UKŌG-6725BHZZ	BB	

5. Supplies

No.	NAME	PARTS CODE	PRICE RANK	DESCRIPTION
1	ROLL PAPER	DPAPR1006CSZZ	AR	5 roll/pack
2	INK LIBBON	PRBN-6644RCZZ	AZ	

6. Options

For installation of the options, refer to the Installation Manual which is issued separately.

CHAPTER 3. SRV. RESET AND MASTER RESET

1. SRV. reset (Program Loop Reset)

Used to return the machine back to its operational state after a lock-up has occurred.

Procedure

- Method 1
  1) Unplug the AC cord from the wall outlet.
  2) Set the mode switch to (SRV′) position.
  3) Plug in the AC cord to the wall outlet.
  4) Turn to (SRV) position from (SRV′) position.
- Method 2
  1) Set the mode switch to PGM2 position.
  2) Turn off the AC switch.
  3) While holding down JOURNAL FEED key and RECEIPT FEED key, Turn on the AC switch.

Note: When disassembling and reassembling always power up using method 1 only. Method 2 will not reset the CKDC8.

Note: SRV programming job#926-B must be set to "4" to allow PGM program loop reset.

2. Master reset (All memory clear)

There are two possible methods to perform a master reset.

- MRS-1

Used to clear all memory contents and return machine back to its initial settings and return keyboard back to default keyboard layout.

Procedure

1) Unplug the AC cord from the wall outlet.
2) Set the MODE switch to the (SRV′) position.
3) Plug in the AC cord to the wall outlet.
4) While holding down JOURNAL FEED key, turn to (SRV) position from (SRV′) position.

- MRS-2

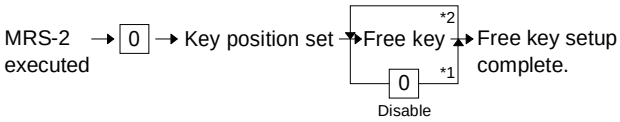
  Used to clear all memory and keyboard contents.
  This reset returns all programming back to defaults. The keyboard must be entered by hand.
  This reset is used if an application needs different keyboard layout other than that supplied by a normal MRS-1.

Procedure

1) Unplug the AC cord from the wall outlet.
2) Set the MODE switch to the (SRV′) position.
3) Plug in the AC cord to the wall outlet.
4) While holding down JOURNAL FEED key and RECEIPT FEED key, turn to (SRV) position from (SRV′) position.
5) Key position assignment:

✳ After the execution of MRS-2, only the RECEIPT FEED and JOURNAL FEED keys can remain effective on key assignment. Any key can be assigned on any key position on the main keyboard.

[key setup procedure]



NOTES:

✳1: When the 0 key is pressed, the key of the key number on display is disabled.

✳2: Push the key on the position to be assigned. With this, the key of the key number on display is assigned to that key position.

Key number	Key name	Key number	Key name
1	Numeric key "0"	10	Numeric key "9"
2	Numeric key "1"	11	Numeric key "00"
3	Numeric key "2"	12	Numeric key "000"
4	Numeric key "3"	13	Decimal point key
5	Numeric key "4"	14	CL key
6	Numeric key "5"	15	@/FOR key
7	Numeric key "6"	16	SBTL key
8	Numeric key "7"	17	CA/AT key
9	Numeric key "8"		

CHAPTER 4. HARDWARE DESCRIPTION

1. Hard ware block diagram

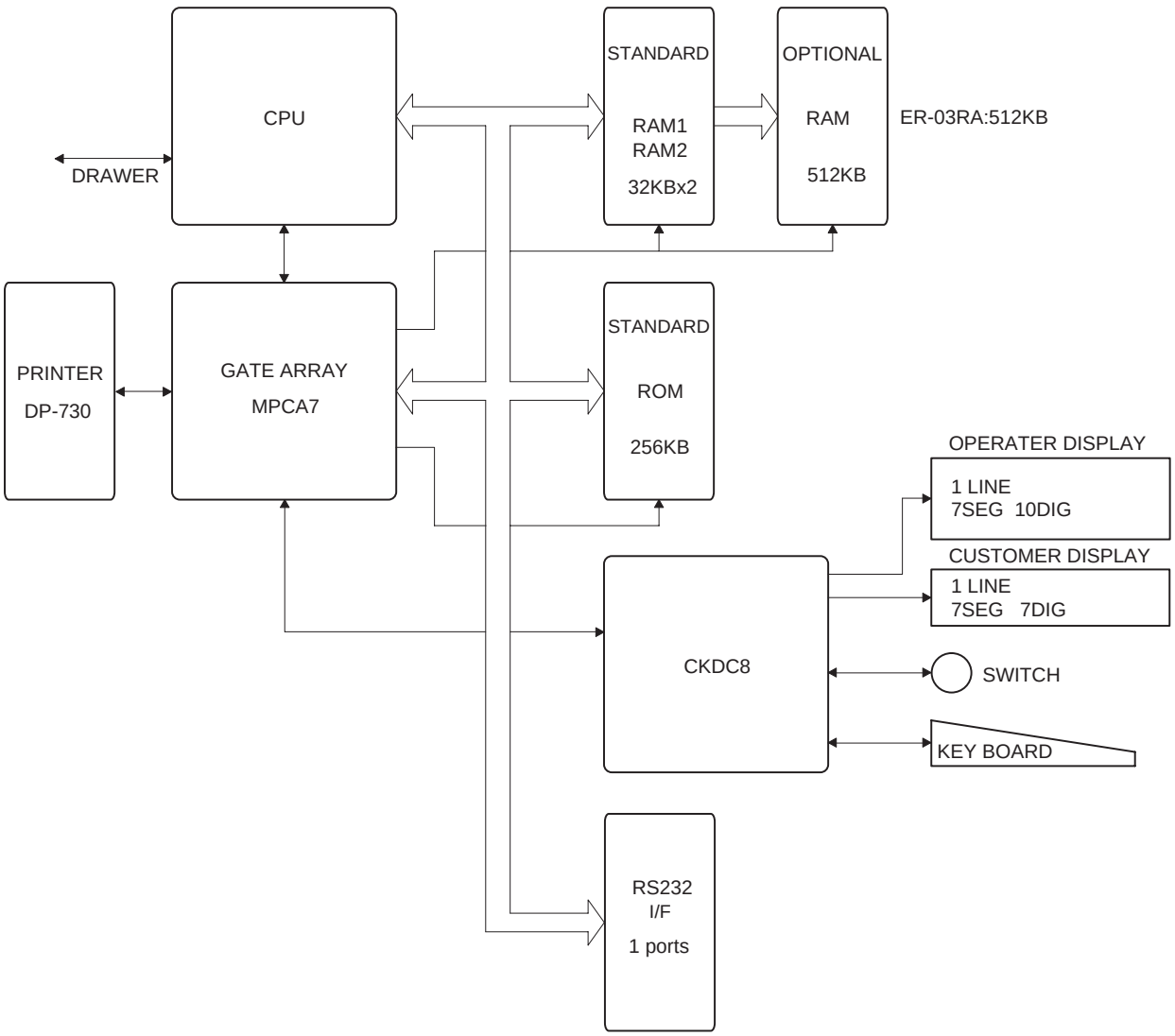
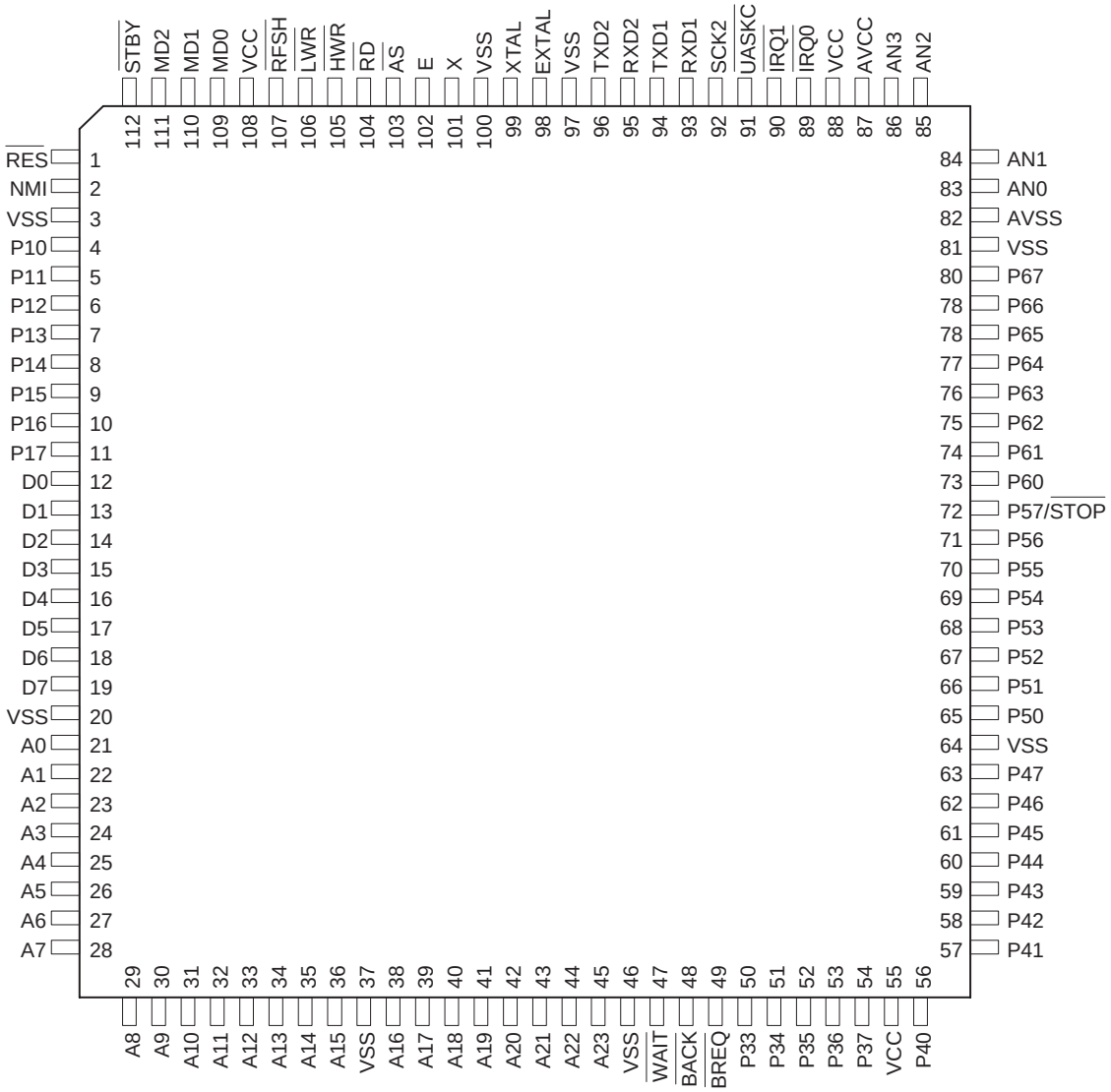


Fig. 1-1

2. Description of main LSI's

2-1. CPU (HD6415108-10)

1) Pin configuration



HD6415108-10 pin configuration

Fig. 2-1

2) Block diagram

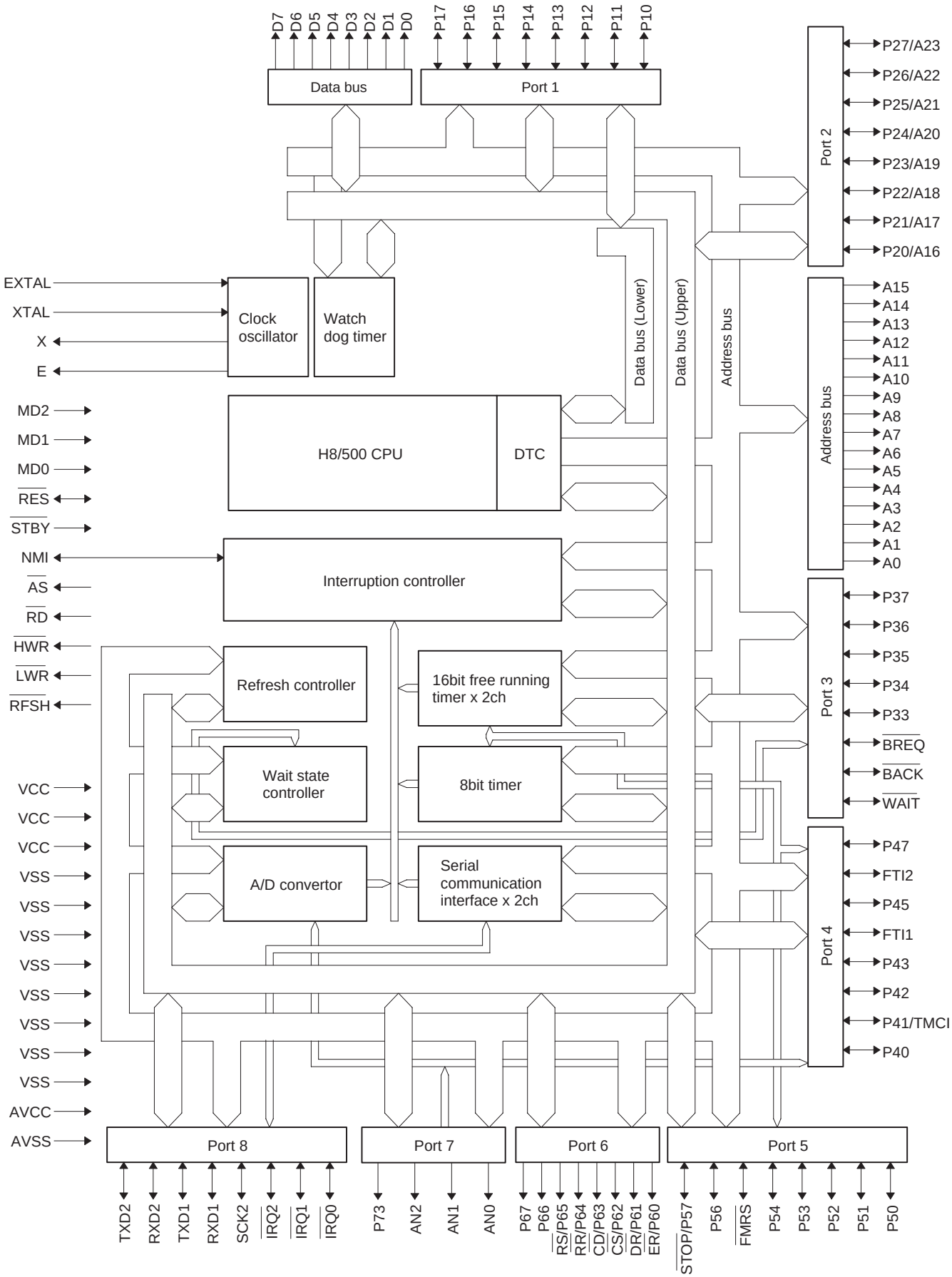


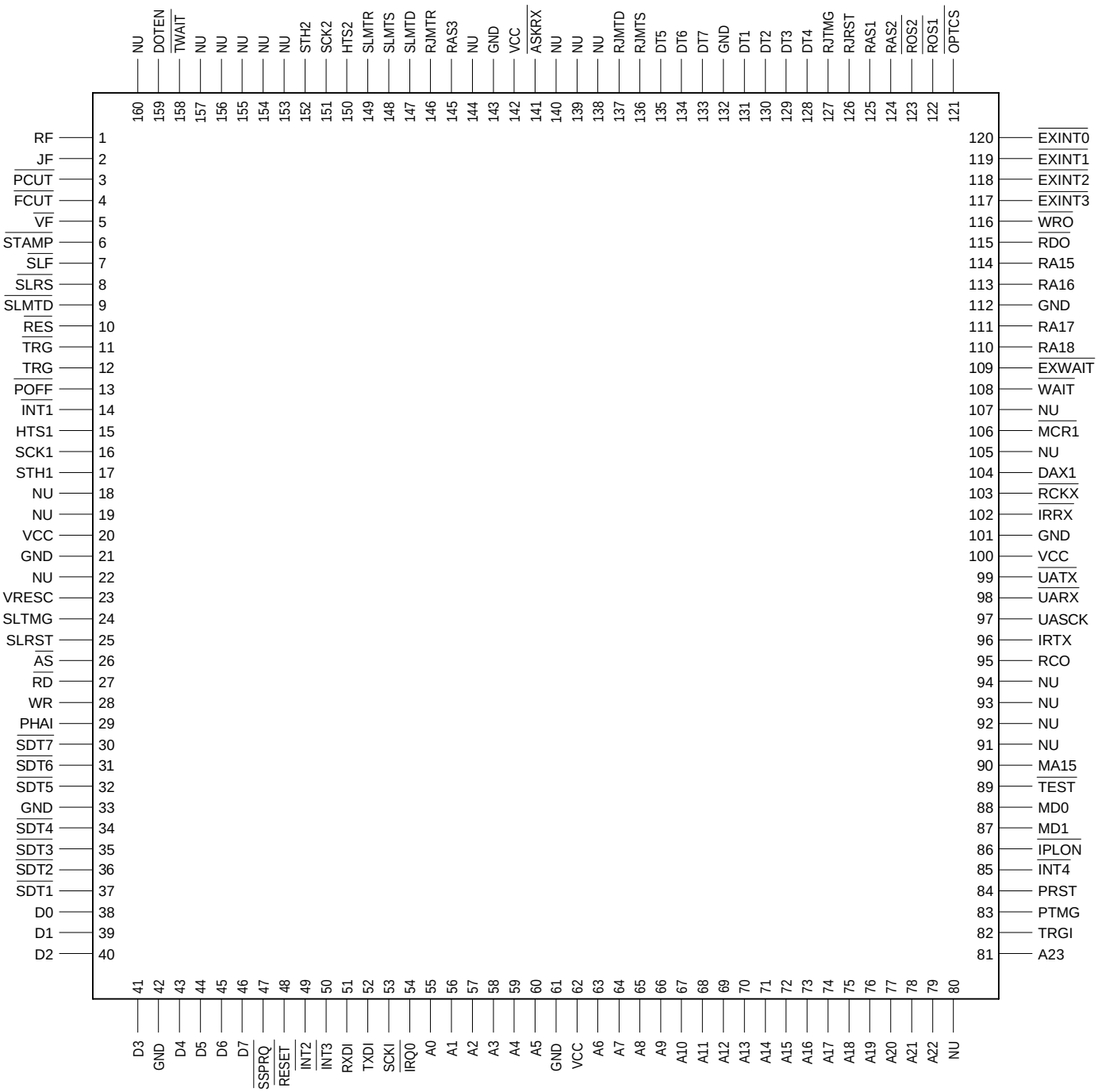
Fig. 2-2

3) Pin description

PIN No.	SYMBOL	SIGNAL NAME	IN/ OUT	FUNCTION
1	/RES	/RESET	IN	RESET INPUT from CKDC WUTH BUFFER
2	NMi	NMi	IN	NON-MASKABLE INTERRUPT INPUT FOR SSP INTERRUPT INPUT
3	VSS	VSS		GND
4	P10	ERC	OUT	EVENT READ CANCEL (to CKDC)
5	P11	LDRQ	OUT	LOAD REQUEST (to CKDC)
6	P12	/SHEN	IN	SHIFT ENABLE (from CKDC)
7	P13	/FRES	OUT	FISCAL MEMORY RESET (NU)
8	P14	BUSY	IN	FISCAL MEMORY BUSY (NU) Pull-up
9	P15	/RDY	IN	FISCAL MEMORY READY (NU) Pull-up
10	P16	PDS	IN	POP-UP DISPLAY SENSOR (NU) Pull-up
11	P17		IN	GND Nu
12	D0	D0	I/O	DATA BUS 0
13	D1	D1	I/O	DATA BUS 1
14	D2	D2	I/O	DATA BUS 2
15	D3	D3	I/O	DATA BUS 3
16	D4	D4	I/O	DATA BUS 4
17	D5	D5	I/O	DATA BUS 5
18	D6	D6	I/O	DATA BUS 6
19	D7	D7	I/O	DATA BUS 7
20	VSS	VSS		GND
21	A0	A0	OUT	ADDRESS BUS 0
22	A1	A1	OUT	ADDRESS BUS 1
23	A2	A2	OUT	ADDRESS BUS 2
24	A3	A3	OUT	ADDRESS BUS 3
25	A4	A4	OUT	ADDRESS BUS 4
26	A5	A5	OUT	ADDRESS BUS 5
27	A6	A6	OUT	ADDRESS BUS 6
28	A7	A7	OUT	ADDRESS BUS 7
29	A8	A8	OUT	ADDRESS BUS 8
30	A9	A9	OUT	ADDRESS BUS 9
31	A10	A10	OUT	ADDRESS BUS 10
32	A11	A11	OUT	ADDRESS BUS 11
33	A12	A12	OUT	ADDRESS BUS 12
34	A13	A13	OUT	ADDRESS BUS 13
35	A14	A14	OUT	ADDRESS BUS 14
36	A15	A15	OUT	ADDRESS BUS 15
37	VSS	VSS		GND
38	A16	A16	OUT	ADDRESS BUS 16
39	A17	A17	OUT	ADDRESS BUS 17
40	A18	A18	OUT	ADDRESS BUS 18
41	A19	A19	OUT	ADDRESS BUS 19
42	A20	A20	OUT	ADDRESS BUS 20
43	A21	A21	OUT	ADDRESS BUS 21
44	A22	A22	OUT	ADDRESS BUS 22
45	A23	A23	OUT	ADDRESS BUS 23
46	VSS	VSS		GND
47	/WAIT	/WAIT	IN	Wait signal from MPCA
48	/BACK	/BACK	OUT	Bus control request acknowl edge (Nu)
49	/BREQ	/BREQ	IN	Bus control request (Nu) pull-up
50	P33	DOPS	IN	Drawer open sencer signal
51	P34	/DR0	OUT	Drawer open drive signal
52	P35	/DR1	OUT	Option drawer 1 drive signal
53	P36	NU	IN	(Nu) GND
54	P37	NU	IN	(Nu) GND
55	VCC	VCC		+5V
56	P40	/IFV	IN	Slip printer enable (Nu) pull-up
57	P41	/PTMG	IN	Printer (Dp-730) timing signal from MPCA
58	P42	/TOF	IN	Slip TOF signal (Nu) pull-up
59	P43	/BOF	IN	Slip BOF signal (Nu) pull-up
60	P44	/PRST	IN	Printer (Dp-730) Reset signal from MPCA
61	P45	/NEJ	IN	Near END signal jounal
62	P46		IN	CKDC interface shift enable signal (NU) GND
63	P47	/NER	IN	Near END signal receipt
64	VSS	VSS		GND
65	P50	TRG1	OUT	Dot pulse adjust signal
66	P51	/PSTOP	OUT	Nu
67	P52	/CKDCR2	OUT	Nu
68	P53	OPDS	IN	Nu (GND)
69	P54	FVPON	OUT	Nu
70	P55	FMRS	IN	Nu (GND)
71	P56	/SLIPLMP	OUT	Nu
72	P57	/STOP	OUT	Nu
73	P60	/ERS	OUT	ER signal for RS232 (Equipment Ready)
74	P61	/DRS	IN	DR signal for RS232 (Data set Ready)
75	P62	/CSS	IN	CS signal for RS232 (Clear to Send)
76	P63	/CDS	IN	CD signal for RS232 (Carrier Detect)
77	P64	/RR	OUT	RR signal for RS232 (Ready to Receive) (Nu)
78	P65	/RSS	OUT	RS signal for RS232 (Request to Send)
79	P66	(/RI), /CI	IN	CI signal for RS232 (Calling Indicator)
80	P67	HP	IN	Printer (Dp-730) Home position pulse
81	VSS	VSS		GND
82	AVSS	AVSS	IN	GND
83	P70	VPJ	IN	Validation sensor journal (NU) GND
84	P71	VPR	IN	Validation sensor receipt (NU) GND
85	P72	VPTEST	IN	+24V test input
86	P73		IN	Validation sense signal (Nu) GND
87	AVCC	AVCC	IN	+5V
88	VCC	VCC		+5V
89	P80	/iRQ0	IN	Interrupt signal 0 from MPCA
90	P81	/iRQ1 (/RSRQ)	IN	Interrupt signal from OPTION PWB
91	P82	/iRQ2	IN	Interrupt signal (Nu) pull-up
92	P83	SCK2	OUT	CKDC & FMC i/F sync shift clock
93	P84	RXD	IN	RS232C RECEIVE DATA
94	P85	TXD	OUT	RS232C SEND DATA
95	P86	RXD2	IN	CKDC, Fiscal memory unit I/F shift input data
96	P87	TXD2	OUT	CKDC, Fiscal memory unit I/F shift output data
97	VSS	VSS		GND
98	EXTAL	EXTAL	IN	X-TAL (14.7456MHz)
99	XTAL	XTAL	IN	X-TAL (14.7456MHz)
100	VSS	VSS		GND
101	ϕ	ϕ	OUT	System clock (7.3728MHz)
102	E		OUT	E clock (NU)
103	/AS	/AS	OUT	Address strobe
104	/RD	/RD	OUT	Read
105	/HWR	/WR	OUT	Write
106	/LWR		OUT	Nu
107	/RFSH	/RFSH	OUT	Refresh cycle (NU)
108	VCC	VCC		+5V
109	MD0	MD0	IN	+5V (MODE 3)
110	MD1	MD1	IN	+5V (MODE 3)
111	MD2	MD2	IN	GND (MODE 3)
112	/STBY	/STBY	IN	+5V (Nu)

2-2. G.A (MPCA7)

1) Pin configuration



GATE ARRAY (LZ9AH39)
MPCA7

Fig. 2-3

2) Block diagram

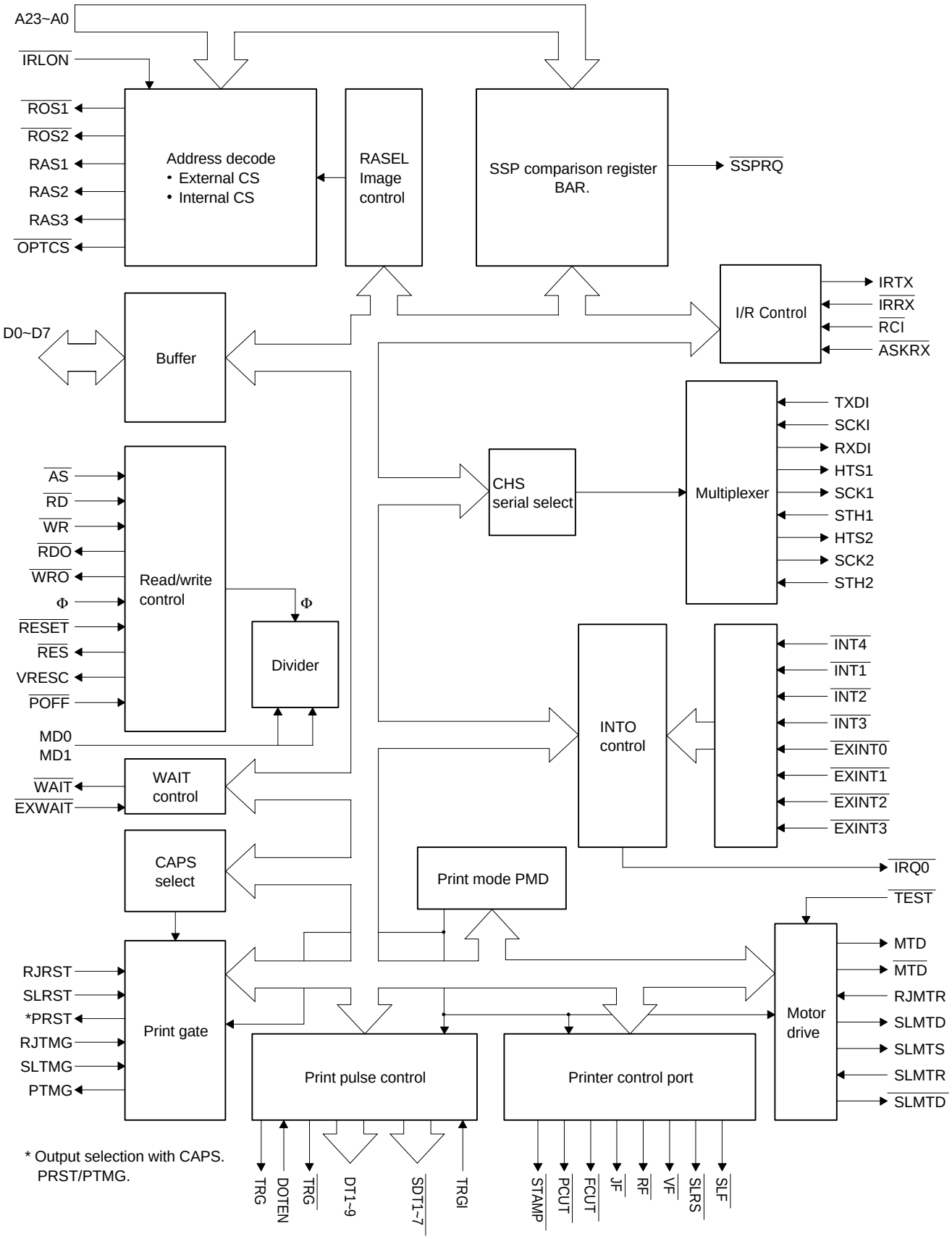


Fig. 2-4

3) Pin description

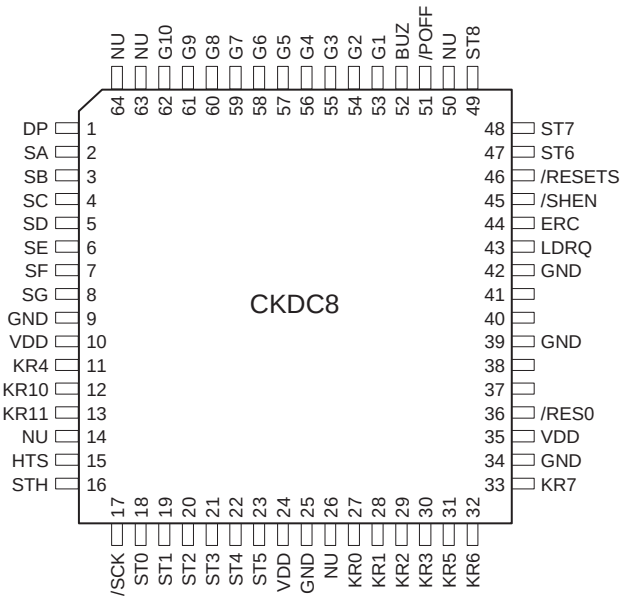
Pin No.	Signal name	In/ Out	Function
1	RF	Out	Receipt side paper feed solenoid
2	JF	Out	Journal side paper feed solenoid
3	$\overline{\text{PCUT}}$	Out	Printer partial cut signal (NU)
4	$\overline{\text{FCUT}}$	Out	Printer auto cut signal (NU)
5	$\overline{\text{VF}}$	Out	Multi line validation paper feed (NU)
6	$\overline{\text{STAMP}}$	Out	Printer stamp signal (NU)
7	$\overline{\text{SLFS}}$	Out	Slip printer paper feed singnal (NU)
8	$\overline{\text{SLRS}}$	Out	Slip printer release signal (NU)
9	$\overline{\text{SLMTD}}$	Out	Slip printer motor drive signal (NU)
10	$\overline{\text{RES}}$	Out	Peripheral output reset
11	$\overline{\text{TRG}}$	Out	Dot head trigger signal (NU)
12	TRG	Out	Dot head trigger signal
13	$\overline{\text{POFF}}$	In	Power off signal input
14	$\overline{\text{INT1}}$	In	(NU)
15	HTS1	Out	8 bit serial port output (for CKDC8)
16	SCK1	Out	Serial port shift clock output (for CKDC8)
17	STH1	In	8 bit serial port input (for CKDC8)
18	RAS VZ	—	Chip select (NU)
19	—	—	Nu
20	VCC	—	+5V
21	GND	—	GND
22	INTMCR	—	Interrupt (NU)
23	VRESC	Out	Turns active when reset and power down is met
24	SLTMG	In	Slip printer timing signal (NU)
25	SLRST	In	Slip printer reset signal (NU)
26	$\overline{\text{AS}}$	In	Address strobe
27	$\overline{\text{RD}}$	In	Read strobe
28	$\overline{\text{WR}}$	In	Write strobe
29	ϕ	In	(ϕ) System clock (7.3728 MHz)
30	$\overline{\text{SDT7}}$	Out	Slip printer printhead drive signal (dot7) (NU)
31	$\overline{\text{SDT6}}$	Out	Slip printer printhead drive signal (dot6) (NU)
32	$\overline{\text{SDT5}}$	Out	Slip printer printhead drive signal (dot5) (NU)
33	GND	—	GND
34	$\overline{\text{SDT4}}$	Out	Slip printer printhead drive signal (dot4) (NU)
35	$\overline{\text{SDT3}}$	Out	Slip printer printhead drive signal (dot3) (NU)
36	$\overline{\text{SDT2}}$	Out	Slip printer printhead drive signal (dot2) (NU)
37	$\overline{\text{SDT1}}$	Out	Slip printer printhead drive signal (dot1) (NU)
38	D0	I/O	Data bus 0
39	D1	I/O	Data bus 1
40	D2	I/O	Data bus 2
41	D3	I/O	Data bus 3
42	GND	—	GND
43	D4	I/O	Data bus 4
44	D5	I/O	Data bus 5
45	D6	I/O	Data bus 6
46	D7	I/O	Data bus 7
47	$\overline{\text{SPRQ}}$	Out	SSP interrupt request to CPU
48	$\overline{\text{RESET}}$	In	MPCA reset
49	$\overline{\text{SHEN}}$	In	Shift enable from CKDC8

Pin No.	Signal name	In/ Out	Function
50	$\overline{\text{INT3}}$	In	Interrupt signal (Nu)
51	RXD2	Out	8 bit serial port output to CPU
52	TXD2	In	8 bit serial port input from CPU
53	SCK2	In	Serial port shift clock input from CPU.
54	$\overline{\text{IRQ0}}$	Out	Interrupt request to CPU
55	A0	In	Address bus 0
56	A1	In	Address bus 1
57	A2	In	Address bus 2
58	A3	In	Address bus 3
59	A4	In	Address bus 4
60	A5	In	Address bus 5
61	GND	—	GND
62	VCC	—	+5V
63	A6	In	Address bus 6
64	A7	In	Address bus 7
65	A8	In	Address bus 8
66	A9	In	Address bus 9
67	A10	In	Address bus 10
68	A11	In	Address bus 11
69	A12	In	Address bus 12
70	A13	In	Address bus 13
71	A14	In	Address bus 14
72	A15	In	Address bus 15
73	A16	In	Address bus 16
74	A17	In	Address bus 17
75	A18	In	Address bus 18
76	A19	In	Address bus 19
77	A20	In	Address bus 20
78	A21	In	Address bus 21
79	A22	In	Address bus 22
80	$\overline{\text{LCDC}}$	—	LCD CS (NU)
81	A23	In	Address bus 23
82	TRGI	In	Dot pulse control/drive signal
83	$\overline{\text{PTMG}}$	Out	Printer timing signal
84	$\overline{\text{PRST}}$	Out	Printer reset signal
85	$\overline{\text{RDY}}$	In	Ready from FMC unit
86	$\overline{\text{IPLON}}$	In	To option connector (NU)
87	MD1	In	Mode select input (+5V)
88	MD0	In	Mode select input (GND)
89	$\overline{\text{TEST}}$	In	+5V
90	MA15	—	Image address 15 (NU)
91	MA18	—	Nu
92	MA19	—	Nu
93	RCVRDY1	—	Nu
94	RCVRDY2	—	Nu
95	RC0	—	Remote control encord signal for CPU
96	IRTX	—	I/R output for LED (NU)
97	UASCK	—	I/R serial data shift clock (NU)
98	$\overline{\text{UARX}}$	—	I/R serial data for CPU (NU)
99	$\overline{\text{UATX}}$	—	I/R serial data from CPU (NU)
100	VCC	—	+5V
101	GND	—	GND
102	$\overline{\text{IRRX}}$	—	I/R input from I/R unit (NU)
103	$\overline{\text{RCI}}$	—	I/R input from I/R unit (NU)
104	DAX1	—	System clock (7.3728MHz)

Pin No.	Signal name	In/ Out	Function	
105	DAX2	—	Nu	
106	$\overline{\text{MCR1}}$	—	Nu	
107	$\overline{\text{MCR2}}$	—	Nu	
108	$\overline{\text{WAIT}}$	Out	Wait request signal	
109	$\overline{\text{EXWAIT}}$	In	External wait control input signal	
110	RA18	Out	Nu	
111	RA17	Out	Nu	
112	GND	—	GND	
113	RA16	Out	Nu	
114	RA15	Out	Nu	
115	$\overline{\text{RDO}}$	Out	Expansion RD signal	Option
116	$\overline{\text{WRO}}$	Out	Expansion WR signal	
117	$\overline{\text{EXINT3}}$	In	Expansion interruption signal 3	Option
118	$\overline{\text{EXINT2}}$	In	Expansion interruption signal 2	
119	$\overline{\text{EXINT1}}$	In	Expansion interruption signal 1	
120	$\overline{\text{EXINT0}}$	In	Expansion interruption signal 0	
121	$\overline{\text{0PTCS}}$	Out	Chip select base signal for expansion option	
122	$\overline{\text{ROS1}}$	Out	ROM 1 chip select signal	
123	$\overline{\text{ROS2}}$	Out	ROM 2 chip select signal (NU)	
124	RAS2	Out	RAM 2 chip select signal	
125	RAS1	Out	RAM 1 ship select signal	
126	RJRST	In	Printer reset signal	
127	RJTMG	In	Printer timing signal	
128	DT4	Out	Printer dot signal 4	
129	DT3	Out	Printer dot signal 3	
130	DT2	Out	Printer dot signal 2	
131	DT1	Out	Printer dot signal 1	
132	GND	—	GND	
133	DT7	Out	Printer dot signal 7	
134	DT6	Out	Printer dot signal 6	
135	DT5	Out	Printer dot signal 5	
136	$\overline{\text{MTD}}$	Out	Printer motor $\overline{\text{drive}}$ signal	
137	MTD	Out	Printer motor drive signal	
138	DOT9	Out	Printer dot signal 9 (NU)	
139	DOT8	Out	Printer dot signal 8 (NU)	
140	SYNC	—	Nu (+5V)	
141	$\overline{\text{ASKRX}}$	—	I/R input from I/R unit (NU)	
142	VCC	—	+5V	
143	GND	—	GND	
144	—	—	Nu	
145	RAS3	Out		
146	RJMTR	In	Printer motor lock detection signal (NU)	
147	SLMTD	In	Nu	
148	SLMTS	In	Nu	
149	SLMTR	In	GND	
150	HTS2	Out	Serial output to FMC unit (NU)	
151	SCK2	Out	Serial clock to FMC unit (NU)	
152	STH2	In	Serial input to FMC unit (NU) pull-up	
153	—	—	Nu	
154	—	—	Nu	
155	—	—	Nu	
156	—	—	Nu	
157	—	—	Nu	
158	LCDWT	—	Nu	
159	DOTEN	Out	Dot drive enable signal	
160	RASP	—	Nu	

2-3. CKDC8

1) Pin configulation



2) Pin assignment (CKDC8)

Pin No.	SYMBOL	SIGNAL NAME	IN/ OUT	FUNCTION
1	DP	DP	OUT	DISPLAY SEGMENT Dp
2	A	SA	OUT	DISPLAY SEGMENT a
3	B	SB	OUT	DISPLAY SEGMENT b
4	C	SC	OUT	DISPLAY SEGMENT c
5	D	SD	OUT	DISPLAY SEGMENT d
6	E	SE	OUT	DISPLAY SEGMENT e
7	F	SF	OUT	DISPLAY SEGMENT f
8	G	SG	OUT	DISPLAY SEGMENT g
9	VSS0	GND		GND
10	VDD0	VDD		VDD
11	KR4	KR4	IN	KEY RETURN 4
12	KR10	KR10	IN	KEY RETURN (feed clerk MRS sw)
13	KR11	KR11	IN	KEY RETURN (MODE sw)
14	KR8	NU	IN	GND
15	HTS	HTS	IN	
16	STH	STH	OUT	
17	/SCK	/SCK	IN	SHIFT CLOCK
18	ST0	ST0	OUT	KEY STROBE 0
19	ST1	ST1	OUT	KEY STROBE 1
20	ST2	ST2	OUT	KEY STROBE 2
21	ST3	ST3	OUT	KEY STROBE 3
22	ST4	ST4	OUT	KEY STROBE 4
23	ST5	ST5	OUT	KEY STROBE 5
24	VDD1	VDD		VDD
25	AXSS	GND		GND
26	KR9	NU		GND
27	KR0	KR0	IN	KEY RETURN 0
28	KR1	KR1	IN	KEY RETURN 1
29	KR2	KR2	IN	KEY RETURN 2
30	KR3	KR3	IN	KEY RETURN 3
31	KR5	KR5	IN	KEY RETURN 5
32	KR6	KR6	IN	KEY RETURN 6

Pin No.	SYMBOL	SIGNAL NAME	IN/ OUT	FUNCTION
33	KR7	KR7	IN	KEY RETURN 7
34	AVRF	GND		
35	AVDD	VDD		
36	/RESET	/RES0	IN	
37	XT2			32.768 KHz
38	XT1			
39	IC	GND		
40	X2			4.19 MHz
41	X1			
42	VSS1	GND		
43	LDRQ	LDRQ	IN	LORD REQUEST
44	ERC	ERC	IN	EVENT READ CANCEL
45	SHEN	/SHEN	OUT	SHIFT ENABLE
46	/RES1	/RESETS	OUT	SYSTEM TO RESET
47	ST6	ST6	OUT	KEY STROBE 6
48	ST7	ST7	OUT	KEY STROBE 7
49	ST8	ST8	OUT	KEY STROBE 8
50	ST9	NU	OUT	KEY STROBE 9
51	/POFF	/POFF	IN	POWER OFF
52	BUZ	BUZ	OUT	BUZZER
53	T0	G1	OUT	DISPLAY DIGIT 1
54	T1	G2	OUT	DISPLAY DIGIT 2
55	T2	G3	OUT	DISPLAY DIGIT 3
56	T3	G4	OUT	DISPLAY DIGIT 4
57	T4	G5	OUT	DISPLAY DIGIT 5
58	T5	G6	OUT	DISPLAY DIGIT 6
59	T6	G7	OUT	DISPLAY DIGIT 7
60	T7	G8	OUT	DISPLAY DIGIT 8
61	T8	G9	OUT	DISPLAY DIGIT 9
62	T9	G10	OUT	DISPLAY DIGIT 10
63	T10	NU	OUT	DISPLAY DIGIT 11
64	ID	NU	OUT	DISPLAY SEGMENT ▼

3. Clock generator

1) CPU (HD64151010FX)

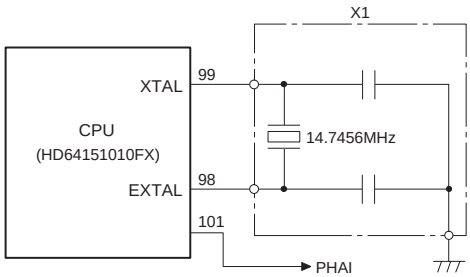


Fig. 3-1

Basic clock is supplied from a 14.7456MHz ceramic oscillator.
The CPU contains an oscillation circuit from which the basic clock is internally driven. If the CPU was not operating properly, the signal does not appear on this line in most cases.

2) CKDC8 oscillation circuit

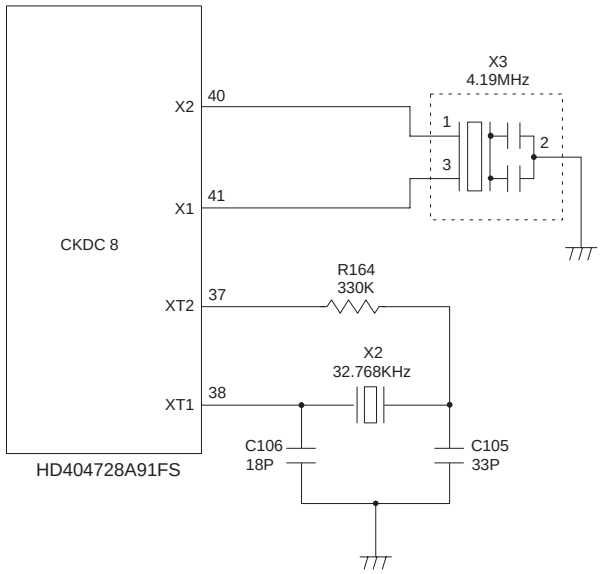


Fig. 3-2

Two oscillators are connected to the CKDC8.
The main clock X3 generates 4.19MHz which is used during power on.
When power is turned off, the CKDC8 goes into the standby mode and the main clock stops.
The sub-clock X2 generates 32.768KHz which is primarily used to update the internal RTC (real time clock). During the standby mode, it keeps oscillating to update the clock and monitoring the power recovery.

4. Reset (POFF) circuit

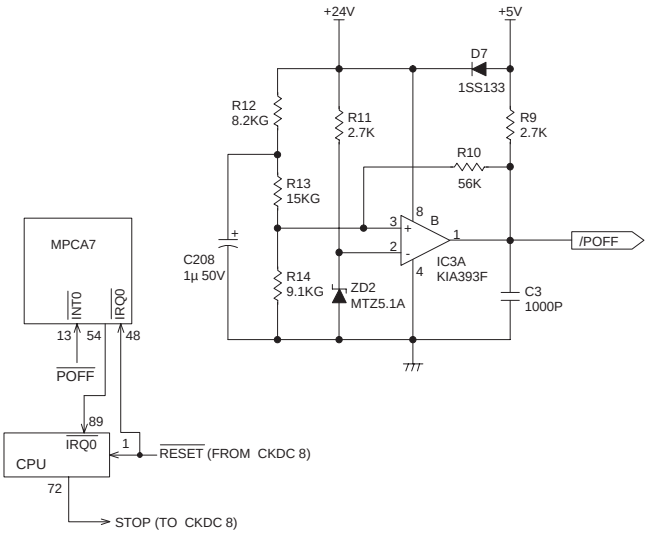
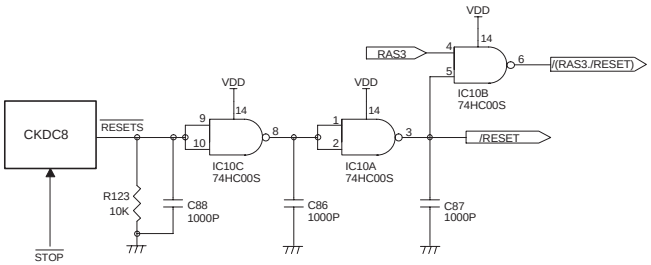


Fig. 4-1

In order to prevent memory loss at a time of power off and power supply failure of the ECR, the power supply condition is monitored at all times. When a power failure is met, the CPU suspends the execution of the current program and immediately executes the power-off program to save the data in the CPU registers in the external S-RAM with the signal $\overline{\text{STOP}}$ forced low to prepare for the power-off situation. The signal $\overline{\text{STOP}}$ is supplied to the CKDC8 as signal $\overline{\text{RESET}}$ to reset the devices.

This circuit monitors +24V supply voltage.

The voltage at the (–) pin of the comparator IC3A is always maintained to 5.1V by means of the zener diode ZD2, while +24V supply voltage is divided through the resistors R12, R13, and R14, and is applied to the (+) pin. When normal +24V is in supply, 6.8V is supplied to the (+) pin, therefore, signal $\overline{\text{POFF}}$ is at a high level. When +24V supply voltage decreases due to a power off or any other reason, the voltage at the (+) pin also decreases. When +24V supply voltage drops, the voltage at the (+) pin drops below +5.1V, which causes $\overline{\text{POFF}}$ to go low, thus predicting the power-off situation.



The $\overline{\text{STOP}}$ signal from the CPU is converted into the $\overline{\text{RESETS}}$ signal by the CKDC6.

The $\overline{\text{RESETS}}$ signal from the CKDC8 is converted into the $\overline{\text{RESET}}$ signal at the gate backed-up by the VRAM power, performing the system reset.

5. Memory control

1) Memory map

① All range memory map

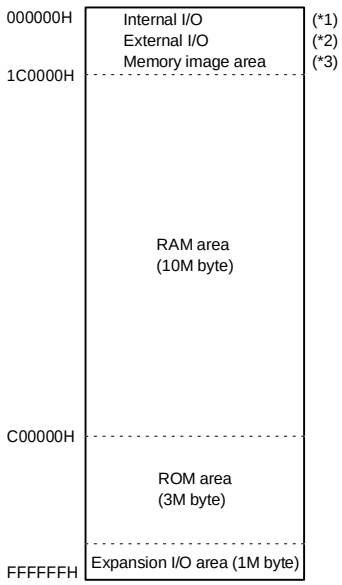


Fig. 5-1

(✳1) “Internal I/O” means the registers in the H8/510.

(✳2) “External I/O” means the base system I/O area to be addressed in page 0.

(✳3) "Memory image area" means the lower 32KB of ROM area which is projected to 000000H ~ 007FFFH for allowing reset start and other vector addressing, or the lower 32KB of RAM area which is projected to 008000H ~ 00FE7FH for allowing 0 page addressing of work RAM area.

(✳4) “Expansion I/O” means expansion I/O device area which isaddressed to area other than page 0.

② 0 page memory map

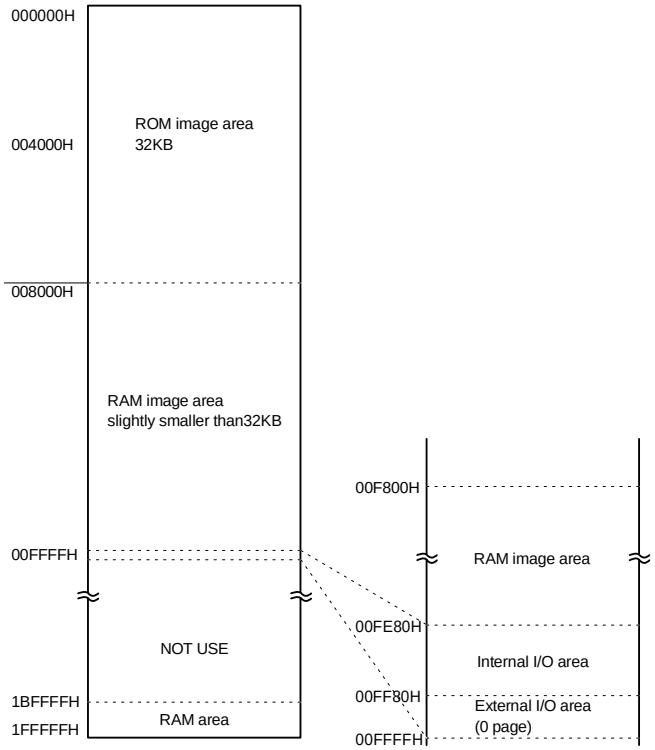


Fig. 5-2

- ROM image area: Image is formed in ROM area address C00000H to C07FFFH. This area is identical to IPL ROM area which will beseparately developed.
- RAM image area: Image is formed in RAM area address 1F0000H to 1F7E7FH. (✳Note)

  ✳ Note: Image can be formed in lower 32KB of RAS2.

③ ROM area memory map

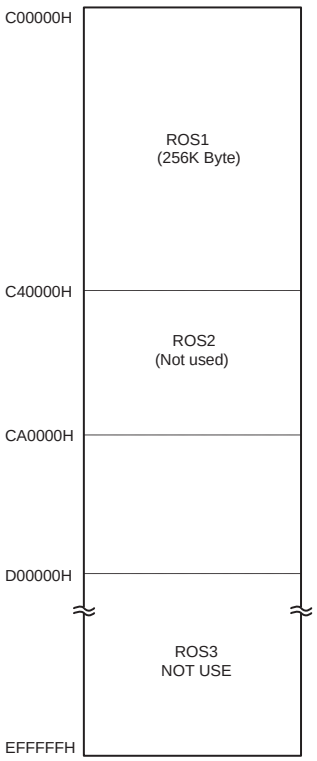


Fig. 5-3

④ RAM area memory map

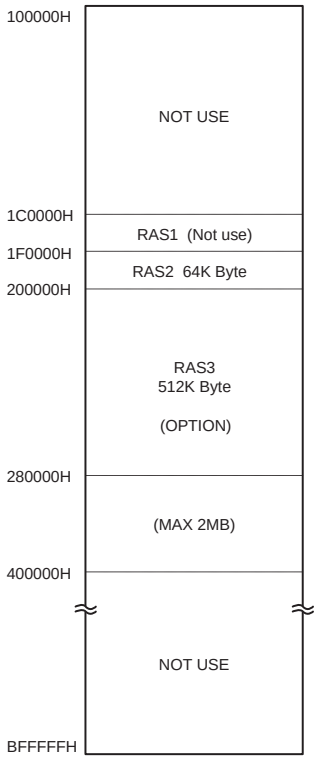


Fig. 5-4

∗ Note: RAS2 signal is formed as OR in the image area of 0 page. (lower32KB).

⑤ I/O area memory map

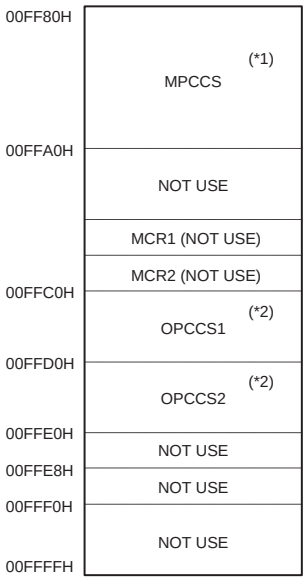


Fig. 5-5

∗ Note 1: MPCCS signal is the base signal for MPCA7 internal registerdecoding, and does not exist as an internal signal.

∗ Note 2: OPCCS1 and OPCCS2 signals are decoded in the OPC (optionperipheral controller) using the base signal OPTCS for optiondecoding. They does not exist as external signals.

2) Block diagram

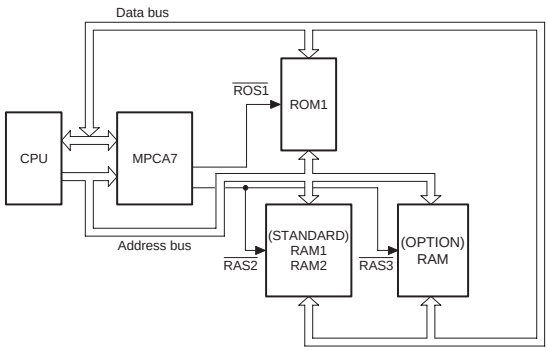


Fig. 5-6

① ROM control

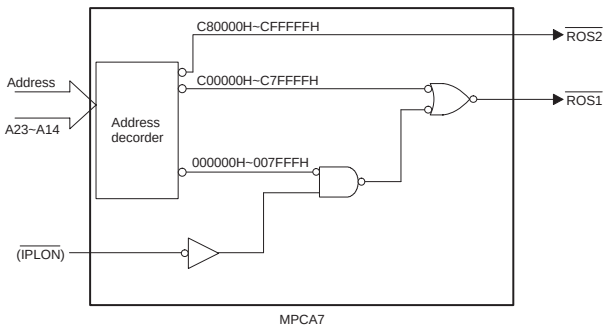


Fig. 5-7

IPLON: IPL board detection signal incorporated in the option slot. Note used in the ER-A445P. (Not used)

Access is performed with two ROM chip select signals $\overline{ROS1}$ and $\overline{ROS2}$, which decode 512KB address area respectively to access-max. 4MB ROM.

② RAM control

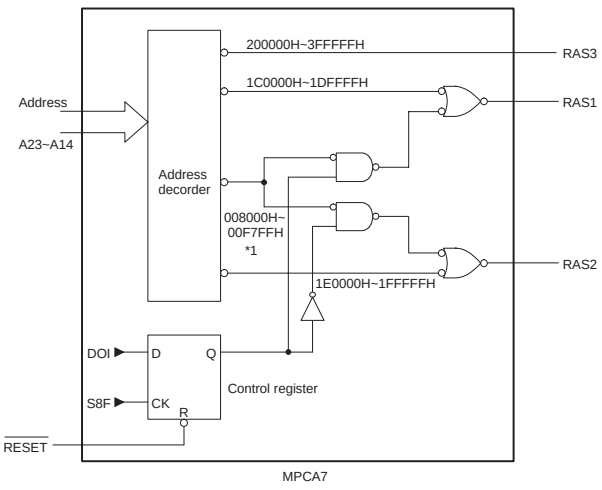


Fig. 5-8

Access is performed with two RAM chip select signals, RAS2 and RAS3. The control register in MPCA7 allows selection of pageimage memory area. (RAS1 is selected for initializing.)

∗ : For 0 page image area, selection between RAS2 and RAS3 can bemade with the control register. The 0 page control registerperforms initializing at the timing of no stack processimmediately after resetting.

6. SSP circuit

1) Block diagram

This is the circuit employed to do the Special Service Preset(SSP).

(Block diagram)

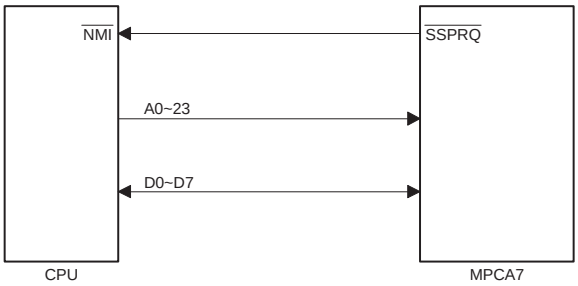


Fig. 6-1

(MPCA7 block diagram)

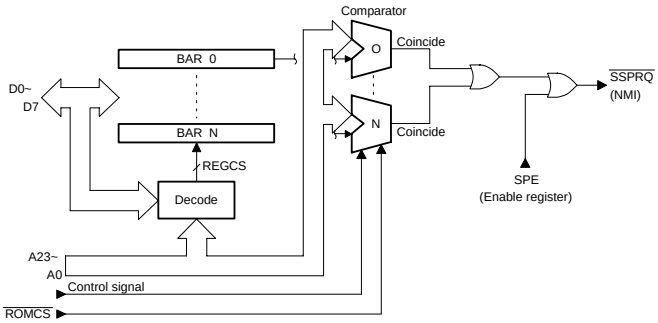


Fig. 6-2

As the address detection system, the brake address register comparison system is employed though the mapping system was employed in the conventional monitor RAM. The address registerlocated in MPCA is always compared with the system address bus to monitor and generate NMI signal at a synchronized timing and togo to NMI exception process.

In the exception process routine service routine, the entry address is checked to go to SSP sub routine.

Entry to the break address register (BAR) is performed through address FFFF00H or later decoded in MPCA7.

2) SSP register

The break address register (BAR) is accessed through direct address of FFFF00H~FFFFFFH. Entry number is 32 entry.

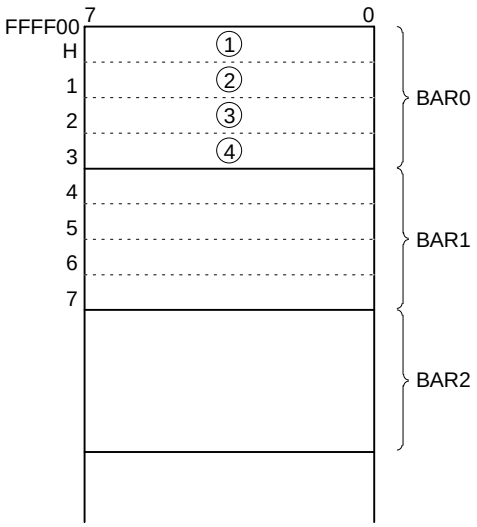
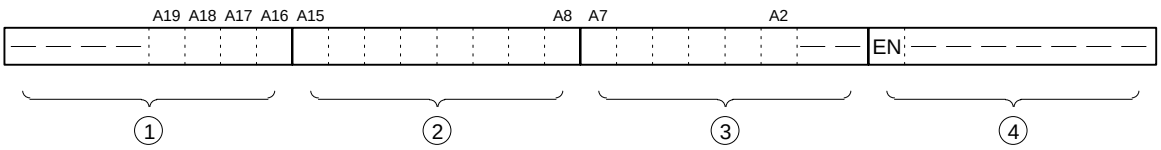


Fig. 6-3

Each BAR is composed of 4 byte address. Bit composition is as follows:



Upper bits

Intermediate bits

Lower bits

Enable register
EN (bit7) = 1 Enable
= 0 Inhibit

Don't care for "-----."

< BAR composition >

Fig. 6-4

④ is the enable register. The entry registers of the break address are assigned to ①, ②, and ③. Each bit of address corresponds to each bit position, writing to ①, ②, and ③ is performed without shifting. The corresponding area is 1MB space of ROS1 and ROS2.

3) SSP register access method

Access to SSP break address register is performed through the temporary register as shown below:

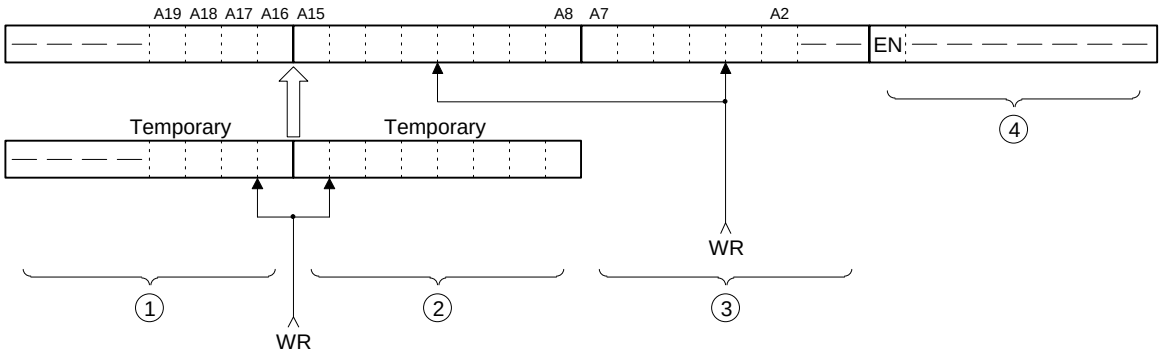


Fig. 6-5

Enable flags can be accessed individually.
Though enable register ④ can be accessed individually, writing to brake address registers ① and ② is performed at the same time as writing to brake address register ③ through the temporary register.
Therefore, set ① and ② to temporary, then write into ③ at last.
Since the temporary register is commonly used by BAR sets, thefollowing register setting is performed after completion ofsetting of each break address register.

③ SSP control method

Access to the enable register and the brake address register is only possible when writing to them from the CPU.

bit 7	6	5	4	3	2	1	0	
0	0	0	CMP4	CMP3	CMP2	CMP1	CMP0	(FFFFFFH)

Information on which brake register the SSP brake is detected in is read as binary data by reading address FFFFFFH (*1).
Used in an expanded register.
Normally is a reserve bit. Whenreading, fixed to 0.
If there are 32 break registers, binary expression is made with the above 5 bits, and 0th is "00000_B" and 31st is "11111_B."
When detected simultaneously by two or more break registers, onewith the smaller BAR number is read as binary data.
The brake signals (NMI) and the above detection data (CMP0~4) areheld until the above detection data are read. So read should bemade in the NMI sub routine. (Clear by FFFFFFH read.)

∗ 1: FFFFFFH is not fulldecoded. (FFFF00H~FFFFFFH). Therefore,unnecessary read access in parentheses should not be performed.

7. PRINTER control circuit

1) Block diagram

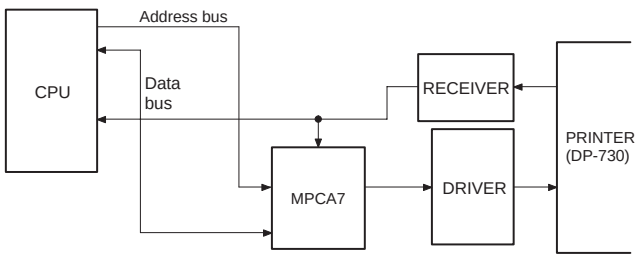
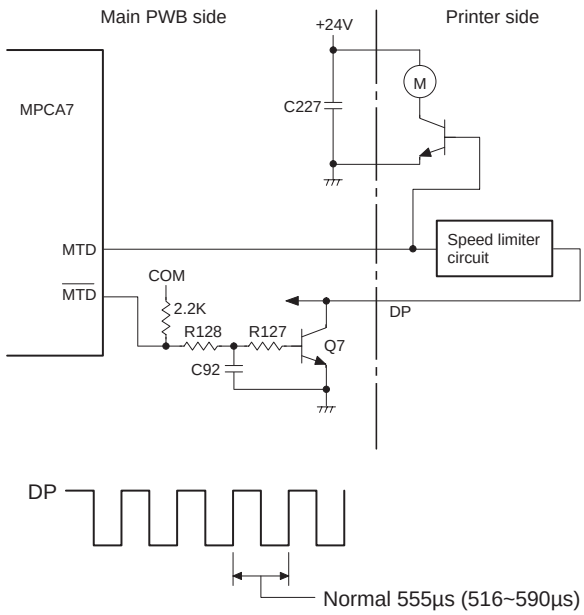


Fig. 7-1

2) General description of the printer controller

The DP-730 is used as the R/J printer. The printer mechanical timing control is made by the CPU through MPCA7.

3) Printer motor drive circuit



When the MTD is high, the motor rotates.
When the MTD is low, the motor stops.

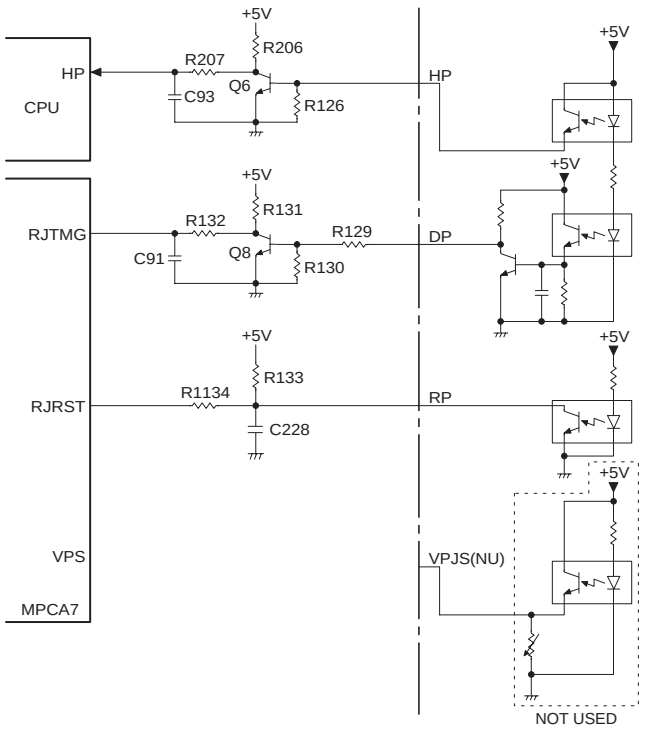
<Motor lock protection>

When an abnormal load is applied to the mechanism, the DP (Dot Pulse) frequency is checked to prevent against the motor burn-out, the timing belt shift, and gear damage. If the following condition is made, the CPU stops the motor rotation.

① When starting the motor: When the cycle from starting to the 100th pulse of DP is 16ms. (The one pulse cycle of DP is normally 555us.)

② During constant rotation of the motor: When one pulse of DP is 1100us or more.

4) Printer sensor circuit



The printer supplies the RP (Reset Pulse) signal, the HP (Home Position) signal, and the DP (Dot Pulse) signal) to control printing timing and conduction timing of solenoids. It also supplies the VPJ signal to detect the presence of validation paper. These sensor are photo interrupters.

① RP (RJRST) signal
This signal is outputted once for every reciprocating motion of the print head. It indicates the reference position of the HP signal.

The rear edge of RP (OFF -- ON) is used as the signal.

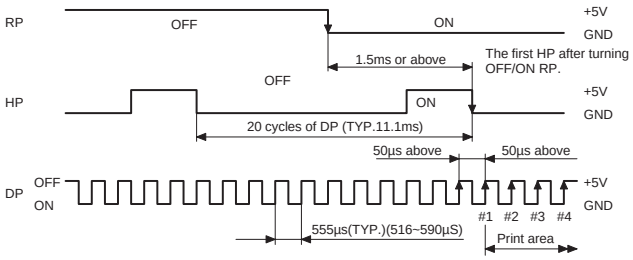
② HP signal
The pulse signal is outputted from the slit in the disk installed to the DC motor shaft. It is used as the reference signal for starting counting of the DP signal. It is generated once for twenty DP signals. The rear edge of the HP signal (ON -- OFF) immediately after generation of the RP signal is used as the signal.

③ DP (RJTMG) signal
The pulse signal is outputted from the slit in the disk installed to the DC motor shaft. It is used as the control signal for the print solenoid and the paper feed solenoid.

The front edge of the output signal (ON -- OFF) is used as the signal.

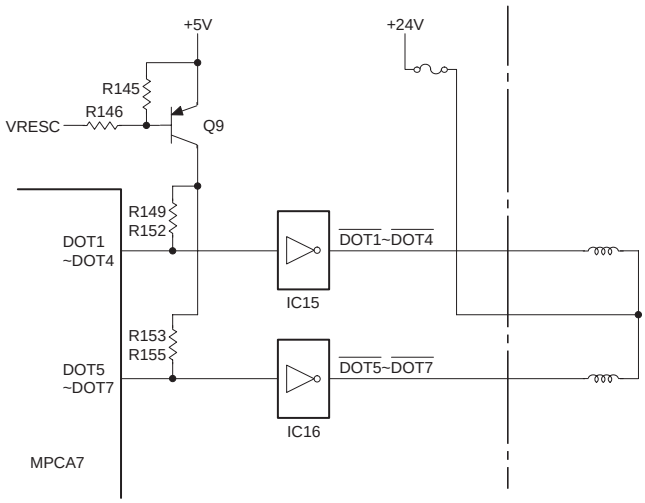
④ VPJS (VPJ) signal
The presence of a validation card is detected by interruption of the photo interrupter LED light by the validation card.

Relation ship among RP/HP/DP



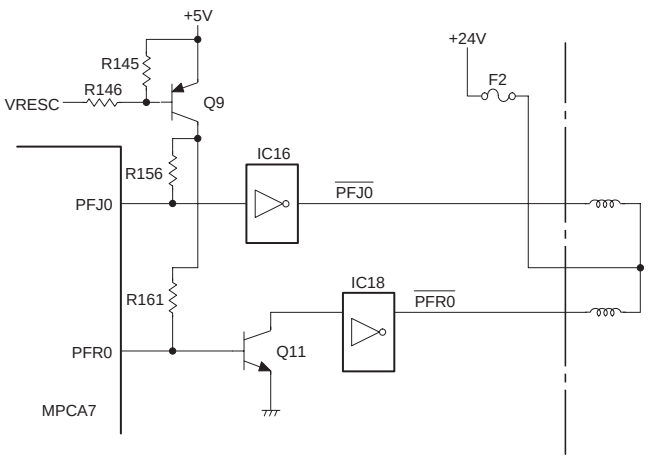
* The waveforms are those indicated with arrow in Fig.3-3.

5) Dot solenoid drive circuit



The DOT1 ~ DOT7 (the dot solenoid drive signals from the MPCA7) are pulled up by the VRESE and converted into LOW by the driver IC. A +24V voltage is applied to the solenoid. This operates the dot wire.

6) Paper feed circuit



The PFJ0 (the journal paper fed signal from the MPCA7) and the PFR0 (the receipt paper feed signal) are pulled up by the VRESE and converted into LOW level. A +24V voltage is applied to the solenoid. This operates the paper feed solenoid.

7) Caution

CAUTION

If fuse F2 should be blown, the dot head solenoid may be shorted. Be sure to check the head impedance and driver breakdown.

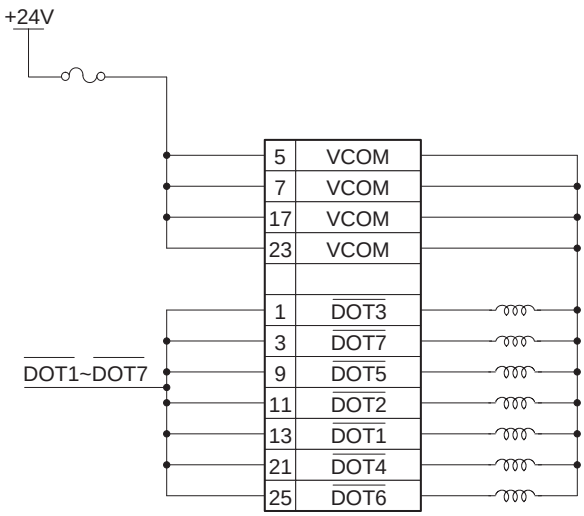
When fuse F2 is blown:

① Remove F2, and perform the service resetting. The set the mode switch to a position other than SRV and SRV' and turn off the power.

② Install fuse F2 (1A) and turn on the power.
If the fuse blows with the above operation, driver 4AC16 may be shorted.

③ Turn off the power.

④ Disconnect the printer cable from the printer. Measure impedance between the printer body connector pin 5 and the following pins: 1, 3, 9, 11, 13, 21, 25
The impdenace must be 10.5Ω ± 10%.
If impedance is outside the above range, the dot solenoid is bad. Replace the dot head unit.



8. Drawer drive circuit

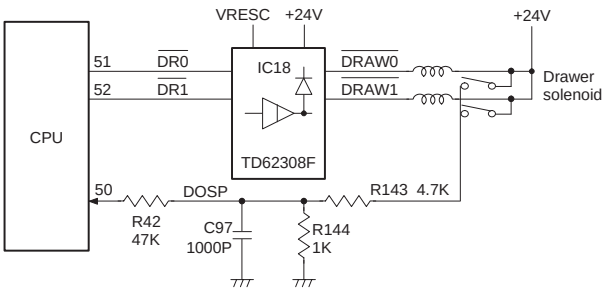


Fig. 8-1

The drawer is directly supported by the CPU. No action starts when the power supply is not steady as the output stage of the driver is pulled VP by VRESC signal.

Drawer open and close is sensed with the microswitch provided in the drawer whose signal is level converted with R74 and R73 and directly read by the CPU.

9. Key, display, time buzzer controls

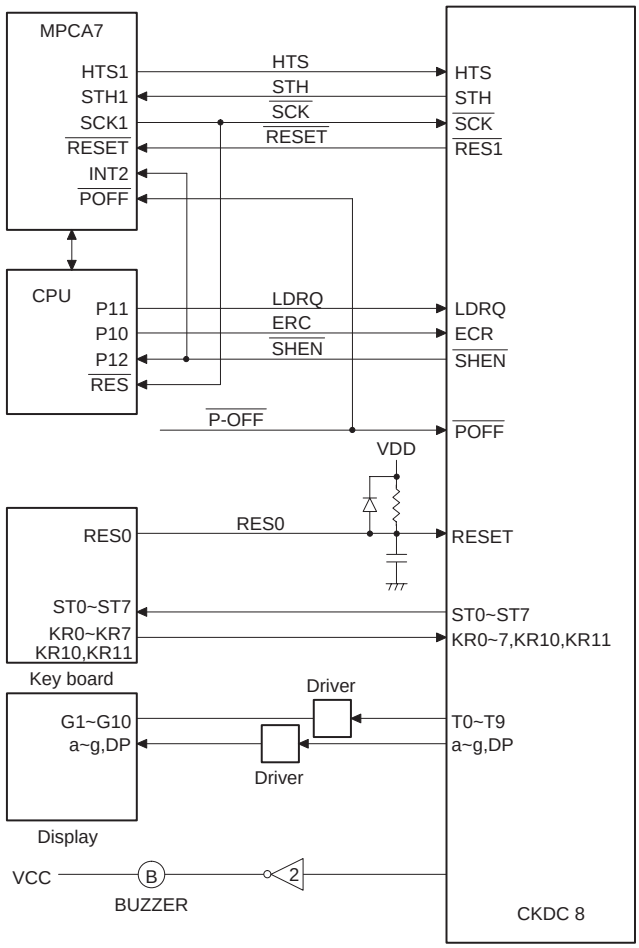


Fig. 9-1

1) Power on sequence

During service interruption, the CKDC8 senses POF within 500msec. When service interruption is cancelled by turning on the power, the CKDC8 cancels resetting of the CPU in the command mode. After initializing each port, the CPU reads the start condition (1 byte).

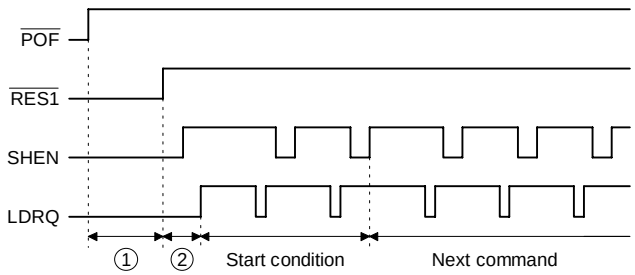


Fig. 9-2

After sampling POF High, the CKDC5 performs mode scan and key scan at ①, then cancels resetting of the CPU. After being cancelled, the CPU initializes each port at ② and reads the start condition.

After being cancelled, the CPU reads the start condition without fail to set the sift mode. If, however, the first starting is made in other than SRV mode after the CKDC8 resets the CPU without request from the CPU, the CKDC8 sets the start condition supposing that starting is made in SRV mode.

2) Power off sequence

When the CPU senses a service interruption, it performs necessary procedures for CPU stop. Then the CPU outputs a reset request to the CKDC5.

Reset request

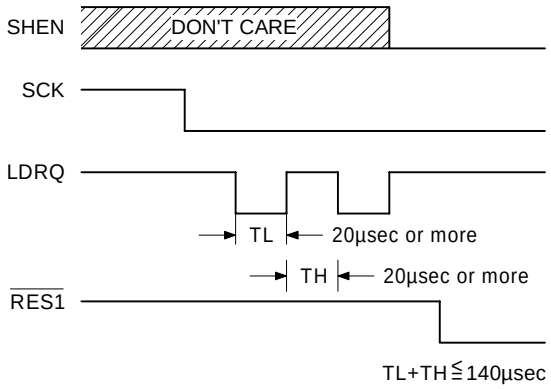


Fig. 9-3

When the CPU senses a service interruption or an error, it performs necessary procedure for CPU stop and issues reset request.

CPU procedures necessary for reset request

① All CPU interrupts are made DI.

② SCK is driven to low.

③ Keep LDRQ at LOW level for 20usec or more and drive it HIGH.

④ Loop ① to ③. During looping, access should not be made to external memory.

⑤ It should be within 140usec from rising of one LDRQ to rising of another.

When, however, the CKDC8 senses a service interruption at POF, it stops displaying. Service interruption procedure is performed after receiving reset request from the CPU. If reset request is not sent from the CPU within 100msec the service interruption procedure is started after 110 ±10msec to go into the stand-by mode.

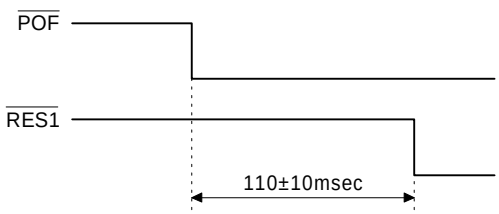


Fig. 9-4

3) Key and switch scanning

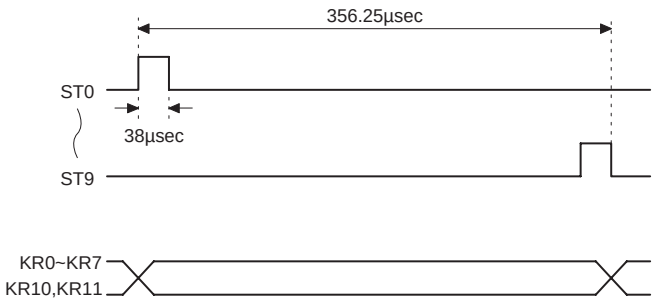


Fig. 9-5

As the strobe signal, 8 bits of ST0 - 8 are used.

KR0 - KR7 are used as the key return signal. KR10 is used as the return signal of the paper feed key, cashier key and MRS switch. KR11 is used as the return signal of the mode switch.

4) DISPLAY CONTROL

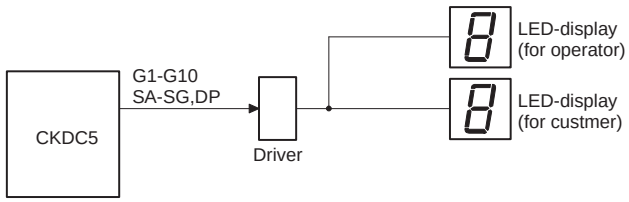


Fig. 9-6

CKDC8 directly drives the LED display unit.

10. Power supply circuit

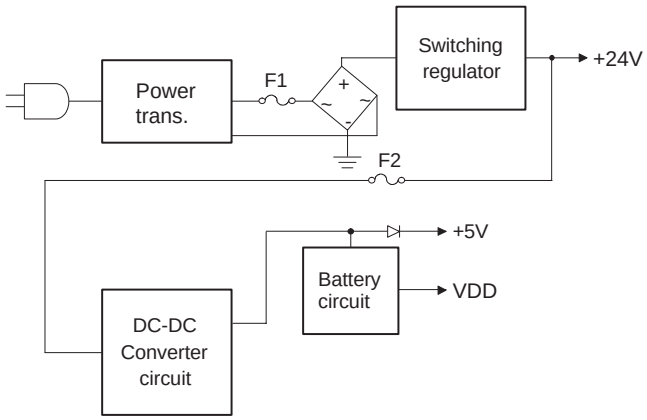


Fig. 10-1

+24V: Printer, solenoid power

+5V: VCC (Logic power)

VDD: Battery charge, Battery back-uped power, CKDC-8 and RAM Back-up power

CHAPTER 5. TEST FUNCTION

1. General

1) This diagnostic program has been developed for diagnosing machine functions in the field. The program is contained within the ER-A440.
   The diagnostic program is stored in the external ROM which will be executed by the CPU (H8/510) which requires the following diagnostic operations:
   a) Proper power supply voltages are mandatory for logic circuits (+5V, VDD, POFF, +12.5V, +24V).
   b) CPU input/output pins, CPU internal logic, CKDC8, MPCA7, system bus and common ROM/RAM must be working properly.

2. Operational procedure

To start the diagnostic program, you must enter the following command.
3-digit test item number → key in the SRV mode.

The key assignment must be properly set and the ROM and RAM must be operating properly to go into this mode. This is necessary because the control jumps to the program area in the SRV mode. A master reset must be performed before operating the ECR for the first time. After any option is installed, a program reset is required. When the master reset or program reset is performed, be sure to check the printout on the journal paper.

Master reset:	Turn power on in the SRV' mode and change it to the SRV mode with the JF key pressed.
Journal print:	MASTER RESET ***
Program reset:	Turn power on in the SRV' mode and change it to the SRV mode.
Journal print:	PRG. RESET ***

3. Test command list

With the SRV mode and the following test code entry, the test start.

CODE	DESCRIPTION
100	Display & Buzzer test
101	Key code & Cashier key test
102	R/J printer test
104	Keyboard test
105	Mode switch test
106	Printer sensor test
108	Calendar oscklllator test
109	SSP test
110	Drawer open sensor test (For standard drawer)
111	Drawer open sensor test (For remote drawer)
120	Standard RAM test
130	Standard ROM test
150	Printer dot pulse width adjustment
200	Option RAM test
500	RS-232 loop back test

4. Test contents

[1] Display & Buzzer test

1) Key operation

100 → CA/AT

2) Functional description

Display the following message on the front and the rear display boards.

1. 2. 3. 4. 5. 6. 7. 8. 9. 0.

A decimal point shifts from lower number of digit by one digit (per 200m sec.).

Next, display the following segments (for approx. 1 sec.).

8. 8. 8. 8. 8. 8. 8. 8. 8. 8.

Repeat the above two kinds of displays.

Sound a buzzer continuously during test.

3) Check items

a) The display must be correctly shown at each position.
b) The luminosity of displays must be uniform and even at each position.
c) Abnormal buzzer sound is not allowed.

4) Test termination

Press any key. The test terminates with the test and message printed

1 0 0

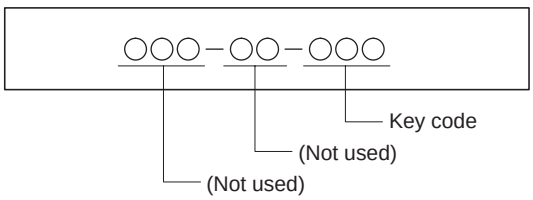
[2] Key code & Cashier key test

1) Key operation

101 → CA/AT

2) Functional description

Key code, MRS switch state and Cashier code are displayed.



3) Check items

a) Key code

HARDWARE CODE" of the following keys will be displayed ever time the keys are pressed.
"---" indicates that a key is struck twice and also that input data is not accepted.

[KEY POSITION CODE]

<ALL KEY>

								65	68	67	58	77	78
								66	55	56	57	48	38
R	J	63	62	61	52	51	60	40	45	35	46	47	37
74	43	33	42	32	41	31	50	30	76	75	36	28	27
14	23	24	22	72	21	71	20	70	15	05	16	17	18
04	13	03	12	02	11	01	10	00	26	25	06	07	08

<ER-A440 STANDARD KEY BOARD LAYOUT>

									68	67	58	77	78
								66	55	56	57	48	38
R	J	63	62	61	52	51		40	45	35	46	47	37
74	43	33	42	32	41	31		30	76	75	36	28	27
14	23	24	22	72	21	71		70	15	05	16	17	18
04	13	03	12	02	11	01		00	26	25	06		08

4) Test termination

Change the mode switch position other than SRV position to terminate the test.

The test terminates with the test and message printed

101

[3] R/J printer test

1) Key operation

102 → CA/AT

2) Functional description

Display the following message.

1 2 3 4 5 6 7 8 9 0

Print the following characters.

<RECEIPT>

ZZZZZZZZZZZZZZZZZZZZZZZZ
ZZZZZZZZZZZZZZZZZZZZZZZZ
ZZZZZZZZZZZZZZZZZZZZZZZZ

3 lines of Z(24 characters) are printed

<JOURNAL>

ZZZZZZZZZZZZZZZZZZZZZZZZ
ZZZZZZZZZZZZZZZZZZZZZZZZ
ZZZZZZZZZZZZZZZZZZZZZZZZ

3 lines of Z(24 characters) are printed

3) Check items

a) The head of printing position must be exactly aligned for "RECEIPT" and "JOURNAL".

b) Printed characters must be free of stain and blur.

4) Test termination

This check is terminated automatically.

[4] Keyboard test

1) Key operation

XXXX 104 → CA/AT

XXXX: Sumcheck data

Standard keyboard layout sumcheck data	
ER-A440	2266

2) Functional description

Keyboard test is performed with the sumcheck data of key code.
For sumcheck data, data are inputted to the upper upper four digits befor the diagnostics code.
The data are compared with the added data which are added until the final key (TL) is pressed. if the data agree with the added data, the end print is made. If not, the error print is made.
The su check data is obtained by totalizing all key hardware codes except for the (TL) key and converting the total into a decimal figure.

[ALL KEY LAYOUT]

								41	44	43	3A	4D	4E
								42	37	38	39	30	26
R	J	3F	3E	3D	34	33	3C	28	2D	23	2E	2F	25
4A	2B	21	2A	20	29	1F	32	1E	4C	4B	24	1C	1B
0E	17	18	16	48	15	47	14	46	0F	05	10	11	12
04	0D	03	0C	02	0B	01	0A	00	1A	19	06	07	08

[STANDARD KEYBOARD LAYOUT]

SUMCHECK DATA = 4A + 0E + 04 + 2B + 17 + · · · · · · · · = 2266

									44	43	3A	4D	4E
								42	37	38	39	30	26
R	J	3F	3E	3D	34	33		28	2D	23	2E	2F	25
A4	2B	21	2A	20	29	1F		1E	4C	4B	24	1C	1B
0E	17	18	16	48	15	47		46	0F	05	10	11	12
04	0D	03	0C	02	0B	01		00	1A	19	06		08

Display the following message on the front display.

1 0 4 ○○○

Key code

3) Check items

a) Check of the display in the test and the content of end print.

4) Test termination

This check is terminated automatically.

The test terminates with the test and message printed

Normal end

1 0 4

Error

E-----	1 0 4

[5] Mode switch test

1) Key operation

105 → CA/AT

2) Functional description

Display the following message on the front display.

1 0 5	X

When the Mode Switch is switched over in the following order, a numerical value corresponding to each position of mode switch is displayed at X.

Mode:	SRV	→	PGM2	→	PGM1	→	OFF	→	OP X/Z	→
x :	0	→	1	→	2	→	9	→	3	→
	SRV	←	X2/Z2	←	X1/Z1	←	MGR	←	REG	←
	0	←	7	←	6	←	5	←	4	←

3) Check items

a) Check of the display in the test and the content of end print.

4) Test termination

The test terminates with the test and message printed

Normal end

1 0 5

Error

E-----	1 0 5

[6] Printar sensor test

1) Key operation

106 → CA/AT

2) Functional description

State of the paper near end sensor is sensed and displayed.

1 0 6	X-X

X: JOURNAL side

Y: RECEIPT side

3) Check items

X, Y	Description
C	Paper near end sensor not detected. (Paper is existed)
O	Paper near end sensor detected. (Paper is not existed)

∗ "C" is always display when no sensor is used.

4) Test termination

Press any key. The test terminates with the test and message printed

1 0 6

[7] Calendar oscillator test

1) Key operation

108 → CA/AT

2) Functional description

This program is used to test the calendar oscillator function.

Display:

∗ ∗ – ∗ ∗

"∗∗ – ∗∗" shows the current time.
"–" is blinking. (500ms ON and OFF)

3) Check items

Time elapsed after master reset must be displayed.

4) Test termination

Press any key. The terminates with the test and message printed

1 0 8

[8] SSP test

1)Key operation

109 → CA/AT

2) Functional description

If an SSP is programmed, its contents are automatically chacked and the result is printed.

Display:

1 0 9

3) Check items

Check printing of the termination message.

4) Test termination

This check is terminated automatically.

The test terminates with the test and message printed

Normal end

```
|          109          |
```

Error

```
|  E-----    109        |
```

SSP table full

```
|  F-----    109        |
```

∗ In this SSP check, set the data for check in the empty area of SSP entry REG and erase the data for check after completion of check. Therefore SSP setting before check is not cleard.
If therefore there is no SSP entry REG remainedfor SSP check, F-print is performed to terminate the program without check.

[9] Drawer open sensor test (For standard test)

1) Key operation

110 → CA/AT

2) Functional description

State of the drawer open sensor is sensed and displayed.

```
|  1 1 0        X       |
```

3) Check items

X	Description
O	Drawer open sensor detected. (Drawer opend)
C	Drawer open sensor not detected. (Drawer closed)

a) Check opening of the specified drawer.

b) Check the display indication when the drawer is open and closed.

4) Test termination

Press any key. The test terminates with the test and message printed

```
|          110          |
```

[10] Drawer open sensor test (For remote drawer)

1) Key operation

111 → CA/AT

2) Functional description

State of the drawer open sensor is sensed and displayed.

```
|  1 1 1        X       |
```

3) Check items

X	Description
O	Drawer open sensor detected. (Drawer opend)
C	Drawer open sensor not detected. (Drawer closed)

a) Check opening of the specified drawer.

b) Check the display indication when the drawer is open and closed.

4) Test termination

Press any key. The test terminates with the test and message printed

```
|          111          |
```

[11] Standard RAM test

1) Key operation

120 → CA/AT

2) Functional description

Perform the following check for the standard RAM 128 KByte SRAM. The memory contents should not be changed before and after the check.

Perform the following processes for memory address to be checked (1E0000H~1F0000H).

PASS1: Save memory data.

PASS2: Write data "0000H."

PASS3: Read and compare data "0000H," write data "5555H."

PASS4: Read and compare data "5555H," write data "AAAAH."

PASS5: Read and compare data "AAAAH."

PASS6: Restore the memory data.

If a compare error occurs in the check sequence PASS1-PASS6, an error print is made. If no error occurs through all address, the check ends normally.

The following address check is performed further.

Check point address = 1E0000H, 1E0001H
1E0002H, 1E0004H
1E0008H, 1E0010H
1E0020H, 1E0040H
1E0080H, 1E0100H
1E0200H, 1E0400H
1E0800H, 1E1000H
1E2000H, 1E4000H
1E8000H, 1F0000H

7-SEGMENT DISPLAY: 1 2 0

3) Check the following items:

Check the termination printout.

4) Test termination

The test terminates after printing the termination printout.

Termination printout:

```
Normal termination      |          120
Abnormal termination    |  Ex-----   120
                        |          *****
```

X = 01: Data check error
02: Address check error

Note: When an error occurs, the error print is performed and the check is terminated. The error occurrence address is shown in hexadecimal at positions shown with ∗∗∗∗∗.

[12] Standard ROM test

1) Key operation

130 → CA/AT

2) Functional description

Sum check of the standard ROM (C00000H - C7FFFFH) is performed. If the lower two digits of SUM is 10H, it is normal.

7-SEGMENT DISPLAY: 1 3 0

3) Check the following items:

Check the printout after the test.

4) Test termination

The test automatically terminates with termination message.

Normal termination print		130
	ROM1	27020✱✱✱✱✱
		✱✱✱✱✱
Error termination print	E – – – –	130
	ROM1	27020✱✱✱✱✱
		✱✱✱✱✱

Note: "✱✱✱✱✱" means the ROM version number.
The underlined section (10 bytes) of code table is provided in the ROM as a standard and the table content is always printed.
The table position is the upper 10 digits of the ROM address.
The check sum correction address is the last address -0FH.

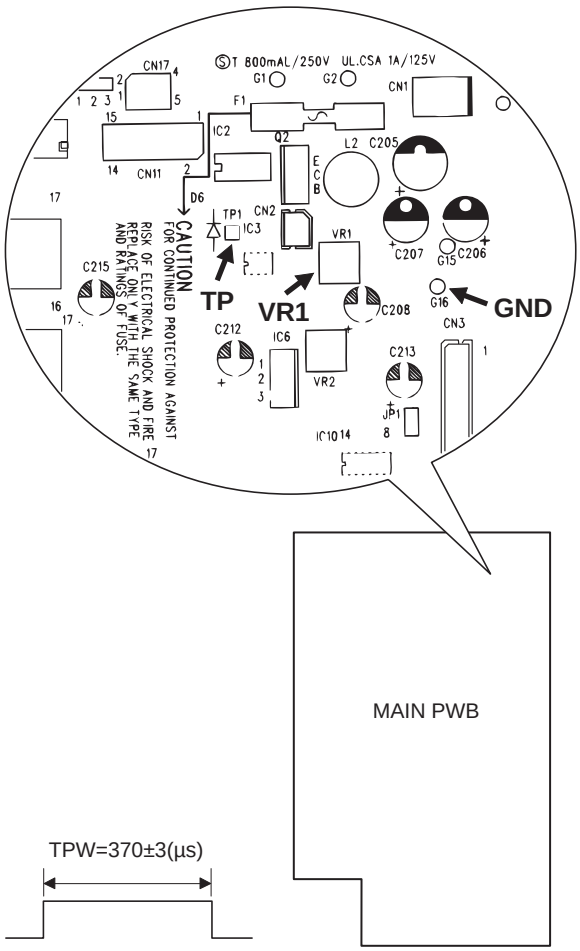
[13] Printer dot pulse width adjustment

1) Key operation

150 → CA/AT

2) Functional description

Adujustment width of TPW at the test point TP1.
The pulse width of TPWW canw bwe adjusted using the 200K pot VR1.



3) Check items

a) The pulse width of TPW must be adjusted to that at the above test point TP1.

4) Test termination

Do the program reset.

[14] Option RAM test

1) Key operation

200 → CA/AT

JOB #NO.	RAM NO.	Memory to be checked	Address area to be checked
200	Option RAM	ER-03RA	200000H ~ 27FFFFH

2) Content

The following check are performed for the optional RAM.

The following process is performed for memory addresses to be checked.

PASS1: memory data save

PASS2: Data "0000H" write

PASS3: Data "0000H" read and comparison, data "5555H" write

PASS4: Data "5555H" read and comparison, data "AAAAH" write

PASS5: Data "AAAAH" read and comparison

PASS6: Memory data restore

If a compare error is found in the check sequence from PASS1 to PASS6, error print (error code E1) is performed. If there is no error found to the end of the last address, the operation is completed normally.
Then the following address check is performed. "○" shows a valid address, and "X" shows an invalid address.
In case of an error, error code E2 is printed.

Check Address	JOB#201(ER-03RA)
200000H	○
200001H	○
200002H	○
200004H	○
200008H	○
200010H	○
200020H	○
200040H	○
200080H	○
200100H	○
200200H	○
200400H	○
200800H	○
201000H	○
202000H	○
204000H	○
208000H	○
210000H	○
220000H	○
240000H	○
260000H	○

7-SEGMENT DISPLAY: 2 0 0

3) Check the following items.

Check the termination print.

4) Test termination

The test terminates after printing the termination printout.
Termination print

E01---	200	(data check error)
E02---	200	(address check error)
	✳✳✳✳✳	
	200	(normal end)

✳✳✳✳✳✳: Error address

[15] RS-232 loop back test

Connect the loop back connector(UKOG-6705RCZZ) to RS232 connector.

1) Key operation

500 → CA/AT

2) Functional description

Control signal check

OUT PUT		INPUT			
/ER	/RS	/DR	/CI	/CD	/CS
OFF	OFF	OFF	OFF	OFF	OFF
OFF	ON	OFF	OFF	ON	ON
ON	OFF	ON	ON	OFF	OFF
ON	ON	ON	ON	ON	ON

Data communication check
Perform 256-byte branch loop back test between SD and RD.

DATA: $00 - $FF BAUD RATE: 9600 BPS

Display:

5 0 0

4) Test termination

This check is terminated automatically.
The test terminates with the test and message printed

Normal end

RS TEST OK

Error

RS TEST ✳✳NG ✳✳ ER XX

XX: Error code	
E1	ER-DR error
E2	ER-CI error
E3	RS-CD error
E4	RS-CS error
E5	SD-RD error (DATA error)
E6	SD-RD error (DATA error/Flaming error)

CHAPTER 6. DOWN LOAD FUNCTION

1. General

RAM data can be transmitted in the following two methods.

Save the data before servicing as follows:

① ECR ⟷ ECR

- Cable: 9 pin D-SUB – 9 pin D-SUB

Fig. 1-1

② ECR ⟷ ER-02FD

- Cable: 9 pin D-SUB – 25 pin D-SUB

Fig. 1-2

2. SIO interface specification

1) Operation:	Simplex
2) Line configuration:	Direct connect
3) Data rate:	19200, 9600, 4800, 2400, 1200, 600, 300BPS (Selected by SRV JOB#903-A)
4) Sync mode:	Asynchronous
5) Checking:	Vertical parity (odd)
6) Code:	7 bits (ASCII)
7) Bit sequence:	LSB first
8) Line level:	RS232 level
9) Data forma:	

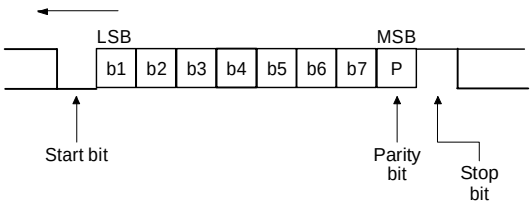
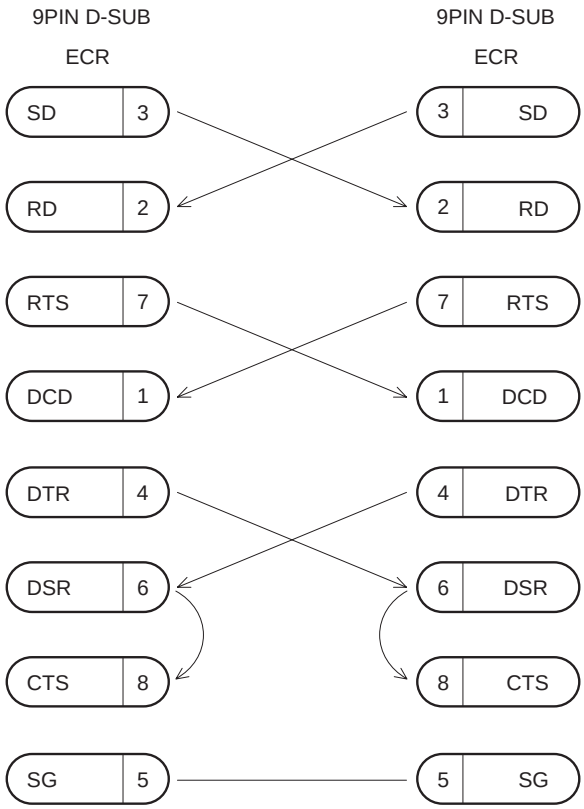


FIg. 2-1

3. Location of connector pins

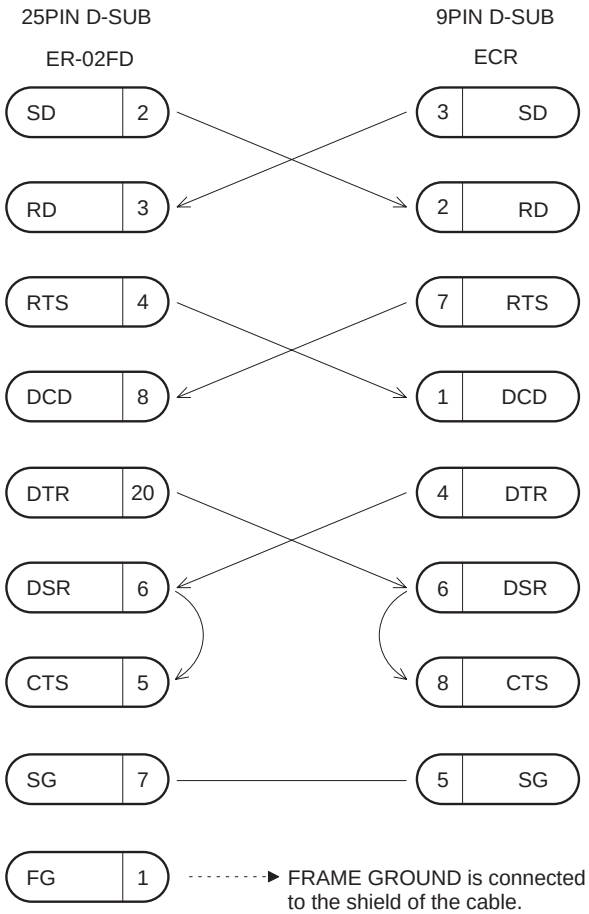
① ECR-ECR cable



SD : TRANSMITTED DATA
RD : RECEIVED DATA
DTR: DATA TERMINAL READY
DSR: DATA SET READY
RTS: REQUEST TO SEND
DCD: DATA CARRIER DETECTOR
CTS: CLEAR TO SEND

Fig. 3-1

② ECR-ER-02FD cable



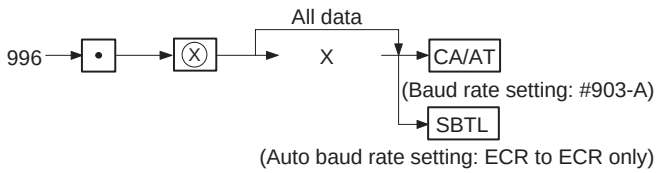
SD : TRANSMITTED DATA
RD : RECEIVED DATA
DTR: DATA TERMINAL READY
DSR: DATA SET READY
RTS: REQUEST TO SEND
DCD: DATA CARRIER DETECTOR
CTS: CLEAR TO SEND
FG : FRAME GROUND

Fig. 3-2

4. Application specification

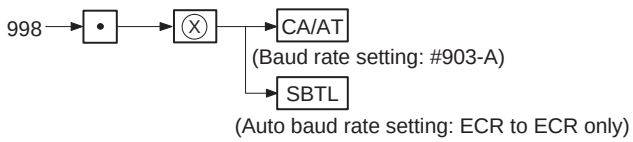
The following service (SRV) modes are available for the serial data transfer of the ECR

1) Data transmit (Source side)



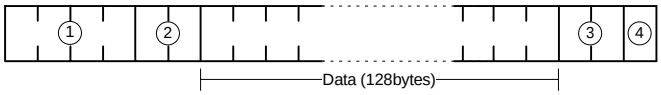
X: 0=SSP DATA

2) Data receive (Target)



5. Data format

A single byte image of the RAM data to be transmitted is divided into a high order 4 bits and low order 4 bits and converted into ASCII code. Then, the image of the memory is sent in the following format:



① Memory top address: 0000H ~ FFFFH
Top address of the memory to be transmitted in ASCII number.

② Page:1F ~ 27,00
Page of the memory to be transmitted in ASCII number.

③ Sum check

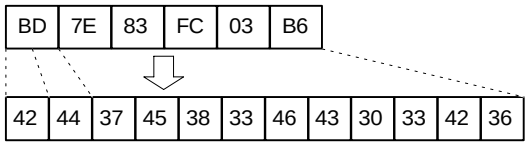
④ End code: Hex 0D

NOTE:

- In order that contents of RAM memory may not over-ride pages for this job, RAM image is sent in unit of 64 bytes from the address 0000. In other words, 128 bytes are sent at one time on the transmit data format.

RAM DATA FORMAT

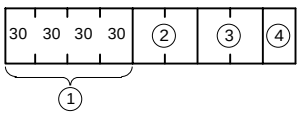
Exhibit:



Code table

HEX	ASCII	Character	HEX	ASCII	Character
0	30	0	8	38	8
1	31	1	9	39	9
2	32	2	A	41	A
3	33	3	B	42	B
4	34	4	C	43	C
5	35	5	D	44	D
6	36	6	E	45	E
7	37	7	F	46	F

6. END record



① End message: Fixed to 30303030.

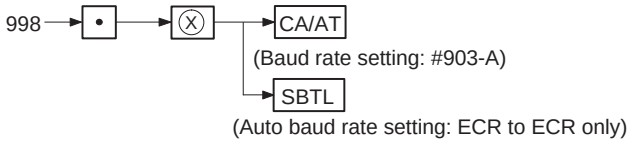
② End massage: Fixed to 4646.

③ Sum check

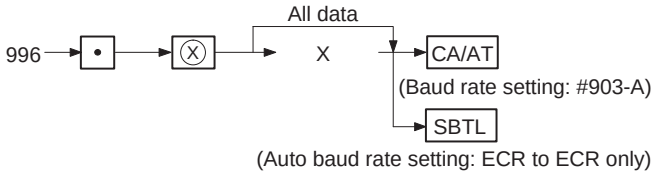
④ End code: CR (0D)

7. Operational method

1) To prepare an ECR to receive data from another ECR or the ER-02FD, the memory size of the receiving unit must the same as or greater than the sending unit.
2) Master reset the receiving ECR.
3) Connect loader cable between ECRs.
4) Set the receiving ECR ready to receive.



5) Start the sending ECR.



X: 0 = SSP

6) Transmission status.

Description of error status

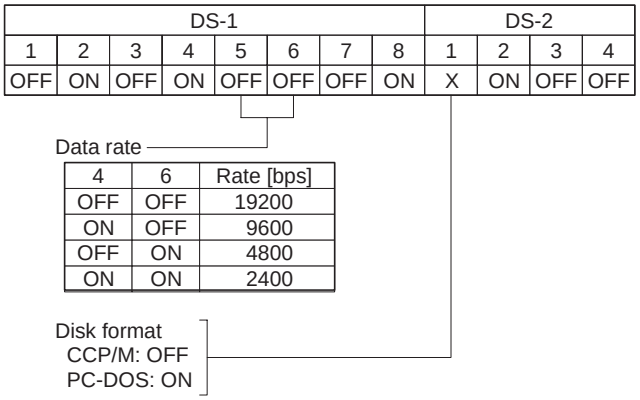
1: Application error (Command error)
2: Application error (Parity error)
3: Application error (Check sum error)
4: Application error (Data size error)
5: Hard ware error
6: Power off error
7: Time out error
11: Application error (Transmit data size error)
12: Application error (Block sequence error)

7) Service reset the receiving ECR.

8. Saving/Loading of data to/From the FD unit Configuration

1) Turn off the power switch of the ER-02FD, and set the DIP switches of the FD unit as follows:

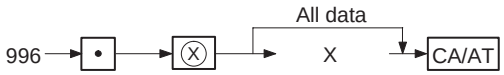
ER-02FD (The ER-01FD functions of the ER-02FD are used.)



2) Connect the cable.

Saving data

1) Turn on the power switch and insert a floppy disk which has been formatted.
2) Start the SEND JOB on the ECR side as follows:

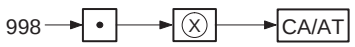


X: 0 = SSP

3) Data transmission is started and the green lamp on the ER-02FD blinks.

Loading data

1) Turn on the power switch and insert the floppy disk which stores the data.
2) Start the RECEIVE JOB on the ECR side as follows:



3) Press the SEND key on the FD unit.
4) Data transmission is started and the Green lamp on the ER-02FD blinks.
5) Service reset the ECR.

CHAPTER 7. SERVICE PRECAUTION

1. Error code table

When the following error codes are displayed, press the ₹ key and take a proper action according to the table below.

Error code	Error status	Action
E01	Registration error	Make a correct key entry.
E02	Misoperation error	Make a correct key entry.
E03	Undefined code is entered.	Enter a correct code, or declare it by the programming.
E04	Paper empty	Replace a journal paper roll with a new one.
E05	Secret code error	Enter a correct secret code.
E07	Memory is full.	Expand the file within a capacity of memory.
E11	Compulsory depression of the *i* key for direct finalization	Press the *i* key and continue the operation.
E12	Compulsory tendering	Make a tendering operation.
E26	File type error	Create files correctly.
E27	Power-off	
E31	Compulsory non-add code entry	Enter a non-add code.
E32	No entry of your cashier code	Make a cashier code entry.
E33	The current cashier code should not be changed.	Change a cashier after finalizing the transaction.
E34	Overflow limitation error	Make a registration within a limit of entry.
E35	The open price entry is inhibited.	Make a preset price entry.
E36	The preset price entry is inhibited.	Make an open price entry.
E37	The direct finalization is inhibited.	Make a tendering operation.
E39	Power-off during validation printing	Print a validation again.
E67	Registration buffer is full.	
E76	The drawer is still opened.	Close the drawer.
E86	Communication error	
E87	Data format error	
E88	Time-out error	
E94	Age verification error	The dept./PLU is protected by the age limitation.

2. Conditions for soldering circuit parts

To solder the following parts manually, follow the conditions described below.

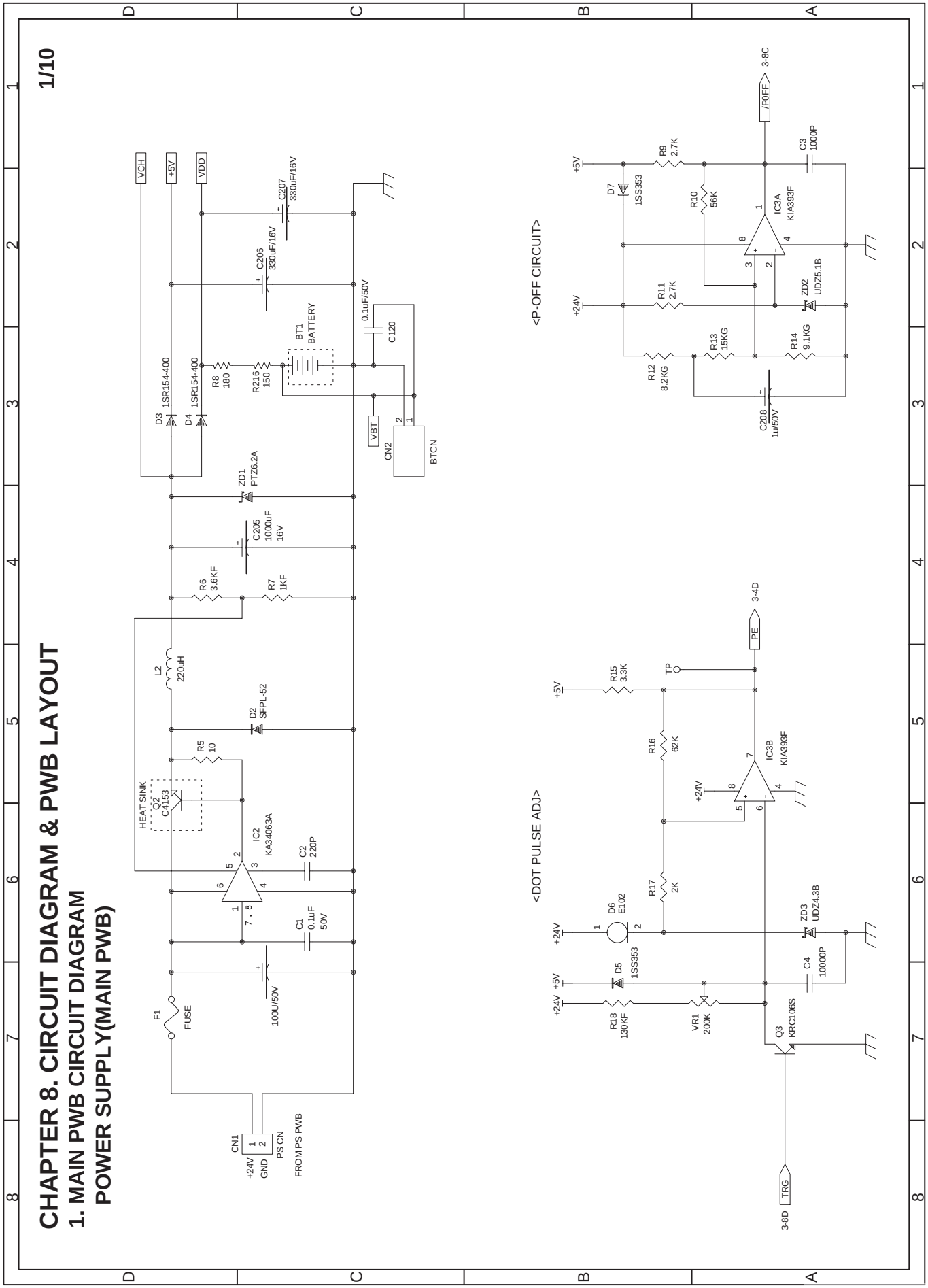
PARTS NAME	PARTS CODE	LOCATION	CONDITIONS FOR SOLDERING
Front LED (HDSP5621)	VHPHDSP5621−1	Front LED PWB: FND1-5	315°C/2 sec.
Pop-up LED (HDSP-F501#S02)	VHPHDSPF501−1	Pop-up LED PWB: FND1-10	315°C/2 sec.

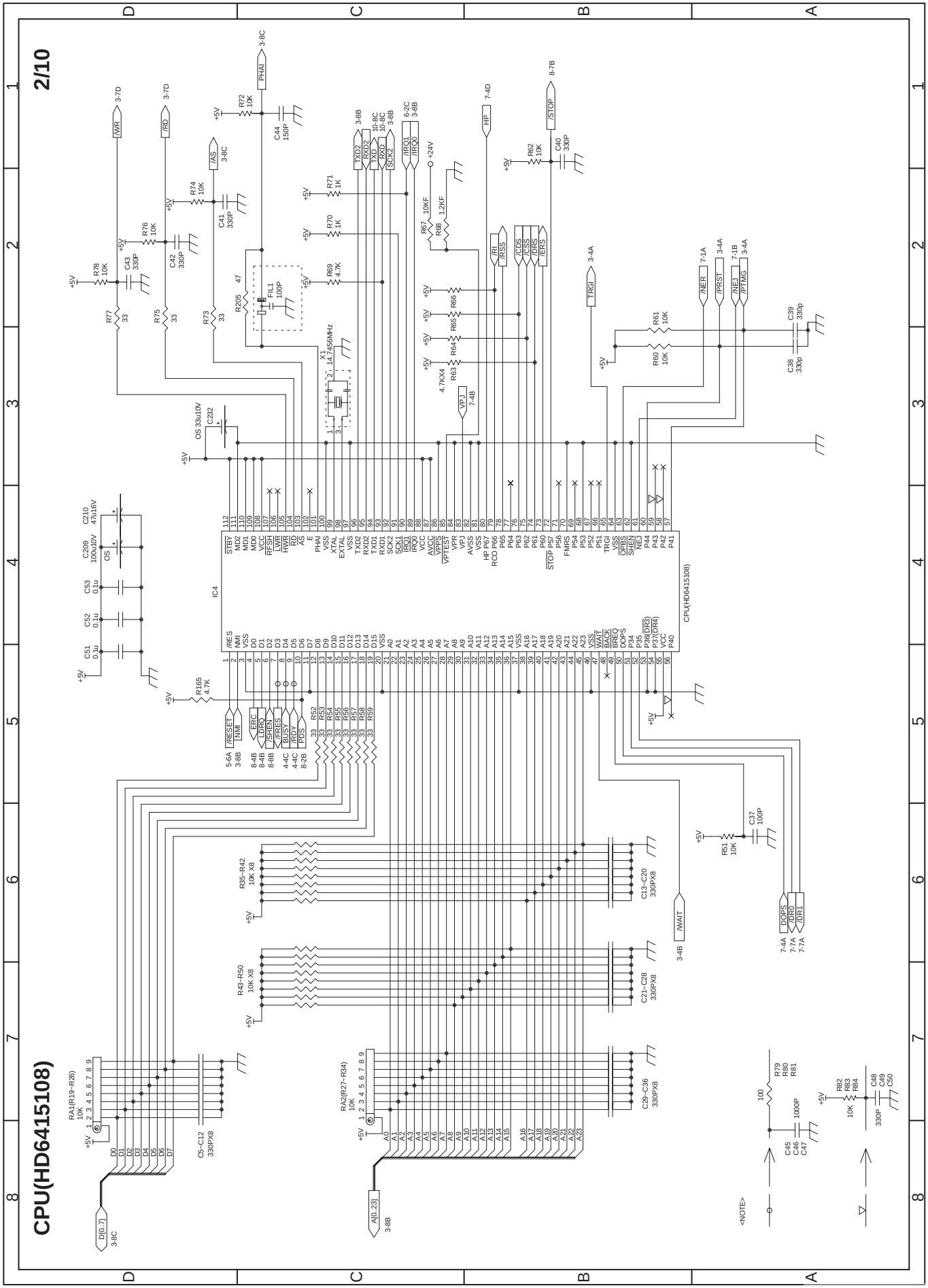
CHAPTER 8. CIRCUIT DIAGRAM & PWB LAYOUT

1. MAIN PWB CIRCUIT DIAGRAM

POWER SUPPLY(MAIN PWB)

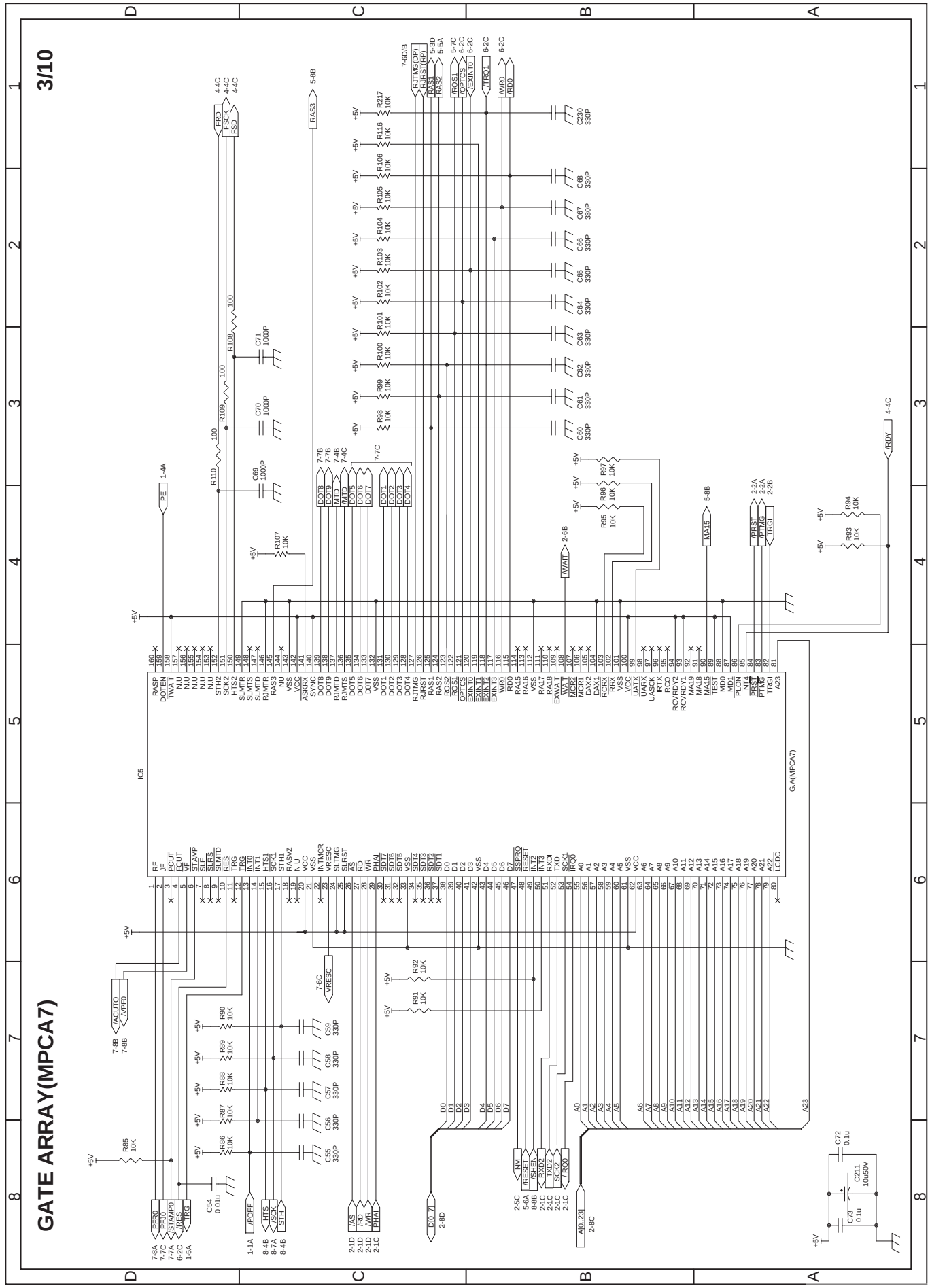
1/10





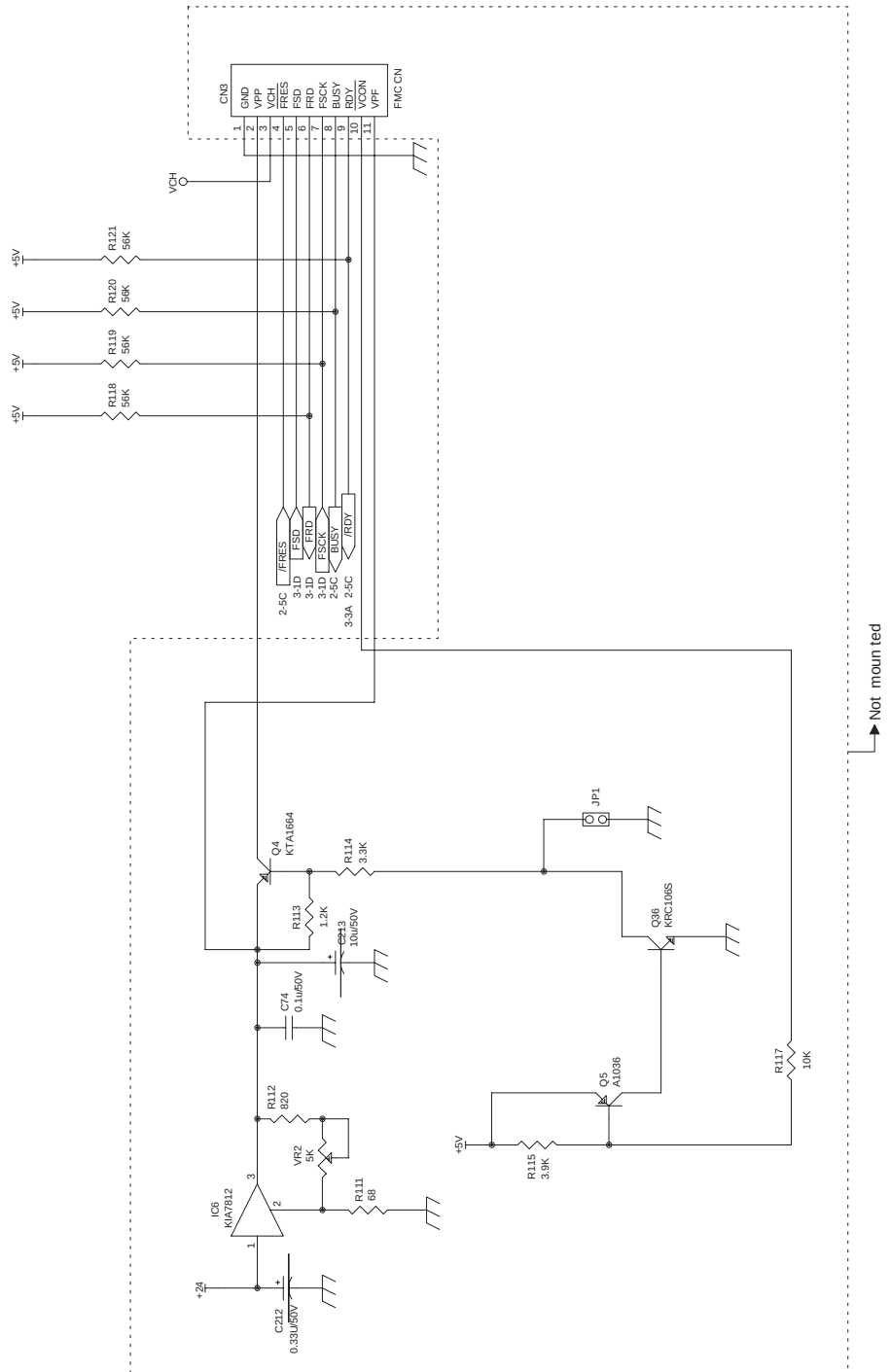
GATE ARRAY(MPCA7)

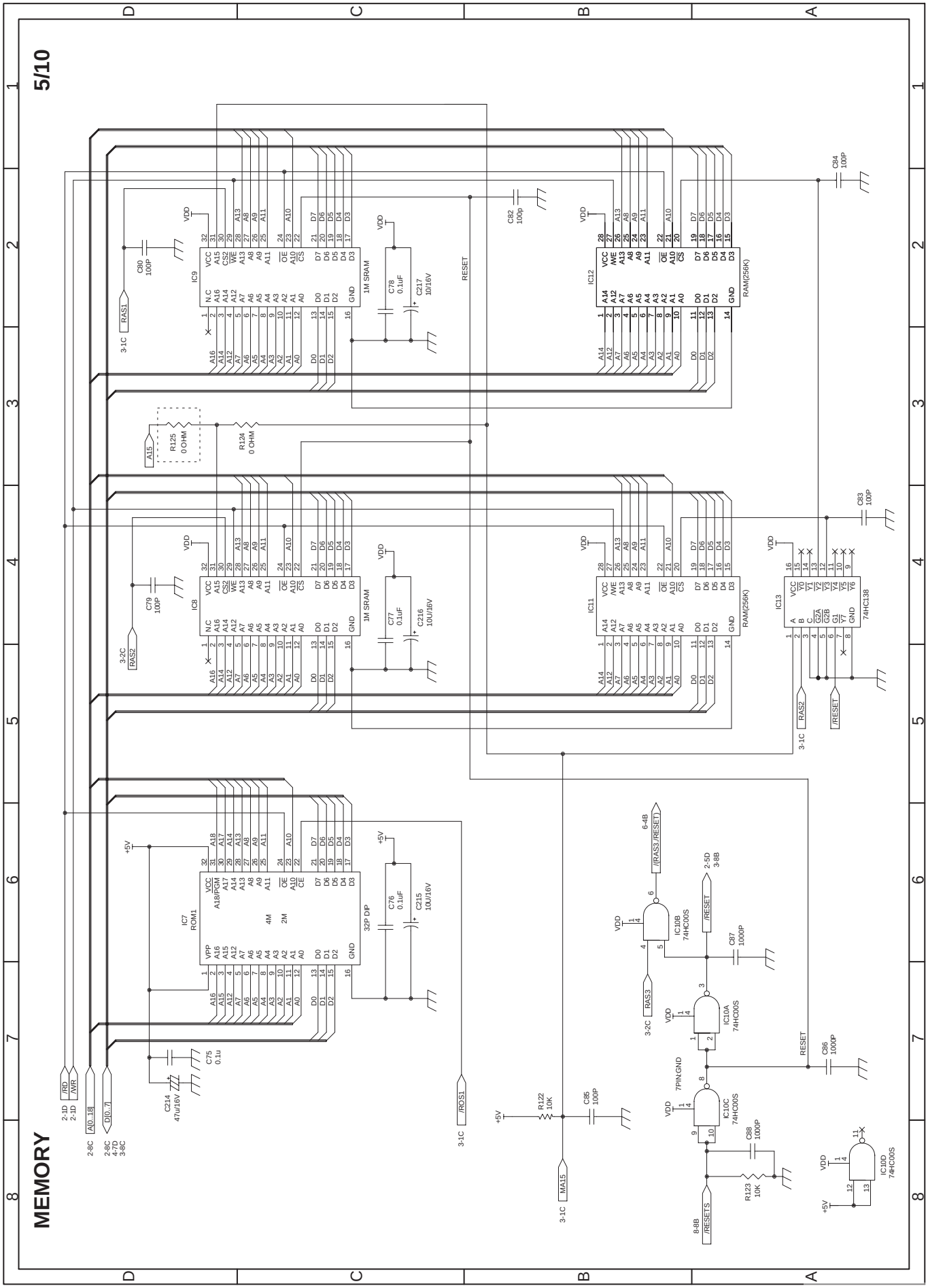
3/10



FMC CONTROL CIRCUIT (NOT USED)

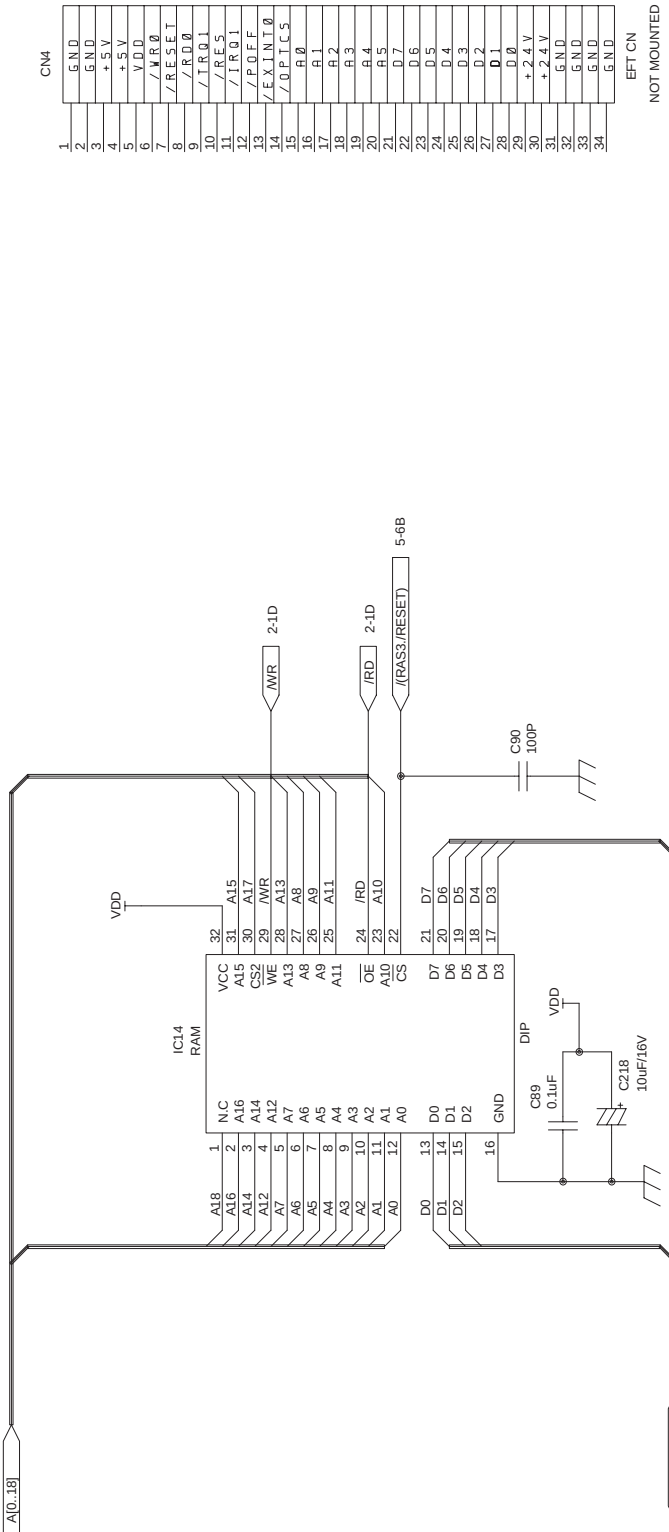
4/10

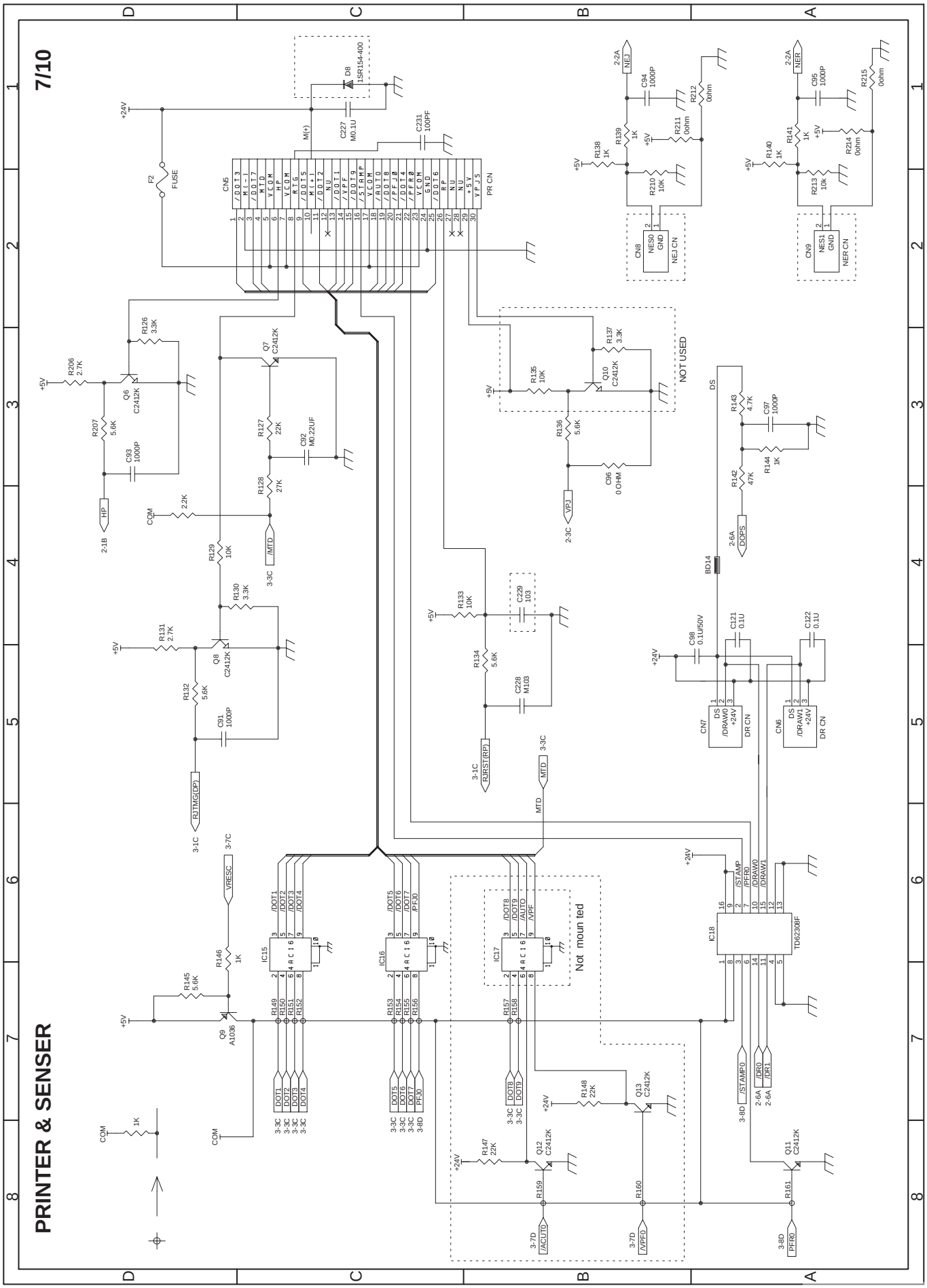




OPTION MEMORY (OPT CN)

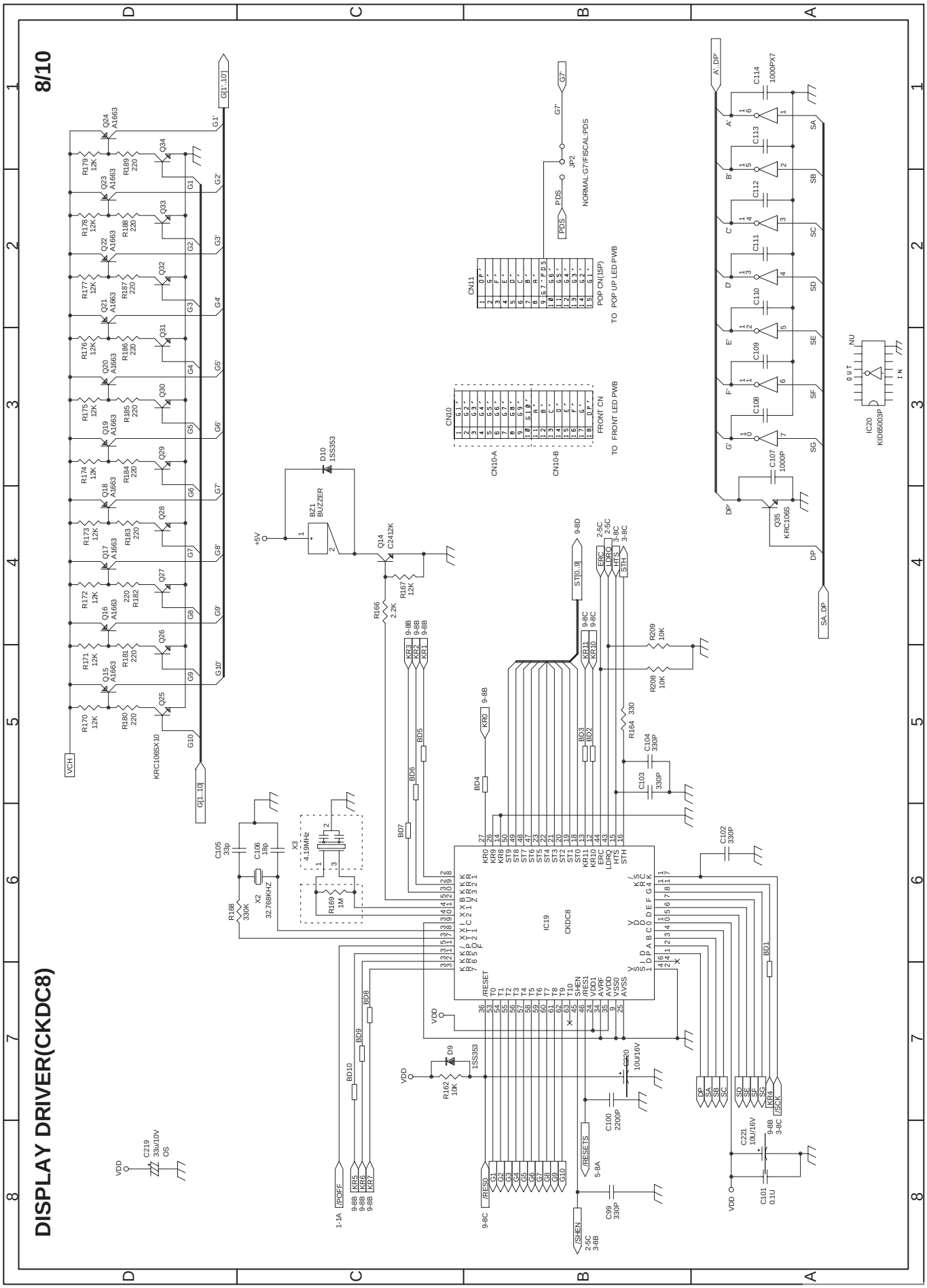
6/10

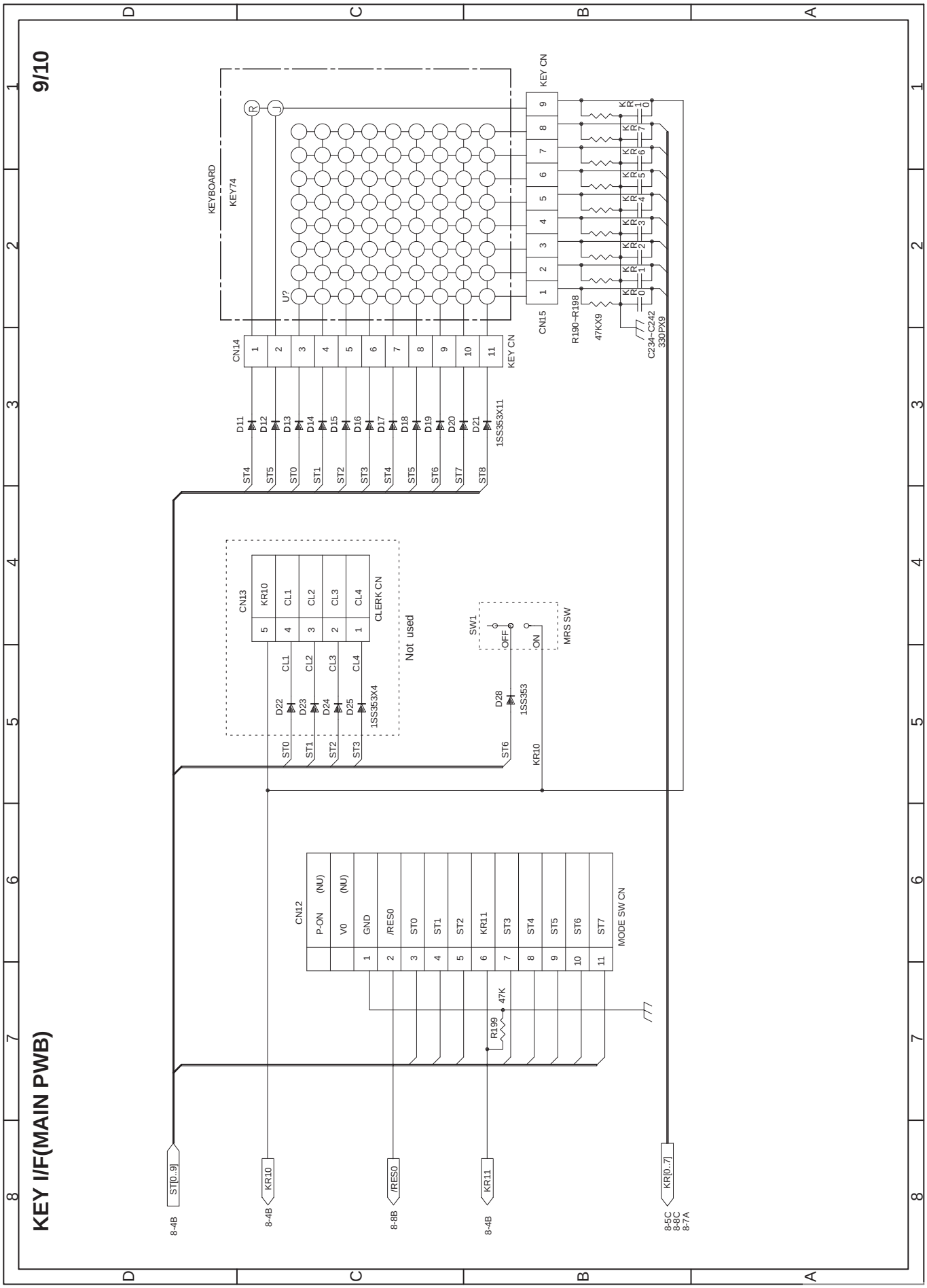


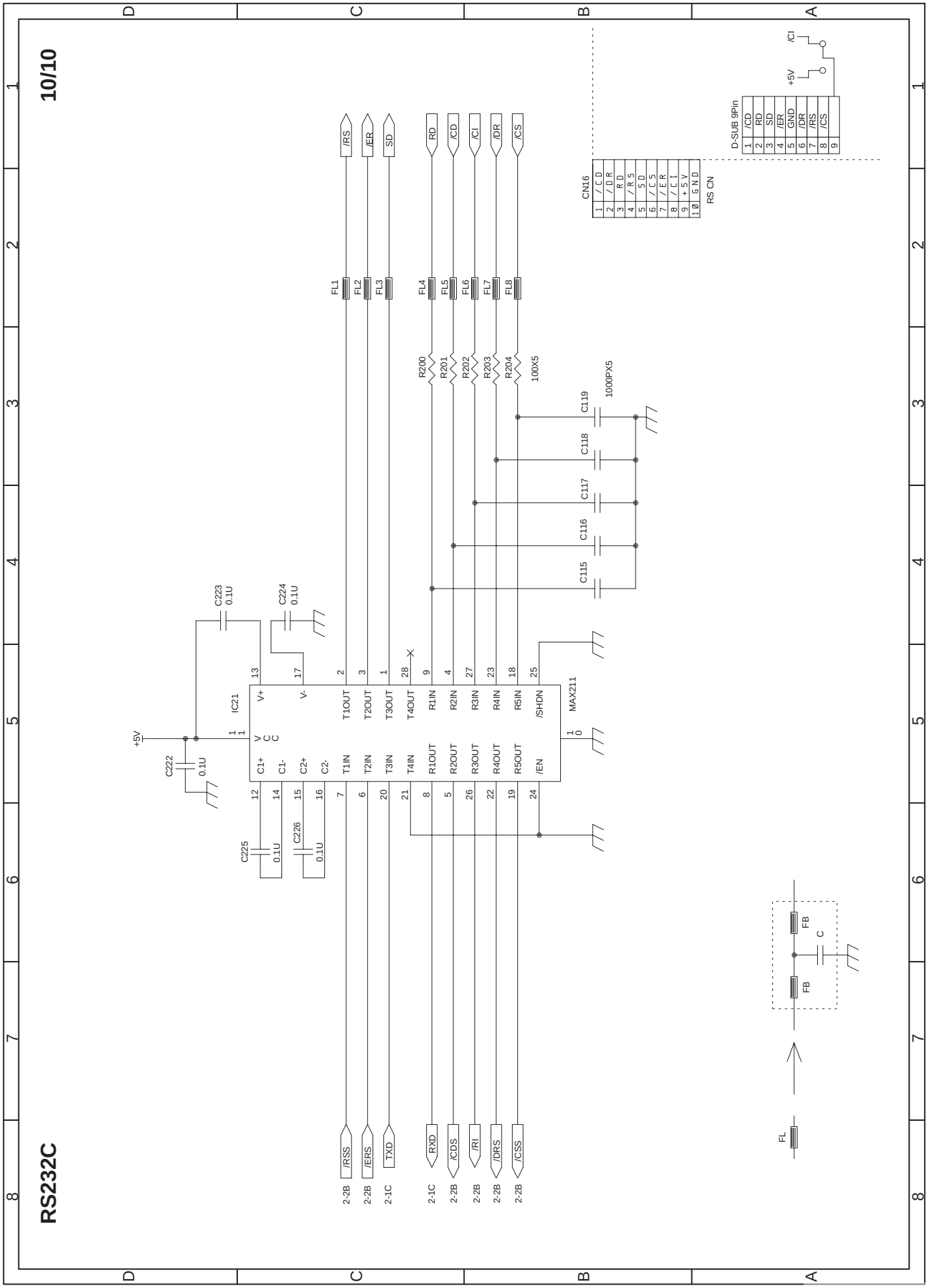


8/10

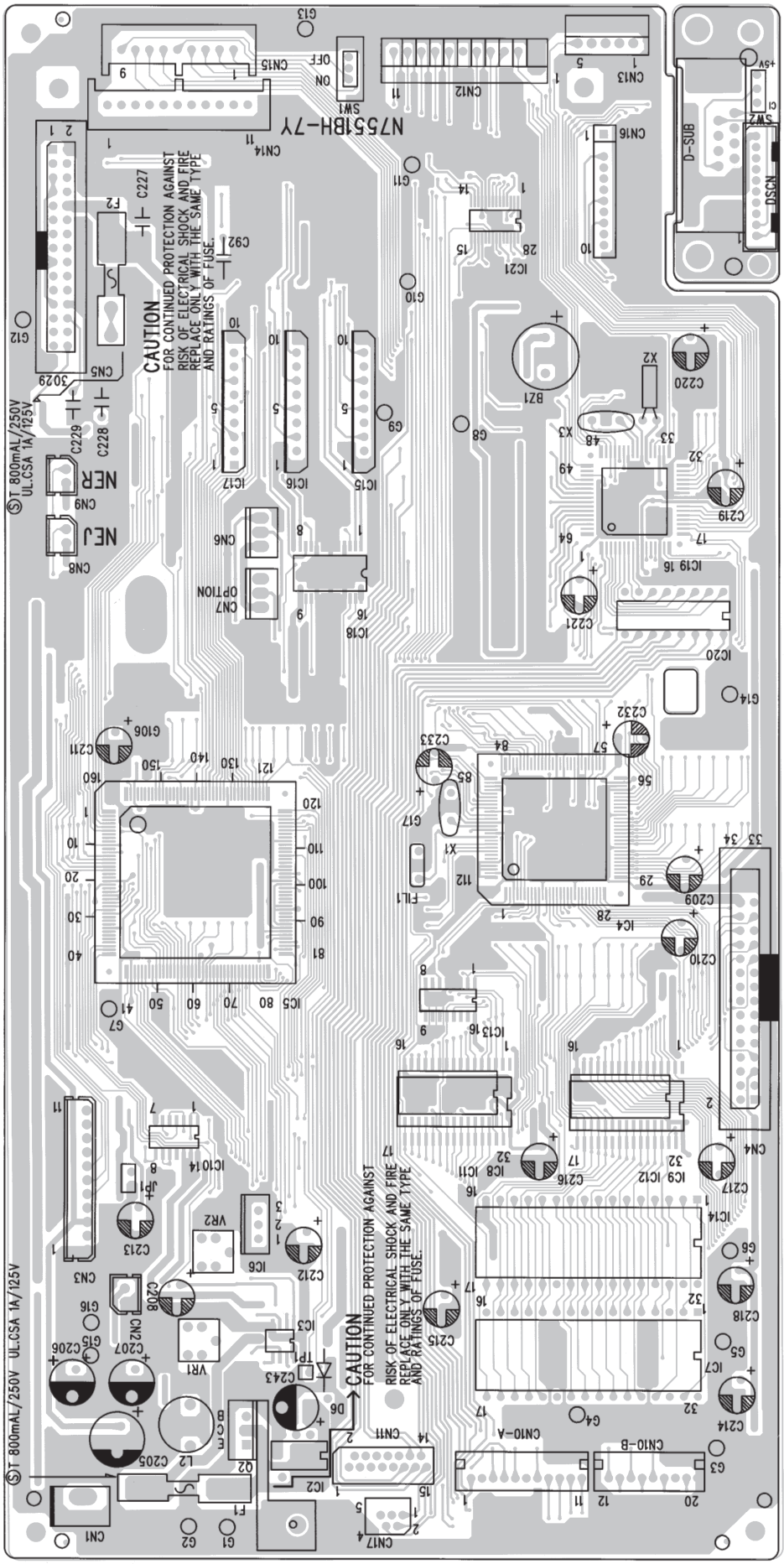
DISPLAY DRIVER(CKDC8)



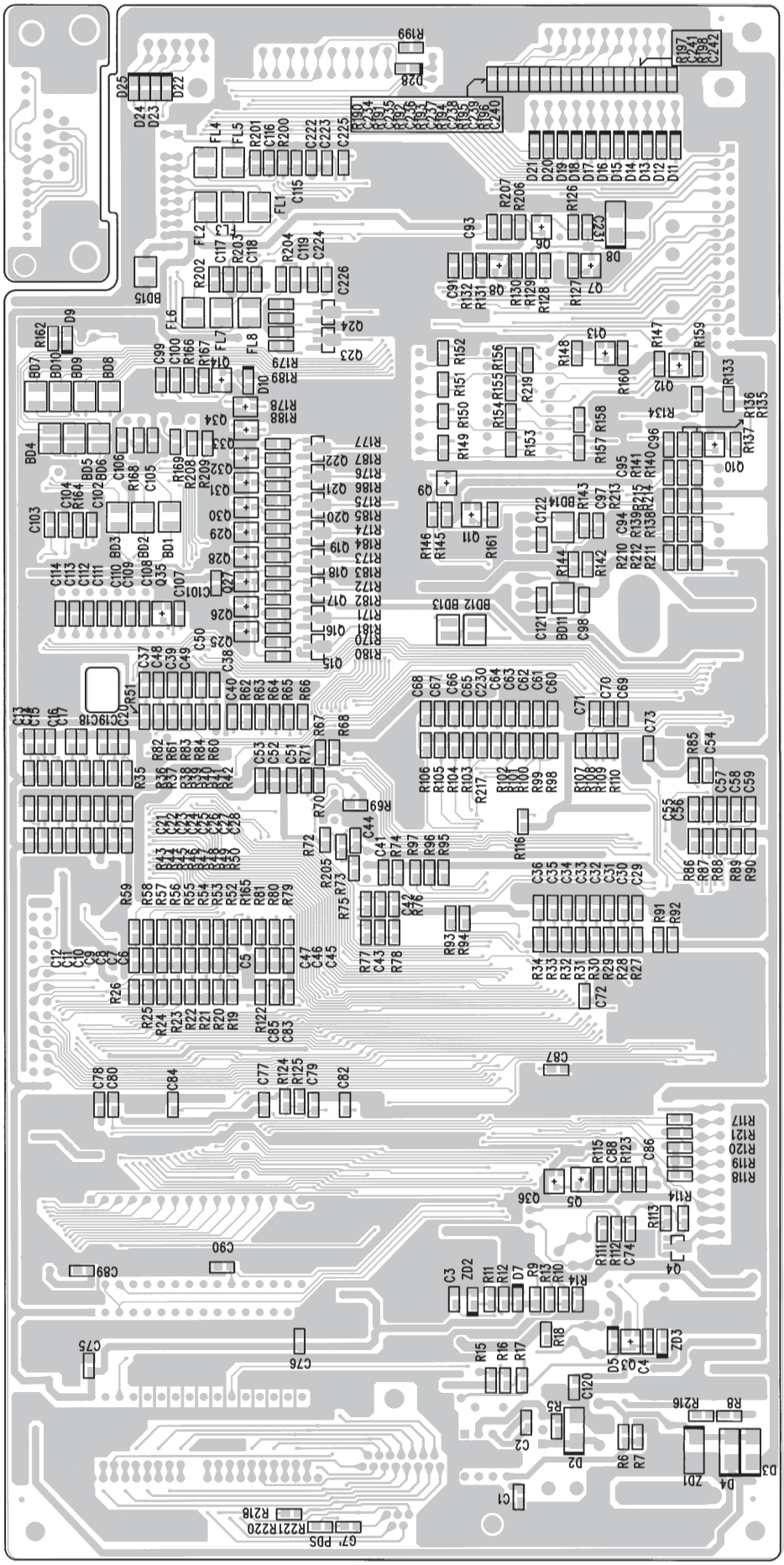




2. MAIN PWB LAYOUT
(1) SIDE A

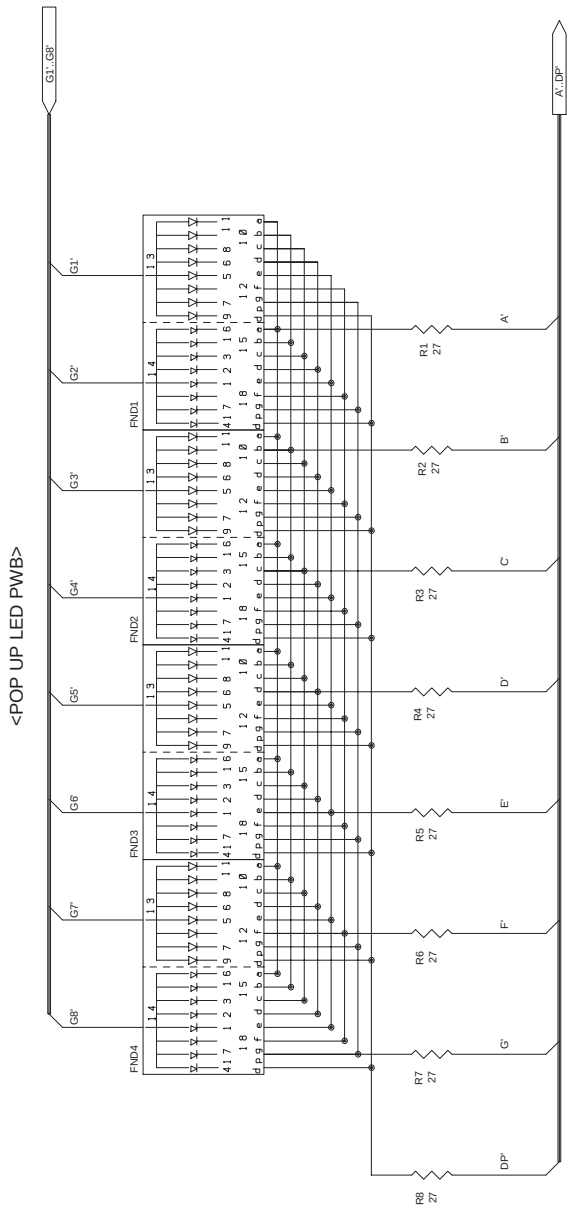


(2) SIDE B



3. FRONT PWB/POP UP PWB

1/1

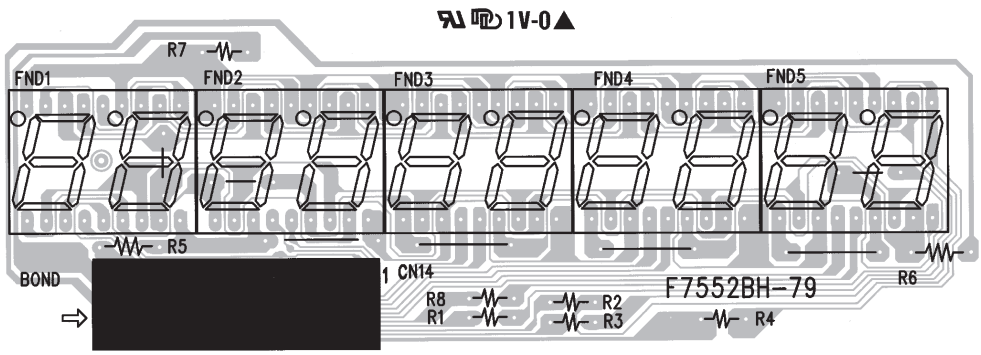


CN1

1	G1'
2	G2'
3	G3'
4	G4'
5	G5'
6	G6'
7	G7'
8	A'
9	B'
10	C'
11	D'
12	E'
13	F'
14	G'
15	DP'

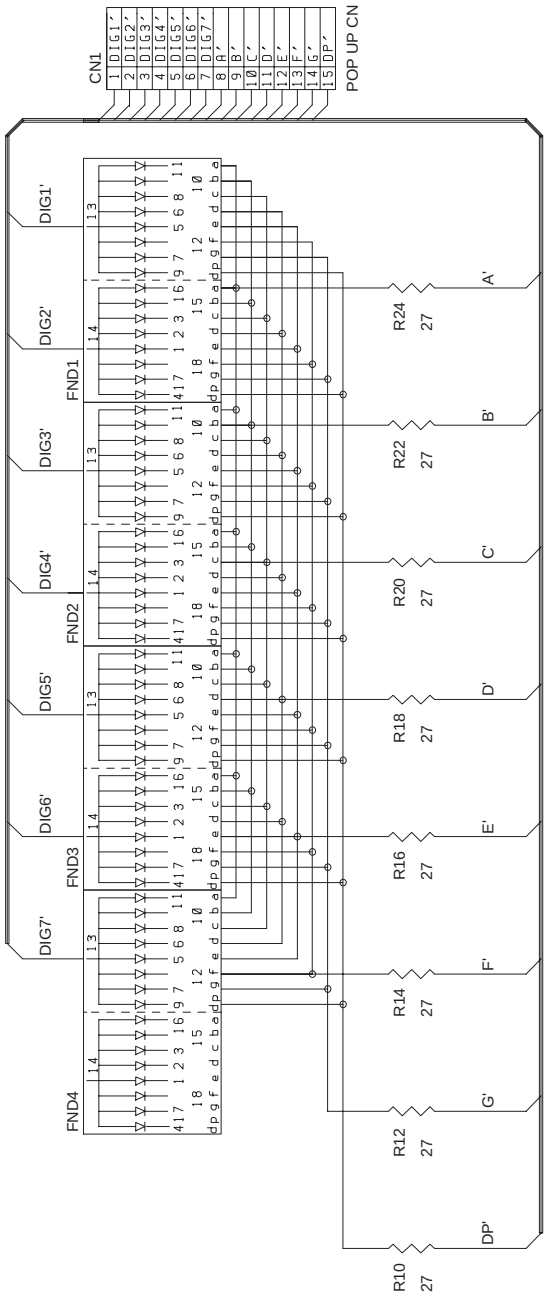
POP CN(NORMAL)

4. FRONT DISPLAY PWB

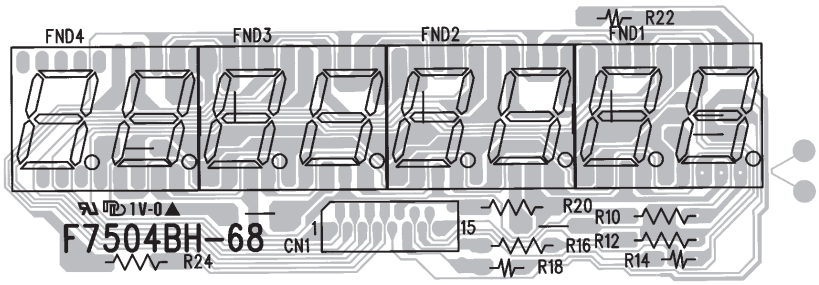


1/1

5. POP-UP PWB

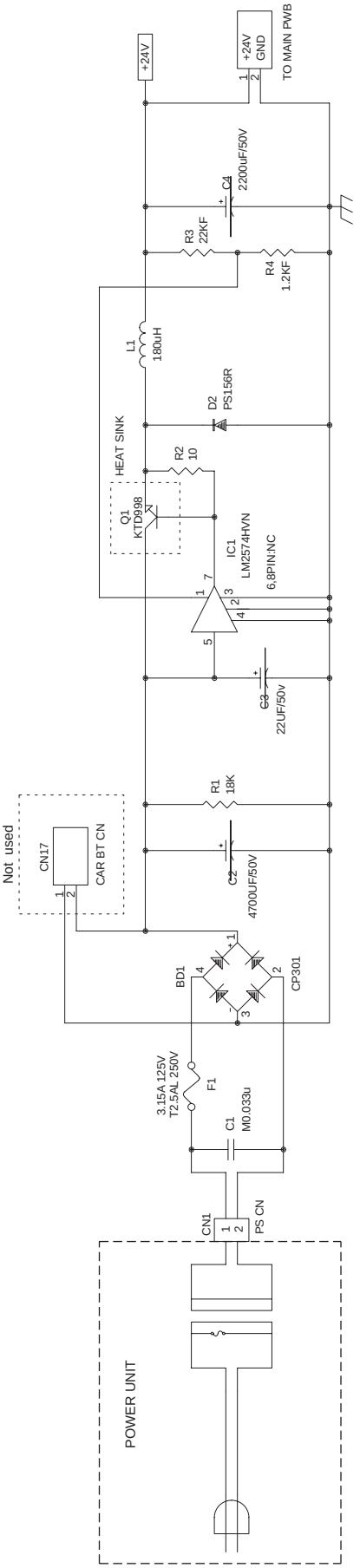


6. POP-UP DISPLAY PWB

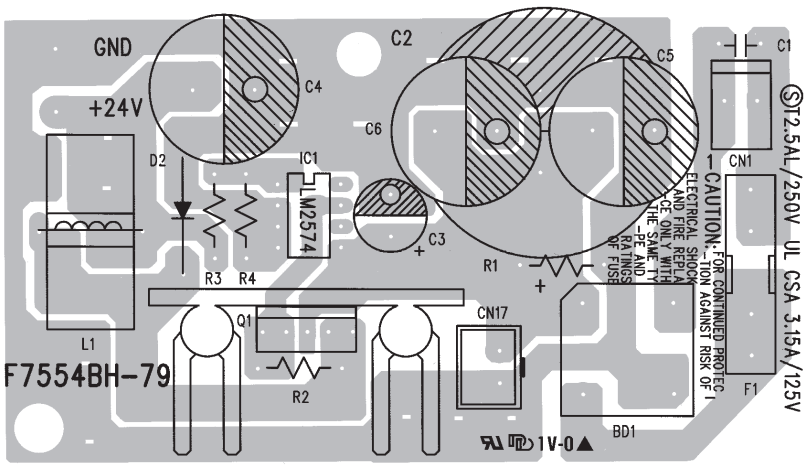


7. PS PWB

1/1



8. PS PWB



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Yamatokoriyama, Nara 639-1103, Japan
1998 March Printed in Japan