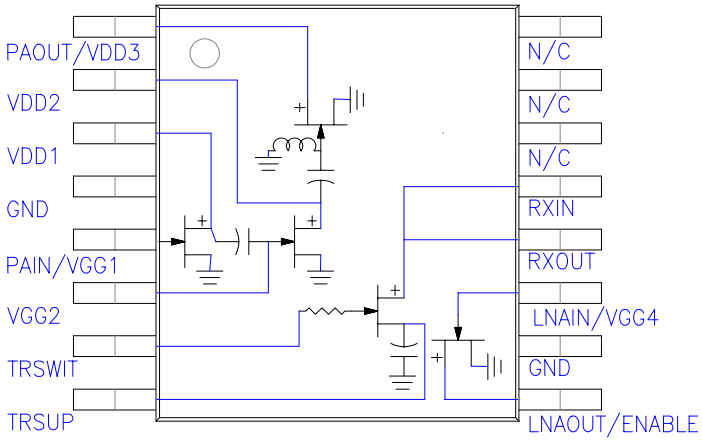
3.6V Integrated RF Front-End for DECT
ITT2207GF

PRELIMINARY

FEATURES

- 3.6V Operation
- Single Positive Supply
- 55% Power Added Efficiency
- 100% Duty Cycle
- 1.6 dB LNA Noise Figure
- 16 Pin TSSOP Full Downset Plastic Package
- Self-Aligned MSAG®-Lite MESFET Process



DESCRIPTION

The ITT2207GF is an integrated DECT front-end based on GaAsTEK's GaAs Self-Aligned MSAG® MESFET Process. This product has an integrated power amplifier, low noise amplifier, and switch in one surface mount package.

MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	+5.5	V
Reverse DC Supply Voltage	$-V_{DD}$	-0.7	V
RF Input Power, PA_{IN}	P_{IN}	+10	mW
RF Input Power, LNA_{IN}	P_{IN}	+10	mW
Junction Temperature	T_J	+150	°C
Storage Temperature	T_{STG}	-40 to +175	°C

ELECTRICAL CHARACTERISTICS T_s (Solder Point Temperature) = 40 °C

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency	f	1880	—	1930	MHz
Transmit Path (Power Amplifier + T/R Switch) $V_{DD1,2,3}$= 3.6V, P_{IN}=-2 dBm, TR_{SUP}=3.6V, TR_{SWIT}=3.6V, LNA_{ENABLE}=0.0V, f=1900MHz					
Load Power (at Ant)	P_{OUT}		25		dBm
Current Consumption	$I_{DD1,2,3}$		226		mA
Input VSWR				2:1	
Harmonics	—		-41		dBc
Duty Cycle	—			100	%
Forward Isolation (RF_{IN} to Ant) $V_{DD1,2,3}$=0.0V	—		54		dB
Forward Isolation (ANT to LNA_{OUT})	—		34		dB
Receive Path (T/R Switch + Low Noise Amplifier) $V_{DD1,2,3}$= 0.0V, TR_{SUP}=3.6V, TR_{SWIT}=0.0V, LNA_{ENABLE}=2.4V, f=1900MHz					
Current Consumption	LNA_{ENABLE}		4.3		mA
Noise Figure (Ant to LNA_{OUT})	NF		2.1		dB
Gain (Ant to LNA_{OUT})	G		15		dB
Third-Order Input Intercept Point	IIP_3		3.5		dBm
Reverse Isolation (LNA_{OUT} to ANT)	—		18		dB
Thermal Resistance (Junction of 3rd stage FET to solder point of pin 13)	R_{th}		37.5		°C/W

GaAsTEK
A UNIT OF ITT INDUSTRIES
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
Tel: 1-540-563-3949
1-888-563-3949 (USA)
Fax: 1-540-563-8616

TYPICAL CHARACTERISTICS

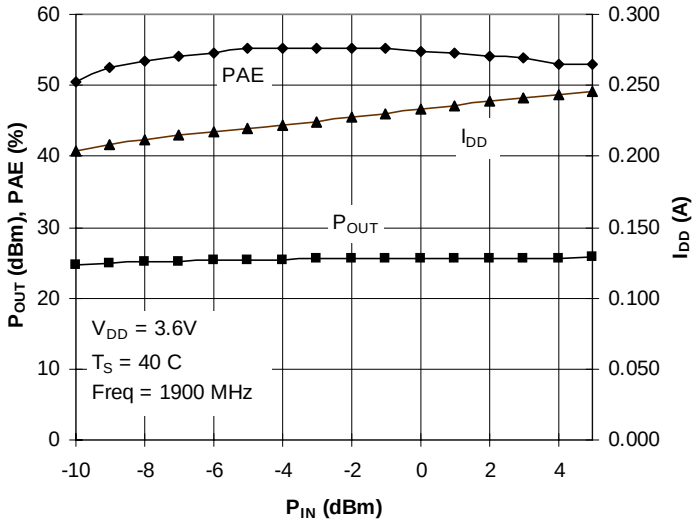


Figure 1. Output power, efficiency and supply current vs. input power

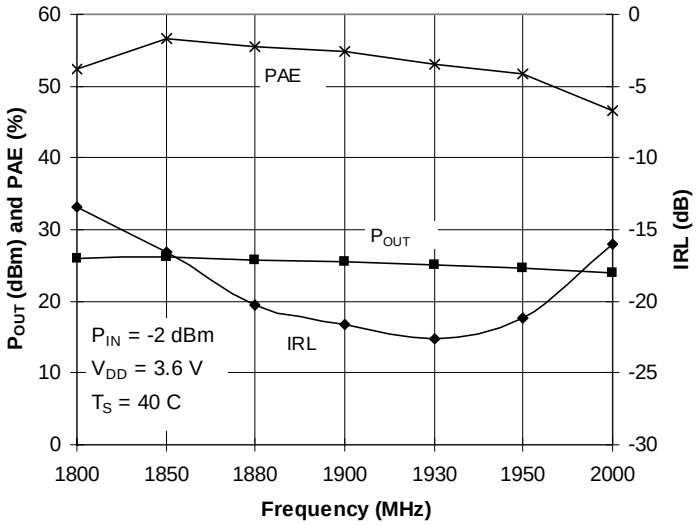


Figure 2. Output power, efficiency and input return loss vs. frequency.

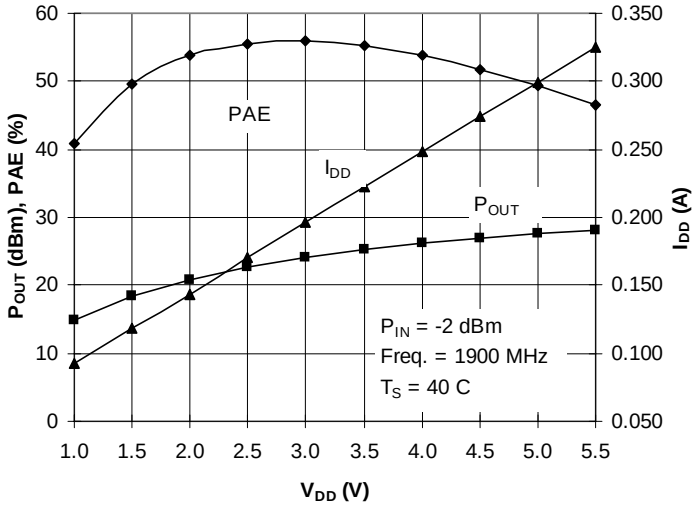


Figure 3. Output power, efficiency and supply current vs. supply voltage

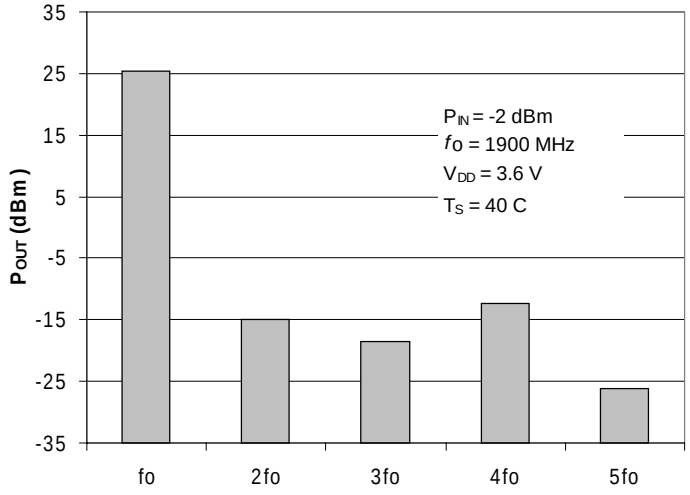


Figure 4. Harmonics

GaAsTEK
5310 Valley Park Drive
Roanoke, VA 24019 USA
www.gaastek.com
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1-888-563-3949 (USA)
Fax: 1-540-563-8616

TYPICAL CHARACTERISTICS (CONT)

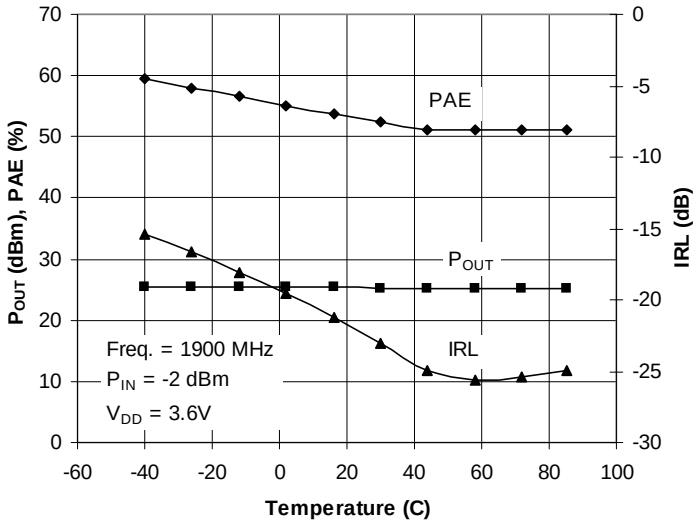

Figure 5. Output power, efficiency and supply current vs. temperature

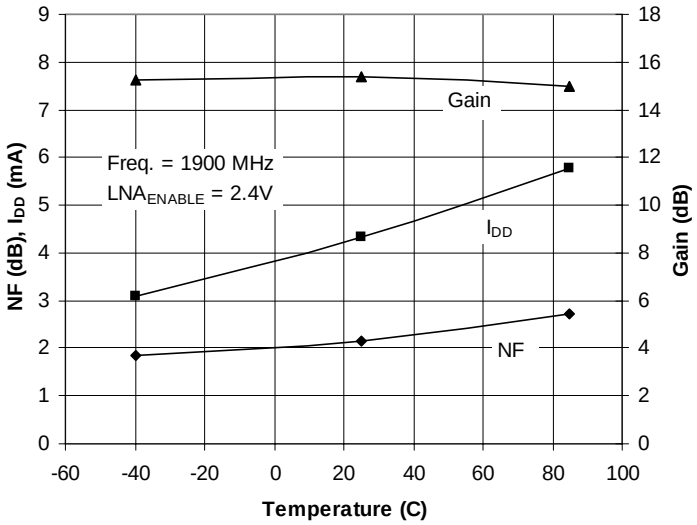

Figure 6. Noise figure, gain and supply current vs. temperature

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5310 Valley Park Drive
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APPLICATION INFORMATION

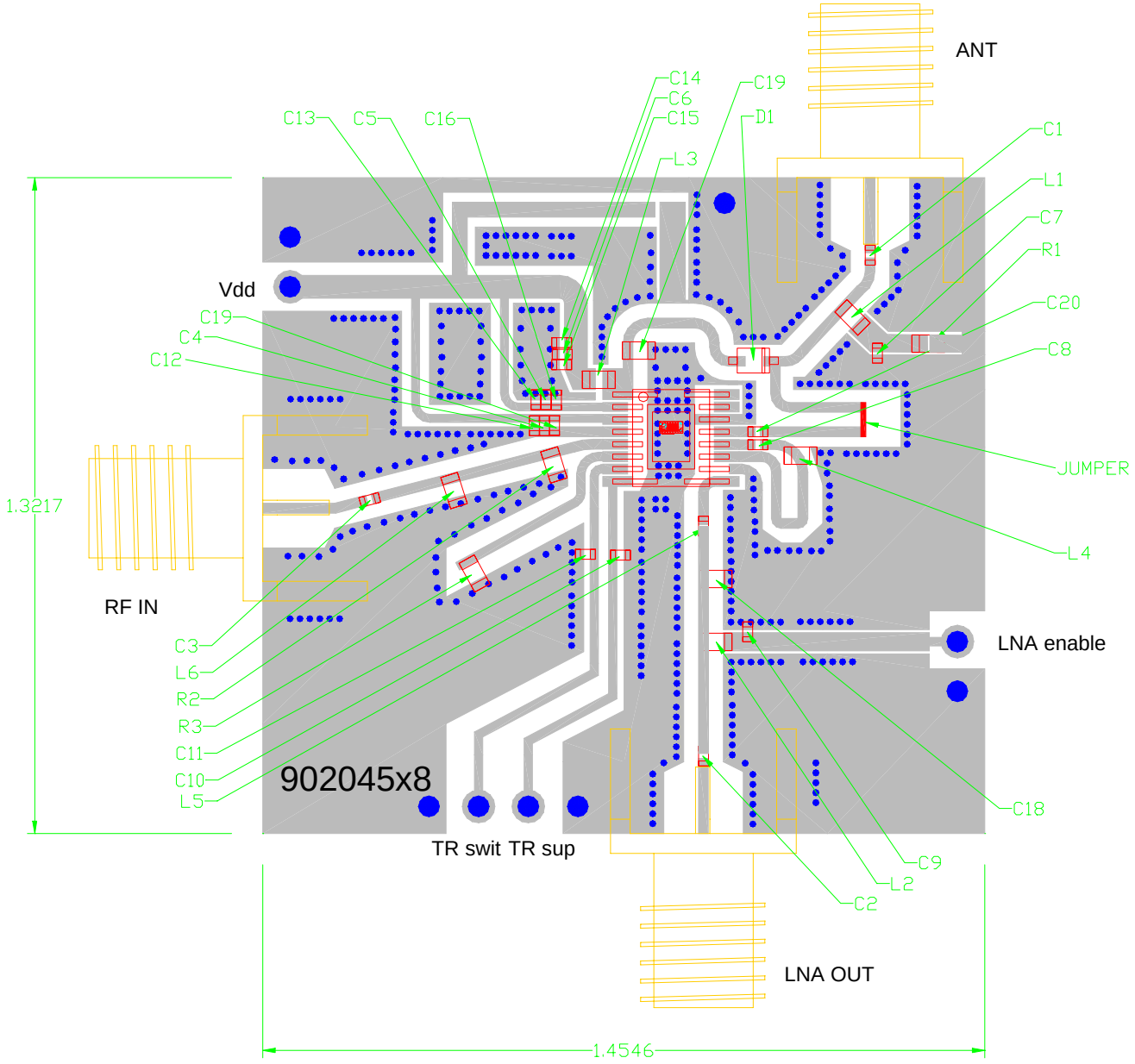

Figure 7. Component layout and printed circuit drawing for evaluation board.

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APPLICATION INFORMATION (CONT)

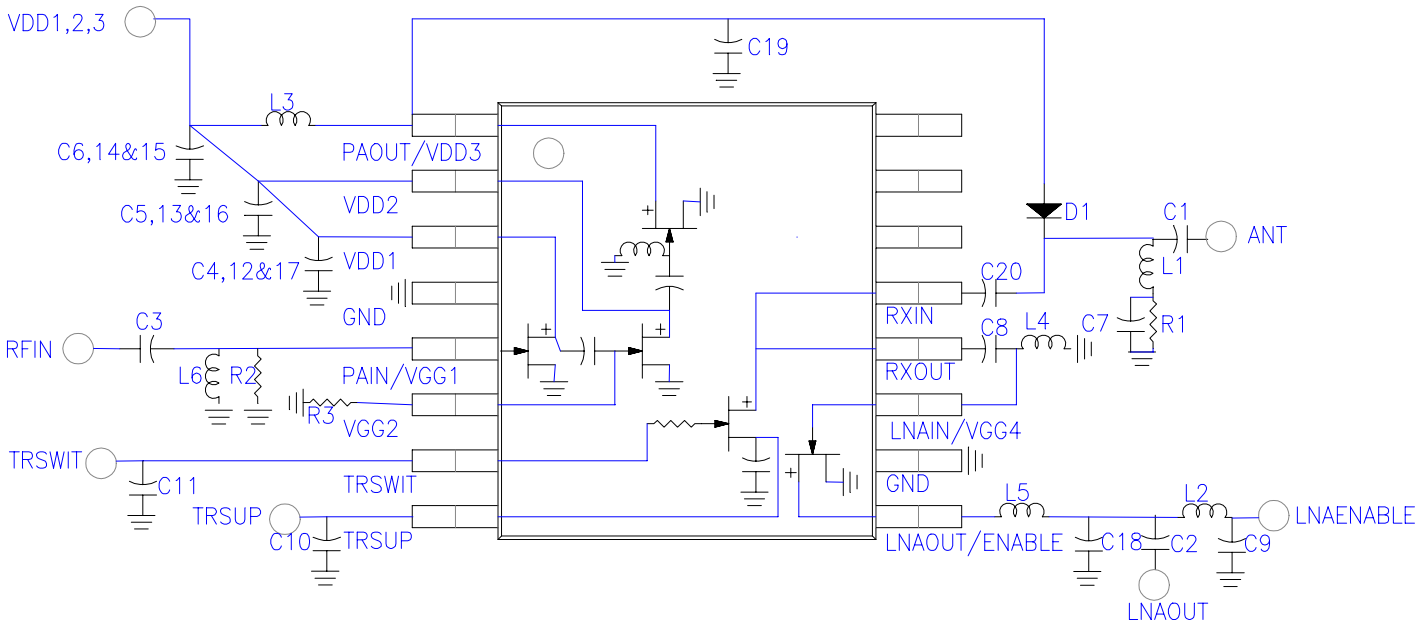

Figure 8. Evaluation Board Schematic

External components:

C1 – C11	MuRata 100 pF 0402 GRM36C0G101J50
C12 – C14	MuRata 0.1 µF 0402 GRM36Y5V104Z1
C15 – C17	MuRata 33 pF 0402 GRM36C0G330J50
C18	Dielectric Labs 2.2 pF 0603 C06CF2R2B5UL
C19	Dielectric Labs 2.4 pF 0603 C06CF2R4B5UL
C20	MuRata 22 pF 0402 GRM36C0G220G50
L1 – L3	Coilcraft 27 nH 0603 0603CS-27NXJBB
L4	Toko 3.3 nH 0603 LL1608-F3N3K
L5	Coilcraft 7.5 nH 0402 0402 0402CS-7N5XJB
L6	Toko 2.7 nH 0805 LL2012-F2N7S
R1 – R2	Panasonic 301Ω 0603 ERJ-3EKF3010
R3	Panasonic 10 Ω 0603 ERJ-3EKF10R0V
D1	Siemens Pin Diode BAR6303W

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GaAsTEK TEST SET UPS

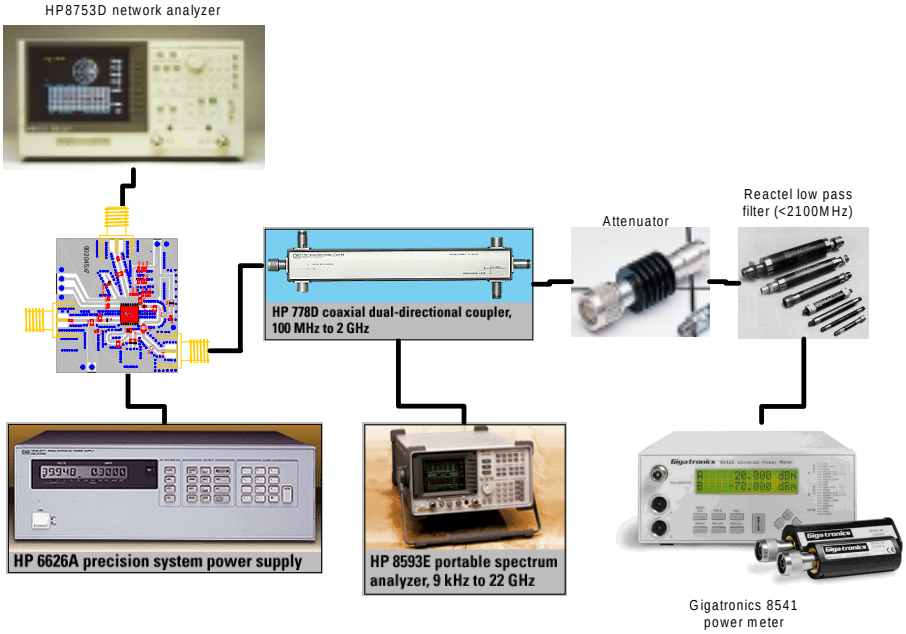

Figure 9. Transmit path power, current, and spurious.

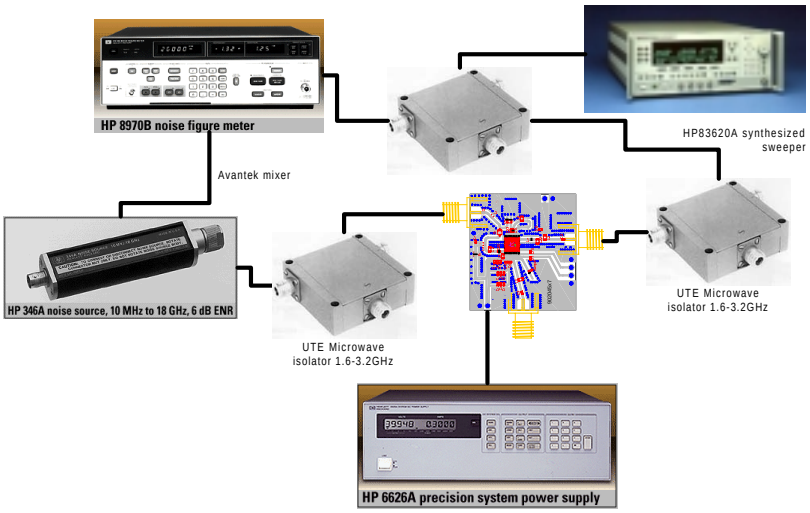

Figure 10. Receive path noise figure and gain.

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