

# 8-bit, serial IN, parallel OUT driver

## BA829

The BA829 is an 8-bit, serial input, parallel output driver. This is a monolithic IC developed for use in thermal print heads, LED character displays, and other similar applications.

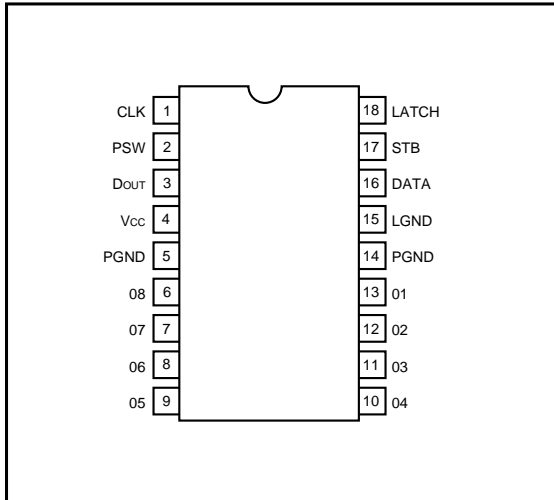
### ●Applications

Thermal print head drivers  
LED character displays

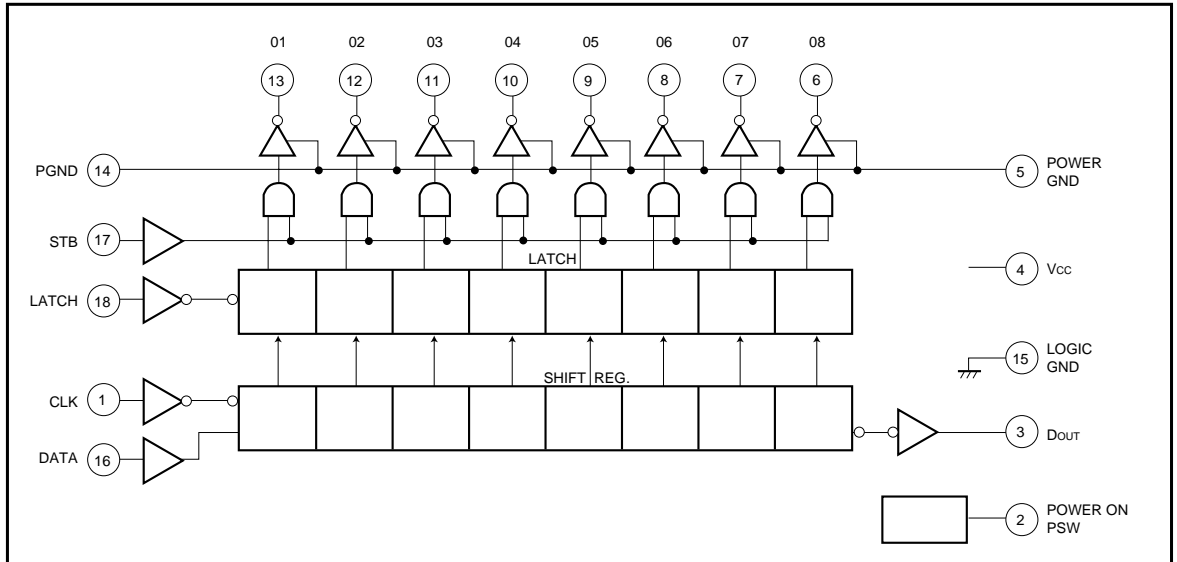
### ●Features

- 1) Can drive up to 300mA.
- 2) Controlling the strobe terminal with the drive timing pulse enables current to be reduced when drive is not being carried out.
- 3) Using the data output terminal for the next data input enables secondary connections.
- 4) The digital ground and power ground are separated.
- 5) A latch is included between the shift register and driver output.
- 6) A stand-by function is built in.  
(10 $\mu$ A typ. at stand-by)

### ●Pin assignments



●Block diagram



●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Applied voltage	V <sub>CC</sub>	7.0	V
Power dissipation	P <sub>d</sub>	1100	mW
Operating temperature	T <sub>opr</sub>	- 25 ~ + 70	°C
Storage temperature	T <sub>stg</sub>	- 55 ~ + 125	°C
Input voltage	V <sub>IN</sub>	- 0.3 ~ V <sub>CC</sub>	V
Output voltage	V <sub>OUT</sub>	15	V

● Recommended operating conditions (Topr = – 25 to + 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage	V <sub>CC</sub>	4.5	5.0	5.5	V	—
Clock frequency	t <sub>CLK</sub>	—	—	500	kHz	—
Power setup time	t <sub>Pset</sub>	500	—	—	ns	Fig.4
Clock pulse width	t <sub>wC</sub>	1	—	—	μs	Fig.4
Data setup time	t <sub>Dset</sub>	300	—	—	ns	Fig.4
Data hold time	t <sub>Dhold</sub>	400	—	—	ns	Fig.4
Latch pulse timing time 1	t <sub>LT1</sub>	600	—	—	ns	Fig.4
Latch pulse timing time 2	t <sub>LT2</sub>	250	—	—	ns	Fig.4
Latch pulse width	t <sub>wL</sub>	800	—	—	ns	Fig.4
Strobe pulse timing time 1	t <sub>ST1</sub>	300	—	—	ns	Fig.4
Strobe pulse timing time 2	t <sub>ST2</sub>	300	—	—	ns	Fig.4
Strobe pulse width	t <sub>wS</sub>	3	—	—	μs	Fig.4
Voltage between GNDs*	V <sub>G</sub>	—	—	0.2	V	—

\* This is the phase differential between the L-GND and the P-GND. Shorting should be kept as close to the power supply as possible, but the range should be such that the phase differential between the L-GND pin and the P-GND pin does not exceed 0.2V.

● Electrical characteristics (unless otherwise noted, Ta = 25°C, V<sub>CC</sub> = 5.0 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Measurement circuit
Supply current (1)	I <sub>CC1</sub>	—	10	20	μA	PSW "L"	Fig.1
Supply current (2)	I <sub>CC2</sub>	—	110	158	mA	PSW "H", STB "H"	Fig.1
Supply current (3)	I <sub>CC3</sub>	—	14	20	mA	PSW "H", STB "L"	Fig.1
Output pin ON voltage	V <sub>OON</sub>	—	0.4	0.6	V	I <sub>OON</sub> = 300mA	Fig.1
Output pin leakage current	I <sub>OOFF</sub>	—	10	50	μA	V <sub>O</sub> = 13.5V	Fig.1
Data transfer speed	f <sub>CLK</sub>	500	—	—	kHz	—	Fig.1
Input high level voltage	V <sub>IH</sub>	2.6	—	—	V	—	Fig.2
Input low level voltage	V <sub>IL</sub>	—	—	0.8	V	—	Fig.2
Input high level current	I <sub>IH1</sub>	—	0.1	10	μA	V <sub>I</sub> = 3.4V, CLK, LATCH, DATA, STB pin	Fig.1
Input low level current	I <sub>IL1</sub>	—	–0.01	–0.1	mA	V <sub>I</sub> = 0.4V, CLK, LATCH, DATA, STB pin	Fig.1
"H" level data output voltage	V <sub>DOH</sub>	2.8	3.0	—	V	I <sub>DOH</sub> = – 400μA	Fig.1
"L" level data output voltage	V <sub>DOL</sub>	—	0.3	0.4	V	I <sub>DOL</sub> = Δ1.6mA	Fig.1
Data output delay time	t <sub>DLH</sub>	—	0.6	1.0	μs	R <sub>LD</sub> = 10kΩ	—
Data output delay time	t <sub>DHL</sub>	—	0.6	2.0	μs	R <sub>LD</sub> = 10kΩ	—
Printing output delay time	t <sub>OLH</sub>	—	—	10	μs	R <sub>L</sub> = 560Ω, V <sub>O</sub> = 13.5V	—
Printing output delay time	t <sub>OHL</sub>	—	—	10	μs	R <sub>L</sub> = 560Ω, V <sub>O</sub> = 13.5V	—
Input high level current	I <sub>IH2</sub>	—	0.04	0.1	mA	V <sub>I</sub> = 3.4V, PSW pin	Fig.1
Input low level current	I <sub>IL2</sub>	—	0.1	10	μA	V <sub>I</sub> = 0.4V, PSW pin	Fig.1

● Measurement circuits

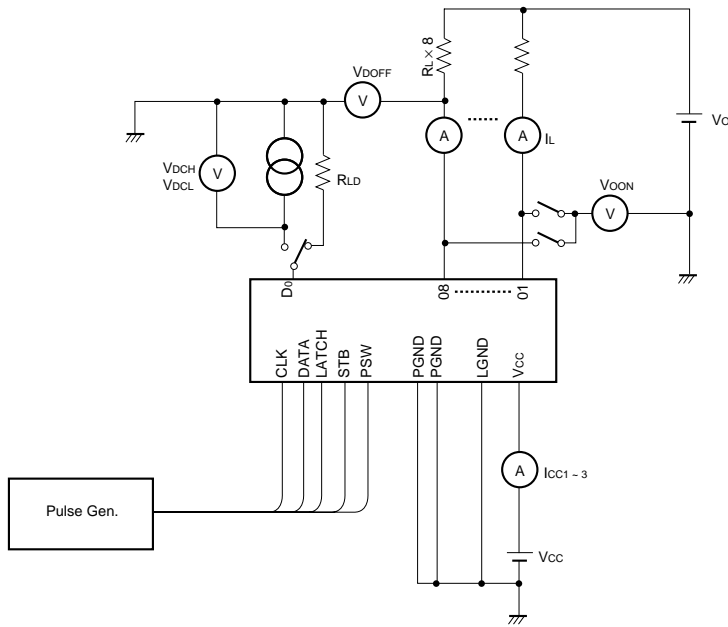


Fig.1

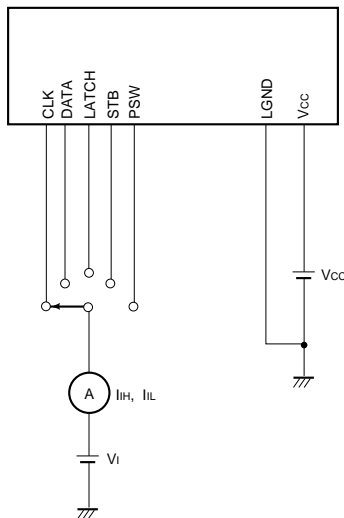
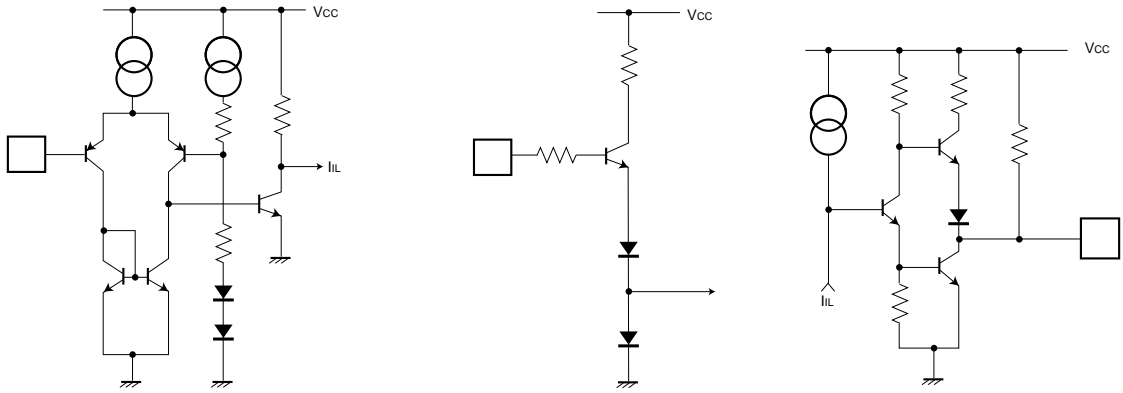


Fig.2

● Input / output circuits



(a) INPUT (CLK , DATA , LATCH , STB )

(b) INPUT (PSW)

(c) OUTPUT (Dout)

Fig.3

● Timing chart

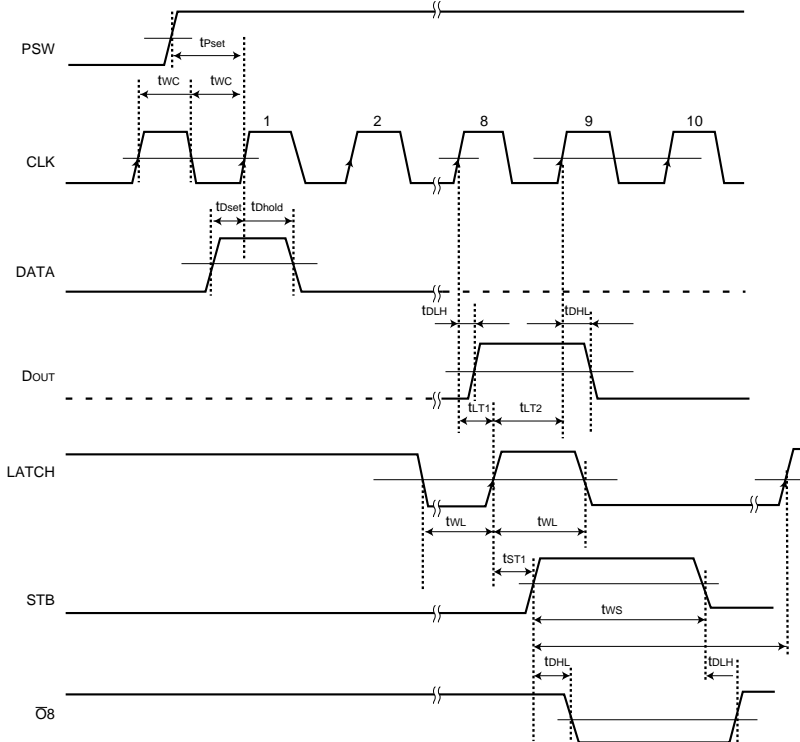


Fig.4

●Application example

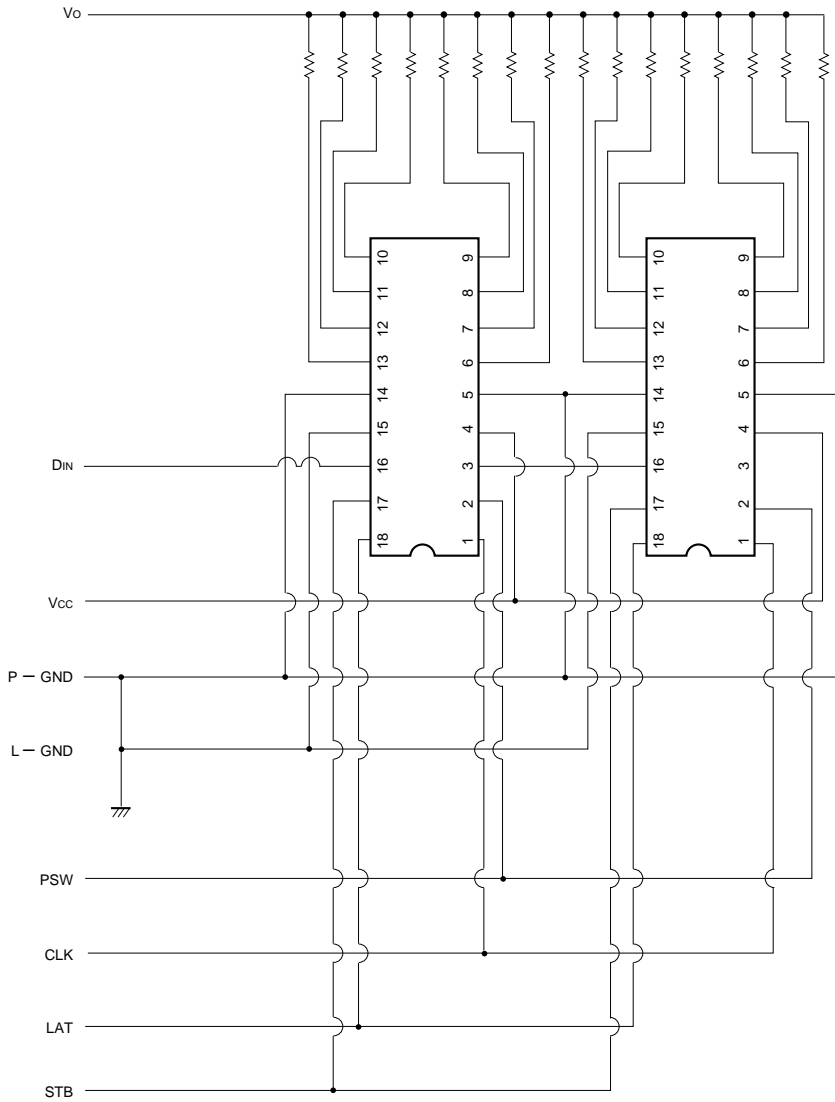


Fig.5

●Electrical characteristic curves

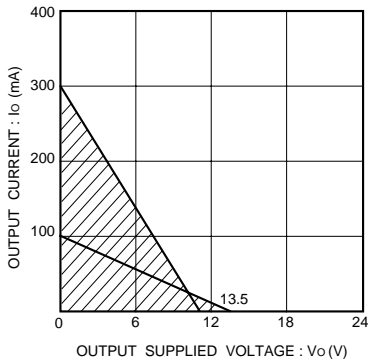


Fig.6 Output supplied voltage vs. output current and range of usability  
This product should be used within the range indicated by the shaded section above, even if the load includes reactance.

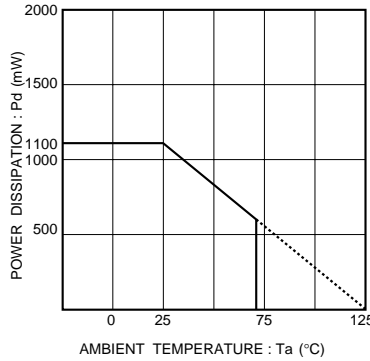


Fig.7 Ambient temperature vs. power dissipation

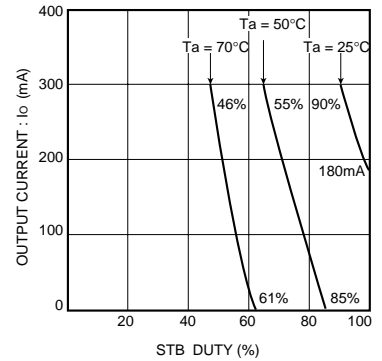


Fig.8 Output duty maximum output current (when all bits are on, duty cycle is 1Hz or higher)

●Circuit operation

The BA829 has the internal configuration shown in the logic diagram, with the following five input pins: clock (CLK), data (DATA), latch (LATCH), strobe (STB), and power switch (PSW).

Data input is synchronized to the clock, with data being read serially at the rising edge and latched at the rising edge of the shift register after it has shifted. The latched data appears at output terminals O<sub>1</sub> to O<sub>8</sub>, depending on the strobe input, with that pulse width

being the same as that of the strobe input.

The data output pin DOUT is used when ICs are connected in cascade format, and when the output for the last stage of the shift register appears, is connected to the next data input pin DATA.

When these clock and strobe latches and power switch are used in common, the output pins can be increased by eight bits each.

In stand-by mode, the power switch is set to "L".

●External dimensions (Units: mm)

