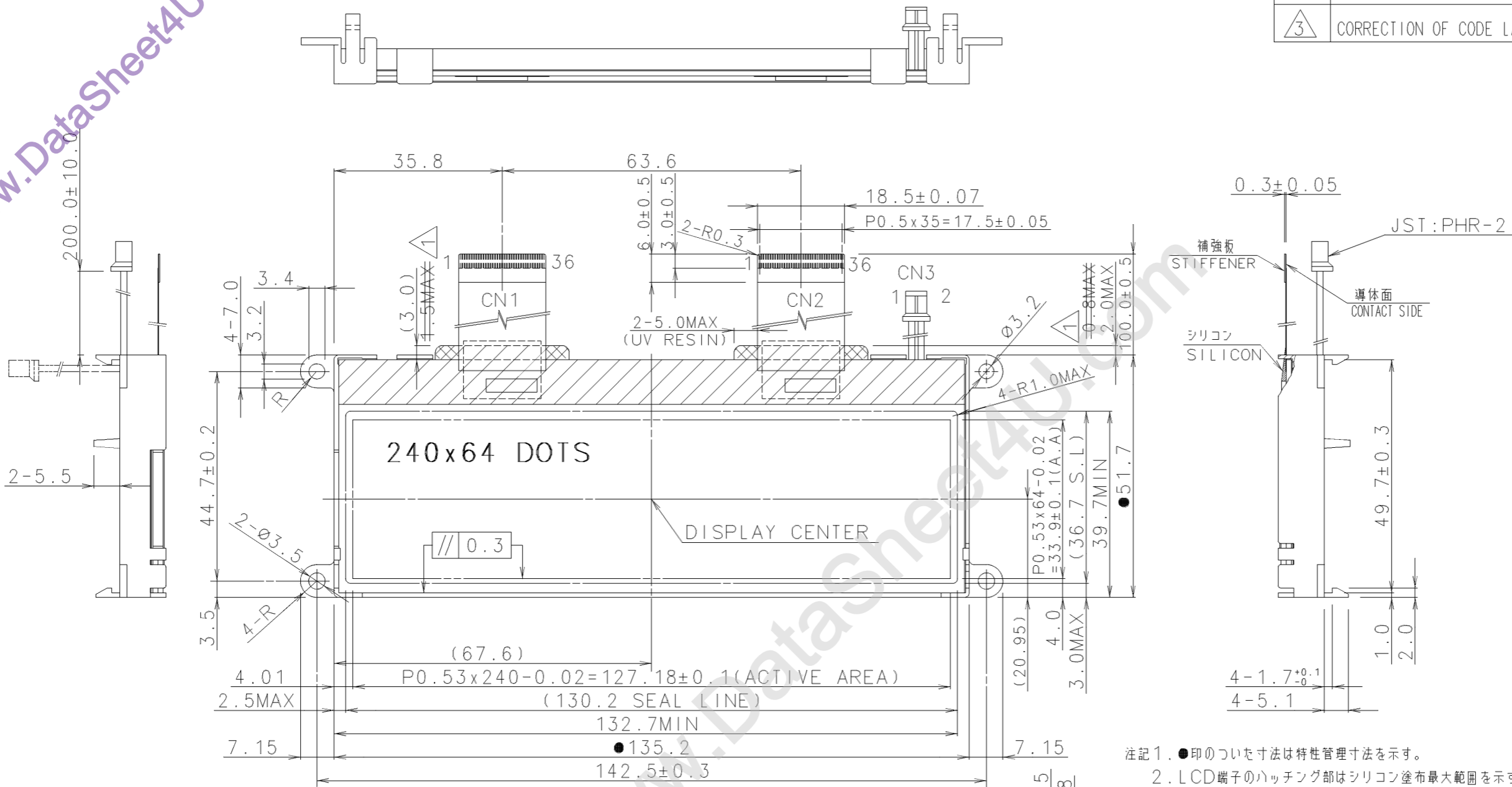


ISSUE	REVISIONS	DRAWN	APPROVED	DATE
①	CHANGE OF SILICON AREA.	M.Nakada	T.Okamoto	JAN.30'02
②	CHANGE OF LED CIRCUIT DIAGRAM.	M.Nakada	T.Okamoto	FEB.04'02
③	CORRECTION OF CODE LABEL.	M.Nakada	T.Okamoto	FEB.15'02

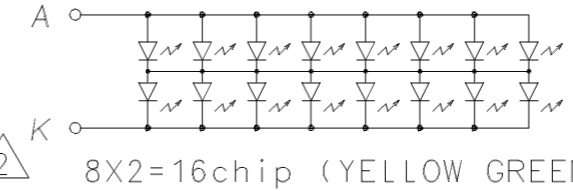


PIN ASSIGNMENT

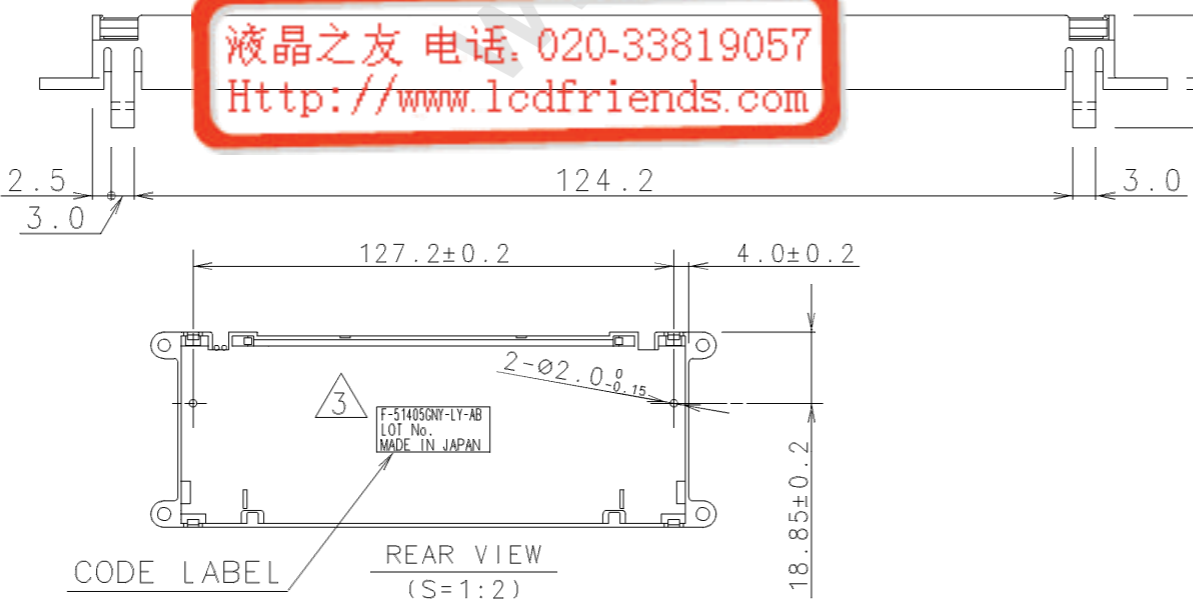
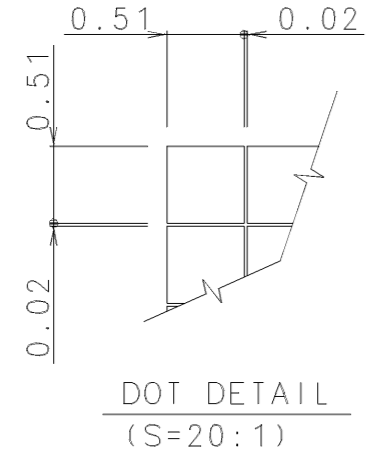
CN1-MASTER (IC1) CN2-SLAVE (IC2)			
No.	Symbol	No.	Symbol
1	NC	21	VOUT
2	FR	22	CAP3-
3	CL	23	CAP1+
4	DOF	24	CAP1-
5	CST	25	CAP2-
6	CS2	26	CAP2+
7	RES	27	V1
8	A0	28	V2
9	WR	29	V3
10	RD	30	V4
11	D0	31	V5
12	D1	32	VR
13	D2	33	C86
14	D3	34	P/S
15	D4	35	IRS
16	D5	36	NC
17	D6		
18	D7		
19	VDD		
20	VSS		

CN3	
No.	Symbol
1	ANODE
2	CATHODE

注記 1. ●印のついた寸法は特性管理寸法を示す。
 2. LCD端子のハッチング部はシリコン塗布最大範囲を示す。
 NOTE 1. ● MARK SETTING DIMENSIONS : SPECIAL CHARACTERISTICS.
 2. HATCHED AREA ON LCD TERMINAL EDGE SHOWS MAXIMUM AREA OF SILICON RESIN.



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MEASURE	TOLERANCE			THIRD ANGLE PROJECTION	DATE DEC.21'01
	A	B	C		
L≤16	±0.1	±0.3	±1	UNIT	APPROVED T.Okamoto
16<L≤63	±0.2	±0.5	±1.5	mm	CHECKED S.Kuwabara
63<L≤250	±0.3	±0.8	±2	SCALE	DRAWN M.Nakada
250<L≤500	±0.5	±1.2	±3	1:1	
500<L	±0.8	±2	±4		
ANGLE	±1°	±5°	±10°		

OPTREX CORPORATION
 DIMENSIONAL OUTLINE
 CODE F-51405GNY-LY-AB
 DWG NO UE-310700C