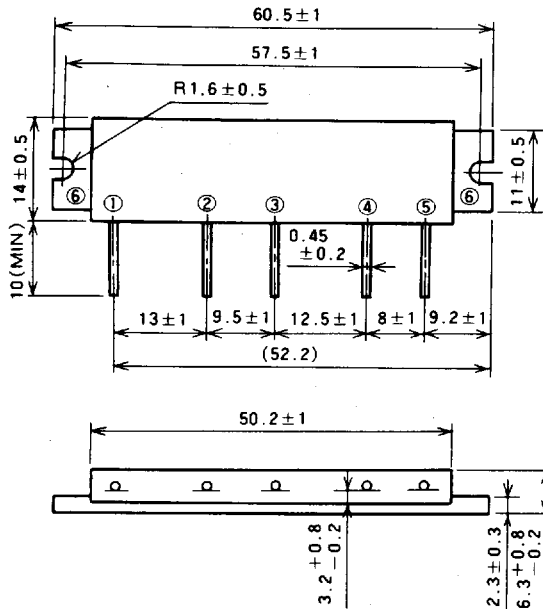
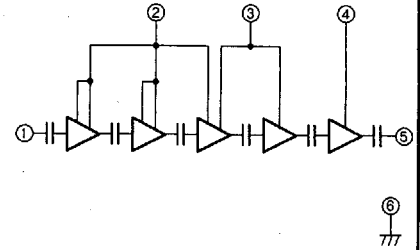


OUTLINE DRAWING

Dimensions in mm

**BLOCK DIAGRAM**

PIN :

- ①Pin : RF INPUT
- ②Vcc1 : 1st. DC SUPPLY
- ③Vcc2 : 2nd. DC SUPPLY
- ④Vcc3 : 3rd. DC SUPPLY
- ⑤Po : RF OUTPUT
- ⑥GND : FIN

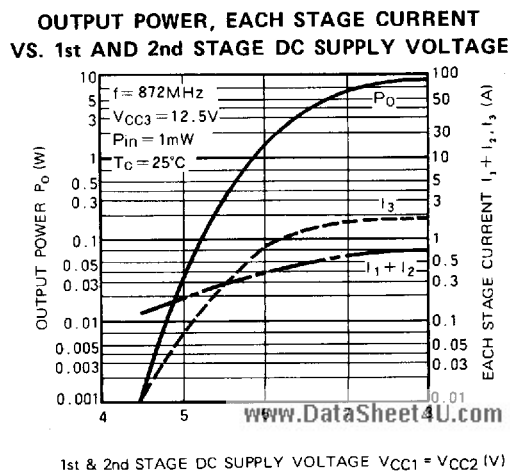
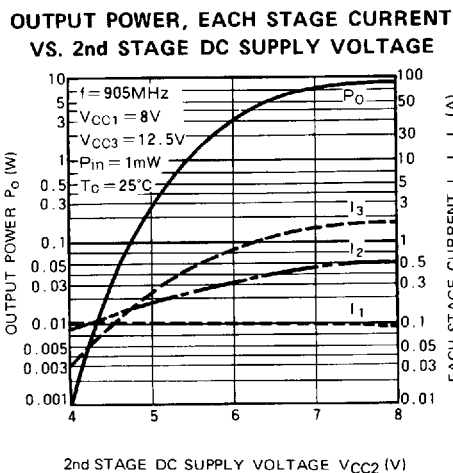
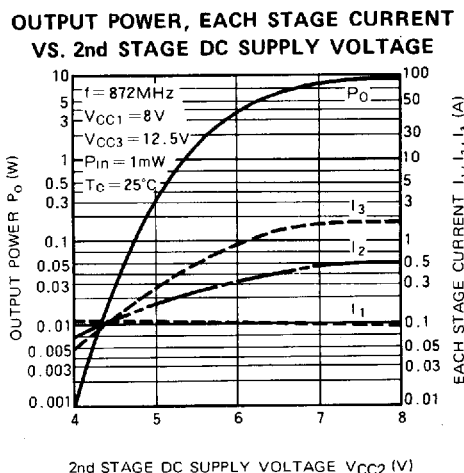
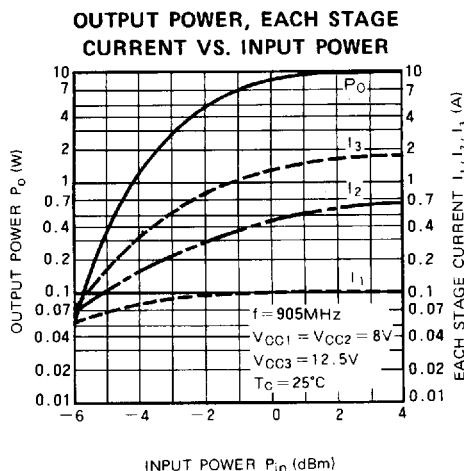
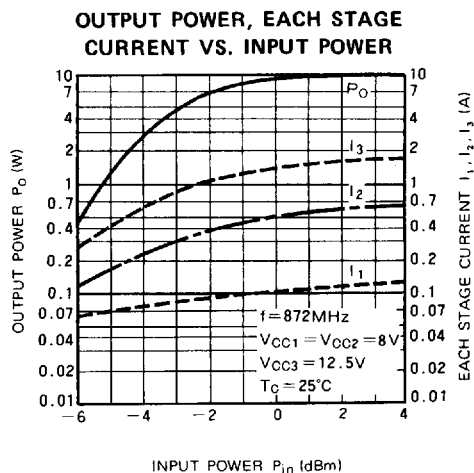
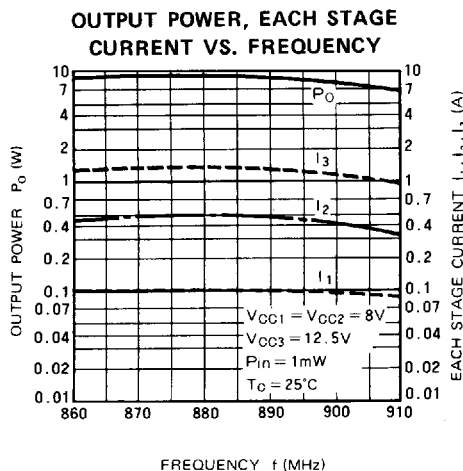
H11**ABSOLUTE MAXIMUM RATINGS** ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc1	Supply voltage		9	V
Vcc2			9	V
Vcc3			17	V
Icc	Total current	$Z_G = Z_L = 50 \Omega$	4	A
P _{in(max)}	Input power	$Z_G = Z_L = 50 \Omega$, $V_{cc1} \leq 12.5\text{V}$	7	mW
P _{O(max)}	Output power	$Z_G = Z_L = 50 \Omega$	10	W
T _{c(OP)}	Operation case temperature		-30~110	°C
T _{stg}	Storage temperature		-40~110	°C

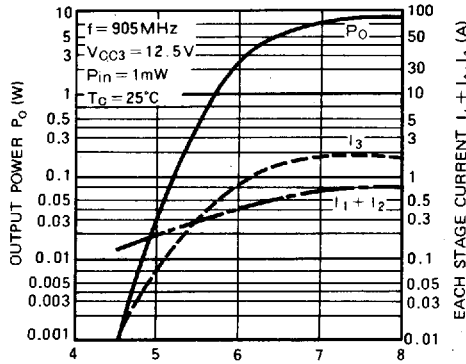
ELECTRICAL CHARACTERISTICS ($T_c = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test conditions	Limits		Unit
			Min	Max	
f	Frequency range	$V_{cc1} = V_{cc2} = 8\text{V}$, $V_{cc3} = 12.5\text{V}$ $P_{in} = 1\text{mW}$ $Z_G = Z_L = 50 \Omega$	872	905	MHz
P _o	Output power		7		W
η_T	Total efficiency		35		%
2f _o	2nd. harmonic			-30	dB
ρ_{in}	Input VSWR			2.8	—
—	Load VSWR tolerance	$V_{cc1} = V_{cc2} = 8\text{V}$, $V_{cc3} = 15.2\text{V}$ $P_o = 7\text{W}$ (P_{in} : controlled), $Z_G = 50 \Omega$ Load VSWR=20:1 (All phase), 5sec.	www.DataSheet4U.com No degradation		—

TYPICAL PERFORMANCE DATA



OUTPUT POWER, EACH STAGE CURRENT
VS. 1st AND 2nd STAGE DC SUPPLY VOLTAGE



1st & 2nd STAGE DC SUPPLY VOLTAGE $V_{CC1} = V_{CC2}$ (V)

Table 1: The conditions at standard operation

Stage	V_{CC} (V)	I_T (mA)	P_{in} (mW)	P_O (mW)
1st	8	45	1	20
2nd	8	80	20	200
3rd	8	160	200	500
4th	8	496	500	2000
5th	12.5	1100	2000	7000

DESIGN CONSIDERATION OF HEAT RADIATION

Please refer to the following consideration when designing a heat sink.

1. Junction temperature of incorporated transistors at standard operation.

(1) Thermal resistances between junction of incorporated transistors and case are shown in the followings.

- First stage transistor
 $R_{th(j-c)1} = 20^\circ\text{C/W}$ (Typ.)
- Second stage transistor
 $R_{th(j-c)2} = 17.5^\circ\text{C/W}$ (Typ.)
- Third stage transistor
 $R_{th(j-c)3} = 16^\circ\text{C/W}$ (Typ.)
- Fourth stage transistor
 $R_{th(j-c)4} = 9^\circ\text{C/W}$ (Typ.)
- Final stage transistor
 $R_{th(j-c)5} = 6.5^\circ\text{C/W}$ (Typ.)

(2) V_{CC} , I_T , RF input & output power conditions at standard operation for each stage transistors are estimated as follows.

$P_O = 7\text{W}$, $V_{CC1} = V_{CC2} = 8\text{V}$, $V_{CC3} = 12.5\text{V}$, $P_{in} = 1\text{mW}$, $\eta_T = 35\%$ (minimum ratings),

$I_{1+2} = 0.781\text{A}$ (Total current from 1st stage to 4th stage)

$I_3 = 1.1\text{A}$ (Current of 5th stage)

The conditions at standard operation for each stage transistors are shown in Table 1.

- Junction temperature of the first stage transistor
 $T_{j1} = (V_{CC1} \times I_{T1} - P_{O1} + P_{in}) \times R_{th(j-c)1} + T_C$ (Note 1)
 $= (8 \times 0.045 - 0.02 + 0.001) \times 20 + T_C$
 $= 6.8 + T_C$ ($^\circ\text{C}$)

Note 1: Case temperature of device

- Junction temperature of the second stage transistor
 $T_{j2} = (V_{CC1} \times I_{T2} - P_{O2} + P_{O1}) \times R_{th(j-c)2} + T_C$
 $= (8 \times 0.08 - 0.2 + 0.02) \times 17.5 + T_C$

$$= 8.1 + T_C$$

- Junction temperature of the third stage transistor
 $T_{j3} = (V_{CC2} \times I_{T3} - P_{O3} + P_{O2}) \times R_{th(j-c)3} + T_C$
 $= (8 \times 0.16 - 0.5 + 0.2) \times 16 + T_C$
 $= 15.7 + T_C$ ($^\circ\text{C}$)
- Junction temperature of the fourth stage transistor
 $T_{j4} = (V_{CC2} \times I_{T4} - P_{O4} + P_{O3}) \times R_{th(j-c)4} + T_C$
 $= (8 \times 0.496 - 2 + 0.5) \times 9 + T_C$
 $= 22.2 + T_C$ ($^\circ\text{C}$)
- Junction temperature of the final stage transistor
 $T_{j5} = (V_{CC3} \times I_{T5} - P_O + P_{O4}) \times R_{th(j-c)5} + T_C$
 $= (12.5 \times 1.1 - 7 + 2) \times 6.5 + T_C$
 $= 56.9 + T_C$ ($^\circ\text{C}$)

2. Heat sink design

In thermal design of heat sink, keep the case temperature below 90°C at output power $P_O = 7\text{W}$ and ambient temperature $= 60^\circ\text{C}$.

The thermal resistance $R_{th(c-a)}$ (Note 2) of the heat sink to realize this:

$$R_{th(c-a)} = \frac{T_C - T_a}{(P_O/\eta_T) - P_O + P_{in}} = \frac{90 - 60}{(7/0.35) - 7 + 0.001} = 2.31$$

$$(\text{C/W})$$

Note 2: Including the contact thermal resistance between device and heat sink

Mounting the device on the heat sink with above thermal resistance, junction temperatures of each transistor become;
 $T_{j1} = 97^\circ\text{C}$, $T_{j2} = 99^\circ\text{C}$, $T_{j3} = 106^\circ\text{C}$, $T_{j4} = 113^\circ\text{C}$,
 $T_{j5} = 147^\circ\text{C}$ at $T_a = 60^\circ\text{C}$, $T_C = 90^\circ\text{C}$.

Since the annual average of ambient temperature is 30°C , junction temperatures of each transistor become;

$$T_{j1} = 67^\circ\text{C}, T_{j2} = 69^\circ\text{C}, T_{j3} = 76^\circ\text{C}, T_{j4} = 76^\circ\text{C}, T_{j5} = 117^\circ\text{C}$$

As the maximum junction temperature of incorporated transistors T_{jmax} are 175°C , application under fully derated condition is ensured.