

### STE140NF20D

# N-channel 200 V, 0.010 Ω, 140 A, ISOTOP STripFET™ II with fast recovery diode Power MOSFET

Preliminary Data

#### **Features**

Туре	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STE140NF20D	200 V	< 0.012 Ω	140 A

- Exceptional dv/dt capability
- Low gate charge
- 100% avalanche tested

#### **Application**

Switching applications

#### **Description**

This Power MOSFET is produced using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. The STE140NF20D offers extremely fast switching performance thanks to the instrinsic fast body diode, making the device ideal for hard switching topologies.

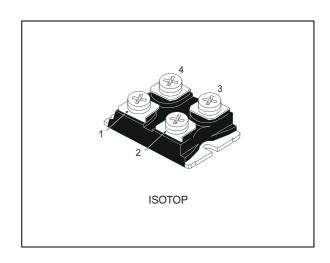


Figure 1. Internal schematic diagram

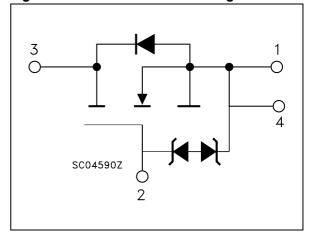


Table 1. Device summary

Order code	Marking	Package	Packaging
STE140NF20D	140NF20D	ISOTOP	Tube

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www.Data STE140NF20D Electrical ratings

### 1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source voltage (V <sub>GS</sub> = 0)	200	V
V <sub>GS</sub>	Gate-source voltage	± 20	V
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> = 25 °C	140	Α
I <sub>D</sub> <sup>(1)</sup>	Drain current (continuous) at T <sub>C</sub> =100 °C	260	Α
I <sub>DM</sub> <sup>(2)</sup>	Drain current (pulsed)	560	Α
P <sub>TOT</sub> (2)	Total dissipation at T <sub>C</sub> = 25 °C	500	W
	Derating factor	4	W/°C
dv/dt <sup>(3)</sup>	Peak diode recovery voltage slope	25	V/ns
T <sub>J</sub> T <sub>stg</sub>	Operating junction temperature Storage temperature - 55 to 15		°C

<sup>1.</sup> The value is rated according  $R_{thj-pcb}$ 

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
R <sub>thj-case</sub>	Thermal resistance junction-case	0.25	°C/W
R <sub>thj-amb</sub>	Thermal resistance junction-ambient	40	°C/W

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I <sub>AR</sub>	Avalanche current, repetitive or not repetitive (1)	TBD	Α
E <sub>AS</sub>	Single pulse avalanche energy (2)	TBD	mJ

<sup>1.</sup> Pulse width limited by Tjmax

<sup>2.</sup> Pulse width limited by safe operating area

<sup>3.</sup>  $I_{SD} \leq$  30 A, di/dt  $\leq$  TBD A/ $\mu$ s,  $V_{DD} \leq$  80%  $V_{(BR)DSS}$ 

<sup>2.</sup> Strating Tj = 25 °C,  $I_D = I_{AR}$ ,  $V_{DD} = 50 \text{ V}$ 

### 2 Electrical characteristics

 $(T_{CASE} = 25 \, ^{\circ}C \text{ unless otherwise specified})$ 

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 1 mA, V <sub>GS</sub> = 0	200			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = max rating, V <sub>DS</sub> =max rating @125 °C			10 100	μA μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±21 V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	2	3	4	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 70 A		0.010	0.012	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
9 <sub>fs</sub>	Forward transconductance	I <sub>D</sub> = 140 A, V <sub>DS</sub> = 150 V		TBD		
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25 \text{ V, f=1 MHz,}$ $V_{GS} = 0$		9900 2000 450		pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	$V_{DD}$ =480 V, $I_{D}$ = 140A $V_{GS}$ = 4.5 V (see Figure 3)		390 TBD TBD		nC nC nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub> t <sub>r</sub> t <sub>d(off)</sub> t <sub>f</sub>	Turn-on delay time Rise time Turn-off delay time Fall time	$V_{DD}$ = 100 V, $I_D$ = 70 A, $R_G$ =4.7 $\Omega$ , $V_{GS}$ =10 V (see Figure 2)		TBD TBD TBD TBD		ns ns ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Тур.	Max	Unit
I <sub>SD</sub>	Source-drain current				140	Α
I <sub>SDM</sub> <sup>(1)</sup>	Source-drain current (pulsed)				560	Α
V <sub>SD</sub> <sup>(2)</sup>	Forward on voltage	I <sub>SD</sub> = 70 A, V <sub>GS</sub> =0			1.6	V
t <sub>rr</sub>	Reverse recovery time	$I_{SD} = 70 \text{ A},$		TBD		ns
$Q_{rr}$	Reverse recovery charge	di/dt = 100 A/μs,		TBD		nC
I <sub>RRM</sub>	Reverse recovery current	V <sub>DD</sub> = 100 V, Tj=150 °C		TBD		Α

<sup>1.</sup> Pulse width limited by safe operating area

<sup>2.</sup> Pulsed: pulse duration=300µs, duty cycle 1.5%

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#### 3 Test circuit

Figure 2. Switching times test circuit for resistive load

Figure 3. Gate charge test circuit

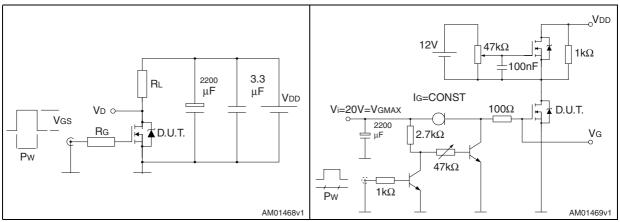


Figure 4. Test circuit for inductive load switching and diode recovery times

Figure 5. Unclamped inductive load test circuit

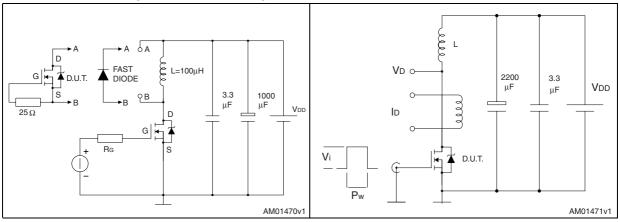
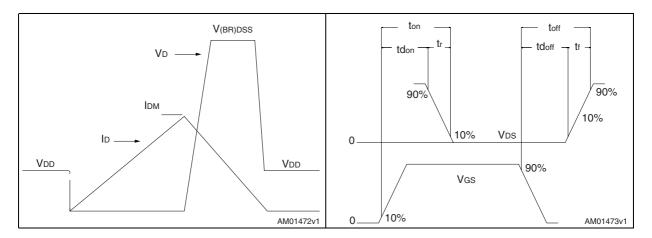


Figure 6. Unclamped inductive waveform

Figure 7. Switching time waveform



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### 4 Package mechanical data

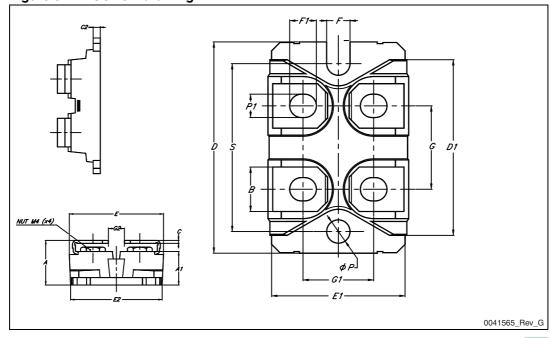
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Table 9. ISOTOP mechanical data

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Dim.		mm	
Dilli.	Min.	Тур.	Max.
А	11.80		12.20
A1	8.90		9.10
В	7.80		8.20
С	0.75		0.85
C2	1.95		2.05
D	37.80		38.20
D1	31.50		31.70
E	25.15		25.50
E1	23.85		24.15
E2		24.80	
G	14.90		15.10
G1	12.60		12.80
G2	3.50		4.30
F	4.10		4.30
F1	4.60		5
фР	4		4.30
P1	4		4.40
S	30.10		30.30

Figure 8. ISOTOP drawing



www.Data STE140NF20D Revision history

## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
27-Jan-2009	1	First release

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