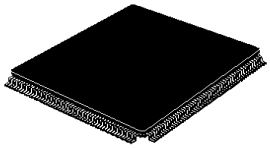
STE400P

10/100 FAST ETHERNET 4 PORT TRANSCEIVER

1 GENERAL DESCRIPTION

The STE400P, also referred to as STEPHY4, is a high performance Fast Ethernet physical layer interface for 10BASE-T and 100BASE-TX applications.
It was designed with advanced CMOS technology to provide a Media Independent Interface (MII) for easy attachment to 10/100 Media Access Controllers (MAC) and a physical media interface for 100BASE-TX of IEEE802.3u and 10BASE-T of IEEE802.3.
The STE400P supports both half-duplex and full-duplex operation, at 10 and 100 Mbps operation. Its operating mode can be set using auto-negotiation, parallel detection or manual control. It also allows for the support of auto-negotiation functions for speed and duplex detection.



PQFP208

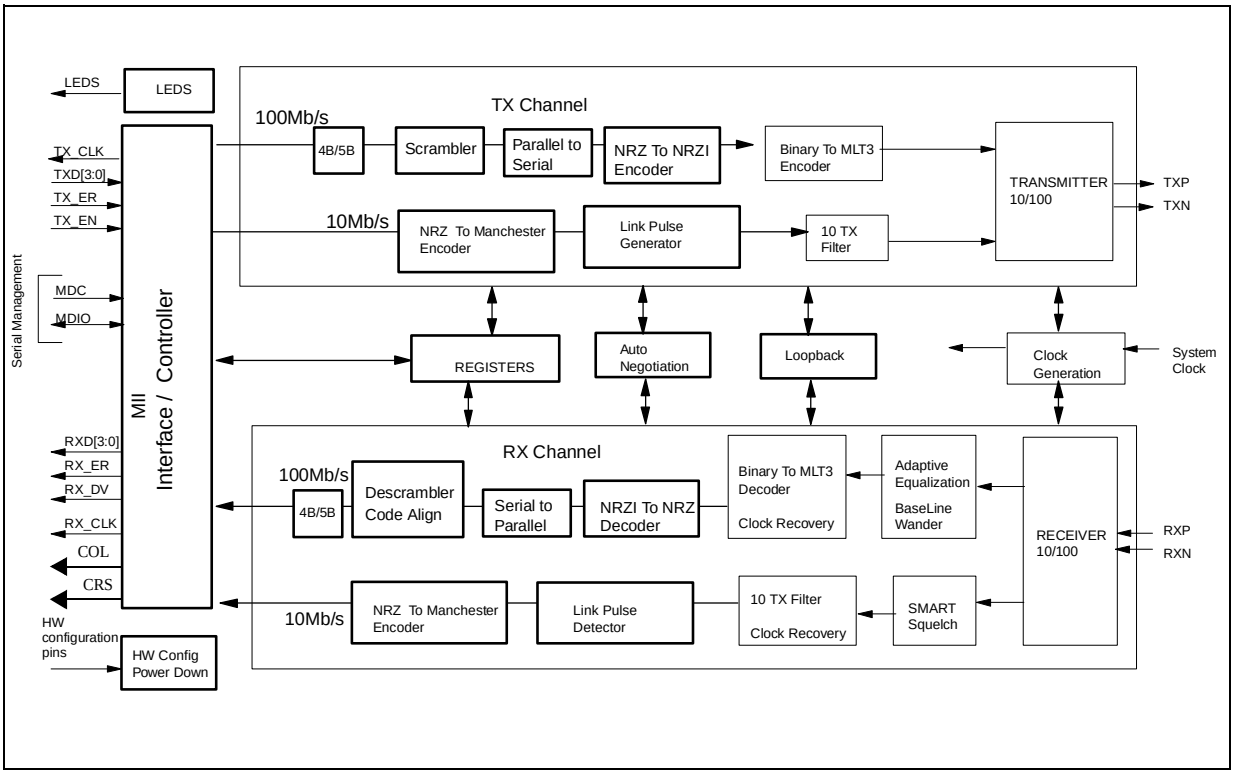
ORDERING NUMBER: STE400P

2 FEATURES

2.1 INDUSTRY STANDARD

- IEEE802.3u 100BASE-TX and IEEE802.3 10BASE-T compliant
- Support for IEEE802.3x flow control
- IEEE802.3u Auto-Negotiation support for 10BASE-T and 100BASE-TX
- MII interface
- Standard CSMA/CD or full duplex supported

Figure 1. BLOCK DIAGRAM FOR 1 PORT



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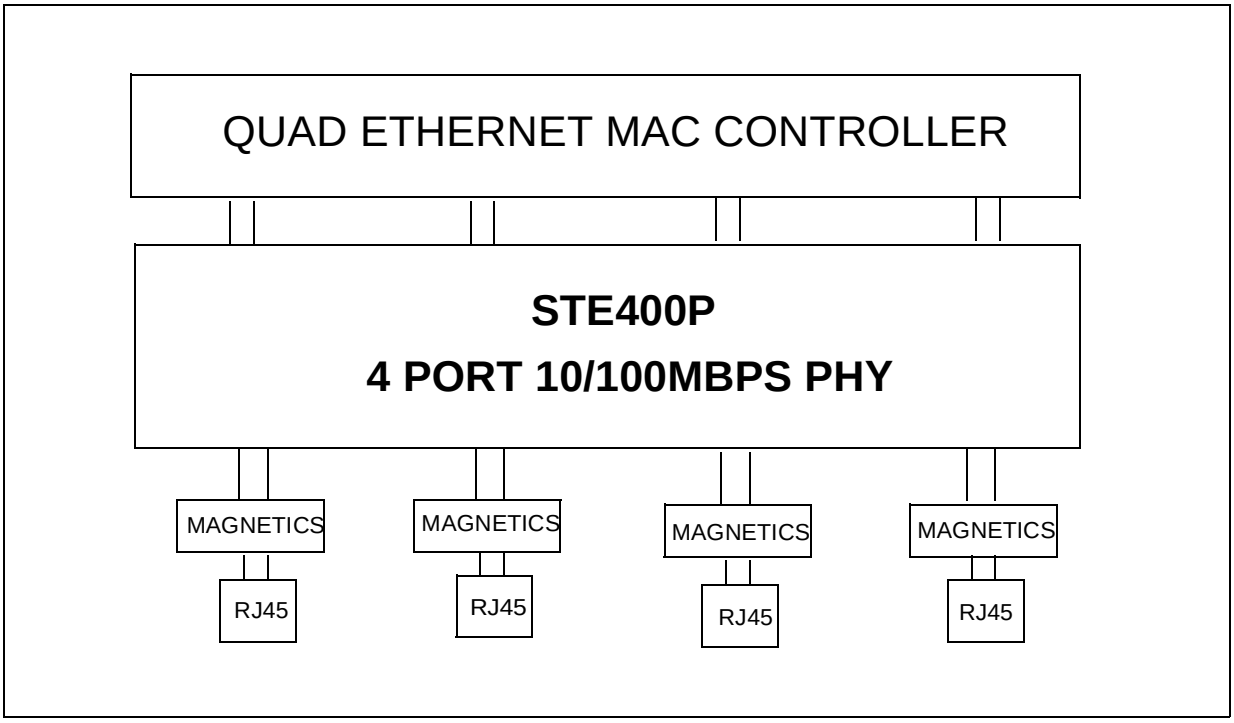
2.2 PHYSICAL LAYER

- Integrates the whole Physical layer functions of 100BASE-TX and 10BASE-T
- Provides Full-duplex operation on both 100Mbps and 10Mbps modes
- Provides Auto-negotiation(NWAY) function of full/half duplex operation for both 10 and 100 Mbps
- Provides MLT-3 transceiver with DC restoration for Base-line wander compensation
- Provides transmit wave-shaper, receive filters, and adaptive equalizer
- Provides loop-back modes for diagnostic
- Builds in Stream Cipher Scrambler/ De-scrambler and 4B/5B encoder/decoder
- Supports external transmit transformer with turn ratio 1.41:1
- Supports external receive transformer with turn ratio 1:1

2.3 LED DISPLAY

- Provides 2 kinds of LED display mode:
- First mode - 3 LED displays for 100Mbps(on) or 10Mbps(off)
- Link(Keeps on when link ok) or Activity(Blink with 10Hz when receiving or transmitting but not collision)
- FD(Keeps on when in Full duplex mode) or Collision(Blink with 20Hz when colliding)
- Second mode – 4 LED displays for 100 Link(On when 100M link or 10 Link(On when 10M link ok
- Activity (Blink with 10Hz when receiving or transmitting)
- FD(Keeps on when in Full duplex mode) or Collision(Blink with 20Hz when colliding)

3 SYSTEM DIAGRAM OF THE STE400P APPLICATION



4 PIN ASSIGNMENT DIAGRAM

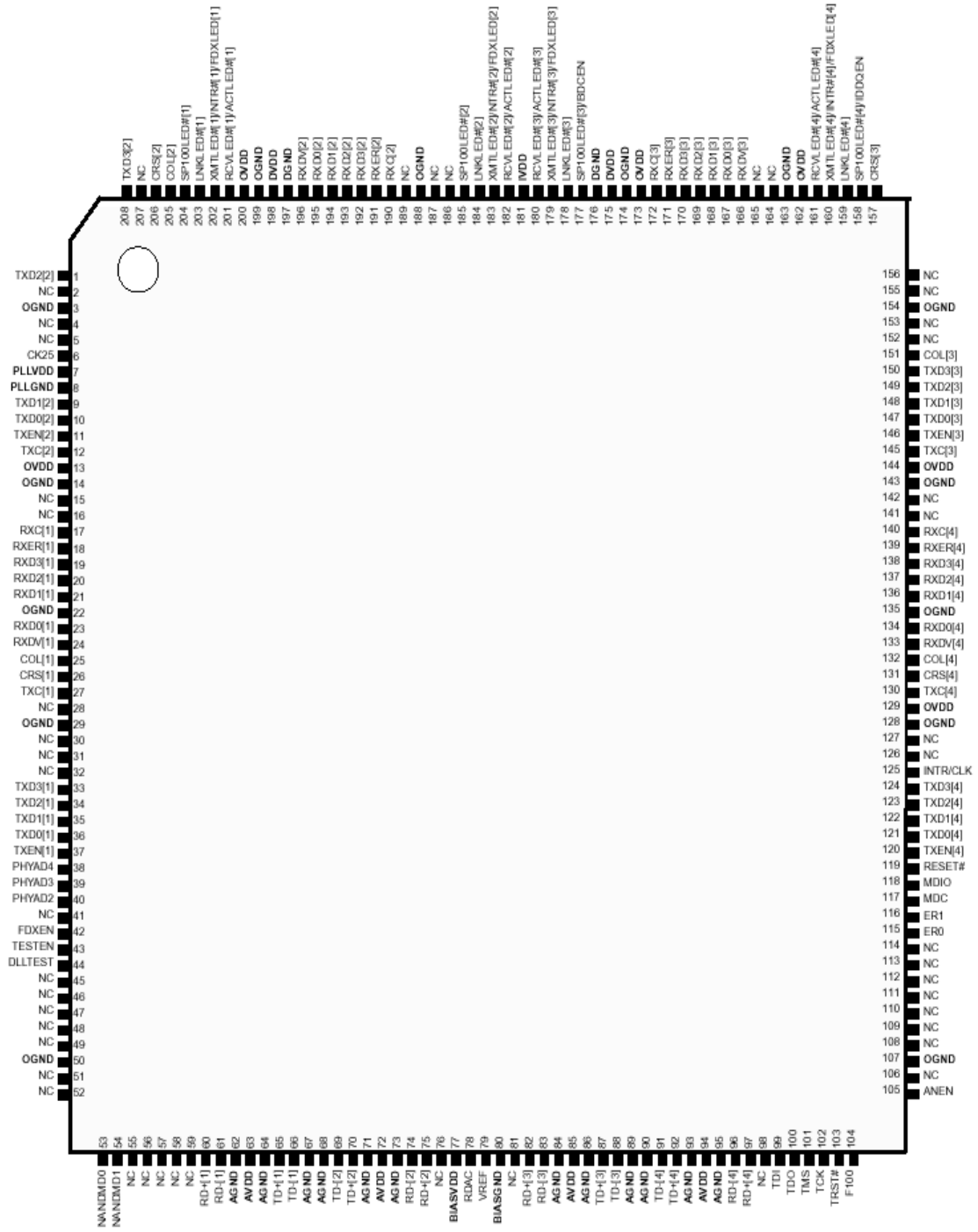


Table 1. Pin Description

Pin.	Name	Type	Description
MII Interface			
33 34 35 36 208 1 9 10 150 149 148 147 124 123 122 121	TXD3 {1} TXD2 {1} TXD1 {1} TXD0 {1} TXD3 {2} TXD2 {2} TXD1 {2} TXD0 {2} TXD3 {3} TXD2 {3} TXD1 {3} TXD0 {3} TXD3 {4} TXD2 {4} TXD1 {4} TXD0 {4}	Ipd	Transmit Data. The Media Access Controller (MAC) drives data to the STE400P using these inputs. These signals must be synchronized to the TX-CLK.
37 11 146 120	TXEN1 TXEN2 TXEN3 TXEN4	Ipd	Transmit Enable. The MAC asserts this signal when it drives valid data on the TXD inputs. This signal must be synchronized to the TX-CLK.
27 12 145 130	TXC1 TXC2 TXC3 TXC4	O3s	**Transmit Clock**. Normally the STE400P drives TX-CLK. Refer to the Clock Requirements discussion in the Functional Description section. 25 MHz for 100 Mbps operation. 2.5 MHz for 10 Mbps operation.
19 20 21 23 192 193 194 195 170 169 168 167 138 137 136 134	RXD3 {1} RXD2 {1} RXD1 {1} RXD0 {1} RXD3 {2} RXD2 {2} RXD1 {2} RXD0 {2} RXD3 {3} RXD2 {3} RXD1 {3} RXD0 {3} RXD3 {4} RXD2 {4} RXD1 {4} RXD0 {4}	O3s	**Receive Data**. The STE400P drives received data on these outputs, synchronous to RX-CLK. RXD4 is driven only in Symbol (5B) Mode.
24 196 166 133	RXDV1 RXDV2 RXDV3 RXDV4	O3s	**Receive Data Valid.** The STE400P asserts This signal when it drives valid data on RXD. This output is synchronous to RX-CLK.
18 191 171 139	RXER1 RXER2 RXER3 RXER4	O3s	**Receive Error.** The STE400P asserts this output when it receives invalid symbols from the network. This signal is synchronous to RX-CLK. In Symbol (5B) Mode this pin is also equivalent to RXD4.

Table 1. Pin Description

Pin.	Name	Type	Description
17 190 172 140	RXC1 RXC2 RXC3 RXC4	O3s	**Receive Clock.** This continuous clock provides reference for RXD. RXDV, and RXER signals. Refer to the Clock Requirements discussion in the Functional Description section. 25 MHz for 100 Mbps operation. 2.5 MHz for 10 Mbps operation.
25 205 151 132	COL1 COL2 COL3 COL4	I/O pd	**Collision Detected**. The STE400P asserts this output when detecting a collision. This output remains High for the duration of the collision. This signal is asynchronous and inactive during full-duplex operation.
26 206 157 131	CRS1 CRS2 CRS3 CRS4	O3s	**Carrier Sense**. During half-duplex operation (PR0:8=0), the STE400P asserts this output when either transmit or receive medium is non idle. During full duplex operation (PR0:8=1), CRS is asserted only when the receive medium is non-idle.
117	MDC	Ipd	**Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 2.5 MHz.
118	MDIO	I/O	**Management Data Input/Output**, Bi-directional serial data channel for PHY communication.
119	RESET#	Ipu	**Reset:** Active low. Resets the STE400P. Pin not included in NAND
Clock			
6	CLK25	I	**Reference clock input.** - **25 MHz** This pin must be driven with a continuous 25 MHz clock.
Media Connections			
65 66 70 69 87 88 92 91	TD+ {1} TD- {1} TD+ {2} TD- {2} TD+ {3} TD- {3} TD+ {4} TD- {4}	Oa	**Transmit Pair:** Differential data is transmitted to the media on the TD+- signal pair
60 61 75 74 82 83 97 96	RD+ {1} RD- {1} RD+ {2} RD- {2} RD+ {3} RD- {3} RD+ {4} RD- {4}	Ia	**Receive Pair:** Differential data from the media is received on the RD+- signal pair
LED			
203 184 178 159	LNKLED# {1} LNKLED# {2} Ser SFRM# LNKLED# {3} LC_SER_LED_EN LNKLED# {4} SER_LED_EN#	O	Link Integrity LED: Active low. This output signal indicates the link status of the PHY. LNKLED is driven low when the link to the PHY is good. Serial LED mode is enabled by “pull-down” of pin 159 during reset. WHen the Serial LED mode is enabled, pin 184 becomes the Serial LED mode frame signal. Low cost serial LED mode is enabled by “pull down” of pin 198 during reset..

Table 1. Pin Description

Pin.	Name	Type	Description
204 185 177 158	SP100LED# {1} SP100LED# {2} SP100LED# {3} SP100LED# {4}	O	Speed 100 LED: Driven low when operating in 100BASE-X modes and high when operating in 10BASE-T modes
202	XMTLED#{1} INTR# {1} FDXLED# {1}	Ood	Transmit Activity LED: Active low output. The transmit activity LED is driven low for approximately 80ms each time there is transmit activity while in the link pass state. When INTR mode is enable, the pin becomes an interrupt output. When FDX LED mode is enabled, the pin becomes FDXLED output. When the Serial LED mode is enabled, pin 183 becomes the Serial LED mode data output signal.
183	XMTLED#{2} INTR# {2} FDXLED# {2} Ser SDO#		
179	XMTLED#{3} INTR# {3} FDXLED# {3}		
160	XMTLED#{4} INTR# {4} FDXLED# {4}		
201	RCVLED#{1} ACTLED {1} LC Ser SCLK#	Ood	Receive Activity LED: Active low output. The receive activity LED is driven low for approximately 80ms each time there is receive activity while in the link pass state. When in either INTR or FDXLED modes, this pin becomes ACTLED output for either receive or transmit activity. When the Serial LED mode is enabled, pin 182 becomes the Serial LED mode clock signal. When the low cost serial LED mode is enabled, pin 201 becomes Low cost serial LED mode clock signal and pin 180 becomes the data output signal.
182	RCVLED# {2} ACTLED# {2} Ser SCLK# {2}		
180	RCVLED# {3} ACTLED# {3} LC Ser SDO#		
161	RCVLED# {4} ACTLED# {4}		
MODE			
42	FDXEN	Ipd	Full-Duplex Enable. When A/N is enabled, FDE determines full-duplex advertisement capability in combination with CFG0 and CFG1. (See Table 2) When A/N is disabled, FDE directly affects full-duplex operation and determines the value of PR0 bit 8 (Full/Half Duplex Mode Select).
38 39 40	PHYAD4 PHYAD3 PHYAD2	Ipd	PHY Address Selects: These inputs set the three MSB's for the MII management PHY addresses. THe two LSB's, PHYAD1, PHYAD0 are internally wired to each of the four ports: PHYAD[00] = Port1,.., PHYAD[11] = Port4.
104	F100	Ipu	Force 100BASE-X Operation: When F100 is high and ANEN is low, all transceivers will be forced to 100BASE-X operation. When F100 is low and ANEN is low, all transceivers are forced to 10BASE-T operation. When ANEN is high, F100 has no effect on operation
105	ANEN	Ipu	Auto Negotiation Enable: When pulled high, Auto-Negotiation begins immediately after reset. When low, it is disabled after reset.

Table 1. Pin Description

Pin.	Name	Type	Description
116 115	ER1 ER0	Ipu	Transmit DAC Edge Rate Control: These pins control the slew rate of each of the transmit DAC's.
43	TESTEN	Ipd	Test Enable: Active-high test control inputs used along with NANDMD1, 0 and PHYAD[4:2] to select the NAND-chain test mode. Both inputs must be driven high during latching of test mode. Must be pulled low or left unconnected during normal operation.
54 53	NANDMD1 NANDMD0	Ipd	NAND Mode: Active-high test control inputs used along with TESTEN and PHYAD[4:2} to select the NAND-chain test mode. Both inputs must be driven high during latching of the test mode. Must be kept at low or left unconnected during normal operation.
125	INTR/clk_20lbk	I/Opd	Bidirectional pad : input - clk_20lbk used to bypass internal 20 MHz PLL, output - intr as per interrupt register.
BIAS			
78	RDAC	B	DAC Bias Resistor: A 5K ohm + - 1% resistor must be connected between this pin and AGND for normal operation.
79	VREF	B	Voltage Reference: Low-impedance bias pin driven by the internal bandgap voltage reference. This pin must be left unconnected during normal operation.
JTAG			
99	TDI	Ipu	Test Data Input: Serial data input to the JTAG TAP controller. Sampled on the rising edge of TCK. If unused, may be left unconnected
100	TDO	O3s	Test Data Output: Serial data output from the JTAG TAP controller. Updated on the falling edge of TCK. Actively driven both high and low when enabled.
101	TMS	Ipu	Test Mode Select: Single control input to the JTAG TAP Controller used to traverse the test-logic state machine. Sampled on the rising edge of TCK. If unused, may be left unconnected
102	TCK	Ipu	Test Clock: Clock input used to synchronize JTAG control and data transfers. If unused, may be left unconnected
103	TRST#	Ipu	Test Reset: Asynchronous active-low reset input to the JTAG TAP controller. Must be held low during power up to insure the TAP controller initializes to the test-logic-reset state. May be pulled low continuously when JTAG functions are not used
44	DLLTEST	Ipu	DLL Bypass Test Enable: This pin is for factory test only and must be connected to DVDD or left floating
Power			
181	IVDD		Input VDD: +5.0V or +3.3V. If any of the inputs are driven to 5.0V, this pin must be connected to the 5.0V supply. If none of the inputs are driven above 3.3V, this pin may be connected to the 3.3V supply
7	PLLVDD		Phase Locked Loop VDD
8	PLLGND		Phase Locked Loop GND
77	BIASVDD		Bias VDD

Table 1. Pin Description

Pin.	Name	Type	Description
80	BIASGND		Bias GND
63 72 85 94	AVDD		Analog VDD
62, 64 67 68 71 73 84 86 89 90 93 95	AGND		Analog GND
175 198	DVDD		Digital Core VDD
176 197	DGND		Digital Core GND
13 129 144 162 173 200	OVDD		Digital Periphery (Output Buffer) VDD
3 14 22 29 50 107 128 135 143 154 163 174 188 199	OGND		Digital Periphery (Output Buffer) GND
Note: #=active low, I=digital input, O=digital output, I/O=bidirectional, Ia=analog input, Oa=analog output, Ipu=digital input w/ internal pull-up, Ipd=digital input w/ internal pull-down, Ood=open-drain input, O3s=three-state output, I/Opd=bidirectional w/ internal pull-down, B=bias.			

5 OPERATIONAL DESCRIPTION

5.1 RESETTING THE STE400P

There are two ways to reset each transceiver in the STE400P. A hardware reset pin has been provided which resets all internal nodes inside the chip to a known state. The reset pulse must be asserted for at least 400 ns. Hardware reset should always be applied to a STE400P after power-up.

Each transceiver also has an individual software reset capability. To perform software reset, a “1’ must be written to bit 15 of the transceiver’s MII Control Register. This bit is self-clearing, i.e. that a second write operation is not necessary to end the reset. There is no effect if a “0” is written to the MII Control Register reset bit.

5.2 ISOLATE MODE

Each transceiver in the STE400P may be isolated from the MII. When a transceiver is put into isolate mode, all MII inputs are ignored, and all MII outputs are set at high impedance. Only the MII management pins operate normally. Upon resetting the chip, the isolate mode is off. Writing a “1” to bit 10 of the MII Control Register puts the transceiver into isolate mode. Writing a “0” to the same bit removes it from isolate mode.

5.3 LOOPBACK MODE

The loopback mode allows in-circuit testing of the STE400P chip. All packets sent in through the TXD pins are looped-back internally to the RXD pins, and are not sent out to the cable. Incoming packets on the cable are ignored. Because of this, the COL pin will normally not be activated during loopback mode. In order to test that the COL pin is actually working, the STE400P may be placed into collision test mode. This mode is enabled by writing a “1” to bit 7 of the MII Control Register. Asserting TXEN will cause the COL output to go high and deasserting TXEn will cause the COL output to go low.

The loopback mode may be entered by writing a “1” to bit 14 of the MII Control Register. In order to resume normal operation, bit 14 of the MII Control Register must be “0”.

Several function bypass modes are also supported which can provide a number of different combinations of feedback paths during loopback testing. These bypass modes include: bypass scrambler, bypass MLT3 encoder and bypass 4B5B encoder.

5.4 FULL DUPLEX MODE

The STE400P supports full duplex operation. While in full-duplex mode, a transceiver may simultaneously transmit and receive packets on the cable. The COL signal is never activated while in full-duplex mode. By default, each transceiver in the STE400P powers up in half-duplex mode.

When Auto Negotiation is disabled, full duplex operation can be enabled either by a pin (FDXEN) or by an MII register bit (Register “0” bit 8). When Auto Negotiation is enabled in DTE mode, full-duplex capability is advertised by default but can be overridden by a write to the Auto-Negotiation Advertisement Register (04h).

5.5 100BASE-T MODE

The same magnetics module is used to interface the twisted-pair cable in 10BASE-T mode and in 100BASE-TX mode. The data will be two-level Manchester coded instead of three level MLT3 and no scrambling/descrambling or 4B5B coding is performed. Data and clock rates are decreased by a factor of 10, with the NII interface operating at 2.5 MHz.

Each transceiver in the STE400P will have a unique PHY address for MII management. THe addresses will be set through the PHY address pins. The pins are latched at the trailing end of reset. Transceiver 1 will have the address AAA00 where AAA=PHYAD4, PHYAD3, PHYAD2. Transceivers 2 - 4 will have addresses AAA01, AAA10 and AAA11, respectively.

6 REGISTERS AND DESCRIPTORS DESCRIPTION

There are 20 registers with 16 bits each supported for each port of the STE400P. This includes 9 basic registers which are defined according to the clause 22 “Reconciliation Sub-layer and Media Independent Interface” and clause 28 “Physical Layer link signaling for 10 Mb/s and 100 Mb/s Auto-Negotiation on twisted pair” of IEEE802.3u standard. In addition, there are 11 registers for advanced chip control and status information.

6.1 MII MANAGEMENT INTERFACE

The STE400P is fully compliant with the IEEE 802.3u MII specifications.

6.2 REGISTER LIST

Table 2. Register List

Address	Reg. Index	Name	Register Descriptions
00h	PR0	Control	MII Control Register
01h	PR1	Status	MII Status Register
02h	PR2	PID HI	PHY Identifier (HI) Register
03h	PR3	PID LO	PHY Identifier (LO) Register
04h	PR4	ANA	Auto-Negotiation Advertisement Register
05h	PR5	ANLPA	Auto-Negotiation Link Partner Ability Register
06h	RP6	ANE	Auto-Negotiation Expansion Register
07h	PR7	NEXT PAGE	Auto-Negotiation Next Page Transmit Register
08h	PR8	LP NXT PG	Auto-Negotiation Link Partner Next Page Transmit Register
10h	PR9	100AUXCTL	100BaseX Auxiliary Control Register
11h	PR10	100AUX SR	100BaseX Auxiliary Status Register
12h	PR11	100 RX EC	100BaseX Receiver Error Counter
13h	PR12	100 FCSC	100BaseX False Carrier Sense Counter
18h	PR13	AUX CSR	Auxiliary Control/Status Register
19h	PR14	AUX SSR	AuxiliaryStatus Summary Register
1Ah	PR15	INT	Interrupt Register
1Bh	PR16	AUX M2	Auxiliary Mode 2 Register
1Ch	PR17	AUX EGSR	Auxiliary Error and General Status Register
1Dh	PR18	AUX MODE	Auxiliary Mode Register
1Eh	PR19	AUX MPR	Auxiliary Multiple PHY Register

6.3 REGISTER DESCRIPTIONS

Table 3. Register Descriptions

Bit #	Name	Descriptions	Default Val	RW Type
PR0, MII Control Register. The default values on power-up/reset are as listed below.				
15	XRST	Reset control. 1: Device will be reset. This bit will be cleared by STE400P itself after the reset is completed.	0	R/W
14	XLBEN	Loop-back mode select. 1: Loop-back mode is selected.	0	R/W
13	SPSEL	Network Speed select. This bit's selection will be ignored if Auto-Negotiation is enabled(bit 12 of PR0 = 1). 1:100Mbps is selected. 0:10Mbps is selected.	0	R/W
12	ANEN	Auto-Negotiation ability control. 1: Auto-Negotiation function is enabled. 0: Auto-Negotiation is disabled.	1	R/W
11	PDEN	Power-down mode control. 1: Power-down mode is selected. Setting this bit puts the STE400P into power-down mode. During the power-down mode, TXP/TXN and all LED outputs are 3-stated, and the MII interface is isolated.	0	R/W
10	ISOEN	0 – Normal operation. 1 – Isolate PHY from MII. Setting this control bit isolates the STE400P from the MII, with the exception of the serial management inter-face. When this bit is asserted, the STE400Pdoes not respond to TXD[3:0], TX-EN, and TX-ER inputs, and it presents a high impedance on its TX-CLK, RX-CLK, RX-DV, RX-ER, D[3:0], COL, and CRS outputs. This bit is initialized to 0 unless the configuration pins for the PHY address are set to 00000h during power-up or reset.	0	R/W
9	RSAN	Re-Start Auto-Negotiation process control. 1: Auto-Negotiation process will be re-started. This bit will be cleared by STE400P itself after the Auto-negotiation restarted.	0	R/W
8	DPSEL	Full/Half duplex mode select. 1: full duplex mode is selected. This bit will be ignored if Auto-Negotiation is enabled (bit 12 of PR0 = 1).	0	R/W
7	COLEN	Collision test control. 1: collision test is enabled. 0: normal operation This bit, when set, causes the COL signal to be asserted as a result of the assertion of TX _EN within 512 BT. De-assertion of TX_EN will cause the COL signal to be de-asserted within 4BT.	0	R/W
6~0	---	Reserved	0	RO
R/W = Read/Write able. RO = Read Only.				

Table 3. Register Descriptions

Bit #	Name	Descriptions	Default Val	RW Type
PR1, MII Status Register. All the bits of this register are read only.				
15	T4	100BASE-T4 ability. Always 0, since STE400P has no T4 ability.	0	RO
14	TXFD	100BASE-TX full duplex ability. Always 1, since STE400P has the 100BASE-TX full duplex ability.	1	RO
13	TXHD	100BASE-TX half duplex ability. Always 1, since STE400P has the 100BASE-TX half duplex ability.	1	RO
12	10FD	10BASE-T full duplex ability. Always 1, since STE400P has 10Base-T full duplex ability.	1	RO
11	10HD	10BASE-T half duplex ability. Always 1, since STE400P has 10Base-T half duplex ability.	1	RO
10~7	---	Reserved	0	RO
6	MFPS	MF Preamble Suppression 0 = Will not accept management frames with preamble suppressed. A minimum of 32 preamble bits are required following power-on or hardware reset. One IDLE bit is required between any two management transactions as per IEEE 802.3u specification. 1 =Accepts management frames with preamble suppressed.	0	R/W
5	ANC	Auto-Negotiation Completed. 0: Auto-Negotiation process is not completed. 1: Auto-Negotiation process is completed.	0	RO
4	RF	Result of remote fault detection. 0: No remote fault condition detected. 1: Remote fault condition detected. This bit is set when the Link Partner transmits a remote fault condition (PR5 bit 13 = 1).	0	RO/LH*
3	AN	Auto-Negotiation ability. Always 1, since STE400P has the Auto-Negotiation ability.	1	RO
2	LINK	Link status. 0: a failure link condition occurred. Read to set. 1: a valid link is established.	0	RO/LL*
1	JAB	Jabber detection. 1: jabber condition is detected (10Base-T only).	0	RO/LH*
0	EXT	Extended register supporting. Always 1, since STE400P supports extended register	1	RO
LL* = Latching Low and clear by read. LH* = Latching High and clear by read.				
PR2- PID HI, PHY Identifier(HI)				
15~0	PHYID1	Pls. see NOTE on next page	1C04h	RO
PR3- PID LO, PHY Identifier (LO)				
15~10	PHYID2	Please see NOTE on next page	000000b	RO

Table 3. Register Descriptions

Bit #	Name	Descriptions	Default Val	RW Type
9~4	MODEL	Model number of STE400P. Six bits manufacture's model number.	000010b	RO
3~0	REV	Revision number of STE400P. Four bits manufacture's revision number.	0001b	RO
NOTE: ST-OUI = {PHYID1[1:0], PHYID2[15:12], PHYID1[9:8], PHYID1[7:2], PHYID1[10:9], PHYID1[15:10]} This translates to ST OUI of : 00-80-E1				
PR4- ANA, Auto-Negotiation Advertisement				
15	NXTPG	Next Page ability. 0: does not provide next page ability. 1: does provide next page ability.	0	R/W
14	---	Reserved		
13	RF	Remote Fault function. 1: with remote fault function.	0	R/W
12,11	---	Reserved		
10	FC	Flow Control function Ability. 1:supports PAUSE operation of flow control for full duplex link.	0	R/W
9	T4	100BASE-T4 Ability. Always 0: since STE400P doesn't have 100BASE-T4 ability.	0	RO
8	TXF	100BASE-TX Full duplex Ability. 1: with 100Base-TX full duplex ability.	1	R/W
7	TXH	100BASE-TX Half duplex Ability. 1: with 100Base-TX ability.	1	R/W
6	10F	10BASE-T Full duplex Ability. 1: with 10Base-T full duplex ability.	1	R/W
5	10H	10BASE-T Half duplex Ability. 1: with 10Base-T ability.	1	R/W
4~0	SF	Select field. Default 00001=IEEE 802.3	00001	RO
PR5- ANLP, Auto-Negotiation Link Partner ability				
15	LPNP	Link partner Next Page ability. 0: link partner without next page ability. 1: link partner with next page ability.	0	RO
14	LPACK	Received Link Partner Acknowledge. 0: link code work had not received yet. 1: link partner successfully received STE400P's Link Code Word.	0	RO
13	LPRF	Link Partner's Remote fault status. 0: no remote fault detected. 1: remote fault detected.	0	RO
12,11	---	Reserved	0	RO

Table 3. Register Descriptions

Bit #	Name	Descriptions	Default Val	RW Type
10	LPFC	Link Partner's Flow control ability. 0: link partner without PAUSE function ability. 1: link partner with PAUSE function full duplex link ability.	0	RO
9	LPT4	Link Partner's 100BASE-T4 ability. 0: link partner without 100BASE-T4 ability. 1: link partner with 100BASE-T4 ability.	0	RO
8	LPTXF	Link Partner's 100BASE-TX Full duplex ability. 0: link partner without 100BASE-TX full duplex ability. 1: link partner with 100BASE-TX full duplex ability.	0	RO
7	LPTXH	Link Partner's 100BASE-TX Half duplex ability. 0: link partner without 100BASE-TX. 1: link partner with 100BASE-TX ability.	0	RO
6	LP10F	Link Partner's 10BASE-T Full Duplex ability. 0: link partner without 10BASE-T full duplex ability. 1: link partner with 10BASE-T full duplex ability.	0	RO
5	LP10H	Link Partner's 10BASE-T Half Duplex ability. 0: link partner without 10BASE-T ability. 1: link partner with 10BASE-T ability.	0	RO
4~0	LPSF	Link partner select field. Default 00001=IEEE 802.3.	00000b	RO
PR6- ANE, Auto-Negotiation expansion				
15~5	---	Reserved	0	RO
4	PDF	Parallel detection fault. 0: no fault detected. 1: a fault detected via parallel detection function.	0	RO/LH*
3	LPNP	Link Partner's Next Page ability. 0: link partner without next page ability. 1: link partner with next page ability.	0	RO
2	NP	STE400P's next Page ability. 0: without next page ability. 1: with next page ability.	1	RO
1	PR	Page Received. 0: no new page has been received. 1: a new page has been received.	0	RO/LH*
0	LPAN	Link Partner Auto-Negotiation ability. 0: link partner has no Auto-Negotiation ability. 1: link partner has Auto-Negotiation ability.	0	RO
LH = High Latching and cleared by reading.				
PR7- NEXT PAGE, Auto-Negotiation Next Page Transmit Register				
15	Next Page	0: Last Page. 1: Additional Next Page or pages will follow.	0	R/W
14	---	Reserved	0	RO
13	Message Page	0: Unformatted Page. 1: Message page.	1	R/W

Table 3. Register Descriptions

Bit #	Name	Descriptions	Default Val	RW Type
12	ACK 2	Acknowledge 2 0: Cannot Comply with message 1: Will Comply with message	0	R/W
11	Toggle	0: Previous value of the transmitted Link Code Word = 0 1: Previous value of the transmitted Link Code Word = 1	0	RO
10~0	Message	Message / Unformatted Code Field	1	R/W
PR8- LP NXT PG, Auto-Negotiation Link Partner Next Page Transmit Register				
15	Next Page	0: Last Page. 1: Additional Next Page(s) will follow.	0	RO
14	---	Reserved	0	RO
13	Message Page	0: Unformatted Page. 1: Message page.	0	RO
12	ACK 2	Acknowledge 2 0: Cannot Comply with message 1: Will Comply with message	0	RO
11	Toggle	0: Previous value of the transmitted Link Code Word = 0 1: Previous value of the transmitted Link Code Word = 1	0	RO
10~0	Message	Message / Unformatted Code Field	0	RO
PR9- 100AUXCTL, 100BASE-X Auxiliary Control Register				
15,14	---	Reserved. Write as 0; Ignore on Read	00	
13	DISTX	1: Disable the Transmitter in the PHY. 0: Normal operation	0	R/W
12,11	---	Reserved. Write as 0; Ignore on Read	00	
10	DIS4B5B	Enable 4B/5B encoder and decoder 1: the 4B/5B encoder and decoder are bypassed 0: the 4B/5B encoder and decoder are enabled..	0	R/W
9	DISCRM	Disable Scramble. 1: the scrambler and de-scrambler are disabled. 0: the scrambler and de-scrambler is enabled.	0	R/W
8	DISNRZI	Enable the conversions between NRZ and NRZI. 1: disable the data conversion between NRZ and NRZI. 0: enable the data conversion of NRZI to NRZ in receiving and NRZ to NRZI in transmitting.	0	R/W
7~0	---	Reserved. Ignore on Read	00000000	
PR10- 100 AUX SR, 100BaseX Auxiliary Status Register				
15~10	---	Reserved	0	RO
9	Locked	1: descrambler locked 0: descrambler unlocked	0	RO

Table 3. Register Descriptions

Bit #	Name	Descriptions	Default Val	RW Type
8	100 LS	Current 100BaseX link status 1: link pass 0: link fail	0	RO
7~6		Reserved		
5	FCD	1: False Carrier Detected since last read 0: no False Carrier since last read	0	RO/LH
4	BAD ESD	1: ESD error detected since last read 0: no ESD error since last read	0	RO/LH
3	RED	1: Receive Error Detected since last read 0: no Receive Error since last read	0	RO/LH
2	TED	1: Transmit Error Detected since last read 0: no Transmit Error code received since last read	0	RO/LH
1	LCKED	1: Lock Error Detected since last read 0: no Lock Error since last read	0	RO/LH
0	MLT3CED	1: MLT3 Code Error Detected since last read 0: no MLT3 Code Error since last read	0	RO/LH
PR11- 100 RX EC, 100BaseX Receiver Error Counter				
15~8	Reserved	Write as “00h”; Ignore when Read	00h	RO
7~0	REC	Number of Non-collision packets with Receive Errors since last Read	00h	RO
PR12- 100 FCSC, 100BaseX False Carrier Sense Counter				
15~8	Reserved	Write as “00h”; Ignore when Read	00h	RO
7~0	FCSC	Number of False Carrier Sense events since last read	00h	RO
PR13- AUX CSR, Auxiliary Control/Status Register				
15	JD	1=Jabber function disabled in PHY 0=Jabber function enabled in PHY	0	R/W
14	LD	1=Link Integrity test disabled in PHY 0=Link Integrity test enabled in PHY	0	R/W
13~8	Reserved	Ignore when Read	000000	RO
7~6	HSQ:LSQ	These two bits define the Squelch Mode of the 10Base-T Carrier Sense mechanism: 00=Normal squelch 01=Low squelch 10=Highl squelch 11=not allowed	00	R/W
5~4	Reserved	Ignore when Read	00	RO
3	ANI	1=Auto Negotiation activated 0=Speed forced manually	1	RO

Table 3. Register Descriptions

Bit #	Name	Descriptions	Default Val	RW Type
2	FI (100/10)	Force Indication 1=Speed forced to 100Base-X 0=Speed forced to 10Base-T	0	RO
1	SI	Speed Indication 1=100Base-X 0=10Base-T	0	RO
0	FDI	Full Duplex Indication 1=Full-duplex active 0=Full-duplex not active	0	RO
PR14- AUX SSR, Auxiliary Status Summary Register				
15	ANC	1=Auto Negotiation process completed	0	RO
14	ANFLGC	1=Auto Negotiation FLP-Link Good Check	0	RO LH
13	ANAD	1=Auto Negotiation acknowledge detected	0	RO LH
12	ANABD	1=Auto Negotiation for link partner ability	0	RO LH
11	ANP	STE400P and link partner Pause Operation bit set	0	RO
10~8	AN HCD	000=NO Highest Common Denominator 001=10Base-T 010=10Base-T Full-duplex 011=100Base-TX 100=100Base-T4 101=100Base-TX Full-duplex 11x= undefined	000	RO
7	ANPDF	1=Parallel Detection fault	0	RO LH
6	LPRF	Link Partner Remote Fault		RO
5	LPPR	1=New page has been received	0	RO LH
4	LPANA	1=Link Partner is Auto-Negotiation capable	0	RO
3	SI	Speed Indicator 1=100 Mbps 0=10 Mbps	0	RO
2	LS	Link Status 1=Link is up (link pass state)	0	RO LL
1	ANE	1=Auto Negotiation Enabled	1	RO
0	JD	1=Jabber condition detected	0	RO LL
PR15- INT, Interrupt Register				
15	FDX LED E	Full Duplex LED Enable	0	R/W

Table 3. Register Descriptions

Bit #	Name	Descriptions	Default Val	RW Type
14	INTR E	Interrupt Enable	0	R/W
13	---	Reserved	0	RO
12	NP Mask	Next-Page Interrupt Mask	1	R/W
11	FDX Mask	Full-duplex Interrupt Mask	1	R/W
10	SPD Mask	SPEED Interrupt Mask	1	R/W
9	LK Mask	Link Interrupt Mask	1	R/W
8	INTR Mask	Master Interrupt Mask	1	R/W
7~5	Reserved		0	RO
4	NP_LP	Link-partner's next-page received		RO LH
3	FDX C	Duplex Change Interrupt	0	RO LH
2	SPD C	Speed Change Interrupt	0	RO LH
1	LNK C	Link Change Interrupt	0	RO LH
0	INTR S	Interrupt Status	0	RO LH
PR16- AUX M2, Auxiliary Mode 2 Register				
15~8	Reserved	Ignore when Read	FFh	RO
7	BEM (10Base-T)	1=10Base-T half duplex TXEN won't echo onto RXDV 0=10Base-T half duplex TXEN will echo onto RXDV	0	R/W
6	TM LED	1=Traffic Meter LED Mode On 0=Traffic Meter LED Mode Off	0	R/W
5	A LED FO	1=Activity LEDs Forced On 0=Activity LEDs not Forced	0	R/W
4	S LED	1=Serial LED Mode enabled 0=Serial LED Mode disabled	0	R/W
3	SQE D	1=SQE not transmitted in 10Base-T half-duplex 0=SQE transmitted in 10Base-T half-duplex	0	R/W
2~0	Reserved	Ignore when Read	000	RO
PR17- AUX EGSR 10Base-T Auxiliary Error and General Status Register				
15~10	Reserved	Ignore when Read	000	RO
9	EOF error	1=EOF detection error	0	RO
8	PI	1=Channel Polarity Inverted	0	RO
7~5	Revision	Revision Number	001	RO

Table 3. Register Descriptions

Bit #	Name	Descriptions	Default Val	RW Type
4	Reserved	Ignore when read	0	RO
3	ANI	1=Auto-Negotiation activated 0=Speed forced manually	1	RO
2	FI (100/10)	Force Indication 1=Speed forced to 100Base-X 0=Speed forced to 10Base-T	0	RO
1	SI	Speed Indication 1=100Base-X 0=10Base-T	0	RO
0	FDI	Full-duplex Indication 1=Full-duplex active 0=Full-duplex not active	0	RO
PR18- AUX MODE, Auxiliary Mode Register				
15~5	Reserved	Write as “00h”; Ignore when Read	000h	R/W
4	A LED FI	1=Disable XMT/RCV Activity LED outputs 0=Allow XMT/RCV Activity LED outputs	0	
3	L LED FI	1=Disable Link LED output 0=Allow Link LED output	0	
2	Reserved		0	RO
1	B TXEN	1=Enable Block TXEN mode	0	R/W
0	Reserved		0	RO
PR19- AUX MPR, Auxiliary Multiple PHY Register				
15	HCD_TX_ FDX	1=Auto Negotiation result is 100Base-TX full-duplex	0	RO
14	HCD_T4	0=STE400P doesn’t support 100Base-T4 ability	0	RO
13	HCD_TX	1=Auto Negotiation result is 100Base-TX	0	RO
12	HCD_FDX (10Base-T)	1=Auto Negotiation result is 10Base-T full-duplex	0	RO
11	HCD (10Base-T)	1=Auto Negotiation result is 10Base-T	0	RO
10~9	Reserved	Ignore when Read	0	RO
8	R AN	1=re-start Auto Negotiation process 0=no effect	0	R/W (SC)
7	ANC	1=Auto Negotiation process Completed 0=Auto Negotiation process not Completed	0	RO
6	FLP_L_GC	1=Auto Negotiation FLP-Link-Good-Check	0	RO
5	AckD	1=Auto Negotiation Acknowledge Detected	0	RO
4	AD	1=Auto Negotiation waiting for LP Ability	0	RO

Table 3. Register Descriptions

Bit #	Name	Descriptions	Default Val	RW Type
3	SI	1=Super Isolate Mode 0=Normal Operation	0	R/W
2~1	Reserved	Write as “00”; Ignore when Read	00	R/W
0	RXER C	1=Enable RXER Code Mode 0=Disable RXER Code Mode	0	R/W
SC = Self Clear				

7 DEVICE OPERATION

The STE400P integrates the IEEE802.3u compliant functions of PCS(physical coding sub-layer), PMA(physical medium attachment) sub-layer, and PMD(physical medium dependent) sub-layer for 100BASE-TX, and the IEEE802.3 compliant functions of Manchester encoding/decoding and transceiver for 10BASE-T. All the functions and operation schemes are described in the following sections.

7.1 100BASE-TX TRANSMIT OPERATION

Regarding the 100BASE-TX transmission, the device provides the transmission functions of PCS, PMA, and PMD for encoding of MII data nibbles to five-bit code-groups (4B/5B), scrambling, serialization of scrambled code-groups, converting the serial NRZ code into NRZI code, converting the NRZI code into MLT3 code, and then driving the MLT3 code into the category 5 Unshielded Twisted Pair cable through an isolation transformer with the turns ratio of 1: 1.

Data code-groups Encoder: In normal MII mode application, the device receives nibble type 4B data via the TxD0~3 inputs of the MII. These inputs are sampled by the device on the rising edge of Tx-clk and passed to the 4B/5B encoder to generate the 5B code-group used by 100BASE-TX.

Idle code-groups: In order to establish and maintain the clock synchronization, the device needs to keep transmitting signals to the medium. The device will generate Idle code-groups for transmission when there is no real data want to be sent by MAC.

Start-of-Stream Delimiter-SSD (/J/K/): In a transmission stream, the first 16 nibbles are MAC preamble. In order to let partner delineate the boundary of a data transmission sequence and to authenticate carrier events, the device will replace the first 2 nibbles of the MAC preamble with /J/K/ code-groups.

End-of-Stream Delimiter-ESD (/T/R/): In order to indicate the termination of the normal data transmissions, the device will insert 2 nibbles of /T/R/ code-group after the last nibble of FCS.

Scrambling: All the encoded data(including the idle, SSD, and ESD code-groups) is passed to the data scrambler to reduce the EMI and spread the power spectrum using a 10-bit scrambler seed loaded at the beginning.

Data conversion of Parallel to Serial, NRZ to NRZI, NRZI to MLT3: After scrambled, the transmission data with 5B type in 25MHz will be converted to serial bit stream in 125MHz by the parallel to serial function. After serialized, the transmission serial bit stream will be further converted from NRZ to NRZI format. This NRZI conversion function can be bypassed, if the bit 7 of PR19 register is cleared as 0. After NRZI converted, the NRZI bit stream is passed through MLT3 encoder to generate the TP-PMD specified MLT3 code. With this MLT3 code, it lowers the frequency and reduces the energy of the transmission signal in the UTP cable and also makes the system easily to meet the FCC specification of EMI.

Wave-Shaper and Media Signal Driver: In order to reduce the energy of the harmonic frequency of transmission signals, the device provides the wave-shaper prior to the line driver to smooth but keep symmetric the rising/falling edge of transmission signals. The wave-shaped signals include the 100BASE-TX and 10BASE-T both are passed to the same media signal driver. This design can simplify the external magnetic connection with single one.

7.2 100BASE-TX RECEIVING OPERATION

Regarding the 100BASE-TX receiving operation, the device provides the receiving functions of PMD, PMA, and PCS for receiving incoming data signals through category 5 UTP cable and an isolation transformer with turns ratio of 1: 1. It includes the adaptive equalizer and baseline wander, data conversions of MLT3 to NRZI, NRZI to NRZ and serial to parallel, the PLL for clock and data recovery, the de-scrambler, and the decoder of 5B/4B.

Adaptive Equalizer and Baseline Wander: Since the high speed signals over the unshielded (or shielded) twisted Pair cable will induce the amplitude attenuation and phase shifting. Furthermore, these effects are depends on the signal frequency, cable type, cable length and the connectors of the cabling. So a reliable adaptive equalizer and baseline wander to compensate all the amplitude attenuation and phase shifting are necessary. In the transceiver, it provides the robust circuits to perform these functions.

MLT3 to NRZI Decoder and PLL for Data Recovery: After receiving the proper MLT3 signals, the device converts the MLT3 to NRZI code for further processing. After adaptive equalizer, baseline wander, and MLT3 to NRZI decoder, the compensated signals with NRZI type in 125MHz are passed to the Phase Lock Loop circuits to extract out the original data and synchronous clock.

Data Conversions of NRZI to NRZ and Serial to Parallel: After data is recovered, the signals will be passed to the NRZI to NRZ converter to generate the 125 MHz serial bit stream. This serial bit stream will be packed to parallel 5B type for further processing. The NRZI to NRZ conversion can be bypassed, if the bit 7 of PR19 register is cleared as 0.

De-scrambling and Decoding of 5B/4B: The parallel 5B type data is passed to de-scrambler and 5B/4B decoder to return their original MII nibble type data.

Carrier sensing: Carrier Sense(CRS) signal is asserted when the STE400P detects any 2 non-contiguous zeros within any 10 bit boundary of the receiving bit stream. CRS is de-asserted when ESD code-group or Idle code-group is detected. In half duplex mode, CRS is asserted during packet transmission or receive. But in full duplex mode, CRS is asserted only during packet reception.

7.3 10BASE-T TRANSMISSION OPERATION

This includes the parallel to serial converter, Manchester Encoder, Link test function, Jabber function and the transmit wave-shaper and line driver described in the section of “Wave-Shaper and Media Signal Driver” of “100BASE-T Transmission Operation”. It also provides Collision detection and SQE test for half duplex application.

7.4 10BASE-T RECEIVE OPERATION

This includes the carrier sense function, receiving filter, PLL for clock and data recovering, Manchester decoder, and serial to parallel converter.

7.5 LOOP-BACK OPERATION

The STE400P provides internal loop-back option for both the 100BASE-TX and 10BASE-T operations. Setting bit 14 of PR0 register to 1 can enable the loop-back option. In this loop-back operation, the TX± and RX± lines are isolated from the media. The STE400P also provides remote loop-back operation for 100BASE-TX operation. Setting bit 9 of PR19 register to 1 enables the remote loop-back operation.

In the 100BASE-TX internal loop-back operation, the data comes from the transmit output of NRZ to NRZI converter then loop-back to the receive path into the input of NRZI to NRZ converter.

In the 100BASE-TX remote loop-back operation, the data is received from RX± pins through receive path to the output of data and clock recover and then loop-back to the input of NRZI to MLT3 converter of transmit path then transmit out to the medium via the transmit line drivers.

In the 10BASE-T loop-back operation, the data is through transmit path and loop-back from the output of the Manchester encoder into the input of Phase Lock Loop circuit of receive path.

7.6 FULL DUPLEX AND HALF DUPLEX OPERATION

The STE400P can operate for either full duplex or half duplex network application. In full duplex, both transmit and receive can be operated simultaneously. Under full duplex mode, collision(COL) signal is ignored and carrier sense(CRS) signal is asserted only when the STE400P is receiving.

In half duplex mode, either transmit or receive can be operated at one time. Under half duplex mode, collision signal is asserted when transmit and receive signals collided and carrier sense asserted during transmission and reception.

7.7 AUTO-NEGOTIATION OPERATION

The Auto-Negotiation function is designed to provide the means to exchange information between the STE400P and the network partner to automatically configure both to take maximum advantage of their abilities, and both are setup accordingly. The Auto-Negotiation function can be controlled through ANE, bit 12 of the PR0 register.

Auto-Negotiation exchanges information with the network partner using the Fast Link Pulses(FLPs) - a burst of link pulses. There are 16 bits of signaling information contained in the burst pulses to advertise all remote partner's capabilities which are determined by the register of PR4. According to this information they find out their highest common capability by following the priority sequence as below:

1. 100BASE-TX full duplex
2. 100BASE-TX half duplex
3. 10BASE-T full duplex
4. 10BASE-T half duplex

During power-up or reset, if Auto-Negotiation is found enabled then FLPs will be transmitted and the Auto-Negotiation function will proceed. Otherwise, the Auto-Negotiation will not occur until the bit 12 of PR0 register is set to 1. When Auto-Negotiation is disabled, then the Network Speed and Duplex Mode are selected by programming PR0 register.

7.8 POWER DOWN OPERATION

To reduce the power consumption, the STE400P is designed with a power down feature, which can save the power consumption significantly. Since the power supply of the 100BASE-TX and 10BASE-T circuits are separated, the STE400P can turn off the circuit of either the 100BASE-TX or 10BASE-T when the other one of them is operating. There is also a Power Down mode which can be selected by PDEN in register PR0 bit 11. During the Power Down mode, TXP/TXN outputs and all LED outputs are 3-stated, and the MII interface is isolated. During Power Down mode the MII management interface is still available for reading and writing device registers. Power Down mode can be exited by clearing bit 11 of register PR0 or by a hardware or software reset (setting PR0:15=1).

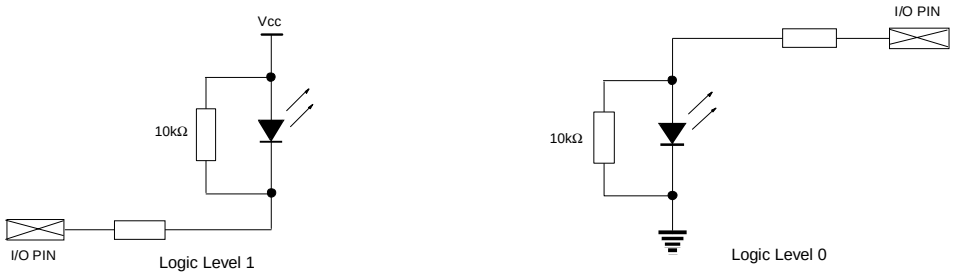
7.9 LED DISPLAY OPERATION

The STE400P provides 2 functions for the LED pins, the detail descriptions about the operation are described in the PIN Description section, and as follows.

7.10 RESET OPERATION

There are two ways to reset the STE400P. First, for hardware reset, the STE400P can be reset via RESET pin (pin 119). The active low Reset input signal is required at least 1 ms to ensure proper reset operation. Second, for software reset, when bit 15 of register PR0 is set to 1, the STE400P will reset entire circuits and registers to their default values, and clear the bit 15 of PR0 to 0. Both hardware and software reset operations initialize all registers to their default values. This process includes re-evaluation of all hardware-configurable registers. Logic levels on several I/O pins are detected during hardware reset period to determine the initial functionality of STE400P. Some of these pins are used as outputs after the reset operation. Care must be taken to ensure that the configuration setup will not interfere with normal operation. Dedicated configuration pins can be tied to the Vcc or ground directly. Configuration pins multiplexed with LED outputs should be weakly pulled up or weakly

pulled down through resistors as shown in the following circuits.



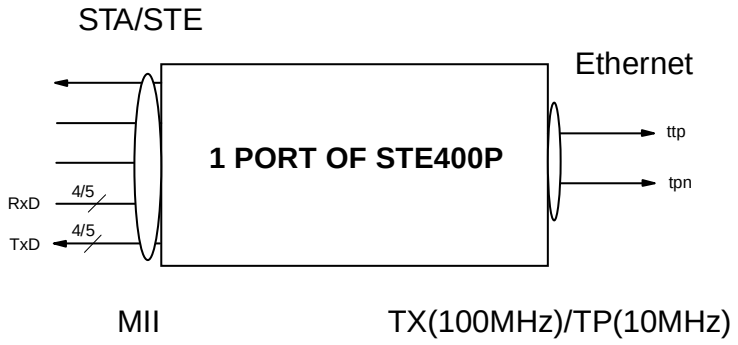
7.11 PREAMBLE SUPPRESSION

Preamble suppression mode in the STE400P is indicated by a one in bit six of the PR1 Register. If it is determined that all PHY devices in the system support preamble suppression, then a preamble is not necessary for each management transaction. The first transaction following power-up/hardware reset requires 32 bits of preamble. The full 32 bit preamble is not required for each additional transaction. The STE400P will respond to management accesses without preamble, but a minimum of one idle bit between management transactions is required as specified in IEEE 802.3u.

7.12 REMOTE FAULT

The remote fault function indicates to a link partner that a fault condition has occurred by using the Remote Fault bit, which is encoded in bit 13 of the Link Code Word. A local device indicates to its link partner that it has found a fault by setting the Remote Fault bit in the Auto-Negotiation register to logic one and renegotiating with the link partner. The Remote Fault bit remains at logic one until successful negotiation with the Link Code Word occurs. The bit will then return to 0. When the message is sent that the Remote Fault bit is set to logic one, the device will set the Remote Fault bit in the MII to logic one if the management function is present.

7.13 TRANSMIT ISOLATION



8 ELECTRICAL SPECIFICATIONS AND TIMINGS

Table 4. Absolute Maximum Ratings

Parameter	Value
Supply Voltage(Vcc)	-0.5 V to 5.5 V
Input Voltage	-0.5 V to VCC + 0.5 V
Output Voltage	-0.5 V to VCC + 0.5 V
Storage Temperature	-65 °C to 150 °C(-85°F to 302°F)
Ambient Temperature	0°C to 70°C(32°F to 158°F)
ESD Protection	2000V

Table 5. General DC Specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
General DC						
Vcc	Supply Voltage		3.15	3.3	3.45	V
10BASE-T Voltage/Current Characteristics						
Vida10	Input Differential Accept Peak Voltage	5MHz ~ 10MHz	585		3100	mV
Vidr10	Input Differential Reject Peak Voltage	5MHz ~ 10MHz	0		585	mV
Vod10	Output Differential Peak Voltage		2200		2800	V
Icc10	Supply Current	100% utilization, min. IPG, Vcc=3.3V, including TX output driver		270		mA
100BASE-TX Voltage/Current Characteristics						
Vida100	Input Differential Accept Peak Voltage		200		1000	mV
Vidr100	Input Differential Reject Peak Voltage		0		200	mV
Vod100	Output Differential Peak Voltage		950		1050	V
Icc100	Supply Current	100% utilization, min. IPG, Vcc=3.3V, including TX output driver		390		mA

Table 6. AC Specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
X1 Specifications						
TX1d	X1 Duty Cycle		45	50	55	%
TX1p	X1 Period			30		ns
TX1t	X1 Tolerance					PPM
10BASE-T Normal Link Pulse(NLP) Timings Specifications						
TNPW	NLP Width	10Mbps		100		ns
TNPC	NLP Period	10Mbps	8		24	ms

Figure 2. Normal Link Pulse timings

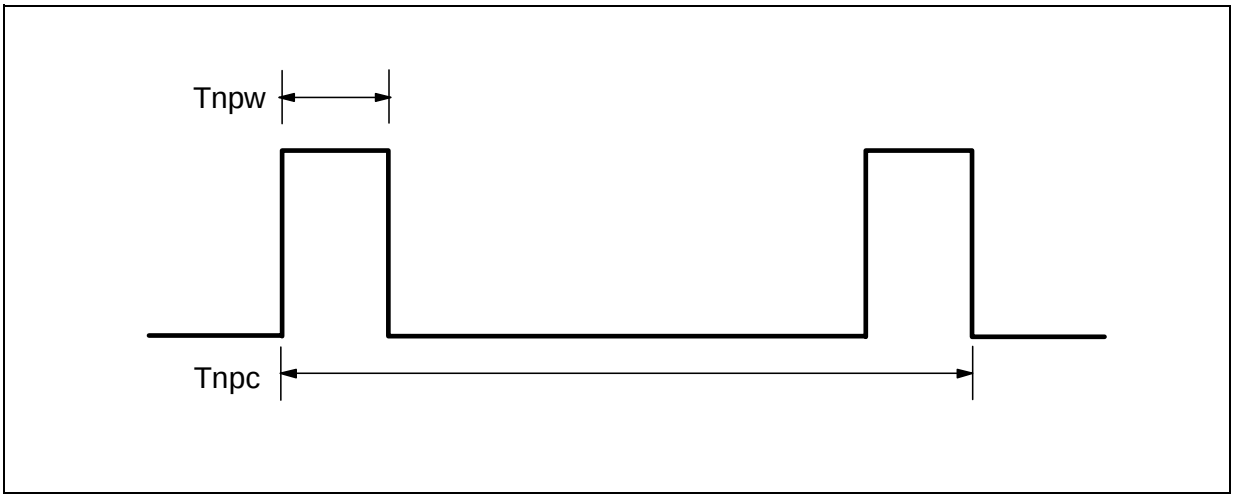


Table 7. AC Specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Auto-Negotiation Fast Link Pulse(FLP) Timings Specifications						
Tflpw	FLP Width			100		ns
Tflcpp	Clock pulse to clock pulse period		111	125	139	µs
Tflcpd	Clock pulse to Data pulse period		55.5	62.5	69.5	µs
-	Number of pulses in one burst		17		33	pulse
Tflbw	Burst Width			2		ms
Tflbp	FLP Burst period		8	16	24	ms

Figure 3. Fast Link Pulse timing

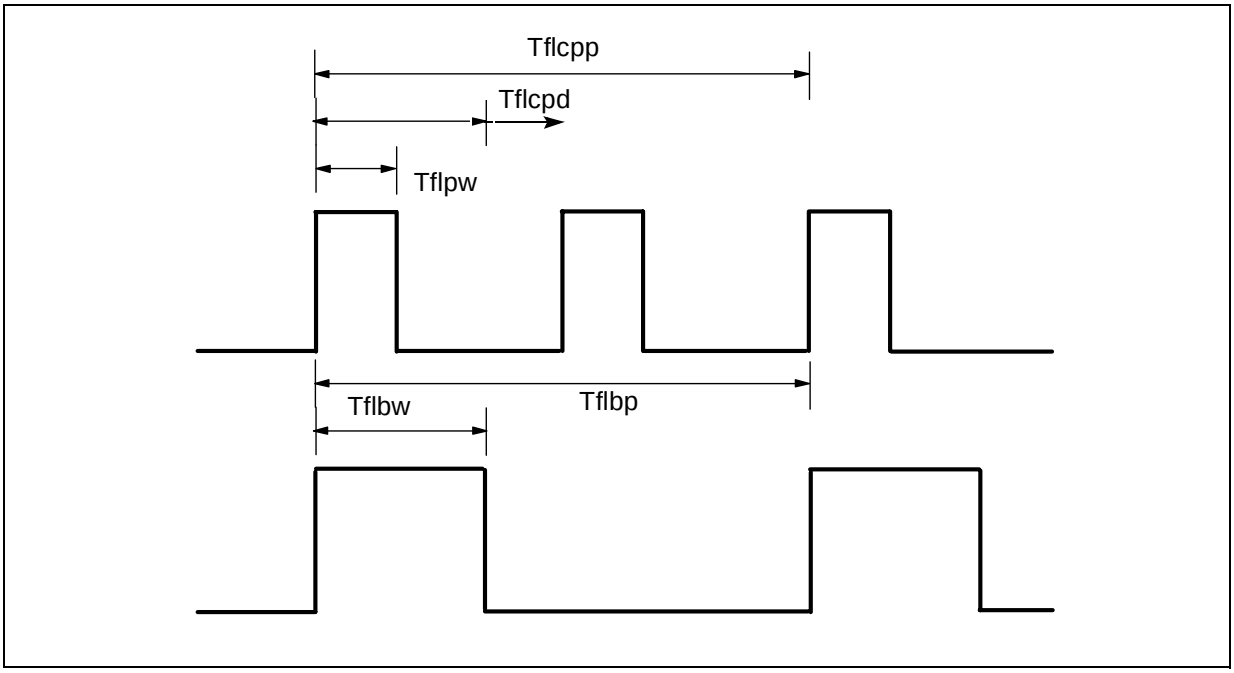


Table 7. AC Specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
100BASE-TX Transmitter AC Timings Specification						
Tjit	TDP-TDN Differential Output Peak Jitter				1.4	ps
MII Management Clock Timing Specifications						
t1	MDC Low Pulse Width		200		—	ns
t2	MDC High Pulse Width		200		—	ns
t3	MDC Period		400		—	ns
t4	MDIO(I) Setup to MDC Rising Edge		10		—	ns
t5	MDIO(O) Hold Time from MDC Rising Edge		10		—	ns
t6	MDIO(O) Valid from MDC Rising Edge		0		300	ns

Figure 4. MII Management Clock Timing

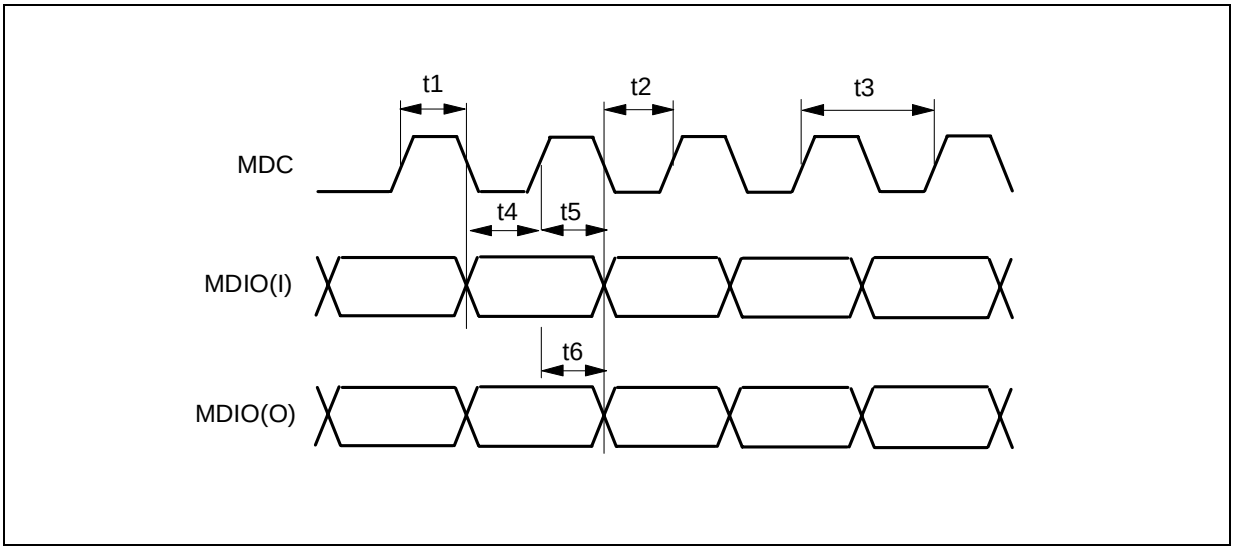


Table 7. AC Specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
MII Receive Timing Specification						
t1	RX-ER, RX-DV, RXD[3:0] Setup to RX-CLK		10		—	ns
t2	RX-ER, RX-DV, RXD[3:0] Hold After RX-CLK		10		—	ns
t3	RX-CLK High Pulse Width (100 Mbits/s)		14		26	ns
	RX-CLK High Pulse Width (10 Mbits/s)			200		ns
t4	RX-CLK Low Pulse Width (100 Mbits/s)		14		26	ns
	RX-CLK Low Pulse Width (10 Mbits/s)		140		260	ns
t5	RX-CLK Period (100 Mbits/s)			40		ns
	RX-CLK Period (10 Mbits/s)			400		ns

Figure 5. MII Receive Timing

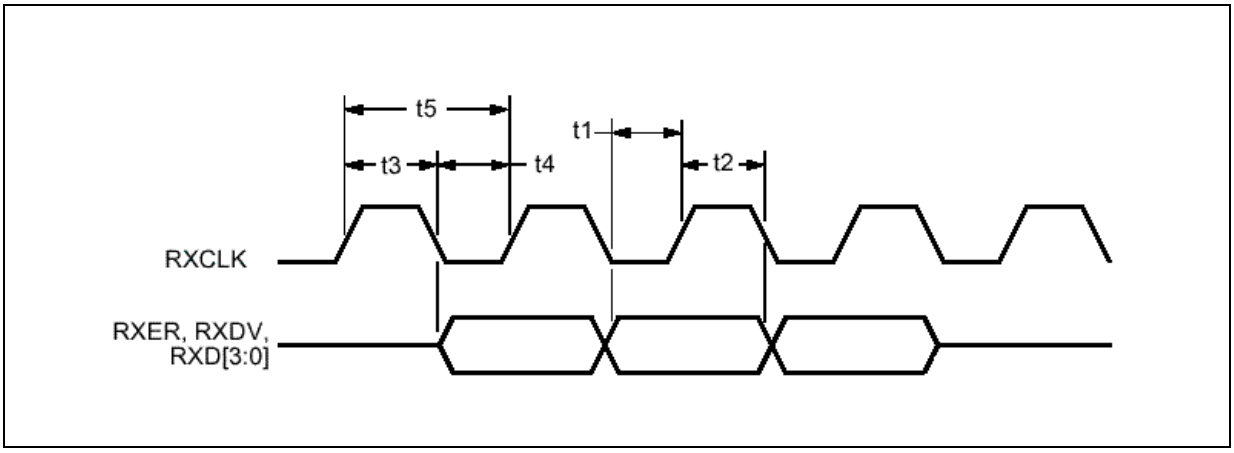


Table 7. AC Specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
MII Transmit Timing Specification						
t1	TX-ER,TX-EN,TXD[3:0] Setup to TX-CLK Rise		10		—	ns
t2	TX-ER,TX-EN,TXD[3:0] Hold After TX-CLK Rise		0		25	ns

Figure 6. MII Transmit Timing

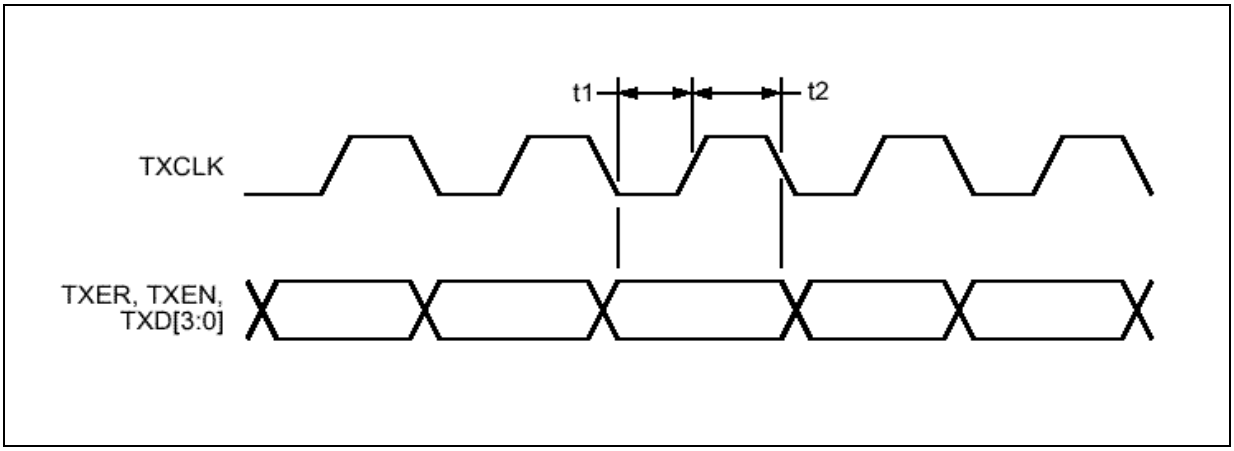


Table 7. AC Specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Receive Timing Specification						
Rt1	Receive Frame to Sampled Edge of RX-DV (100 Mbits/s)		—		15	bits
	Receive Frame to Sampled Edge of RX-DV (10 Mbits/s)		—		22	bits
Rt2	Receive Frame to CRS High (100Mbits/s)		—		13	Bits
	Receive Frame to CRS High (10 Mbits/s)		—		5	bits
Rt3	End of Receive Frame to Sampled Edge of RX-DV (100 Mbits/s)		—		12	bits
	End Receive Frame to Sampled Edge of RX-DV (10 Mbits/s)		—		4	bits
Rt4	End of Receive Frame to CRS Low (100 Mbits/s)		13		24	bits
	End of Receive Frame to CRS Low (10 Mbits/s)		—		4.5	bits

Figure 7. Receive Timing

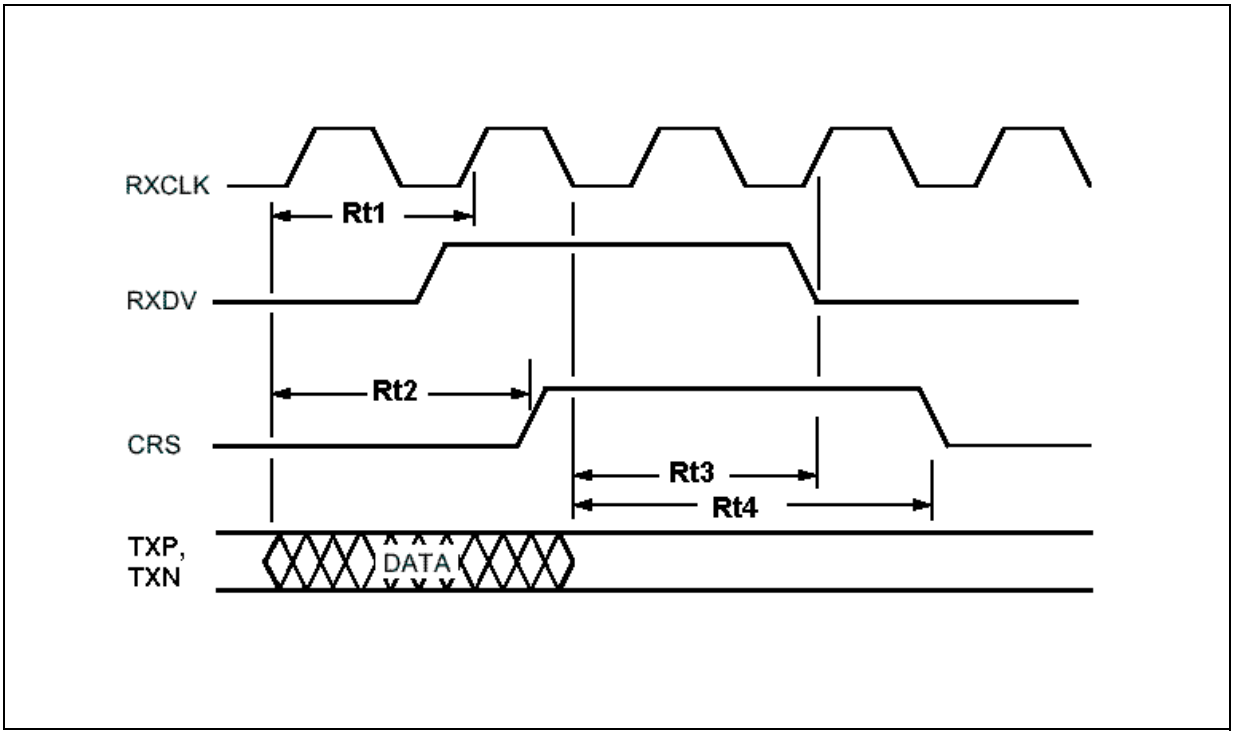


Table 7. AC Specifications

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Transmit Timing Specification						
t1	TX-EN Sampled to CRS High (100 Mbits/s)		0		4	bits
	TX-EN Sampled to CRS High (10 Mbits/s)		—		1.5	bits
t2	TX-EN Sampled to CRS Low (100 Mbits/s)		0		16	bits
	TX-EN Sampled to CRS Low (10 Mbits/s)		—		16	bits
t3	Transmit Latency (100 Mbits/s)		6		14	bits
	Transmit Latency (10 Mbits/s)		4		—	bits
t4	Sampled TX-EN Inactive to End of Frame (100 Mbits/s)		—		17	bits
	Sampled TX-EN Inactive to End of Frame (10 Mbits/s)		—		5	bits

Figure 8. Transmit Timing

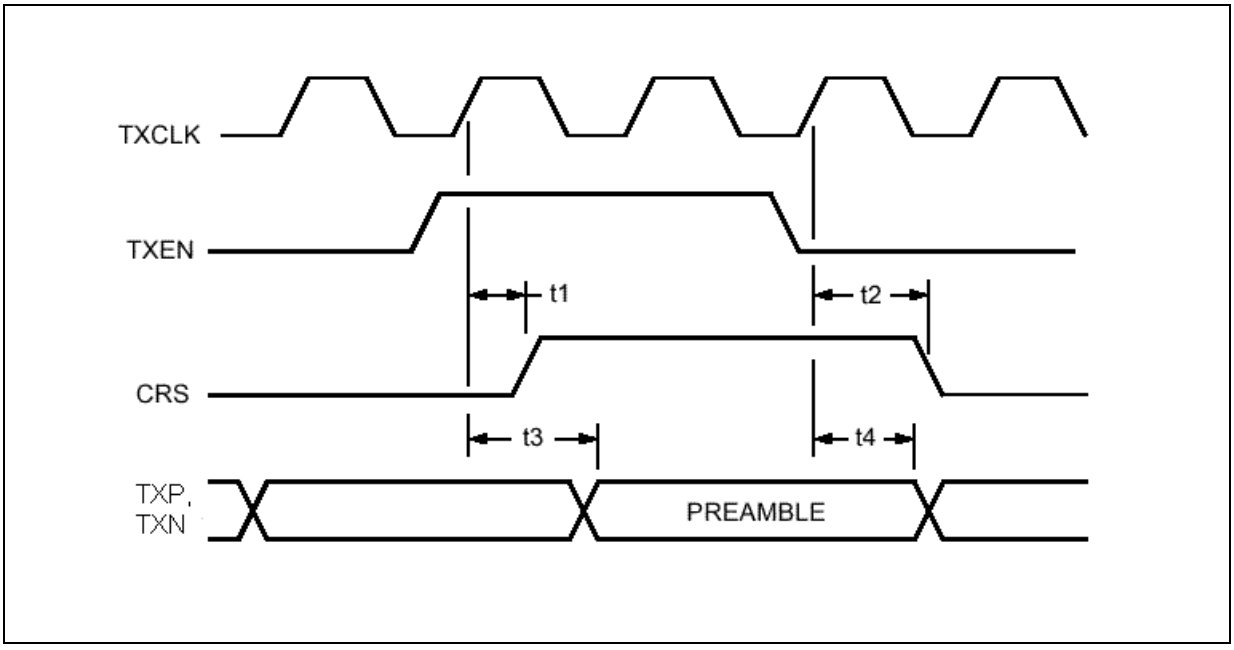
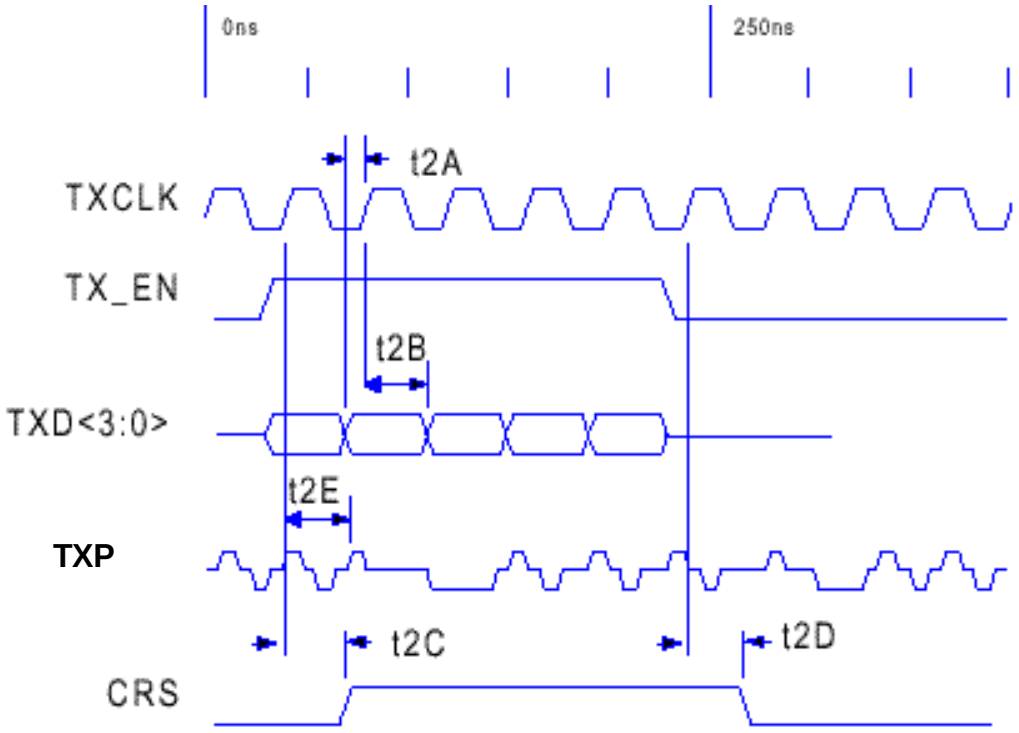
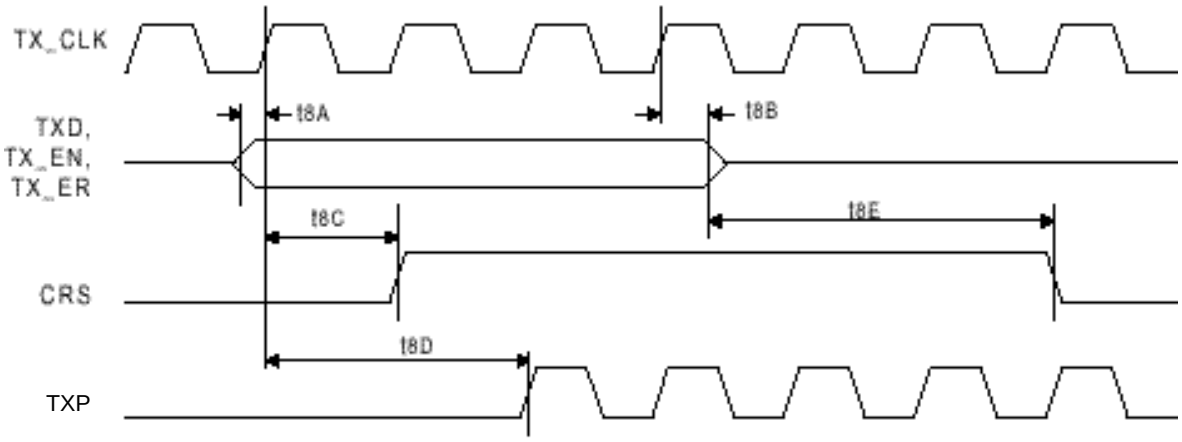


Figure: 11 Transmit Timing



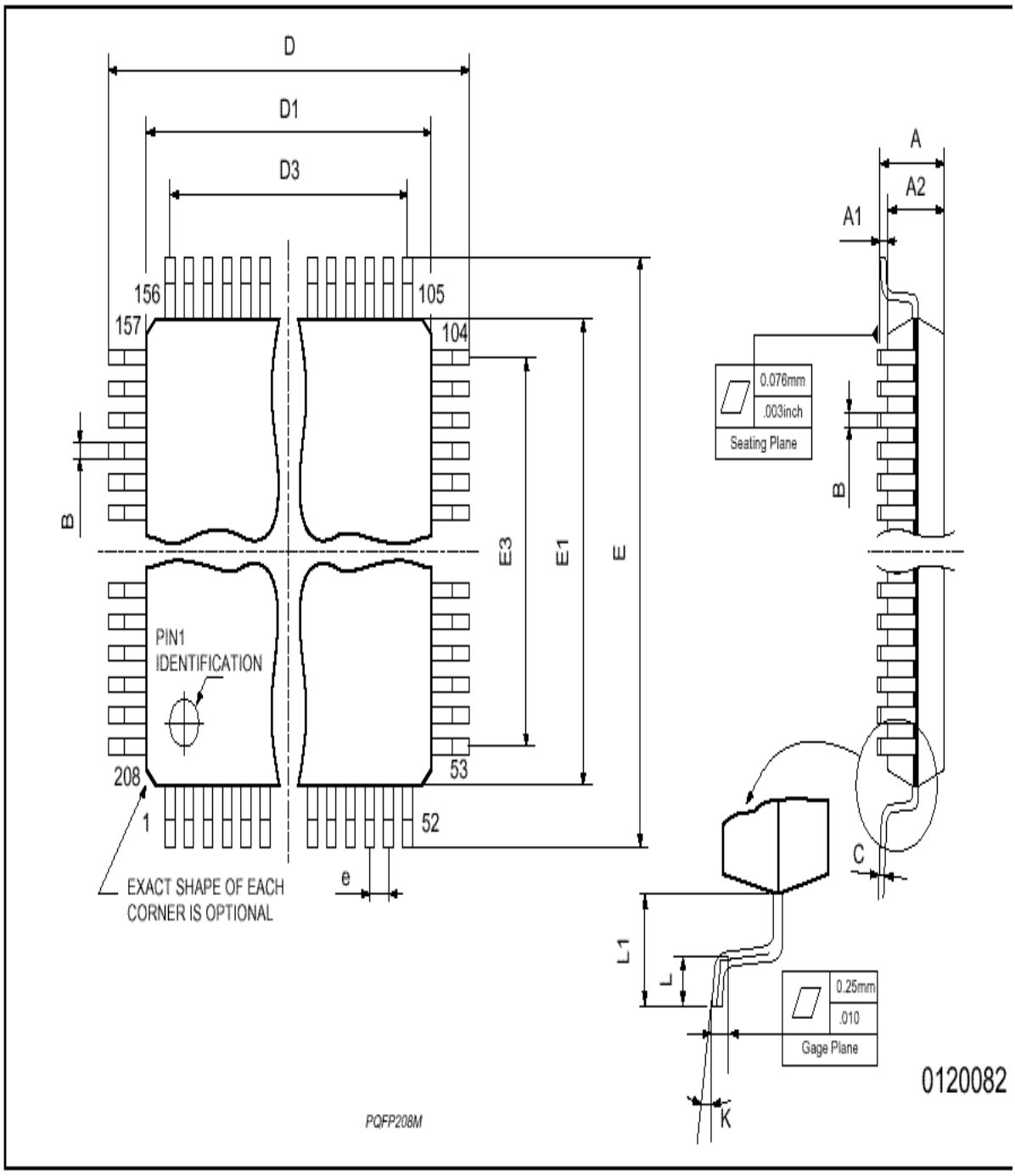
Parameter	Sym	Min	Typ	Max	Units
TXD, TX_EN, TX_ER Setup to TX_CLK High	t2A	10	-	-	ns
TXD, TX_EN, TX_ER Hold from TX_CLK High	t2B	5	-	-	ns
TX_EN sampled to CRS asserted	t2C	-	3	4	BT
TX_EN sampled to CRS de-asserted	t2D	-	4	16	BT
TX_EN sampled to TXP out (Tx latency)	t2E	6	10	14	BT
BT is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate.					

Figure 12: 10Base-T Transmit Timing



Parameter	Sym	Min	Typ	Max	Units
TXD, TX_EN, TX_ER Setup to TX_CLK High	t8A	10	-	-	ns
TXD, TX_EN, TX_ER Hold from TX_CLK High	t8B	5	-	-	ns
TX_EN sampled to CRS asserted	t8C	-	0	4	BT
TX_EN sampled to CRS de-asserted	t8D	-	8		BT
TX_EN sampled to TXP out (Tx latency)	t8E	-	3-5		BT
BT is the duration of one bit as transferred to and from the MAC and is the reciprocal of the bit rate.					

9.0 PACKAGE


D
D1
D3
156
105
157
104
208
53
1
52
B
E3
E1
E
PIN1
IDENTIFICATION
EXACT SHAPE OF EACH
CORNER IS OPTIONAL
e
A
A2
A1
0.076mm
.003inch
Seating Plane
B
C
L1
L
0.25mm
.010
Gage Plane
K
PQFP208M
0120082

PACKAGE TYPE: PQFP 208 / BODY 28X28X3.49mm

REF	Dimensions mm			Dimensions inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX
A			4.10			0.161
A1	0.25			0.010		
A2	3.40	3.20	3.60	0.134	0.126	0.142
B	0.17		0.27	0.007		0.011
C	0.09		0.20	0.003		0.008
D		30.60			1.205	
D1		28.00			1.102	
D3		25.50			1.004	
e		0.50			0.020	
E		30.60			1.205	
E1		28.00			1.102	
E3		25.50			1.004	
L	0.45	0.60	0.75	0.018	0.024	0.029
L1		1.30			0.51	
K	0 deg. (min), 3.5 deg. (typ.), 7 deg.(max)					