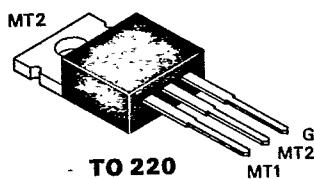


TAG SEMICONDUCTORS LTD



## T1612BH – T1612NH TRIACS

**16.0 A 200–800 V  
50/50/50/50 mA**

The T1612 series of TRIAC's are high performance glass passivated PNPN devices. These parts are intended for general purpose high current applications where moderate gate insensitivity is required.

### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	<b>T1612BH</b>	$V_{DRM}$	200		V	
	<b>T1612DH</b>		400		V	$T_j = -40^\circ\text{C} \text{ to } 125^\circ\text{C}$
	<b>T1612MH</b>		600		V	$R_{GK} = 1\text{ k}\Omega$
	<b>T1612NH</b>		800		V	
On-State Current		$I_T(\text{RMS})$	16		A	All Conduction Angles $T_C = 85^\circ\text{C}$
Nonrept. On-State Current		$I_{TSM}$	165		A	Half Cycle, 60 Hz
Nonrept. On-State Current		$I_{TSM}$	150		A	Half Cycle, 50 Hz
Fusing Current		$I^2t$	112		$\text{A}^2\text{s}$	$t = 10\text{ ms}$
Peak Gate Current		$I_{GM}$	4		A	$10\mu\text{s}$ max.
Peak Gate Dissipation		$P_{GM}$	10		W	$10\mu\text{s}$ max.
Gate Dissipation		$P_{G(\text{AV})}$	1		W	20 ms max.
Operating Temperature		$T_j$	-40	125	$^\circ\text{C}$	
Storage Temperature		$T_{stg}$	-40	125	$^\circ\text{C}$	
Soldering Temperature		$T_{sld}$		250	$^\circ\text{C}$	1.6 mm from case, 10 s max.

### Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions	
Off-State Leakage Current	$I_{DRM}$	2.5	mA		$V_D = V_{DRM}$ $R_{GK} = 1\text{ k}\Omega$ $T_j = 125^\circ\text{C}$	
Off-State Leakage Current	$I_{DRM}$	10	$\mu\text{A}$		$V_D = V_{DRM}$ $R_{GK} = 1\text{ k}\Omega$ $T_j = 25^\circ\text{C}$	
On-State Voltage	$V_T$	1.48	V		at $I_T = 24\text{ A}$ , $T_j = 25^\circ\text{C}$	
On-State Threshold Voltage	$V_{T(\text{TO})}$	0.9	V		$T_j = 125^\circ\text{C}$	
On-State Slope Resistance	$r_T$	25	$\text{m}\Omega$		$T_j = 125^\circ\text{C}$	
Gate Trigger Current	$I_{GT\text{I+}}$ (1)	50	mA		$V_D = 12\text{ V}$	
	$I_{GT\text{I-}}$ (2)	50	mA		$V_D = 12\text{ V}$	
	$I_{GT\text{III-}}$ (3)	50	mA		$V_D = 12\text{ V}$	
	$I_{GT\text{III+}}$ (4)	50	mA		$V_D = 12\text{ V}$	
Gate Trigger Voltage	$V_{GT}$	2.5	V		$V_D = 12\text{ V}$ All Quadrants	
Holding Current	$I_H$	50	mA		$R_{GK} = 1\text{ k}\Omega$	
Critical Rate of Voltage Rise	$dv/dt$	500		$\text{V}/\mu\text{s}$	$V_D = .67 \times V_{DRM}$ $R_{GK} = 1\text{ k}\Omega$ $T_j = 125^\circ\text{C}$	
Critical Rate of Rise, Off-State	$dv/dt_c$	5		$\text{V}/\mu\text{s}$	$I_T = 16\text{ A}$ $di/dt = 7.1\text{ A/ms}$ $T_C = 85^\circ\text{C}$	
Thermal Resistance junc. to case	$R_{\Theta jc}$	1.8	K/W			
Thermal Resistance junc. to amb.	$R_{\Theta ja}$	60	K/W			

