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0.35 μm CMOS Gate Array

CMOS-9HD Family

Considerable cost reduction

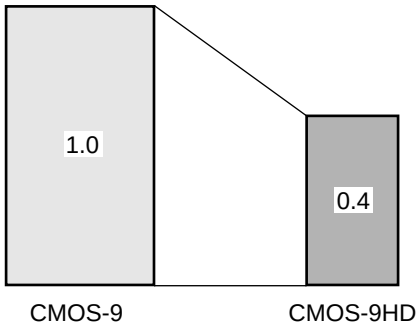
New Products

FEATURES

The CMOS-9HD Family is a channel-less type gate array that uses the 0.35-μm leading-edge process and realizes 960,000 usable gates. This family is adaptable for both high-speed and low-power consumption systems. Currently supporting a 3.3-V supply voltage, it is expected that the future lineup will be able to support a supply voltage of 2.5 V.

High Integration/Low Power Consumption

- Maximum of 960,000 usable gates integrated
- Improved cell structure, higher density
- Lower power consumption (a further 30% reduction from CMOS-9)



◀ **Cell size comparison (1 cell)**

CMOS-9: NEC's conventional 0.35-μm gate array

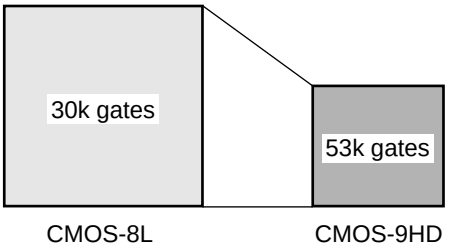
In Pursuit of Lower Cost

- Enhanced cost competitiveness through chip-size shrinkage
- Fewer gate masters leading to further cost reduction

(Example) Comparison with CMOS-8L

Although the 30k-gate CMOS-8L and the 53k-gate CMOS-9HD are similar in terms of price, because the cell density is higher in the CMOS-9HD, for an area of 30k integrated gates or more, the CMOS-9HD is the more cost-competitive choice.

Note that the applicable-package pin-count range differs depending on the chip size, even if the gate scale is identical.



◀ **Chip size comparison**

CMOS-8L: NEC's conventional 0.5-μm gate array

Ultra High-Speed Operation

- t_{PD} = 131 ps (2-input NAND, fanout = 1, standard wiring length)
- t_{PD} = 107 ps (2-input NAND (power gate), fanout = 1, standard wiring length)
- t_{PD} = 229 ps (input buffer, fanout = 1, standard wiring length)
- t_{PD} = 222 ps (input buffer, standard load)
- t_{PD} = 1396 ps (output buffer, C_L = 50 pF)

Provision of Function Block Enabling High Speed/High Integration

- Including high speed and low power, compatible with CMOS-8L Family
- Scan path block
- Driver for clock tree synthesis
- Asynchronous single-port RAM (45 types)
- Asynchronous dual-port RAM (45 types)
- Asynchronous compiled single-port RAM
- Synchronous/asynchronous compiled dual-port RAM

Abundance of Peripheral Blocks

- LVTTL/TTL 5-V withstand voltage interface buffer
- LVTTL interface buffer with fail safe function
- High drive capacity buffer (I_{OL} = 24 mA)
- PCI
- GTL+
- Low-noise buffer
- Buffers with on-chip pull-up resistors (5 kΩ, 50 kΩ)
- Buffers with on-chip pull-down resistors (50 kΩ)
- Digital PLL (33 to 80 MHz)
- Digital PLL (multiple)

Power Consumption

- 0.524 μW/MHz/cell (Internal gates, V_{DD} = 3.3 V)

Support of Variety of Pin Count Packages

- 100- to 304-pin plastic QFP (fine-pitch)
- 160-pin, 208-pin plastic QFP (fine-pitch, with heat spreader)
- 48- to 120-pin plastic TQFP
- 144-pin plastic LQFP
- 225- to 352-pin plastic BGA
- 108- to 304-pin plastic FBGA
- 256- to 696-pin tape BGA (with heat spreader)

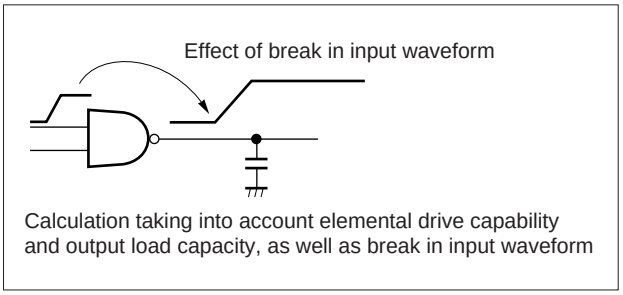
Precision Delay Estimation

<Wiring length calculation>

- Can be calculated using a floorplan
- Floorplan-calculated wiring length can be used in logic synthesis and design rule check programs

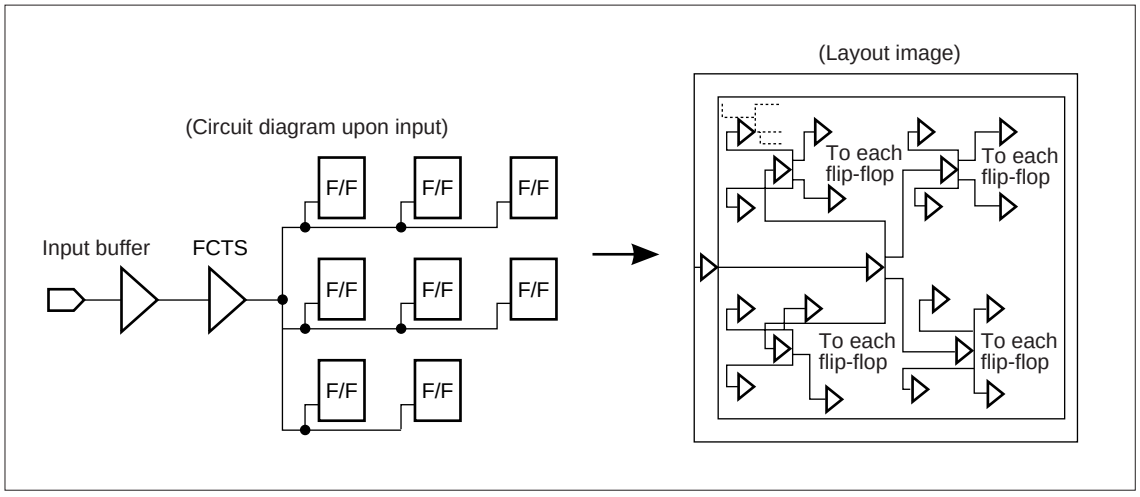
<Delay calculation>

- Takes into account the break in the block's input waveform



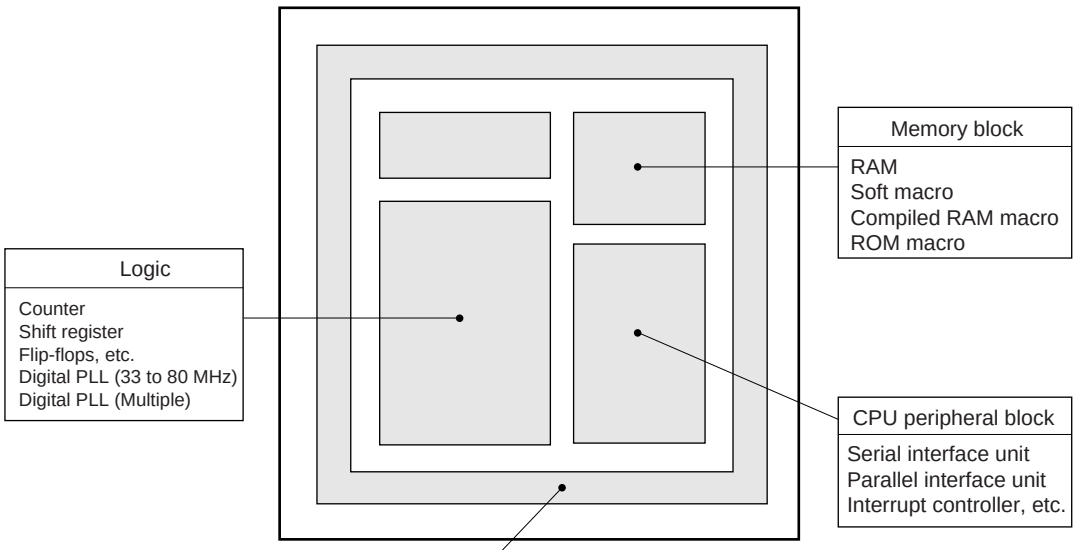
Clock Tree Synthesis

- Clock tree automatically synthesized during layout to minimize clock skew
- Up to 10000 flip-flops can be connected



Multifarious Function Block Mounting Capability

The function blocks ensure functional compatibility with conventional products and facilitate transfer or appropriation of existing design data.



Interface block	
GTL+	Open-drain buffer
PCI[Note]	LVTTL interface buffer with fail safe function
5-V withstand voltage/LVTTL buffer	High drive capacity buffer (I_{OL} = 24 mA)
Low-noise buffer	Buffers with pull-up resistors (5 kΩ, 50 kΩ)
3-state buffer	Buffers with pull-down resistors (50 kΩ)

Note Standard interface recommended by Intel Corp. (PCI = Peripheral Component Interconnect)

Applications (Supported Fields)

All fields from large-scale high-speed processing systems to small and medium scale general applications are covered.

- Multimedia market

  PC, AV, moving picture processing, 3D, etc.

- Communications market

  High-speed communication, cellular terminals, etc.

- OA, industrial, and other applications.

PRODUCT OUTLINE

List of Product Types

3-layer wiring

Part Number	μPD65943	μPD65944	μPD65945	μPD65946	μPD65948	μPD65949	μPD65951	μPD65954	μPD65956	μPD65958
Number of signals	156	180	200	252	308	364	416	496	572	692
Number of pads	172	196	216	268	324	380	436	516	588	708
Number of integrated gates	75740	100602	128338	202630	312684	437136	585390	835664	1096452	1615646
Number of usable gates	53018	70421	89836	141841	218879	262281	321964	459615	603048	807823

Remark The actual number of usable signal lines depends on the package and the number of power supply and GND pins used.

4-layer wiring

Part Number	μPD65961	μPD65964	μPD65966	μPD65968	μPD65969	μPD65970	μPD65971
Number of signals	–	–	–	–	–	–	–
Number of pads	436	516	588	708	764	820	876
Number of integrated gates	585390	835664	1096452	1615646	1904700	2196592	2509284
Number of usable gates	380503	54318	712693	969387	1142820	1317955	1505570

Remark The actual number of usable signal lines depends on the package and the number of power supply and GND pins used.

List of Packages

3-layer wiring

(1/2)

Package	Pins	μPD65943	μPD65944	μPD65945	μPD65946	μPD65948
Plastic QFP (fine-pitch)	100	✓	✓	✓	✓	✓
	120	–	–	–	✓	–
	144	✓	✓	✓	✓	✓
	160	✓	✓	✓	✓	✓
	176	–	✓	✓		
	208	–	–	✓	✓	✓
	240	–	–	–	✓	✓
	304	–	–	–	–	✓
Plastic QFP (fine-pitch)[Note]	160	–	–	–	–	–
	208	–	–	–	–	–
Plastic TQFP	48		–	–	–	–
	64		–	–	–	–
	80	✓				–
	100	✓	–	–	–	✓
	120		–	–	✓	
Plastic LQFP	144	–	–	–	–	✓
Plastic BGA	225	–	–	–		
	256	–	–	–	–	✓
	272	–	–	–	–	
	313	–	–	–	–	–
	352	–	–	–	–	–
Plastic FBGA	108					
	144					
	160					
	176	–	✓	✓		
	208	–	–	–	–	–
	240	–	–	–	–	–
	304	–	–	–	–	–
Plastic BGA (advanced)	672	–	–	–	–	–
Tape BGA[Note]	256	–	–	–	✓	✓
	352	–	–	–	–	–
	420	–	–	–	–	–
	500	–	–	–	–	–
	576	–	–	–	–	–
	696	–	–	–	–	–

Note With heat spreader

Remark ✓: Supported, – : Not supported, Blank : Under consideration

List of Packages

3-layer wiring

(2/2)

Package	Pins	μPD65949	μPD65951	μPD65954	μPD65956	μPD65958
Plastic QFP (fine-pitch)	100	✓	✓	✓	–	–
	120	–	–	–	–	–
	144	✓	✓	–	–	–
	160	✓	✓	✓	✓	–
	176					–
	208	✓	✓	✓	✓	✓
	240	✓	✓	✓	✓	✓
	304	–	✓	✓	✓	✓
Plastic QFP (fine-pitch) Note	160					
	208					
Plastic TQFP	48	–	–	–	–	–
	64	–	–	–	–	–
	80	–	–	–	–	–
	100	✓	–	–	–	–
	120		–	–	–	–
Plastic LQFP	144		–	–	–	–
Plastic BGA	225					–
	256	✓	✓			–
	272	✓	✓		–	–
	313	✓	✓			
	352	✓	✓			✓
Plastic FBGA	108	–	–	–	–	–
	144			–	–	–
	160			–	–	–
	176					–
	208	✓				–
	240	–				
	304	–	–	–		
Plastic BGA (advanced)	672	–	–	–	–	✓
Tape BGA Note	256	✓	✓		–	–
	352	✓	✓	✓	✓	–
	420	–	✓	✓	✓	✓
	500	–	–	✓	✓	✓
	576	–	–	–	✓	✓
	696	–	–	–	–	✓

Note With heat spreader

Remark ✓: Supported, – : Not supported, Blank : Under consideration

List of Packages

4-layer wiring

(1/2)

Package	Pins	μPD65961	μPD65964	μPD65966	μPD65968	μPD65969
Plastic QFP (fine-pitch)[Note]	160	–	–	–	–	–
	208					
Tape BGA[Note]	256	–	–	–	–	–
	352					–
	420					
	500	–				
	576	–	–			
	696	–	–			
Plastic BGA (advanced)	672	–	–	–		

Note With heat spreader
Remark – : Not supported, Blank : Under consideration

4-layer wiring

(2/2)

Package	Pins	μPD65970	μPD65971
Plastic QFP (fine-pitch)[Note]	160	–	–
	208		
Tape BGA[Note]	256	–	–
	352		
	420		
	500		
	576		
	696		
Plastic BGA (advanced)	672		

Note With heat spreader
Remark – : Not supported, Blank : Under consideration

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}		–0.5 to +4.6	V
Input voltage				
LVTTL interface buffer	V_I	$V_I < V_{DD} + 0.5$ V	–0.5 to +4.6	V
LVTTL interface buffer with fail safe function	V_I	$V_I < V_{DD} + 0.5$ V	–0.5 to +4.6	V
TTL 5-V withstand voltage interface buffer	V_I	$V_I < V_{DD} + 3.0$ V	–0.5 to +6.6	V
Output voltage				
LVTTL output buffer	V_O	$V_O < V_{DD} + 0.5$ V	–0.5 to +4.6	V
TTL 5-V output buffer	V_O	$V_O < V_{DD} + 3.0$ V	–0.5 to +6.6	V
5-V output buffer for CMOS	V_O	$V_O < V_{DD} + 3.0$ V	–0.5 to +6.6	V
Input/output voltage	V_I/V_O	Normal I/O pin	–0.5 to V_{DD} + 0.5	V
Output current[Note]	I_O	I_{OL} = 1 mA (FV0A)	3	mA
		I_{OL} = 2 mA (FV0B)	7	mA
		I_{OL} = 3 mA (FO09)	10	mA
		I_{OL} = 6 mA (FO04)	20	mA
		I_{OL} = 9 mA (FO01)	30	mA
		I_{OL} = 12 mA (FO02)	40	mA
		I_{OL} = 18 mA (FO03)	60	mA
		I_{OL} = 24 mA (FO06)	75	mA
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Note Output current: Indicates the maximum value of the current that is allowed to flow directly through this output pin.

Remark With the exception of the buffer with fail safe function, be sure to input voltage to the I/O pins only after the supply voltage has been fixed.

Recommended Operating Range

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	LVTTL interface	3.00	3.30	3.60	V
High-level input voltage	V_{IH}		2.0		V_{DD}	V
Low-level input voltage	V_{IL}		0		0.8	V
Positive trigger voltage	V_P		1.4		2.4	V
Negative trigger voltage	V_N		0.8		1.6	V
Hysteresis voltage	V_H		0.3		1.5	V
High-level input voltage	V_{IH}	TTL 5-V withstand voltage	2.0		5.5	V
Low-level input voltage	V_{IL}	interface	0		0.8	V
Positive trigger voltage	V_P		1.4		2.4	V
Negative trigger voltage	V_N		0.8		1.6	V
Hysteresis voltage	V_H		0.3		1.5	V
Input rise time	t_{ri}	Normal input	0		200	ns
Input fall time	t_{fi}		0		200	ns
Input rise time	t_{ri}	Schmitt input	0		10	ms
Input fall time	t_{fi}		0		10	ms

DC Characteristics (V_{DD} = 3.3 V ±0.3 V)

(1/3)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Static current consumption[Note 1]						
μPD65943, μPD65944, μPD65945, μPD65946, μPD65948, μPD65949,	I_{DDS}	$V_I = V_{DD}$ or GND		2.0	300	μA
μPD65951, μPD65954, μPD65956	I_{DDS}	$V_I = V_{DD}$ or GND		0	400	μA
μPD65958	I_{DDS}	$V_I = V_{DD}$ or GND		4.0	800	μA
Off-state output current[Note 2]						
LVTTL output	I_{OZ}	$V_O = V_{DD}$ or GND			±10	μA
TTL 5-V withstand voltage output	I_{OZ}	$V_O = V_{DD}$ or GND			±10	μA
5-V withstand voltage for CMOS	I_{OZ}	$V_O = V_{DD}$ or GND			±10	μA
Output current flow[Note 3] 5-V output for CMOS	I_R	V_{PU} = 5.5 V, R_{PU} =2 kΩ, V_O = 3.0 V			0.1	μA
Output short-circuit current[Note 4]	I_{OS}	V_O = GND			–250	mA
Input leakage current						
Normal input	I_I	$V_I = V_{DD}$ or GND			±1.0	μA
With pull-up resistor (50 kΩ)	I_I	V_I = GND	–28	–83	–190	μA
With pull-up resistor (5 kΩ)	I_I	V_I = GND	–280	–700	–1900	μA
With pull-down resistor (50 kΩ)	I_I	$V_I = V_{DD}$	28	83	190	μA
Pull-up resistor 50 kΩ	R_{PU}		18.9	39.8	107.1	kΩ
Pull-up resistor 5 kΩ	R_{PU}		1.9	4.7	10.7	kΩ
Pull-down resistor 50 kΩ	R_{PD}		18.9	39.8	107.1	kΩ

Notes 1. When using I/O blocks (etc.) with pull-up/pull-down resistors incorporated, the static current consumption increases.

2. Because there is a bias toward the 5-V protection circuit in the TTL 5-V withstand voltage and 5-V withstand voltage for CMOS 3-state or I/O buffers, the output-off state current increases slightly.

3. When the LSI supply current is pulled up to a higher voltage in the CMOS output buffer, a current that flows from the output pin to inside the LSI is generated.

4. The output short-circuit time is less than 1 second and for 1 LSI pin only.

Remarks 1. The + and – symbols attached to the current values in the table indicate the direction of the current. The symbol is + when the current is flowing into the device, and - when flowing out of the device.

2. Blanks in the table indicate that the values are undergoing evaluation.

DC Characteristics (V_{DD} = 3.3 V ±0.3 V)

(2/3)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low-level output current						
3 mA buffer (FO09)	I_{OL}	LVTTL output type	3.00			mA
6 mA buffer (FO04)	I_{OL}	V_{OL} = 0.4 V	6.00			mA
9 mA buffer (FO01)	I_{OL}		9.00			mA
12 mA buffer (FO02)	I_{OL}		12.00			mA
18 mA buffer (FO03)	I_{OL}		18.00			mA
24 mA buffer (FO06)	I_{OL}		24.00			mA
1 mA buffer (FV0A)	I_{OL}	TTL 5-V withstand voltage	1.00			mA
2 mA buffer (FV0B)	I_{OL}	output type	2.00			mA
3 mA buffer (FV09)	I_{OL}	V_{OL} = 0.4 V	3.00			mA
6 mA buffer (FV04)	I_{OL}		6.00			mA
9 mA buffer (FV01)	I_{OL}		9.00			mA
12 mA buffer (FV02)	I_{OL}		12.00			mA
18 mA buffer (FV03)	I_{OL}		18.00			mA
24 mA buffer (FV06)	I_{OL}		24.00			mA
3 mA buffer (FY09)	I_{OL}	5-V withstand voltage output	3.00			mA
6 mA buffer (FY04)	I_{OL}	for CMOS type	6.00			mA
9 mA buffer (FY01)	I_{OL}	V_{OL} = 0.4 V	9.00			mA
12 mA buffer (FY02)	I_{OL}		12.00			mA
18 mA buffer (FY03)	I_{OL}		18.00			mA
24 mA buffer (FY06)	I_{OL}		24.00			mA

DC Characteristics (V_{DD} = 3.3 V ±0.3 V)

(3/3)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-level output current						
3 mA buffer (FO09)	I_{OH}	LVTTL output type	–3.00			mA
6 mA buffer (FO04)	I_{OH}	V_{OH} = 2.4 V	–6.00			mA
9 mA buffer (FO01)	I_{OH}		–9.00			mA
12 mA buffer (FO02)	I_{OH}		–12.00			mA
18 mA buffer (FO03)	I_{OH}		–18.00			mA
24 mA buffer (FO06)	I_{OH}		–24.00			mA
1 mA buffer (FV0A)	I_{OH}	TTL 5-V withstand voltage	–1.00			mA
2 mA buffer (FV0B)	I_{OH}	output type	–1.00			mA
3 mA buffer (FV09)	I_{OH}	V_{OH} = 2.4 V	–3.00			mA
6 mA buffer (FV04)	I_{OH}		–3.00			mA
9 mA buffer (FV01)	I_{OH}		–3.00			mA
12 mA buffer (FV02)	I_{OH}		–3.00			mA
18 mA buffer (FV03)	I_{OH}		–6.00			mA
24 mA buffer (FV06)	I_{OH}		–6.00			mA
Low-level output voltage						
LVTTL output type	V_{OL}	I_{OL} = 0 mA			0.1	V
LVTTL output type (with 5 kΩ pull-up resistor)	V_{OL}	I_{OL} = 0 mA			0.2	V
TTL 5-V withstand voltage output type	V_{OL}	I_{OL} = 0 mA			0.1	V
5-V withstand voltage output for CMOS type	V_{OL}	I_{OL} = 0 mA			0.1	V
High-level output voltage						
LVTTL output type	V_{OH}	I_{OH} = 0 mA	V_{DD} – 0.1			V
TTL 5-V withstand voltage output type	V_{OH}	I_{OH} = 0 mA	V_{DD} – 0.2			V

AC Characteristics

The values in the table below refer to when the supply voltage of the internal gate array block is 3.3 V.

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Toggle frequency	f_{tog}	Internal toggle F/F (fanout = 2)		670			MHz
Propagation delay time	t_{PD}	Internal gates	Fanout = 1, wiring length 0 mm		94		ps
			Fanout = 1, standard wiring length		131		ps
			Standard load		108		ps
		Internal gates, power gates, 2NAND	Fanout = 1, standard wiring length		107		ps
			Standard load		94		ps
		Input buffers	Fanout = 1, standard wiring length		229		ps
			Standard load		222		ps
		Output buffer (FO01) C_L = 15 pF			1396		ps
Output rise time	t_r	Output buffer (FO01) C_L = 15 pF			2391		ps
Output fall time	t_f	Output buffer (FO01) C_L = 15 pF			1872		ps

Remark Standard load: Fanout = 2, wiring length 0 mm

TEST DESIGN

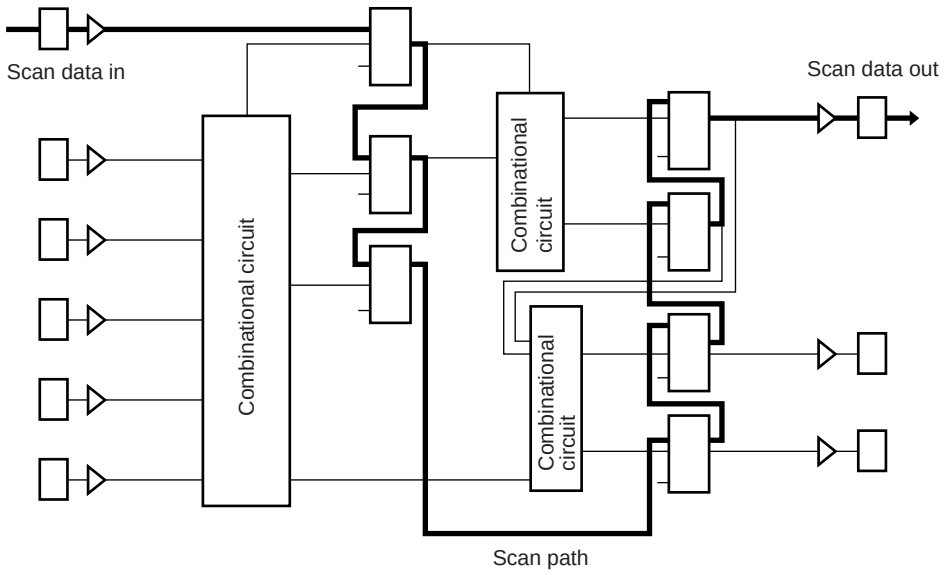
Scan Path Test

The scan path test is an effective technique in test simplification design. The ATG (Automatic Testpattern Generator) makes it possible to automatically generate a test pattern with high fault coverage.

The features of NEC's scan path test are outlined below.

- Automatic configuration of scan path
- Faults of asynchronous clock detectable
- Check tools for scan path design rule fully provided

Outline of Scan Path Test Method



DEVELOPMENT TOOLS

Easy interface with your EWS or PC

Users can choose the following tools to their environment.

Caution Some functions may not be supported. Make it sure before use.

OPENCAD™ V5.3 Configuration Tool

Function	NEC Tool	Interface Data	Commercially Available Tool Interface
Function simulator	–	• Net list PWC/EDIF (2.0.0)/ Verilog HDL	ModelSim™ Note 1/Verilog-XL™/VCS™
Schematic editor	Vdraw™ Note 1		–
Logic synthesis	–		Design Compiler™
Gate-level simulator Note 2	V. sim™ Note 1		ModelSim Note 1/Verilog-XL/VCS
Formal verifier	–		Formality™
STA Note 2	Tiara Note 1	• Test pattern ALBA/LOGPAT	PrimeTime™
Fault simulation Note 3	C. FGRADE™		–
Design for test	NEC_SCAN		Testgen™ Note 4
Floor planner Note 4	ace_floorplan galet_floorplan	• Delay data SDF	–
Layout and wiring Notes 3, 4	Galet	• Timing limit	Gate Ensemble™ Silicon Ensemble™

Notes 1. Tool supported in the Windows NT™ version
2. Sign-off tool
3. Tool not supported in the HP™ version
4. Individually supported tool

Remark Platform : SUN™ (Solaris™)/HP (HP-UX™)/PC-9800 series (Windows NT)/IBM PC/AT™ (Windows NT)
GUI : X11R5/Motif™ 1.2/Windows NT

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