Preliminary Specification

N E C
ELECTRON DEVICE

MOS INTEGRATED CIRCUITS

# μPD16300GF

41bit DC • PDP driver

The μPD16302 is a ROW driver utilized high Bi-CMOS process for DC plasma display panel. It consists of a 41bit bidirectional shift register and high voltage NPN Transistor.

It operates 5V (CMOS input level) and drives 150V and 500mA max. (Open collector output)

Features :

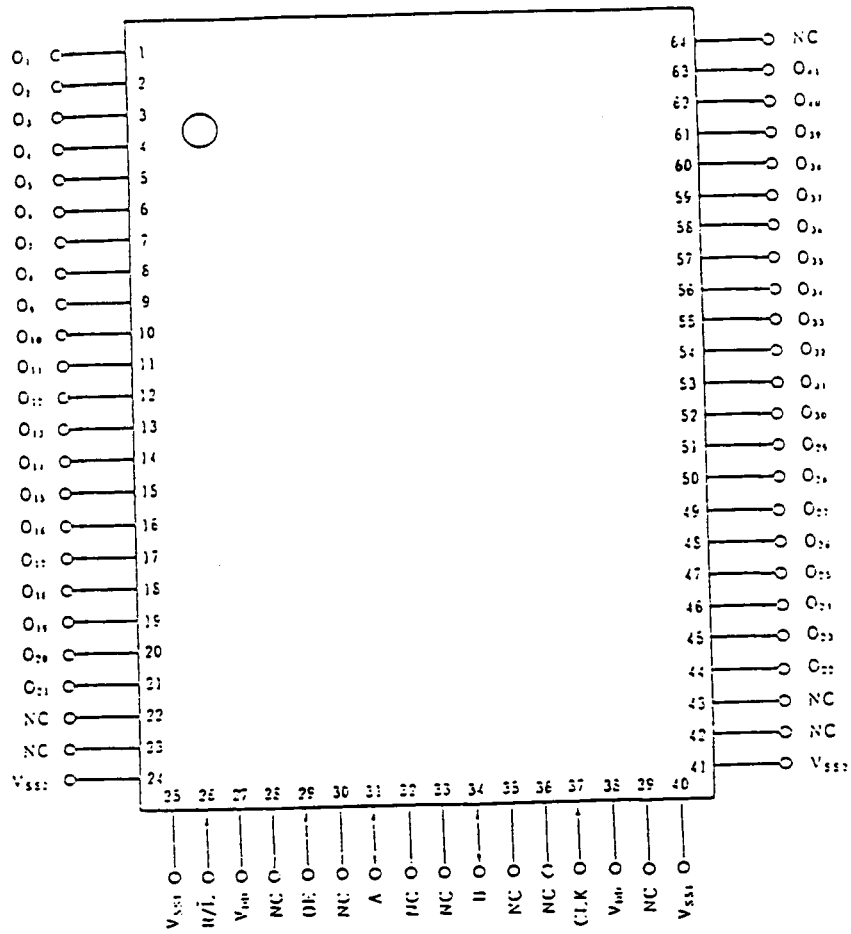
- High voltage Transistor + CMOS structure
- High voltage current output (150V, 500mA max.)
- Built-in 41bit bidirectional shift register
- Low power dissipation (1mA max., Ta = -40 ~ +85℃)
- Symmetry pin configuration by tridirectional lead quad flat package
  : 100 pin Plastic flat package
- Wide operating temperature (-40 ~ +85℃)

- ORDERING INFORMATION :

  μPD16300GF-3L9 : 80pin Plastic QFP (tri directional lead)

● PIN CONNECTION

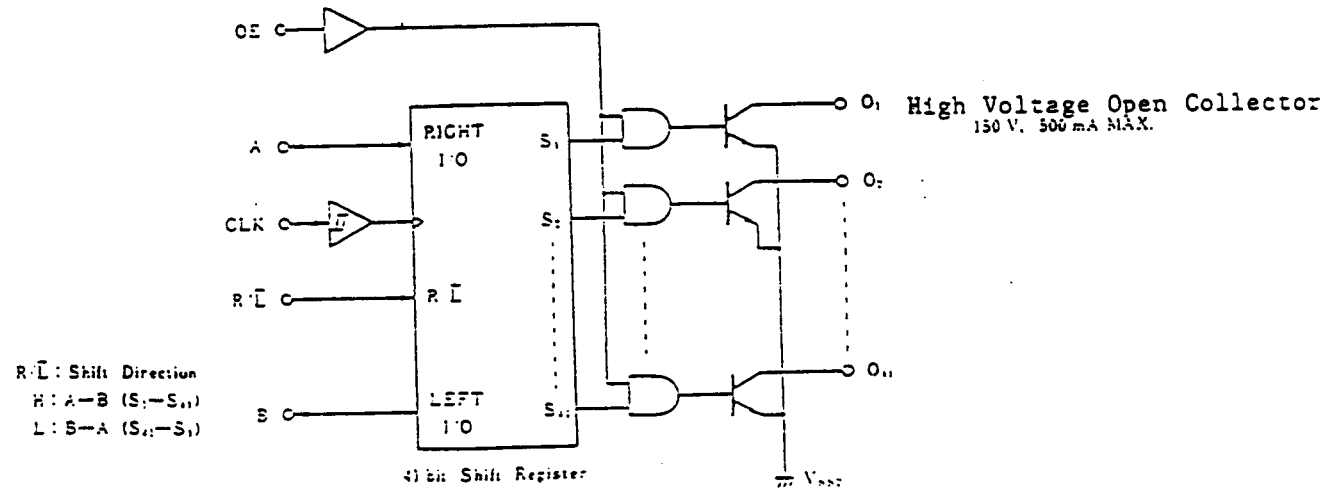
=== TOP VIEW ===




Please connect outside between the same power supply pins, such as VDDs and, Vss1 and Vss2.

Please open 33pin because of connecting lead frame.

=== Block Diagram ===



## Pin Configuration

| SYMBOL | Pin Name | Pin No. | Function |
|---|---|---|---|
| OE | Output Enable Input | 29 | H : O1-41 Data Output<br>L : O1-41 High Impedance |
| A | Right Date I/O | 31 | Serial Data input/output<br>R/L=H : A=IN, B=OUT<br>R/L=L : B=IN, A=OUT |
| B | Left Data I/O | 34 | |
| CLK | Shift Clock Input | 37 | Positive edge active |
| R/$\overline{L}$ | Shift Direction Control Input | 26 | H : Right shift mode<br>A→O1～O41→B<br>L : Left shift mode<br>B→O41～O1→A |
| O1 ～O41 | High Voltage Output | 1-21, 44-63 | 150V 500mA max. |
| VDD | Logic Power Supply | 27, 38 | 5V± 10% |
| VSS1 | Ground (Logic) | 25, 40 | —— |
| VSS2 | Ground (Driver) | 24, 41 | —— |
| NC | No Connection | 22, 23, 28, 30, 32, 33, 35, 36, 39, 42, 43, 64 | No connection<br>Please open 33 pin. |

Truth Table 1 (Shift Register)

| R/L | CLK | A | B | SHIFT REGISTER |
|---|---|---|---|---|
| H | ↑ | S1 input | S40 output ×1 | Data shift (to Right) |
| H | H OR L | | S41 output | No change |
| L | ↑ | S2 output ×2 | S41 input | Data shift (to Left) |
| L | H OR L | S1 output | | No change |

×1 ····· When CLK is positive edge active, S40 shifts to S41 and appears to be B.

×2 ····· When CLK is positive edge active, S2 shifts to S1 and appears to be A.

Truth Table 2 (Driver)

| DATA | OE | O1-41 |
|---|---|---|
| × | L | Z (all off) |
| L | H | Z |
| H | H | L |

H = High level, L = Low level, × = H or L

Z = High Impedance (Driver off)

DATA = Contents of Shift Register

## Absolute Maximum Ratings
(Ta=25℃, Vss = 0V)

| ITEMS | SYMBOL | RATINGS | UNIT |
|---|---|---|---|
| Logic Power Supply | VDD | -0.5～+7.0 | V |
| Input Voltage | VI | -0.5～VDD+0.5 | V |
| Logic Output Voltage | VO1 | -0.5～VDD1+0.5 | V |
| Driver Output Voltage | VO2 | -0.5～150 | V |
| Driver Maximum current | IO2 | 500 ※1 | mA |
| Power Dissipation/Package | PD | 1000 | mW |
| Operating Temperature | Topt | -40～+85 | ℃ |
| Storage Temperature | Tstg | -65～+150 | ℃ |

※1 ····· Duty ≦ 1/41

## Recommended Operating Conditions
(Ta = -40 ～ +85℃, Vss = 0V)

| ITEM | SYMBOL | MIN. | TYP. | MAX. | UNIT. |
|---|---|---|---|---|---|
| Logic Power Supply | VDD1 | 4.5 | 5 | 5.5 | V |
| High Level Input Voltage | VIH | 0.7 VDD | | VDD | V |
| Low Level Input Voltage | VIL | 0 | | 0.2 VDD | V |
| Driver Power Supply | VO2 | 30 | | 110 | V |
| Driver Output Current | IO2 | | | 300 | mA |

Electrical Characteristics
(Ta = 25℃, VDD = 4.5~5.5V, Vss = 0V)

| ITEM | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| High Level Output Voltage | VOH1 | Logic IOH1=-1mA | 0.9 VDD | | | V |
| Low Level Output Voltage | VOL1 | Logic IOL1=1mA | | | 0.1 VDD | V |
| Low Level Output Voltage | VOL2 | O1-41, IOL2=300mA | | 6 | 10 | V |
| Output leak current | ITL | VO2=110V, OE=Vss | | | 10 | μA |
| High level input current | II | VI=VDD or Vss | | | ±1 | μA |
| High Level Input Voltage | VIH | | 0.7 VDD | | | V |
| Low Level Input Voltage | VIL | | | | 0.2 VDD | V |
| Stand by Current | IDD | O1-41 1 output on Ta=-40 ~ +85℃ | | | 1.0 | mA |
| | | O1-41, 1 output on, Ta=25℃ | | | 100 | μA |

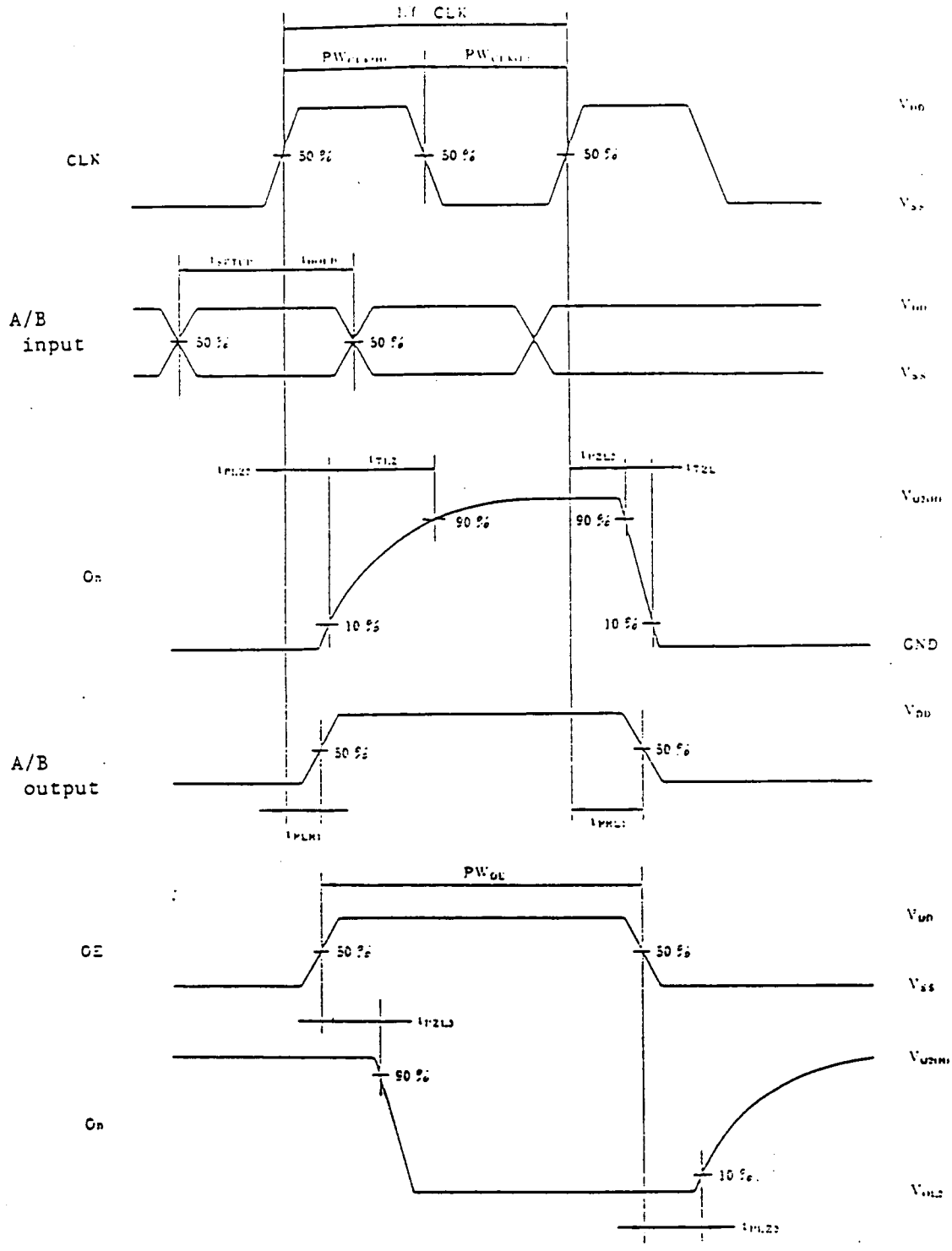
Switching Characteristics
(Ta = 25℃, VDD = 4.5 ~ 5.5V, VO2(H) = 110V
CL=150pF, RL=470Ω)

| ITEM | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Delay time | t PHL1 | CLK→A/B | | | 100 | ns |
| | t PLH1 | | | | 100 | ns |
| | t PZL2 | CLK→O1~O41 | | | 100 | ns |
| | t PLZ2 | | | | 1.0 | μs |
| | t PZL3 | OE→O1~O41 | | | 100 | ns |
| | t PLZ3 | | | | 1.0 | μs |
| Output Transient Time | t TLZ | O1-41 | | | 1.0 | μs |
| | t TZL | | | | 0.1 | μs |
| Maximum Clock Frequency | f MAX | Duty=50% | 10 | | | MHz |
| Input Capasitance | CI | | | | 10 | pF |

Timing Requirement Conditions
(Ta = -40 ~ +85℃, VDD1 = 4.5 ~ 5.5V)

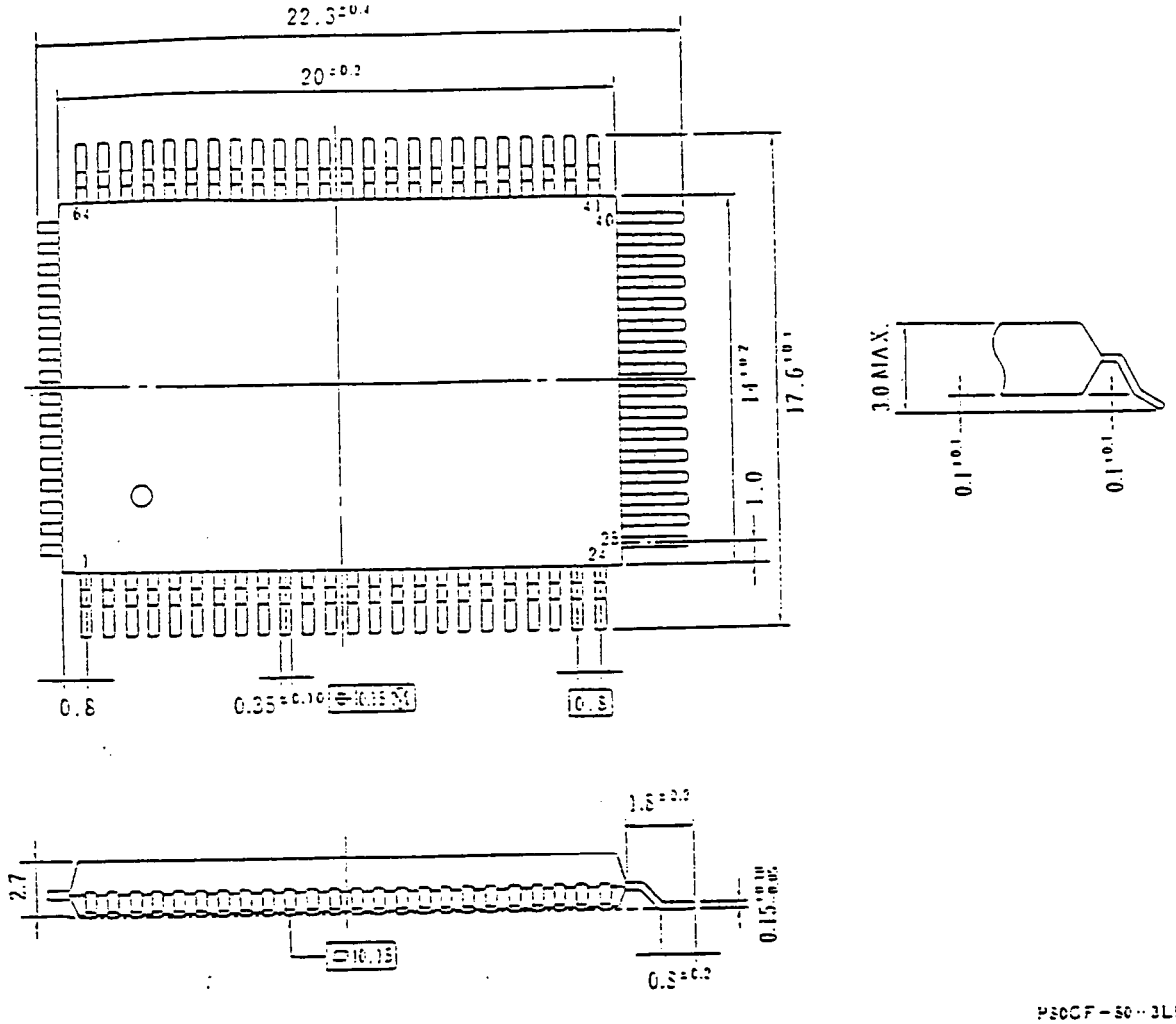
| ITEM | SYMBOL | CONDITION | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| Clock Pulse Width | PWCLK | | 50 | | | ns |
| Enable Pulse Width | PWOE | | 1.2 | | | μs |
| Data Setup Time | t SETUP | | 30 | | | ns |
| Data Hold Time | t HOLD | | 10 | | | ns |

=== AC characteristics wave chart ===



=== Outline ===

80pin plastic QFP (Tri directional Lead) unit:mm




P80GF-80-3L9