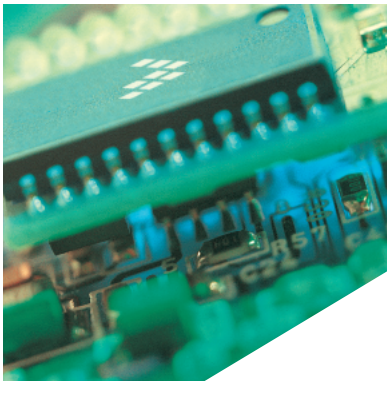
Freescale Semiconductor Data Book.

Advanced Clock Drivers.



DL207
Rev. 2
8/2004

Launched by Motorola
freescale semiconductor

Advanced Clock Drivers Device Data

Foreword

This publication includes technical information for the several product families that comprise Freescale Semiconductor Advanced Clock Drivers products. Freescale's broad portfolio of devices support voltage levels from 2.5 V to 5.0 V in both CMOS I/O and various differential I/O technologies. Advanced Clock Drivers are developed by the Freescale Semiconductor Timing Solutions Operations organization.

All devices are listed in alphanumeric order in the *Device Index* of this book. Just turn to the appropriate page for technical details of the known device.

A *Selector Guide* by product family is provided at the beginning of the book to aid you in identifying devices that meet your application and functional performance requirements.

Complete device specifications are provided in the form of *Data Sheets* which are categorized into the six product types: Clock Generators, QUICCClocks, Failover / Redundant Clocks, Clock Synthesizers, Zero-Delay Buffers, LVCMOS Fanout Buffers, and Differential Fanout Buffers.

Chapters on *Packaging Information* and *Application Notes* include additional information to aid you in the design process.

The information in this book has been carefully checked and is believed to be accurate; however, no responsibility is assumed for inaccuracies.

This document was revised in 2004 during the Motorola to Freescale Semiconductor, Inc. transition. References to Motorola still appear in this current revision. If this document is revised, all references to Motorola will be removed at that time.

Printed in U.S.A.

Freescale Semiconductor Technical Support and Literature

Worldwide Access:	Internet:	www.freescale.com
	E-mail:	support@freescale.com

Quick References:

Technical Support	www.freescale.com/support For Technical or Literature questions or comments you may select “Technical Support”, log in and use the “Service Request” feature.
Retrieve/Order Literature	You may directly access PDF files on the website, or use the shopping cart to request Postal delivery of our literature. To browse and order literature through the Literature Distribution Center, select “Order Literature” on the main “Documentation” page.

Telephone, Fax, and E-mail Contacts:

North and South America:	Phone:	+1-800-521-6274 or +1-480-768-2130	
	Fax:	+1-480-768-2131	
	E-mail:	support@freescale.com	
	For fastest response use the Worldwide Internet access listed above.		
Europe, Middle East, and Africa:	Phone:	+44 1296 380 456	(English)
		+46 8 52200080	(English)
		+49 89 92103 559	(German)
		+33 1 69 35 48 48	(French)
	Fax:	+49 89 92103 466	(German and English)
	E-mail:	support@freescale.com	
Asia/Pacific:*	Phone:	+800 2666 8080*	(Toll Free within Asia/Pacific)
		+000 800 852 1155	(Toll Free within India)
	Fax:	+852 2661 7736	(Chinese and English)
	E-mail:	support.asia@freescale.com	
Japan:	Phone:	0120 191 014	(Toll Free: Domestic only)
	Fax:	0120 191 060	(Toll Free: Domestic only)
	E-mail:	support.japan@freescale.com	
	Internet:	www.freescale.co.jp	

*Countries covered within Asia/Pacific are: China, Taiwan, South Korea, Macau, Malaysia, Singapore, Thailand, Australia and New Zealand.

To get Pricing and Delivery for a product:

Budgetary pricing is available for most products on the Freescale web site; however, to obtain pricing and delivery quotes, contact your local authorized distributor or Freescale sales representative. To find your local distributor, visit **www.freescale.com**, select “Where to Buy” on the Freescale Home Page.

Freescale Semiconductor's Technical Information Center:

The Freescale Semiconductor Technical Information Center (TIC) is a worldwide service organization that provides our customers and distributors with the following services:

- Access to technical information and literature
- Answers to questions on Freescale Semiconductor products
- Assistance in locating Technical Training on Freescale Semiconductor's microprocessors, embedded processors, and microcontroller products.

Technical Information and Literature:

To complement Freescale Semiconductor's broad line of products, we offer a complete library of technical literature. Data books detail the electrical characteristics of our products. User's manuals describe the capabilities of our products in circuit and system design. Visit our *Products* Library and *Documentation* Library at **www.freescale.com**. From the Home Page you can select "Products" and then the desired Product Family or "Support" and then "Documentation" from the menu. From the *Products* Library, our customers can quickly browse device-specific information in our Product Catalog.

From the *Documentation* Library, our customers can perform the following functions:

- Download files found in the online catalog or through the online search
- Order data sheets, data books, user's manuals, selector guides, stocked CDs, and any other inventory item in print or on a CD-ROM
- Select literature files and create a fully customized CD-ROM through our CD-ON-DEMAND process.

The literature service is free-of-charge. However, literature and CD quantities are limited. If you need larger quantities (for example, for a special promotion), contact your local authorized distributor, Freescale sales representative, or use the contact information listed on the previous page.

Technical Questions and Support:

We strive to provide you the information you need. Our Web sites are designed to provide detailed information on our current devices and system solutions. The support pages offer device errata, technical training course information, and answers to frequently asked questions. To submit a written technical request, visit **www.freescale.com**. Select "Support", then "Technical Support" from the menu. Written technical requests help eliminate misunderstandings and shorten answer response intervals.

Requests generated from this Internet interface are automatically fed into a worldwide customer database as a technical service request. You immediately receive a service request reference number. This reference number enables you to view the request status, deliver additional information directly to our specialists, and cancel or re-open a request by using the Internet interface.

This customer database enables us to direct your service request to the appropriate person and track the response time. Through our worldwide network, one of our Freescale specialists can immediately start working on your service request. We are located in the Americas, Europe, Middle East, Africa, Asia/Pacific, and Japan. Our goal is to answer your request within two days. In most cases, our customers receive an overnight response. We have developed a system to respond to you, the customer, in the most efficient and timely manner possible.

Technical Training on Freescale Semiconductor products:

We can assist you in locating Web-based training on our web site, or instructor-lead processor training courses in your region. These training courses enable design engineers to quickly gain product knowledge; getting designs to market faster. Through our Training Partners in-plant courses are available where instructors come to your premises or a convenient location, to present the training to your design engineers. Alternatively, in cases where course attendance is too small to justify a training course of its own, general training courses are available through our Training Partners. These courses accommodate a single or small number of engineers that can join in with those of other companies.

To see available Technical Training for Freescale Semiconductor products:

Visit **www.freescale.com**, select "Design Support" from the menu, and then select "Training".

ATTENTION: Freescale Semiconductor Advanced Clock Driver Customers

The Timing Solutions Operation of Freescale Semiconductor is currently undergoing a technology update on several of the Advanced Clock Driver devices. This technology update moves the current product to a newer process technology. This semiconductor technology update results in an introduction of a pin and functional equivalent device, which will provide superior electrical performance.

The following tables list the devices that are involved in this technology update. These lists also contain the replacement device part number.

Please consult the selector guide and associated device data sheets for the details of these devices. If additional product information is desired please contact your local Freescale Semiconductor representative.

Clock Generators

Old Device	Replaced by
MPC930	MPC9330
MPC931	MPC9331
MPC950	MPC9350
MPC951	MPC93R51
MPC952	MPC93R52
MPC972	MPC9772
MPC973	MPC9773
MPC974	MPC9774
MPC992	MPC9992
MPC993	MPC9993
MPC9952	MPC9352

Clock Synthesizers

Old Device	Replaced by
MC12429	MPC9229 or MPC92429
MC12430	MPC9230 or MPC92430
MC12439	MPC9239 or MPC92439

Zero-Delay Buffers

Old Device	Replaced by
MPC953	MPC9653A
MPC958	MPC9658

LVCMOS Fanout Buffers

Old Device	Replaced by
MPC946	MPC9446
MPC947	MPC9447
MPC948	MPC9448
MPC949	MPC9449

Differential Fanout Buffers

Old Device	Replaced by
MC100EP111	MC100ES6111
MC100EP210	MC100ES6210
MC100EP220	MC100ES6220
MC100EP221	MC100ES6221
MC100EP222	MC100ES6222

Advanced Clock Drivers Device Data

Table of Contents

Device Index

Chapter One
Advanced Clock Drivers Selector Guide

Freescale Semiconductor provides a one stop shop for your high performance clocking needs. Our broad portfolio of devices support voltage levels from 2.5 V to 5.0 V in both CMOS I/O and various differential I/O technologies. With one of the widest selection of products in the industry, Freescale Semiconductor should be your first stop when you need to design a high performance clock tree.

Advanced Clock Drivers are developed by the Freescale Semiconductor Timing Solutions Operations organization.

To Replace Devices in an Existing Design

Call your local Freescale Semiconductor Sales Office or Distributor to determine the closest replacement device.

Applications Assistance

Applications assistance is available from your nearest Freescale Semiconductor Sales office.

Access Advanced Clock Drivers Technical Information On-Line

Freescale Semiconductor has provided a World Wide Web Server to deliver it's technical data to the global Internet community. Technical data (such as data sheets, application notes, and selector guides) are available on the Internet server with full, easy text search capabilities. Ordering literature from the Literature Center is available on-line. Other features of Freescale Semiconductor's Internet server include the availability of a searchable press release database, technical training information with on-line registration capabilities, an on-line technical support form to send technical questions and receive answers through e-mail, information on product groups, full search capabilities of device models, a listing of authorized distributors, and links directly to other Freescale Semiconductor World Wide Web servers.

To access Freescale Timing Solutions Operations information, use one of the following URLs:

www.freescale.com/Clocks
www.freescale.com/AdvancedClockDrivers
www.freescale.com/TimingSolutions

Clock Generator Reference Table

Introduction

This classification of product uses PLL technology to generate output clocks that are synchronous, and in most cases phase aligned, to an input reference clock. Limited frequency synthesis and zero delay performance is provided.

Device	Processor and Application	Temp. Range (°C) (T_A)	V_{CC} (V)	Package	Output Frequency Range (MHz)	Max Output Skew (ps)	Max Period Jitter (ps)	Input	No. of Outputs	Status
MPC9315	Telecom/Networking Applications	-40 to 85	3.3/ 2.5	32 LQFP	18 to 160	120	8 (rms)	2 selectable LVCMOS	8 LVCMOS	P
MPC9330	Pentium or PowerPC603/740/750 Class Processor Designs (on-board crystal oscillator)	0 to 70	3.3	32 LQFP	16 to 200	150	250	XTAL LVCMOS	6 LVCMOS	P
MPC9331	Pentium or PowerPC603/740/750 Class Processor Designs (faster VCO than 930)	0 to 70	3.3	32 LQFP	16 to 200	150	125	LVCMOS LVPECL	6 LVCMOS	P
MPC9350	Networking and Telecommunications Ideal for PowerQUICC II and PowerPC MPC74XX applications	-40 to 85	3.3/ 2.5	32 LQFP	25 to 200	200	—	XTAL LVCMOS	9 LVCMOS	P
MPC9351	Networking and Telecommunications Ideal for PowerQUICC II and PowerPC MPC74XX applications	-40 to 85	3.3/ 2.5	32 LQFP	25 to 200	100	—	LVCMOS LVPECL	9 LVCMOS	P
MPC9352	General Purpose or RISC/CSIC Class Processor Designs	-40 to 85	3.3/ 2.5	32 LQFP	16 to 200	150	200	LVCMOS	11 LVCMOS	P
MPC93H51	High output drive version of MPC93R51	0 to 70	3.3	32 LQFP	240	150	15 (rms)	LVCMOS LVPECL	9 LVCMOS	P
MPC93R51	Networking and Telecommunications Ideal for PowerQUICC II and PowerPC MPC74XX applications	0 to 70	3.3	32 LQFP	240	150	15 (rms)	LVCMOS LVPECL	9 LVCMOS	P
MPC93H52	High output drive version of MPC93R52	0 to 70	3.3	32 LQFP	240	200	—	LVCMOS	11 LVCMOS	P
MPC93R52	General Purpose or RISC/CSIC Class Processor Designs	0 to 70	3.3	32 LQFP	240	200	—	LVCMOS	11 LVCMOS	P
MPC9600	General purpose 2.5 V, high fanout zero delay buffer	-40 to 85	3.3/ 2.5	48 LQFP	25 to 200	150	50	LVCMOS LVPECL	21 LVCMOS	P
MPC9772	General Purpose or RISC/CSIC Class Designs (independent output enable/disable “lo-power” scheme)	0 to 70	3.3	52 LQFP	25 to 240	300	150	XTAL LVCMOS	12 LVCMOS	P
MPC9773	Pentium or PowerPC603/740/750 Class Designs (output enable/disable “lo-power” scheme)	0 to 70	3.3	52 LQFP	25 to 240	300	150	LVCMOS LVPECL	12 LVCMOS	P
MPC97H73	High output drive version of MPC9773	0 to 70	3.3	52 LQFP	25 to 240	300	150	LVCMOS LVPECL	12 LVCMOS	P
MPC9774	Fault Tolerant (redundant Clock Source needed) Pentium/PowerPC603/740/750/RISC Class Processor Design	0 to 70	3.3	52 LQFP	25 to 125	300	90	LVCMOS	15 LVCMOS	P
MPC97H74	High output drive version of MPC9774	0 to 70	3.3	52 LQFP	25 to 125	300	90	LVCMOS	15 LVCMOS	P
MPC9992	Pentium or PowerPC603/740/750 Class Designs (output enable/disable “lo-power” scheme)	-40 to 85	3.3/ 2.5	32 LQFP	20 to 400	150	TBD	LVPECL XTAL	7 Differential Pairs	S

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

Clock Generator Reference Table (continued)

Device	Processor and Application	Temp. Range (°C) (T_A)	V_{CC} (V)	Package	Output Frequency Range (MHz)	Max Output Skew (ps)	Max Period Jitter (ps)	Input	No. of Outputs	Status
MC88915FN55	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	0 to 70	5.0	28 PLCC	5 to 55	500	—	CMOS	8 LVCMOS	P
MC88915FN70	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	0 to 70	5.0	28 PLCC	5 to 70	500	—	CMOS	8 LVCMOS	P
MC88915TFN55	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	-40 to 85	5.0	28 PLCC	55	500	—	CMOS	8 LVCMOS	P
MC88915TFN70	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	-40 to 85	5.0	28 PLCC	5 to 70	500	—	CMOS	8 LVCMOS	P
MC88915TFN100	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	-40 to 85	5.0	28 PLCC	5 to 100	500	—	CMOS	8 LVCMOS	P
MC88915TFN133	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	-40 to 85	5.0	28 PLCC	5 to 133	500	—	CMOS	8 LVCMOS	P
MC88915TFN160	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	0 to 70	5.0	28 PLCC	5 to 160	500	—	CMOS	8 LVCMOS	P
MC88LV915TFN	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	0 to 70	3.3	28 PLCC	5 to 100	500	—	CMOS	8 LVCMOS	P
MC88LV926DW	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	0 to 70	3.3	20 SOIC 300 Mil	5 to 133	500	—	CMOS	6 LVCMOS	P
MC88916DW70/80	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	-40 to 85	5.0	20 SOIC 300 Mil	5 to 80	500	—	CMOS	6 LVCMOS	P
MC88920DW	PC Work Station, Servers, Memory Modules, Graphics Cards, High End Printers, Networking, and Telecom	-40 to 85	5.0	20 SOIC 300 Mil	5 to 50	500	—	CMOS	6 LVCMOS	P

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

QUICCClock Reference Table

Introduction

This classification of products is specifically designed to meet the clock requirements for the PowerPC and PowerQUICC microprocessors and microcontrollers. Although designed for PowerPC processors these devices also provide the widely used clock frequencies for most microprocessor families.

Device	Processor and Application	Temp. Range (°C)	V_{CC} (V)	Package	Output Frequencies	Input	No. of Outputs	Status
MPC9817	Low-cost PowerPC ISA and PowerQUICC designs	-40 to 85	3.3	20 SSOP	25, 33, 50, 66	Crystal or LVCMOS	5 + 3 reference outputs	S
MPC9850	PowerQUICC 3 w/Rapid I/O	-40 to 85	3.3 Core 3.3 or 2.5 I/O	100 MAPBGA	16, 25, 33, 50, 83, 100, 125, 133,166	Crystal LVCMOS LVPECL	8-LVCMOS 2-Rapid I/O 1 @ 25 MHz ref	S
MPC9855	PowerPC, PowerQUICC 2 and PowerQUICC 3 w/o Rapid I/O	-40 to 85	3.3 Core 3.3 or 2.5 I/O	100 MAPBGA	16, 25, 33, 50, 83, 100, 125, 133,166	Crystal LVCMOS LVPECL	8-LVCMOS 2 @ 25 MHz ref	S

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

Failover or Redundant Clock Reference Table

Introduction

Redundant or Failover Clock Applications are required for high reliability telecommunications, networking and other applications where the loss of a clock source would cause system failure. Clock sources for these applications may be generated by master system clocks and distributed over a backplane to various modules in a pc board, chassis or electronics cabinet.

Device	Processor and Application	Temp. Range (°C) (T_A)	V_{CC} (V)	Package	Output Frequency Range (MHz)	Max Output Skew (ps)	Max Period Jitter (ps)	Input	No. of Outputs	Status
MPC9892	Systems with clock redundancy needs (high-end computing and telecomm) Differential LVPECL 50 MHz to 90 MHz input frequency	-40 to 85	3.3	32 LQFP	50 to 180	150	TBD	LVPECL	5 Differential Pairs	S
MPC9893	Systems with clock redundancy needs (high-end computing and telecomm), FAILOVER Clock	-40 to 85	3.3/ 2.5	48 LQFP	25 to 200	TBD	TBD	LVCMOS	12 LVCMOS	P
MPC9894	Four (4) input redundant clock with I^2C configuration interface	-40 to 105 (T_J)	3.3/ 2.5	100 PBGA	21.25 to 340	TBD	TBD	LVPECL	8 LVPECL	S
MPC9895	Systems with clock redundancy needs (high-end computing and telecomm), FAILOVER Clock with restore function	-40 to 85	3.3	100 PBGA	25 to 200	TBD	TBD	LVCMOS	12 LVCMOS	S
MPC9993	Systems with clock redundancy needs (high-end computing and telecomm) Differential LVPECL 50 MHz to 90 MHz input frequency	-40 to 85	3.3	32 LQFP	50 to 200	150	TBD	LVPECL	5 Differential Pairs	P
MPC99J93	Systems with clock redundancy needs (high-end computing and telecomm) Differential LVPECL 50 MHz to 90 MHz input frequency	-40 to 85	3.3	32 LQFP	50 to 180	150	TBD	LVPECL	5 Differential Pairs	P

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

Clock Synthesizer Reference Table

Introduction

This classification of products uses PLL technology to synthesize high frequency clocks from low cost crystal sources. Programmable frequency steps are typically 1 MHz or less with output frequencies as high as 800 MHz.

Device	Processor and Application	Temp. Range (°C) (T_A)	V_{CC} (V)	Package	Output Frequency Range (MHz)	Max Period Jitter (ps)	Input	Outputs	Status
MPC9229	Clock source for 25 MHz to 450 MHz processor designs (serial and/or parallel) 1 MHz steps	0 to 70	3.3	28 PLCC 32 LQFP	400	25	XTAL	LVPECL	P
MPC9230	Clock source for 50 MHz to 900 MHz processor designs (serial and/or parallel) 1 MHz steps	0 to 70	3.3	28 PLCC 32 LQFP	800	25	XTAL LVCMOS	LVPECL	P
MPC9239	Clock source for 50 MHz to 900 MHz processor designs (serial and/or parallel) 16.66 MHz steps	0 to 70	3.3	28 PLCC 32 LQFP	900	25	XTAL LVCMOS	LVPECL	P
MPC9259	Clock source for 50 MHz to 900 MHz processor designs (serial or parallel) 16.66 MHz steps	0 to 70	3.3	32 LQFP	900	25	XTAL LVCMOS	LVDS	S
MPC92429	Clock source for 25 MHz to 450 MHz processor designs (serial and/or parallel) 1 MHz steps	0 to 70	3.3	28 PLCC 32 LQFP	400	25	XTAL	LVPECL	S
MPC92430	Clock source for 50 MHz to 900 MHz processor designs (serial and/or parallel) 1 MHz steps	0 to 70	3.3	28 PLCC 32 LQFP	800	25	XTAL LVCMOS	LVPECL	S
MPC92432	Mid-range to high performance telecom, networking, and computing applications	-40 to 85	3.3	48 LQFP	21.25 to 1360	TBD	Crystal LVCMOS	2 LVPECL	S
MPC92439	Clock source for 50 MHz to 900 MHz processor designs (serial and/or parallel) 16.66 MHz steps	0 to 70	3.3	28 PLCC 32 LQFP	900	25	XTAL LVCMOS	LVPECL	IN
MPC926508	Clock synthesizer for networking applications (Pin compatible with ICS650-08)	-40 to 85	3.3	20 TSSOP	100 to 133	—	XTAL LVCMOS	LVCMOS	P

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

Zero-Delay Buffer Reference Table

Introduction

This classification of products uses PLL technology to reproduce exact copies, in frequency and phase, of the input reference clock. These specialized products provide superior AC performance to clock generators, but lack any frequency synthesis capabilities.

Device	Processor and Application	Temp. Range (°C) (T_A)	V_{CC} (V)	Package	Output Frequency Range (MHz)	Max Output Skew (ps)	Max Period Jitter (ps)	Input	Outputs	Status
MPC9608	General Purpose Zero-delay applications, Companion to PowerQUICK and PPC designs, DRAM applications	-40 to 85	3.3	32 LQFP	12.5 to 200	150	150	LVCMOS	10 LVCMOS	P
MPC961C	General Purpose also PowerQUICC: Zero-delay applications (CMOS clock signal retiming without insertion delay) DRAM driver	-40 to 85	3.3/ 2.5	32 LQFP	50 to 200	150	10 (RMS)	LVCMOS Ref LVCMOS fdbk	17 + feed-back LVCMOS	P
MPC961P	Zero-delay applications (PECL clock signal retiming without insertion delay)	-40 to 85	3.3/ 2.5	32 LQFP	50 to 200	150	10 (RMS)	LVPECL Ref LVCMOS fdbk	17 + feed-back LVCMOS	P
MPC962304	General Purpose Zero-delay applications (Pin compatible with CY2304)	0 to 70 or -40 to 85	3.3	8 SOIC	133	200		LVCMOS	4 + feed-back LVCMOS	IN
MPC962305	General Purpose Zero-Delay applications. (Pin compatible with CY2305/CY23S05)	0 to 70 or -40 to 85	3.3	8 SOIC 8 TSSOP 16 SOIC 16 TSSOP	133	250	200	LVCMOS	4 + feed-back LVCMOS	S
MPC962308	General Purpose Zero-delay applications. (Pin compatible with CY2308/CY23S08)	0 to 70 or -40 to 85	3.3	16 SOIC 16 TSSOP	133	200	200	LVCMOS	8 LVCMOS	S
MPC962309	General Purpose Zero-delay applications. (Pin compatible with CY2309/CY23S09)	0 to 70 or -40 to 85	3.3	8 SOIC 8 TSSOP 16 SOIC 16 TSSOP	133	250	200	LVCMOS	8 + feed-back LVCMOS	S
MPC9653A	High Performance Clock Tree Design, PC100SDRAM	0 to 70	3.3	32 LQFP	125	150	100	LVPECL Ref LVCMOS fdbk	8 + feed-back LVCMOS	P
MPC9658	Very High Performance Clock Tree Design up to 200 MHz, PC100SDRAM	0 to 70	3.3	32 LQFP	250	120	80	LVPECL Ref LVCMOS fdbk	10 + feed-back LVCMOS	P
MPC96877	DDR2 zero-delay application	0 to 70	1.8	52 VFBGA 40 MLF	125 to 270	TBD	40	SSTL-18	10 SSTL-18	S

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

LVCMOS Fanout Buffer Reference Table

Introduction

This classification of product uses digital circuitry to produce multiple copies of its input clock. In some cases the output frequencies will be divided down versions of the input clock.

Device	Processor and Application	Temp. Range (°C) (T_A)	V_{CC} (V)	Package	Max Output Frequency (MHz)	Max Output Skew (ps)	Max Part-Part Skew (ns)	Input	Outputs	Status
MPC905	Pentium PCI Processor Bus Clock or PCI Bus Hi-Speed Transmission Line Driver	0 to 70	3.3	16 SOIC	100	500	—	XTAL external LVCMOS	6	P
MPC940L	General Purpose or RISC/CSIC PCI Clock Distribution to Synchronous Memory (better performance than MPC9109)	0 to 70	3.3/ 2.5	32 QFP/LQFP	250	150	1.7	LVPECL LVCMOS	18	P
MPC941	General Purpose or RISC/CSIC PCI Clock Distribution to Synchronous Memory (more outputs than MPC940)	-40 to 85	3.3/ 2.5	48 QFP	250	250	1.2	LVPECL LVCMOS	27	P
MPC942C	Pentium II and other high performance synchronous designs (CMOS inputs)	0 to 70	3.3/ 2.5	32 LQFP	250	250	1	LVTTL LVCMOS	18	P
MPC942P	Pentium II and other high performance synchronous designs (PECL inputs)	0 to 70	3.3/ 2.5	32 LQFP	250	250	1	LVPECL	18	P
MPC9109	General Purpose or RISC/CSIC PCI Clock Distribution to Synchronous Memory	0 to 70	3.3/ 2.5	32 QFP/LQFP	250	150	1.7	LVPECL LVCMOS	18	P
MPC9443	Low Voltage High-performance Telecom, Networking and computing Applications	-40 to 85	3.3/ 2.5 †	48 LQFP	250	200	—	LVPECL LVCMOS	16	P
MPC9446	Low Voltage Mid-range and High-performance Telecom, Networking and Computing Applications	-40 to 85	3.3/ 2.5 †	32 LQFP	250	200	—	LVCMOS	10	P
MPC9447	General Purpose or RISC/CSIC Class Processor Clock Fanout for L2 Cache	-40 to 85	3.3/ 2.5	32 LQFP	275	150	TBD	LVTTL	9	P
MPC9448	General Purpose or RISC/CSIC Class Processor Clock Fanout for L2 Cache (faster & more outputs than the MPC947)	-40 to 85	3.3/ 2.5	32 LQFP	275	150	TBD	LVPECL LVCMOS	12	P
MPC9449	General Purpose or RISC/CSIC Class Processor PCI Clock Distribution to Synch Memory (5 more outputs than the MPC946)	-40 to 85	3.3/ 2.5	52 LQFP	200	200	TBD	LVPECL LVCMOS	15	P
MPC94551	1:4 LVCMOS fanout buffer	-40 to 85	3.3	8 SOIC	160	250	TBD	LVCMOS	4	S
MPC9456	Low Voltage Mid-range and High-performance Telecom, Networking and Computing Applications	-40 to 85	3.3/ 2.5 †	32 LQFP	250	250	—-	LVPECL	10	P

† Supports single and mixed mode power supply

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

Differential Fanout Buffer Reference Table

Introduction

This classification of product uses digital circuitry to produce multiple copies of its input clock. In some cases the output frequencies will be divided down versions of the input clock.

Device	Processor and Application	Temp. Range (°C) (T_J)	V_{CC} (V)	Package	Max Part-Part Skew (ps)	Max Output Skew (ps)	Output Technology	Input	Outputs	Status
MC100ES6011	ECL Differential Fanout Buffer	-40 to 85 (T_A)	3.3/ 2.5	8 SOIC 8 TSSOP	150	20	LVPECL	ECL	1:2	P
MC100ES6014	Differential ECL/PECL/HSTL Clock Driver	-40 to 85 (T_A)	3.3/ 2.5	20 TSSOP	225	45	LVPECL	ECL PECL HSTL	1:5	P
MC100ES6017	ECL Quad Differential Receiver	-40 to 85 (T_A)	3.3	20 SOIC	TBD	TBD	LVPECL	LVPECL	Quad 1:1	IN
MC100ES60T22	Dual LVTTL/LVCMOS to Differential LVPECL Translator	-40 to 85 (T_A)	3.3	8 SOIC	300	n/a	PECL	LVTTL LVCMOS	Dual 1:1	S
MC100ES60T23	Dual Differential LVPECL to LVTTL Translator	-40 to 85 (T_A)	3.3	8 SOIC	TBD	TBD	LVTTL	LVPECL	Dual 1:1	IN
MC100ES6030	ECL Triple D flip-flop with set and reset	-40 to 85 (T_A)	3.3/ 2.5	20 SOIC	TBD	TBD	PECL	PECL	Triple 1:1	S
MC100ES6039	ECL ÷2/4, ÷4/6 Clock Generation Chip	-40 to 85 (T_A)	3.3/ 2.5	20 SOIC	TBD	TBD	PECL	PECL LVDS HSTL	1:4	P
MC100ES6056	ECL Dual Differential 2:1 Multiplexer	-40 to 85 (T_A)	3.3	20 SOIC 20 TSSOP	200	50	LVPECL	ECL	Dual 2:1	P
MC100ES6111	Clock distribution schemes requiring “very low” part-to-part and output-to-output skews	0 to 110	3.3/ 2.5	32 LQFP	250	35	3 GHz LVPECL	ECL LVPECL HSTL	1:10	P
MC100ES6130	2.5 GHz PECL/ECL clock driver with 2:1 differential input MUX	-40 to 85 (T_A)	3.3/ 2.5	16 TSSOP	150	25	PECL	PECL LVDS HSTL	1:4	P
MC100ES6139	ECL divided by 2/4, divided by 4/5/6 Clock Generation Chip	-40 to 85 (T_A)	3.3	20 SOIC 20 TSSOP	TBD	TBD	LVPECL	ECL	1:4	P
MC100ES6210	Clock distribution schemes requiring “very low” part-to-part and output-to-output skews	0 to 110	3.3/ 2.5	32 LQFP	175	35	3 GHz LVPECL	ECL LVPECL	Dual 1:5	P
MC100ES6220	LV/PECL Designs needing low skew. Telecom BackBone Equipment, Semi Test Equipment	0 to 110	3.3/ 2.5	52 LQFP exposed pad	200	50	3 GHz LVPECL	ECL LVPECL	Dual 1:10 DIFF	P
MC100ES6221	LV/PECL Designs needing low skew. Telecom BackBone Equipment, Semi Test Equipment	0 to 110	3.3/ 2.5	52 LQFP exposed pad	300	50	3 GHz LVPECL	ECL LVPECL	1:20 DIFF	P
MC100ES6222	LV/PECL Designs needing low skew. Telecom BackBone Equipment, Semi Test Equipment	0 to 110	3.3/ 2.5	52 LQFP exposed pad	300	50	3 GHz LVPECL	ECL LVPECL	1:15 DIFF	P
MC100ES6226	Clock distribution schemes requiring “extremely low” part-to-part and output-to-output skews	0 to 110	3/ 2.5	32 LQFP	325	35	3 GHz LVPECL	LVPECL	1:9	P

Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

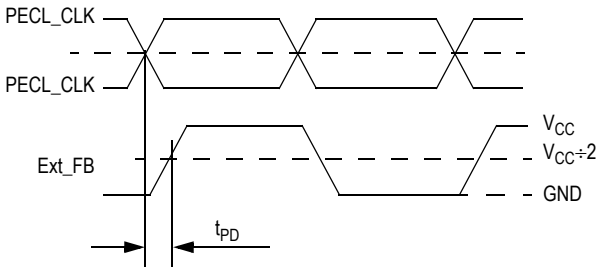
Differential Fanout Buffer Reference Table (continued)

Device	Processor and Application	Temp. Range (°C) (T_J)	V_{CC} (V)	Package	Max Part-Part Skew	Max Output Skew (ps)	Output Technology	Input	Outputs	Status
MC100ES6254	Differential 2x2 clock switch and Fanout Buffer	0 to 110	3/ 2.5	32 LQFP	250	35	3 GHz LVPECL	LVPECL	Single 1:6 or Double 1:3	P
MC100ES6535	1:4 LVCMOS to LVPECL clock fanout buffer	-40 to 85 (T_A)	3.3	20 TSSOP	190	30	PECL	PECL	1:4	P
MC100ES7011H	1:2 differential HSTL/LVDS clock fanout buffer	0 to 110	3.3	8 SOIC	TBD	TBD	LVDS	LVDS HSTL	1:2	IN
MC100ES7011P	1:2 differential PECL to LVDS clock fanout buffer	0 to 110	3.3	8 SOIC	TBD	TBD	LVDS	PECL	1:2	IN
MC100ES7014	1:5 differential LVDS clock fanout buffer	0 to 110	3.3	20 TSSOP	TBD	TBD	LVDS	PECL LVDS	1:5	IN
MC100ES7111	Clock distribution schemes requiring very low part-to-part and output-to-output skews	0 to 110	3.3	32 LQFP	TBD	TBD	LVDS	LVPECL HSTL LVDS	1:10	IN
MC100ES8011H	1:2 differential HSTL clock fanout buffer	0 to 110	3.3	8 SOIC	TBD	TBD	HSTL	HSTL	1:2	IN
MC100ES8011P	1:2 differential PECL to HSTL clock fanout buffer	0 to 110	3.3	8 SOIC	TBD	TBD	HSTL	PECL	1:2	IN
MC100ES8014	1:5 differential HSTL clock fanout buffer	0 to 110	3.3	20 TSSOP	TBD	TBD	HSTL	PECL HSTL	1:5	IN
MC100ES8111	Clock distribution schemes requiring “extremely low” part-to-part and output-to-output skews	0 to 110	3.3	32 LQFP	200	50	HSTL	HSTL LVPECL	1:10	P

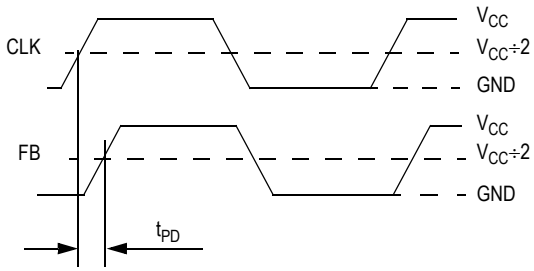
Legend:

IN = In Development (TARGET specifications) P = Production (FINAL specifications) S = Sampling (PRELIM specifications)

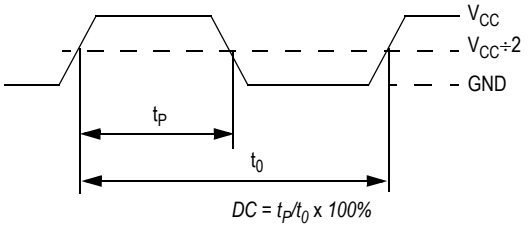
Clock Characteristic Diagrams



Propagation Delay (t_{PD}, static phase offset)
Test Reference (PECL)

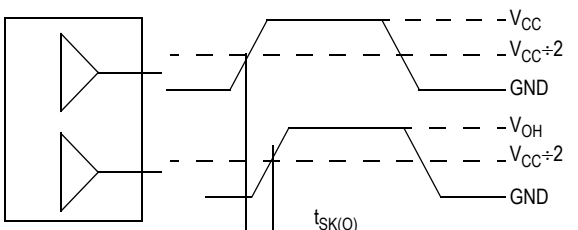


Propagation Delay (t_{PD}, static phase offset)
Test Reference (CMOS)



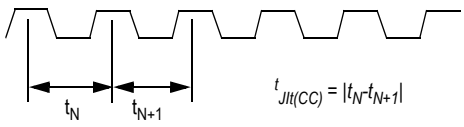
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Output Duty Cycle (DC)



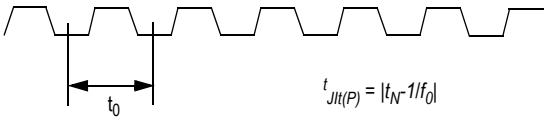
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Output-to-Output Skew $t_{SK(O)}$



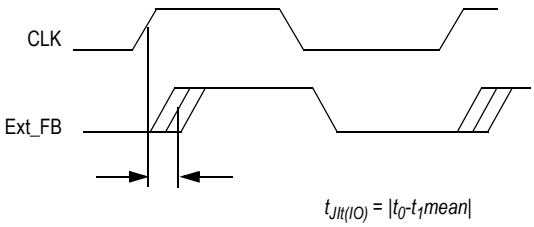
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Cycle-to-Cycle Jitter



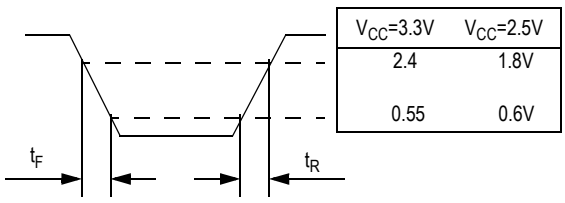
The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

I/O (Phase) Jitter



Transition Time Test Reference

Chapter Two
Clock Generator Data Sheets

Clock Generator Device Index

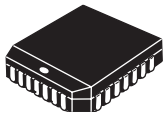
Order number: MC88915T
Rev 6, 08/2004

Low Skew CMOS PLL Clock Drivers, 3-State

55, 70, 100, 133, and 160 MHz Versions

MC88915TFN55
MC88915TFN70
MC88915TFN100
MC88915TFN133
MC88915TFN160

LOW SKEW CMOS
PLL CLOCK DRIVER



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776-02

The MC88915T Clock Driver utilizes phase-locked loop (PLL) technology to lock its low skew outputs frequencies and phase onto an input reference clock. It is designed to provide clock distribution for high performance PCs and workstations. For a 3.3 V version, see the MC88LV915T data sheet.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the MC88915T to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88915s can lock onto a single reference clock, ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 9).

Five “Q” outputs (Q0–Q4) are provided with less than 500 ps skew between their rising edges. The $\overline{Q5}$ output is inverted (180° phase shift) from the “Q” outputs. The 2X_Q output runs at twice the “Q” output frequency, while the Q/2 runs at 1/2 the “Q” frequency.

The VCO is designed to run optimally between 20 MHz and the 2X_Q f_{max} specification. The wiring diagrams in Figure 7 detail the different feedback configurations, creating specific input/output frequency relationships. Possible frequency ratios of the “Q” outputs to the SYNC input are 2:1, 1:1, and 1:2.

The FREQ_SEL pin provides one bit programmable divide-by in the feedback path of the PLL. It selects between divide-by-1 and divide-by-2 of the VCO before its signal reaches the internal clock distribution section of the chip (see Figure 2. MC88915T Block Diagram (All Versions)). In most applications FREQ_SEL should be held high (÷1). If a low frequency reference clock input is used, holding FREQ_SEL low (÷2) allows the VCO to run in its optimal range (>20 MHz and >40 MHz for the TFN133 version).

In normal phase-locked operation the PLL_EN pi is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88915 in a static “test mode.” In this mode, there is no frequency limitation on the input clock, necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board-level testing (see APPLICATIONS INFORMATION FOR ALL VERSIONS).

Pulling the $\overline{OE}/\overline{RST}$ pin low puts the clock outputs 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2 into a high impedance state (3-state). After the $\overline{OE}/\overline{RST}$ pin goes back high Q0–Q4, $\overline{Q5}$, and Q/2 will be reset in the low state, with 2X_Q being the inverse of the selected SYNC input. Assuming PLL_EN is low, the outputs will remain reset until the 88915 sees a SYNC input pulse.

A lock indicator output (LOCK) will go high when the loop is in steady-state phase and frequency lock. The LOCK output will go low if phase-lock is lost, or when the PLL_EN pin is low. The LOCK output will go high no later than 10 ms after the 88915 sees a SYNC signal and full 5.0 V V_{CC}.

Features

- Five outputs (Q0–Q4) with output-output skew < 500 ps, each being phase and frequency locked to the SYNC input
- The phase variation from part-to-part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t_{PD} specification, defining the part-to-part skew).
- Input/output phase-locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5 MHz – 2X_Q f_{max} specification (10 MHz – 2X_Q f_{max} for the TFN133 version)
- Additional outputs available at 2X and +2 the system “Q” frequency. Also, a $\overline{Q}$ (180° phase shift) output available
- All outputs have ±36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL-level compatible. ±88 mA I_{OL}/I_{OH} specifications guarantee 50 Ω transmission line switching on the incident edge.
- Test mode pin (PLL_EN) provided for low frequency testing. Two selectable CLOCK inputs for test or redundancy purposes. All outputs can go into high impedance (3-state) for board test purposes.
- Lock indicator (LOCK) accuracy indicates a phase-locked state

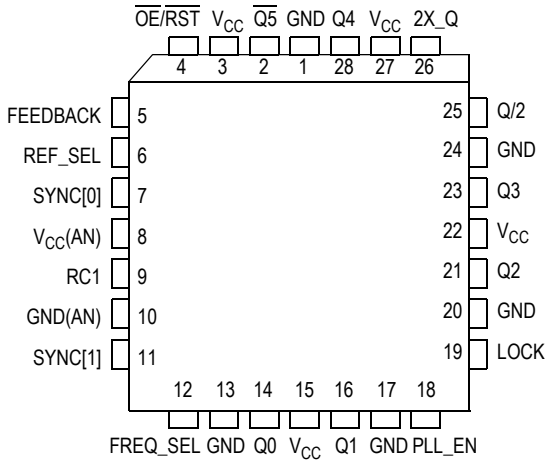


Figure 1. Pinout: 28-Lead PLCC (Top View)

Table 1. Pin Summary

Pin Name	Number	I/O	Function
SYNC[0]	1	Input	Reference clock input
SYNC[1]	1	Input	Reference clock input
REF_SEL	1	Input	Chooses reference between SYNC[0] and SYNC[1]
FREQ_SEL	1	Input	Doubles VCO internal frequency (low)
FEEDBACK	1	Input	Feedback input to phase detector
RC1	1	Input	Input for external RC network
Q(0–4)	5	Output	Clock output (locked to SYNC)
$\overline{Q5}$	1	Output	Inverse of clock output
2x_Q	1	Output	2 x clock output (Q) frequency (synchronous)
Q/2	1	Output	Clock output (Q) frequency ÷ 2 (synchronous)
LOCK	1	Output	Indicates phase lock has been achieved (high when locked)
$\overline{OE}/\overline{RST}$	1	Input	Output enable/asynchronous reset (active low)
PLL_EN	1	Input	Disables phase-lock for low frequency testing
V_{CC}, GND	11		Power and ground pins (note pins 8 and 10 are “analog” supply pins for internal PLL only)

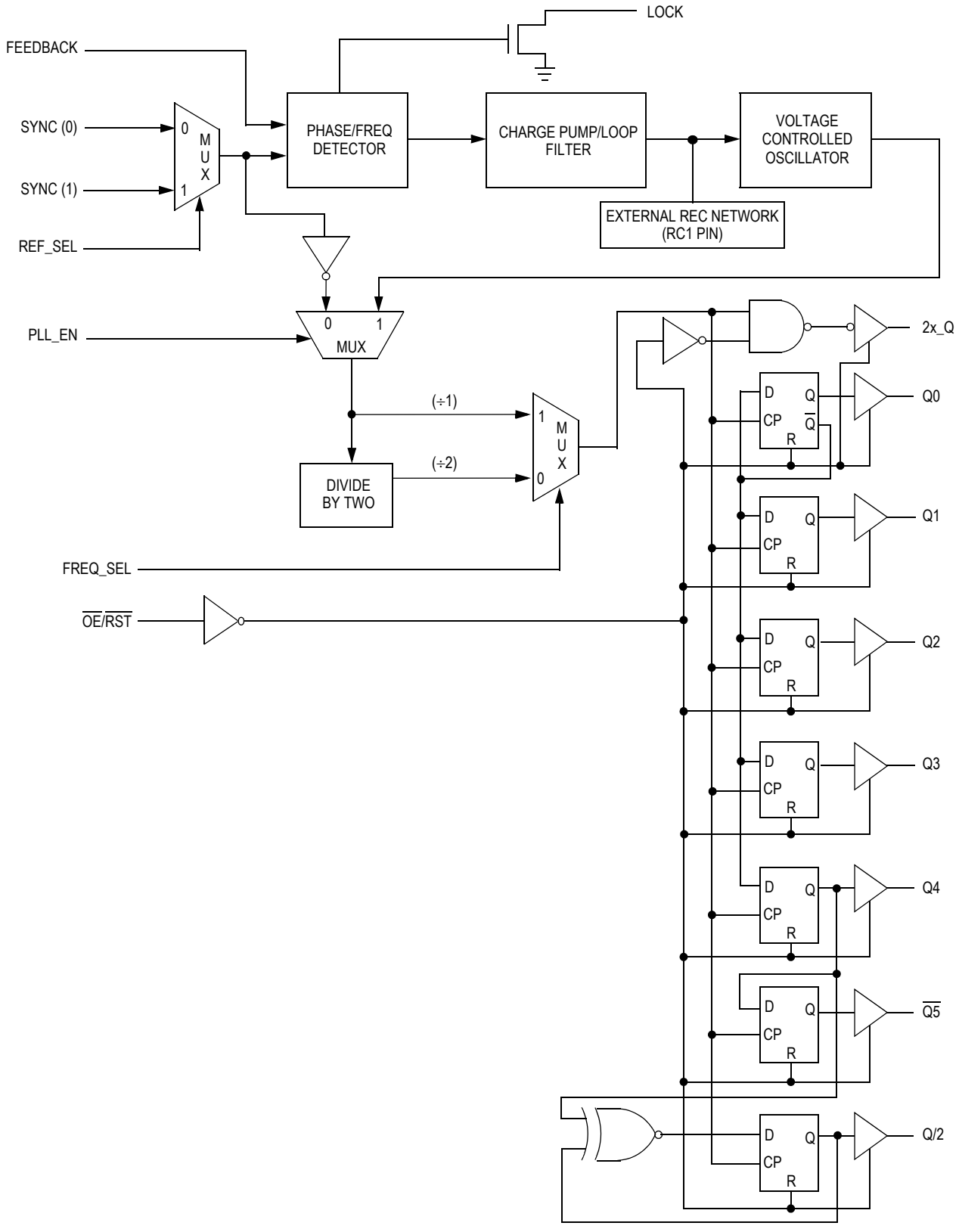


Figure 2. MC88915T Block Diagram (All Versions)

MC88915TFN55 AND MC88915TFN70

Table 2. SYNC Input Timing Requirements

Symbol	Parameter	Minimum		Maximum	Unit
		TFN70	TFN55		
$t_{RISE/FALL}$, SYNC Inputs	Rise/Fall Time, SYNC Inputs from 0.8 to 2.0 V	—	—	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period SYNC Inputs	28.5[1]	36.0[1]	200[2]	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% ± 25%			

1. These t_{CYCLE} minimum values are valid when “Q” output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 7**b**.
2. Information in Table 22 and in Note 3 of the AC specification notes describe this specification with its limits depending on what output is fed back, and if FREQ_SEL is high or low.

Table 3. DC Electrical Characteristics (Voltages Referenced to GND)
T_A = –40°C to +85°C for 55 MHz Version; T_A = 0°C to +70°C for 70 MHz Version; V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA[1]	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = 36 mA[1]	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	± 1.0	μA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} – 2.1 V	5.25	2.0	mA
I_{OLD}	Minimum Dynamic Output Current	V_{OLD} = 1.0 V Maximum	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85 V Minimum	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3-State Leakage Current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.25	± 50[2]	μA

1. Maximum test duration is 2.0 ms, one output loaded at a time.
2. Specification value for I_{OZ} is preliminary, will be finalized upon “MC” status.

Table 4. Capacitance and Power Specifications

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1[1]	Power Dissipation @ 50 MHz with 50 Ω Thevenin Termination	23 mW/Output 184 mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2[1]	Power Dissipation @ 50 MHz with 50 Ω Parallel Termination to GND	57 mW/Output 456 mW/Device	mW	V_{CC} = 5.0 V T = 25°C

1. PD_1 nd PD_2 mW/Output numbers are for a “Q” output.

MC88915TFN55 AND MC88915TFN70 (Continued)

Table 5. Frequency Specifications (T_A = –40°C to +85 °C, V_{CC} = 5.0 V ± 5%)

Symbol	Parameter	Guaranteed Minimum		Unit
		TFN70	TFN55	
f_{max}[1]	Maximum Operating Frequency (2X_Q Output)	70	55	MHz
	Maximum Operating Frequency (Q0–Q4, $\overline{Q5}$ Output)	35	27.5	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 Ω terminated to V_{CC}/2.

Table 6. AC Characteristics (T_A = –40°C to +85°C, V_{CC} = 5.0 V ± 5%, Load = 50 Ω Terminated to V_{CC}/2)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2 V_{CC} and 0.8 V_{CC})	1.0	2.5	ns	Into a 50 Ω Load Terminated to V_{CC}/2
$t_{RISE/FALL}$[1] 2X_Q Output	Rise/Fall Time into a 20 pF Load, with Termination Specified in Note[2]	0.5	1.6	ns	t_{RISE}: 0.8 V – 2.0 V t_{FALL}: 2.0 V – 0.8 V
$t_{PULSEWIDTH}$[1] (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q4, Q4, $\overline{Q5}$, Q/2 @ V_{CC}/2	0.5 t_{CYCLE} – 0.5[2]	0.5 t_{CYCLE} + 0.5[2]	ns	Into a 50 Ω Load Terminated to V_{CC}/2
$t_{PULSEWIDTH}$[1] (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5 V 66 MHz 50 MHz 40 MHz	0.5 t_{CYCLE} – 0.5[2] 0.5 t_{CYCLE} – 1.0 0.5 t_{CYCLE} – 1.5	0.5 t_{CYCLE} + 0.5[2] 0.5 t_{CYCLE} + 1.0 0.5 t_{CYCLE} + 1.5	ns	Must Use Termination Specified in Note[2]
$t_{PULSEWIDTH}$[1] (2X_Q Output)	Output Pulse Width: 2X_Q @ V_{CC}/2 50 – 65 MHz 40 – 49 MHz 66 – 70 MHz	0.5 t_{CYCLE} – 1.0[2] 0.5 t_{CYCLE} – 1.5 0.5 t_{CYCLE} – 0.5	0.5 t_{CYCLE} + 1.0[2] 0.5 t_{CYCLE} + 1.5 0.5 t_{CYCLE} + 0.5	ns	Into a 50 Ω Load Terminated to V_{CC}/2
t_{PD}[1,3] SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1 MΩ from RC1 to An V_{CC})		ns	See Note[4] and Figure 4 for Detailed Explanation
		–1.05	–0.40		
		(With 1 MΩ from RC1 to An GND)			
		+1.25	+3.25		
t_{SKEWr}[1,4] (Rising)[5]	Output-to-Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
t_{SKEWf}[1,4] (Falling)	Output-to-Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
$t_{SKEWall}$[1,4]	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
t_{LOCK}[5]	Time Required to Acquire Phase-Lock from Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL}[6]	Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low
t_{PHZ}, t_{PLZ}[6]	Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low

1. These specifications are not tested. They are guaranteed by statistical characterization. See AC specification Note 1.
2. t_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
3. The t_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With V_{CC} fully powered on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1 μF, t_{LOCK} minimum is with C1 = 0.01 μF.
6. The t_{PZL}, t_{PHZ}, t_{PLZ} minimum and maximum specifications are estimates. The final guaranteed values will be available when "MC" status is reached.

MC88915TFN100

Table 7. SYNC Input Timing Requirements

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$, SYNC Inputs	Rise/Fall Time, SYNC Inputs from 0.8 to 2.0 V	—	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period SYNC Inputs	20.0[1]	200[2]	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% ± 25%		

1. These t_{CYCLE} minimum values are valid when “Q” output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 7**b**.
2. Information in Table 22 and in Note 3 of the AC specification notes describe this specification with its limits depending on what output is fed back, and if FREQ_SEL is high or low.

Table 8. DC Electrical Characteristics (Voltages Referenced to GND) T_A = –40°C to +85°C, V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA[1]	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = 36 mA[1]	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	± 1.0	μA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} –2.1 V	5.25	2.0[2]	mA
I_{OLD}	Minimum Dynamic Output Current[3]	V_{OLD} = 1.0 V Maximum	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85 V Minimum	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3-State Leakage Current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.25	± 50[4]	μA

1. I_{OL} and I_{OH} are 12 mA and –12 mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0 ms, one output loaded at a time.
4. Specification value for I_{OZ} is preliminary, will be finalized upon “MC” status.

Table 9. Capacitance and Power Specifications

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1[1]	Power Dissipation @ 50 MHz with 50 Ω Thevenin Termination	23 mW/Output 184 mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2[1]	Power Dissipation @ 50 MHz with 50 Ω Parallel Termination to GND	57 mW/Output 456 mW/Device	mW	V_{CC} = 5.0 V T = 25°C

1. PD_1 nd PD_2 mW/Output numbers are for a “Q” output.

Table 10. Frequency Specifications (T_A = –40°C to +85 °C, V_{CC} = 5.0 V ± 5%)

Symbol	Parameter	Guaranteed Minimum	Unit
		TFN100	
f_{max}[1]	Maximum Operating Frequency (2X_Q Output)	100	MHz
	Maximum Operating Frequency (Q0–Q4, $\overline{Q5}$ Output)	50	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 Ω terminated to V_{CC}/2.

MC88915TFN100 (Continued)

Table 11. AC Characteristics (T_A = –40°C to +85°C, V_{CC} = 5.0 V ± 5%, Load = 50 Ω Terminated to V_{CC}/2)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2 V_{CC} and 0.8 V_{CC})	1.0	2.5	ns	Into a 50 Ω Load Terminated to V_{CC}/2
$t_{RISE/FALL}$[1] 2X_Q Output	Rise/Fall Time into a 20 pF Load, with Termination Specified in Note[2]	0.5	1.6	ns	t_{RISE}: 0.8 V – 2.0 V t_{FALL}: 2.0 V – 0.8 V
$t_{PULSEWIDTH}$[1] (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q4, Q4, $\overline{Q5}$, Q/2 @ V_{CC}/2	0.5 t_{CYCLE} – 0.5[2]	0.5 t_{CYCLE} + 0.5[2]	ns	Into a 50 Ω Load Terminated to V_{CC}/2
$t_{PULSEWIDTH}$[1] (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5 V	0.5 t_{CYCLE} – 0.5[2]	0.5 t_{CYCLE} + 0.5[2]	ns	Must Use Termination Specified in Note[2]
$t_{PULSEWIDTH}$[1] (2X_Q Output)	Output Pulse Width: 2X_Q @ V_{CC}/2 40 – 49 MHz 50 – 65 MHz 66 – 100 MHz	0.5 t_{CYCLE} – 1.5[2] 0.5 t_{CYCLE} – 1.0 0.5 t_{CYCLE} – 0.5	0.5 t_{CYCLE} + 1.5[2] 0.5 t_{CYCLE} + 1.0 0.5 t_{CYCLE} + 0.5	ns	Into a 50 Ω Load Terminated to V_{CC}/2
t_{PD}[1,3] SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1 MΩ from RC1 to An V_{CC})		ns	See Note[4] and Figure 4 for Detailed Explanation
		–1.05	–0.30		
		(With 1 MΩ from RC1 to An GND)			
		+1.25	+3.25		
t_{SKEWr}[1,4] (Rising)[5]	Output-to-Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
t_{SKEWf}[1,4] (Falling)	Output-to-Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
$t_{SKEWall}$[1,4]	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
t_{LOCK}[5]	Time Required to Acquire Phase-Lock from Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL}[6]	Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low
t_{PHZ}, t_{PLZ}[6]	Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low

1. These specifications are not tested. They are guaranteed by statistical characterization. See AC specification Note 1.
2. t_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
3. The t_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With V_{CC} fully powered on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1 μF, t_{LOCK} minimum is with C1 = 0.01 μF.
6. The t_{PZL}, t_{PHZ}, t_{PLZ} minimum and maximum specifications are estimates. The final guaranteed values will be available when "MC" status is reached.

MC88915TFN133

Table 12. SYNC Input Timing Requirements

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$, SYNC Inputs	Rise/Fall Time, SYNC Inputs from 0.8 to 2.0 V	—	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period SYNC Inputs	15.0[1]	100[2]	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% ± 25%		

1. These t_{CYCLE} minimum values are valid when “Q” output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 7**b**.
2. Information in Table 22 and in Note 3 of the AC specification notes describe this specification with its limits depending on what output is fed back, and if FREQ_SEL is high or low.

Table 13. DC Electrical Characteristics (Voltages Referenced to GND) T_A = –40°C to +85°C, V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA[1]	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = 36 mA[1]	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	± 1.0	μA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} –2.1 V	5.25	2.0[2]	mA
I_{OLD}	Minimum Dynamic Output Current[3]	V_{OLD} = 1.0 V Maximum	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85 V Minimum	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3-State Leakage Current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.25	± 50[4]	μA

1. I_{OL} and I_{OH} are 12 mA and –12 mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0 ms, one output loaded at a time.
4. Specification value for I_{OZ} is preliminary, will be finalized upon “MC” status.

Table 14. Capacitance and Power Specifications

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1[1]	Power Dissipation @ 50 MHz with 50 Ω Thevenin Termination	23 mW/Output 184 mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2[1]	Power Dissipation @ 50 MHz with 50 Ω Parallel Termination to GND	57 mW/Output 456 mW/Device	mW	V_{CC} = 5.0 V T = 25°C

1. PD_1 nd PD_2 mW/Output numbers are for a “Q” output.

Table 15. Frequency Specifications (T_A = –40°C to +85 °C, V_{CC} = 5.0 V ± 5%)

Symbol	Parameter	Guaranteed Minimum	Unit
		TFN133	
f_{max}[1]	Maximum Operating Frequency (2X_Q Output)	133	MHz
	Maximum Operating Frequency (Q0–Q4, $\overline{Q5}$ Output)	66	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 Ω terminated to V_{CC}/2.

MC88915TFN133 (Continued)

Table 16. AC Characteristics (T_A = –40°C to +85°C, V_{CC} = 5.0 V ± 5%, Load = 50 Ω Terminated to V_{CC}/2)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2 V_{CC} and 0.8 V_{CC})	1.0	2.5	ns	Into a 50 Ω Load Terminated to V_{CC}/2
$t_{RISE/FALL}$[1] 2X_Q Output	Rise/Fall Time into a 20 pF Load, with Termination Specified in Note[2]	0.5	1.6	ns	t_{RISE}: 0.8 V – 2.0 V t_{FALL}: 2.0 V – 0.8 V
$t_{PULSEWIDTH}$[1] (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q4, Q4, $\overline{Q5}$, Q/2 @ V_{CC}/2	0.5 t_{CYCLE} – 0.5[2]	0.5 t_{CYCLE} + 0.5[2]	ns	Into a 50 Ω Load Terminated to V_{CC}/2
$t_{PULSEWIDTH}$[1] (2X_Q Output)	Output Pulse Width: 66 – 133 MHz 2X_Q @ 1.5 V 40 – 65 MHz	0.5 t_{CYCLE} – 0.5[2] 0.5 t_{CYCLE} – 0.9	0.5 t_{CYCLE} + 0.5[2] 0.5 t_{CYCLE} + 0.9	ns	Must Use Termination Specified in Note[2]
$t_{PULSEWIDTH}$[1] (2X_Q Output)	Output Pulse Width: 66 – 133 MHz 2X_Q @ V_{CC}/2 40 – 65 MHz	0.5 t_{CYCLE} – 0.5[2] 0.5 t_{CYCLE} – 0.9	0.5 t_{CYCLE} + 0.5[2] 0.5 t_{CYCLE} + 0.9	ns	Into a 50 Ω Load Terminated to V_{CC}/2
t_{PD}[1,3] SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1 MΩ from RC1 to An V_{CC})		ns	See Note[4] and Figure 4 for Detailed Explanation
		–1.05	–0.25		
		(With 1 MΩ from RC1 to An GND)			
		+1.25	+3.25		
t_{SKEWr}[1,4] (Rising)[5]	Output-to-Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
t_{SKEWf}[1,4] (Falling)	Output-to-Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
$t_{SKEWall}$[1,4]	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
t_{LOCK}[5]	Time Required to Acquire Phase-Lock from Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL}[6]	Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low
t_{PHZ}, t_{PLZ}[6]	Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low

1. These specifications are not tested. They are guaranteed by statistical characterization. See AC specification Note 1.
2. t_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
3. The t_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
4. Under equally loaded conditions and at a fixed temperature and voltage.
5. With V_{CC} fully powered on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1 μF, t_{LOCK} minimum is with C1 = 0.01 μF.
6. The t_{PZL}, t_{PHZ}, t_{PLZ} minimum and maximum specifications are estimates. The final guaranteed values will be available when "MC" status is reached.

MC88915TFN160

Table 17. SYNC Input Timing Requirements

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$, SYNC Inputs	Rise/Fall Time, SYNC Inputs from 0.8 to 2.0 V	—	3.0	ns
t_{CYCLE}, SYNC Inputs	Input Clock Period SYNC Inputs	12.5[1]	100[2]	ns
Duty Cycle SYNC Inputs	Input Duty Cycle SYNC Inputs	50% ± 25%		

1. These t_{CYCLE} minimum values are valid when “Q” output is fed back and connected to the FEEDBACK pin. This is the configuration shown in Figure 7**b**.
2. Information in Table 22 and in Note 3 of the AC specification notes describe this specification with its limits depending on what output is fed back, and if FREQ_SEL is high or low.

Table 18. DC Electrical Characteristics (Voltages Referenced to GND) T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 5%

Symbol	Parameter	Test Conditions	V_{CC} V	Target Limit	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{out} = 0.1 V or V_{CC} –0.1 V	4.75 5.25	2.0 2.0	V
V_{IL}	Maximum Low-Level Input Voltage	V_{out} = 0.1 V or V_{CC} – 0.1 V	4.75 5.25	0.8 0.8	V
V_{OH}	Minimum High-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = –36 mA[1]	4.75 5.25	4.01 4.51	V
V_{OL}	Maximum Low-Level Output Voltage	V_{in} = V_{IH} or V_{IL} I_{OH} = 36 mA[1]	4.75 5.25	0.44 0.44	V
I_{in}	Maximum Input Leakage Current	V_I = V_{CC} or GND	5.25	± 1.0	μA
I_{CCT}	Maximum I_{CC}/Input	V_I = V_{CC} –2.1 V	5.25	2.0[2]	mA
I_{OLD}	Minimum Dynamic Output Current[3]	V_{OLD} = 1.0 V Maximum	5.25	88	mA
I_{OHD}		V_{OHD} = 3.85 V Minimum	5.25	–88	mA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_I = V_{CC} or GND	5.25	1.0	mA
I_{OZ}	Maximum 3-State Leakage Current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND	5.25	± 50[4]	μA

1. I_{OL} and I_{OH} are 12 mA and –12 mA respectively for the LOCK output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration is 2.0 ms, one output loaded at a time.
4. Specification value for I_{OZ} is preliminary, will be finalized upon “MC” status.

Table 19. Capacitance and Power Specifications

Symbol	Parameter	Typical Values	Unit	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	40	pF	V_{CC} = 5.0 V
PD_1[1]	Power Dissipation @ 50 MHz with 50 Ω Thevenin Termination	15 mW/Output 120 mW/Device	mW	V_{CC} = 5.0 V T = 25°C
PD_2[1]	Power Dissipation @ 50 MHz with 50 Ω Parallel Termination to GND	57 mW/Output 456 mW/Device	mW	V_{CC} = 5.0 V T = 25°C

1. PD_1 nd PD_2 mW/Output numbers are for a “Q” output.

Table 20. Frequency Specifications (T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 5%)

Symbol	Parameter	Guaranteed Minimum	Unit
		TFN160	
f_{max}[1]	Maximum Operating Frequency (2X_Q Output)	160	MHz
	Maximum Operating Frequency (Q0–Q4, $\overline{Q5}$ Output)	80	MHz

1. Maximum Operating Frequency is guaranteed with the part in a phase-locked condition, and all outputs loaded with 50 Ω terminated to V_{CC}/2.

MC88915TFN160 (Continued)

Table 21. AC Characteristics (T_A = 0°C to +70°C, V_{CC} = 5.0 V ± 5%, Load = 50 Ω Terminated to V_{CC}/2)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.2 V_{CC} and 0.8 V_{CC})	1.0	2.5	ns	Into a 50 Ω Load Terminated to V_{CC}/2
$t_{RISE/FALL}$ 2X_Q Output	Rise/Fall Time	0.5	1.6	ns	t_{RISE}: 0.8 V – 2.0 V t_{FALL}: 2.0 V – 0.8 V
$t_{PULSEWIDTH}$ (Q0–Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q4, Q4, $\overline{Q5}$, Q/2 @ V_{CC}/2	0.5 t_{CYCLE} – 0.5[2]	0.5 t_{CYCLE} + 0.5[2]	ns	Into a 50 Ω Load Terminated to V_{CC}/2
$t_{PULSEWIDTH}$ (2X_Q Output)	Output Pulse Width: 80 MHz 2X_Q @ 1.5 V 100 MHz 133 MHz 160 MHz	0.5 t_{CYCLE} – 0.7 0.5 t_{CYCLE} – 0.5 0.5 t_{CYCLE} – 0.5 TBD	0.5 t_{CYCLE} + 0.7 0.5 t_{CYCLE} + 0.5 0.5 t_{CYCLE} + 0.5 TBD	ns	
t_{PD}[1] SYNC Feedback	SYNC Input to Feedback Delay (Measured at SYNC0 or 1 and FEEDBACK Input Pins)	(With 1 MΩ from RC1 to An V_{CC})		ns	See Note[2] and Figure 4 for Detailed Explanation
	133 MHz 160 MHz	–1.05 –0.9	–0.25 –0.10		
t_{CYCLE} (2x_Q Output)	Cycle-to-Cycle Variation 133 MHz 160 MHz	t_{CYCLE} – 300 ps t_{CYCLE} – 300 ps	t_{CYCLE} + 300 ps t_{CYCLE} + 300 ps		
t_{SKEWr}[3] (Rising)[4]	Output-to-Output Skew Between Outputs Q0–Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
t_{SKEWf}[3] (Falling)	Output-to-Output Skew Between Outputs Q0–Q4 (Falling Edges Only)	—	500	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
$t_{SKEWall}$[3]	Output-to-Output Skew 2X_Q, Q/2, Q0–Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs into a Matched 50 Ω Load Terminated to V_{CC}/2
t_{LOCK}[4]	Time Required to Acquire Phase-Lock from Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL}[5]	Output Enable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low
t_{PHZ}, t_{PLZ}[5]	Output Disable Time $\overline{OE}$/$\overline{RST}$ to 2X_Q, Q0–Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured with the PLL_EN Pin Low

1. T_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
2. The T_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
3. Under equally loaded conditions and at a fixed temperature and voltage.
4. With V_{CC} fully powered on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1 μF, t_{LOCK} minimum is with C1 = 0.01 μF.
5. The t_{PZL}, t_{PHZ}, t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when "MC" status is reached.

APPLICATIONS INFORMATION FOR ALL VERSIONS

General AC Specification Notes

1. Several specifications can only be measured when the MC88915TFN55, 70 and 100 are in phase-locked operation. It is not possible to have the part in phase-lock on automated test equipment (ATE). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88915TFN55, 70 and 100 units were fabricated with key transistor properties intentionally varied to create a 14-cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area, to set performance limits of ATE testable specifications within those to be guaranteed by statistical characterization. In this way, all units passing the ATE test will meet or exceed the non-tested specifications limits.
2. These two specs ($t_{RISE/FALL}$ and t_{PULSE} Width 2X_Q output) guarantee the MC88915T meets the 40 MHz and 33 MHz MC68040 P-Clock input specification (at 80 MHz and 66 MHz, respectively). For these two specs to be guaranteed by Freescale Semiconductor, the termination scheme shown below in Figure 3 must be used.
3. The wiring diagrams and explanations in Figure 7 demonstrate the input and output frequency relationships for three possible feedback configurations. The allowable SYNC input range for each case is also indicated. There are two allowable SYNC frequency ranges, depending whether FREQ_SEL is high or low. Although not shown, it is possible to feed back the $\overline{Q5}$ output, thus creating a 180° phase shift between the SYNC input and the "Q" outputs. Table 22 below summarizes the allowable SYNC frequency range for each possible configuration.

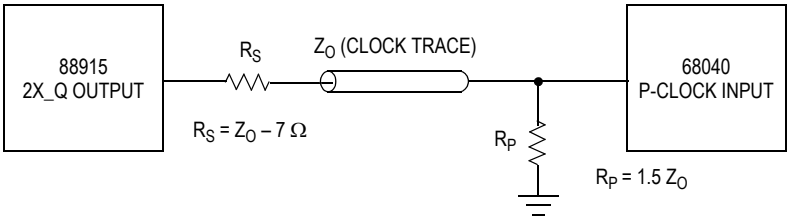


Figure 3. MC68040 P-Clock Input Termination Scheme

Table 22. Allowable SYNC Input Frequency Ranges for Different Feedback Configurations

FREQ_SEL Level	Feedback Output	Allowable SYNC Input Frequency Range (MHz)	Corresponding VCO Frequency Range	Phase Relationships of the "Q" Outputs to Rising SYNC Edge
HIGH	Q/2	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
HIGH	Any "Q" (Q0–Q4)	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	0°
HIGH	$\overline{Q5}$	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	180°
HIGH	2X_Q	20 to (2X_Q FMAX Spec)	20 to (2X_Q FMAX Spec)	0°
LOW	Q/2	2.5 to (2X_Q FMAX Spec)/8	20 to (2X_Q FMAX Spec)	0°
LOW	Any "Q" (Q0–Q4)	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	0°
LOW	$\overline{Q5}$	5 to (2X_Q FMAX Spec)/4	20 to (2X_Q FMAX Spec)	180°
LOW	2X_Q	10 to (2X_Q FMAX Spec)/2	20 to (2X_Q FMAX Spec)	0°

4. A 1 MΩ resistor tied to either Analog V_{CC} or Analog GND, depicted in Figure 4, is required to ensure no jitter is present on the MC88915T outputs. This technique causes a phase offset between the SYNC input and the output connected to the FEEDBACK input, measured at the input pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were determined by measuring the phase relationship for the 14 lots described in Note 1 while the part was in phase-locked operation. The actual measurements were made with a 10 MHz SYNC input (1.0 ns edge rate from 0.8 V – 2.0 V) with the Q/2 output fed back. The phase measurements were made at 1.5 V. The Q/2 output was terminated at the FEEDBACK input with 100 Ω to V_{CC} and 100 Ω to ground.

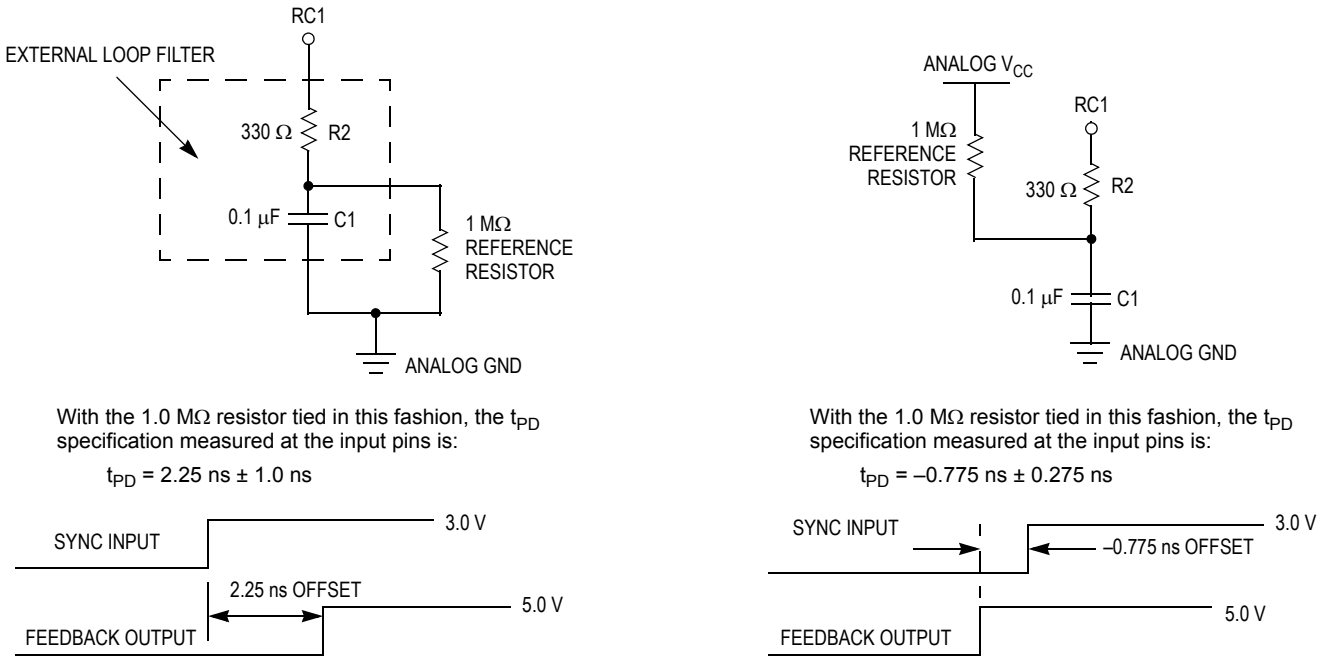


Figure 4. Depiction of the Fixed SYNC to Feedback Offset (t_{PD}) Which Is Present When a 1 mΩ Resistor is Tied to V_{CC} or Ground

5. The t_{SKEWr} specification guarantees the rising edges of outputs Q/2, Q0, Q1, Q2, Q3, and Q4 will always fall within a 500 ps window within one part. However, if the relative position of each output within this window is not specified, the 500 ps window must be added to each side of the t_{PD} specification limits to calculate the total part-to-part skew. For this reason, the absolute distribution of these outputs are provided in Table 23. When taking the skew data, Q0 was used as a reference, so all measurements are relative to this output. The information in Table 23 is derived from measurements taken from the 14 process lots described in Note 1, over the temperature and voltage range.

Table 23. Relative Positions of Outputs Q/2, Q0–Q4, 2X_Q Within the 500 ps t_{SKEWr} Spec Window

Output	– (ps)	+ (ps)
Q0	0	0
Q1	–72	40
Q2	–44	276
Q3	–40	255
Q4	–274	–34
Q/2	–16	250
2X_Q	–633	–35

6. **Calculation of Total Output-to-Skew Between Multiple Parts (Part-to-Part Skew)**

   By combining the t_{PD} specification and the information in Note 5, the worst case output-to-output skew between multiple 88915s connected in parallel can be calculated. This calculation assumes all parts have a common SYNC input clock with equal delay of input signal to each part. This skew value is valid at the 88915 output pins only (equally loaded), it does not include PCB trace delays due to varying loads.

   With a 1.0 MΩ resistor tied to analog V_{CC} as shown in Note 4, the t_{PD} spec. limits between SYNC and the Q/2 output (connected to the FEEDBACK pin) are –1.05 ns and –0.5 ns. To calculate the skew of any given output between two or more parts, the absolute value of the distribution of the output given in Table 23 must be subtracted and added to the lower and upper t_{PD} spec limits respectively. For output Q2, [276 – (–44)] = 320 ps is the absolute value of the distribution. Therefore, [–1.05 ns – 0.32 ns] = –1.37 ns is the lower t_{PD} limit, and [–0.5 ns + 0.32 ns] = –0.18 ns is the upper limit. Therefore, the worst case skew of output Q2 between any number of parts is |(–1.37) – (–0.18)| = 1.19 ns. Q2 has the worst case skew distribution of any output, so 1.2 ns is the absolute worst case output-to-output skew between multiple parts.

7. Note 4 explains the t_{PD} specification was measured and is guaranteed for the configuration of the Q/2 output connected to the FEEDBACK pin and the SYNC input running at 10 MHz. The fixed offset (t_{PD}) as described above has some dependence on the input frequency and at what frequency the VCO is running. The graphs of Figure 5 demonstrate this dependence.

   The data presented in Figure 5 is from devices representing process extremes, and the measurements were also taken at the voltage extremes (V_{CC} = 5.25 V and 4.75 V). Therefore, the data in Figure 5 is a realistic representation of the variation of t_{PD}.

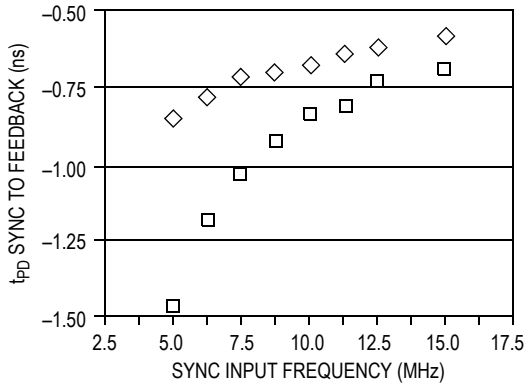


Figure 5a

t_{PD} versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (with 1.0 MΩ Resistor Tied to Analog V_{CC})

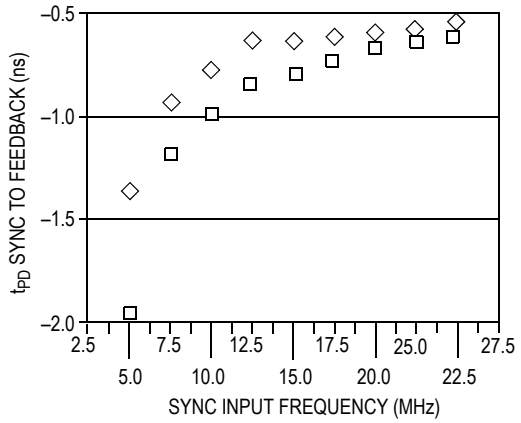


Figure 5b

t_{PD} versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (with 1.0 MΩ Resistor Tied to Analog V_{CC})

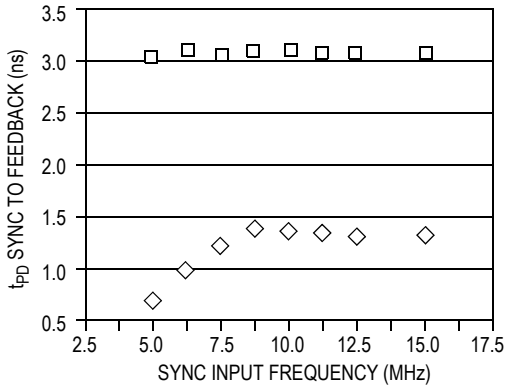


Figure 5c

t_{PD} versus Frequency Variation for Q/2 Output Fed Back, Including Process and Voltage Variation @ 25°C (with 1.0 MΩ Resistor Tied to Analog GND)

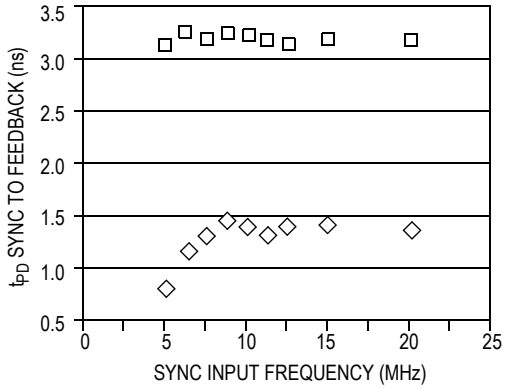


Figure 5d

t_{PD} versus Frequency Variation for Q4 Output Fed Back, Including Process and Voltage Variation @ 25°C (with 1.0 MΩ Resistor Tied to Analog GND)

Figure 5. Graphs

8. The lock indicator pin (LOCK) will reliably indicate a phase-locked condition at SYNC input frequencies down to 10 MHz. At frequencies below 10 MHz, the frequency of correction pulses going into the phase detector form the SYNC and FEEDBACK pins may not be sufficient to allow the lock indicator circuitry to accurately predict a phase-locked condition. The MC88915T is guaranteed to provide stable phase-locked operation down to the appropriate minimum input frequency given in Table 22, even though the LOCK pin may be LOW at frequencies below 10 MHz. The exact minimum frequency where the lock indicator functionality can be guaranteed will be available when the MC88915T reaches “MC” status.

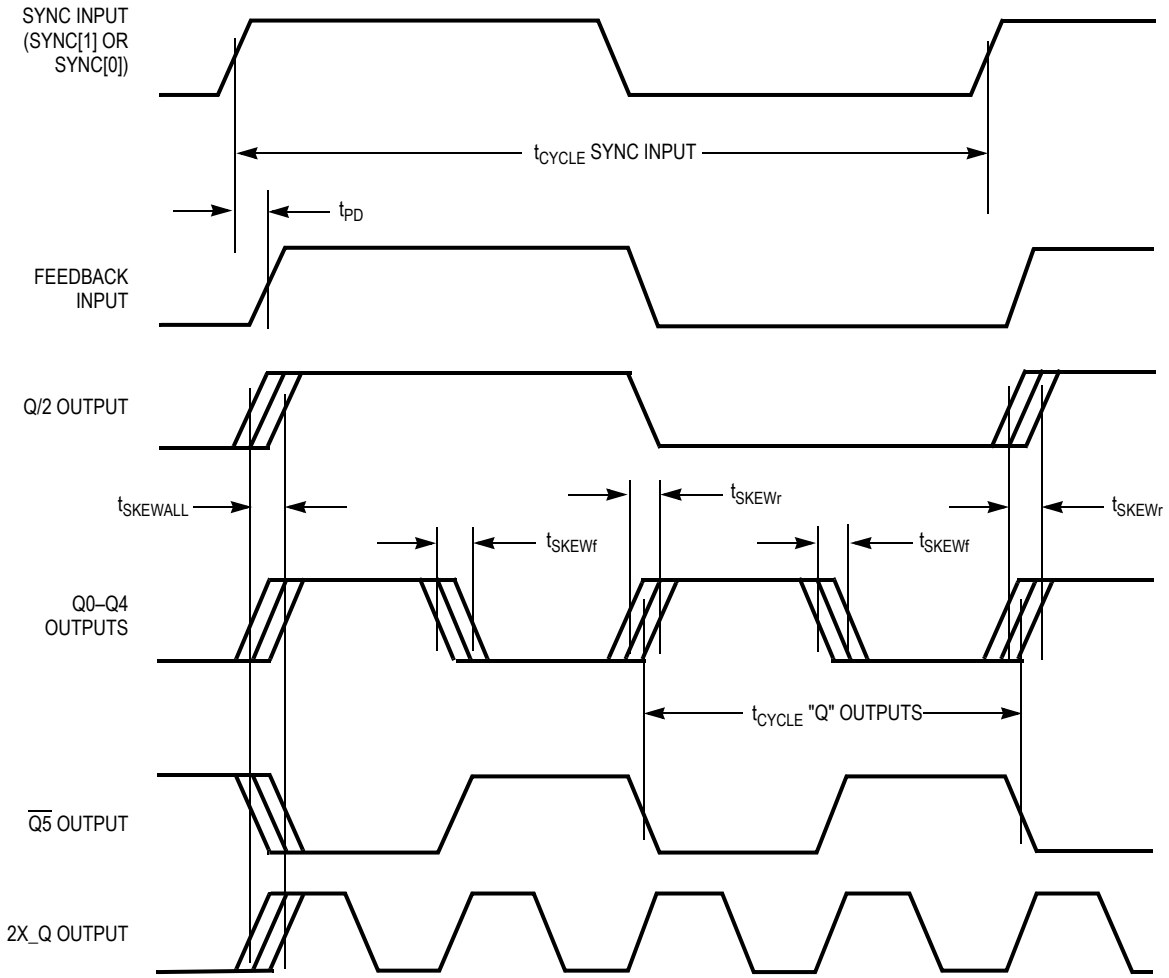
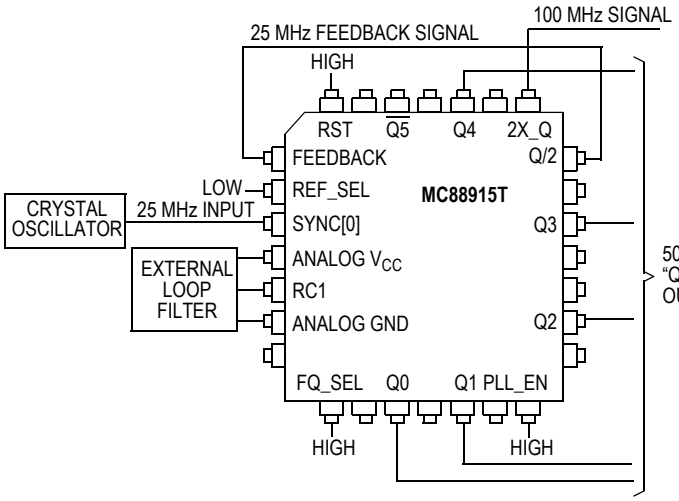


Figure 6. Output/Input Switching Waveforms and Timing Diagrams
(These waveforms represent the hook-up configuration of **Figure 7a**)

TIMING NOTES:

1. The MC88915T aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the VCC/2 crossing point of the appropriate output edges. All skews are specified as “windows,” not as a ± deviation around a center point.
3. If a “Q” output is connected to the FEEDBACK input (this situation is not shown), the “Q” output frequency would match the SYNC input frequency, the 2X_Q output would run at twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency.

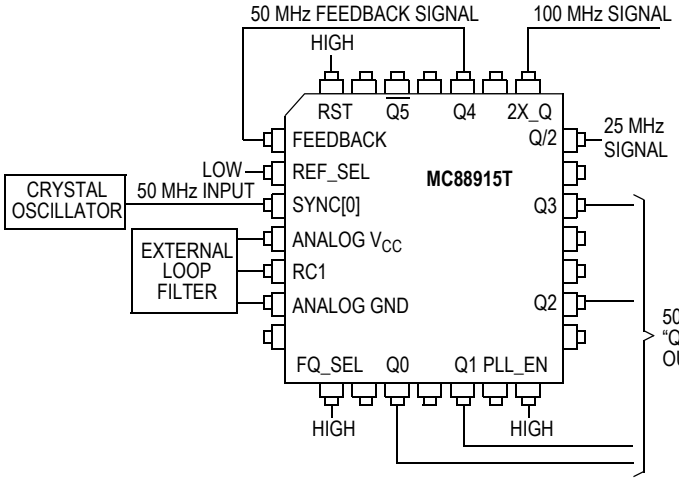


1:2 Input to "Q" Output Frequency Relationship
In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The "Q" outputs (Q0–Q4, $\overline{Q5}$) will always run at 2X the Q/2 frequency, and the 2X_Q output will run at 4X the Q/2 frequency.

Allowable Input Frequency Range:
5 MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL HIGH)
2.5 MHz to (2X_Q FMAX Spec)/8 (for FREQ_SEL LOW)

NOTE: If the $\overline{OE}$/$\overline{RST}$ input is active, a pullup or pull-down resistor isn't necessary at the FEEDBACK pin so it won't when the fed back output goes into 3-state.

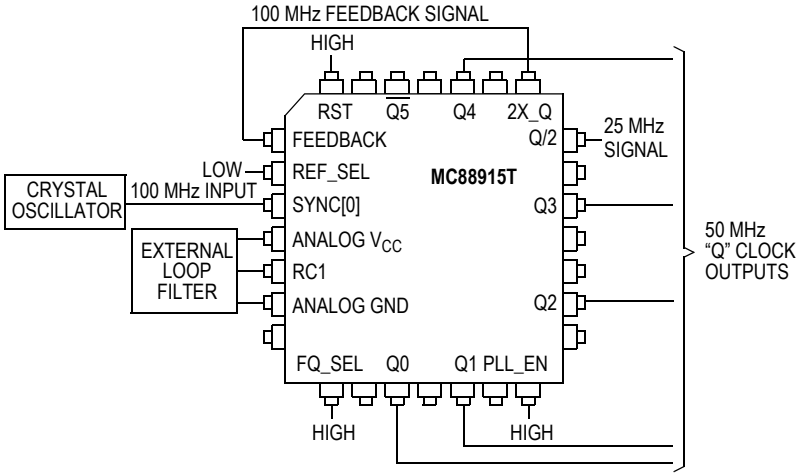
Figure 7a. Wiring Diagram and Frequency Relationships with Q/2 Output Feedback



1:1 Input to "Q" Output Frequency Relationship
In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always rn at 1/2 the "Q" frequency, and the 2X_Q output will run at 2X the "Q" frequency.

Allowable Input Frequency Range:
10 MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL HIGH)
5 MHz to (2X_Q FMAX Spec)/8 (for FREQ_SEL LOW)

Figure 7b. Wiring Diagram and Frequency Relationships with Q4 Output Feedback



2:1 Input to "Q" Output Frequency Relationship
In this application, the 2X_Q output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of 2X_Q and SYNC, thus the 2X_Q frequency will equal the SYNC frequency. The Q/2 output will always run at 1/3 the 2X_Q frequency, and the "Q" outputs will run at 1/2 the 2X_Q frequency.

Allowable Input Frequency Range:
20 MHz to (2X_Q FMAX Spec) (for FREQ_SEL HIGH)
10 MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL LOW)

Figure 7c. Wiring Diagram and Frequency Relationships with 2X_Q Output Feedback

Figure 7. Wiring Diagrams

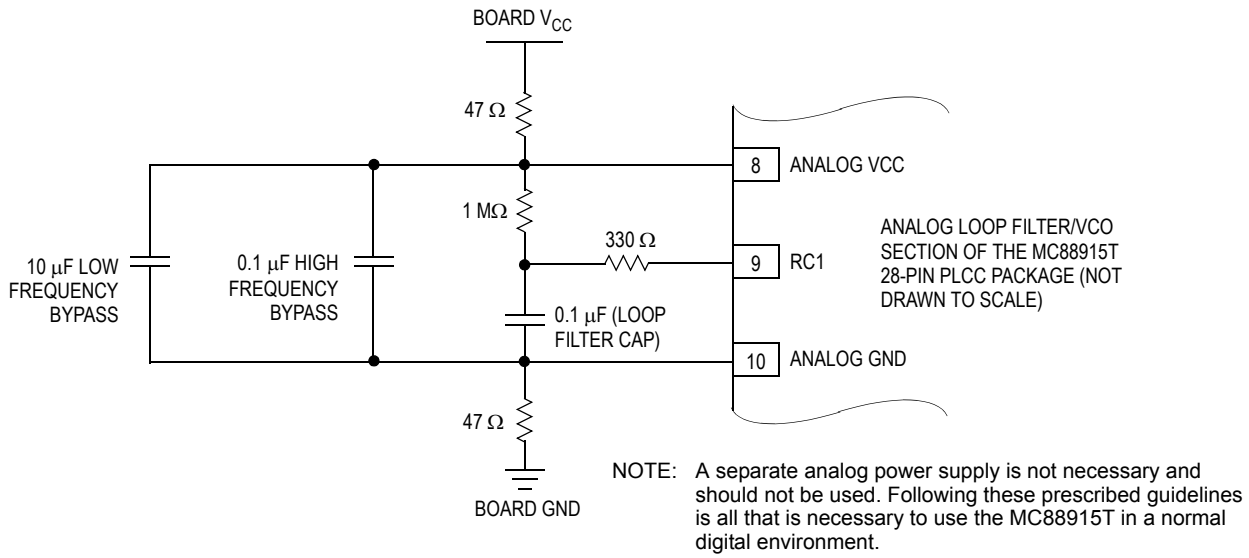


Figure 8. Recommended Loop Filter and Analog Isolation Scheme for the MC88915T

Notes Concerning Loop Filter and Board Layout Issues

1. Figure 8 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter-free operation:
   a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.
   b. The 47 Ω resistors, the 10 μF low frequency bypass capacitor, and the 0.1 μF high frequency bypass capacitor form a wide bandwidth filter minimizing the 88915T's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure a 100 mV step deviation on the digital V_{CC} supply, causing no more than a 100 ps phase deviation o the 88915T outputs. A 250 mV step deviation on VCC using the recommended filter values should cause no more than 250 ps phase deviation; if a 25 μF bypass capacitor is used (instead of 10 μF) a 250 mV V_{CC} step should cause no more than a 100 ps phase deviation.

      If good bypass techniques are used on a board design near components potentially causing digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88915T's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 8 is to give the 88915T additional protection from the power supply and ground plane transients potentially occurring in a high frequency, high speed digital system.
   c. There are no special requirements set forth for the loop filter resistors (1.0 MΩ and 330 Ω). The loop filter capacitor (0.1 μF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.
   d. The 1.0 M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead-band. If the VCO (2X_Q output) is running above 40 MHz, the 1.0 MΩ resistor provides the correct amount of current injection into the charge pump
      (2–3 μA). For the TFN55, 70 or 100, if the VCO is running below 40 MHz, a 1.5 MΩ reference resistor should be used (instead of 1 MΩ).
2. In addition to the bypass capacitors used in the analog filter of Figure 8, there should be a 0.1 μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88915T outputs. In addition to reducing potential for noise in the "analog" section of the chip. These bypass capacitors should also be tied as close to the 88915T package as possible.

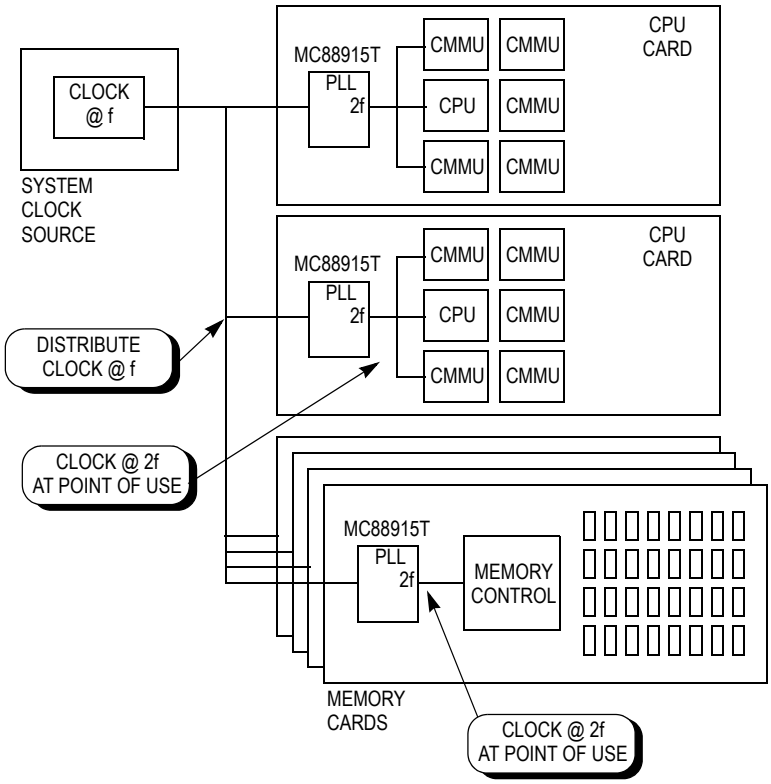


Figure 9. Representation of a Potential Multi-Processing Application Utilizing the MC88915T for Frequency Multiplication and Low Board-to-Board Skew

MC88915T System Level Testing Functionality

Three-state functionality was added to the 100 MHz version of the MC88915T to ease system board testing. Bringing the $\overline{OE}/\overline{RST}$ pin low will put all outputs (except for LOCK) into the high impedance state. As long as the PLL_EN pin is low, the Q0–Q4, $\overline{Q5}$, and the Q/2 outputs will remain in the low state after the $\overline{OE}/\overline{RST}$ until a falling SYNC edge is seen. The 2X_Q output is the inverse of the SYNC signal in this mode. If the 3-state functionality is used, a pull-up or pull-down resistor must be tied to the FEEDBACK input pin to prevent it from floating when the fed back output goes into high impedance.

With the PLL_EN pin low the selected SNC signal is gated directly into the internal clock distribution network, bypassing and disabling the VCO. In this mode the outputs are directly driven by the SYNC input (per the block diagram). This mode can also be used for low frequency board testing.

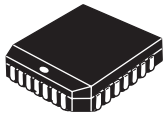
NOTE: If the outputs are put into 3-state during normal PLL operation, the loop will be broken and phase-lock will be lost. It will take a maximum of 10 ms (t_{LOCK} spec) to regain phase-lock after the $\overline{OE}/\overline{RST}$ pin goes back high.

Order number: MC88LV915T
Rev 3, 08/2001

Low Voltage Low Skew CMOS PLL Clock Driver, 3-State

MC88LV915T

LOW SKEW CMOS PLL CLOCK DRIVER



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776-02

The MC88LV915T Clock Driver utilizes phase-locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for high performance PC's and workstations.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple components on a board. The PLL also allows the MC88LV915T to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency. Multiple 88LV915's can lock onto a single reference clock, which is ideal for applications when a central system clock must be distributed synchronously to multiple boards (see Figure 6).

Five “Q” outputs (Q0-Q4) are provided with less than 500 ps skew between their rising edges. The $\overline{Q5}$ output is inverted (180° phase shift) between their rising edges. The $\overline{Q5}$ output is inverted (180° phase shift) from the “Q” outputs. The 2X_Q output runs at twice the “Q” output frequency, while the Q/2 runs at 1/2 the “Q” frequency.

The VCO is designed to run optimally between 20 MHz and the 2X_Q F_{max} specification. The wiring diagrams in detail the different feedback configurations which create specific input/output frequency relationships. Possible frequency ratios of the “Q” outputs to the SYNC input are 2:1, 1:1, and 1:2.

The FREQ_SEL pin provides one bit programmable divide-by in the feedback path of the PLL. It selects between divide-by-1 and divide-by-2 of the VCO before its signal reaches the internal clock distribution section of the chip (see Figure 2). In most applications FREQ_SEL should be held high (÷1). If a low frequency reference clock input is used, holding FREQ_SEL low (÷2) will allow the VCO to run in its optimal range (>20MHz).

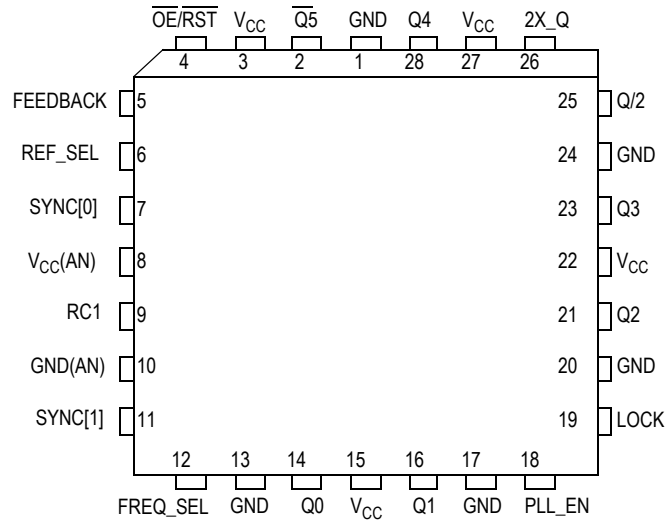
In normal phase-locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88LV915T in a static “test mode”. In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment. The second SYNC input can be used as a test clock input to further simplify board-level testing (see Applications Information for All Versions).

Pulling the $\overline{OE}/\overline{RST}$ pin low puts the clock outputs 2X_Q, Q0-Q4, $\overline{Q5}$ and Q/2 into a high impedance state (3-state). After the $\overline{OE}/\overline{RST}$ pin goes back high Q0-Q4, $\overline{Q5}$ and Q/2 will be reset in the low state, with 2X_Q being the inverse of the selected SYNC input. Assuming PLL_EN is low, the outputs will remain reset until the 88LV915 sees a SYNC input pulse.

A lock indicator output (LOCK) will go high when the loop is in steady-state phase and frequency lock. The LOCK output will go low if phase-lock is lost or when the PLL_EN pin is low. The LOCK output will go high no later than 10ms after the 88LV915 sees a SYNC signal and full 5V V_{CC}.

Features

- Five Outputs (Q0-Q4) with Output-Output Skew < 500 ps each being phase and frequency locked to the SYNC input
- The phase variation from part-to-part between the SYNC and FEEDBACK inputs is less than 550 ps (derived from the t_{PD} specification, which defines the part-to-part skew)
- Input/Output phase-locked frequency ratios of 1:2, 1:1, and 2:1 are available
- Input frequency range from 5MHz - 2X_Q FMAX spec.
- Additional outputs available at 2X and +2 the system “Q” frequency. Also a $\overline{Q}$ (180° phase shift) output available
- All outputs have ±36 mA drive (equal high and low) at CMOS levels, and can drive either CMOS or TTL inputs. All inputs are TTL-level compatible. ±88mA I_{OL}/I_{OH} specifications guarantee 50Ω transmission line switching on the incident edge
- Test Mode pin (PLL_EN) provided for low frequency testing. Two selectable CLOCK inputs for test or redundancy purposes. All outputs can go into high impedance (3-state) for board test purposes
- Lock Indicator (LOCK) accuracy indicates a phase-locked state



FN SUFFIX
PLASTIC PLCC
CASE 776–02

Figure 1. Pinout: 28-Lead PLCC (Top View)

Table 1. Pin Summary

Pin Name	Number	I/O	Function
SYNC[0]	1	Input	Reference clock input
SYNC[1]	1	Input	Reference clock input
REF_SEL	1	Input	Chooses reference between SYNC[0] and SYNC[1]
FREQ_SEL	1	Input	Doubles VCO Internal Frequency (low)
FEEDBACK	1	Input	Feedback input to phase detector
RC1	1	Input	Input for external RC network
Q(0-4)	5	Output	Clock output (locked to SYNC)
$\overline{Q5}$	1	Output	Inverse of clock output
2X_Q	1	Output	2 x clock output (Q) frequency (synchronous)
Q/2	1	Output	Indicates phase lock has been achieved (high when locked)
LOCK	1	Output	Output Enable/Asynchronous reset (active low)
$\overline{OE}/\overline{RST}$	1	Input	Disables phase-lock for low frequency testing
PLL_EN	1	Input	Power and ground pins (NOTE: Pins 8 and 10 are “analog” supply pins for internal PLL only)
V_{CC}, GND	11		

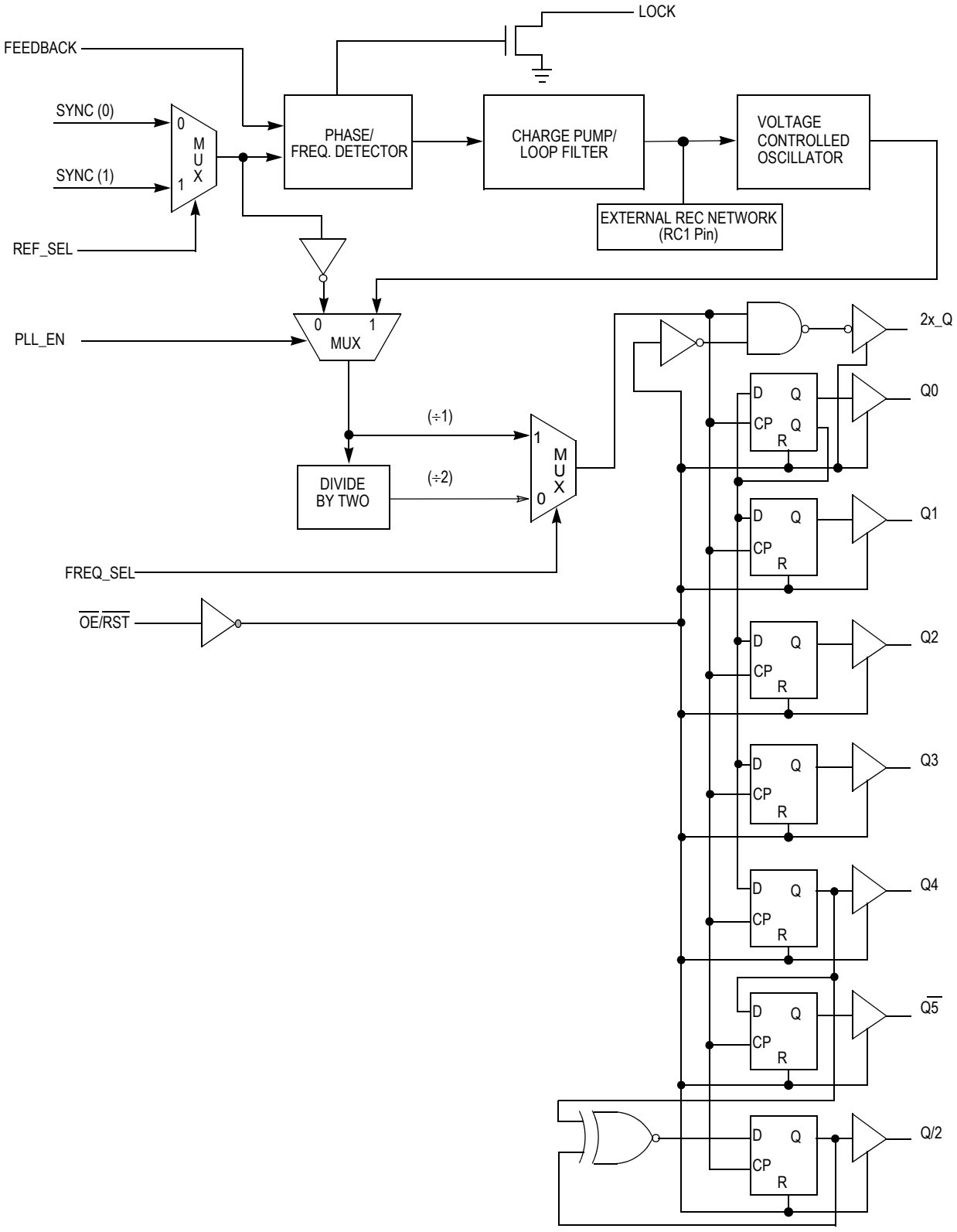


Figure 2. MC88LV915T Block Diagram

Table 2. Maximum Ratings[1]

Symbol	Parameter	Limits	Unit
V_{CC}, AV_{CC}	DC Supply Voltage Referenced to GND	-0.5 to 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, Per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, Per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current Per Output Pin	±50	mA
T_{stg}	Storage Temperature	-65 to +150	°C

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Table 3. Recommended Operating Conditions

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	3.3 ±0.3	V
V_{in}	DC Input Voltage	0 to V_{CC}	V
V_{out}	DC Output Voltage	0 to V_{CC}	V
T_A	Ambient Operating Temperature	0 to 70	°C
ESD	Static Discharge Voltage	> 1000	V

Table 4. DC Characteristics (T_A = 0°C to 70°C; V_{CC} = 3.3 V ± 0.3 V)

Symbol	Parameter	V_{CC}	Guaranteed Limits	Unit	Condition
V_{IH}	Minimum High Level Input Voltage	3.0 3.3	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} - 0.1 V
V_{IL}	Minimum Low Level Input Voltage	3.0 3.3	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} - 0.1 V
V_{OH}	Minimum High Level Output Voltage	3.0 3.3	2.4 2.7	V	V_{IN} = V_{IH} or V_{IL} I_{OH}= -24 mA
V_{OL}	Minimum Low Level Output Voltage	3.0 3.3	0.44 0.44	V	V_{IN} = V_{IH} or V_{IL} I_{OH}= 24 mA
I_{IN}	Maximum Input Leakage Current	3.6	±1.0	μA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	3.6	2.0	mA	V_I = V_{CC} - 2.1 V
I_{OLD}	Minimum Dynamic[3] Output Current	3.6	+50	mA	V_{OLD} = 1.25 V
I_{OHD}		3.6	-50	mA	V_{OHD} =2.35 V
I_{CC}	Maximum Quiescent Supply Current	3.6	TBD	μA	V_I = V_{CC}, GND

1. I_{OL} is +12 mA for the $\overline{RST}$_$\overline{OUT}$ output.
2. The PLL_EN input pin is not guaranteed to meet this specification.
3. Maximum test duration 2.0 ms, one output loaded at a time.

Table 5. SYNC Input Timing Requirements

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$ SYNC Input	Rise/Fall Time, SYNC Input From 0.8 V to 2.0 V	–	5.0	ns
t_{CYCLE}, SYNC Input	Input Clock Period SYNC Input	1 f_{2X_Q}/4	100	ns
Duty Cycle	Duty Cycle, SYNC Input	50% ± 25%		

Table 6. Frequency Specifications (T_A = 0°C to 70°C; V_{CC} = 3.3 V ± 0.3 V)

Symbol	Parameter	Guaranteed Minimum	Unit
Fmax (2X_Q)	Maximum Operating Frequency, 2X_Q Output	100	MHz
Fmax ('Q')	Maximum Operating Frequency, Q0-Q3 Outputs	50	MHz

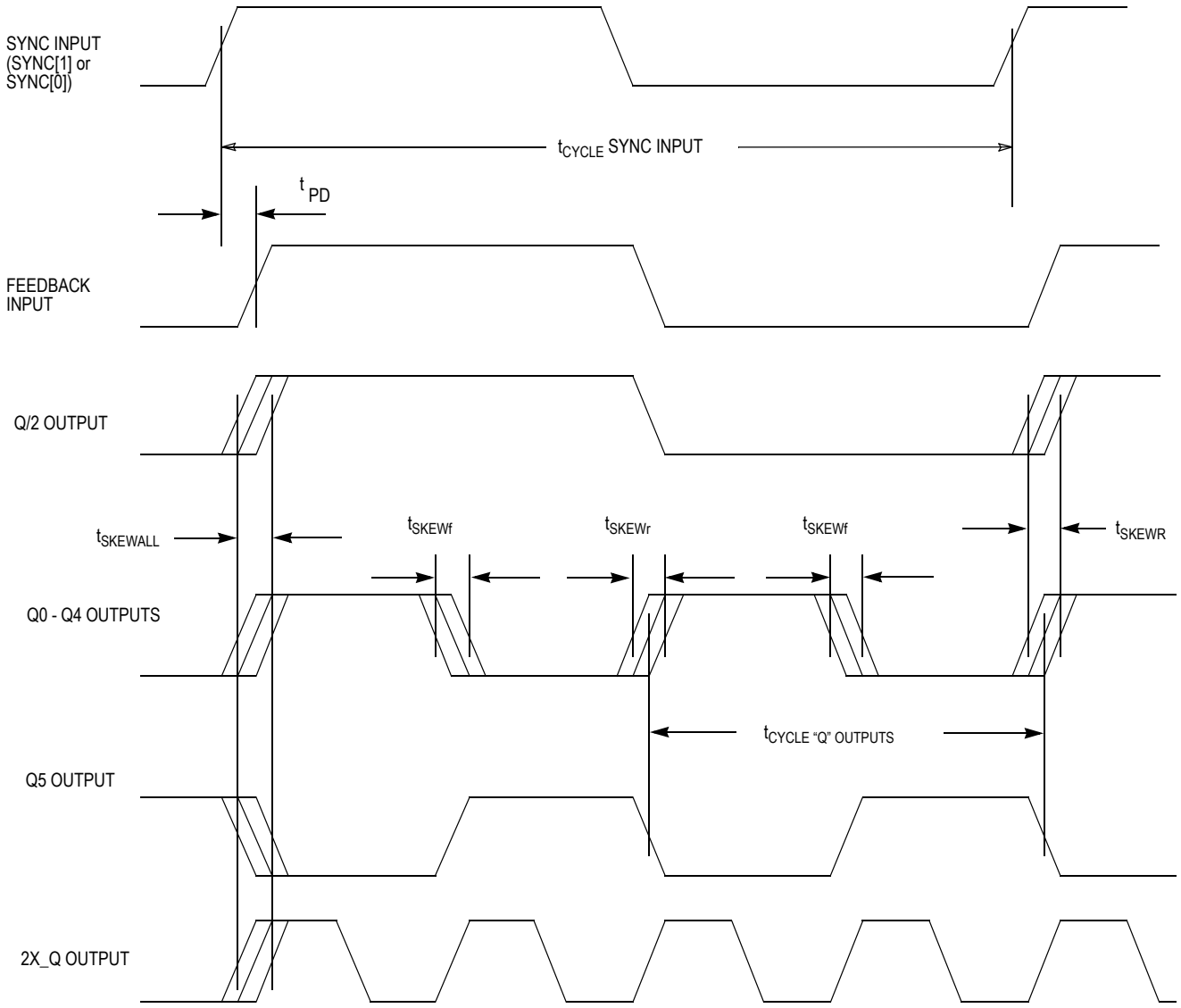
NOTE: Maximum Operating Frequency is guaranteed with the 88LV926 in a phase-locked condition.

Table 7. AC Characteristics (T_A = 0° C to +70° C, V_{CC} = 3.3 V ± 0.3 V, Load = 50 Ω Terminated to $V_{CC}/2$)

Symbol	Parameter	Min	Max	Unit	Condition
$t_{RISE/FALL}$ Outputs	Rise/Fall Time, All Outputs (Between 0.8 to 2.0 V)	0.5	2.0	ns	Into a 50 Ω Load Terminated to $V_{CC}/2$
$t_{PULSE\ WIDTH}$ (Q0-Q4, $\overline{Q5}$, Q/2)	Output Pulse Width: Q0, Q1, Q2, Q3, Q4, $\overline{Q5}$, Q/2 @ $V_{CC}/2$	0.5 t_{CYCLE} - 0.5[1]	0.5 t_{CYCLE} + 0.5[1]	ns	Into a 50 Ω Load Terminated to $V_{CC}/2$
$t_{PULSE\ WIDTH}$ (2X_Q Output)	Output Pulse Width: 2X_Q @ 1.5 V 40 MHz 66 MHz 80 MHz 100 MHz	0.5 t_{CYCLE} - 1.5 0.5 t_{CYCLE} - 1.0 0.5 t_{CYCLE} - 1.0 0.5 t_{CYCLE} - 1.0	0.5 t_{CYCLE} + 0.5 0.5 t_{CYCLE} + 0.5 0.5 t_{CYCLE} + 0.5 0.5 t_{CYCLE} + 0.5	ns	Into a 50 Ω Load Terminated to $V_{CC}/2$
t_{CYCLE}[1] (2x_Q Output)	Cycle-to-Cycle Variation 2x_Q @ $V_{CC}/2$ 40MHz 66 MHz 80 MHz 100 MHz	t_{CYCLE} - 600ps t_{CYCLE} - 300ps t_{CYCLE} - 300ps t_{CYCLE} - 400ps	t_{CYCLE} + 600ps t_{CYCLE} + 300ps t_{CYCLE} + 300ps t_{CYCLE} + 400ps		
t_{PD}[2] SYNC Feedback		(With 1 MΩ from RC1 to An V_{CC})		ns	
	SYNC Input to Feedback Delay 66 MHz (Measured at SYNC0 or 1 and 80 MHz FEEDBACK Input Pins) 100 MHz	-1.65 -1.45 -1.25	-1.05 -0.85 -0.65		
t_{SKEWr}[3] (Rising) See Note 4	Output-to-Output Skew Between Outputs Q0-Q4, Q/2 (Rising Edges Only)	—	500	ps	All Outputs Into a Matched 50 Ω Load Terminated to $V_{CC}/2$
t_{SKEWf}[3] (Falling)	Output-to-Output Skew Between Outputs Q0-Q4 (Falling Edges Only)	—	750	ps	All Outputs Into a Matched 50 Ω Load Terminated to $V_{CC}/2$
$t_{SKEWall}$[3]	Output-to-Output Skew 2X_Q, Q/2, Q0-Q4 Rising, $\overline{Q5}$ Falling	—	750	ps	All Outputs Into a Matched 50 Ω Load Terminated to $V_{CC}/2$
t_{LOCK}[4]	Time Required to Acquire Phase-Lock From Time SYNC Input Signal is Received	1.0	10	ms	Also Time to LOCK Indicator High
t_{PZL}[5]	Output Enable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0-Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low
t_{PHZ},t_{PLZ}[5]	Output Disable Time $\overline{OE}/\overline{RST}$ to 2X_Q, Q0-Q4, $\overline{Q5}$, and Q/2	3.0	14	ns	Measured With the PLL_EN Pin Low

1. t_{CYCLE} in this spec is 1/Frequency at which the particular output is running.
2. The t_{PD} specification's min/max values may shift closer to zero if a larger pullup resistor is used.
3. Under equally loaded conditions and at a fixed temperature and voltage.
4. With V_{CC} fully powered-on, and an output properly connected to the FEEDBACK pin. t_{LOCK} maximum is with C1 = 0.1 μF, t_{LOCK} minimum is with C1 = 0.01 μF.
5. The t_{PZL}, t_{PHZ}, t_{PLZ} minimum and maximum specifications are estimates, the final guaranteed values will be available when 'MC' status is reached.

APPLICATIONS INFORMATION FOR ALL VERSIONS

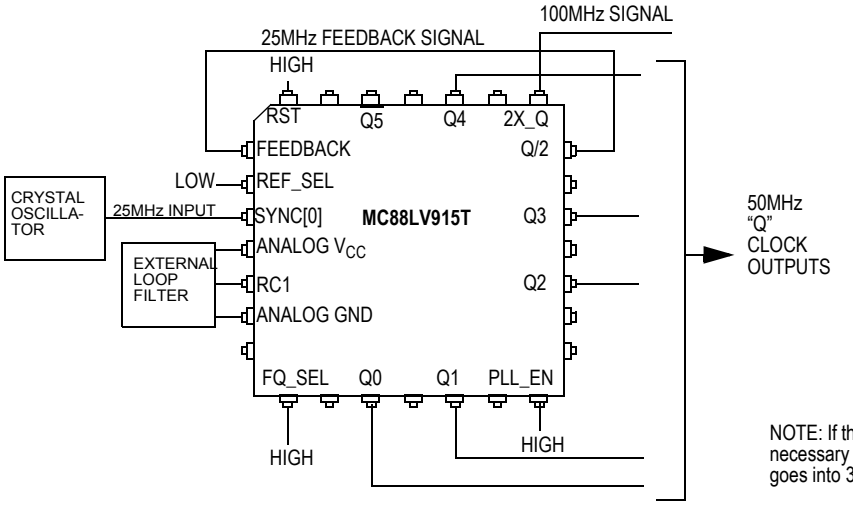


(These waveforms represent the hook-up configuration of Figure 4a)

Timing Notes:

1. The MC88LV915T aligns rising edges of the FEEDBACK input and SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges. All skews are specified as 'windows', not as a ± deviation around a center point.
3. If a "Q" output is connected to the FEEDBACK input (this situation is not shown), the "Q" output frequency would match the SYNC input frequency, the 2X_Q output would run at twice the SYNC frequency, and the Q/2 output would run at half the SYNC frequency.

Figure 3. Output/Input Switching Waveforms and Timing Diagrams

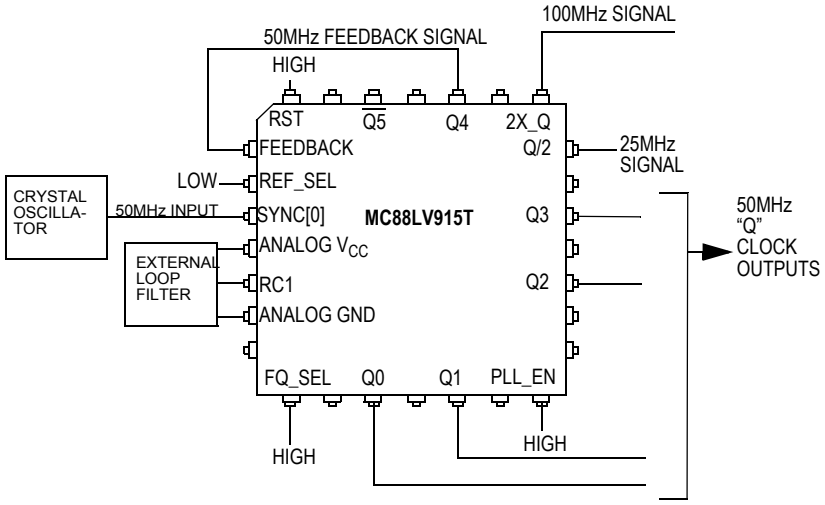


1:2 Input to "Q" Output Frequency Relationship
In this application, the Q/2 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q/2 and SYNC, thus the Q/2 frequency will equal the SYNC frequency. The "Q" outputs (Q0-Q4, Q5) will always run at 2X the Q/2 frequency, and the 2X_Q output will run at 4X the Q/2 frequency.

Allowable Input Frequency Range:
5MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL HIGH)
2.5MHz to (2X_Q FMAX Spec)/8 (for FREQ_SEL LOW)

NOTE: If the $\overline{OE}$/$\overline{RST}$ input is active, a pull-up or pull-down resistor isn't necessary at the FEEDBACK pin so it won't when the fed back output goes into 3-state.

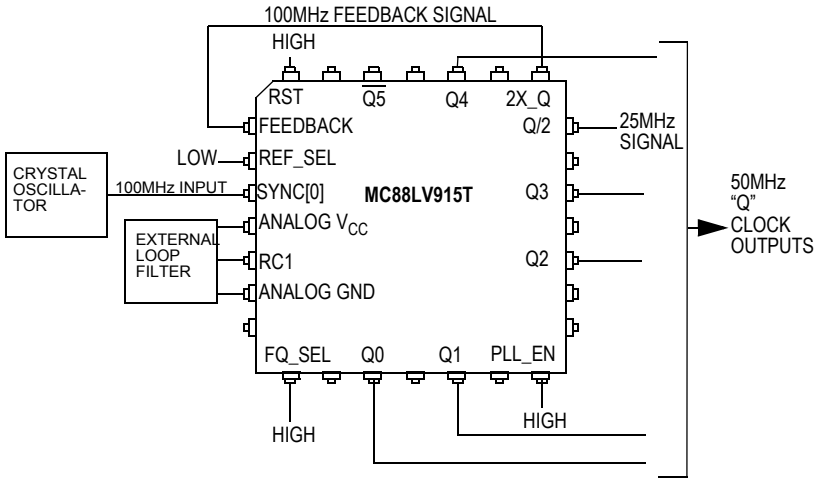
Figure 4a. Wiring Diagram and Frequency Relationships with Q/2 Output Feedback



1:1 Input to "Q" Output Frequency Relationship
In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the "Q" frequency, and the 2X_Q output will run at 2X the "Q" frequency.

Allowable Input Frequency Range:
10MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL HIGH)
5MHz to (2X_Q FMAX Spec)/4 (for FREQ_SEL LOW)

Figure 4b. Wiring Diagram and Frequency Relationships with Q4 Output Feedback



2:1 Input to "Q" Output Frequency Relationship
In this application, the Q4 output is connected to the FEEDBACK input. The internal PLL will line up the positive edges of Q4 and SYNC, thus the Q4 frequency (and the rest of the "Q" outputs) will equal the SYNC frequency. The Q/2 output will always run at 1/2 the "Q" frequency, and the 2X_Q output will run at 2X the "Q" frequency.

Allowable Input Frequency Range:

20MHz to (2X_Q FMAX Spec) (for FREQ_SEL HIGH)
10MHz to (2X_Q FMAX Spec)/2 (for FREQ_SEL LOW)

Figure 4c. Wiring Diagram and Frequency Relationships with 2X_Q Output Feedback

Figure 4. Wiring Diagrams

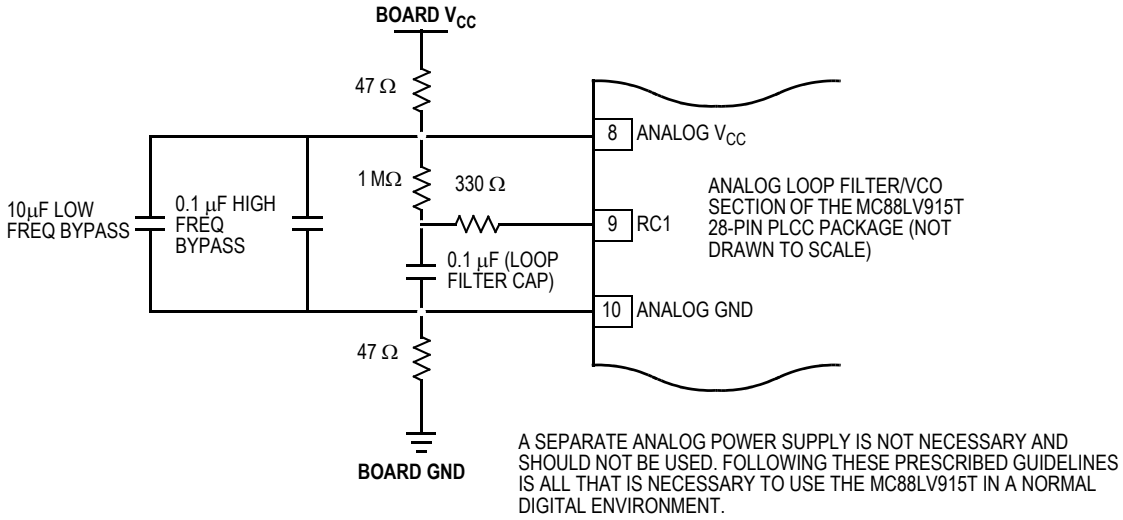


Figure 5. Recommended Loop Filter and Analog Isolation Scheme for the MC88LV915T

NOTES CONCERNING LOOP FILTER AND BOARD LAYOUT ISSUES

1. Figure 5 shows a loop filter and analog isolation scheme, effective in most applications. The following guidelines should be followed ensuring stable and jitter-free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47 Ω resistors, the 10 μF low frequency bypass capacitor, and the 0.1 μF high frequency bypass capacitor form a wide bandwidth filter that will minimize the 88LV915T's sensitivity to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100pS phase deviation on the 88LV915T outputs. A 250mV step deviation on V_{CC} using the recommended filter values should cause no more than a 250pS phase deviation; if a 25 μF bypass capacitor is used (instead of 10 μF) a 250 mV V_{CC} step should cause no more than a 100 pS phase deviation.

If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88LV915T's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 5 is to give the 88LV915T additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (1 MΩ and 330 Ω). The loop filter capacitor (0.1 μF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 1 M reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead-band. If the VCO (2X_Q output) is running above 40 MHz, the 1 MΩ resistor provides the correct amount of current injection into the charge pump (2-3 μA). For the TFN55, 70 or 100, if the VCO is running below 40 MHz, a 1.5 MΩ reference resistor should be used (instead of 1 MΩ).

2. In addition to the bypass capacitors used in the analog filter of Figure 5, there should be a 0.1 μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88LV915T outputs, in addition to reducing potential for noise in the ‘analog' section of the chip. These bypass capacitors should also be tied as close to the 88LV915T package as possible.

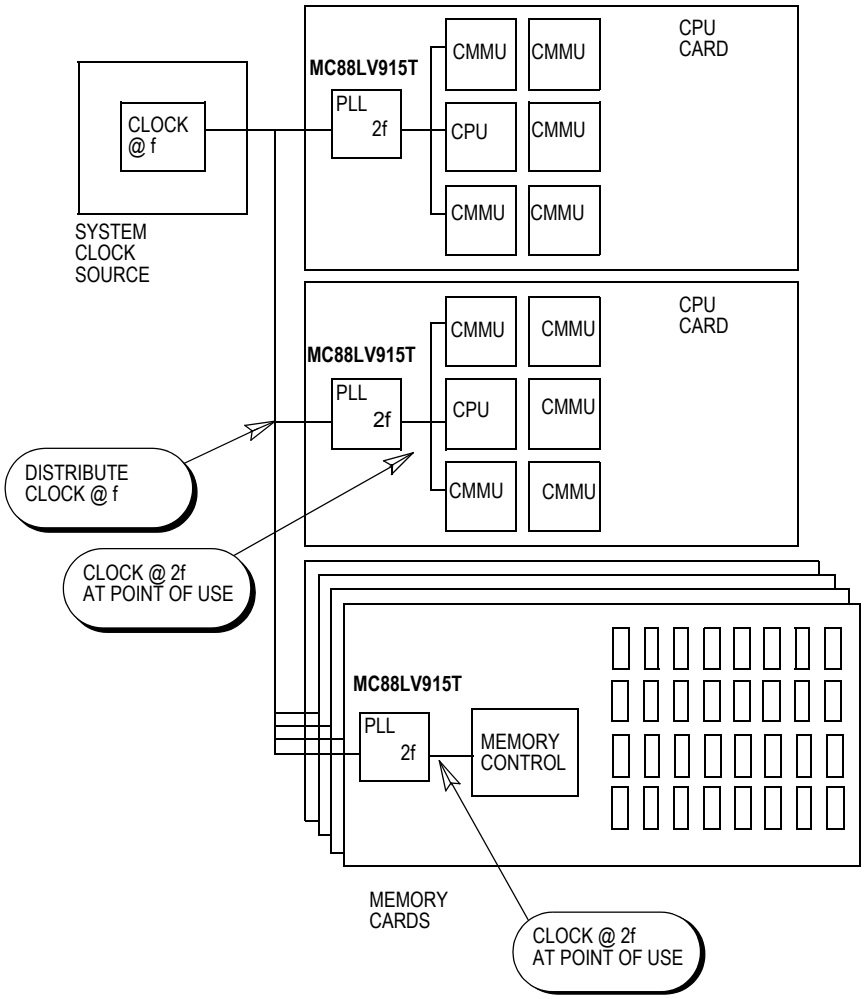


Figure 6. Representation of a Potential Multi-Processing Application Utilizing the MC88LV915T for Frequency Multiplication and Low Board-to-Board Skew

MC88LV915T SYSTEM LEVEL TESTING FUNCTIONALITY

Three-state functionality has been added to the 100 MHz version of the MC88LV915T to ease system board testing. Bringing the $\overline{OE}/\overline{RST}$ pin low will put all outputs (except for LOCK) into the high impedance state. As long as the PLL_EN pin is low, the Q0-Q4, Q5, and the Q/2 outputs will remain reset in the low state after the $\overline{OE}/\overline{RST}$ until a falling SYNC edge is seen. The 2X_Q output will be the inverse of the SYNC signal in this mode. If the 3-state functionality will be used, a pull-up or pull-down resistor must be tied to the FEEDBACK input pin to prevent it from floating when the feedback output goes into high impedance.

With the PLL_EN pin low the selected SYNC signal is gated directly into the internal clock distribution network, bypassing and disabling the VCO. In this mode the outputs are directly driven by the SYNC input (per the block diagram). This mode can also be used for low frequency board testing.

Note: If the outputs are put into 3-state during normal PLL operation, the loop will be broken and phase-lock will be lost. It will take a maximum of 10 mS (t_{LOCK} spec) to regain phase-lock after the $\overline{OE}/\overline{RST}$ pin goes back high.

Order number: MC88LV926
Rev 5, 08/2004

Low Skew CMOS PLL 68060 Clock Driver

MC88LV926

LOW SKEW CMOS PLL
68080 CLOCK DRIVER

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751D-06

The MC88LV926 Clock Driver utilizes phase-locked loop technology to lock its low skew outputs' frequency and phase onto an input reference clock. It is designed to provide clock distribution for CISC microprocessor or single processor RISC systems. The $\overline{\text{RST}}\_\overline{\text{IN}}/\overline{\text{RST}}\_\overline{\text{OUT}}$(LOCK) pins provide a processor reset function designed specifically for the MC68/EC/LC030/040/060 microprocessor family. To support the 68060 processor, the 88LV926 operates from a 3.3 V as well as a 5.0 V supply.

The PLL allows the high current, low skew outputs to lock onto a single clock input and distribute it with essentially zero delay to multiple locations on a board. The PLL also allows the MC88LV926 to multiply a low frequency input clock and distribute it locally at a higher (2X) system frequency.

Features

- 2X_Q Output Meets All Requirements of the 50 and 66 MHz 68060 Microprocessor PCLK Input Specifications
- Low Voltage 3.3 V V_{CC}
- Three Outputs (Q0–Q2) With Output–Output Skew <500 ps
- $\overline{\text{CLKEN}}$ Output for Half Speed Bus Applications
- The Phase Variation From Part—to—Part Between SYNC and the ‘Q' Outputs Is Less Than 600 ps (Derived From the T_{PD} Specification, Which Defines the Part–to–Part Skew)
- SYNC Input Frequency Range From 5.0 MHz to 2X_Q F_{Max}/4
- All Outputs Have ± 36 mA Drive (Equal High and Low) CMOS Levels
- Can Drive Either CMOS or TTL Inputs. All Inputs Are TTL—Level Compatible with V_{CC} = 3.3 V
- Test Mode Pin (PLL_EN) Provided for Low Frequency Testing

Three ‘Q' outputs (Q0–Q2) are provided with less than 500ps skew between their rising edges. A 2X_Q output runs at twice the ‘Q' output frequency. The 2X_Q output is ideal for 68060 systems which require a 2X processor clock input, and it meets the tight duty cycle spec of the 50 and 66MHz 68060. The QCLKEN output is designed to drive the $\overline{\text{CLKEN}}$ input of the 68060 when the bus logic runs at half of the microprocessor clock rate. The QCLKEN output is skewed relative to the 2X_Q output to ensure that $\overline{\text{CLKEN}}$ setup and hold times of the 68060 are satisfied. A Q/2 frequency is fed back internally, providing a fixed 2X multiplication from the ‘Q' outputs to the SYNC input. Since the feedback is done internally (no external feedback pin is provided) the input/output frequency relationships are fixed. The $\overline{\text{Q3}}$ output provides an inverted clock output to allow flexibility in the clock tree design.

In normal phase–locked operation the PLL_EN pin is held high. Pulling the PLL_EN pin low disables the VCO and puts the 88LV926 in a static ‘test mode'. In this mode there is no frequency limitation on the input clock, which is necessary for a low frequency board test environment.

The $\overline{\text{RST}}\_\overline{\text{OUT}}$(LOCK) pin doubles as a phase–lock indicator. When the $\overline{\text{RST}}\_\overline{\text{IN}}$ pin is held high, the open drain $\overline{\text{RST}}\_\overline{\text{OUT}}$ pin will be pulled actively low until phase–lock is achieved. When phase–lock occurs, the $\overline{\text{RST}}\_\overline{\text{OUT}}$(LOCK) is released and a pull–up resistor will pull the signal high. To give a processor reset signal, the RST_IN pin is toggled low, and the $\overline{\text{RST}}\_\overline{\text{OUT}}$(LOCK) pin will stay low for 1024 cycles of the ‘Q' output frequency after the $\overline{\text{RST}}\_\overline{\text{IN}}$ pin is brought back high.

Description of the $\overline{\text{RST}}\_\overline{\text{IN}}/\overline{\text{RST}}\_\overline{\text{OUT}}$(LOCK) Functionality

The $\overline{\text{RST}}\_\overline{\text{IN}}$ and $\overline{\text{RST}}\_\overline{\text{OUT}}$(LOCK) pins provide a 68030/040/060 processor reset function, with the $\overline{\text{RST}}\_\overline{\text{OUT}}$ pin also acting as a lock indicator. If the $\overline{\text{RST}}\_\overline{\text{IN}}$ pin is held high during system power–up, the $\overline{\text{RST}}\_\overline{\text{OUT}}$ pin will be in the low state until steady state phase/frequency lock to the input reference is achieved. 1024 ‘Q' output cycles after phase–lock is achieved the $\overline{\text{RST}}\_\overline{\text{OUT}}$(LOCK) pin will go into a high impedance state, allowing it to be pulled high by an external pull–up resistor (see the AC/DC specs for the characteristics of the $\overline{\text{RST}}\_\overline{\text{OUT}}$(LOCK) pin). If the $\overline{\text{RST}}\_\overline{\text{IN}}$ pin is held low during power–up, the $\overline{\text{RST}}\_\overline{\text{OUT}}$(LOCK) pin will remain low.

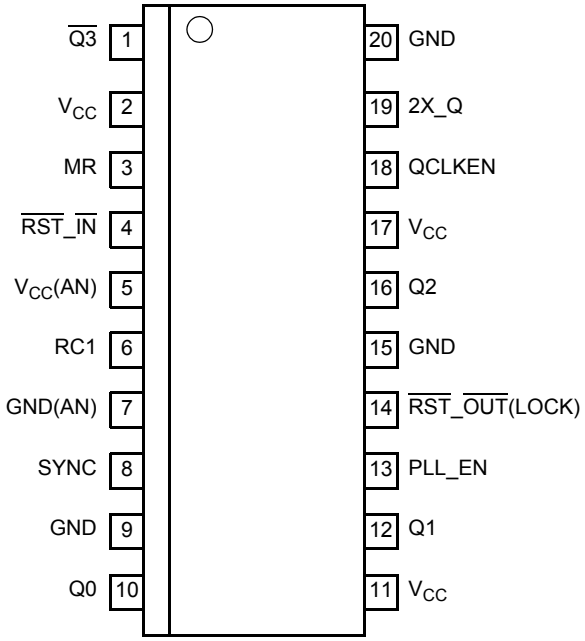


Figure 1. Pinout: 20–Lead Wide SOIC Package (Top View)

Description of the RST_IN/RST_OUT(LOCK) Functionality (continued)

After the system start–up is complete and the 88LV926 is phase–locked to the SYNC input signal (RST_OUT high), the processor reset functionality can be utilized. When the RST_IN pin is toggled low (min. pulse width=10nS), RST_OUT(LOCK) will go to the low state and remain there for 1024 cycles of the 'Q' output frequency (512 SYNC cycles). During the time in which the RST_OUT(LOCK) is actively pulled low, all the 88LV926 clock outputs will continue operating correctly and in a locked condition to the SYNC input (clock signals to the 68030/040/060 family of processors must continue while the processor is in reset). A propagation delay after the 1024th cycle RST_OUT(LOCK) goes back to the high impedance state to be pulled high by the resistor.

Power Supply Ramp Rate Restriction for Correct 030/040 Processor Reset Operation During System Start-up

Because the RST_OUT(LOCK) pin is an indicator of phase-lock to the reference source, some constraints must be placed on the power supply ramp rate to make sure the RST_OUT(LOCK) signal holds the processor in reset during system start-up (power–up). With the recommended loop filter values (see Figure 7) the lock time is approximately 10ms. The phase–lock loop will begin attempting to lock to a reference source (if it is present) when V_{CC} reaches 2V. If the V_{CC} ramp rate is significantly slower than 10ms, then the PLL could lock to the reference source, causing RST_OUT(LOCK) to go high before the 88LV926 and '030/040 processor is fully powered up, violating the processor reset specification. Therefore, if it is necessary for the RST_IN pin to be held high during power-up, the V_{CC} ramp rate must be less than 10mS for proper 68030/040/060 reset operation.

This ramp rate restriction can be ignored if the RST_IN pin can be held low during system start-up (which holds RST_OUT low). The RST_OUT(LOCK) pin will then be pulled back high 1024 cycles after the RST_IN pin goes high.

Table 1. Capacitance and Power Specifications

Symbol	Parameter	Value Type	Unit	Test Conditions
C_{IN}	Input Capacitance	4.5[1]	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	40[1]	pF	V_{CC} = 5.0V
PD_1	Power Dissipation at 33MHz With 50Ω Thevenin Termination	15mW/Output[1] 90mW/Device	mW	V_{CC} = 5.0V T = 25°C
PD_2	Power Dissipation at 33MHz With 50Ω Parallel Termination to GND	37.5mW/Output[1] 225mW/Device	mW	V_{CC} = 5.0V T = 25°C

1. Value at V_{CC} = 3.3 V TBD

Table 2. Maximum Ratings[1]

Symbol	Parameter	Limits	Unit
V_{CC}, AV_{CC}	DC Supply Voltage Referenced to GND	–0.5 to 7.0	V
V_{in}	DC Input Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
V_{out}	DC Output Voltage (Referenced to GND)	–0.5 to V_{CC} +0.5	V
I_{in}	DC Input Current, Per Pin	±20	mA
I_{out}	DC Output Sink/Source Current, Per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current Per Output Pin	±50	mA
T_{stg}	Storage Temperature	–65 to +150	°C

1. Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Table 3. Recommended Operating Conditions

Symbol	Parameter	Limits	Unit
V_{CC}	Supply Voltage	3.3 ±0.3	V
V_{in}	DC Input Voltage	0 to V_{CC}	V
V_{out}	DC Output Voltage	0 to V_{CC}	V
T_A	Ambient Operating Temperature	0 to 70	°C
ESD	Static Discharge Voltage	> 1500	V

Table 4. DC Characteristics (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V)[1]

Symbol	Parameter	V_{CC}	Guaranteed Limits	Unit	Condition
V_{IH}	Minimum High Level Input Voltage[1]	3.0 3.3	2.0 2.0	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{IL}	Minimum Low Level Input Voltage	3.0 3.3	0.8 0.8	V	V_{OUT} = 0.1V or V_{CC} – 0.1V
V_{OH}	Minimum High Level Output Voltage	3.0 3.3	2.2 2.5	V	V_{IN} = V_{IH} or V_{IL} = –24mA I_{OH} = –24mA
V_{OL}	Minimum Low Level Output Voltage	3.0 3.3	0.55 0.55	V	V_{IN} = V_{IH} or V_{IL} = +24mA[2] I_{OH} = +24mA
I_{IN}	Maximum Input Leakage Current	3.3	±1.0	µA	V_I = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	3.3	2.0[3]	mA	V_I = V_{CC} – 2.1V
I_{OLD}	Minimum Dynamic[4] Output Current	3.3	50	mA	V_{OLD} = 1.25V Max
I_{OHD}		3.3	–50	mA	V_{OHD} = 2.35 Min
I_{CC}	Maximum Quiescent Supply Current	3.3	750	µA	V_I = V_{CC}, GND

1. The MC88LV926 can also be operated from a 5.0V supply. V_{OH} output levels will vary 1:1 with V_{CC}, input levels and current specs will be unchanged, except $V_{IH;}$ when V_{CC} > 4.0 volts, V_{IH} minimum level is 2.7 volts.
2. I_{OL} is +12mA for the $\overline{RST}$_$\overline{OUT}$ output.
3. Maximum test duration 2.0ms, one output loaded at a time.
4. The PLL_EN input pin is not guaranteed to meet this specification.

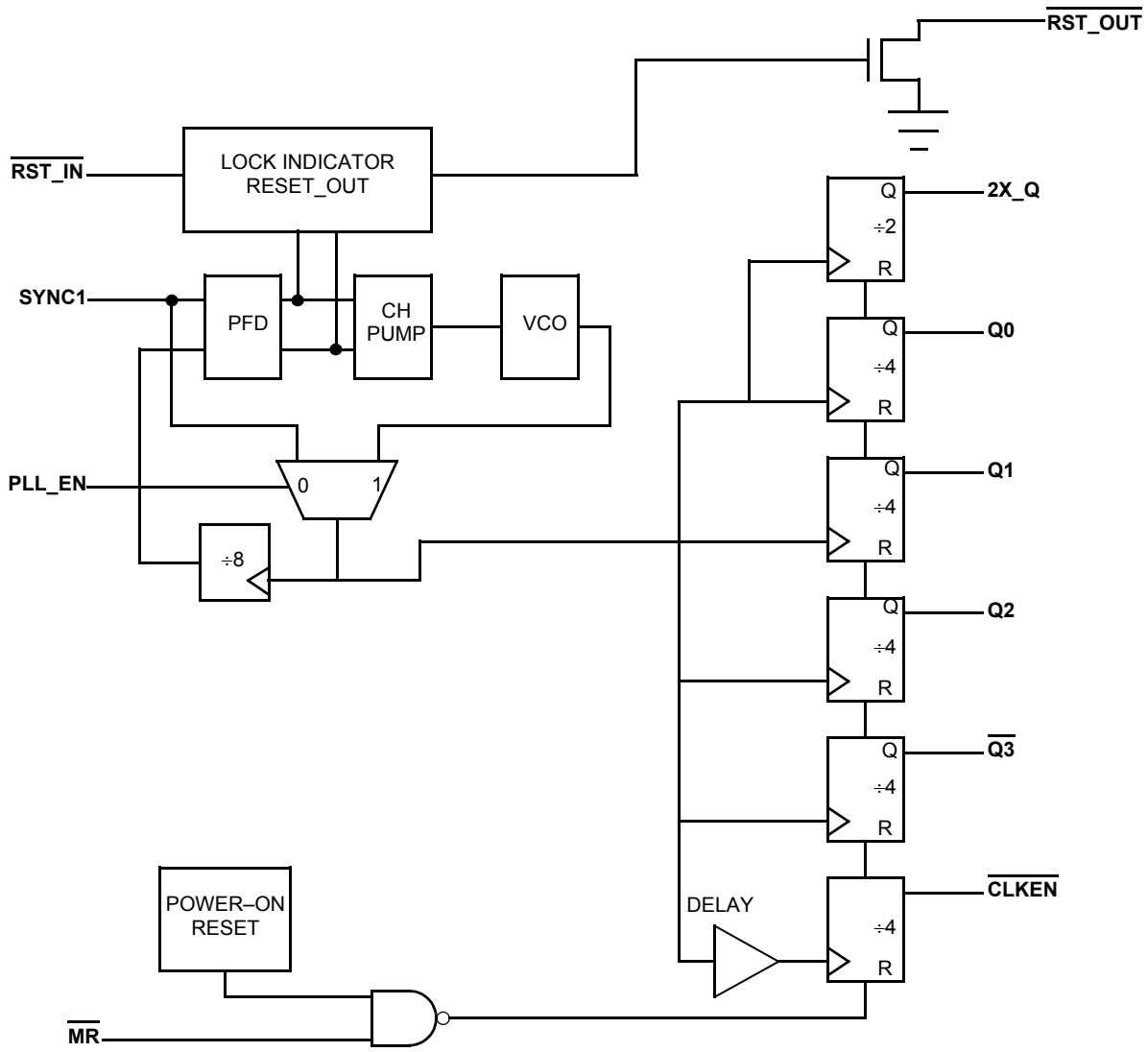


Figure 2. MC88LV926 Logic Block Diagram

Table 5. Sync Input Timing Requirements

Symbol	Parameter	Minimum	Maximum	Unit
$t_{RISE/FALL}$ SYNC Input	Rise/Fall Time, SYNC Input From 0.8V to 2.0V	–	5.0	ns
t_{CYCLE}, SYNC Input	Input Clock Period SYNC Input[1]	1 $f_{2X\_Q}/4$	200[1]	ns
Duty Cycle	Duty Cycle, SYNC Input	50% ± 25%		

1. When V_{CC} > 4.0 volts, Maximum SYNC Input Period is 125ns.

Table 6. Frequency Specifications (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V or 5.0V ±5%)

Symbol	Parameter	Guaranteed Minimum	Unit
Fmax (2X_Q)	Maximum Operating Frequency, 2X_Q Output	66	MHz
Fmax ('Q')	Maximum Operating Frequency, Q0–Q3 Outputs	33	MHz

NOTE: Maximum Operating Frequency is guaranteed with the 88LV926 in a phase–locked condition.

Table 7. AC Characteristics (T_A = 0°C to 70°C; V_{CC} = 3.3V ± 0.3V or 5.0V ±5%)

Symbol	Parameter	Minimum	Maximum	Unit	Condition
$t_{RISE/FALL}$ All Outputs	Rise/Fall Time, into 50Ω Load	0.3	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{RISE/FALL}$ 2X_Q Output	Rise/Fall Time into a 50Ω Load	0.5	1.6	ns	t_{RISE} – 0.8V to 2.0V t_{FALL} – 2.0V to 0.8V
$t_{pulse\ width(a)}$[1] (Q0, Q1, Q2, $\overline{Q3}$)	Output Pulse Width Q0, Q1, Q2, Q3 at 1.65V	$0.5t_{cycle}$ – 0.5	$0.5t_{cycle}$ + 0.5	ns	50Ω Load Terminated to V_{CC}/2 (See Application Note 3)
$t_{pulse\ width(b)}$[1] (2X_Q Output)	Output Pulse Width 2X_Q at 1.65V	$0.5t_{cycle}$ – 0.5	$0.5t_{cycle}$ + 0.5	ns	50Ω Load Terminated to V_{CC}/2 (See Application Note 3)
t_{SKEWr}[2] (Rising)	Output–to–Output Skew Between Outputs Q0–Q2 (Rising Edge Only)	–	500	ps	Into a 50Ω Load Terminated to V_{CC}/2 (See Timing Diagram in Figure 6)
t_{SKEWf}[2] (Falling)	Output–to–Output Skew Between Outputs Q0–Q2 (Falling Edge Only)	–	1.0	ns	Into a 50Ω Load Terminated to V_{CC}/2 (See Timing Diagram in Figure 6)
$t_{SKEWall}$[2]	Output–to–Output Skew 2X_Q, Q0–Q2, $\overline{Q3}$	–	750	ps	Into a 50Ω Load Terminated to V_{CC}/2 (See Timing Diagram in Figure 6)
t_{SKEW} QCLKEN[1,2]	Output–to–Output Skew $\overline{QCLKEN}$ to 2X_Q 2X_Q = 50MHz 2X_Q = 66MHz	9.7[6] 7.0[6]	–	ns	Into a 50Ω Load Terminated to V_{CC}/2 (See Timing Diagram in Figure 6)
t_{LOCK}[3]	Phase–Lock Acquisition Time, All Outputs to SYNC Input	1	10	ms	
t_{PHL} $\overline{MR}$ – Q[1]	Propagation Delay, $\overline{MR}$ to Any Output (High–Low)	1.5	13.5	ns	Into a 50Ω Load Terminated to V_{CC}/2
t_{REC}, $\overline{MR}$ to SYNC[5, 1]	Reset Recovery Time rising $\overline{MR}$ edge to falling SYNC edge	9	–	ns	
t_W, $\overline{MR}$ LOW[5, 1]	Minimum Pulse Width, $\overline{MR}$ input Low	5	–	ns	
t_W, $\overline{RST\_IN}$ LOW[1]	Minimum Pulse Width, $\overline{RST\_IN}$ Low	10	–	ns	When in Phase–Lock
t_{PZL}[1]	Output Enable Time $\overline{RST\_IN}$ Low to $\overline{RST\_OUT}$ Low	1.5	16.5	ns	See Application Note 5
t_{PLZ}[1]	Output Enable Time $\overline{RST\_IN}$ High to $\overline{RST\_OUT}$ High Z	1016 'Q' Cycles (508 Q/2 Cycles)	1024 'Q' Cycles (512 Q/2 Cycles)	ns	See Application Note 5

1. These specifications are not tested, they are guaranteed by statistical characterization. See Application Note 1 for a discussion of this methodology.
2. Under equally loaded conditions and at a fixed temperature and voltage.
3. With V_{CC} fully powered–on: t_{CLOCK} Max is with C1 = 0.1μF; t_{LOCK} Min is with C1 = 0.01μF.
4. See Application Note 4 for the distribution in time of each output referenced to SYNC.
5. Specification is valid only when the PLL_EN pin is low.
6. Guaranteed that $\overline{QCLKEN}$ will meet the setup and hold time requirement of the 68060.

APPLICATION NOTES

1. Several specifications can only be measured when the MC88LV926 is in phase-locked operation. It is not possible to have the part in phase-lock on automated test equipment (ATE). Statistical characterization techniques were used to guarantee those specifications which cannot be measured on the ATE. MC88LV926 units were fabricated with key transistor properties intentionally varied to create a 14 cell designed experimental matrix. IC performance was characterized over a range of transistor properties (represented by the 14 cells) in excess of the expected process variation of the wafer fabrication area. Response Surface Modeling (RSM) techniques were used to relate IC performance to the CMOS transistor properties over operation voltage and temperature. IC performance to each specification and fab variation were used in conjunction with Yield Surface Modeling™ (YSM™) methodology to set performance limits of ATE testable specifications within those which are to be guaranteed by statistical characterization. In this way, all units passing the ATE test will meet or exceed the non–tested specifications limits.
2. A 470KΩ resistor tied to either Analog V_{CC} or Analog GND, as shown in Figure 3, is required to ensure no jitter is present on the MC88LV926 outputs. This technique causes a phase offset between the SYNC input and the Q0 output, measured at the pins. The t_{PD} spec describes how this offset varies with process, temperature, and voltage. The specs were arrived at by measuring the phase relationship for the 14 lots described in note 1 while the part was in phase–locked operation. The actual measurements were made with a 10MHz SYNC input (1.0ns edge rate from 0.8V to 2.0V). The phase measurements were made at 1.5V. See Figure 3 for a graphical description.
3. Two specs ($t_{RISE/FALL}$ and t_{PULSE} Width 2X_Q output, see AC Specifications) guarantee that the MC88LV926 meets the 33MHz and 66MHz 68060 P–Clock input specification.

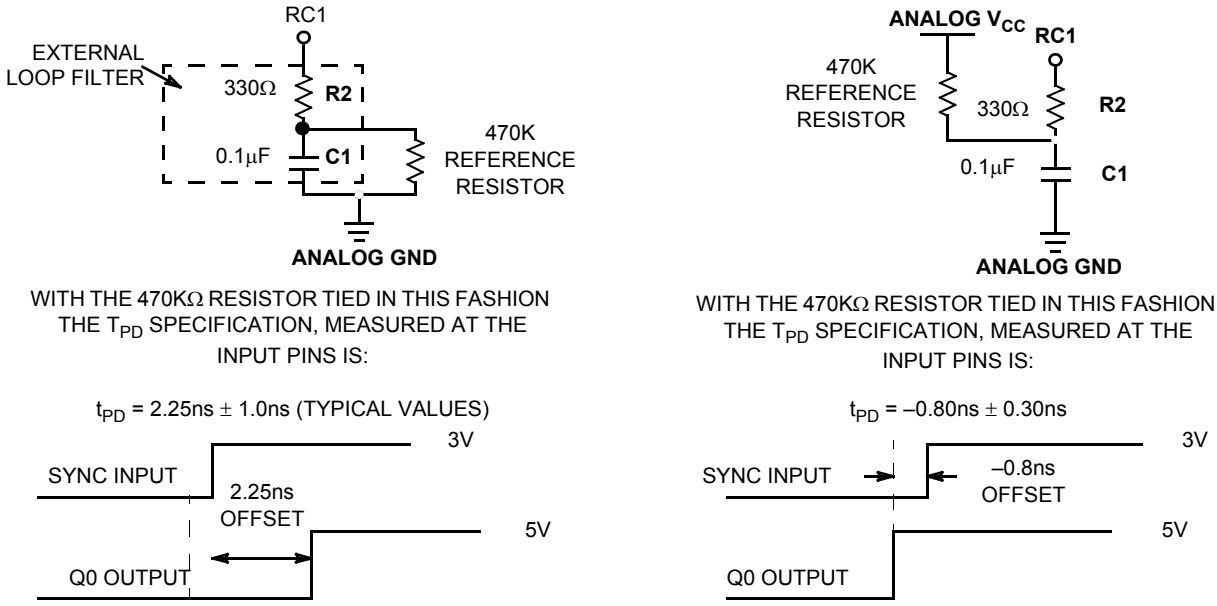


Figure 3. Depiction of the Fixed SYNC to Q0 Offset (t_{PD}) Which Is Present When a 470KΩ Resistor Is Tied to V_{CC} or Ground

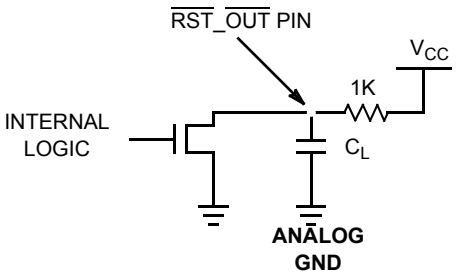


Figure 4. RST_OUT Test Circuit

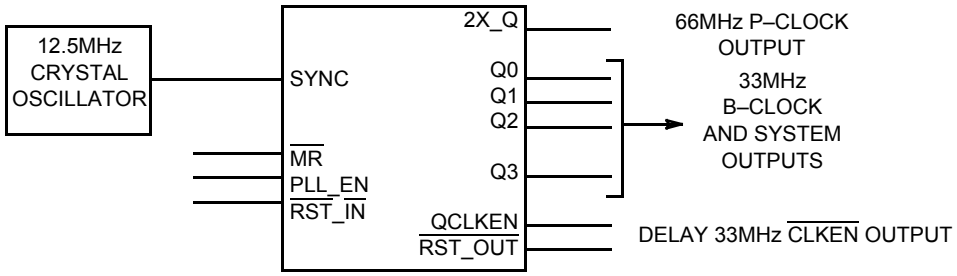
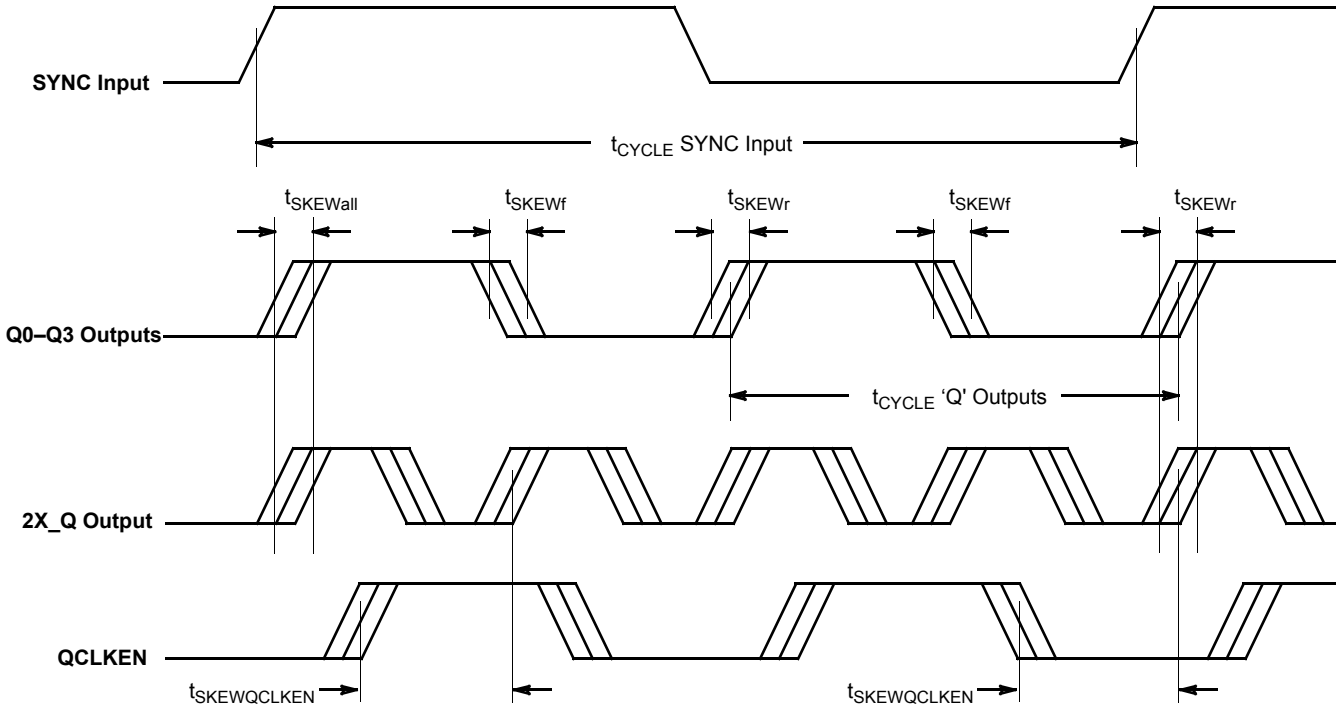


Figure 5. Logical Representation of the MC88LV926 With Input/Output Frequency Relationships



TIMING NOTES:
1. The MC88LV926 aligns rising edges of the outputs and the SYNC input, therefore the SYNC input does not require a 50% duty cycle.
2. All skew specs are measured between the $V_{CC}/2$ crossing point of the appropriate output edges. All skews are specified as 'windows', not as a ± deviation around a center point.

Figure 6. Output/Input Switching Waveforms and Timing Relationships

4. The t_{PD} spec includes the full temperature range from 0°C to 70°C and the full V_{CC} range from 3.0V to 3.3V. If the ΔT and ΔV_{CC} is a given system are less than the specification limits, the t_{PD} spec window will be reduced. The t_{PD} window for a given ΔT and ΔV_{CC} is given by the following regression formula:

TBD

5. The $\overline{RST}\_\overline{OUT}$ pin is an open drain N–Channel output. Therefore an external pull–up resistor must be provide to pull up the $\overline{RST}\_\overline{OUT}$ pin when it goes into the high impedance state (after the MC88LV926 is phase–locked to the reference input with $\overline{RST}\_\overline{IN}$ held high or 1024 ‘Q' cycles after the $\overline{RST}\_\overline{IN}$ pin goes high when the part is locked). In the t_{PLZ} and t_{PZL} specifications, a 1KΩ resistor is used as a pull–up as shown in Figure 3.

NOTES CONCERNING LOOP FILTER AND BOARD LAYOUT ISSUES

1. Figure 7 shows a loop filter and analog isolation scheme which will be effective in most applications. The following guidelines should be followed to ensure stable and jitter–free operation:

1a. All loop filter and analog isolation components should be tied as close to the package as possible. Stray current passing through the parasitics of long traces can cause undesirable voltage transients at the RC1 pin.

1b. The 47Ω resistors, the 10μF low frequency bypass capacitor, and the 0.1μF high frequency bypass capacitor form a wide bandwidth filter that will make the 88LV926 PLL insensitive to voltage transients from the system digital V_{CC} supply and ground planes. This filter will typically ensure that a 100mV step deviation on the digital V_{CC} supply will cause no more than a 100ps phase deviation on the 88LV926 outputs. A 250mV step deviation on V_{CC} using the recommended filter values will cause no more than a 250ps phase deviation; if a 25μF bypass capacitor is used (instead of 10μF) a 250mV V_{CC} step will cause no more than a 100ps phase deviation.

. If good bypass techniques are used on a board design near components which may cause digital V_{CC} and ground noise, the above described V_{CC} step deviations should not occur at the 88LV926's digital V_{CC} supply. The purpose of the bypass filtering scheme shown in Figure 6 is to give the 88LV926 additional protection from the power supply and ground plane transients that can occur in a high frequency, high speed digital system.

1c. There are no special requirements set forth for the loop filter resistors (470K and 330Ω). The loop filter capacitor (0.1uF) can be a ceramic chip capacitor, the same as a standard bypass capacitor.

1d. The 470K reference resistor injects current into the internal charge pump of the PLL, causing a fixed offset between the outputs and the SYNC input. This also prevents excessive jitter caused by inherent PLL dead–band. If the VCO (2X_Q output) is running above 40MHz, the 470K resistor provides the correct amount of current injection into the charge pump (2–3μA). If the VCO is running below 40MHz, a 1MΩ reference resistor should be used (instead of 470K).

2. In addition to the bypass capacitors used in the analog filter of Figure 7, there should be a 0.1μF bypass capacitor between each of the other (digital) four V_{CC} pins and the board ground plane. This will reduce output switching noise caused by the 88LV926 outputs, in addition to reducing potential for noise in the ‘analog' section of the chip. These bypass capacitors should also be tied as close to the 88LV926 package as possible.

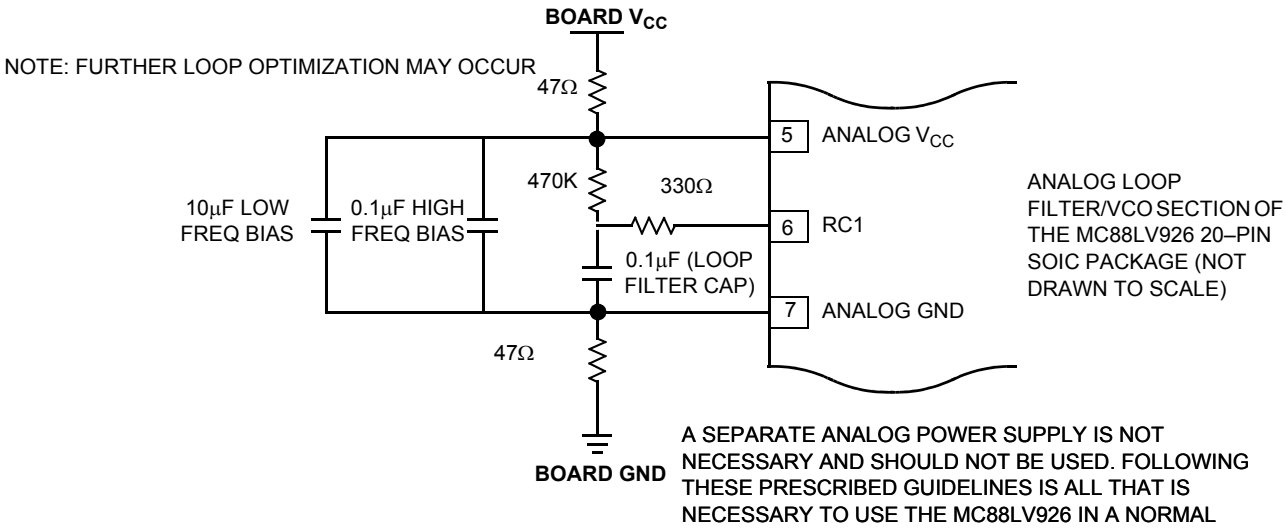


Figure 7. Recommended Loop Filter and Analog Isolation Scheme for the MC88LV926

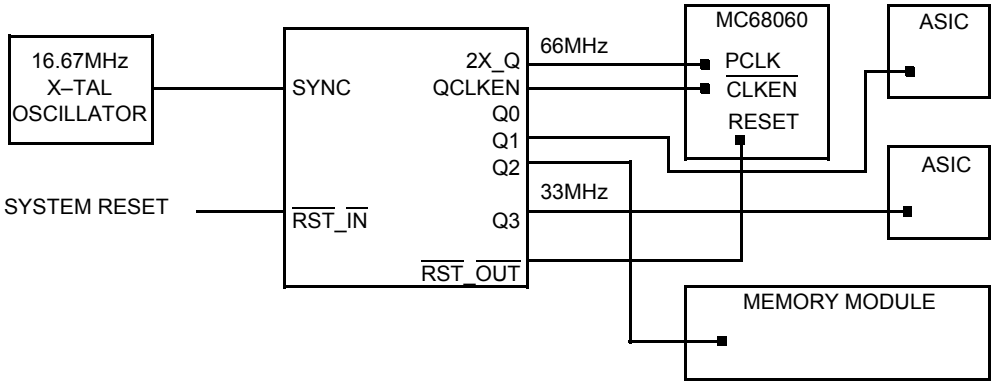


Figure 8. Typical MC88LV926/MC68060 System Configuration

Order number: MPC9315
Rev 3, 08/2004

2.5V and 3.3V CMOS PLL Clock Generator and Driver

MPC9315

LOW VOLTAGE
2.5V AND 3.3V PLL
CLOCK GENERATOR

FA SUFFIX
LQFP PACKAGE
CASE 873A-03

The MPC9315 is a 2.5V and 3.3V compatible, PLL based clock generator designed for low-skew clock distribution in low-voltage mid-range to high-performance telecom, networking and computing applications. The MPC9315 offers 8 low-skew outputs and 2 selectable inputs for clock redundancy. The outputs are configurable and support 1:1, 2:1, 4:1, 1:2 and 1:4 output to input frequency ratios. In addition, a selectable output 180° phase control supports advanced clocking schemes with inverted clock signals. The MPC9315 is specified for the extended temperature range of –40 to +85°C.

Features

- Configurable 8 outputs LVCMOS PLL clock generator
- Compatible to various microprocessors such as PowerQuicc I and II
- Wide range output clock frequency of 18.75 to 160 MHz
- 2.5V and 3.3V CMOS compatible
- Designed for mid-range to high-performance telecom, networking and computer applications
- Fully integrated PLL supports spread spectrum clocking
- Supports applications requiring clock redundancy
- Max. output skew of 120 ps (80 ps within one bank)
- Selectable output configurations (1:1, 2:1, 4:1, 1:2, 1:4 frequency ratios)
- Two selectable LVCMOS clock inputs
- External PLL feedback path and selectable feedback configuration
- Tristable outputs
- 32-Lead LQFP package
- Ambient operating temperature range of -40 to +85°C
- 32-Lead Pb-free Package Available

Functional Description

The MPC9315 utilizes PLL technology to frequency and phase lock its outputs onto an input reference clock. Normal operation requires a connection of one of the device outputs to the selected feedback (FB0 or FB1) input to close the PLL feedback path. The reference clock frequency and the output divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. With available output dividers of divide-by-1, divide-by-2 and divide-by-4 the internal VCO of the MPC9315 is running at either 1x, 2x or 4x of the reference clock frequency. The frequency of the QA, QB, QC output groups is either the equal, one half or one fourth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB and FSELC pins, respectively. The available output to input frequency ratios are 4:1, 2:1, 1:1, 1:2 and 1:4. The REF_SEL pin selects one of the two available LVCMOS compatible reference input (CLK0 and CLK1) supporting clock redundant applications. The selectable feedback input pin allows the user to select different feedback configurations and input to output frequency ratios. The MPC9315 also provides a static test mode when the PLL supply pin (V_{CCA}) is pulled to logic low state (GND). In test mode, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The test mode is intended for system diagnostics, test and debug purpose. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the $\overline{OE}$ pin (logic high state). In PLL mode, deasserting $\overline{OE}$ causes the PLL to lose lock due to no feedback signal presence at FB0 or FB1. Asserting $\overline{OE}$ will enable the outputs and close the phase locked loop, also enabling the PLL to recover to normal operation. The MPC9315 is fully 2.5V and 3.3V compatible and requires no external loop filter components. All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9315 outputs can drive one or two traces giving the devices an effective fanout of 1:18. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

The fully integrated PLL of the MPC9315 allows the low skew outputs to lock onto a clock input and distribute it with essentially zero propagation delay to multiple components on the board. In zero-delay buffer mode, the PLL minimizes phase offset between the outputs and the reference signal.

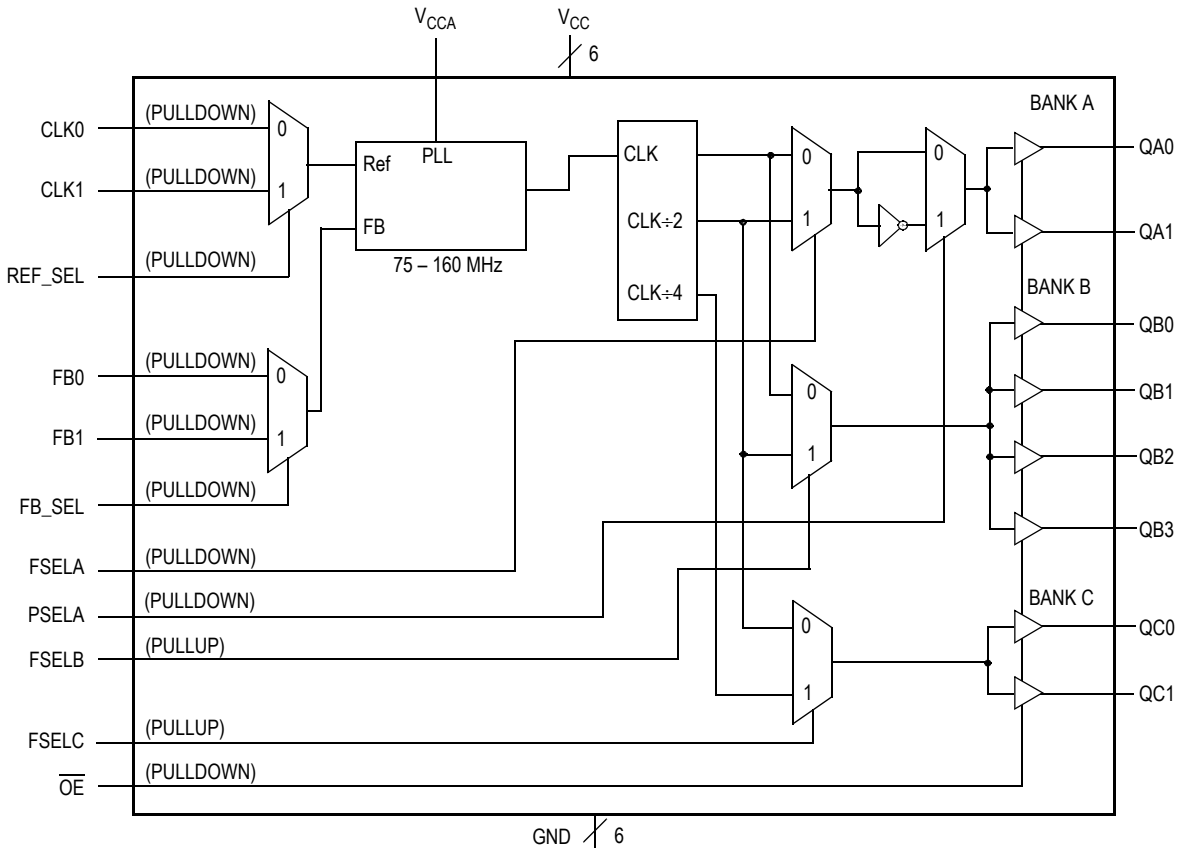


Figure 1. MPC9315 Logic Diagram

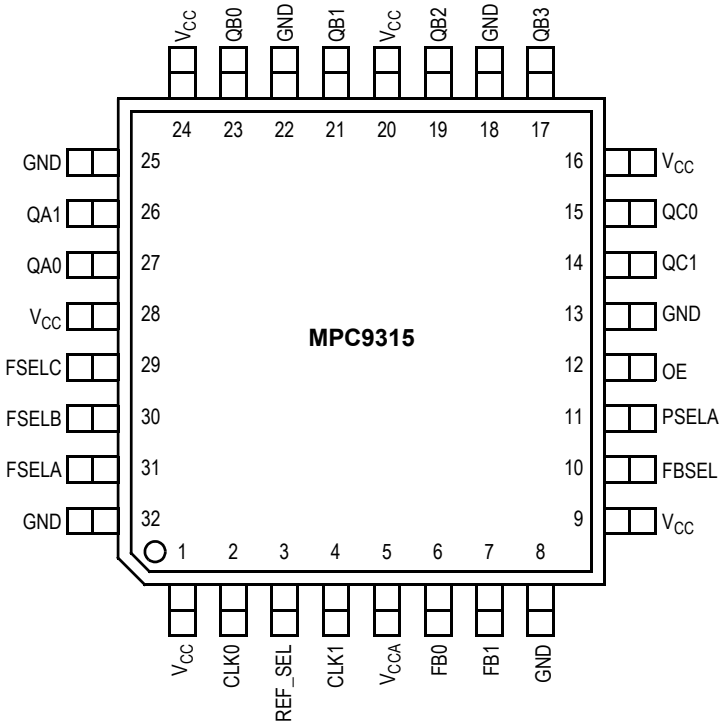


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLK0	Input	LVCMOS	Reference clock input
CLK1	Input	LVCMOS	Alternative clock input
FB0	Input	LVCMOS	PLL feedback input
FB1	Input	LVCMOS	Alternative feedback input
REF_SEL	Input	LVCMOS	Selects clock input reference clock input, default low (pull-down)
FB_SEL	Input	LVCMOS	Selects PLL feedback clock input, default low (pull-down)
FSELA	Input	LVCMOS	Selects divider ratio of bank A outputs, default low (pull-down)
FSELB	Input	LVCMOS	Selects divider ratio of bank B outputs, default low (pull-up)
FSELC	Input	LVCMOS	Selects divider ratio of bank C outputs, default low (pull-up)
PSELA	Input	LVCMOS	Selects phase of bank A outputs
QA0, QA1	Output	LVCMOS	Bank A outputs
QB0 to QB3	Output	LVCMOS	Bank B outputs
QC0, QC1	Output	LVCMOS	Bank C outputs
$\overline{OE}$	Input	LVCMOS	Output tristate
V_{CCA}		Supply	Analog (PLL) positive supply voltage. Requires external RC filter
V_{CC}		Supply	Digital positive supply voltage
GND		Ground	Digital negative supply voltage (ground)

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	CLK0	CLK1
FB_SEL	0	FB0	FB1
FSELA	0	QAx = VCO clock frequency	QA0, QA1 = VCO clock frequency ÷ 2
FSELB	1	QBx = VCO clock frequency	QB0 - QB3 = VCO clock frequency ÷ 2
FSELC	1	QCx = VCO clock frequency ÷ 2	QC0, QC1 = VCO clock frequency ÷ 4
PSELA	0	0° (QA0, QA1 non-inverted)	180° (QA0, QA1 inverted)
V_{CCA}	none	V_{CCA} = GND, PLL off and bypassed for static test and diagnosis	V_{CCA} = 3.3 or 2.5V, PLL enabled
MR	0	Normal operation	Reset (VCO clamped to min. range)
$\overline{OE}$	0	Outputs enabled	Outputs disabled (tristate), open PLL loop

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	4.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	-55	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD (Machine Model)	200			V	
HBM	ESD (Human Body Model)	2000			V	
LU	Latch-Up	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH}=–24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24mA[1] I_{OL}= 12mA
Z_{OUT}	Output Impedance		14 - 17		Ω	
I_{IN}	Input Current[2]			±200	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current		3.5	7.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

1. The MPC9315 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
2. Inputs have pull-up or pull-down resistors affecting the input current.

Table 6. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	÷1 feedback ÷2 feedback ÷4 feedback PLL bypass mode	100[2] 37.50 18.75 0		160 80 40 TBD	MHz MHz MHz MHz	PLL locked PLL locked PLL locked V_{CCA} = GND
f_{VCO}	VCO Lock Range		75[b]		160	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output ÷2 output ÷4 output	75 37.50 18.75		160 80 40	MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
t_r, t_f	CLK0, CLK1 Input Rise/Fall Time				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (Static Phase Offset)	CLK0 or CLK1 to FB	-150		+150	ps	PLL locked
$t_{SK(\varnothing)}$	Output-to-Output Skew	Within one bank Any output			80 120	ps ps	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
BW	PLL closed loop bandwidth	÷1 feedback ÷2 feedback ÷4 feedback		TBD 2.0 - 20 0.6 - 6.0		MHz MHz MHz	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	(1σ)		10	22	ps	RMS value
$t_{JIT(PER)}$	Period Jitter	(1σ)		8.0	15	ps	RMS value
$t_{JIT(\varnothing)}$	I/O Phase Jitter	(1σ)		8.0 - 25[3]	TBD	ps	RMS value
t_{LOCK}	Maximum PLL Lock Time				1.0	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. The VCO range in ÷1 feedback configuration (e.g. QAx connected to FBx and FSELA = 0) is limited to $100 \le f_{VCO} \le 160$ MHz. Please see next revision of the MPC9315 for improved VCO frequency range.
3. I/O jitter depends on VCO frequency. Please see application section for I/O jitter versus VCO frequency characteristics.

Table 7. DC Characteristics (V_{CC} = 2.5V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.8			V	I_{OH}=–15 mA[1]
V_{OL}	Output Low Voltage			0.6	V	I_{OL}= 15mA
Z_{OUT}	Output Impedance		17 - 20		Ω	
I_{IN}	Input Current[2]			±200	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

1. The MPC9315 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
2. Inputs have pull-up or pull-down resistors affecting the input current.

Table 8. AC Characteristics (V_{CC} = 2.5V ± 5%, T_A = -40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	÷2 feedback ÷4 feedback PLL bypass mode	37.50 18.75 0		80 40 TBD	MHz MHz MHz	PLL locked PLL locked VCCA = GND
f_{VCO}	VCO Lock Range		75[2]		160[b]	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output ÷2 output ÷4 output	75 37.50 18.75		160 80 40	MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
t_r, t_f	CLK0, CLK1 Input Rise/Fall Time				1.0	ns	0.7 to 1.7V
$t_{(\varnothing)}$	Propagation Delay (Static Phase Offset)	CLK0 or CLK1 to FB	-150		+150	ps	PLL locked
$t_{SK(\varnothing)}$	Output-to-Output Skew	Within one bank Any output			80 120	ps ps	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				12	ns	
$t_{PZL, LZ}$	Output Enable Time				12	ns	
BW	PLL closed loop bandwidth	÷2 feedback ÷4 feedback		1.0 - 10 0.4 - 3.0		MHz MHz	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	(1σ)		10	22	ps	RMS value
$t_{JIT(PER)}$	Period Jitter	(1σ)		8.0	15	ps	RMS value
$t_{JIT(\varnothing)}$	I/O Phase Jitter	(1σ)		10 - 25[3]	TBD	ps	RMS value
t_{LOCK}	Maximum PLL Lock Time				1.0	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. ÷1 feedback is responsible for V_{CC} = 2.5V operation. Please see application section for I/O jitter versus VCO frequency characteristics.
3. I/O jitter depends on VCO frequency. Please see application section for I/O jitter versus VCO frequency characteristics.

APPLICATIONS INFORMATION

Programming the MPC9315

The PLL of the MPC9315 supports output clock frequencies from 18.75 to 160 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency range between 75 and 160 MHz for stable and optimal operation. The FSELA, FSELB, FSELC pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:1, 1:2, 1:4 as well as 2:1 and 4:1, Table 9, Table 10, and Table 11 illustrate the various output configurations and frequency ratios supported by the MPC9315. PSELA controls the output phase of the QA0 and QA1 outputs, allowing the user to generate inverted clock signals synchronous to non-inverted clock signals. See also Example Configurations for the MPC9315 for further reference.

Table 9. Output Frequency Relationship for QA0 connected to FB0[1]

Inputs			Outputs		
FSELA	FSELB	FSELC	QA0, QA1	QB0–QB3	QC0, QC1
0	0	0	CLK	CLK	CLK ÷ 2
0	0	1	CLK	CLK	CLK ÷ 4
0	1	0	CLK	CLK ÷ 2	CLK ÷ 2
0	1	1	CLK	CLK ÷ 2	CLK ÷ 4
1	0	0	CLK	2 * CLK	CLK
1	0	1	CLK	2 * CLK	CLK ÷ 2
1	1	0	CLK	CLK	CLK
1	1	1	CLK	CLK	CLK ÷ 2

1. Output frequency relationship with respect to input reference frequency CLK.

Table 10. Output Frequency Relationship for QB0 connected to FB0[1]

Inputs			Outputs		
FSELA	FSELB	FSELC	QA0, QA1	QB0–QB3	QC0, QC1
0	0	0	CLK	CLK	CLK ÷ 2
0	0	1	CLK	CLK	CLK ÷ 4
0	1	0	2 * CLK	CLK	CLK
0	1	1	2 * CLK	CLK	CLK ÷ 2
1	0	0	CLK ÷ 2	CLK	CLK ÷ 2
1	0	1	CLK ÷ 2	CLK	CLK ÷ 4
1	1	0	CLK	CLK	CLK
1	1	1	CLK	CLK	CLK ÷ 2

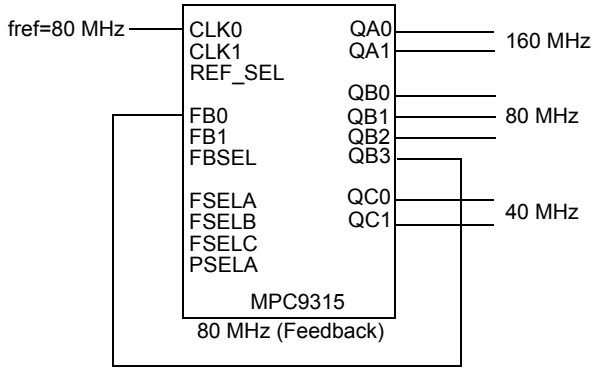
1. Output frequency relationship with respect to input reference frequency CLK.

Table 11. Output Frequency Relationship for QC0 connected to FB0[1]

Inputs			Outputs		
FSELA	FSELB	FSELC	QA0, QA1	QB0–QB3	QC0, QC1
0	0	0	2 * CLK	2 * CLK	CLK
0	0	1	4 * CLK	4 * CLK	CLK
0	1	0	2 * CLK	CLK	CLK
0	1	1	4 * CLK	2 * CLK	CLK
1	0	0	CLK	2 * CLK	CLK
1	0	1	2 * CLK	4 * CLK	CLK
1	1	0	CLK	CLK	CLK
1	1	1	2 * CLK	2 * CLK	CLK

1. Output frequency relationship with respect to input reference frequency CLK.

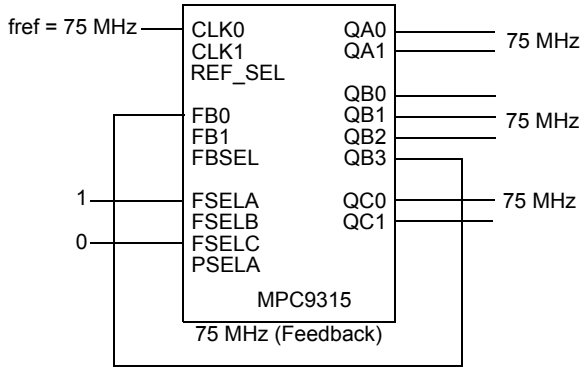
Example Configurations for the MPC9315



MPC9315 default configuration (feedback of QB3 = 100 MHz). All control pins are left open.

Frequency range	Min	Max
Input	37.50 MHz	80 MHz
QA outputs	75.00 MHz	160 MHz
QB outputs	37.50 MHz	80 MHz
QC outputs	18.75 MHz	40 MHz

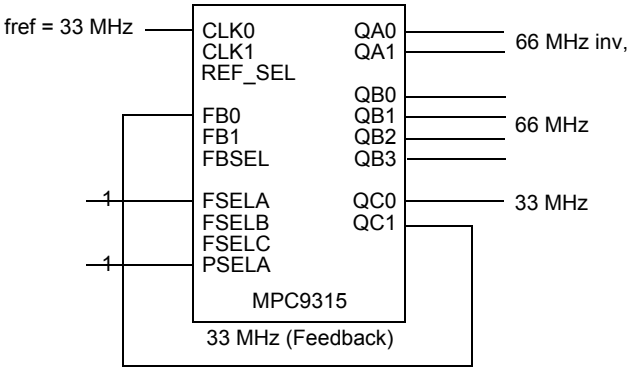
Figure 3. MPC9315 Default Configuration



MPC9315 1:1 frequency configuration (feedback of QB3 = 75 MHz). FSELA = H, FSELC = L. All other control pins are left open.

Frequency range	Min	Max
Input	37.50 MHz	80 MHz
QA outputs	37.50 MHz	80 MHz
QB outputs	37.50 MHz	80 MHz
QC outputs	37.50 MHz	80 MHz

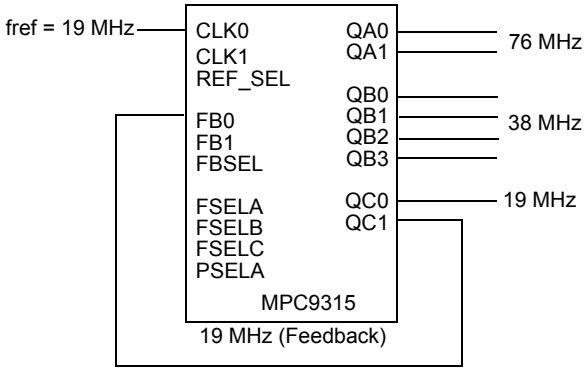
Figure 4. MPC9315 Zero Delay Buffer Configuration



MPC9315 1:1 frequency configuration (feedback of QC1 = 33 MHz). FSELA = PSELA = H. All other control pins are left open.

Frequency range	Min	Max
Input	18.75 MHz	40 MHz
QA outputs	37.50 MHz	80 MHz
QB outputs	37.50 MHz	80 MHz
QC outputs	18.75 MHz	40 MHz

Figure 5. MPC9315 180° Phase Inversion Configuration



MPC9315 4x, 2x, 1x frequency configuration (feedback of QC1 = 19 MHz). All control pins are left open.

Frequency range	Min	Max
Input	18.75 MHz	40 MHz
QA outputs	75.00 MHz	160 MHz
QB outputs	37.50 MHz	80 MHz
QC outputs	18.75 MHz	40 MHz

Figure 6. MPC9315 x4 Multiplier Configuration

Using the MPC9315 in Zero-Delay Applications

The external feedback option of the MPC9315 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC9315 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$ relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9315 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (TCLK or PCLK) of two or more MPC9315 are connected together, the maximum overall timing uncertainty from the common TCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \bullet CF$$

This maximum timing uncertainty consists of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

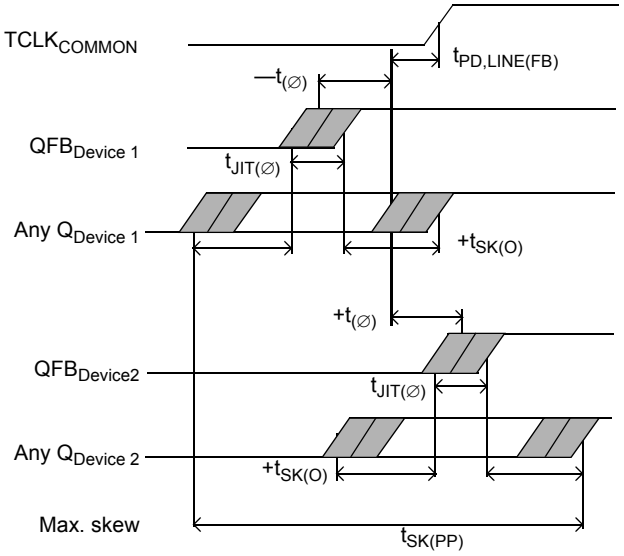


Figure 7. MPC9315 max. Device-to-Device Skew

Due to the statistical nature of I/O jitter, an RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 12.

Table 12. Confidence Factor CF

CF	Probability of Clock Edge within the Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –300 ps to +300 ps relative to TCLK (V_{CC}=3.3V and f_{VCO} = 160 MHz):

$t_{SK(PP)}$ = *[–150ps...150ps] + [–150ps...150ps] + [(10ps @ –3)...(10ps @ 3)] +* $t_{PD,\ LINE(FB)}$

$t_{SK(PP)}$ = *[–300ps...300ps]* + $t_{PD,\ LINE(FB)}$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for V_{CC}=3.3V (10 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (160 MHz for the MPC9315). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 8. Max. I/O Jitter (RMS) versus frequency for VCC=2.5V and Figure 9. Max. I/O Jitter (RMS) versus frequency for VCC=3.3V can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

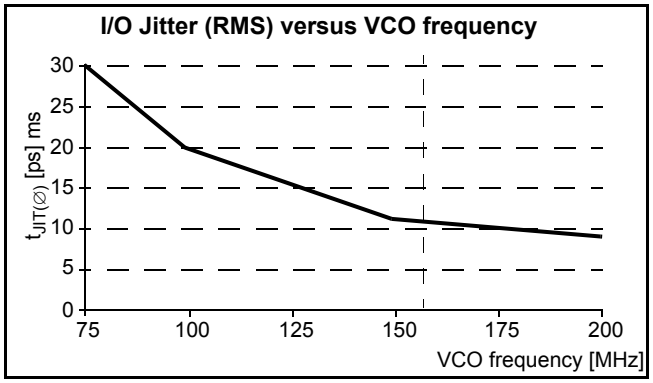


Figure 8. Max. I/O Jitter (RMS) versus frequency for V_{CC}=2.5V

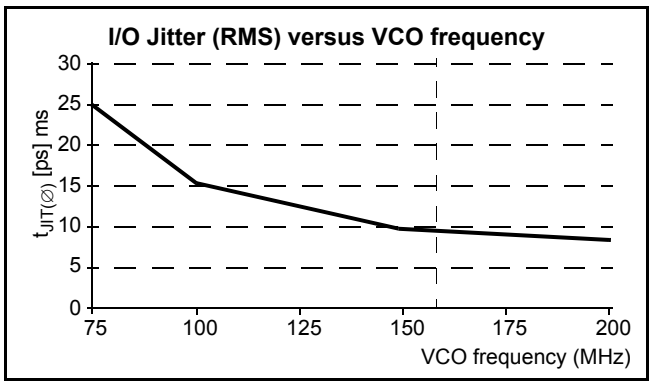


Figure 9. Max. I/O Jitter (RMS) versus frequency for V_{CC}=3.3V

Power Supply Filtering

The MPC9315 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for

instance I/O jitter. The MPC9315 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9315. Figure 10. VCCA Power Supply Filter illustrates a typical power supply filter scheme. The MPC9315 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V (V_{CC}=3.3V or V_{CC}=2.5V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 10. VCCA Power Supply Filter must have a resistance of 270Ω (V_{CC}=3.3V) or 9-10Ω (V_{CC}=2.5V) to meet the voltage drop criteria.

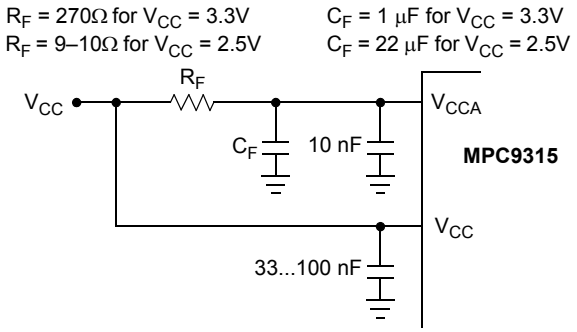


Figure 10. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 10. VCCA Power Supply Filter, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9315 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9315 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9315 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 11. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9315 clock driver is effectively doubled due to its capability to drive multiple lines.

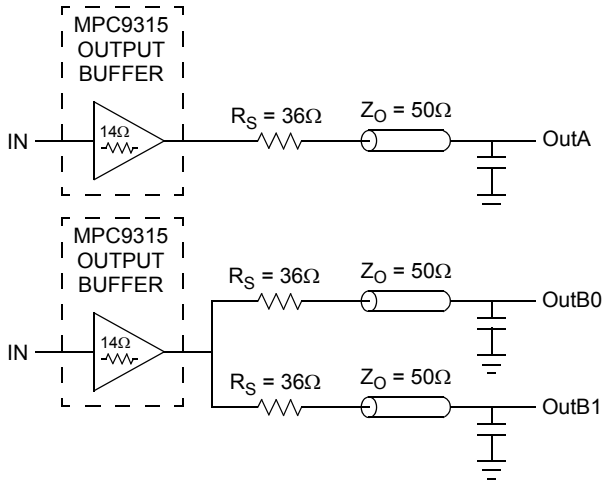


Figure 11. Single versus Dual Transmission Lines

The waveform plots in Figure 11. Single versus Dual Transmission Lines show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9315 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9315. The output waveform in Figure 12. Single versus Dual Line Termination Waveforms shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination

of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S+R_0 +Z_0))$

$Z_0 = 50\Omega \parallel 50\Omega$

$R_S = 36\Omega \parallel 36\Omega$

$R_0 = 14\Omega$

$V_L = 3.0 (25 \div (18+17+25)$

$= 1.31V$

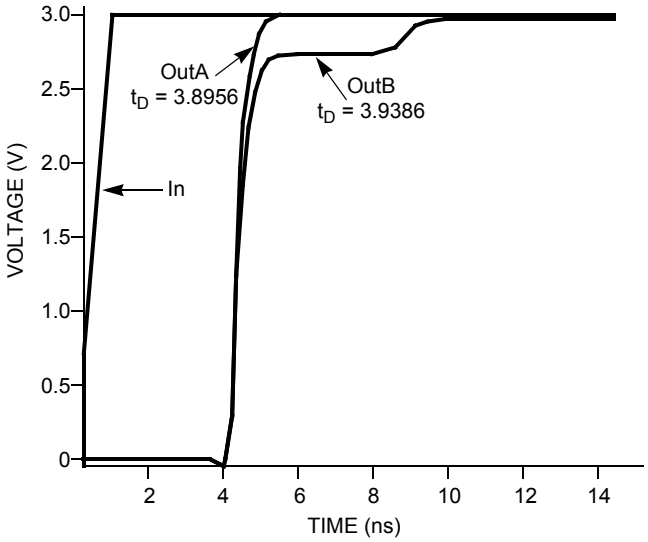


Figure 12. Single versus Dual Line Termination Waveforms

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 13. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

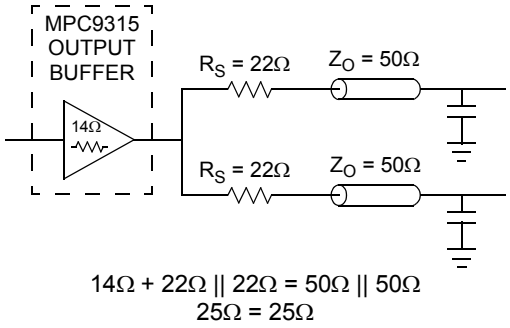


Figure 13. Optimized Dual Line Termination

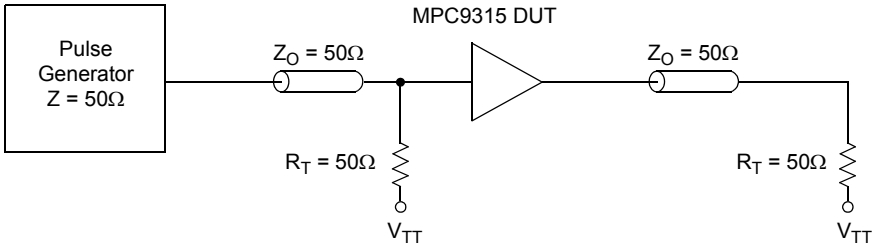


Figure 14. CLK0, CLK1 MPC9315 AC test reference

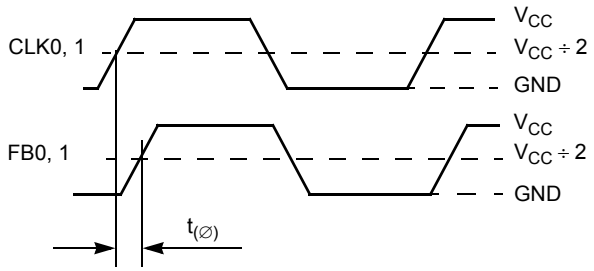
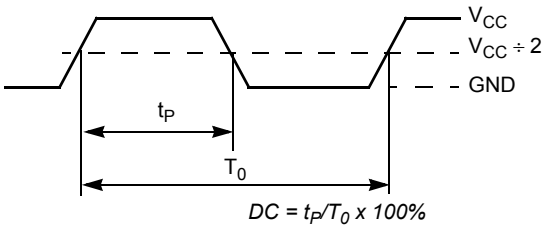
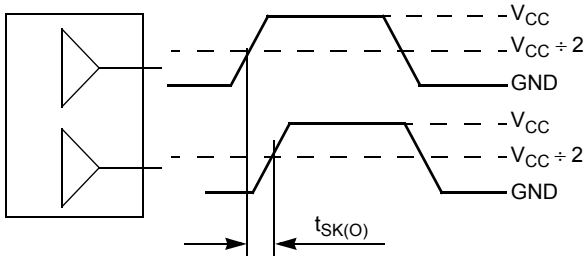


Figure 15. Propagation delay ($t_{(\varnothing)}$, SPO) test reference



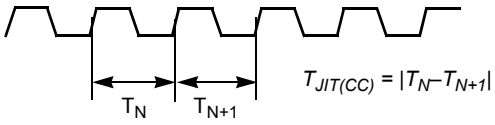
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)



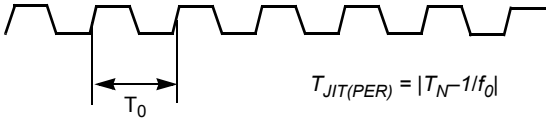
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 17. Output-to-output Skew $t_{SK(O)}$



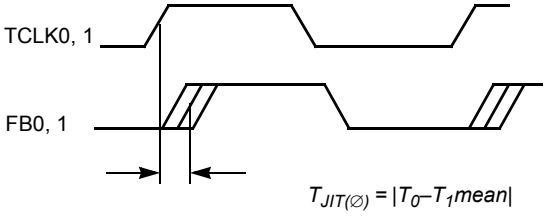
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 18. Cycle-to-cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 19. Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 20. I/O Jitter

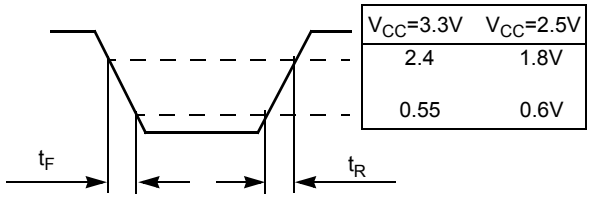


Figure 21. Output Transition Time Test Reference

Order number: MPC9330
Rev 4, 08/2004

3.3V 1:60 LVCMOS PLL Clock Generator

MPC9330

3.3V 1:6 LVCMOS PLL CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC9330 is a 3.3 V compatible, 1:6 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance telecomm, networking and computing applications. With output frequencies up to 120 MHz and output skews less than 150 ps the device meets the needs of the most demanding clock applications. The MPC9330 is specified for the temperature range of 0°C to +70°C.

Features

- 1:6 PLL based low-voltage clock generator
- 3.3 V power supply
- Generates clock signals up to 120 MHz
- Maximum output skew of 150 ps
- On-chip crystal oscillator clock reference
- Alternative LVCMOS PLL reference clock input
- Internal and external PLL feedback
- PLL multiplies the reference clock by 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3, or x/4
- Supports zero-delay operation in external feedback mode
- Synchronous output clock stop in logic low eliminates output runt pulses
- Power_down feature reduces output clock frequency
- Drives up to 12 clock lines
- 32-lead LQFP packaging
- 32-lead Pb-free package available
- Ambient temperature range 0°C to +70°C
- Internal power-up reset
- Pin and function compatible to the MPC930

Functional Description

The MPC9330 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9330 requires either the selection of internal PLL feedback or the connection of one of the device outputs to the feedback input to close the PLL feedback path in external feedback mode. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. In external PLL feedback configuration and with the available post-PLL dividers (divide-by-2, divide-by-4 and divide-by-6), the internal VCO of the MPC9330 is running at either 4x, 8x, 12x, 16x, or 24x of the reference clock frequency. In internal feedback configuration (divide-by-16) the internal VCO is running 16x of the reference frequency. The frequency of the QA, QB, QC output banks is a division of the VCO frequency and can be configured independently for each output bank using the FSELA, FSELB and FSELC pins, respectively. The available output to input frequency ratios are 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3, or x/4.

The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible input as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be disabled (high-impedance) by deasserting the OE/$\overline{\text{MR}}$ pin. In the PLL configuration with external feedback selected, deasserting OE/MR causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Asserting OE/MR will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation. The MPC9330 output clock stop control allows the outputs to start and stop synchronously in the logic low state, without the potential generation of runt pulses.

The MPC9330 is fully 3.3 V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9330 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

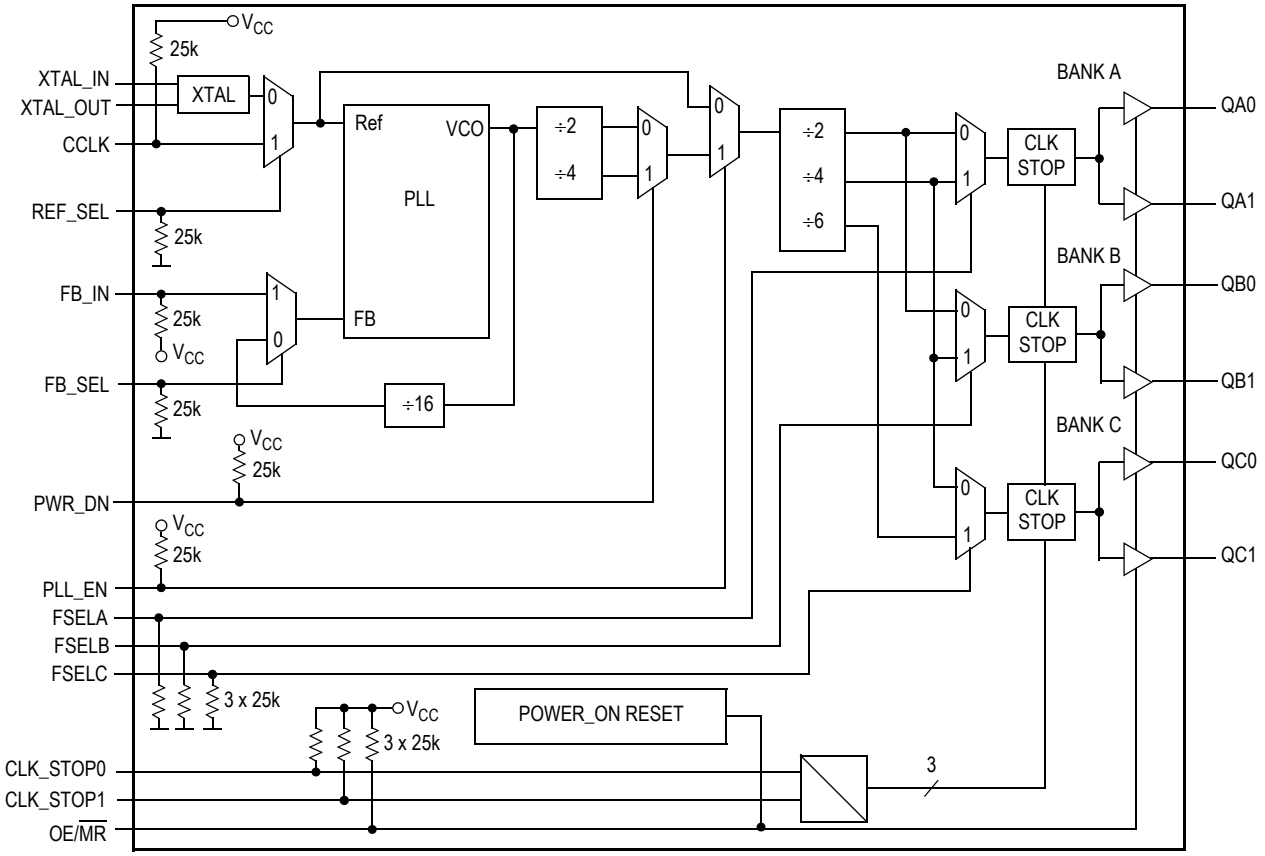
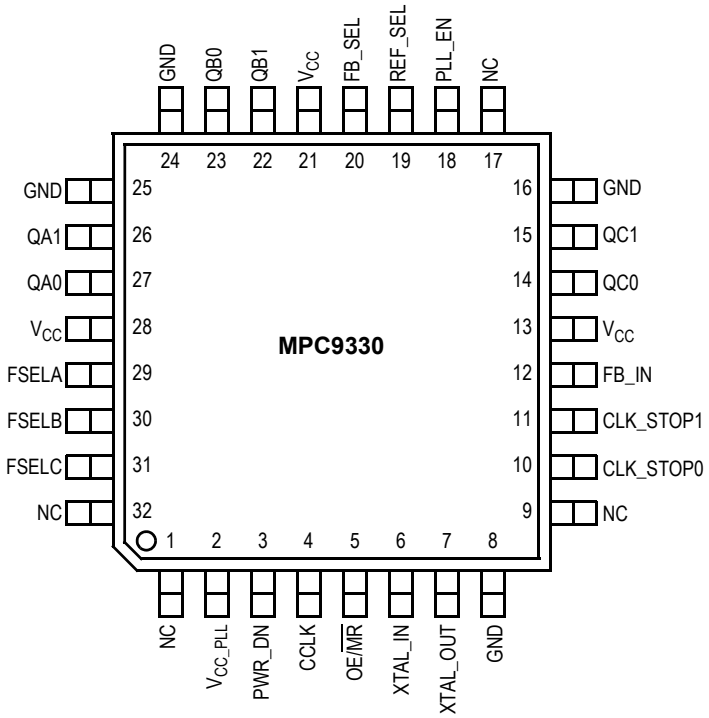


Figure 1. MPC9330 Logic Diagram



It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see application section for details.

Figure 2. MPC9330 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVCMOS	PLL reference clock signal
XTAL_IN, XTAL_OUT	Input	Analog	Crystal oscillator interface
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to an output
FB_SEL	Input	LVCMOS	Feedback select
REF_SEL	Input	LVCMOS	Reference clock select
PWR_DN	Input	LVCMOS	Output frequency and power down select
FSELA	Input	LVCMOS	Frequency divider select for bank A outputs
FSELB	Input	LVCMOS	Frequency divider select for bank B outputs
FSELC	Input	LVCMOS	Frequency divider select for bank C outputs
PLL_EN	Input	LVCMOS	PLL enable/disable
CLK_STOP0-1	Input	LVCMOS	Clock output enable/disable
OE/$\overline{MR}$	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
QA0-1, QB0-1, QC0-1	Output	LVCMOS	Clock outputs
GND	Supply	Ground	Negative power supply
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	The crystal oscillator output is the PLL reference clock	CCLK is the PLL reference clock
FB_SEL	0	Internal PLL feedback of 16. $f_{VCO} = 16 * f_{ref}$	External feedback. Zero-delay operation enabled for CCLK as reference clock
PLL_EN	1	Test mode with PLL disabled. The reference clock is substituted for the internal VCO output. MPC9330 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
PWR_DN	1	VCO ÷ 2 (High output frequency range)	VCO ÷ 4 (Low output frequency range)
FSELA	0	Output divider ÷ 2	Output divider ÷ 4
FSELB	0	Output divider ÷ 2	Output divider ÷ 4
FSELC	0	Output divider ÷ 4	Output divider ÷ 6
CLK_STOP[0:1]	11	See Table 3	
OE/$\overline{MR}$	1	Outputs disabled (high-impedance state) and reset of the device. During reset in external feedback configuration, the PLL feedback loop is open. The VCO is tied to its lowest frequency. The MPC9330 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLK). Reset does not affect PLL lock in internal feedback configuration.	Outputs enabled (active)

PWR_DN, FSELA, FSELB and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 8 through Table 10 for supported frequency ranges and output to input frequency ratios.

Table 3. Clock Output Synchronous Disable (CLK_STOP) Function Table[1]

CLK_STOP0	CLK_STOP1	QA[0:1]	QB[0:1]	QC[0:1]
0	0	Active	Stopped in logic L state	Stopped in logic L state
0	1	Active	Stopped in logic L state	Active
1	0	Stopped in logic L state	Stopped in logic L state	Active
1	1	Active	Active	Active

1. Output operation for OE/$\overline{MR}$=1 (outputs enabled). OE/$\overline{MR}$=0 will disable (high-impedance state) all outputs independent on CLK_STOP[0:1]

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24 mA I_{OL}= 12 mA
Z_{OUT}	Output Impedance		14 – 17		Ω	
I_{IN}	Input Current[2]			±100	µA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		5.0	10	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current		5.0	10	mA	All V_{CC} Pins

1. The MPC9330 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
2. Inputs have pull-down or pull-up resistors affecting the input current.

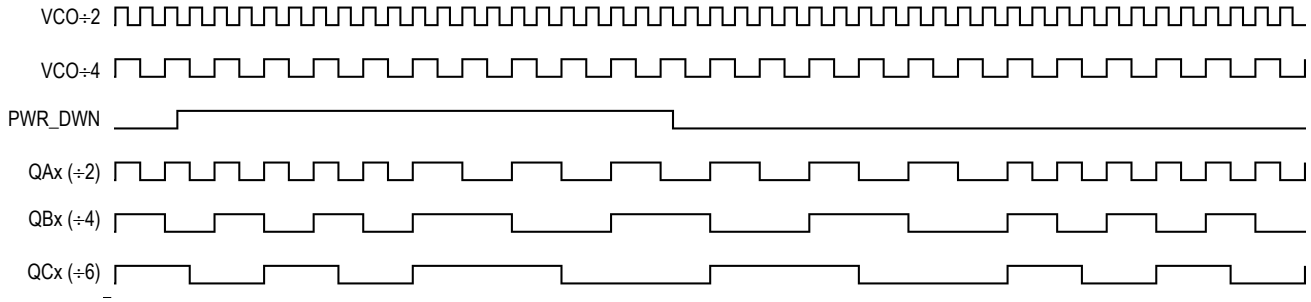
Table 7. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency[2]	÷ 4 feedback[3]	50		120	MHz	PLL locked
	PLL mode, external feedback	÷ 8 feedback	25		60	MHz	
		÷ 12 feedback	16.67		40	MHz	
		÷ 16 feedback	12.5		30	MHz	
		÷ 24 feedback	8.33		20	MHz	
	PLL mode, internal feedback	⟨÷ 16 feedback)	12.5		30	MHz	
	Input Reference Frequency in PLL bypass mode[4]				TBD	MHz	
f_{VCO}	VCO Lock Frequency Range[5]		200		480	MHz	
f_{XTAL}	Crystal Interface Frequency Range[6]		10		25	MHz	
f_{MAX}	Output Frequency	÷ 4 output	50		120	MHz	PLL locked
		÷ 8 output	25		60	MHz	
		÷ 12 output	16.67		40	MHz	
		÷ 16 output	12.5		30	MHz	
		÷ 24 output	8.33		20	MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
$t_{PW, MIN}$	Minimum Input Reference Pulse Width		2			ns	
t_r, t_f	CCLK Input Rise/Fall Time				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (SPO)[7] for the	- entire f_{ref} range	-1.2		+1.2	°	
		- f_{ref} = 8.33 MHz	-400		+400	ps	
		- f_{ref} = 50.0 MHz	-70		+70	ps	
$t_{sk(o)}$	Output-to-Output Skew[8]	(within output bank)			50	ps	
		(any output)			150	ps	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter			50	300	ps	
$t_{JIT(PER)}$	Period Jitter			35	250	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1σ)		10	70	ps	
BW	PLL closed loop bandwidth[9]	÷ 4 feedback		0.8-5.0		MHz	
	PLL mode, external feedback	÷ 8 feedback		0.5-2.0		MHz	
		÷ 12 feedback		0.3-1.0		MHz	
		÷ 16 feedback		0.25-0.6		MHz	
		÷ 24 feedback		0.2-0.5		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

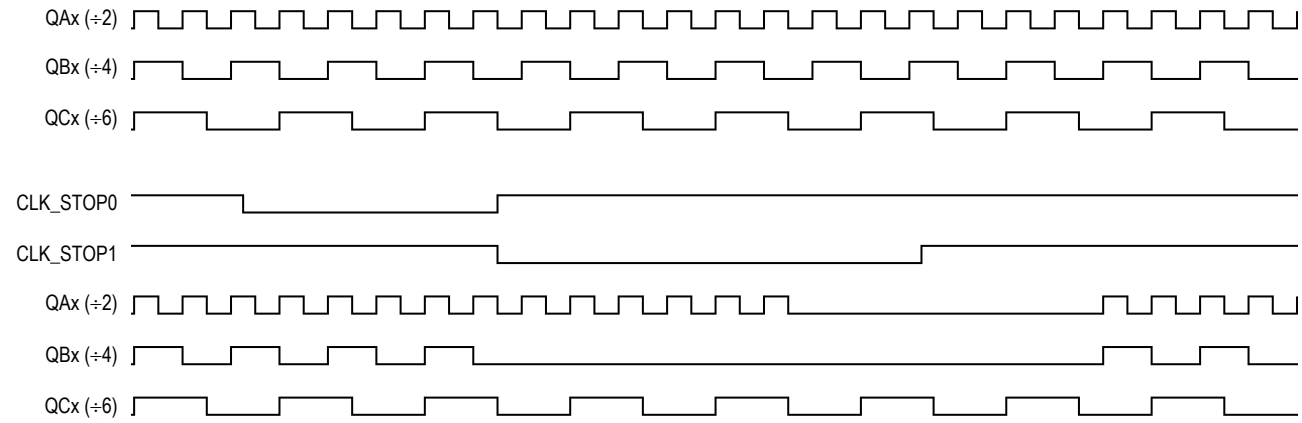
1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. PLL mode requires PLL_EN = 0 to enable the PLL.
3. ÷4 feedback (FB) can be accomplished by setting PWR_DN = 0 and the connection of one ÷2 output to FB_IN. See Table 3 to Table 5 for other feedback configurations.
4. In bypass mode, the MPC9330 divides the input reference clock.
5. The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
6. The usable crystal frequency range depends on the VCO lock frequency and the PLL feedback ratio.
7. SPO is the static phase offset between CCLK and FB_IN (FB_SEL=1 and PLL locked). $t_{sk(o)}$ [ps] = $t_{sk(o)}$ [°] B(fref ÷ 360°)
8. Skew data applicable for equally loaded outputs only.
9. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Output Power Down (PWR_DN) Timing Diagram



Output Clock Stop (CLK_STOP) Timing Diagram



Programming the MPC9330

The MPC9330 supports output clock frequencies from 8.33 to 120 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 480 MHz for stable and optimal operation. The FSELA, FSELB, FSELC and PWR_DN pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:4, 1:3, 1:2, 1:1, 2:3, 4:3 and 3:2. Table 8 through Table 10 illustrate the various output configurations and frequency ratios supported by the MPC9330.

Table 8. MPC9330 Example Configurations (Internal Feedback: FB_SEL = 0)

fref[1] [MHz]	PWR_DN	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
12.5–30.0	0	0	0	0	fref · 4 (50-120 MHz)	fref · 4 (50-120 MHz)	fref · 2 (25-60 MHz)
	0	0	0	1	fref · 4 (50-120 MHz)	fref · 4 (50-120 MHz)	fref ·4 ÷ 3 (16.6-40 MHz)
	0	0	1	0	fref · 4 (50-120 MHz)	fref · 2 (25-60 MHz)	fref · 2 (25-60 MHz)
	0	0	1	1	fref · 4 (50-120 MHz)	fref · 2 (25-60 MHz)	fref · 4 ÷ 3 (16.6-40 MHz)
	0	1	0	0	fref · 2 (25-60 MHz)	fref · 4 (50-120 MHz)	fref · 2 (25-60 MHz)
	0	1	0	1	fref · 2 (25-60 MHz)	fref · 4 (50-120 MHz)	fref · 4 ÷ 3 (16.6-40 MHz)
	0	1	1	0	fref · 2 (25-60 MHz)	fref · 2 (25-60 MHz)	fref · 2 (25-60 MHz)
	0	1	1	1	fref · 2 (25-60 MHz)	fref · 2 (25-60 MHz)	fref · 4 ÷ 3 (16.6-40 MHz)
	1	0	0	0	fref · 2 (25-60 MHz)	fref · 2 (25-60 MHz)	fref (12.5-30 MHz)
	1	0	0	1	fref · 2 (25-60 MHz)	fref · 2 (25-60 MHz)	fref · 2 ÷ 3 (8.33-20 MHz)
	1	0	1	0	fref · 2 (25-60 MHz)	fref (12.5-30 MHz)	fref (12.5-30 MHz)
	1	0	1	1	fref · 2 (25-60 MHz)	fref (12.5-30 MHz)	fref · 2 ÷ 3 (8.33-20 MHz)
	1	1	0	0	fref (12.5-30 MHz)	fref · 2 (25-60 MHz)	fref (12.5-30 MHz)
	1	1	0	1	fref (12.5-30 MHz)	fref · 2 (25-60 MHz)	fref · 2 ÷ 3 (8.33-20 MHz)
	1	1	1	0	fref (12.5-30 MHz)	fref (12.5-30 MHz)	fref (12.5-30 MHz)
	1	1	1	1	fref (12.5-30 MHz)	fref (12.5-30 MHz)	fref · 2 ÷ 3 (8.33-20 MHz)

1. fref is the input clock reference frequency (CCLK or XTAL)

Table 9. MPC9330 Example Configurations (External Feedback and PWR_DN = 0)

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 4[2]	50–120	0	0	0	fref (50-120 MHz)	fref (50-120 MHz)	fref ÷ 2 (25-60 MHz)
		0	0	1	fref (50-120 MHz)	fref (50-120 MHz)	fref ÷ 3 (16.6-40 MHz)
		0	1	0	fref (50-120 MHz)	fref ÷ 2 (25-60 MHz)	fref ÷ 2 (25-60 MHz)
		0	1	1	fref (50-120 MHz)	fref ÷ 2 (25-60 MHz)	fref ÷ 3 (16.6-40 MHz)
VCO ÷ 8[3]	25–60	1	0	0	fref (25-60 MHz)	fref · 2 (50-120 MHz)	fref (25-60 MHz)
		1	0	1	fref (25-60 MHz)	fref · 2 (50-120 MHz)	fref 2 ÷ 3 (16.6-40 MHz)
		1	1	0	fref (25-60 MHz)	fref (25-60 MHz)	fref (25-60 MHz)
		1	1	1	fref (25-60 MHz)	fref (25-60 MHz)	fref 2 ÷ 3 (16.6-40 MHz)
VCO ÷ 12[4]	16.67–40	0	0	1	fref · 3 (50-120 MHz)	fref · 3 (50-120 MHz)	fref (16.6-40 MHz)
		0	1	1	fref · 3 (50-120 MHz)	fref · 3 ÷ 2 (25-60 MHz)	fref (16.6-40 MHz)
		1	0	1	fref · 3 ÷ 2 (25-60 MHz)	fref · 3 (50-120 MHz)	fref (16.6-40 MHz)
		1	1	1	fref · 3 ÷ 2 (25-60 MHz)	fref · 3 ÷ 2 (25-60 MHz)	fref (16.6-40 MHz)

1. fref is the input clock reference frequency (CCLK or XTAL)
2. QAx connected to FB_IN and FSELA=0, PWR_DN=0
3. QAx connected to FB_IN and FSELA=1, PWR_DN=0
4. QCx connected to FB_IN and FSELC=1, PWR_DN=0

Table 10. MPC9330 Example Configurations (External Feedback and PWR_DN = 1)

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 16[2]	12.5–30	1	0	0	fref (12.5-30 MHz)	fref 2 (25-60 MHz)	fref (12.5-30 MHz)
		1	0	1	fref (12.5-30 MHz)	fref 2 (25-60 MHz)	fref 2 ÷ 3 (8.33-20 MHz)
		1	1	0	fref (12.5-30 MHz)	fref (12.5-30 MHz)	fref (12.5-30 MHz)
		1	1	1	fref (12.5-30 MHz)	fref (12.5-30 MHz)	fref 2 ÷ 3 (8.33-20 MHz)
VCO ÷ 24[3]	8.33–20	0	0	1	fref 3 (25-60 MHz)	fref 3 (25-60 MHz)	fref (8.33-20 MHz)
		0	1	1	fref 3 (25-60 MHz)	fref 3 ÷ 2 (12.5-30 MHz)	fref (8.33-20 MHz)
		1	0	1	fref 3 ÷ 2 (12.5-30 MHz)	fref 3 (25-60 MHz)	fref (8.33-20 MHz)
		1	1	1	fref 3 ÷ 2 (12.5-30 MHz)	fref 3 ÷ 2 (12.5-30 MHz)	fref (8.33-20 MHz)

1. fref is the input clock reference frequency (CCLK or XTAL)
2. QAx connected to FB_IN and FSELA=1, PWR_DN=1
3. QCx connected to FB_IN and FSELC=1, PWR_DN=1

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9330 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9330 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9330. Figure 3 illustrates a typical power supply filter scheme. The MPC9330 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 5 mA (10 mA maximum), assuming that a minimum of 2.985 V must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 3 should have a resistance of 10–15 Ω to meet the voltage drop criteria.

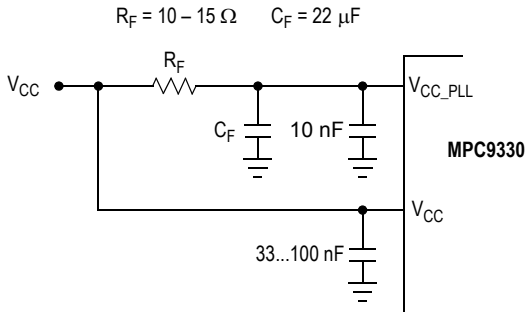


Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9330 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9330 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola Application Note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9330 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9330 clock driver is effectively doubled due to its capability to drive multiple lines.

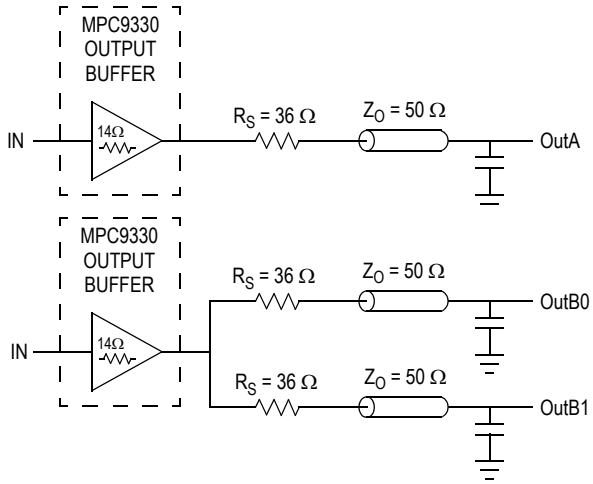


Figure 4. Single versus Dual Transmission Lines

The waveform plots in Figure 4 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9330 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9330. The output waveform in Figure 5. Single versus Dual Waveforms shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output

impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S+R_0 +Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18+14+25)$$
$$= 1.31\ V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

1. Final skew data pending specification.

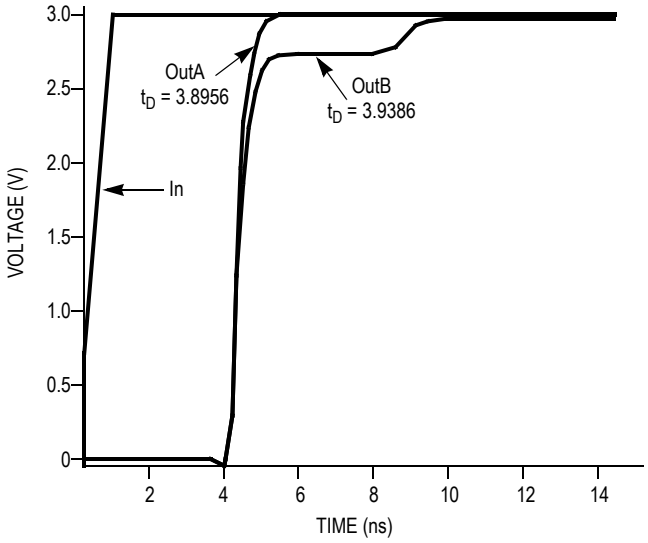
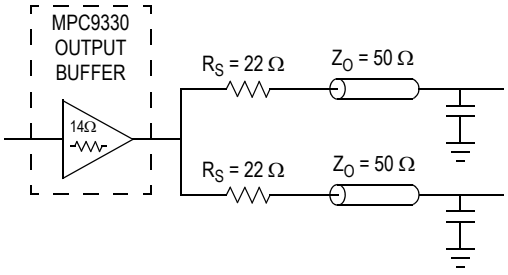


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\Omega + 22\ \Omega \parallel 22\ \Omega = 50\ \Omega \parallel 50\ \Omega$
$25\ \Omega = 25\ \Omega$

Figure 6. Optimized Dual Line Termination

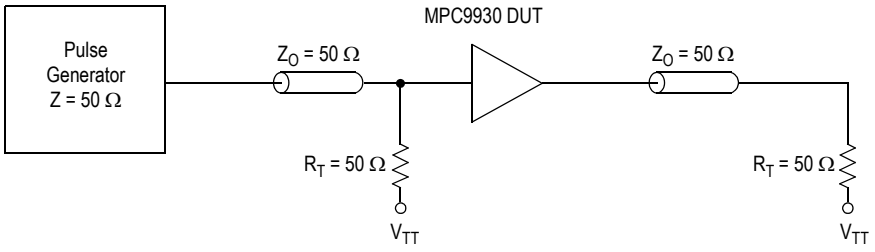
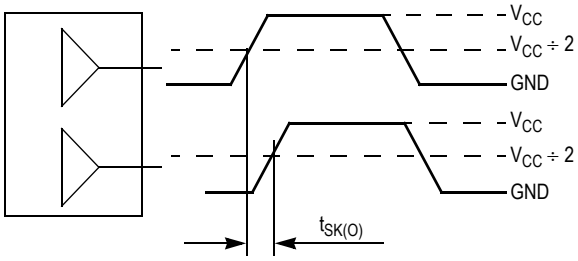


Figure 7. CCLK MPC9330 AC Test Reference for V_{cc} = 3.3 V



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output-to-Output Skew $t_{SK(O)}$

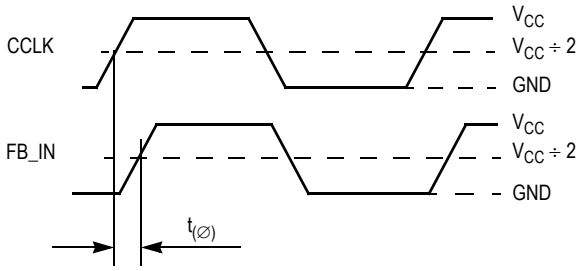
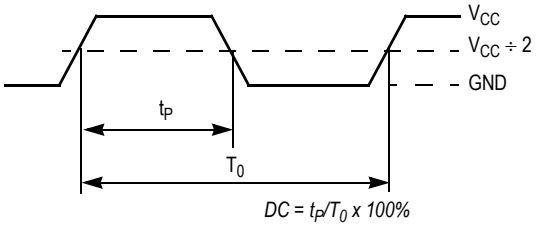
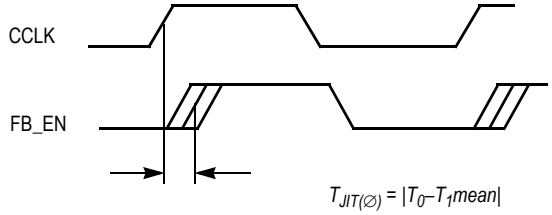


Figure 9. Propagation Delay ($t_{(\varnitheta)}$, static phase offset) Test Reference



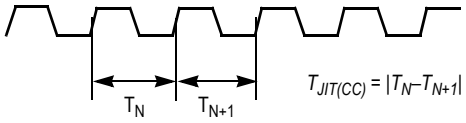
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 10. Output Duty Cycle (DC)



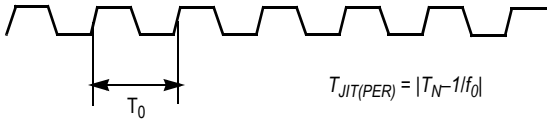
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 11. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 12. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 13. Period Jitter

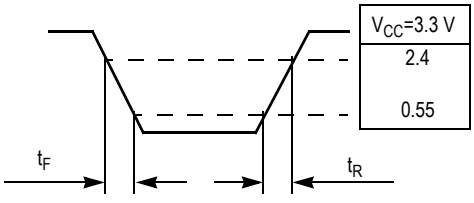


Figure 14. Output Transition Time Test Reference

3.3V 1:6 LVCMOS PLL Clock Generator

MPC9331

LOW VOLTAGE
3.3V LVCMOS 1:6
CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC9331 is a 3.3V compatible, 1:6 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking, and computing applications. With output frequencies up to 240 MHz and output skews less than 150 ps, the device meets the needs of most the demanding clock applications. The MPC9331 is specified for the temperature range of 0°C to +70°C.

Features

- 1:6 PLL based low-voltage clock generator
- 3.3V power supply
- Generates clock signals up to 240 MHz
- Maximum output skew of 150 ps
- Differential LVPECL reference clock input
- Alternative LVCMOS PLL reference clock input
- Internal and external PLL feedback
- Supports zero-delay operation in external feedback mode
- PLL multiplies the reference clock by 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3 or x/4
- Synchronous output clock stop in logic low eliminates output runt pulses
- Power_down feature reduces output clock frequency
- Drives up to 12 clock lines
- 32-lead LQFP packaging
- 32-lead Pb-free Package Available
- Ambient temperature range 0°C to +70°C
- Internal Power-Up Reset
- Pin and function compatible to the MPC931

Functional Description

The MPC9331 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9331 requires either the selection of internal PLL feedback or the connection of one of the device outputs to the feedback input to close the PLL feedback path in external feedback mode. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. In external PLL feedback configuration and with the available post-PLL dividers (divide-by-2, divide-by-4, and divide-by-6), the internal VCO of the MPC9331 is running at either 2x, 4x, 6x, 8x, or 12x of the reference clock frequency. In internal feedback configuration (divide-by-8) the internal VCO is running 8x of the reference frequency. The frequency of the QA, QB, QC output banks is a division of the VCO frequency and can be configured independently for each output bank using the FSELA, FSELB, and FSELC pins, respectively. The available output to input frequency ratios are 4x, 3x, 2x, 1x, 4/3x, 3/2x, 2/3x, x/2, x/3, or x/4.

The REF_SEL pin selects the differential LVPECL or the LVCMOS compatible input as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) by deasserting the OE/$\overline{\text{MR}}$ pin. In the PLL configuration with external feedback selected, deasserting OE/$\overline{\text{MR}}$ causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Asserting OE/$\overline{\text{MR}}$ will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation. The MPC9331 output clock stop control allows the outputs to start and stop synchronously in logic low state, without the potential generation of runt pulses.

The MPC9331 is fully 3.3V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS except signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9331 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

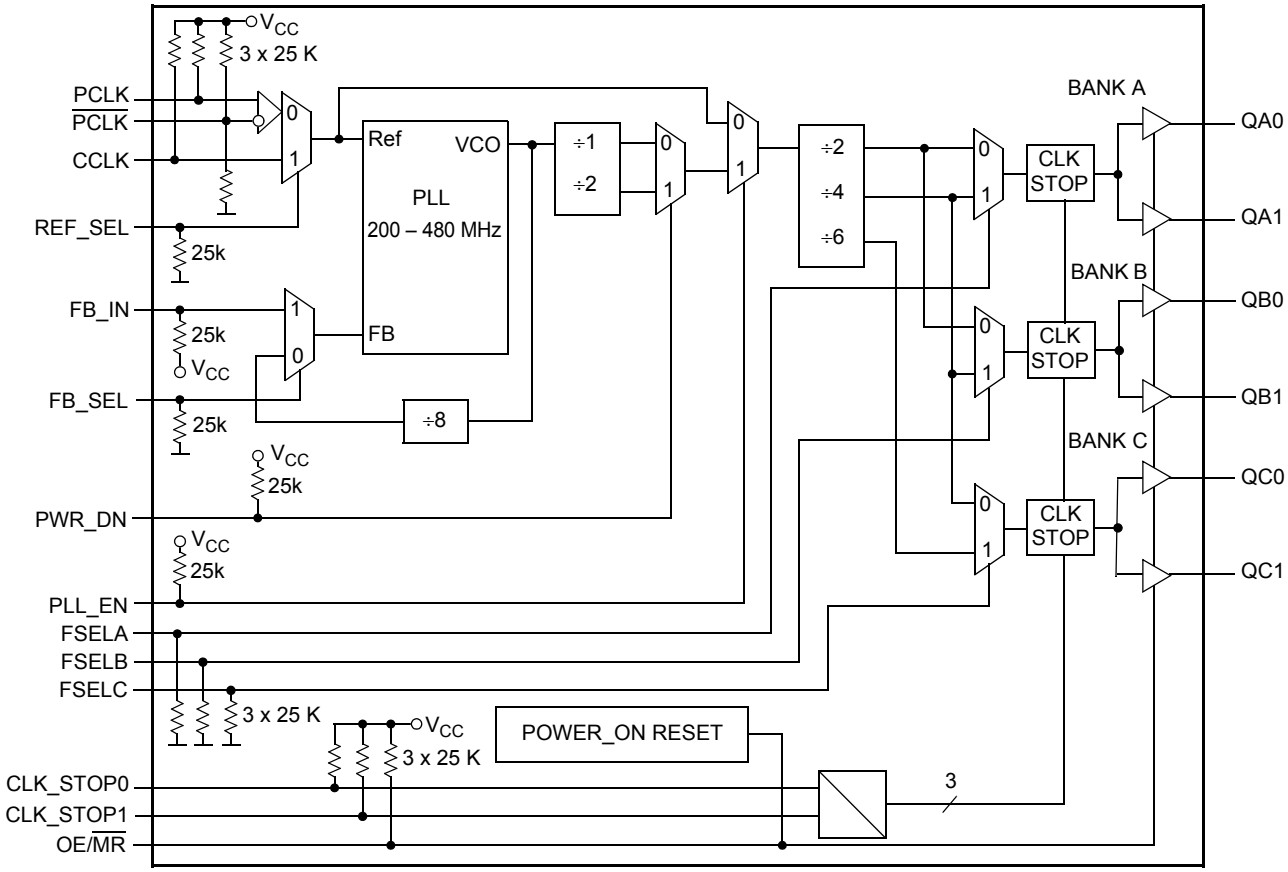
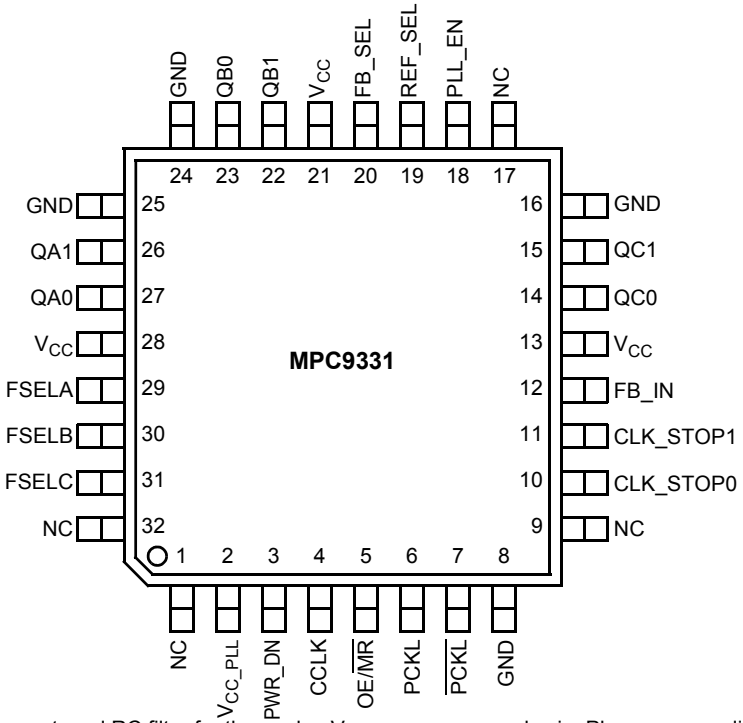


Figure 1. MPC9331 Logic Diagram



It is recommended to use an external RC filter for the analog V_{CC_PLL} power supply pin. Please see application section for details.

Figure 2. MPC9331 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVCMOS	PLL reference clock signal
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	Differential PECL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to an output
FB_SEL	Input	LVCMOS	Feedback select
REF_SEL	Input	LVCMOS	Reference clock select
PWR_DN	Input	LVCMOS	Output frequency and power down select
FSELA	Input	LVCMOS	Frequency divider select for bank A outputs
FSELB	Input	LVCMOS	Frequency divider select for bank B outputs
FSELC	Input	LVCMOS	Frequency divider select for bank C outputs
PLL_EN	Input	LVCMOS	PLL enable/disable
CLK_STOP0-1	Input	LVCMOS	Clock output enable/disable
OE/$\overline{\text{MR}}$	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
QA0-1, QB0-1, QC0-1	Output	LVCMOS	Clock outputs
GND	Supply	Ground	Negative power supply (GND)
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use external RC filter for the analog power supply pin $V_{CC\_PLL.}$ Please see applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	PCLK is the PLL reference clock	CCLK is the PLL reference clock
FB_SEL	1	Internal PLL feedback of 8. $f_{VCO} = 8 * f_{ref}$	External feedback. Zero-delay operation enabled for CCLK or PCLK as reference clock
PLL_EN	1	Test mode with PLL disabled. The reference clock is substituted for the internal VCO output. MPC9331 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
PWR_DN	1	VCO ÷ 1 (High output frequency range)	VCO ÷ 2 (Low output frequency range)
FSELA	0	Output divider ÷ 2	Output divider ÷ 4
FSELB	0	Output divider ÷ 2	Output divider ÷ 4
FSELC	0	Output divider ÷ 4	Output divider ÷ 6
OE/$\overline{\text{MR}}$	1	Outputs disabled (high-impedance state) and reset of the device. During reset in external feedback configuration, the PLL feedback loop is open. The VCO is tied to its lowest frequency. The MPC9331 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLK or PCLK). Reset does not affect PLL lock in internal feedback configuration.	Outputs enabled (active)
CLK_STOP[0:1]	11	See Table 3	

PWR_DN, FSELA, FSELB and FSELC control the operating PLL frequency range and input/output frequency ratios.
See Table 8 through Table 10 for supported frequency ranges and output to input frequency ratios.

Table 3. Clock Output Synchronous Disable (CLK_STOP) Function Table[1]

CLK_STOP0	CLK_STOP1	QA[0:1]	QB[0:1]	QC[0:1]
0	0	Active	Stopped in logic L state	Stopped in logic L state
0	1	Active	Stopped in logic L state	Active
1	0	Stopped in logic L state	Stopped in logic L state	Active
1	1	Active	Active	Active

1. Output operation for OE/$\overline{MR}$=1 (outputs enabled). OE/$\overline{MR}$=0 will disable (high-impedance state) all outputs independent on CLK_STOP[0:1]

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage				0.8	V	LVCMOS
V_{PP}	Peak-to-peak input voltage	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK, $\overline{PCLK}$	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA[2]
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output impedance			14 – 17		Ω	
I_{IN}	Input Current[3]				±200	μA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current			8.0	12	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current[4]				26	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification
2. The MPC9331 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
3. Inputs have pull-down or pull-up resistors affecting the input current.
4. OE/$\overline{MR}$=0 (outputs in high-impedance state).

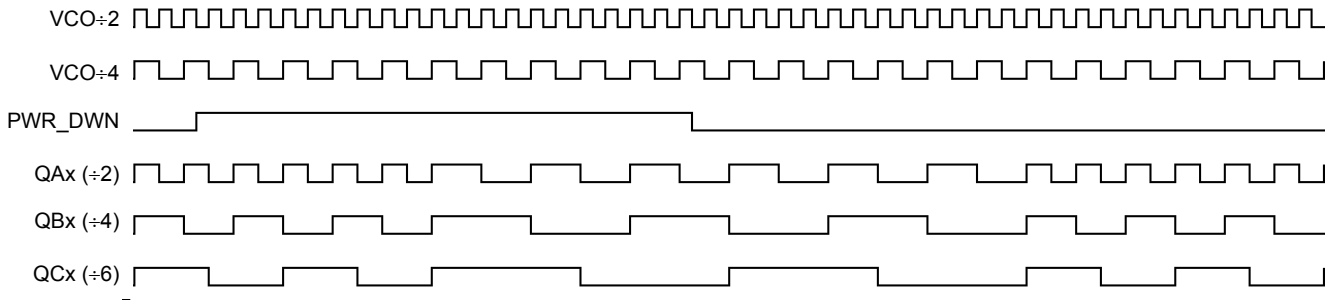
Table 7. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to 70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input reference frequency PLL mode, external feedback PLL mode, internal feedback Input reference frequency in PLL bypass mode[2]	÷2 feedback ÷4 feedback ÷6 feedback ÷8 feedback ÷12 feedback (÷8 feedback)	100.0 50.0 33.3 25.0 16.67 25.0		240.0 120.0 80.0 60.0 40.0 60.0 240	MHz MHz MHz MHz MHz MHz MHz	PLL locked
f_{VCO}	VCO lock frequency range[3]		200		480	MHz	
f_{MAX}	Output Frequency	÷2 output ÷4 output ÷6 output ÷8 output ÷12 output	100.0 50.0 33.3 25.0 16.67		240.0 120.0 80.0 60.0 40.0	MHz MHz MHz MHz MHz	PLL locked
V_{PP}	Peak-to-peak input voltage	PCLK, $\overline{PCLK}$	400		1000	mV	LVPECL
V_{CMR}[4]	Common Mode Range	PCLK, $\overline{PCLK}$	1.2		V_{CC} – 0.9	V	LVPECL
$t_{PW,MIN}$	Input Reference Pulse Width[5]		2.0			ns	
t_R, t_F	CCLK Input Rise/Fall Time[6]				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)	CCLK to FB_IN[7] PCLK to FB_IN[9] CCLK or PCLK to FB_IN[8]	–250 –180 –3.0	–130 –30	–50 +120 +3.0	ps ps °	FB_SEL = 1 and PLL locked
$t_{sk(O)}$	Output-to-output Skew				150	ps	
DC	Output duty cycle[9]		(T÷2)–500	T÷2	(T÷2)+500	ps	
t_R, t_F	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				8.0	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter[10]				200	ps	
$t_{JIT(PER)}$	Period Jitter				125	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1 σ)			25	ps	
BW	PLL closed loop bandwidth[11] PLL mode, external feedback	÷ 4 feedback ÷ 6 feedback ÷ 8 feedback ÷12 feedback		2.0–8.0 1.2–4.0 1.0–3.0 0.7–2.0		MHz MHz MHz MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

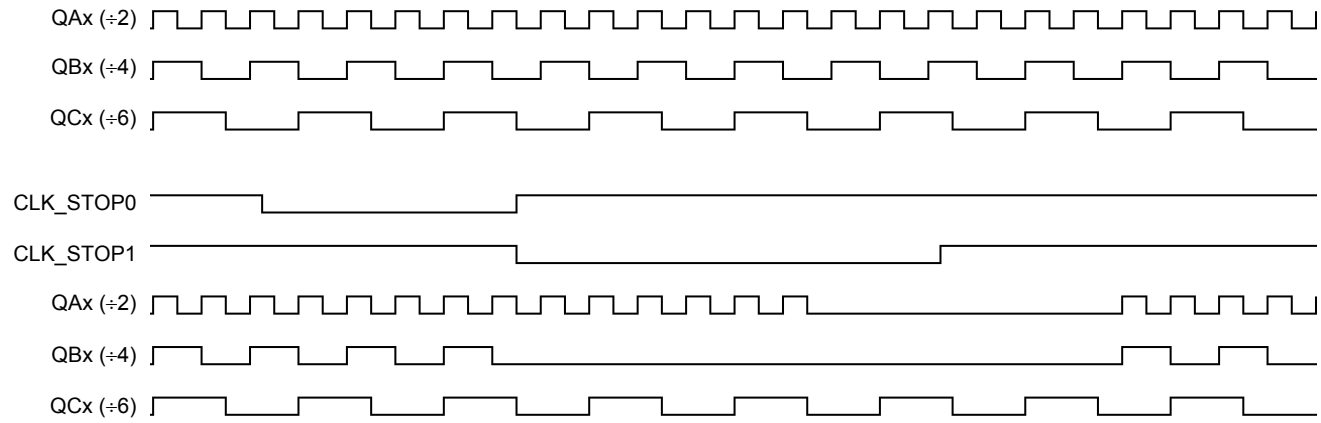
1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. In bypass mode, the MPC9331 divides the input reference clock.
3. The input frequency f_{REF} must match the VCO frequency range divided by the feedback divider ratio FB: $f_{REF} = f_{VCO} \div FB$.
4. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
5. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% – DC_{REF,MIN}$.
6. The MPC9331 will operate with input rise/fall times up to 3.0 ns, but the AC characteristics, specifically $t_{(\varnothing)}$, $t_{PW,MIN}$, DC and f_{MAX} can only be guaranteed if t_R, t_F are within the specified range.
7. Data valid for f_{REF}=50 MHz and a PLL feedback of ÷8 (e.g. QAx connected to FB_IN and FSELA=1, PWR_DN=1).
8. Data valid for 16.67 MHz < f_{REF} < 100 MHz and any feedback divider. $t_{sk(O)}$ [s] = $t_{sk(O)}$ [°] ÷ ($f_{REF} \cdot 360°$).
9. Output duty cycle is DC = (0.5 ± 500 ps · f_{OUT}) · 100%. (e.g. the DC range at f_{OUT} = 100 MHz is 45% < DC < 55%).
10. All outputs in ÷4 divider configuration.
11. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Output Power Down (PWR_DN) Timing Diagram



Output Clock Stop (CLK_STOP) Timing Diagram



Programming the MPC9331

The MPC9331 supports output clock frequencies from 16.67 to 240 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 480 MHz for stable and optimal operation. The FSELA, FSELB, FSELC and PWR_DN pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 4:1, 3:1, 2:1, 1:1, 1:2, 2:3 and 3:2. Table 8 illustrates the various output configurations and frequency ratios supported by the MPC9331. See also Table 9 and Table 10 for further reference.

Table 8. MPC9331 Example Configurations (Internal Feedback: FB_SEL = 0)

fref[1] [MHz]	PWR_DN	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
25.0 – 60.0	0	0	0	0	fref · 4 (100-240 MHz)	fref · 4 (100-240 MHz)	fref · 2 (50-120 MHz)
	0	0	0	1	fref · 4 (100-240 MHz)	fref · 4 (100-240 MHz)	fref ·4÷3 (33.3-80 MHz)
	0	0	1	0	fref · 4 (100-240 MHz)	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)
	0	0	1	1	fref · 4 (100-240 MHz)	fref · 2 (50-120 MHz)	fref ·4÷3 (33.3-80 MHz)
	0	1	0	0	fref · 2 (50-120 MHz)	fref · 4 (100-240 MHz)	fref · 2 (50-120 MHz)
	0	1	0	1	fref · 2 (50-120 MHz)	fref · 4 (100-240 MHz)	fref ·4÷3 (33.3-80 MHz)
	0	1	1	0	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)
	0	1	1	1	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)	fref ·4÷3 (33.3-80 MHz)
	1	0	0	0	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)	fref (25.0-60 MHz)
	1	0	0	1	fref · 2 (50-120 MHz)	fref · 2 (50-120 MHz)	fref ·2÷3 (16.67-40 MHz)
	1	0	1	0	fref · 2 (50-120 MHz)	fref (25.0-60 MHz)	fref (25.0-60 MHz)
	1	0	1	1	fref · 2 (50-120 MHz)	fref (25.0-60 MHz)	fref ·2÷3 (16.67-40 MHz)
	1	1	0	0	fref (25.0-60 MHz)	fref · 2 (50-120 MHz)	fref (25.0-60 MHz)
	1	1	0	1	fref (25.0-60 MHz)	fref · 2 (50-120 MHz)	fref ·2÷3 (16.67-40 MHz)
	1	1	1	0	fref (25.0-60 MHz)	fref (25.0-60 MHz)	fref (25.0-60 MHz)
	1	1	1	1	fref (25.0-60 MHz)	fref (25.0-60 MHz)	fref ·2÷3 (16.67-40 MHz)

1. fref is the input clock reference frequency (CCLK or PCLK)

Table 9. MPC9331 Example Configurations (External Feedback and PWR_DN = 0)

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 2[2]	100 – 240	0	0	0	fref (100-240 MHz)	fref (100-240 MHz)	fref ÷ 2 (50-120 MHz)
		0	0	1	fref (100-240 MHz)	fref (100-240 MHz)	fref ÷ 3 (33.3-80 MHz)
		0	1	0	fref (100-240 MHz)	fref ÷ 2 (50-120 MHz)	fref ÷ 2 (50-120 MHz)
		0	1	1	fref (100-240 MHz)	fref ÷ 2 (50-120 MHz)	fref ÷ 3 (33.3-80 MHz)
VCO ÷ 4[3]	50 –120	1	0	0	fref (50-120 MHz)	fref ·2 (100-240 MHz)	fref (50-120 MHz)
		1	0	1	fref (50-120 MHz)	fref ·2 (100-240 MHz)	fref ·2÷3 (33.3-80 MHz)
		1	1	0	fref (50-120 MHz)	fref (100-240 MHz)	fref (50-120 MHz)
		1	1	1	fref (50-120 MHz)	fref (100-240 MHz)	fref ·2 ÷ 3 (33.3-80 MHz)
VCO ÷ 6[4]	33.3 – 80	0	0	1	fref ·3 (100-240 MHz)	fref ·3 (100-240 MHz)	fref (33.3-80 MHz)
		0	1	1	fref ·3 (100-240 MHz)	fref ·3 ÷ 2 (50-120 MHz)	fref (33.3-80 MHz)
		1	0	1	fref ·3 ÷ 2 (50-120 MHz)	fref ·3 (100-240 MHz)	fref (33.3-80 MHz)
		1	1	1	fref ·3 ÷ 2 (50-120 MHz)	fref ·3 ÷ 2 (50-120 MHz)	fref (33.3-80 MHz)

1. fref is the input clock reference frequency (CCLK or PCLK)
2. QAx connected to FB_IN and FSELA=0, PWR_DN=0
3. QAx connected to FB_IN and FSELA=1, PWR_DN=0
4. QCx connected to FB_IN and FSELC=1, PWR_DN=0

Table 10. MPC9331 Example Configurations (External Feedback and PWR_DN = 1**)**

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:1]:fref ratio	QB[0:1]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 8[2]	25.0 – 60.0	1	0	0	fref 25-60 MHz)	fref ·2 (50-120 MHz)	fref (2.25-60 MHz)
		1	0	1	fref (25-60 MHz)	fref ·2 (50-120 MHz)	fref ·2÷3 (16.6-40 MHz)
		1	1	0	fref (25-60 MHz)	fref (25-60 MHz)	fref (25-60 MHz)
		1	1	1	fref (25-60 MHz)	fref (25-60 MHz)	fref ·2÷3 (16.6-40 MHz)
VCO ÷ 12[3]	16.67 – 40	0	0	1	fref ·3 (50-120 MHz)	fref ·3 (50-120 MHz)	fref (16.67-40 MHz)
		0	1	1	fref ·3 (50-120 MHz)	fref ·3 ÷ 2 (25-60 MHz)	fref (16.67-40 MHz)
		1	0	1	fref ·3 ÷ 2 (25-60 MHz)	fref ·3 (50-120 MHz)	fref (16.67-40 MHz)
		1	1	1	fref ·3 ÷ 2 (25-60 MHz)	fref ·3 ÷ 2 (25-60 MHz)	fref (16.67-40 MHz)

1. fref is the input clock reference frequency (CCLK or PCLK)
2. QAx connected to FB_IN and FSELA=1, PWR_DN=1
3. QCx connected to FB_IN and FSELC=1, PWR_DN=1

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9331 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9331 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9331. Figure 3 illustrates a typical power supply filter scheme. The MPC9331 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 8 mA (12 mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CC_PLL} pin.

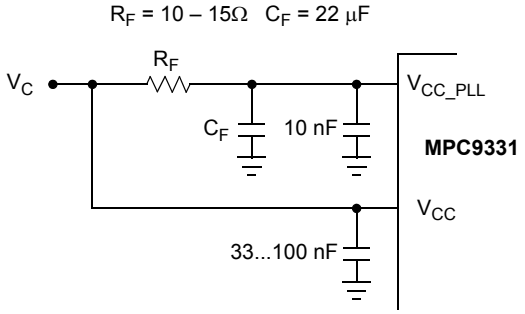


Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for RF and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9331 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9331 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9331 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9331 clock driver is effectively doubled due to its capability to drive multiple lines.

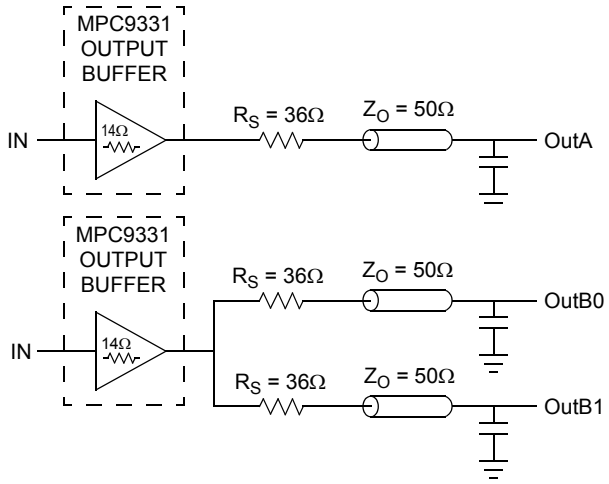


Figure 4. Single versus Dual Transmission Lines

The waveform plots in Figure 5. Single versus Dual Line Termination Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9331 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9331. The output waveform in Figure 5. Single versus Dual Line Termination Waveforms shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel

combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S+R_0 +Z_0))$

$Z_0 = 50\Omega \parallel 50\Omega$

$R_S = 36\Omega \parallel 36\Omega$

$R_0 = 14\Omega$

$V_L = 3.0 (25 \div (18+14+25)$

$= 1.31V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification.

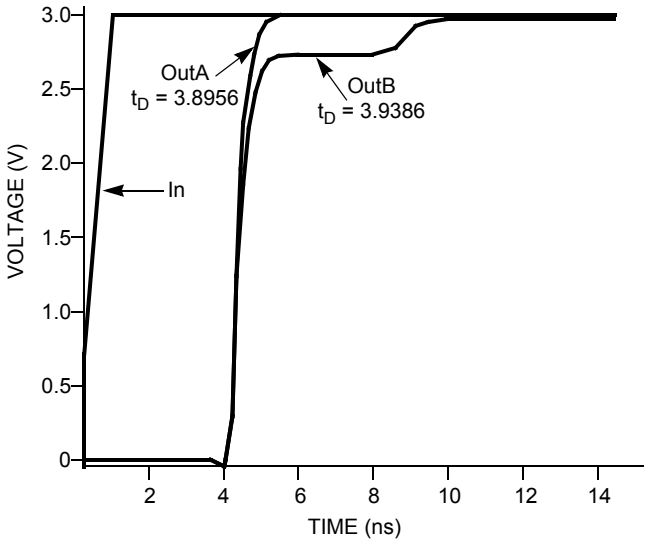


Figure 5. Single versus Dual Line Termination Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

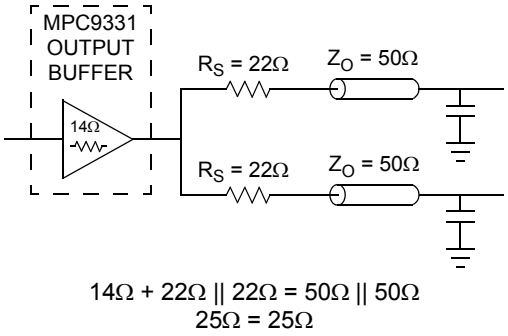


Figure 6. Optimized Dual Line Termination

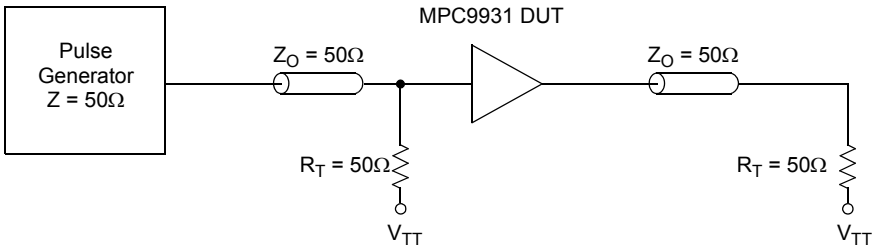
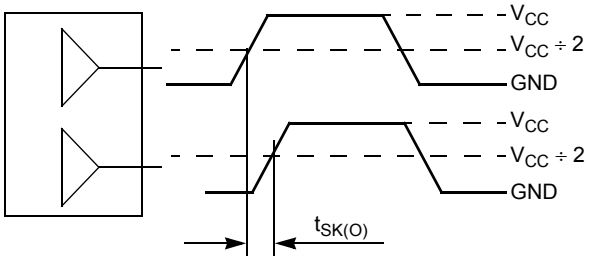


Figure 7. CCLK MPC9331 AC Test Reference for V_{cc} = 3.3V



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output-to-Output Skew $t_{SK(O)}$

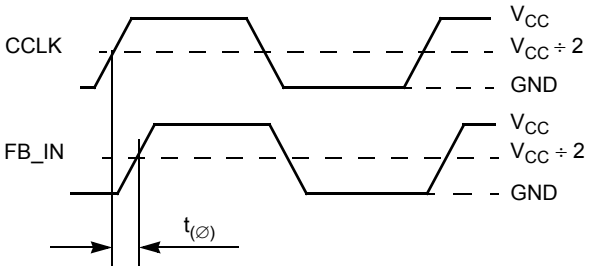
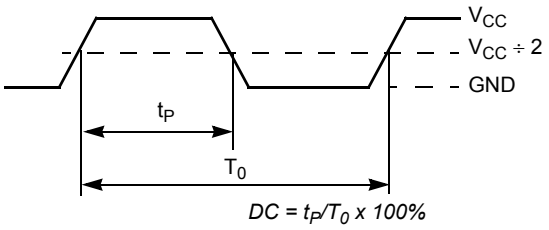
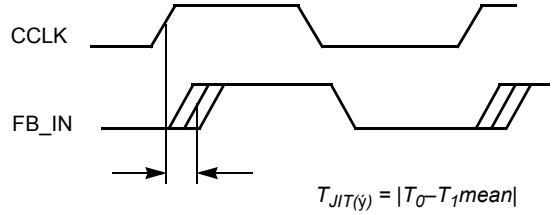


Figure 9. Propagation Delay ($t_{(\varnothing)}$, Static Phase offset) Test Reference



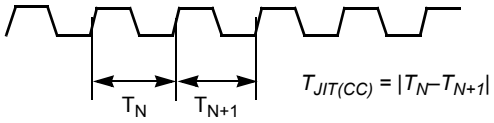
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 10. Output Duty Cycle (DC)



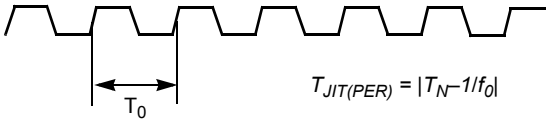
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 11. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 12. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 13. Period Jitter

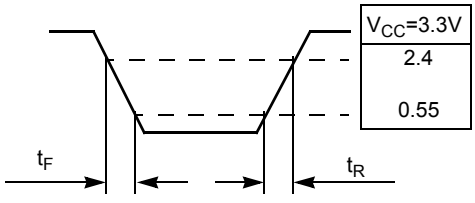


Figure 14. Output Transition Time Test Reference

Low Voltage PLL Clock Driver

MPC9350

**LOW VOLTAGE
3.3V AND 2.5V PLL
CLOCK GENERATOR**

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC9350 is a 2.5V and 3.3V compatible, PLL-based clock generator targeted for high performance clock distribution systems. With output frequencies of up to 200 MHz and maximum output skews of 150 ps, the MPC9350 is ideal for the most demanding clock tree designs. The device offers 9 low skew clock outputs, with each one configurable to support the clocking needs of the various high-performance microprocessors, including the PowerQuicc II integrated communication microprocessor. The extended temperature range of the MPC9350 supports telecommunication and networking requirements. The device employs a fully differential PLL design to minimize cycle-to-cycle and long-term jitter.

Features

- 9 output LVCMOS PLL clock generator
- 25 – 200 MHz output frequency range
- 2.5V and 3.3V compatible
- Compatible to various microprocessors such as PowerQuicc II
- Supports networking, telecommunications and computer applications
- Fully integrated PLL
- Configurable outputs: divide-by-2, 4 and 8 of VCO frequency
- Selectable output to input frequency ratio of 8:1, 4:1, 2:1 or 1:1
- Oscillator or crystal reference inputs
- Internal PLL feedback
- Output disable
- PLL enable/disable
- Low skew characteristics: maximum 150 ps output-to-output
- 32-lead LQFP package
- 32-lead Pb-free Package Available
- Temperature range –40°C to +85°C

Functional Description

The MPC9350 generates high frequency clock signals and provides nine exact frequency-multiplied copies of the reference clock signal. The internal PLL allows the MPC9350 to operate in frequency locked condition and to multiply the input reference clock. The reference clock frequency and the divider in the internal feedback path determine the VCO frequency. Two selectable PLL feedback frequency ratios are available on the MPC9350 to provide input frequency range flexibility. The FBSEL pin selects between divide-by-16 or divide-by-32 of the VCO frequency for PLL feedback. This feedback divider must be selected to match the VCO frequency range. With the available feedback output dividers, the internal VCO of the MPC9350 is running at either 16x or 32x of the reference clock frequency. The frequency of the QA, QB, QC and QD outputs is either one half, one fourth or one eighth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB, FSELC and FSELD pins, respectively. The available output to input frequency ratios are 16:1, 8:1, 4:1 and 2:1. The REF_SEL pin selects the crystal oscillator input or the LVCMOS compatible reference input (TCLK). TCLK also provides an external test clock in static test mode when the PLL enable pin (PLL_EN) is pulled to logic low state. In test mode, the selected input reference clock is routed directly to the output dividers without using the PLL. The test mode is intended for system diagnostics, test and debug purposes. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the $\overline{OE}$ pin (logic high state). In PLL mode, deasserting $\overline{OE}$ maintains PLL lock due to the internal feedback path. The MPC9350 is fully 2.5V and 3.3V compatible and requires no external loop filter components. The on-chip crystal oscillator requires no external components beyond a series resonant crystals. All inputs except the crystal oscillator interface accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9350 outputs can drive one or two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

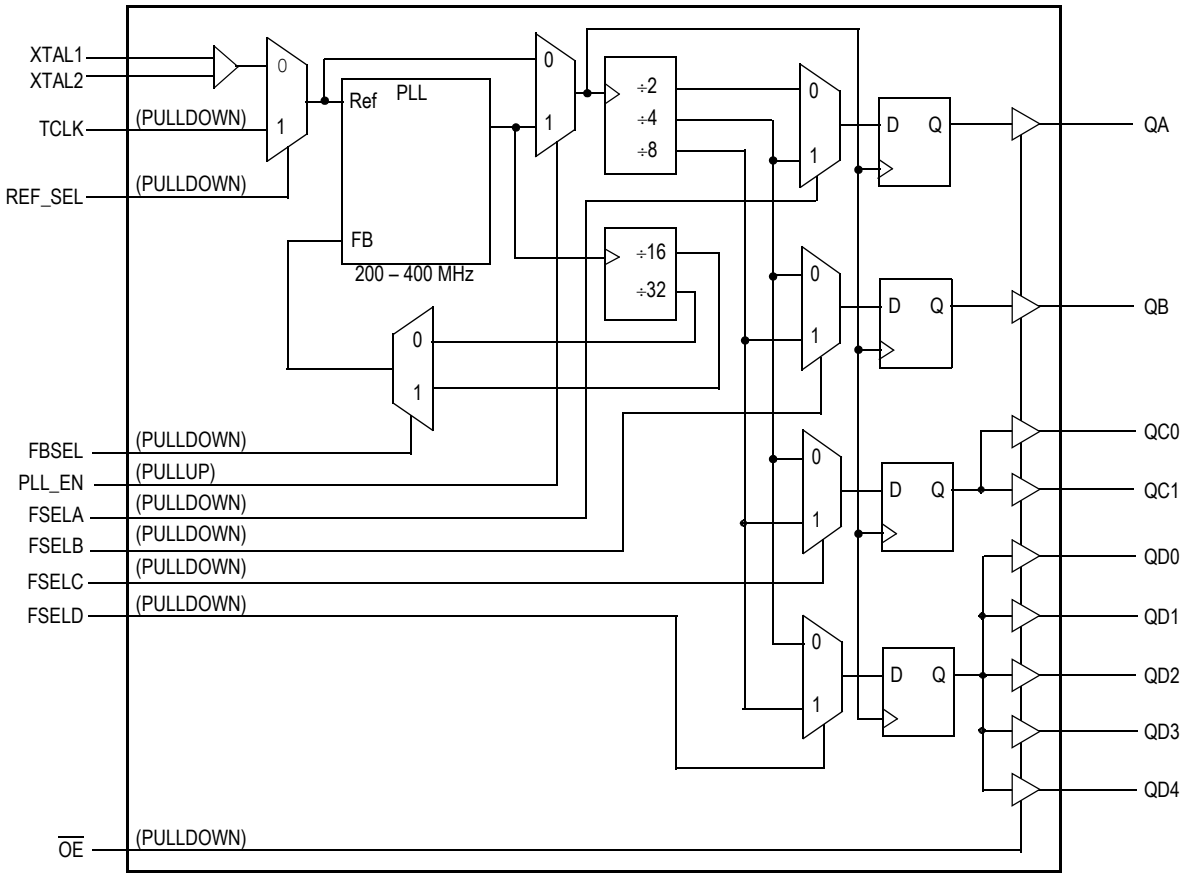


Figure 1. MPC9350 Logic Diagram

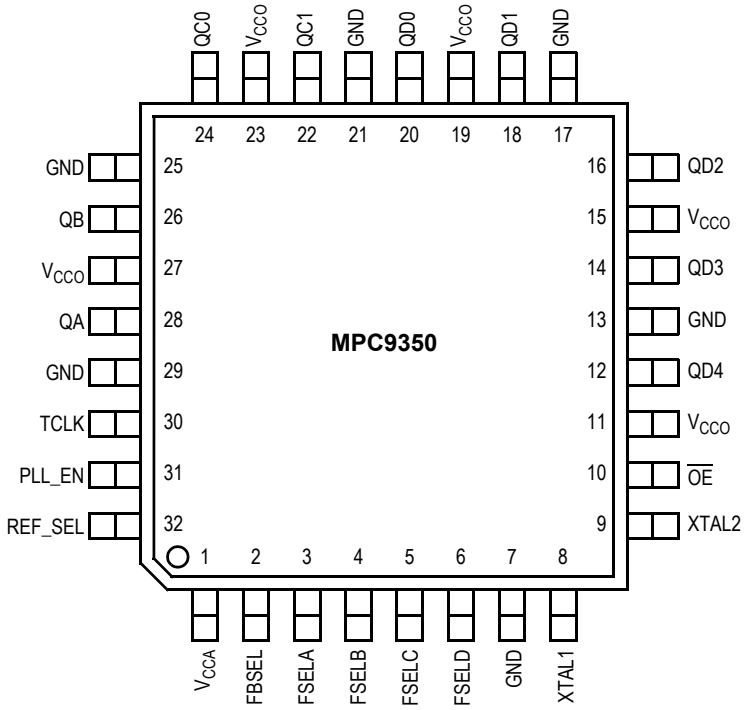


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1. Pin Description

Number	Name	Type	Description
XTAL1, XTAL2	Input	Analog	Crystal oscillator terminals
TCLK	Input	LVCMOS	Single ended reference clock signal or test clock
FBSEL	Input	LVCMOS	Selects feedback divider ratio
REF_SEL	Input	LVCMOS	Selects input reference source
FSELA	Input	LVCMOS	Output A divider selection
FSELB	Input	LVCMOS	Output B divider selection
FSELC	Input	LVCMOS	Outputs C divider selection
FSELD	Input	LVCMOS	Outputs D divider selection
OE	Input	LVCMOS	Output enable/disable
QA	Output	LVCMOS	Bank A clock output
QB	Output	LVCMOS	Bank B clock output
QC0, QC1	Output	LVCMOS	Bank C clock outputs
QD0 – QD4	Output	LVCMOS	Bank D clock outputs
GND	Supply	Ground	Negative power supply
V_{CCA}	Supply	V_{CC}	Positive power supply for the PLL
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	Selects XTAL	Selects TCLK
PLL_EN	1	Test mode with PLL disabled. The input clock is directly routed to the output dividers	PLL enabled. The VCO output is routed to the output dividers
FBSEL	0	Selects feedback divider ÷ 32 VCO = 32 * Input reference clock	Selects feedback divider ÷ 16 VCO = 16 * Input reference clock
$\overline{OE}$	0	Outputs enabled	Outputs disabled
FSELA	0	QA = VCO ÷ 2	QA = VCO ÷ 4
FSELB	0	QB = VCO ÷ 4	QB = VCO ÷ 8
FSELC	0	QC = VCO ÷ 4	QC = VCO ÷ 8
FSELD	0	QD = VCO ÷ 4	QD = VCO ÷ 8

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	4.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	–40	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage	–0.3		0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH}=–24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24 mA I_{OL}= 12 mA
I_{IN}	Input Current			200	µA	V_{IN} = 0V or V_{IN} = V_{CC}
Z_{OUT}	Output impedance		14 – 17		Ω	
C_{IN}	Input capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		10		pF	Per Output
I_{CCA}	Maximum PLL Supply Current			10	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins
V_{TT}	Output termination voltage		V_{CC}÷2		V	

1. The MPC9350 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

Table 5. AC Characteristics (V_{CC} = 3.3V ± 5% or V_{CC} = 2.5V ± 5%, T_A = -40° to 85°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency ÷ 16 feedback ÷ 32 feedback Static Test Mode	 12.5 6.25 0		 25 12.5 300	 MHz MHz MHz	 FBSEL = 1 FBSEL = 0 PLL_EN = 0
f_{XTAL}	Crystal Oscillator Frequency	10		25	MHz	XTAL inputs
f_{VCO}	VCO Frequency	200		400	MHz	PLL_EN = 1
f_{MAX}	Maximum Output Frequency ÷ 2 output ÷ 4 output ÷ 8 output	 100 50 25		 200 100 50	 MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle	25		75	%	
t_r, t_f	TLCK Input Rise/Fall Time V_{CC} = 2.5V V_{CC} = 3.3V			1.0 1.0	ns ns	0.7V to 1.7V 0.8V to 2.0V
$t_{sk(o)}$	Output-to-output Skew		45	150	ps	
t_{PW}	Output Duty Cycle	45	50	55	ps	T=Clock period
t_r, t_f	Output Rise/Fall Time	0.1	0.5	1.0	ns	see **Figure 10**
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
BW	PLL closed loop bandwidth ÷ 16 feedback (V_{CC} = 3.3V) ÷ 16 feedback (V_{CC} = 2.5V) ÷ 32 feedback (V_{CC} = 3.3V) ÷ 32 feedback (V_{CC} = 2.5V)		 2.0 – 8.0 1.0 – 4.0 1.5 – 3.5 0.7 – 2.0		 MHz MHz MHz MHz	
$t_{JIT(CC)}$	Cycle-to-cycle jitter single frequency multiple frequencies		30 100	200 300	ps ps	
$t_{JIT(PER)}$	Period Jitter ÷ 16 feedback ÷ 32 feedback		30 80	150 200	ps ps	
t_{LOCK}	Maximum PLL Lock Time			1	ms	
$t_{JIT(∅)}$	I/O Phase Jitter (RMS)		5 – 20		ps	RMS value

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.

Table 6. DC Characteristics (V_{CC} = 2.5V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage	–0.3		0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.8			V	I_{OH} = –15 mA[1]
V_{OL}	Output Low Voltage			0.6	V	I_{OL} = 15 mA
Z_{OUT}	Output impedance		17 – 20		Ω	
I_{IN}	Input Current			200	μA	V_{IN} = 0V or V_{IN} = V_{CC}
C_{IN}	Input capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		10		pF	Per Output
I_{CCA}	Maximum PLL Supply Current			10	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins
V_{TT}	Output termination voltage		V_{CC}÷2		V	

1. The MPC9350 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

APPLICATIONS INFORMATION

Programming the MPC9350

The MPC9350 clock driver outputs can be configured into several divider modes.In addition, the internal feedback of the device allows for flexibility in establishing two input to output frequency relationships. The output division settings establish the output frequency relationship. The output divider of the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 7 and Table 8 illustrate the various output configurations. The tables describe the outputs using the input clock frequency CLK as a reference.

In addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 25 MHz to 200 MHz while the VCO frequency range is specified from 200 MHz to 400 MHz and should not be exceeded for stable operation.

Table 7. Output Frequency Relationship[1] FBSEL = 1, (VC0 = 32 * CLK)

Inputs				Outputs			
FSELA	FSELB	FSELC	FSELD	QA	QB	QC0, QC1	QD0–QD4
0	0	0	0	16 * CLK	8 * CLK	8 * CLK	8 * CLK
0	0	0	1	16 * CLK	8 * CLK	8 * CLK	4 * CLK
0	0	1	0	16 * CLK	8 * CLK	4 * CLK	8 * CLK
0	0	1	1	16 * CLK	8 * CLK	4 * CLK	4 * CLK
0	1	0	0	16 * CLK	4 * CLK	8 * CLK	8 * CLK
0	1	0	1	16 * CLK	4 * CLK	8 * CLK	4 * CLK
0	1	1	0	16 * CLK	4 * CLK	4 * CLK	8 * CLK
0	1	1	1	16 * CLK	4 * CLK	4 * CLK	4 * CLK
1	0	0	0	8 * CLK	8 * CLK	8 * CLK	8 * CLK
1	0	0	1	8 * CLK	8 * CLK	8 * CLK	4 * CLK
1	0	1	0	8 * CLK	8 * CLK	4 * CLK	8 * CLK
1	0	1	1	8 * CLK	8 * CLK	4 * CLK	4 * CLK
1	1	0	0	8 * CLK	4 * CLK	8 * CLK	8 * CLK
1	1	0	1	8 * CLK	4 * CLK	8 * CLK	4 * CLK
1	1	1	0	8 * CLK	4 * CLK	4 * CLK	8 * CLK
1	1	1	1	8 * CLK	4 * CLK	4 * CLK	4 * CLK

1. Output frequency relationship with respect to input reference frequency CLK. Consult the MPC9351 data sheet for more input to output relationships in external feedback mode.

Table 8. Output Frequency Relationship[1] FBSEL = 0, (VC0 = 16 * CLK)

Inputs				Outputs			
FSELA	FSELB	FSELC	FSELD	QA	QB	QC0, QC1	QD0–QD4
0	0	0	0	8 * CLK	4 * CLK	4 * CLK	4 * CLK
0	0	0	1	8 * CLK	4 * CLK	4 * CLK	2 * CLK
0	0	1	0	8 * CLK	4 * CLK	2 * CLK	4 * CLK
0	0	1	1	8 * CLK	4 * CLK	2 * CLK	2 * CLK
0	1	0	0	8 * CLK	2 * CLK	4 * CLK	4 * CLK
0	1	0	1	8 * CLK	2 * CLK	4 * CLK	2 * CLK
0	1	1	0	8 * CLK	2 * CLK	2 * CLK	4 * CLK
0	1	1	1	8 * CLK	2 * CLK	2 * CLK	2 * CLK
1	0	0	0	4 * CLK	4 * CLK	4 * CLK	4 * CLK
1	0	0	1	4 * CLK	4 * CLK	4 * CLK	2 * CLK
1	0	1	0	4 * CLK	4 * CLK	2 * CLK	4 * CLK
1	0	1	1	4 * CLK	4 * CLK	2 * CLK	2 * CLK
1	1	0	0	4 * CLK	2 * CLK	4 * CLK	4 * CLK
1	1	0	1	4 * CLK	2 * CLK	4 * CLK	2 * CLK
1	1	1	0	4 * CLK	2 * CLK	2 * CLK	4 * CLK
1	1	1	1	4 * CLK	2 * CLK	2 * CLK	2 * CLK

1. Output frequency relationship with respect to input reference frequency CLK. Consult the MPC9351 data sheet for more input to output relationships in external feedback mode.

Power Supply Filtering

The MPC9350 is a mixed analog/digital product and as such, it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9350 provides separate power supplies for the output buffers (V_{CCO}) and the phase-locked loop (V_{CCA}) of the device.

The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC9350. Figure 3 illustrates a typical power supply filter scheme. The MPC9350 is most susceptible to noise with spectral content in the 10kHz to 5MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC9350. From the data sheet the I_{VCCA} current (the current sourced through the V_{CCA} pin) is typically 10 mA (15 mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CCA} pin. Very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 3 must have a resistance of 10–15 Ω to meet the voltage drop criteria for V_{CC} = 3.3V. For V_{CC} = 2.5V operation, R_S must be selected to maintain the minimum V_{CC} specification of 2.375V for the PLL supply pin for proper operation. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10 Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

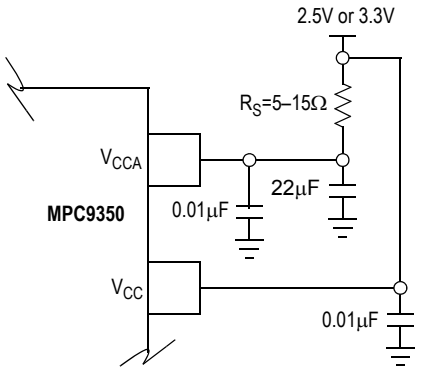


Figure 3. Power Supply Filter

Although the MPC9350 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9350 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 15Ω, the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9350 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9350 clock driver is effectively doubled due to its capability to drive multiple lines.

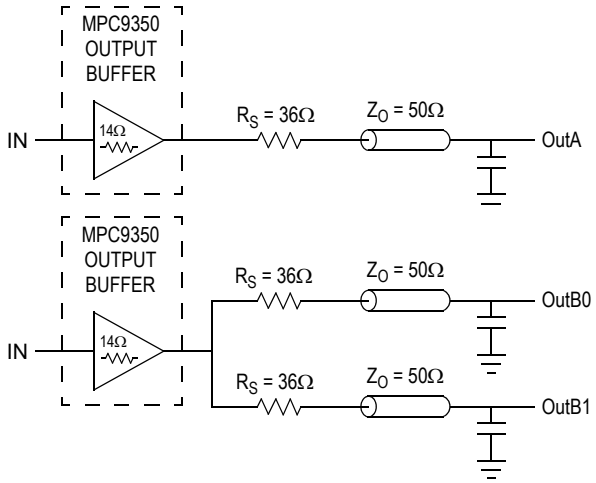


Figure 4. Single versus Dual Transmission Lines

The waveform plots in Figure 5. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9350 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to

maintain the tight output-to-output skew of the MPC9350. The output waveform in Figure 5 shows a step in the waveform. This step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S+R_0 +Z_0))$

$Z_0 = 50\Omega \parallel 50\Omega$

$R_S = 36\Omega \parallel 36\Omega$

$R_0 = 17\Omega$

$V_L = 3.0 (25 \div (18+17+25))$

$= 1.25V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment toward the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

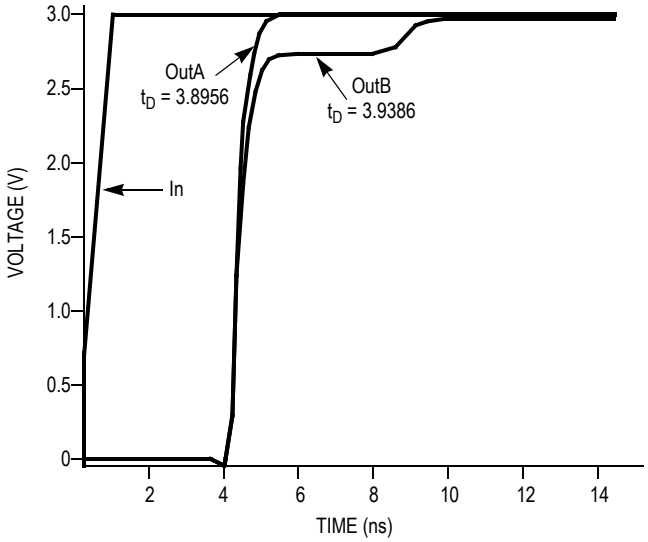
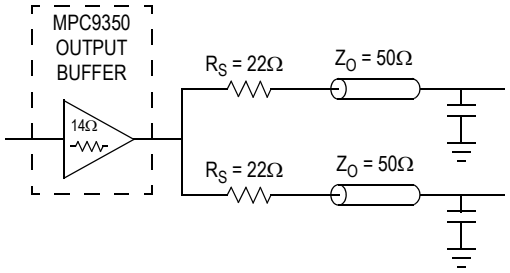


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$

$25\Omega = 25\Omega$

Figure 6. Optimized Dual Line Termination

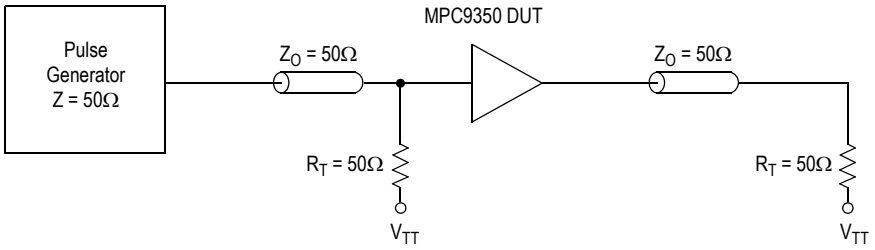
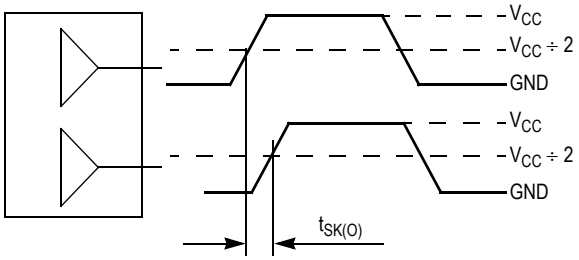
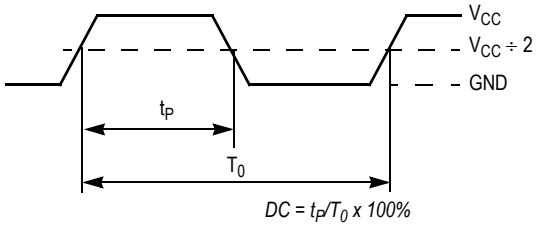


Figure 7. TCLK MPC9350 AC Test Reference for V_{cc} = 3.3V and V_{cc} = 2.5V



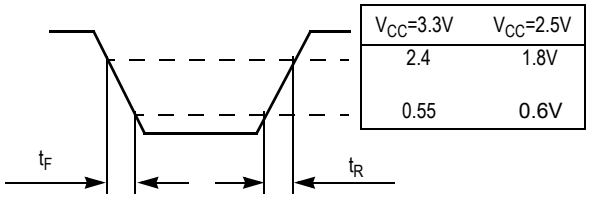
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output-to-Output Skew $t_{SK(O)}$



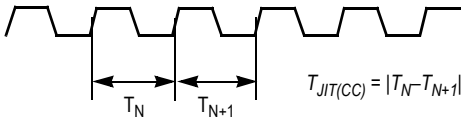
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 9. Output Duty Cycle (DC)



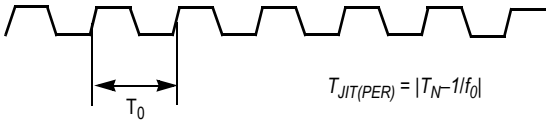
The time from the maximum low level voltage to minimum high level of a clock signal, expressed in ns

Figure 10. Transition Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 11. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 12. Period Jitter

Order number: MPC9351
Rev 3, 08/2004

Low Voltage PLL Clock Driver

MPC9351

LOW VOLTAGE
2.5 V AND 3.3 V PLL
CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC9351 is a 2.5 V and 3.3 V compatible, PLL based clock generator targeted for high performance clock distribution systems. With output frequencies of up to 200 MHz and a maximum output skew of 150 ps the MPC9351 is an ideal solution for the most demanding clock tree designs. The device offers 9 low skew clock outputs, each is configurable to support the clocking needs of the various high-performance microprocessors including the PowerQuicc II integrated communication microprocessor. The extended temperature range of the MPC9351 supports telecommunication and networking requirements.The device employs a fully differential PLL design to minimize cycle-to-cycle and long-term jitter.

Features

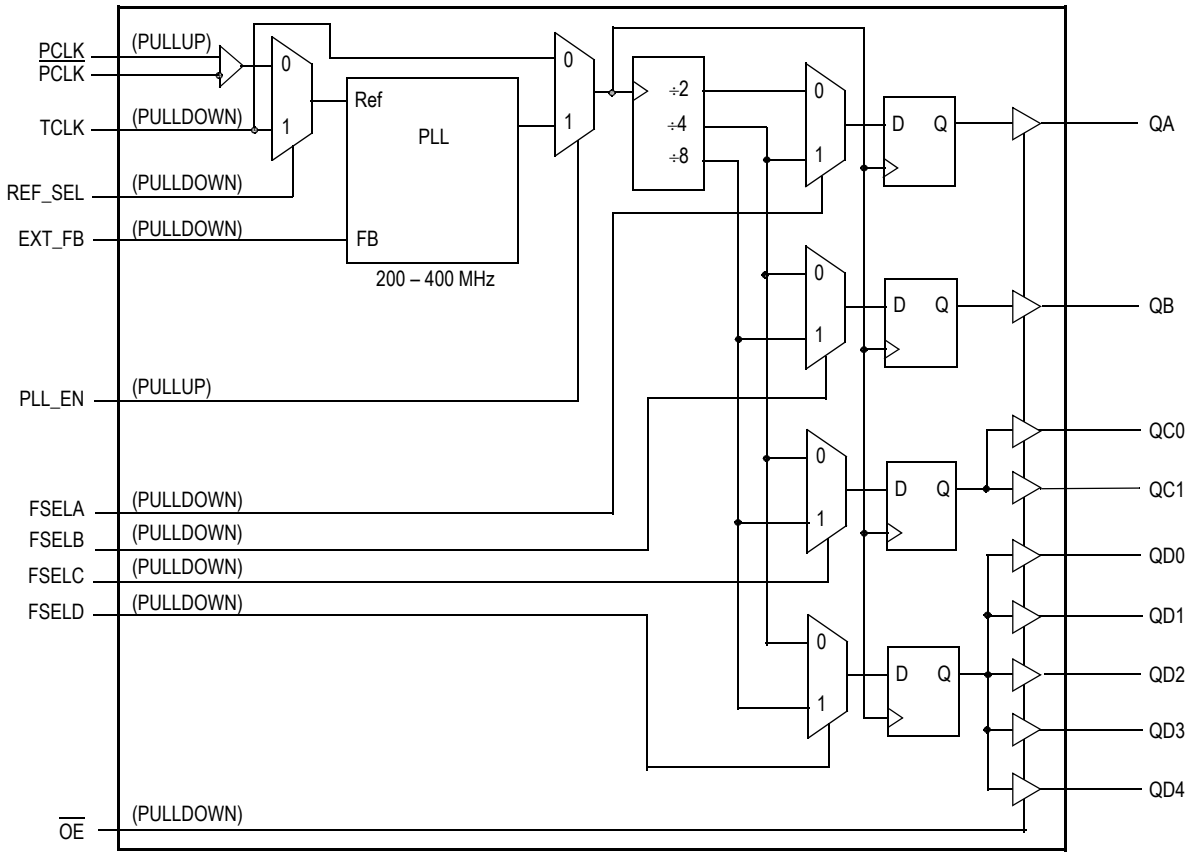
- 9 outputs LVCMOS PLL clock generator
- 25 – 200 MHz output frequency range
- Fully integrated PLL
- 2.5 V and 3.3 V compatible
- Compatible to various microprocessors such as PowerQuicc II
- Supports networking, telecommunications and computer applications
- Configurable outputs: divide-by-2, 4 and 8 of VCO frequency
- LVPECL and LVCMOS compatible inputs
- External feedback enables zero-delay configurations
- Output enable/disable and static test mode (PLL enable/disable)
- Low skew characteristics: maximum 150 ps output-to-output
- Cycle-to-cycle jitter max. 22 ps RMS
- 32-lead LQFP package
- 32-lead Pb-free Package Available
- Ambient Temperature Range -40°C to +85°C

Functional Description

The MPC9351 utilizes PLL technology to frequency and phase lock its outputs onto an input reference clock. Normal operation of the MPC9351 requires a connection of one of the device outputs to the EXT_FB input to close the PLL feedback path. The reference clock frequency and the output divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. With available output dividers of divide-by-2, divide-by-4 and divide-by-8 the internal VCO of the MPC9351 is running at either 2x, 4x or 8x of the reference clock frequency. The frequency of the QA, QB, QC and QD outputs is either the one-half, one-fourth or one-eighth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB, FSELC and FSELD pins, respectively. The available output-to-input frequency ratios are 4:1, 2:1, 1:1, 1:2 and 1:4. The REF_SEL pin selects the differential LVPECL (PCLK and PCLK) or the LVCMOS compatible reference input (TCLK). The MPC9351 also provides a static test mode when the PLL enable pin (PLL_EN) is pulled to logic low state. In test mode, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The test mode is intended for system diagnostics, test and debug purposes. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the $\overline{OE}$ pin (logic high state). In PLL mode, deasserting $\overline{OE}$ causes the PLL to loose lock due to no feedback signal presence at EXT_FB. Asserting $\overline{OE}$ will enable the outputs and close the phase locked loop, also enabling the PLL to recover to normal operation. The MPC9351 is fully 2.5 V and 3.3 V compatible and requires no external loop filter components. All inputs except PCLK and $\overline{PCLK}$ accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9351 outputs can drive one or two traces giving the device an effective fanout of 1:18. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

Application Information

The fully integrated PLL of the MPC9351 allows the low skew outputs to lock onto a clock input and distribute it with essentially zero propagation delay to multiple components on the board. In zero-delay buffer mode, the PLL minimizes phase offset between the outputs and the reference signal.



The MPC9351 requires an external RC filter for the analog power supply pin V_{CCA}. Please see application section for details.

Figure 1. MPC9351 Logic Diagram

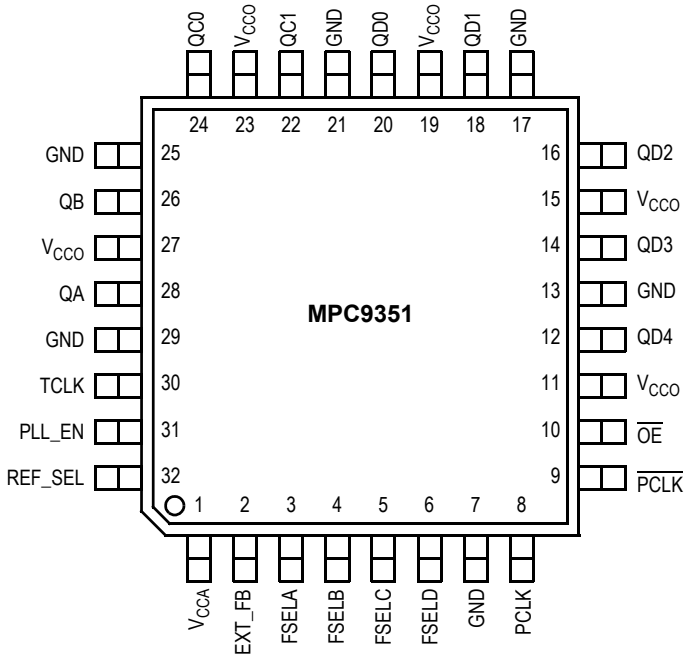


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1. Pin Descriptions

Number	Name	Type	Description
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	Differential clock reference Low voltage positive ECL input
TCLK	Input	LVCMOS	Single ended reference clock signal or test clock
EXT_FB	Input	LVCMOS	Feedback signal input, connect to a QA, QB, QC, QD output
REF_SEL	Input	LVCMOS	Selects input reference clock
FSELA	Input	LVCMOS	Output A divider selection
FSELB	Input	LVCMOS	Output B divider selection
FSELC	Input	LVCMOS	Outputs C divider selection
FSELD	Input	LVCMOS	Outputs D divider selection
$\overline{\text{OE}}$	Input	LVCMOS	Output enable/disable
QA	Output	LVCMOS	Bank A clock output
QB	Output	LVCMOS	Bank B clock output
QC0, QC1	Output	LVCMOS	Bank C clock outputs
QD0 – QD4	Output	LVCMOS	Bank D clock outputs
V_{CCA}	Supply	V_{CC}	Positive power supply for the PLL
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core
GND	Supply	Ground	Negative power supply

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	Selects PCLK as reference clock	Selects TCLK as reference clock
PLL_EN	1	Test mode with PLL disabled. The input clock is directly routed to the output dividers	PLL enabled. The VCO output is routed to the output dividers
$\overline{\text{OE}}$	0	Outputs enabled	Outputs disabled, PLL loop is open VCO is forced to its minimum frequency
FSELA	0	QA = VCO ÷ 2	QA = VCO ÷ 4
FSELB	0	QB = VCO ÷ 4	QB = VCO ÷ 8
FSELC	0	QC = VCO ÷ 4	QC = VCO ÷ 8
FSELD	0	QD = VCO ÷ 4	QD = VCO ÷ 8

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	4.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–55	150	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} ÷ 2		V	
MM	ESD (Machine Model)	200			V	
HBM	ESD (Human Body Model)	2000			V	
LU	Latch-Up	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage				0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK, $\overline{PCLK}$	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA[2]
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance			14 –17		Ω	
I_{IN}	Input Leakage Current				±200	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current			3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current				1.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9351 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

Table 6. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	÷ 2 feedback	100		200	MHz	PLL_EN = 1
		÷ 4 feedback	50		100	MHz	PLL_EN = 1
		÷ 8 feedback	25		50	MHz	PLL_EN = 1
		Static test mode	0		300	MHz	PLL_EN = 0
f_{VCO}	VCO Frequency		200		400	MHz	
f_{MAX}	Maximum Output Frequency	÷ 2 output	100		200	MHz	
		÷ 4 output	50		100	MHz	
		÷ 8 output	25		50	MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	500		1000	mV	LVPECL
V_{CMR}[2]	Common Mode Range	PCLK, $\overline{PCLK}$	1.2		V_{CC} – 0.9	V	LVPECL
t_r, t_f	TCLK Input Rise/Fall Time				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)						
		TCLK to EXT_FB	–50		+150	ps	PLL locked
		PCLK to EXT_FB	+25		+325	ps	PLL locked
$t_{sk(o)}$	Output-to-Output Skew				150	ps	
DC	Output Duty Cycle	100 – 200 MHz	45	50	55	%	
		50 – 100 MHz	47.5	50	52.5	%	
		25 – 50 MHz	48.75	50	51.75	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, ZH}$	Output Enable Time				10	ns	
BW	PLL closed loop bandwidth	÷ 2 feedback		9.0 –– 20.0		MHz	–3 db point of
		÷ 4 feedback		3.0 – 9.5		MHz	PLL transfer characteristic
		÷ 8 feedback		1.2 – 2.1		MHz	
$t_{JIT(CC)}$	Cycle-to-cycle jitter Single Output Frequency Configuration	÷ 4 feedback		10	22	ps	RMS value
$t_{JIT(PER)}$	Period Jitter Single Output Frequency Configuration	÷ 4 feedback		8.0	15	ps	RMS value
$t_{JIT(\varnothing)}$	I/O Phase Jitter			4.0 – 17		ps	RMS value
t_{LOCK}	Maximum PLL Lock Time				1.0	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}
2. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.

Table 7. DC Characteristics (V_{CC} = 2.5V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage				0.7	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK, $\overline{PCLK}$	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage		1.8			V	I_{OH} = –15 mA[2]
V_{OL}	Output Low Voltage				0.6	V	I_{OL} = 15 mA
Z_{OUT}	Output Impedance			17 – 20		Ω	
I_{IN}	Input Leakage Current				±200	μA	V_{IN} = V_{CC} or GND
C_{IN}	Input Capacitance			4.0		pF	
C_{PD}	Power Dissipation Capacitance			10		pF	Per Output
I_{CCA}	Maximum PLL Supply Current			3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current				1.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9351 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.

Table 8. AC Characteristics (V_{CC} = 2.5V ± 5%, T_A = -40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	÷ 2 feedback	100		200	MHz	
		÷ 4 feedback	50		100	MHz	
		÷ 8 feedback	25		50	MHz	
f_{VCO}	VCO Frequency		200		400	MHz	
f_{MAX}	Maximum Output Frequency	÷ 2 output	100		200	MHz	
		÷ 4 output	50		100	MHz	
		÷ 8 output	25		50	MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	500		1000	mV	LVPECL
V_{CMR}[2]	Common Mode Range	PCLK, $\overline{PCLK}$	1.2		V_{CC} – 0.6	V	LVPECL
t_r, t_f	TCLK Input Rise/Fall Time				1.0	ns	0.7 to 1.7V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)						
		TCLK to EXT_FB	–100		+100	ps	PLL locked
		PCLK to EXT_FB	0		+300	ps	PLL locked
$t_{sk(o)}$	Output-to-Output Skew				150	ps	
DC	Output Duty Cycle	100 – 200 MHz	45	50	55	%	
		50 – 100 MHz	47.5	50	52.5	%	
		25 – 50 MHz	48.75	50	51.75	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8V
$t_{PLZ, HZ}$	Output Disable Time				12	ns	
$t_{PZL, ZH}$	Output Enable Time				12	ns	
BW	PLL closed loop bandwidth	÷ 2 feedback		4.0 – 15.0		MHz	–3dB point of PLL transfer
		÷ 4 feedback		2.0 – 7.0		MHz	characteristic
		÷ 8 feedback		0.7 – 2.0		MHz	
$t_{JIT(CC)}$	Cycle-to-cycle jitter Single Output Frequency Configuration	÷ 4 feedback		10	22	ps	RMS value
$t_{JIT(PER)}$	Period Jitter Single Output Frequency Configuration	÷ 4 feedback		8.0	15	ps	RMS value
$t_{JIT(\varnothing)}$	I/O Phase Jitter			6.0 – 25		ps	RMS value
t_{LOCK}	Maximum PLL Lock Time				1.0	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}
2. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.

APPLICATIONS INFORMATION

Programming the MPC9351

The MPC9351 clock driver outputs can be configured into several divider modes, in addition the external feedback of the device allows for flexibility in establishing various input to output frequency relationships. The output divider of the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensures that the output duty cycle is always 50%. Table 9 illustrates the various output configurations, the table describes the outputs using the input clock frequency CLK as a reference.

The output division settings establish the output relationship, in addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 25 MHz to 200 MHz while the VCO frequency range is specified from 200 MHz to 400 MHz and should not be exceeded for stable operation.

Table 9. Output Frequency Relationship[1] for an Example Configuration

Inputs				Outputs			
FSELA	FSELB	FSELC	FSELD	QA	QB	QC	QD
0	0	0	0	2 * CLK	CLK	CLK	CLK
0	0	0	1	2 * CLK	CLK	CLK	CLK ÷ 2
0	0	1	0	4 * CLK	2 * CLK	CLK	2* CLK
0	0	1	1	4 * CLK	2 * CLK	CLK	CLK
0	1	0	0	2 * CLK	CLK ÷ 2	CLK	CLK
0	1	0	1	2 * CLK	CLK ÷ 2	CLK	CLK ÷ 2
0	1	1	0	4 * CLK	CLK	CLK	2 * CLK
0	1	1	1	4 * CLK	CLK	CLK	CLK
1	0	0	0	CLK	CLK	CLK	CLK
1	0	0	1	CLK	CLK	CLK	CLK ÷ 2
1	0	1	0	2 * CLK	2 * CLK	CLK	2 * CLK
1	0	1	1	2 * CLK	2 * CLK	CLK	CLK
1	1	0	0	CLK	CLK ÷ 2	CLK	CLK
1	1	0	1	CLK	CLK ÷ 2	CLK	CLK ÷ 2
1	1	1	0	2 * CLK	CLK	CLK	2 * CLK
1	1	1	1	2 * CLK	CLK	CLK	CLK

1. Output frequency relationship with respect to input reference frequency CLK. QC1 is connected to EXT_FB. More frequency ratios are available by the connection of QA to the feedback input (EXT_FB).

Using the MPC9351 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9351. For these applications the MPC9351 offers a differential LVPECL clock input pair as a PLL reference. This allows for the use of differential LVPECL primary clock distribution devices such as the Motorola MC100EP111 or MC10EP222, taking advantage of its superior low-skew performance. Clock trees using LVPECL for clock distribution and the MPC9351 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers.

The external feedback option of the MPC9351 PLL allows for its use as a zero-delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC9351 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$ relative to the feedback output.

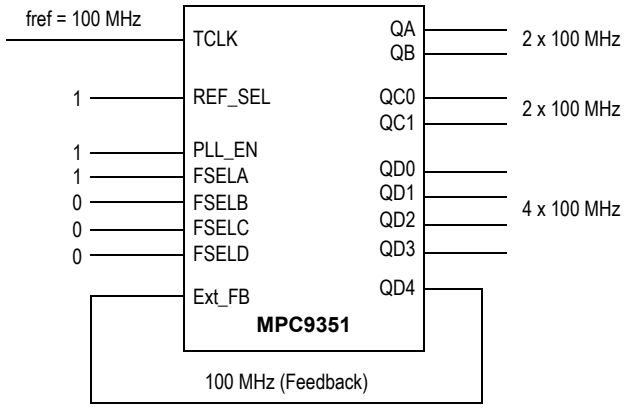


Figure 3. MPC9351 Zero-Delay Configuration (Feedback of QD4)

Calculation of Part-to-Part Skew

The MPC9351 zero-delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (TCLK or PCLK) of two or more MPC9351 are connected together, the maximum overall timing uncertainty from the common TCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

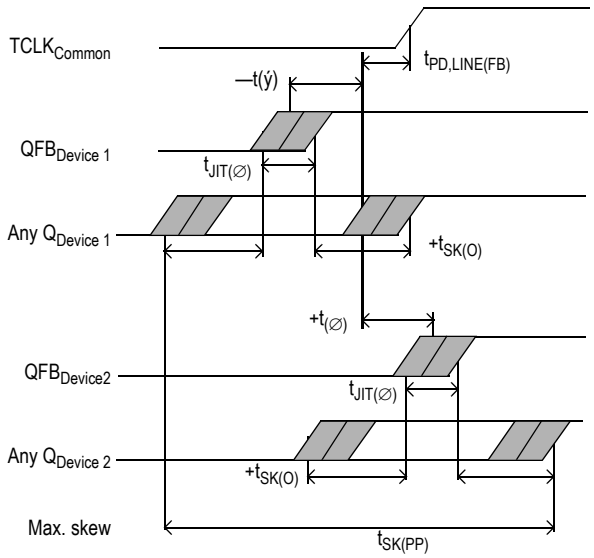


Figure 4. MPC9351 Maximum Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

Table 10. Confidence Factor CF

CF	Probability of Clock Edge within the Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation, an I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –251 ps to 351 ps relative to TCLK (V_{CC} = 3.3 V and f_{VCO} = 400 MHz):

$$t_{SK(PP)} = [–50\ ps...150\ ps] + [–150\ ps...150\ ps] + [(17ps \cdot –3)...(17ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–251\ ps...351\ ps] + t_{PD,\ LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for V_{CC} = 3.3 V (17 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (200 MHz for the MPC9351). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 5 and Figure 6 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew ($t_{SK(PP)}$).

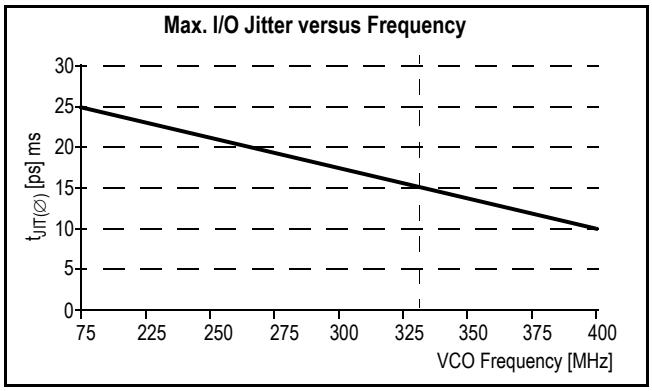


Figure 5. Maximum I/O Jitter (RMS) versus frequency for V_{CC}=2.5 V

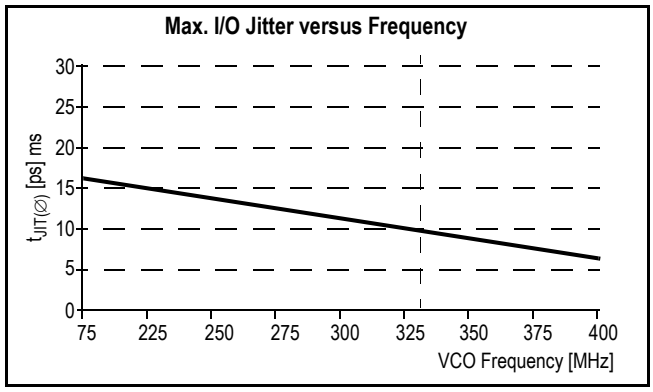


Figure 6. Maximum I/O Jitter (RMS) versus frequency for V_{CC}=3.3 V

Power Supply Filtering

The MPC9351 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9351 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment, where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9351. Figure 7. V_{CCA} Power Supply Filter illustrates a typical power supply filter

scheme. The MPC9351 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor (R_F). From the data sheet, the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325 V (V_{CC} = 3.3 V or V_{CC} = 2.5 V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 7 must have a resistance of 270 Ω (V_{CC} = 3.3 V) or 9–10 Ω (V_{CC} = 2.5 V) to meet the voltage drop criteria.

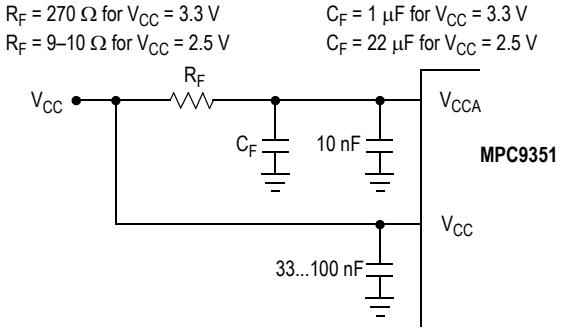


Figure 7. V_{CCA} Power Supply Filter

The minimum values for R_F and the and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7, the filter cut-off frequency is around 3–5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9351 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9351 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9351 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 8 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9351 clock driver is effectively doubled due to its capability to drive multiple lines.

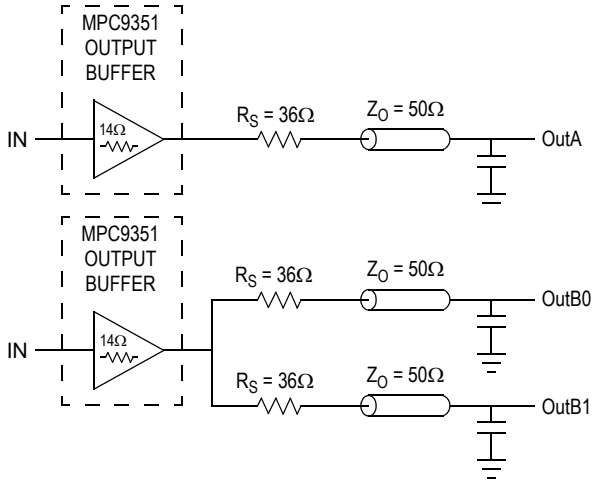


Figure 8. Single versus Dual Transmission Lines

The waveform plots in Figure 9. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9351 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9351. The output waveform in Figure 9 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18 + 17 + 25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

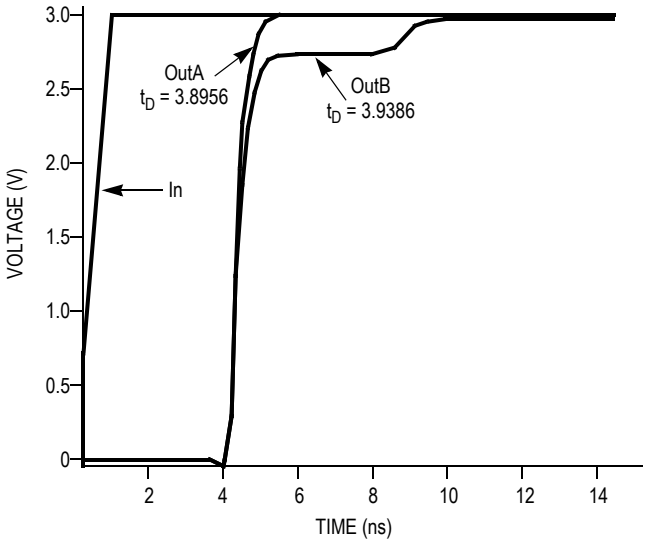
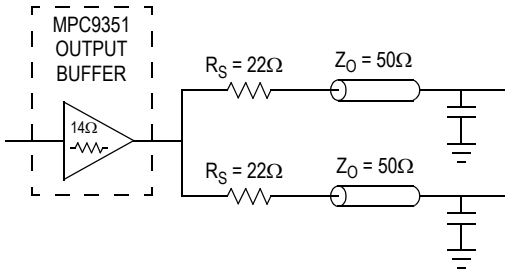


Figure 9. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 10 should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



14Ω + 22Ω || 22Ω = 50Ω || 50Ω
25Ω = 25Ω

Figure 10. Optimized Dual Line Termination

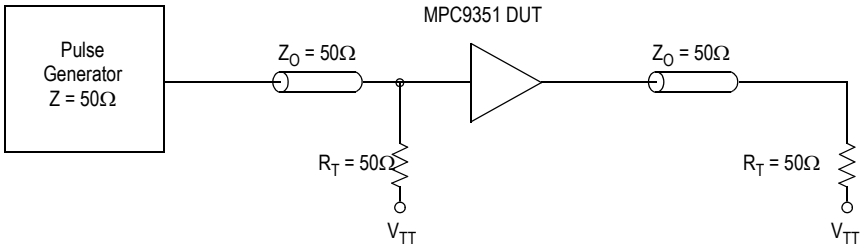


Figure 11. TCLK MPC9351 AC Test Reference for V_{cc} = 3.3 V and V_{cc} = 2.5 V

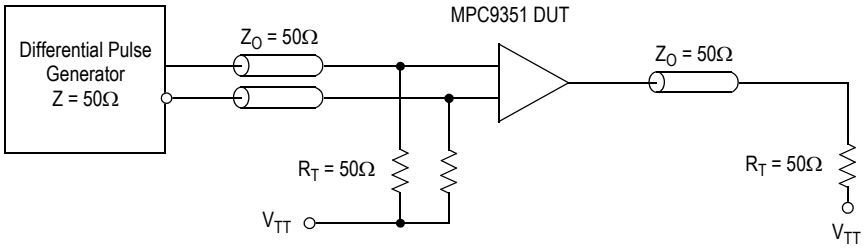


Figure 12. PCLK MPC9351 AC Test Reference

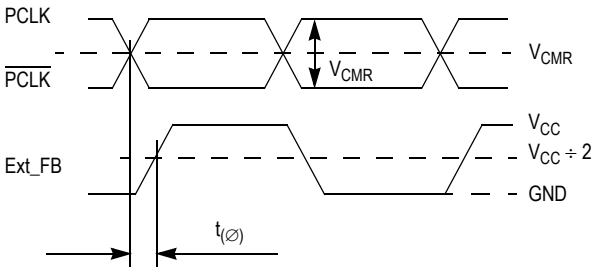


Figure 13. Propagation Delay (t_{PD}, static phase offset) Test Reference

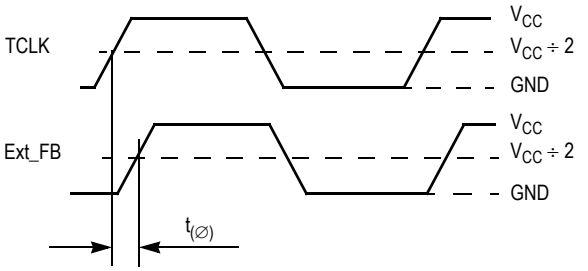
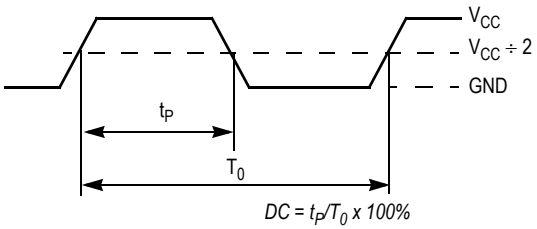
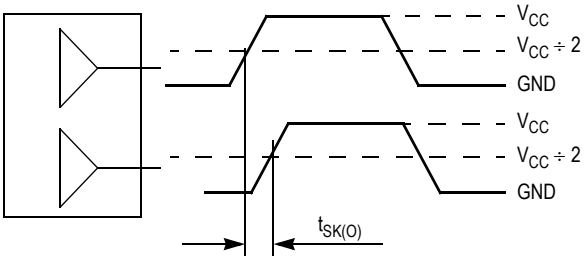


Figure 14. Propagation Delay (t_{PD}) Test Reference



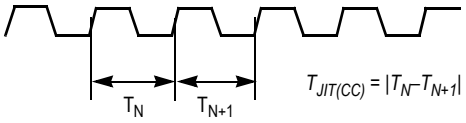
The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 15. Output Duty Cycle (DC)



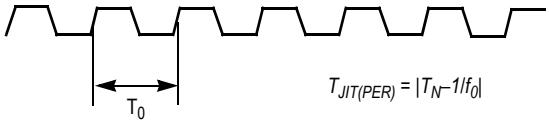
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 16. Output-to-Output Skew $t_{SK(O)}$



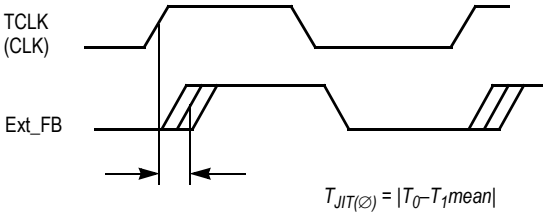
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 17. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 18. Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 19. I/O Jitter

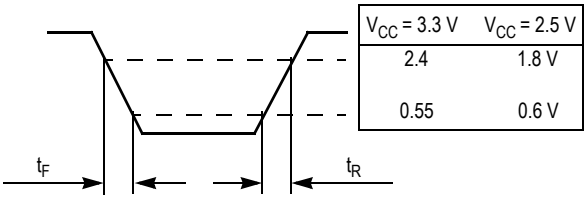


Figure 20. Transition Time Test Reference

Order number: MPC93H51
Rev 3, 08/2004

Low Voltage PLL Clock Drive

MPC93H51

**LOW VOLTAGE 3.3 V
PLL CLOCK GENERATOR**

FA SUFFIX
LQFP PACKAGE
CASE 873A-03

The MPC93H51 is a 3.3V compatible, PLL based clock generator targeted for high performance clock distribution systems. With output frequencies of up to 240 MHz and a maximum output skew of 150 ps the MPC93H51 is an ideal solution for the most demanding clock tree designs. The device offers 9 low skew clock outputs, each is configurable to support the clocking needs of the various high-performance microprocessors including the PowerQuicc II integrated communication microprocessor. The devices employs a fully differential PLL design to minimize cycle-to-cycle and long-term jitter.

Features

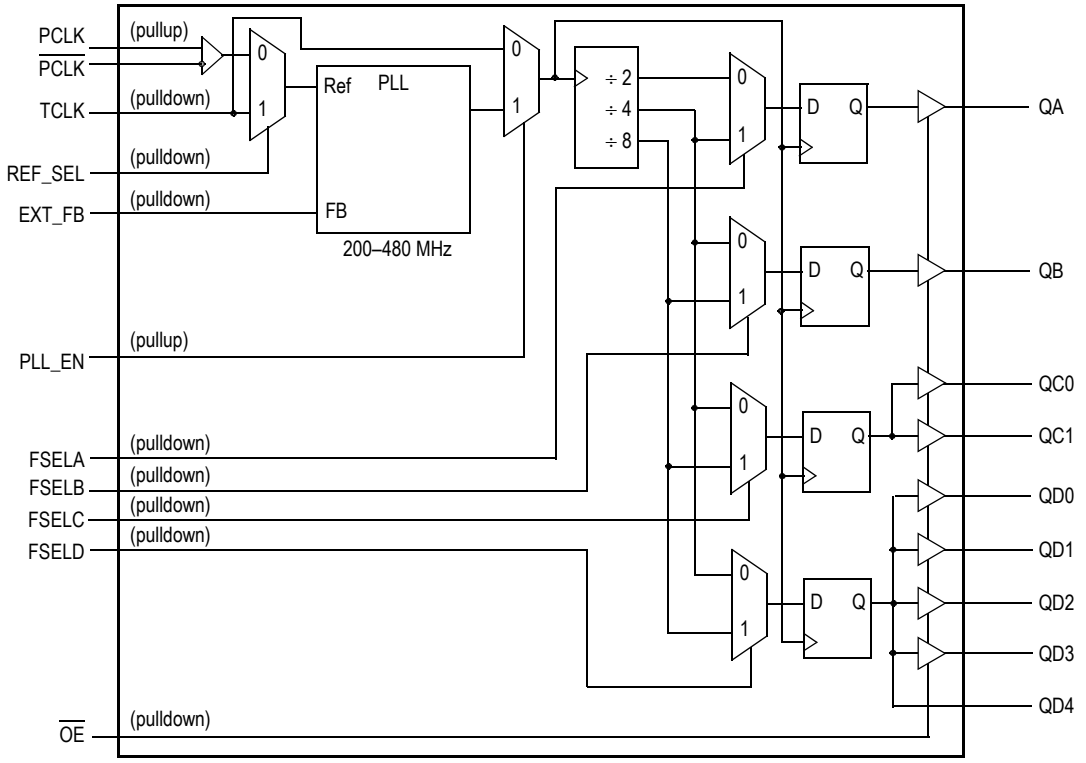
- 9 outputs LVCMOS PLL clock generator
- 25 – 240 MHz output frequency range
- Fully integrated PLL
- Compatible to various microprocessors such as PowerQuicc II
- Supports networking, telecommunications and computer applications
- Configurable outputs: divide-by-2, 4 and 8 of VCO frequency
- LVPECL and LVCMOS compatible inputs
- External feedback enables zero-delay configurations
- Output enable/disable and static test mode (PLL enable/disable)
- Low skew characteristics: maximum 150 ps output-to-output
- 32-lead LQFP package
- 32-lead Pb-free Package Available
- Ambient Temperature Range 0°C to +70°C
- Pin & Function Compatible with the MPC951

Functional Description

The MPC93H51 utilizes PLL technology to frequency and phase lock its outputs onto an input reference clock. Normal operation of the MPC93H51 requires a connection of one of the device outputs to the EXT_FB input to close the PLL feedback path. The reference clock frequency and the output divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. With available output dividers of divide-by-4 and divide-by-8 the internal VCO of the MPC93H51 is running at either 4x or 8x of the reference clock frequency. The frequency of the QA, QB, QC and QD outputs is either the one half, one fourth or one eighth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB, FSELC and FSELD pins, respectively. The available output to input frequency ratios are 4:1, 2:1, 1:1, 1:2 and 1:4. The REF_SEL pin selects the differential LVPECL (PCLK and $\overline{\text{PCLK}}$) or the LVCMOS compatible reference input (TCLK). The MPC93H51 also provides a static test mode when the PLL enable pin (PLL_EN) is pulled to logic low state. In test mode, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The test mode is intended for system diagnostics, test and debug purpose. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the $\overline{\text{OE}}$ pin (logic high state). In PLL mode, deasserting $\overline{\text{OE}}$ causes the PLL to loose lock due to no feedback signal presence at EXT_FB. Asserting OE will enable the outputs and close the phase locked loop, also enabling the PLL to recover to normal operation. The MPC93H51 is 3.3V compatible and requires no external loop filter components. All inputs except PCLK and $\overline{\text{PCLK}}$ accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC93H51 outputs can drive one or two traces giving the devices an effective fanout of 1:18. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

Application Information

The fully integrated PLL of the MPC93H51 allows the low skew outputs to lock onto a clock input and distribute it with essentially zero propagation delay to multiple components on the board. In zero-delay buffer mode, the PLL minimizes phase offset between the outputs and the reference signal.



The MPC93H51 requires an external RC filter for the analog power supply pin V_{CCA}. Please see APPLICATIONS INFORMATION for details.

Figure 1. MPC93H51 Logic Diagram

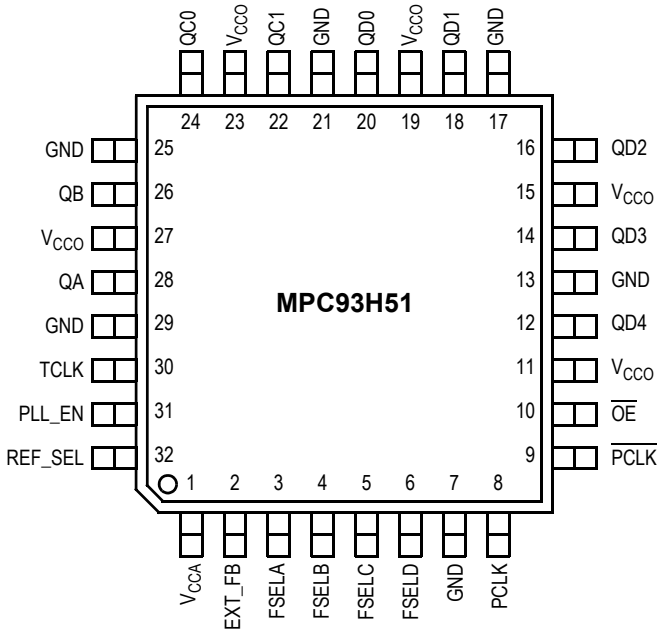


Figure 2. Pinout: 32-Lead LQFP Package Pinout (Top View)

Table 1. Pin Description

Pin	I/O	Type	Function
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	Differential clock reference Low voltage positive ECL input
TCLK	Input	LVCMOS	Single ended reference clock signal or test clock
EXT_FB	Input	LVCMOS	Feedback signal input, connect to a QA, QB, QC, QD output
REF_SEL	Input	LVCMOS	Selects input reference clock
FSELA	Input	LVCMOS	Output A divider selection
FSELB	Input	LVCMOS	Output B divider selection
FSELC	Input	LVCMOS	Outputs C divider selection
FSELD	Input	LVCMOS	Outputs D divider selection
OE	Input	LVCMOS	Output enable/disable
QA	Output	LVCMOS	Bank A clock output
QB	Output	LVCMOS	Bank B clock output
QC0, QC1	Output	LVCMOS	Bank C clock outputs
QD0 – QD4	Output	LVCMOS	Bank D clock outputs1.5
V_{CCA}	Supply	V_{CC}	Positive power supply for the PLL
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core
GND	Supply	Ground	Negative power supply

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	Selects PCLK as reference clock	Selects TCLK as reference clock
PLL_EN	1	Test mode with PLL disabled. The input clock is directly routed to the output dividers	PLL enabled. The VCO output is routed to the output dividers
OE	0	Outputs enabled	Outputs disabled, PLL loop is open VCO is forced to its minimum frequency
FSELA	0	QA = VCO ÷ 2	QA = VCO ÷ 4
FSELB	0	QB = VCO ÷ 4	QB = VCO ÷ 8
FSELC	0	QC = VCO ÷ 4	QC = VCO ÷ 8
FSELD	0	QD = VCO ÷ 4	QD = VCO ÷ 8

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	150	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD (Machine Model)	200			V	
HBM	ESD (Human Body Model)	2000			V	
LU	Latch-Up	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0° to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range PCLK, $\overline{PCLK}$	1.0		V_{CC}-0.6	V	LVPECL
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA[2]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance		7 – 10		Ω	
I_{IN}	Input Leakage Current			±150	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current		6.0	12.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current		10.0	14.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC93H51 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0° to 70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency[2]	÷ 4 feedback ÷ 8 feedback Static test mode	50 25 0		120 60 300	MHz MHz MHz	PLL_EN = 1 PLL_EN = 1 PLL_EN = 0
f_{VCO}	VCO Frequency		200		480	MHz	
f_{MAX}	Maximum Output Frequency[2]	÷ 2 output ÷ 4 output ÷ 8 output	100 50 25		240 120 60	MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	500		1000	mV	LVPECL
V_{CMR}[3]	Common Mode Range	PCLK, $\overline{PCLK}$	1.2		V_{CC}-0.9	V	LVPECL
t_r, t_f[4]	TCLK Input Rise/Fall Time				1.0	ns	0.8 to 2.0 V
$t_{(\varnothing)}$	Propagation Delay (static phase offset) TCLK to EXT_FB PCLK to EXT_FB		 –150 0		 +150 +250	 ps ps	 PLL locked PLL locked
$t_{sk(o)}$	Output-to-Output Skew				300	ps	
DC	Output Duty Cycle	100 – 240 MHz 50 – 120 MHz 25 – 60 MHz	45 47.5 48.75	50 50 50	55 52.5 51.75	% % %	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time				7.0	ns	
$t_{PZL, ZH}$	Output Enable Time				6.0	ns	
BW	PLL closed loop bandwidth	÷ 2 feedback ÷ 4 feedback ÷ 8 feedback		9.0 – 20.0 3.0 – 9.5 1.2 – 2.1		MHz MHz	-3 db point of PLL transfer characteristic
$t_{JIT(CC)}$	Cycle-to-cycle jitter Single Output Frequency Configuration	÷ 4 feedback			40	ps	RMS value
$t_{JIT(PER)}$	Period Jitter Single Output Frequency Configuration	÷ 4 feedback			25	ps	RMS value
$t_{JIT(\varnothing)}$	I/O Phase Jitter				30	ps	RMS value
t_{LOCK}	Maximum PLL Lock Time				5	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}
2. The PLL will be unstable with a divide by 2 feedback ratio.
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
4. The MPC93H51 will operate with input rise/fall times up to 3.0 ns, but the AC characteristics, specifically $t_{(\varnothing)}$, can only be guaranteed if t_r/t_f are within the specified range.

APPLICATIONS INFORMATION

Programming the MPC93H51

The MPC93H51 clock driver outputs can be configured into several divider modes, in addition the external feedback of the device allows for flexibility in establishing various input to output frequency relationships. The output divider of the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. Table 7 illustrates the various output configurations, the table describes the outputs using the input clock frequency CLK as a reference.

The output division settings establish the output relationship, in addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 25 MHz to 240 MHz while the VCO frequency range is specified from 200 MHz to 480 MHz and should not be exceeded for stable operation.

Table 7. Output Frequency Relationship[1] for an Example Configuration

Inputs				Outputs			
FSELA	FSELB	FSELC	FSELD	QA	QB	QC	QD
0	0	0	0	2 * CLK	CLK	CLK	CLK
0	0	0	1	2 * CLK	CLK	CLK	CLK ÷ 2
0	0	1	0	4 * CLK	2 * CLK	CLK	2* CLK
0	0	1	1	4 * CLK	2 * CLK	CLK	CLK
0	1	0	0	2 * CLK	CLK ÷ 2	CLK	CLK
0	1	0	1	2 * CLK	CLK ÷ 2	CLK	CLK ÷ 2
0	1	1	0	4 * CLK	CLK	CLK	2 * CLK
0	1	1	1	4 * CLK	CLK	CLK	CLK
1	0	0	0	CLK	CLK	CLK	CLK
1	0	0	1	CLK	CLK	CLK	CLK ÷ 2
1	0	1	0	2 * CLK	2 * CLK	CLK	2 * CLK
1	0	1	1	2 * CLK	2 * CLK	CLK	CLK
1	1	0	0	CLK	CLK ÷ 2	CLK	CLK
1	1	0	1	CLK	CLK ÷ 2	CLK	CLK ÷ 2
1	1	1	0	2 * CLK	CLK	CLK	2 * CLK
1	1	1	1	2 * CLK	CLK	CLK	CLK

1. Output frequency relationship with respect to input reference frequency CLK. QC1 is connected to EXT_FB.

Using the MPC93H51 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC93H51. For these applications the MPC93H51 offers a differential LVPECL clock input pair as a PLL reference. This allows for the use of differential LVPECL primary clock distribution devices such as the Motorola MC100EP111 or MC10EP222, taking advantage of its superior low-skew performance. Clock trees using LVPECL for clock distribution and the MPC93H51 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers.

The external feedback option of the MPC93H51 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC93H51 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$ relative to the feedback output.

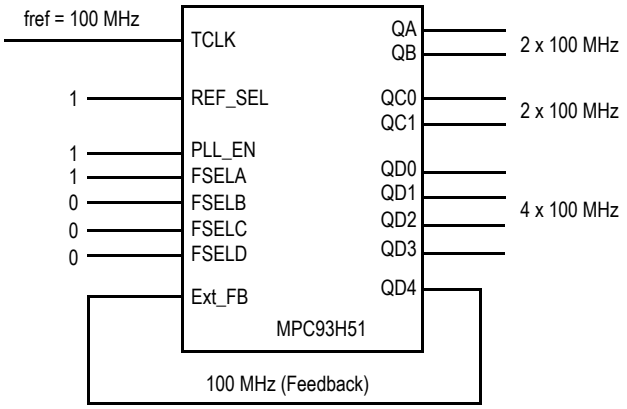


Figure 3. MPC93H51 Zero-Delay Configuration (Feedback of QD4)

Calculation of Part-to-Part Skew

The MPC93H51 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (TCLK or PCLK) of two or more MPC93H51 are connected together, the maximum overall timing uncertainty from the common TCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \bullet CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

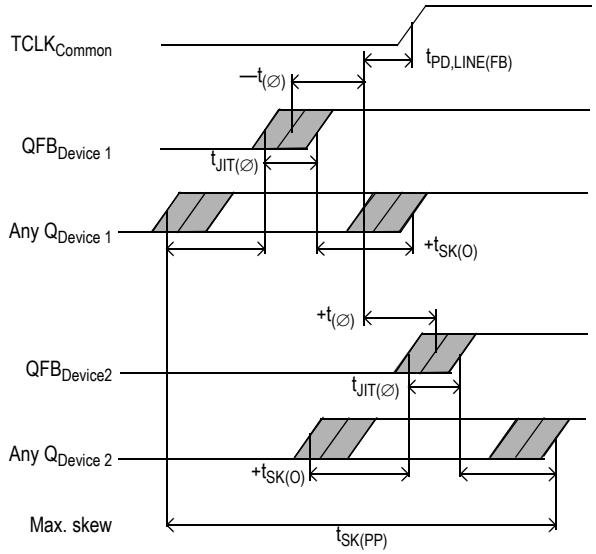


Figure 4. MPC93H51 Maximum Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8. Confidence Factor CF

CF	Probability of Clock Edge within the Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –251 ps to 351 ps relative to TCLK (V_{CC} = 3.3 V and f_{VCO} = 400 MHz):

$t_{SK(PP)}$ = *[–50ps...150ps] + [–150ps...150ps] + [(17ps @ –3)...(17ps @ 3)] +* $t_{PD,\ LINE(FB)}$

$t_{SK(PP)}$ = *[–251ps...351ps]* + $t_{PD,\ LINE(FB)}$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for V_{CC} = 3.3 V (17 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (200 MHz for the MPC93H51). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 5 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

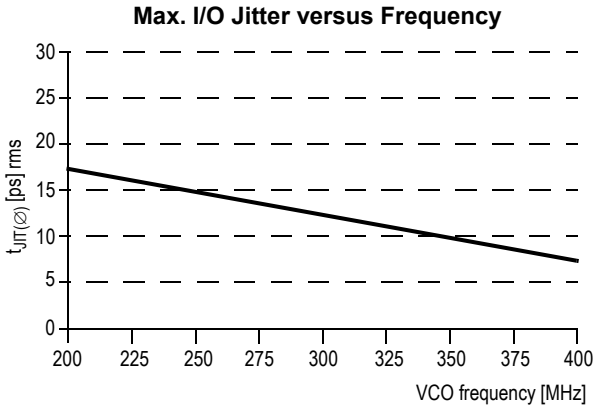


Figure 5. Maximum I/O Jitter (RSM) versus Frequency for V_{CC} = 3.3 V

Power Supply Filtering

The MPC93H51 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC93H51 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC93H51.

Figure 6. V_{CCA} Power Supply Filter illustrates a typical power supply filter scheme. The MPC93H51 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 6 mA (12 mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 6 must have a resistance of 5–15 Ω to meet the voltage drop criteria.

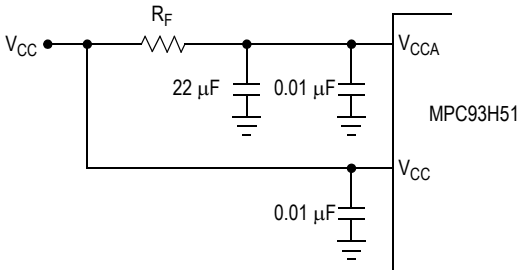


Figure 6. V_{CCA} Power Supply Filter

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC93H51 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC93H51 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC93H51 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 7 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC93H51 clock driver is effectively doubled due to its capability to drive multiple lines.

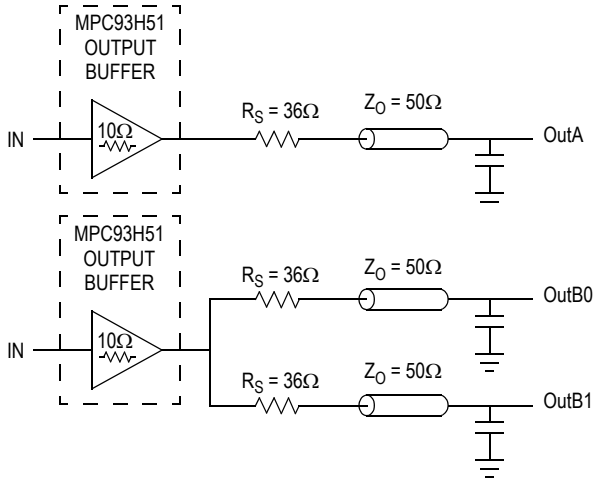


Figure 7. Single versus Dual Transmission Lines

The waveform plots in Figure 8. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC93H51 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC93H51. The output waveform in Figure 8 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18 + 17 + 25)$$
$$= 1.31\ V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 9. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

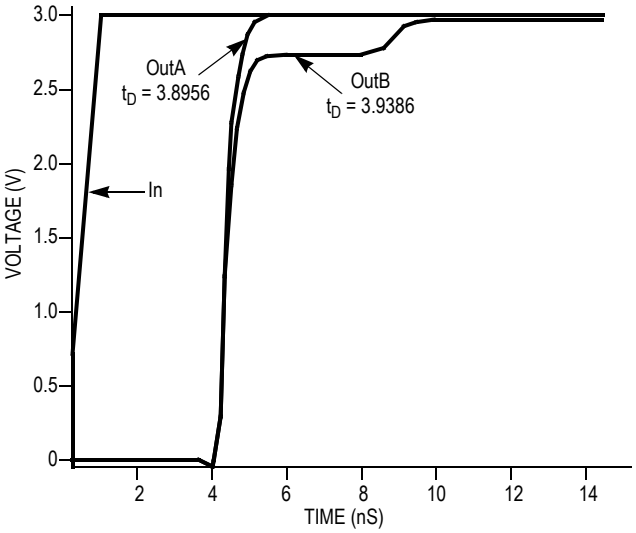
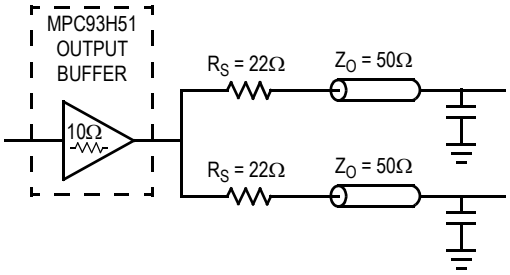


Figure 8. Single versus Dual Waveforms



14 Ω + 22 Ω || 22 Ω = 50 Ω || 50 Ω
25 Ω = 25 Ω

Figure 9. Optimized Dual Line Termination

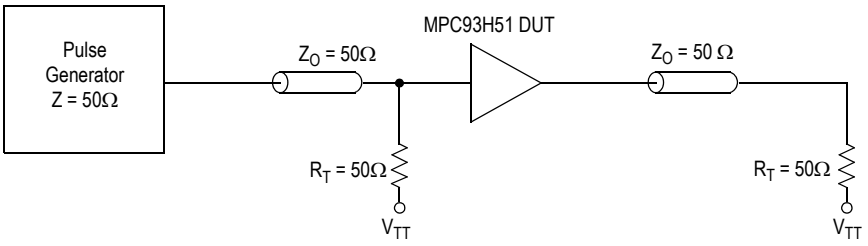


Figure 10. TCLK MPC93H51 AC Test Reference for V_{CC} = 3. 3V

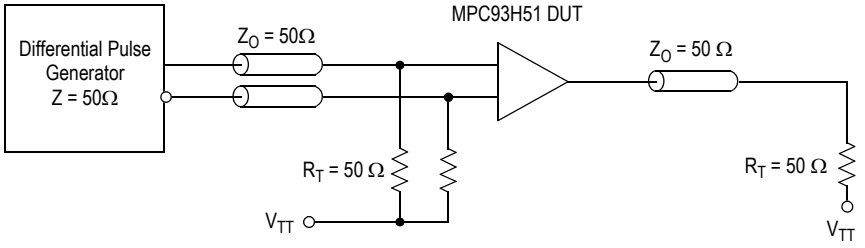


Figure 11. PCLK MPC93H51 AC Test Reference

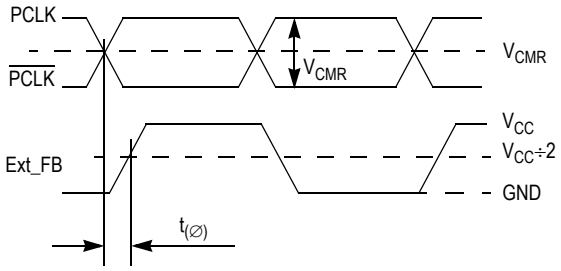


Figure 12. Propagation Delay (t_{PD}, status phase offset) Test Reference

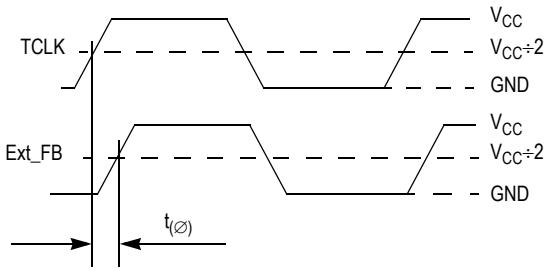
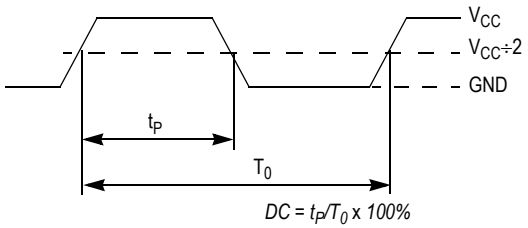
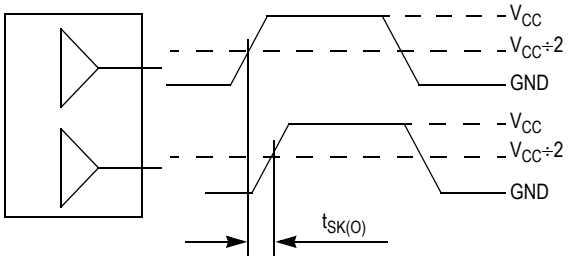


Figure 13. Propagation Delay (t_{PD}) Test Reference



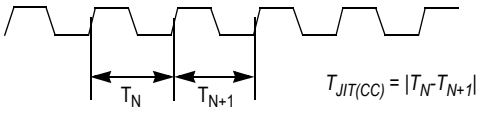
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 14. Output Duty Cycle (DC)



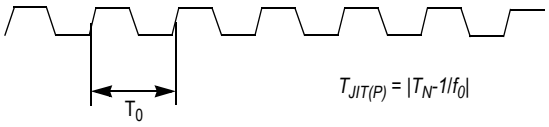
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 15. Output-to-Output Skew $t_{SK(O)}$



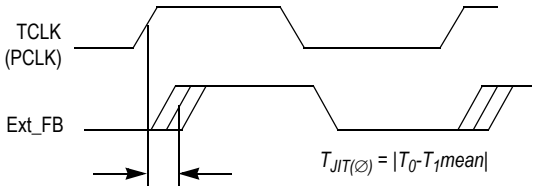
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 16. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 17. Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 18. I/O Jitter

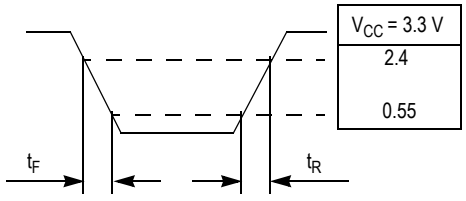


Figure 19. Transition Time Test Reference

Low Voltage PLL Clock Driver

MPC93R51

LOW VOLTAGE 3.3V PLL CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC93R51 is a 3.3V compatible, PLL based clock generator targeted for high performance clock distribution systems. With output frequencies of up to 240 MHz and a maximum output skew of 150 ps the MPC93R51 is an ideal solution for the most demanding clock tree designs. The device offers 9 low skew clock outputs, each is configurable to support the clocking needs of the various high-performance microprocessors including the PowerQuicc II integrated communication microprocessor. The devices employs a fully differential PLL design to minimize cycle-to-cycle and long-term jitter.

Features

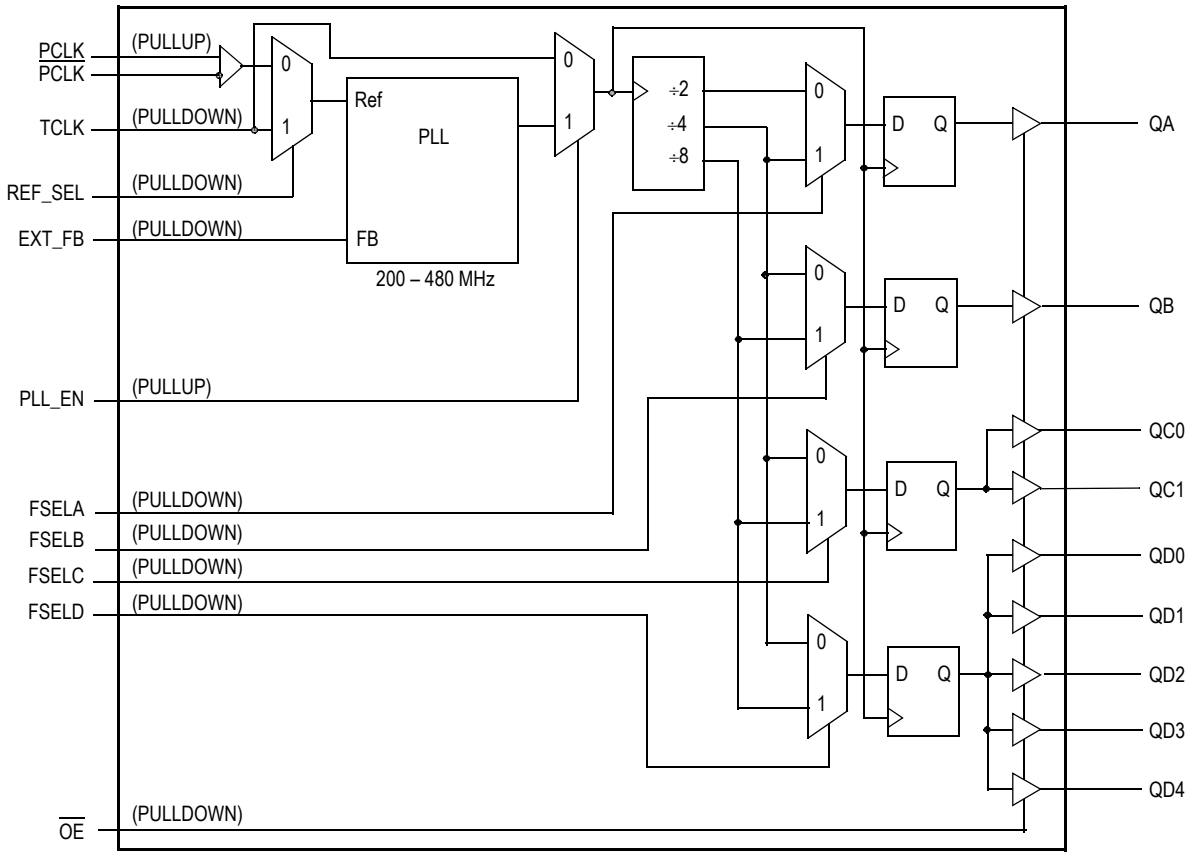
- 9 outputs LVCMOS PLL clock generator
- 25 - 240 MHz output frequency range
- Fully integrated PLL
- Compatible to various microprocessors such as PowerQuicc II
- Supports networking, telecommunications and computer applications
- Configurable outputs: divide-by-2, 4 and 8 of VCO frequency
- LVPECL and LVCMOS compatible inputs
- External feedback enables zero-delay configurations
- Output enable/disable and static test mode (PLL enable/disable)
- Low skew characteristics: maximum 150 ps output-to-output
- Cycle-to-cycle jitter max. 22 ps RMS
- 32-lead LQFP package
- 32-lead Pb-free Package Available
- Ambient Temperature Range 0°C to +70°C
- Pin & Function Compatible with the MPC951

Functional Description

The MPC93R51 utilizes PLL technology to frequency and phase lock its outputs onto an input reference clock. Normal operation of the MPC93R51 requires a connection of one of the device outputs to the EXT_FB input to close the PLL feedback path. The reference clock frequency and the output divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. With available output dividers of divide-by-4 and divide-by-8 the internal VCO of the MPC93R51 is running at either 4x or 8x of the reference clock frequency. The frequency of the QA, QB, QC and QD outputs is either the one half, one fourth or one eighth of the selected VCO frequency and can be configured for each output bank using the FSELA, FSELB, FSELC and FSELD pins, respectively. The available output to input frequency ratios are 4:1, 2:1, 1:1, 1:2 and 1:4. The REF_SEL pin selects the differential LVPECL (PCLK and $\overline{\text{PCLK}}$) or the LVCMOS compatible reference input (TCLK). The MPC93R51 also provides a static test mode when the PLL enable pin (PLL_EN) is pulled to logic low state. In test mode, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The test mode is intended for system diagnostics, test and debug purpose. This test mode is fully static and the minimum clock frequency specification does not apply. The outputs can be disabled by deasserting the $\overline{\text{OE}}$ pin (logic high state). In PLL mode, deasserting $\overline{\text{OE}}$ causes the PLL to loose lock due to no feedback signal presence at EXT_FB. Asserting $\overline{\text{OE}}$ will enable the outputs and close the phase locked loop, also enabling the PLL to recover to normal operation. The MPC93R51 is 3.3V compatible and requires no external loop filter components. All inputs except PCLK and $\overline{\text{PCLK}}$ accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC93R51 outputs can drive one or two traces giving the devices an effective fanout of 1:18. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

Application Information

The fully integrated PLL of the MPC93R51 allows the low skew outputs to lock onto a clock input and distribute it with essentially zero propagation delay to multiple components on the board. In zero-delay buffer mode, the PLL minimizes phase offset between the outputs and the reference signal.



The MPC93R51 requires an external RC filter for the analog power supply pin V_{CCA}. Please see application section for details.

Figure 1. MPC93R51 Logic Diagram

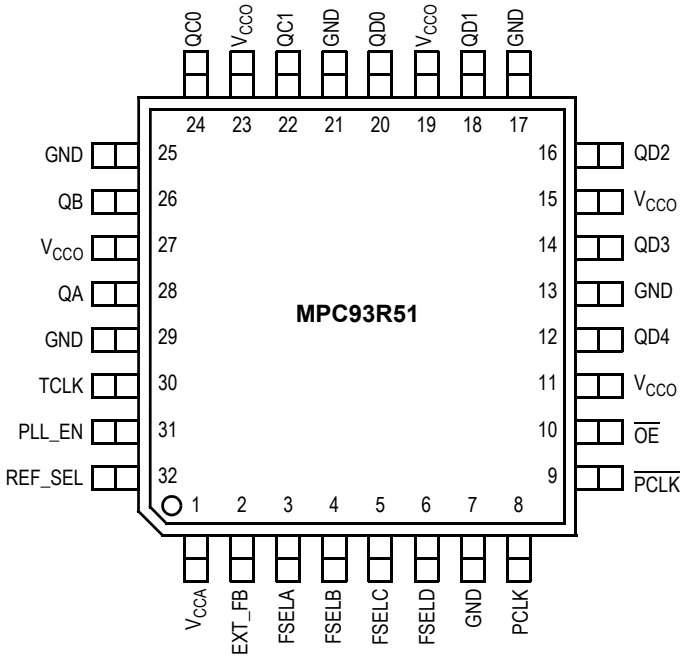


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1. Pin Description

Number	Name	Type	Description
PCLK, $\overline{PCLK}$	Input	LVPECL	Differential clock reference Low voltage positive ECL input
TCLK	Input	LVCMOS	Single ended reference clock signal or test clock
EXT_FB	Input	LVCMOS	Feedback signal input, connect to a QA, QB, QC, QD output
REF_SEL	Input	LVCMOS	Selects input reference clock
FSELA	Input	LVCMOS	Output A divider selection
FSELB	Input	LVCMOS	Output B divider selection
FSELC	Input	LVCMOS	Outputs C divider selection
FSELD	Input	LVCMOS	Outputs D divider selection
$\overline{OE}$	Input	LVCMOS	Output enable/disable
QA	Output	LVCMOS	Bank A clock output
QB	Output	LVCMOS	Bank B clock output
QC0, QC1	Output	LVCMOS	Bank C clock outputs
QD0 – QD4	Output	LVCMOS	Bank D clock outputs
V_{CCA}	Supply	V_{CC}	Positive power supply for the PLL
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core
GND	Supply	Ground	Negative power supply

Table 2. Function Table

Control	Default	0	1
REF_SEL	0	Selects PCLK as reference clock	Selects TCLK as reference clock
PLL_EN	1	Test mode with PLL disabled. The input clock is directly routed to the output dividers	PLL enabled. The VCO output is routed to the output dividers
$\overline{OE}$	0	Outputs enabled	Outputs disabled, PLL loop is open VCO is forced to its minimum frequency
FSELA	0	QA = VCO ÷ 2	QA = VCO ÷ 4
FSELB	0	QB = VCO ÷ 4	QB = VCO ÷ 8
FSELC	0	QC = VCO ÷ 4	QC = VCO ÷ 8
FSELD	0	QD = VCO ÷ 4	QD = VCO ÷ 8

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	**Table 4Supply Voltage**	-0.3	4.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-55	150	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD (Machine Model)	200			V	
HBM	ESD (Human Body Model)	2000			V	
LU	Latch-Up	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}			4.0		pF	Inputs

Table 6. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0° to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range PCLK, $\overline{PCLK}$	1.0		V_{CC}–0.6	V	LVPECL
V_{OH}	Output High Voltage	2.4			V	I_{OH}=–24 mA[2]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24 mA I_{OL}= 12 mA
Z_{OUT}	Output Impedance		14 –17		Ω	
I_{IN}	Input Leakage Current			±150	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current		7.0	10	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC93R51 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

Table 7. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0° to 70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency[2]	÷ 4 feedback ÷ 8 feedback Static test mode	50 25 0		120 60 300	MHz MHz MHz	PLL_EN = 1 PLL_EN = 1 PLL_EN = 0
f_{VCO}	VCO Frequency		200		480	MHz	
f_{MAX}	Maximum Output Frequency[2]	÷ 2 output ÷ 4 output ÷ 8 output	100 50 25		240 120 60	MHz MHz MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	500		1000	mV	LVPECL
V_{CMR}[3]	Common Mode Range	PCLK, $\overline{PCLK}$	1.2		V_{CC}–0.9	V	LVPECL
t_r, t_f[4]	TCLK Input Rise/Fall Time				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset) TCLK to EXT_FB PCLK to EXT_FB		 -50 +25		 +150 +325	 ps ps	 PLL locked PLL locked
$t_{sk(o)}$	Output-to-Output Skew				150	ps	
DC	Output Duty Cycle	100 – 240 MHz 50 – 120 MHz 25 – 60 MHz	45 47.5 48.75	50 50 50	55 52.5 51.75	% % %	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				7.0	ns	
$t_{PZL, ZH}$	Output Enable Time				6.0	ns	
BW	PLL closed loop bandwidth	÷ 4 feedback ÷ 8 feedback		3.0 – 9.5 1.2 – 2.1		MHz MHz	–3 db point of PLL transfer characteristic
$t_{JIT(CC)}$	Cycle-to-cycle jitter Single Output Frequency Configuration	÷ 4 feedback		10	22	ps	RMS value
$t_{JIT(PER)}$	Period Jitter Single Output Frequency Configuration	÷ 4 feedback		8.0	15	ps	RMS value
$t_{JIT(\varnothing)}$	I/O Phase Jitter			4.0 – 17		ps	RMS value
t_{LOCK}	Maximum PLL Lock Time				1.0	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}
2. The PLL will be unstable with a divide by 2 feedback ratio
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
4. The MPC93R51 will operate with input rise/fall times up to 3.0 ns, but the AC characteristics, specifically $t_{(\varnothing)}$, can only be guaranteed if t_r/t_f are within the specified range.

APPLICATIONS INFORMATION

Programming the MPC93R51

The MPC93R51 clock driver outputs can be configured into several divider modes, in addition the external feedback of the device allows for flexibility in establishing various input to output frequency relationships. The output divider of the four output groups allows the user to configure the outputs into 1:1, 2:1, 4:1 and 4:2:1 frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. Table 8. Output Frequency Relationship for an Example Configuration illustrates the various output configurations, the table describes the outputs using the input clock frequency CLK as a reference.

The output division settings establish the output relationship, in addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 25 MHz to 240 MHz while the VCO frequency range is specified from 200 MHz to 480 MHz and should not be exceeded for stable operation.

Table 8. Output Frequency Relationship[1] for an Example Configuration

Inputs				Outputs			
FSELA	FSELB	FSELC	FSELD	QA	QB	QC	QD
0	0	0	0	2 * CLK	CLK	CLK	CLK
0	0	0	1	2 * CLK	CLK	CLK	CLK ÷ 2
0	0	1	0	4 * CLK	2 * CLK	CLK	2* CLK
0	0	1	1	4 * CLK	2 * CLK	CLK	CLK
0	1	0	0	2 * CLK	CLK ÷ 2	CLK	CLK
0	1	0	1	2 * CLK	CLK ÷ 2	CLK	CLK ÷ 2
0	1	1	0	4 * CLK	CLK	CLK	2 * CLK
0	1	1	1	4 * CLK	CLK	CLK	CLK
1	0	0	0	CLK	CLK	CLK	CLK
1	0	0	1	CLK	CLK	CLK	CLK ÷ 2
1	0	1	0	2 * CLK	2 * CLK	CLK	2 * CLK
1	0	1	1	2 * CLK	2 * CLK	CLK	CLK
1	1	0	0	CLK	CLK ÷ 2	CLK	CLK
1	1	0	1	CLK	CLK ÷ 2	CLK	CLK ÷ 2
1	1	1	0	2 * CLK	CLK	CLK	2 * CLK
1	1	1	1	2 * CLK	CLK	CLK	CLK

1. Output frequency relationship with respect to input reference frequency CLK. QC1 is connected to EXT_FB.

Using the MPC93R51 in zero-delay applications

Nested clock trees are typical applications for the MPC93R51. For these applications the MPC93R51 offers a differential LVPECL clock input pair as a PLL reference. This allows for the use of differential LVPECL primary clock distribution devices such as the Motorola MC100EP111 or MC10EP222, taking advantage of its superior low-skew performance. Clock trees using LVPECL for clock distribution and the MPC93R51 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers.

The external feedback option of the MPC93R51 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC93R51 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$ relative to the feedback output.

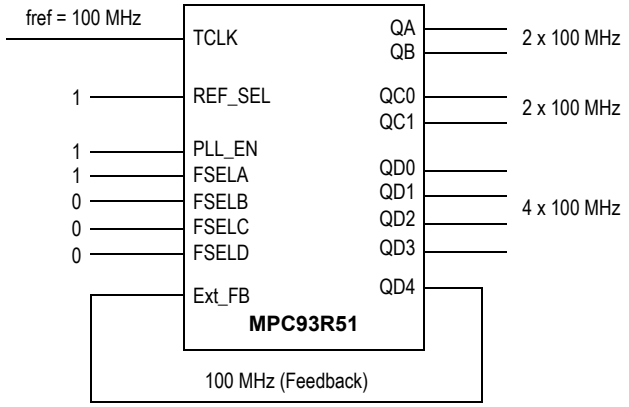


Figure 3. MPC93R51 Zero-Delay Configuration (Feedback of QD4)

Calculation of part-to-part skew

The MPC93R51 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (TCLK or PCLK) of two or more MPC93R51 are connected together, the maximum overall timing uncertainty from the common TCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

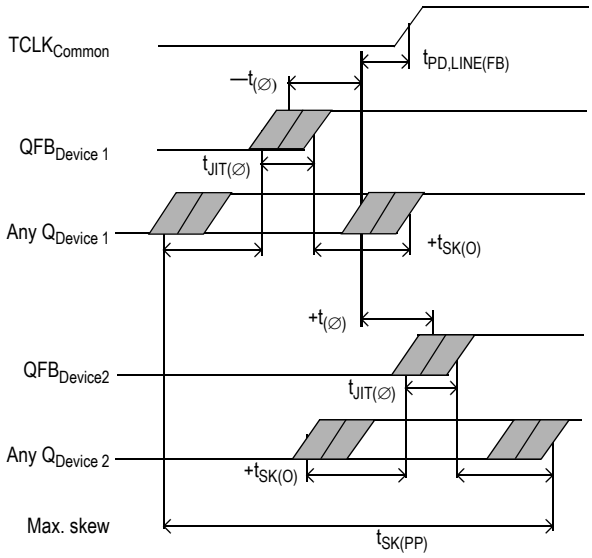


Figure 4. MPC93R51 Max. Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 9.

Table 9. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –251 ps to 351 ps relative to TCLK (V_{CC}=3.3V and f_{VCO} = 400 MHz):

$$t_{SK(PP)} = [-50ps...150ps] + [-150ps...150ps] + [(17ps \cdot -3)...(17ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [-251ps...351ps] + t_{PD,\ LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for V_{CC}=3.3V (17 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (200 MHz for the MPC93R51). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 5 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

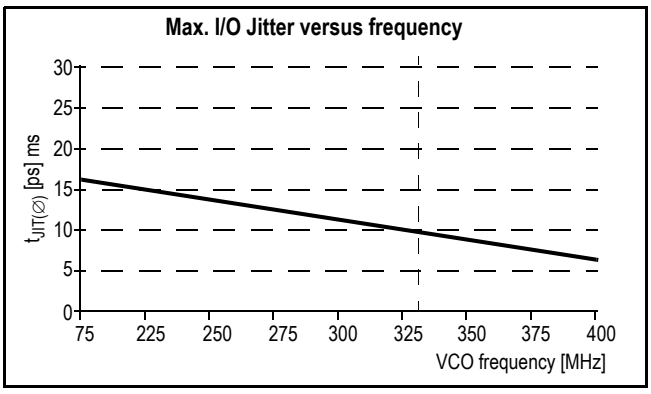


Figure 5. Max. I/O Jitter (RMS) Versus Frequency for V_{CC}=3.3V

Power Supply Filtering

The MPC93R51 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC93R51 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC93R51.

Figure 6. V_{CCA} Power Supply Filter illustrates a typical power supply filter scheme. The MPC93R51 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 6 must have a resistance of 5-15Ω to meet the voltage drop criteria.

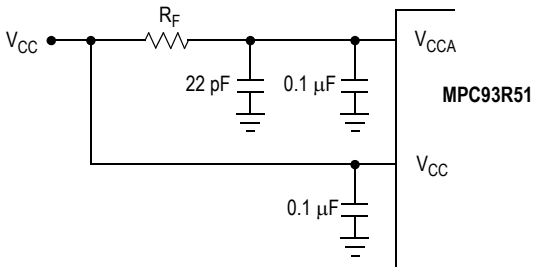


Figure 6. V_{CCA} Power Supply Filter

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC93R51 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC93R51 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC93R51 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 7. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC93R51 clock driver is effectively doubled due to its capability to drive multiple lines.

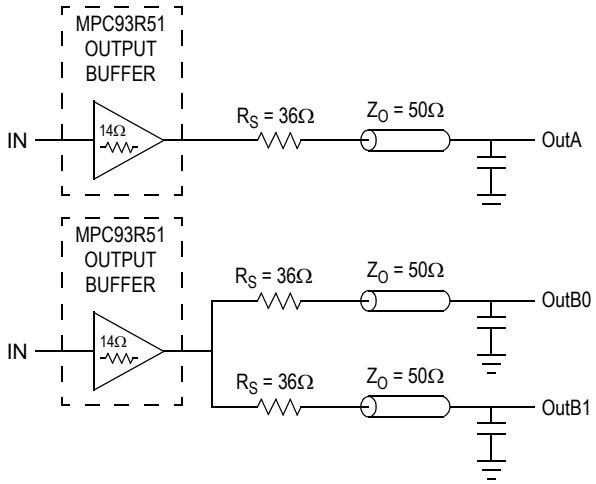


Figure 7. Single versus Dual Transmission Lines

The waveform plots in Figure 8. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC93R51 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC93R51. The output waveform in Figure 8 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 (25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

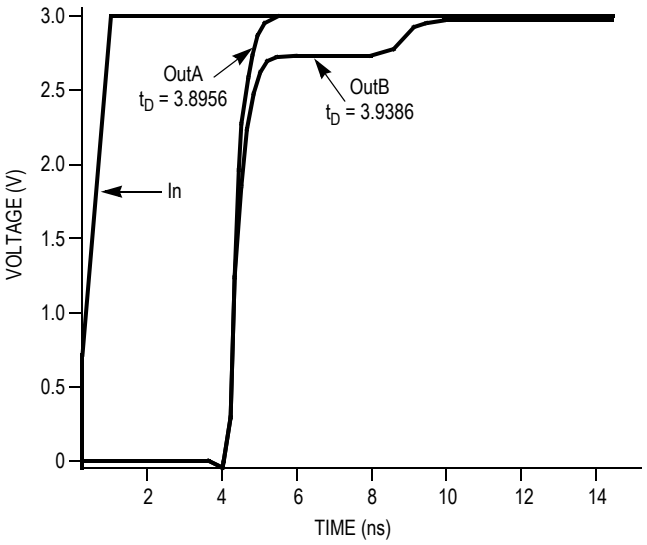
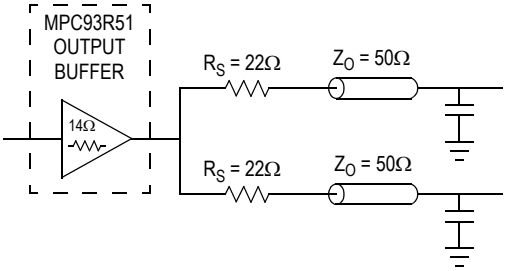


Figure 8. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 9. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$

$25\Omega = 25\Omega$

Figure 9. Optimized Dual Line Termination

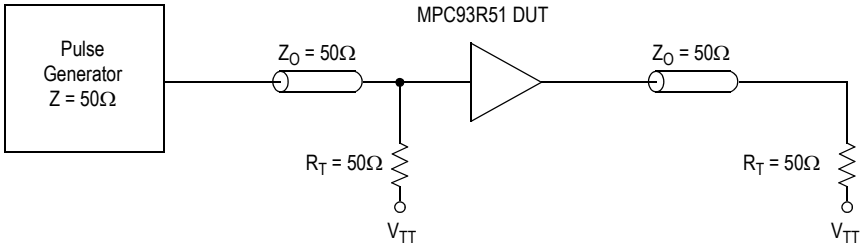


Figure 10. TCLK MPC93R51 AC Test Reference for V_{CC} = 3.3V

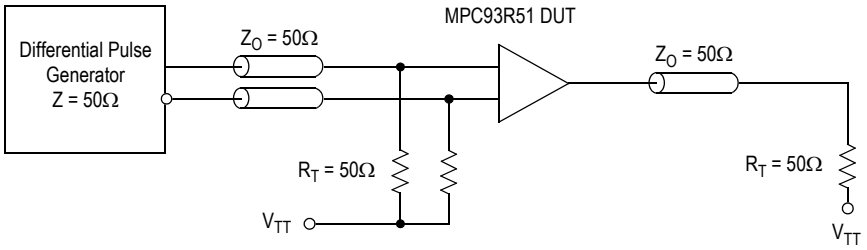


Figure 11. PCLK MPC9R351 AC Test Reference

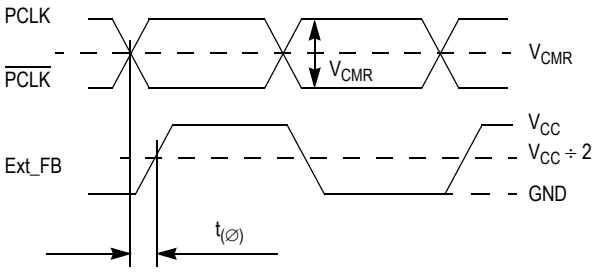


Figure 12. Propagation Delay (t_{PD}, Static Phase Offset) Test Reference

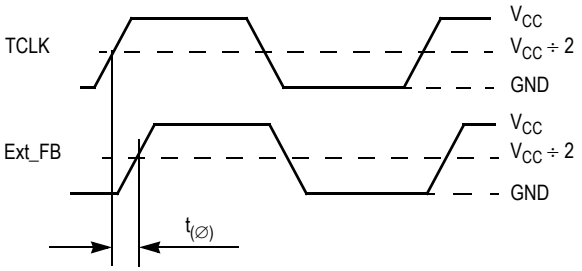
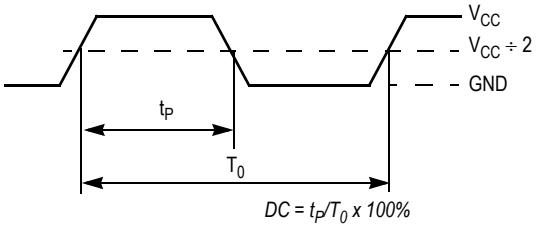
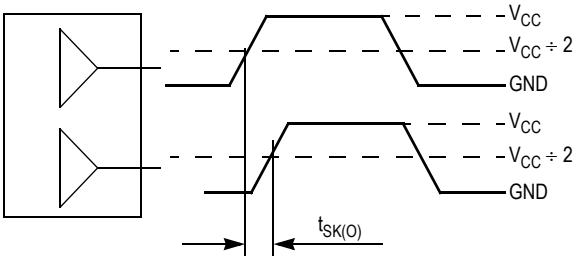


Figure 13. Propagation Delay (t_{PD}) Test Reference



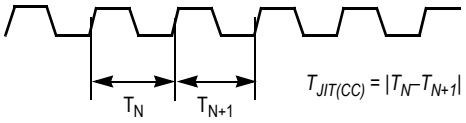
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 14. Output Duty Cycle (DC)



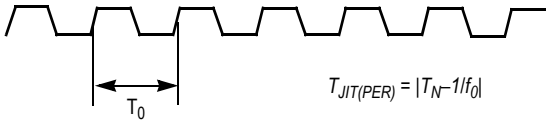
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 15. Output-to-Output Skew $t_{SK(O)}$



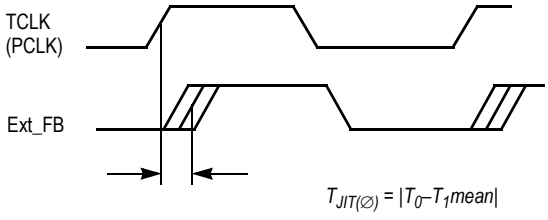
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 16. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 17. Period Jitter



The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 18. I/O Jitter

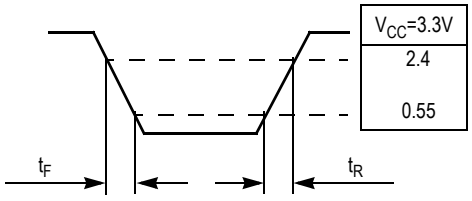


Figure 19. Transition Time Test Reference

Order number: MPC9352
Rev 4, 08/2004

3.3V/2.5V 1:11 LVCMOS Zero Delay Clock Generator

MPC9352

LOW VOLTAGE
3.3V/2.5V LVCMOS 1:11
CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC9352 is a 3.3V or 2.5V compatible, 1:11 PLL based clock generator targeted for high performance clock tree applications. With output frequencies up to 200 MHz and output skews lower than 200 ps the device meets the needs of most demanding clock applications.

Features

- Configurable 11 outputs LVCMOS PLL clock generator
- Fully integrated PLL
- Wide range of output clock frequency of 16.67 MHz to 200 MHz
- Multiplication of the input reference clock frequency by 3, 2, 1, 3 ÷ 2, 2 ÷ 3, 1 ÷ 3 and 1 ÷ 2
- 2.5V and 3.3V LVCMOS compatible
- Maximum output skew of 200 ps
- Supports zero-delay applications
- Designed for high-performance telecom, networking and computing applications
- 32-lead LQFP package
- 32-lead Pb-free Package Available
- Ambient Temperature Range –40°C to +85°C

Functional Description

The MPC9352 is a fully 3.3V or 2.5V compatible PLL clock generator and clock driver. The device has the capability to generate output clock signals of 16.67 to 200 MHz from external clock sources. The internal PLL optimized for its frequency range and does not require external look filter components. One output of the MPC9352 has to be connected to the PLL feedback input FB_IN to close the external PLL feedback path. The output divider of this output setting determines the PLL frequency multiplication factor. This multiplication factor, F_RANGE and the reference clock frequency must be selected to situate the VCO in its specified lock range. The frequency of the clock outputs can be configured individually for all three output banks by the FSELx pins supporting systems with different but phase-aligned clock frequencies.

The PLL of the MPC9352 minimizes the propagation delay and therefore supports zero-delay applications. All inputs and outputs are LVCMOS compatible. The outputs are optimized to drive parallel terminated 50Ω transmission lines. Alternatively, each output can drive up to two series terminated transmission lines giving the device an effective fanout of 22.

The device also supports output high-impedance disable and a PLL bypass mode for static system test and diagnosis. The MPC9352 is packaged in a 32 ld LQFP.

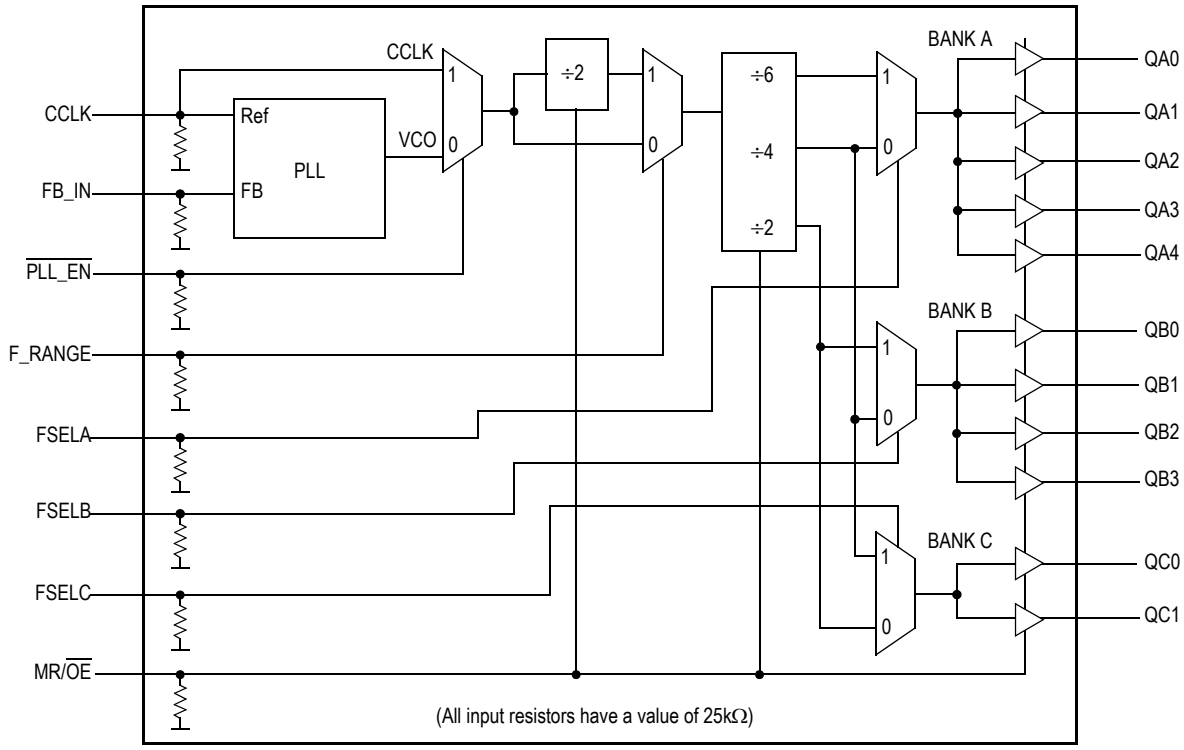
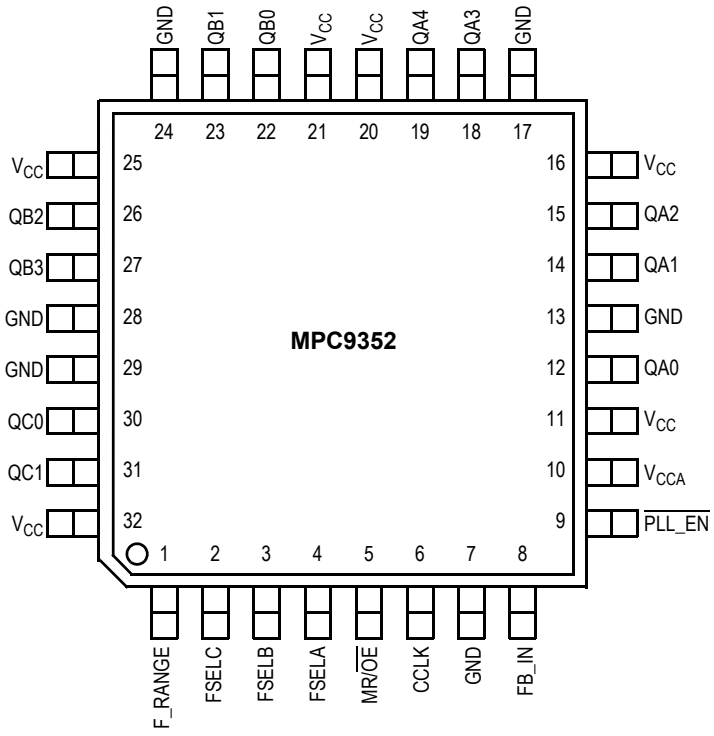


Figure 1. MPC9352 Logic Diagram



It is recommended to use an external RC filter for the analog power supply pin V_{CCA}. Please see application section for details.

Figure 2. MPC9352 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVCMOS	PLL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to an output
F_RANGE	Input	LVCMOS	PLL frequency range select
FSELA	Input	LVCMOS	Frequency divider select for bank A outputs
FSELB	Input	LVCMOS	Frequency divider select for bank B outputs
FSELC	Input	LVCMOS	Frequency divider select for bank C outputs
$\overline{\text{PLL\_EN}}$	Input	LVCMOS	PLL enable/disable
MR/$\overline{\text{OE}}$	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
QA0–4, QB0–3, QC0–1	Output	LVCMOS	Clock outputs
GND	Supply	Ground	Negative power supply
V_{CCA}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CCA}. Please see applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
F_RANGE, FSELA, FSELB, and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 9 and Table 10 for supported frequency ranges and output to input frequency ratios.			
F_RANGE	0	VCO ÷ 1 (High input frequency range)	VCO ÷ 2 (Low input frequency range)
FSELA	0	Output divider ÷ 4	Output divider ÷ 6
FSELB	0	Output divider ÷ 4	Output divider ÷ 2
FSELC	0	Output divider ÷ 2	Output divider ÷ 4
MR/$\overline{\text{OE}}$	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset, the PLL feedback loop is open and the VCO is operating at its lowest frequency. The MPC9352 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CCLK).
$\overline{\text{PLL\_EN}}$	0	Normal operation mode with PLL enabled.	Test mode with PLL disabled. CCLK is substituted for the internal VCO output. MPC9352 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24 mA I_{OL}= 12 mA
Z_{OUT}	Output impedance		14 – 17		Ω	
I_{IN}	Input Current[2]			±200	µA	V_{IN}=V_{CC} or V_{IN}=GND
I_{CCA}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}[3]	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

1. The MPC9352 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
2. Inputs have pull-down resistors affecting the input current.
3. I_{CCQ} is the DC current consumption of the device with all outputs open in high impedance state and the inputs in its default state or open.

Table 6. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency in PLL mode[2]	÷4 feedback	50.0		100.0	MHz	
		÷6 feedback	33.3		66.6	MHz	
		÷8 feedback	25.0		50.0	MHz	
		÷12 feedback	16.67		33.3	MHz	
	Input reference frequency in PLL bypass mode[3]				250.0	MHz	
f_{VCO}	VCO lock frequency range[4]		200		400	MHz	
f_{MAX}	Output Frequency	÷2 output[5]	100		200	MHz	
		÷4 output	50		100	MHz	
		÷6 output	33.3		66.6	MHz	
		÷8 output	25		50	MHz	
		÷12 output	16.67		33.3	MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
t_r, t_f	CCLK Input Rise/Fall Time				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay CCLK to FB_IN (static phase offset)	f_{ref} > 40 MHz	–50		+150	ps	PLL locked
		f_{ref} < 40 MHz	–200		+150	ps	
$t_{sk(O)}$	Output-to-output Skew[6]	all outputs, any frequency			200	ps	
		within QA output bank			200	ps	
		within QB output bank			100	ps	
		within QC output bank			100	ps	
DC	Output duty cycle		47	50	53	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				8	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter						
		output frequencies mixed			400	ps	
		outputs are in any ÷4 and ÷6 combination			250	ps	
		all outputs same frequency			100	ps	
$t_{JIT(PER)}$	Period Jitter	output frequencies mixed			200	ps	
		outputs are in any ÷4 and ÷6 combination			150	ps	
		all outputs same frequency			75	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	÷4 feedback divider RMS (1 σ)[7]		15		ps	
		÷6 feedback divider RMS (1 σ)		20		ps	
		÷8 feedback divider RMS (1 σ)		18 – 20		ps	
		÷12 feedback divider RMS (1 σ)		25		ps	
BW	PLL closed loop bandwidth[8]	÷4 feedback		3.0 – 10.0		MHz	
		÷6 feedback		1.5 – 6.0		MHz	
		÷8 feedback		1.0 – 3.5		MHz	
		÷12 feedback		0.5 – 2.0		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. PLL mode requires PLL_EN=0 to enable the PLL and zero-delay operation. It is not recommended to use a ÷2 divider for feedback.
3. In PLL bypass mode, the MPC9352 divides the input reference clock.
4. The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
5. See Table 9 and Table 10 for output divider configurations.
6. See application section for part-to-part skew calculation.
7. See application section for a jitter calculation for other confidence factors than 1 σ.
8. –3 dB point of PLL transfer characteristics.

Table 7. DC Characteristics (V_{CC} = 2.5V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	–0.3		0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.8			V	I_{OH}=–15 mA[1]
V_{OL}	Output Low Voltage			0.6	V	I_{OL}= 15mA
Z_{OUT}	Output Impedance		17 – 20		Ω	
I_{IN}	Input Current			±200	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CCQ}[2]	Maximum Quiescent Supply Current			1.0	mA	All V_{CC} Pins

1. The MPC9352 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.
2. I_{CCQ} is the DC current consumption of the device with all outputs open in high impedance state and the inputs in its default state or open.

Table 8. AC Characteristics (V_{CC} = 2.5V ± 5%, T_A = –40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency in PLL mode[2]	÷4 feedback	50.0		100.0	MHz	
		÷6 feedback	33.3		66.6	MHz	
		÷8 feedback	25.0		50.0	MHz	
		÷12 feedback	16.67		33.3	MHz	
	Input reference frequency in PLL bypass mode[3]				250.0	MHz	
f_{VCO}	VCO lock frequency range[4]		200		400	MHz	
f_{MAX}	Output Frequency	÷2 output[5]	100		200	MHz	
		÷4 output	50		100	MHz	
		÷6 output	33.3		66.6	MHz	
		÷8 output	25		50	MHz	
		÷12 output	16.67		33.3	MHz	
f_{refDC}	Reference Input Duty Cycle		25		75	%	
t_r, t_f	CCLK Input Rise/Fall Time				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay CCLK to FB_IN (static phase offset)	f_{ref} > 40 MHz	–50		+150	ps	PLL locked
		f_{ref} < 40 MHz	–200		+150	ps	
$t_{sk(O)}$	Output-to-output Skew[6]	all outputs, any frequency			200	ps	
		within QA output bank			200	ps	
		within QB output bank			100	ps	
		within QC output bank			100	ps	
DC	Output duty cycle		47	50	53	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8V
$t_{PLZ, HZ}$	Output Disable Time				8	ns	
$t_{PZL, ZH}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter						
		output frequencies mixed RMS (1 σ)			400	ps	
		outputs are in any ÷4 and ÷6 combination RMS (1 σ)			250	ps	
		all outputs same frequency RMS (1 σ)			100	ps	
$t_{JIT(PER)}$	Period Jitter	output frequencies mixed RMS (1 σ)			200	ps	
		outputs are in any ÷4 and ÷6 combination RMS (1 σ)			150	ps	
		all outputs same frequency RMS (1 σ)			75	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	÷4 feedback divider RMS (1 σ)[7]		15		ps	
		÷6 feedback divider RMS (1 σ)		20		ps	
		÷8 feedback divider RMS (1 σ)		18 – 20		ps	
		÷12 feedback divider RMS (1 σ)		25		ps	
BW	PLL closed loop bandwidth[8]	÷4 feedback		1.0 – 8.0		MHz	
		÷6 feedback		0.7 – 3.0		MHz	
		÷8 feedback		0.5 – 2.5		MHz	
		÷12 feedback		0.4 – 1.0		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. PLL mode requires PLL_EN=0 to enable the PLL and zero-delay operation. It is not recommended to use a ÷2 divider for feedback.
3. In PLL bypass mode, the MPC9352 divides the input reference clock.
4. The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
5. See Table 9 and Table 10 for output divider configurations.
6. See application section for part-to-part skew calculation.
7. See application section for a jitter calculation for other confidence factors than 1 σ.
8. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Programming the MPC9352

The MPC9352 supports output clock frequencies from 16.67 to 200 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 400 MHz for stable and optimal operation. The FSELA, FSELB, FSELC pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:1, 1:2, 1:3, 3:2 as well as 2:3, 3:1 and 2:1. Table 9 and Table 10 illustrates the various output configurations and frequency ratios supported by the MPC9352. See also Figure 3. MPC9352 Default Configuration to Figure 6. MPC9352 Zero Delay Buffer Configuration 2 for further reference. A ÷2 output divider cannot be used for feedback.

Table 9. MPC9352 Example Configuration (F_RANGE = 0)

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 4[2]	50-100	0	0	0	fref (50-100 MHz)	fref (50-100 MHz)	fref * 2 (100-200 MHz)
		0	0	1	fref (50-100 MHz)	fref (50-100 MHz)	fref (50-100 MHz)
		1	0	0	fref * 2÷3 (33-66 MHz)	fref (50-100 MHz)	fref * 2 (100-200 MHz)
		1	0	1	fref * 2÷3 (33-66 MHz)	fref (50-100 MHz)	fref (50-100 MHz)
VCO ÷ 6[3]	33.3-66.67	1	0	0	fref (33-66 MHz)	fref * 3÷2 (50-100 MHz)	fref * 3 (100-200 MHz)
		1	0	1	fref (33-66 MHz)	fref * 3÷2 (50-100 MHz)	fref * 3÷2 (50-100 MHz)
		1	1	0	fref (33-66 MHz)	fref * 3 (100-200 MHz)	fref * 3 (100-200 MHz)
		1	1	1	fref (33-66 MHz)	fref * 3 (100-200 MHz)	fref * 3÷2 (50-100 MHz)

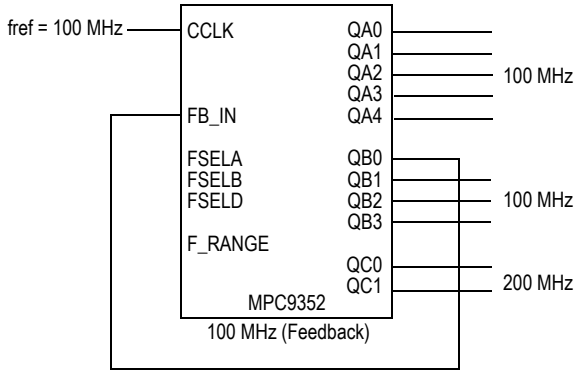
1. fref is the input clock reference frequency (CCLK)
2. QAx connected to FB_IN and FSELA=0
3. QAx connected to FB_IN and FSELA=1

Table 10. MPC9352 Example Configurations (F_RANGE = 1)

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 8[2]	25-50	0	0	0	fref (25-50 MHz)	fref (25-50 MHz)	fref * 2 (50-100 MHz)
		0	0	1	fref (25-50 MHz)	fref (25-50 MHz)	fref (25-50 MHz)
		1	0	0	fref * 2÷3 (16-33 MHz)	fref (25-50 MHz)	fref * 2 (50-100 MHz)
		1	0	1	fref * 2÷3 (16-33 MHz)	fref (25-50 MHz)	fref (25-50 MHz)
VCO ÷ 12[3]	16.67-33.3	1	0	0	fref (16-33 MHz)	fref * 3÷2 (25-50 MHz)	fref * 3 (50-100 MHz)
		1	0	1	fref (16-33 MHz)	fref * 3÷2 (25-50 MHz)	fref * 3÷2 (25-50 MHz)
		1	1	0	fref (16-33 MHz)	fref * 3 (50-100 MHz)	fref * 3 (50-100 MHz)
		1	1	1	fref (16-33 MHz)	fref * 3 (50-100 MHz)	fref * 3÷2 (25-50 MHz)

1. fref is the input clock reference frequency (CCLK)
2. QAx connected to FB_IN and FSELA=0
3. QAx connected to FB_IN and FSELA=1

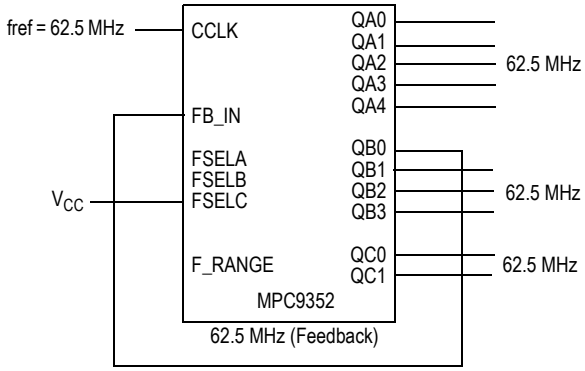
Example Configurations for the MPC9352



MPC9352 default configuration (feedback of QB0 = 100 MHz). All control pins are left open.

Frequency Range	Min	Max
Input	50 MHz	100 MHz
QA outputs	50 MHz	10 MHz
QB outputs	50 MHz	100 MHz
QC outputs	100 MHz	200 MHz

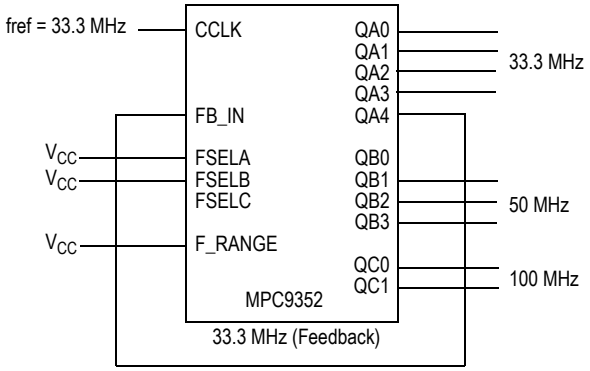
Figure 3. MPC9352 Default Configuration



MPC9352 zero-delay (feedback of QB0 = 62.5 MHz). All control pins are left open except FSELC = 1. All outputs are locked in frequency and phase to the input clock.

Frequency Range	Min	Max
Input	50 MHz	100 MHz
QA outputs	50 MHz	10 MHz
QB outputs	50 MHz	100 MHz
QC outputs	50 MHz	100 MHz

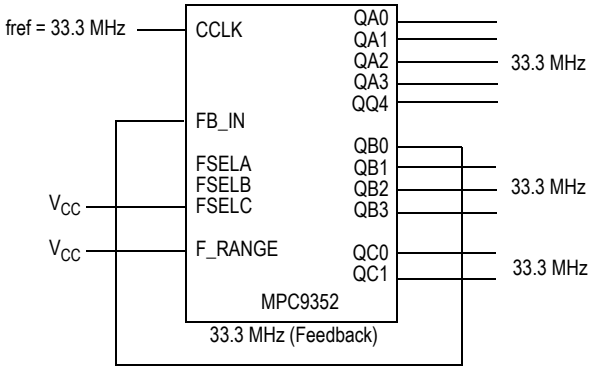
Figure 4. MPC9352 Zero Delay Buffer Configuration



MPC9352 configuration to multiply the reference frequency by 3, 3 ÷ 2 and 1. PLL feedback of QA4 = 33.3 MHz.

Frequency Range	Min	Max
Input	25 MHz	50 MHz
QA outputs	50 MHz	10 MHz
QB outputs	50 MHz	100 MHz
QC outputs	100 MHz	200 MHz

Figure 5. MPC9352 Default Configuration



MPC9352 zero-delay (feedback of QB0 = 33.3 MHz). Equivalent to Table 2 except F_RANGE = 1 enabling a lower input and output clock frequency.

Frequency Range	Min	Max
Input	25 MHz	50 MHz
QA outputs	25 MHz	50 MHz
QB outputs	25 MHz	50 MHz
QC outputs	25 MHz	50 MHz

Figure 6. MPC9352 Zero Delay Buffer Configuration 2

Power Supply Filtering

The MPC9352 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9352 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9352. Figure 7. VCCA Power Supply Filter illustrates a typical power supply filter scheme. The MPC9352 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325V (V_{CC}=3.3V or V_{CC}=2.5V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 7. VCCA Power Supply Filter should have a resistance of 5–15Ω (V_{CC}=3.3V) or 9–10Ω (V_{CC}=2.5V) to meet the voltage drop criteria.

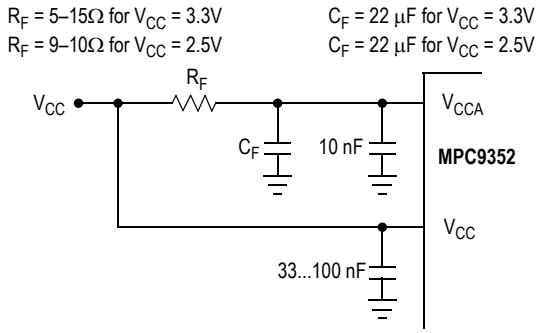


Figure 7. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7. VCCA Power Supply Filter, the filter cut-off frequency is around 3–5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9352 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9352 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9352. Designs using the MPC9352 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9352 clock driver allows for its use as a zero delay buffer. One example configuration is to use a ÷4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9352 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9352 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \bullet CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

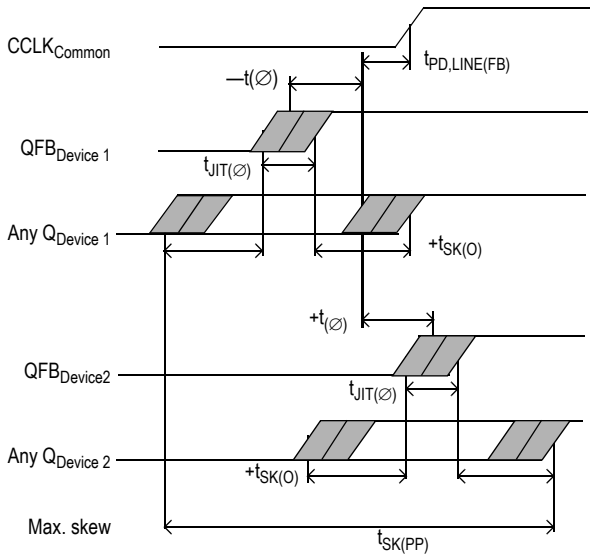


Figure 8. MPC9352 max. device-to-device skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 11.

Table 11. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –445 ps to 395 ps relative to CCLK:

$t_{SK(PP)}$ = *[–200ps...150ps] + [-200ps...200ps] + [(15ps • –3)...(15ps • 3)] +* $t_{PD, LINE(FB)}$

$t_{SK(PP)}$ = *[–445ps...395ps]* + $t_{PD, LINE(FB)}$

Due to the frequency dependence of the I/O jitter, Figure 9. Max. I/O Jitter versus Frequency can be used for a more precise timing performance analysis.

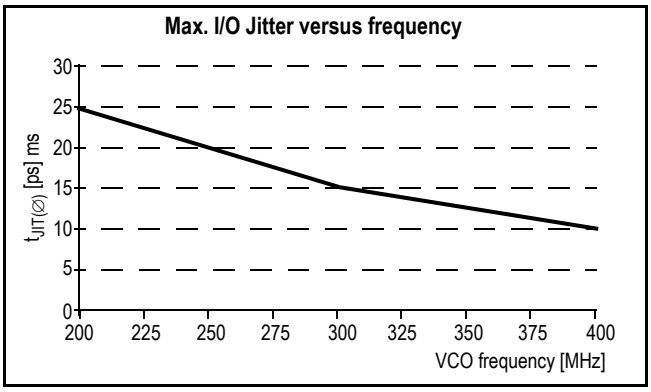


Figure 9. Max. I/O Jitter versus Frequency

Driving Transmission Lines

The MPC9352 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9352 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 10. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9352 clock driver is effectively doubled due to its capability to drive multiple lines.

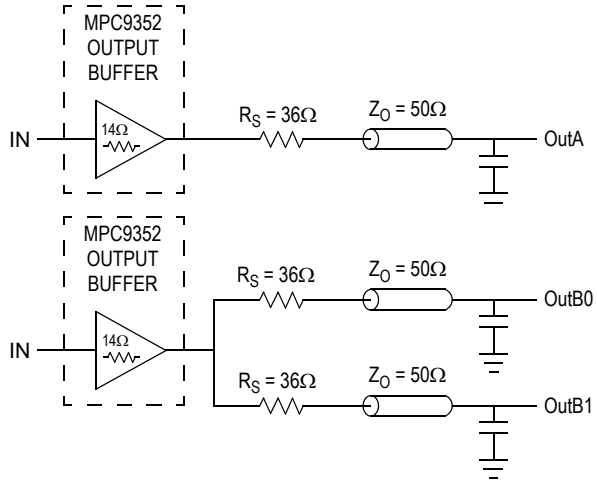


Figure 10. Single versus Dual Transmission Lines

The waveform plots in Figure 11. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9352 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9352. The output waveform in Figure 11. Single versus Dual Waveforms shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S+R_0 +Z_0))$

Z_0 = 50Ω || 50Ω

R_S = 36Ω || 36Ω

R_0 = 14Ω

V_L = 3.0 (25 ÷ (18+17+25))

= 1.31V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

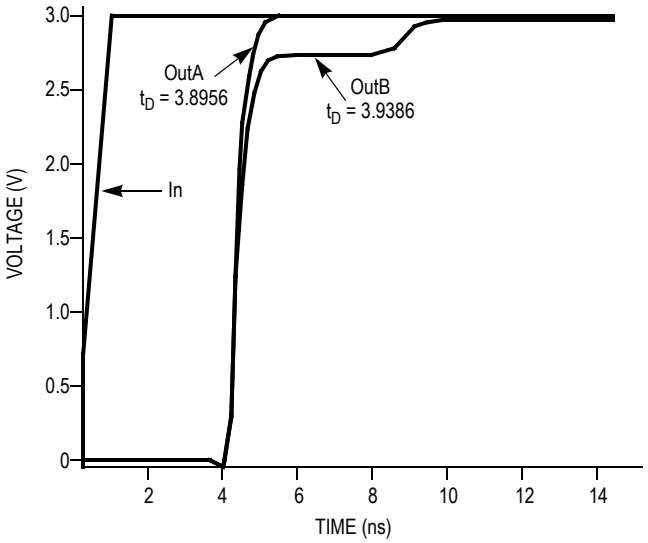


Figure 11. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 12. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

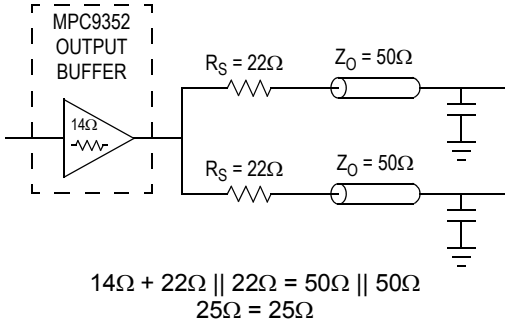


Figure 12. Optimized Dual Line Termination

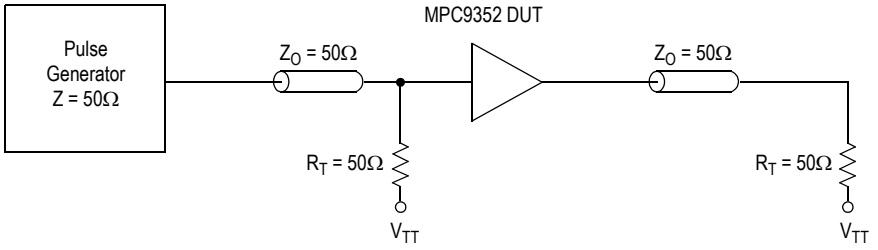
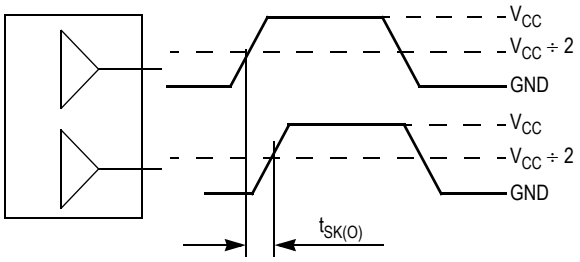


Figure 13. CCLK MPC9352 AC Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 14. Output-to-Output Skew $t_{SK(O)}$

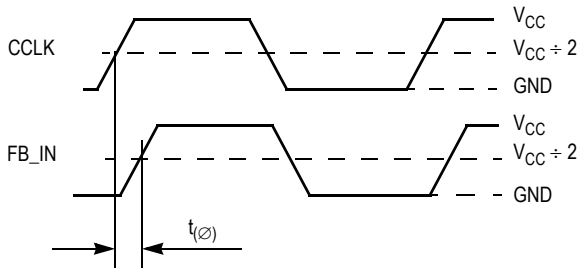
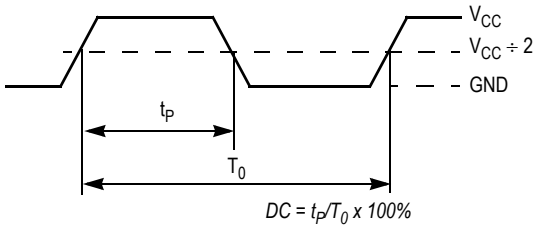
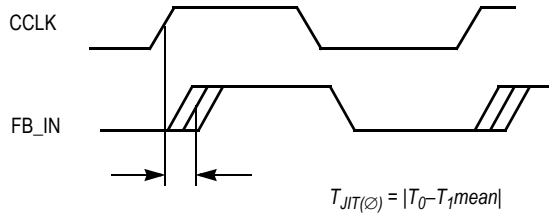


Figure 15. Propagation Delay ($t_{(\varnothing)}$, static phase offset) Test Reference



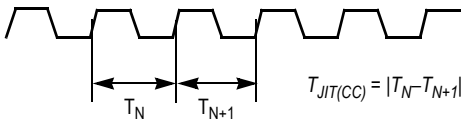
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)



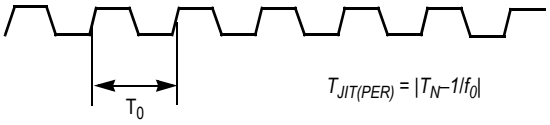
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 17. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 18. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 19. Period Jitter

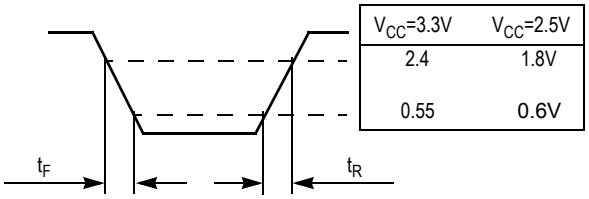


Figure 20. Output Transition Time Test Reference

3.3V 1:11 LVCMOS Zero Delay Clock Generator

MPC93H52

LOW VOLTAGE
3.3V LVCMOS 1:11
CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC93H52 is a 3.3V compatible, 1:11 PLL based clock generator targeted for high performance clock tree applications. With output frequencies up to 240 MHz and output skews lower than 200 ps the device meets the needs of most demanding clock applications.

Features

- Configurable 11 outputs LVCMOS PLL clock generator
- Fully integrated PLL
- Wide range of output clock frequency of 16.67 MHz to 240 MHz
- Multiplication of the input reference clock frequency by 3, 2, 1, 3÷2, 2÷3, 1÷3 and 1÷2
- 3.3V LVCMOS compatible
- Maximum output skew of 200 ps
- Supports zero-delay applications
- Designed for high-performance telecom, networking and computing applications
- 32-lead LQFP package
- 32-lead Pb-free Package Available
- Ambient Temperature Range — 0°C to +70°C
- Pin and function compatible to the MPC952

Functional Description

The MPC93H52 is a fully 3.3 V compatible PLL clock generator and clock driver. The device has the capability to generate output clock signals of 16.67 to 240 MHz from external clock sources. The internal PLL optimized for its frequency range and does not require external look filter components. One output of the MPC93H52 has to be connected to the PLL feedback input FB_IN to close the external PLL feedback path. The output divider of this output setting determines the PLL frequency multiplication factor. This multiplication factor, F_RANGE and the reference clock frequency must be selected to situate the VCO in its specified lock range. The frequency of the clock outputs can be configured individually for all three output banks by the FSELx pins supporting systems with different but phase-aligned clock frequencies.

The PLL of the MPC93H52 minimizes the propagation delay and therefore supports zero-delay applications. All inputs and outputs are LVCMOS compatible. The outputs are optimized to drive parallel terminated 50 Ω transmission lines. Alternatively, each output can drive up to two series terminated transmission lines giving the device an effective fanout of 22.

The device also supports output high-impedance disable and a PLL bypass mode for static system test and diagnosis. The MPC93H52 is package in a 32-lead LQFP.

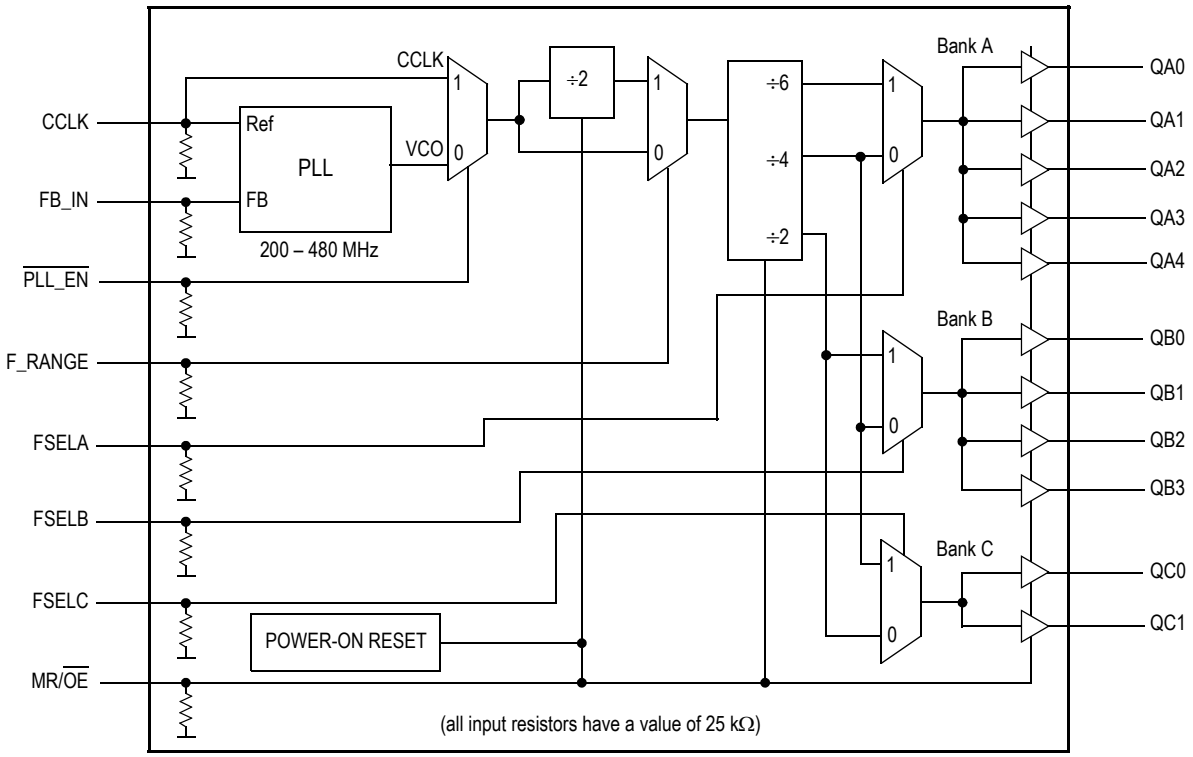
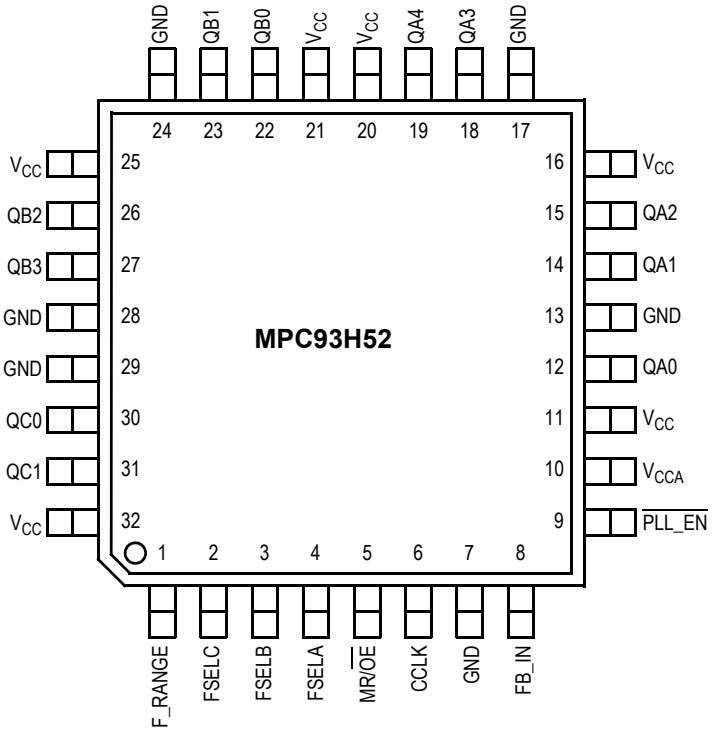


Figure 1. MPC93H52 Logic Diagram



It is recommended to use an external RC filter for the analog power supply pin V_{CCA}. Please see APPLICATIONS INFORMATION for details.

Figure 2. MPC93H52 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVCMOS	PLL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to an output
F_RANGE	Input	LVCMOS	PLL frequency range select
FSELA	Input	LVCMOS	Frequency divider select for bank A outputs
FSELB	Input	LVCMOS	Frequency divider select for bank B outputs
FSELC	Input	LVCMOS	Frequency divider select for bank C outputs
$\overline{\text{PLL\_EN}}$	Input	LVCMOS	PLL enable/disable
MR/OE	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
QA0–4, QB0–3, QC0–1	Output	LVCMOS	Clock outputs
GND	Supply	Ground	Negative power supply
V_{CCA}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CCA}. Please see applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
F_RANGE, FSELA, FSELB, and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 7 and Table 8 for supported frequency ranges and output to input frequency ratios.			
F_RANGE	0	VCO ÷ 1 (High input frequency range)	VCO ÷ 2 (Low input frequency range)
FSELA	0	Output divider ÷ 4	Output divider ÷ 6
FSELB	0	Output divider ÷ 4	Output divider ÷ 2
FSELC	0	Output divider ÷ 2	Output divider ÷ 4
MR/$\overline{\text{OE}}$	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset, the PLL feedback loop is open and the VCO is operating at its lowest frequency. The MPC93H52 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CCLK). The device is reset by the internal power-on reset (POR) circuitry during power-up.
$\overline{\text{PLL\_EN}}$	0	Normal operation mode with PLL enabled.	Test mode with PLL disabled. CCLK is substituted for the internal VCO output. MPC93H52 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD (Machine Model)	200			V	
HBM	ESD (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0° to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance		7 – 10		Ω	
I_{IN}	Input Current[2]			±200	μA	V_{IN} = V_{CC} or V_{IN} = GND
I_{CCA}	Maximum PLL Supply Current		8	12	mA	V_{CCA} Pin
I_{CCQ}[3]	Maximum Quiescent Supply Current		10	16	mA	All V_{CC} Pins

1. The MPC93H52 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
2. Inputs have pull-down resistors affecting the input current.
3. I_{CCQ} is the DC current consumption of the device with all outputs open in high impedance state and the inputs in its default state or open.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0° to 70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency in PLL mode[2 3]	÷4 feedback	50.0		120.0	MHz	
		÷6 feedback	33.3		80.0	MHz	
		÷8 feedback	25.0		60.0	MHz	
		÷12 feedback	16.67		40.0	MHz	
	Input reference frequency in PLL bypass mode[4]		50.0		250.0	MHz	
f_{VCO}	VCO lock frequency range[5]		200		480	MHz	
f_{MAX}	Output Frequency	÷2 output[6]	100		240	MHz	
		÷4 output	50		120	MHz	
		÷6 output	33.3		80	MHz	
		÷8 output	25		60	MHz	
		÷12 output	16.67		40	MHz	
t_{PWMIN}	Minimum Reference Input Pulse Width		2.0			ns	
t_r, t_f	CCLK Input Rise/Fall Time[7]				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay CCLK to FB_IN (static phase offset)	(f_{ref} = 50MHz)	–200		+200	ps ps	PLL locked
$t_{sk(O)}$	Output-to-output Skew[8]	all outputs, any frequency			300	ps	
		within QA output bank			200	ps	
		within QB output bank			200	ps	
		within QC output bank			100	ps	
DC	Output duty cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				8	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter	output frequencies mixed			150	ps	RMS
		all outputs same frequency			25	ps	RMS
$t_{JIT(PER)}$	Period Jitter	output frequencies mixed			75	ps	RMS
		all outputs same frequency			20	ps	RMS
$t_{JIT(\varnothing)}$	I/O Phase Jitter[9]	÷4 feedback divider RMS (1 σ)		40		ps	
		÷6 feedback divider RMS (1 σ)		40		ps	
		÷8 feedback divider RMS (1 σ)		40		ps	
		÷12 feedback divider RMS (1 σ)		40		ps	
BW	PLL closed loop bandwidth[10]	÷4 feedback		2.0–8.0		MHz	
		÷6 feedback		1.0–4.0		MHz	
		÷8 feedback		0.8–2.5		MHz	
		÷12 feedback		0.6–1.5		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}
2. PLL mode requires PLL_EN=0 to enable the PLL and zero-delay operation.
3. The PLL may be unstable with a divide by 2 feedback ratio.
4. In PLL bypass mode, the MPC93H52 divides the input reference clock.
5. The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
6. See Table 7 and Table 8 for output divider configurations.
7. The MPC93H52 will operate with input rise and fall times up to 3.0 ns, but the AC characteristics, specifically $t_{(\varnothing)}$, can only be guaranteed if t_r/t_f are within the specified range.
8. See application section for part-to-part skew calculation.
9. See application section for a jitter calculation for other confidence factors than 1 σ.
10. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Programming the MPC93H52

The MPC93H52 supports output clock frequencies from 16.67 to 240 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 480 MHz for stable and optimal operation. The FSELA, FSELB, FSELC pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:1, 1:2, 1:3, 3:2 as well as 2:3, 3:1 and 2:1. Table 7 illustrates the various output configurations and frequency ratios supported by the MPC93H52. See also Table 8 and to Figure 6. MPC93H52 Zero Delay Buffer Configuration 2 for further reference. A ÷2 output divider cannot be used for feedback.

Table 7. MPC93H52 Example Configuration (F_RANGE = 0)

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 4[2]	50-120	0	0	0	fref (50-120 MHz)	fref (50-120 MHz)	fref · 2 (100-240 MHz)
		0	0	1	fref (50-120 MHz)	fref (50-120 MHz)	fref (50-120 MHz)
		1	0	0	fref · 2÷3 (33-80 MHz)	fref (50-120 MHz)	fref · 2 (100-240 MHz)
		1	0	1	fref · 2÷3 (33-80 MHz)	fref (50-120 MHz)	fref (50-120 MHz)
VCO ÷ 6[3]	33.3-80	1	0	0	fref (33-80 MHz)	fref ·3÷2 (50-120 MHz)	fref · 3 (100-240 MHz)
		1	0	1	fref (33-80 MHz)	fref ·3÷2 (50-120 MHz)	fref ·3÷2 (50-120 MHz)
		1	1	0	fref (33-80 MHz)	fref · 3 (100-240 MHz)	fref · 3 (100-240 MHz)
		1	1	1	fref (33-80 MHz)	fref · 3 (100-240 MHz)	fref ·3÷2 (50-120 MHz)

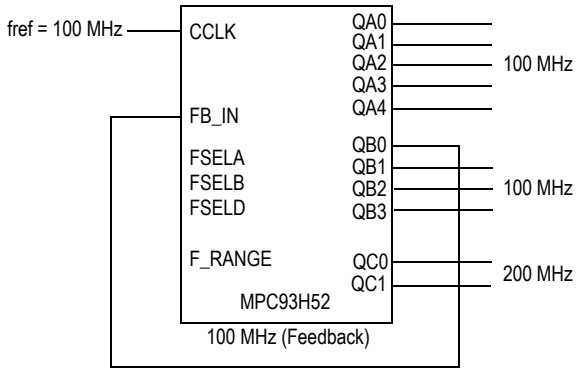
1. fref is the input clock reference frequency (CCLK)
2. fref is the input clock reference frequency (CCLK)
3. fref is the input clock reference frequency (CCLK)

Table 8. MPC93H52 Example Configurations (F_RANGE = 1)

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 8[2]	25-60	0	0	0	fref (25-60 MHz)	fref (25-60 MHz)	fref · 2 (50-120 MHz)
		0	0	1	fref (25-60 MHz)	fref (25-60 MHz)	fref (25-60 MHz)
		1	0	0	fref ·2÷3 (16-40 MHz)	fref (25-60 MHz)	fref · 2 (50-120 MHz)
		1	0	1	fref ·2÷3 (16-40 MHz)	fref (25-60 MHz)	fref (25-60 MHz)
VCO ÷ 12[3]	16.67-40	1	0	0	fref (16-40 MHz)	fref ·3÷2 (25-60 MHz)	fref · 3 (50-120 MHz)
		1	0	1	fref (16-40 MHz)	fref ·3÷2 (25-60 MHz)	fref ·3÷2 (25-60 MHz)
		1	1	0	fref (16-40 MHz)	fref · 3 (50-120 MHz)	fref · 3 (50-120 MHz)
		1	1	1	fref (16-40 MHz)	fref · 3 (50-120 MHz)	fref ·3÷2 (25-60 MHz)

1. fref is the input clock reference frequency (CCLK)
2. QAx connected to FB_IN and FSELA=0
3. QAx connected to FB_IN and FSELA=1

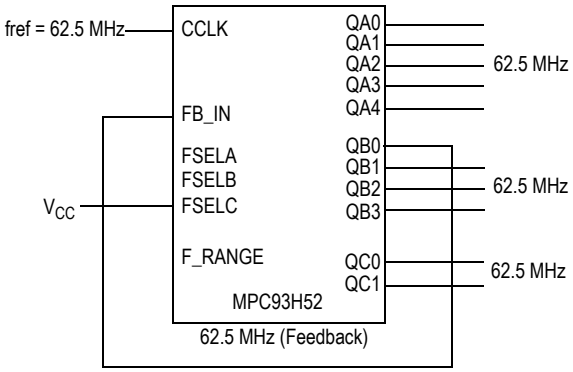
Example Configurations for the MPC93H52



MPC93H52 default configuration (feedback of QB0 = 100 MHz). All control pins are left open.

Frequency range	Min	Max
Input	50 MHz	120 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

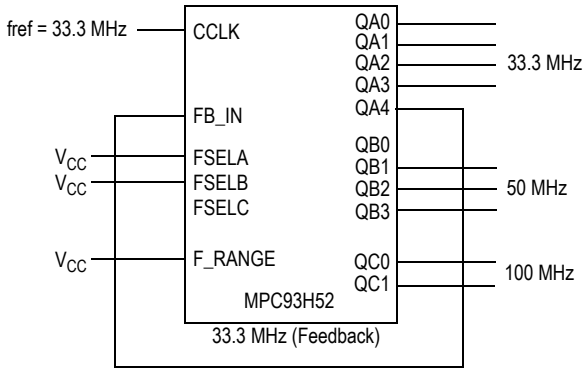
Figure 3. MPC93H52 Default Configuration



MPC93H52 zero-delay (feedback of QB0 = 62.5 MHz). All control pins are left open except FSELC = 1. All outputs are locked in frequency and phase to the input clock.

Frequency range	Min	Max
Input	50 MHz	120 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	50 MHz	120 MHz

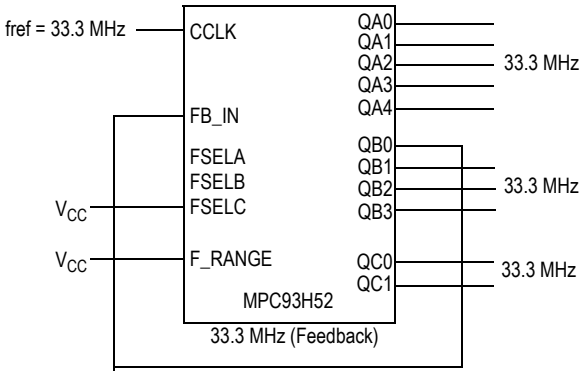
Figure 4. MPC93H52 Default Configuration



MPC93H52 configuration to multiply the reference frequency by 3, 3÷2 and 1. PLL feedback of QA4 = 33.3 MHz.

Frequency range	Min	Max
Input	25 MHz	60 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

Figure 5. MPC93H52 Default Configuration



MPC93H52 zero-delay (feedback of QB0 = 33.3 MHz). Equivalent to Table 2 except F_RANGE = 1 enabling a lower input and output clock frequency.

Frequency range	Min	Max
Input	25 MHz	60 MHz
QA outputs	25 MHz	60 MHz
QB outputs	25 MHz	60 MHz
QC outputs	25 MHz	60 MHz

Figure 6. MPC93H52 Zero Delay Buffer Configuration 2

Power Supply Filtering

The MPC93H52 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC93H52 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC93H52. Figure 7. VCCA Power Supply Filter illustrates a typical power supply filter scheme. The MPC93H52 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 8 mA (12 mA maximum), assuming that a minimum of 2.98V must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 7. VCCA Power Supply Filter should have a resistance of 5–25Ω to meet the voltage drop criteria.

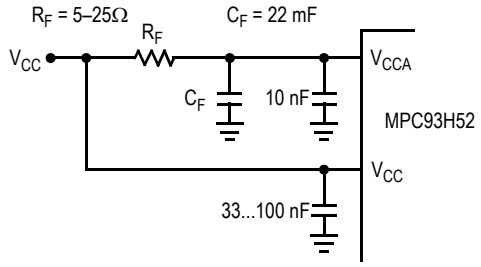


Figure 7. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7. VCCA Power Supply Filter, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC93H52 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC93H52 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC93H52. Designs using the MPC93H52 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC93H52 clock driver allows for its use as a zero delay buffer. One example configuration is to use a ÷4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC93H52 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC93H52 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \bullet CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

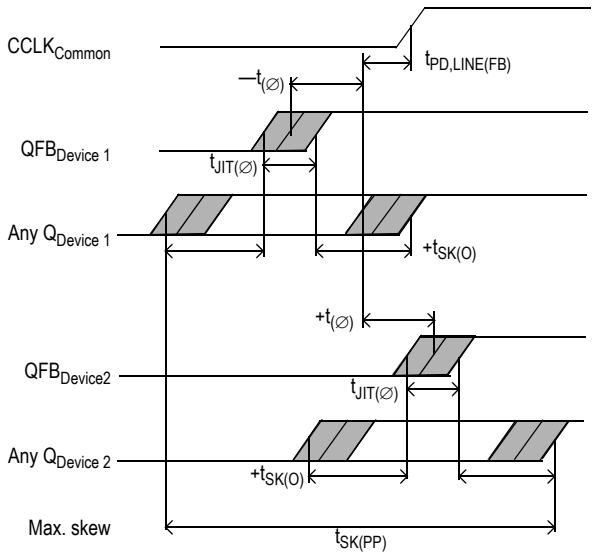


Figure 8. MPC93H51 Maximum Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 9.

Table 9. Confidence Factor CF

CF	Probability of Clock Edge within the Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –445 ps to 395 ps relative to CCLK:

$t_{SK(PP)}$ = *[–200ps...150ps] + [–200ps...200ps] + [(15ps • –3)...(15ps • 3)] +* $t_{PD, LINE(FB)}$

$t_{SK(PP)}$ = *[–445ps...395ps] +* $t_{PD, LINE(FB)}$

Driving Transmission Lines

The MPC93H52 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC93H52 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 9. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC93H52 clock driver is effectively doubled due to its capability to drive multiple lines.

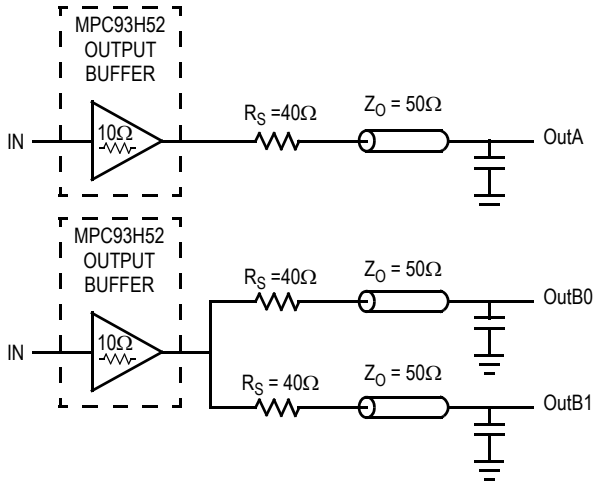


Figure 9. Single versus Dual Transmission Lines

The waveform plots in Figure 10. Single versus Dual Waveforms and Figure 11. Optimized Dual Line Termination show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC93H51 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC93H51. The output waveform in Figure 10. Single versus Dual Waveforms and Figure 11. Optimized Dual Line Termination shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$

$Z_0 = 50\ \Omega \parallel 50\ \Omega$

$R_S = 40\ \Omega \parallel 40\ \Omega$

$R_0 = 10\ \Omega$

$V_L = 3.0\ (25 \div (20 + 10 + 25)$

$= 1.36$ V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.7 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 11. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

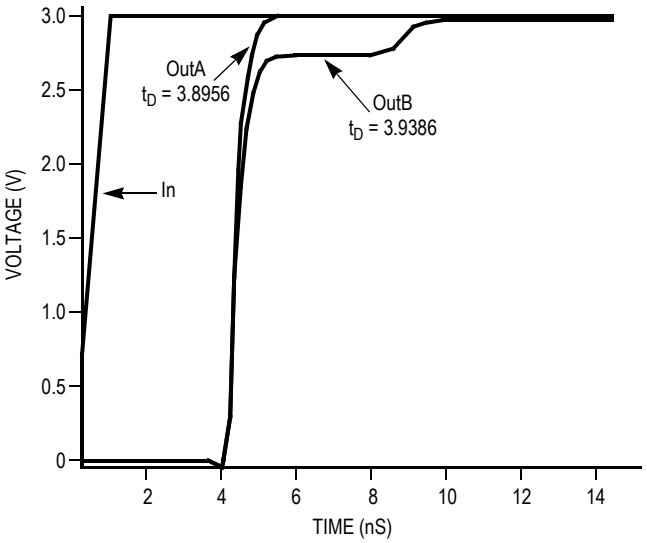


Figure 10. Single versus Dual Waveforms

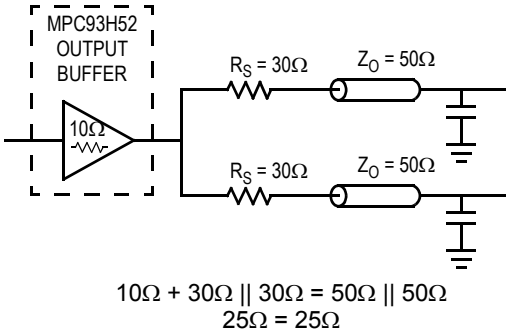


Figure 11. Optimized Dual Line Termination

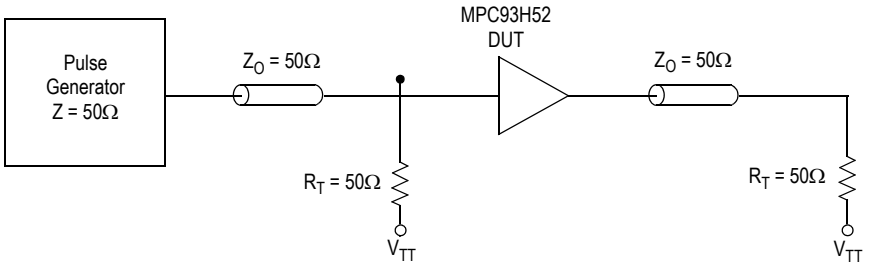
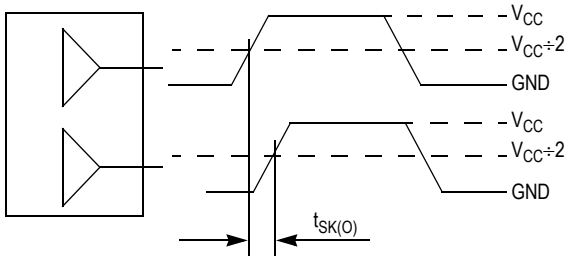


Figure 12. CCLK MPC93H52 AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 13. Output-to-Output Skew $t_{SK(O)}$

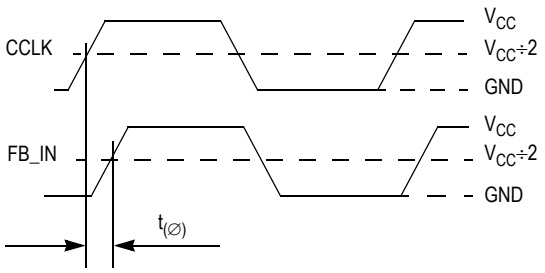
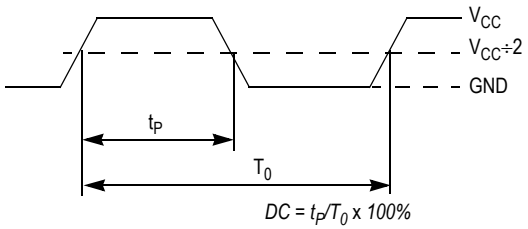
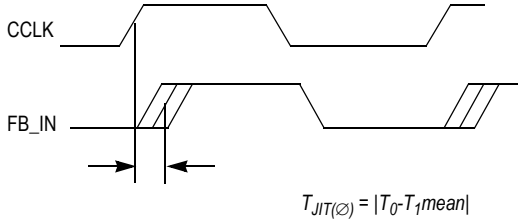


Figure 14. Propagation Delay ($t_{(\varnothing)}$, status phase offset) Test Reference



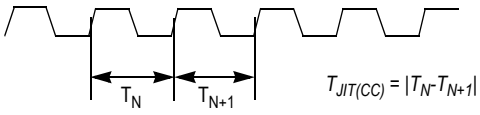
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 15. Output Duty Cycle (DC)



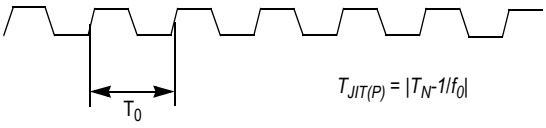
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 16. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 17. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 18. Period Jitter

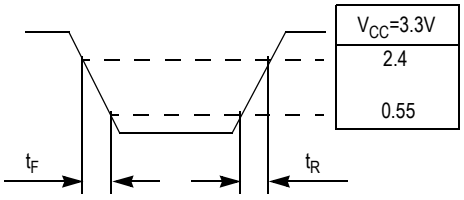


Figure 19. Output Transition Time Test Reference

Order number: MPC93R52
Rev 3, 08/2004

3.3V 1:11 LVCMOS Zero Delay Clock Generator

MPC93R52

LOW VOLTAGE
3.3V LVCMOS 1:11
CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC93R52 is a 3.3V compatible, 1:11 PLL based clock generator targeted for high performance clock tree applications. With output frequencies up to 240 MHz and output skews lower than 200 ps the device meets the needs of most demanding clock applications.

Features

- Configurable 11 outputs LVCMOS PLL clock generator
- Fully integrated PLL
- Wide range of output clock frequency of 16.67 MHz to 240 MHz
- Multiplication of the input reference clock frequency by 3, 2, 1, 3 ÷ 2, 2 ÷ 3, 1 ÷ 3, and 1 ÷ 2
- 3.3V LVCMOS compatible
- Maximum output skew of 200 ps
- Supports zero-delay applications
- Designed for high-performance telecom, networking and computing applications
- 32-lead LQFP package
- 32-lead Pb-free package available
- Ambient Temperature Range – 0°C to +70°C
- Pin and function compatible to the MPC952

Functional Description

The MPC93R52 is a fully 3.3V compatible PLL clock generator and clock driver. The device has the capability to generate output clock signals of 16.67 to 240 MHz from external clock sources. The internal PLL optimized for its frequency range and does not require external look filter components. One output of the MPC93R52 has to be connected to the PLL feedback input FB_IN to close the external PLL feedback path. The output divider of this output setting determines the PLL frequency multiplication factor. This multiplication factor, F_RANGE and the reference clock frequency must be selected to situate the VCO in its specified lock range. The frequency of the clock outputs can be configured individually for all three output banks by the FSELx pins supporting systems with different but phase-aligned clock frequencies.

The PLL of the MPC93R52 minimizes the propagation delay and therefore supports zero-delay applications. All inputs and outputs are LVCMOS compatible. The outputs are optimized to drive parallel terminated 50Ω transmission lines. Alternatively, each output can drive up to two series terminated transmission lines giving the device an effective fanout of 22.

The device also supports output high-impedance disable and a PLL bypass mode for static system test and diagnosis. The MPC93R52 is package in a 32 ld LQFP.

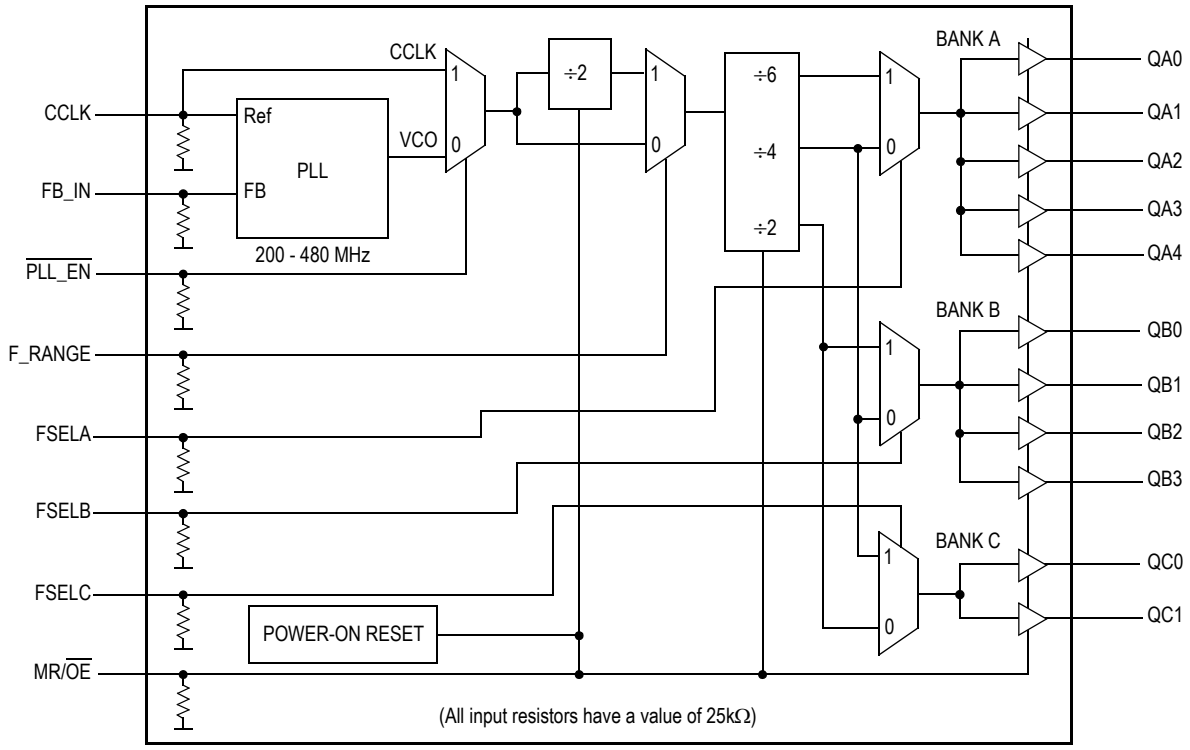
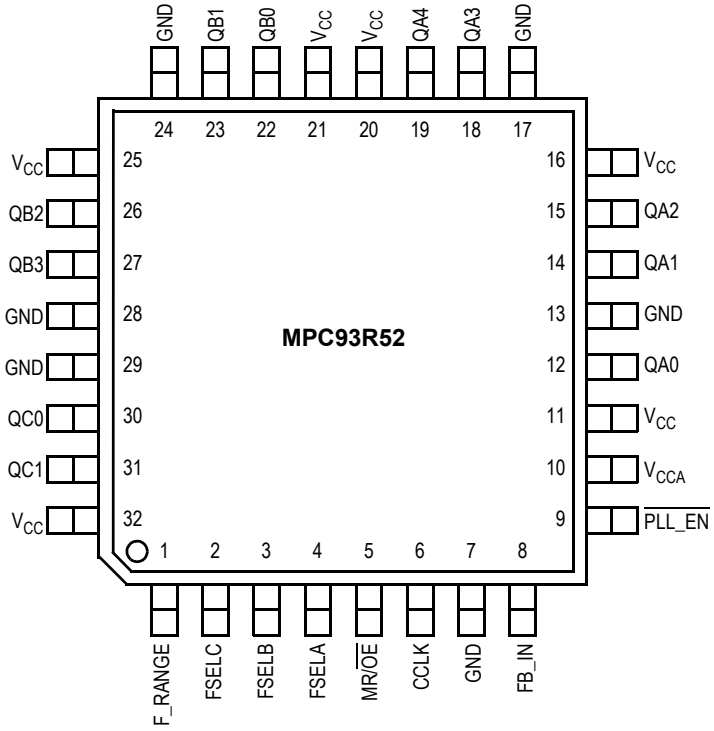


Figure 1. MPC93R52 Logic Diagram



It is recommended to use an external RC filter for the analog power supply pin V_{CCA}. Please see application section for details.

Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVCMOS	PLL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to an output
F_RANGE	Input	LVCMOS	PLL frequency range select
FSELA	Input	LVCMOS	Frequency divider select for bank A outputs
FSELB	Input	LVCMOS	Frequency divider select for bank B outputs
FSELC	Input	LVCMOS	Frequency divider select for bank C outputs
$\overline{\text{PLL\_EN}}$	Input	LVCMOS	PLL enable/disable
MR/$\overline{\text{OE}}$	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
QA0–4, QB0–3, QC0–1	Output	LVCMOS	Clock outputs
GND	Supply	Ground	Negative power supply
V_{CCA}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CCA}. Please see applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
F_RANGE, FSELA, FSELB, and FSELC control the operating PLL frequency range and input/output frequency ratios. See Table 7 and Table 8 for supported frequency ranges and output to input frequency ratios.			
F_RANGE	0	VCO ÷ 1 (High input frequency range)	VCO ÷ 2 (Low input frequency range)
FSELA	0	Output divider ÷ 4	Output divider ÷ 6
FSELB	0	Output divider ÷ 4	Output divider ÷ 2
FSELC	0	Output divider ÷ 2	Output divider ÷ 4
MR/$\overline{\text{OE}}$	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset, the PLL feedback loop is open and the VCO is operating at its lowest frequency. The MPC93R52 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CCLK). The device is reset by the internal power-on reset (POR) circuitry during power-up.
$\overline{\text{PLL\_EN}}$	0	Normal operation mode with PLL enabled.	Test mode with PLL disabled. CCLK is substituted for the internal VCO output. MPC93R52 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0° to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH}=–24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24 mA I_{OL}= 12 mA
Z_{OUT}	Output impedance		14 – 17		Ω	
I_{IN}	Input Current[2]			±200	μA	V_{IN}=V_{CC} or V_{IN}=GND
I_{CCA}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}[3]	Maximum Quiescent Supply Current		7.0	1.0	mA	All V_{CC} Pins

1. The MPC93R52 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
2. Inputs have pull-down resistors affecting the input current.
3. I_{CCQ} is the DC current consumption of the device with all outputs open in high impedance state and the inputs in its default state or open.

Table 6. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0° to 70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input reference frequency in PLL mode[2, 3]	÷4 feedback	50.0		120.0	MHz	
		÷6 feedback	33.3		80.0	MHz	
		÷8 feedback	25.0		60.0	MHz	
		÷12 feedback	16.67		40.0	MHz	
	Input reference frequency in PLL bypass mode[4]		50.0		250.0	MHz	
f_{VCO}	VCO lock frequency range[5]		200		480	MHz	
f_{MAX}	Output Frequency	÷2 output[6]	100		240	MHz	
		÷4 output	50		120	MHz	
		÷6 output	33.3		80	MHz	
		÷8 output	25		60	MHz	
		÷12 output	16.67		40	MHz	
t_{PWMIN}	Minimum Reference Input Pulse Width		2.0			ns	
t_r, t_f	CCLK Input Rise/Fall Time[7]				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay CCLK to FB_IN (static phase offset)	f_{ref} > 50 MHz	–100		+200	ps	PLL locked
$t_{sk(O)}$	Output-to-output Skew[8]	all outputs, any frequency			150	ps	
		within QA output bank			100	ps	
		within QB output bank			100	ps	
		within QC output bank			50	ps	
DC	Output duty cycle		47	50	53	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				8	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter						
		output frequencies mixed			400	ps	
		all outputs same frequency			100	ps	
$t_{JIT(PER)}$	Period Jitter	output frequencies mixed			450	ps	
		all outputs same frequency			100	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter[9]	÷4 feedback divider RMS (1 σ)		40		ps	
		÷6 feedback divider RMS (1 σ)		50		ps	
		÷8 feedback divider RMS (1 σ)		60		ps	
		÷12 feedback divider RMS (1 σ)		80		ps	
BW	PLL closed loop bandwidth[10]	÷4 feedback		2.0 – 8.0		MHz	
		÷6 feedback		1.0 – 4.0		MHz	
		÷8 feedback		0.8 – 2.5		MHz	
		÷12 feedback		0.6 – 1.5		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. PLL mode requires $\overline{PLL\_EN}$=0 to enable the PLL and zero-delay operation.
3. The PLL may be unstable with a divide by 2 feedback ratio.
4. In PLL bypass mode, the MPC93R52 divides the input reference clock.
5. The input frequency f_{ref} on CCLK must match the VCO frequency range divided by the feedback divider ratio FB: $f_{ref} = f_{VCO} \div FB$.
6. See Table 7 and Table 8 for output divider configurations.
7. The MPC93R52 will operate with input rise and fall times up to 3.0 ns, but the AC characteristics, specifically $t_{(\varnothing)}$, can only be guaranteed if t_r/t_f are within the specified range.
8. See application section for part-to-part skew calculation.
9. See application section for jitter calculation for other confidence factors with 1 σ.
10. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Programming the MPC93R52

The MPC93R52 supports output clock frequencies from 16.67 to 240 MHz. Different feedback and output divider configurations can be used to achieve the desired input to output frequency relationship. The feedback frequency and divider should be used to situate the VCO in the frequency lock range between 200 and 480 MHz for stable and optimal operation. The FSELA, FSELB, FSELC pins select the desired output clock frequencies. Possible frequency ratios of the reference clock input to the outputs are 1:1, 1:2, 1:3, 3:2 as well as 2:3, 3:1, and 2:1. Table 7 and Table 8 illustrate the various output configurations and frequency ratios supported by the MPC93R52. See also Figure 3. MPC93R52 Default Configuration to Figure 6. MPC93R52 Zero Delay Buffer Configuration 2 for further reference. A ÷2 output divider cannot be used for feedback.

Table 7. MPC93R52 Example Configuration (F_RANGE = 0)

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 4[2]	50–120	0	0	0	fref (50-120 MHz)	fref (50-120 MHz)	fref * 2 (100-240 MHz)
		0	0	1	fref (50-120 MHz)	fref (50-120 MHz)	fref (50-120 MHz)
		1	0	0	fref * 2÷3 (33-80 MHz)	fref (50-120 MHz)	fref * 2 (100-240 MHz)
		1	0	1	fref * 2÷3 (33-80 MHz)	fref (50-120 MHz)	fref (50-120 MHz)
VCO ÷ 6[3]	33.3–80	1	0	0	fref (33-80 MHz)	fref * 3÷2 (50-120 MHz)	fref * 3 (100-240 MHz)
		1	0	1	fref (33-80 MHz)	fref * 3÷2 (50-120 MHz)	fref * 3÷2 (50-120 MHz)
		1	1	0	fref (33-80 MHz)	fref * 3 (100-240 MHz)	fref * 3 (100-240 MHz)
		1	1	1	fref (33-80 MHz)	fref * 3 (100-240 MHz)	fref * 3÷2 (50-120 MHz)

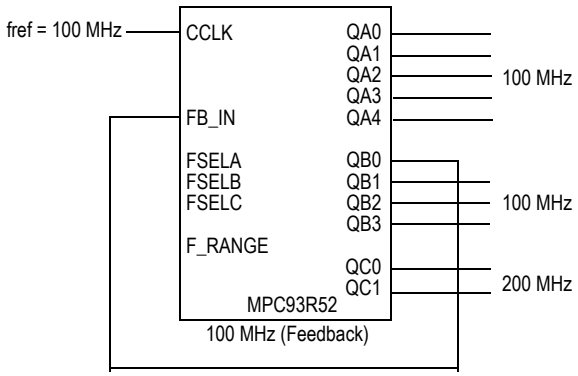
1. fref is the input clock reference frequency (CCLK)
2. QAx connected to FB_IN and FSELA=0
3. QAx connected to FB_IN and FSELA=1

Table 8. MPC93R52 Example Configurations (F_RANGE = 1)

PLL Feedback	fref[1] [MHz]	FSELA	FSELB	FSELC	QA[0:4]:fref ratio	QB[0:3]:fref ratio	QC[0:1]:fref ratio
VCO ÷ 8[2]	25-60	0	0	0	fref (25-60 MHz)	fref (25-60 MHz)	fref * 2 (50-120 MHz)
		0	0	1	fref (25-60 MHz)	fref (25-60 MHz)	fref (25-60 MHz)
		1	0	0	fref * 2÷3 (16-40 MHz)	fref (25-60 MHz)	fref * 2 (50-120 MHz)
		1	0	1	fref * 2÷3 (16-40 MHz)	fref (25-60 MHz)	fref (25-60 MHz)
VCO ÷ 12[3]	16.67–40	1	0	0	fref (16-40 MHz)	fref * 3÷2 (25-60 MHz)	fref * 3 (50-120 MHz)
		1	0	1	fref (16-40 MHz)	fref * 3÷2 (25-60 MHz)	fref * 3÷2 (25-60 MHz)
		1	1	0	fref (16-40 MHz)	fref * 3 (50-120 MHz)	fref * 3 (50-120 MHz)
		1	1	1	fref (16-40 MHz)	fref * 3 (50-120 MHz)	fref * 3÷2 (25-60 MHz)

1. fref is the input clock reference frequency (CCLK)
2. QAx connected to FB_IN and FSELA=0
3. QAx connected to FB_IN and FSELA=1

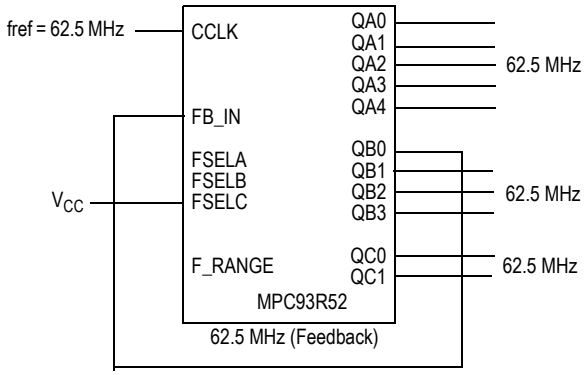
Example Configurations for the MPC93R52



MPC93R52 default configuration (feedback of QB0 = 100 MHz). All control pins are left open.

Frequency range	Min	Max
Input	50 MHz	120 MHz
QA outputs	50 MHz	12 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

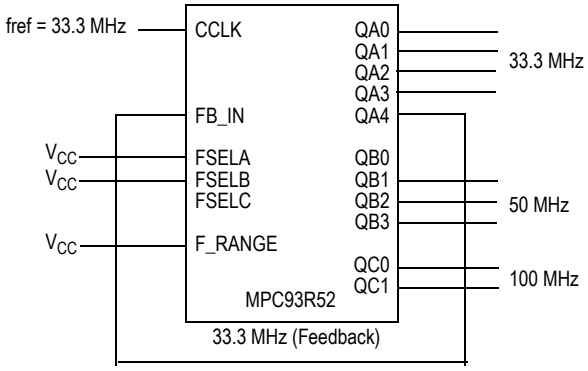
Figure 3. MPC93R52 Default Configuration



MPC93R52 zero-delay (feedback of QB0 = 62.5 MHz). All control pins are left open except FSELC = 1. All outputs are locked in frequency and phase to the input clock.

Frequency range	Min	Max
Input	50 MHz	120 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	50 MHz	120 MHz

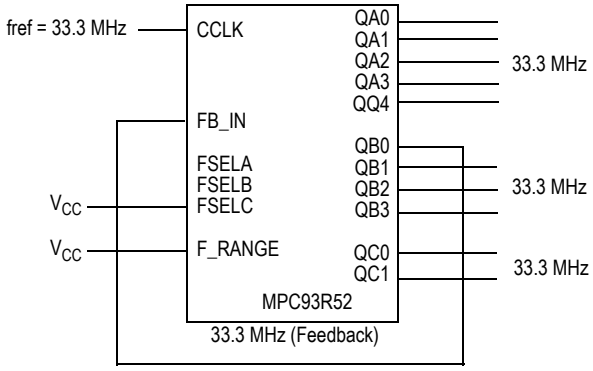
Figure 4. MPC93R52 Zero Delay Buffer Configuration



MPC93R52 configuration to multiply the reference frequency by 3, 3 ÷ 2 and 1. PLL feedback of QA4 = 33.3 MHz.

Frequency range	Min	Max
Input	25 MHz	60 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

Figure 5. MPC93R52 Default Configuration



MPC93R52 zero-delay (feedback of QB0 = 33.3 MHz). Equivalent to Table 2 except F_RANGE = 1 enabling a lower input and output clock frequency.

Frequency range	Min	Max
Input	25 MHz	60 MHz
QA outputs	25 MHz	60 MHz
QB outputs	25 MHz	60 MHz
QC outputs	25 MHz	60 MHz

Figure 6. MPC93R52 Zero Delay Buffer Configuration 2

Power Supply Filtering

The MPC93R52 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC93R52 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC93R52. Figure 7. VCCA Power Supply Filter illustrates a typical power supply filter scheme. The MPC93R52 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.98V must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 7. VCCA Power Supply Filter should have a resistance of 5-25Ω to meet the voltage drop criteria.

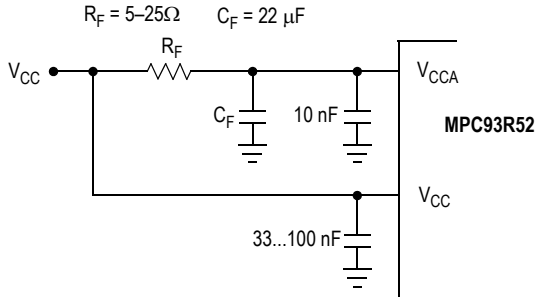


Figure 7. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7. VCCA Power Supply Filter, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC93R52 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC93R52 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC93R52. Designs using the MPC93R52 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC93R52 clock driver allows for its use as a zero delay buffer. One example configuration is to use a ÷4 output as a feedback to the PLL and configuring all other outputs to a divide-by-4 mode. The propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC93R52 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC93R52 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \bullet CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

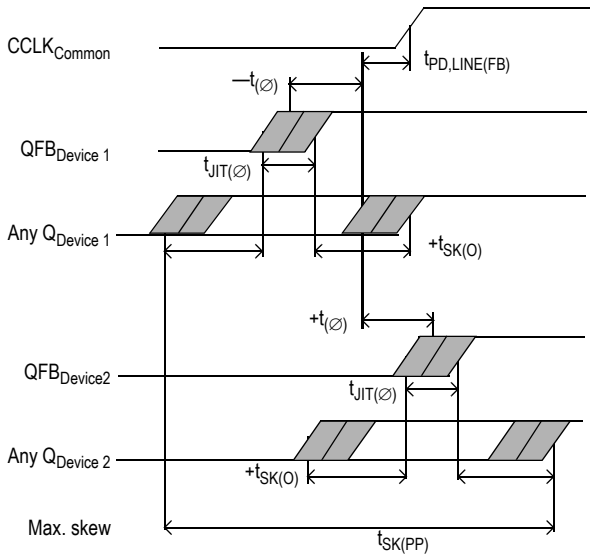


Figure 8. MPC93R52 Max. Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 9.

Table 9. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –445 ps to 395 ps relative to CCLK:

$t_{SK(PP)}$ = *[–200ps...150ps] + [-200ps...200ps] + [(15ps • –3)...(15ps • 3)] +* $t_{PD,\ LINE(FB)}$

$t_{SK(PP)}$ = *[–445ps...395ps]* + $t_{PD,\ LINE(FB)}$

Due to the frequency dependence of the I/O jitter, Figure 9. Max. I/O Jitter versus Frequency, can be used for a more precise timing performance analysis.

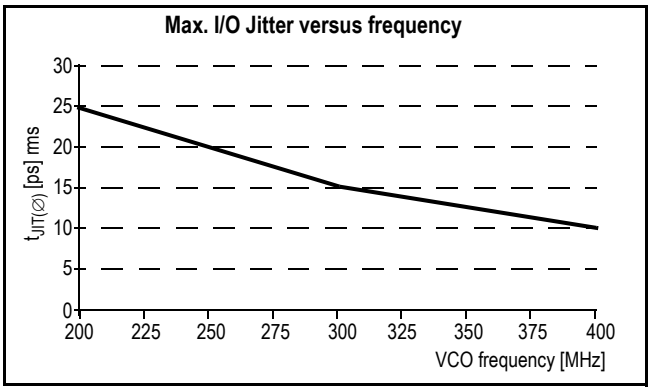


Figure 9. Max. I/O Jitter versus Frequency

Driving Transmission Lines

The MPC93R52 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC93R52 clock driver. For the series terminated case however, there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 10. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC93R52 clock driver is effectively doubled due to its capability to drive multiple lines.

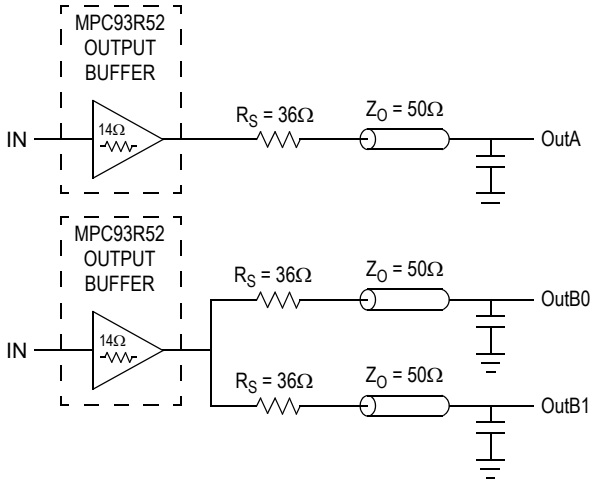


Figure 10. Single versus Dual Transmission Lines

The waveform plots in Figure 11. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC93R52 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC93R52. The output waveform in Figure 11. Single versus Dual Waveforms shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S\ (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0\ (25 \div (18+17+25))$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

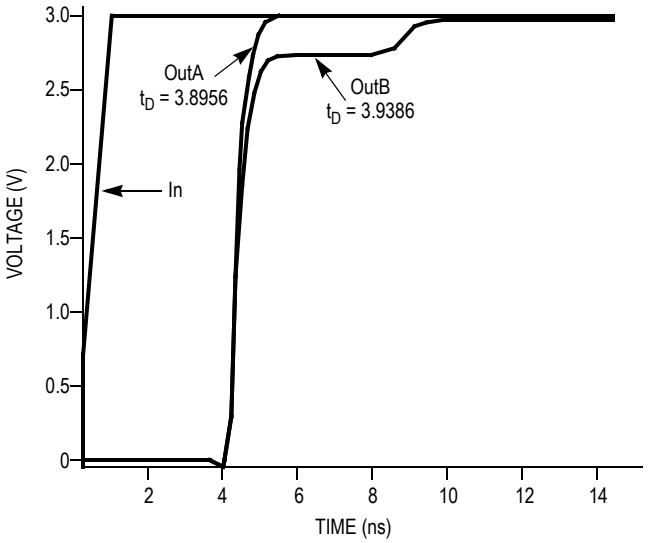


Figure 11. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 12. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

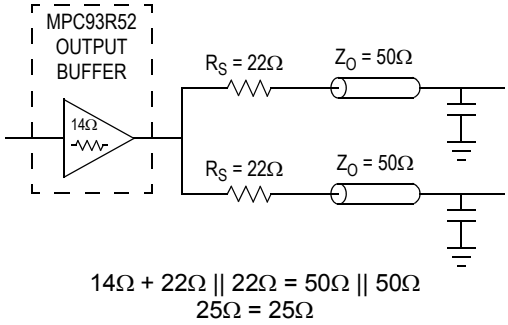


Figure 12. Optimized Dual Line Termination

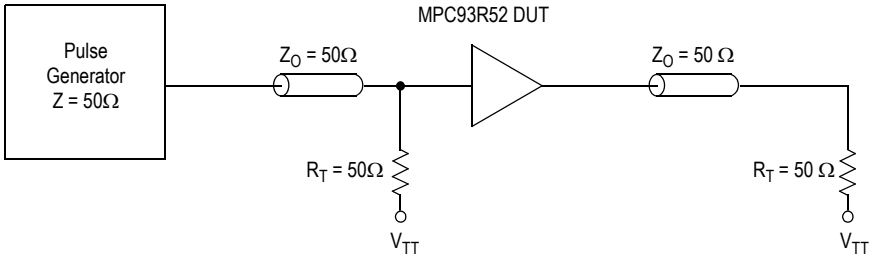
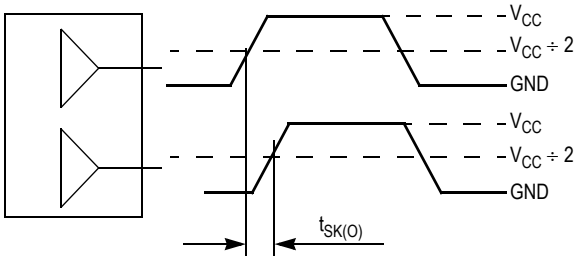


Figure 13. CCLK MPC93R52 AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 14. Output-to-Output Skew $t_{SK(O)}$

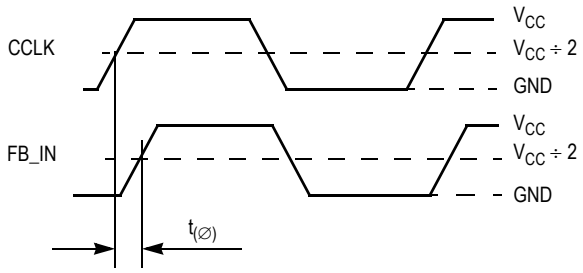
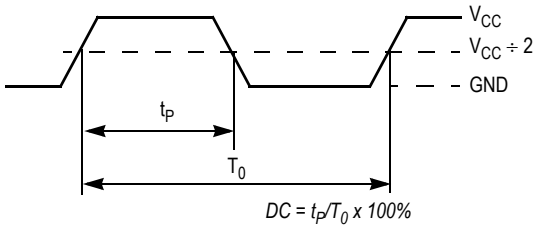
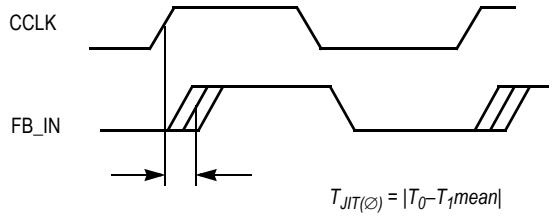


Figure 15. Propagation Delay ($t_{(\varnothing)}$, static phase offset) Test Reference



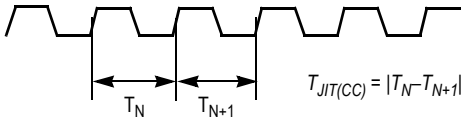
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)



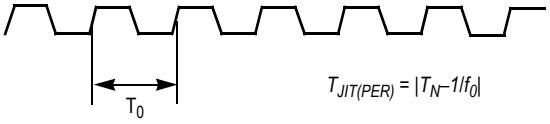
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 17. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 18. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 19. Period Jitter

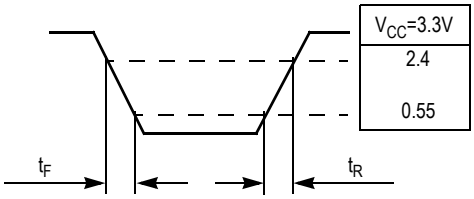


Figure 20. Output Transition Time Test Reference

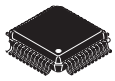
Order number: MPC9600
Rev 3, 08/2004

Product Preview

Low Voltage 2.5 V and 3.3 V CMOS PLL Clock Driver

MPC9600

**3.3 V OR 2.5 V
LOW VOLTAGE CMOS
PLL CLOCK DRIVER**



FA SUFFIX
48-LEAD LQFP PACKAGE
CASE 932-03

The MPC9600 is a low voltage 2.5 V or 3.3 V compatible, 1:21 PLL based clock driver and fanout buffer. With output frequencies up to 200 MHz and output skews of 150 ps, the device meets the needs of the most demanding clock tree applications.

Features

- Multiplication of input frequency by 2, 3, 4, and 6
- Distribution of output frequency to 21 outputs organized in three output banks: QA0-QA6, QB0-QB6, QC0-QC6, each fully selectable
- Fully integrated PLL
- Selectable output frequency range is 50 to 100 MHz and 100 to 200 MHz
- Selectable input frequency range is 16.67 to 33 MHz and 25 to 50 MHz
- LVCMOS outputs
- Outputs disable to high impedance (except QFB)
- LVCMOS or LVPECL reference clock options
- 48-lead QFP packaging
- 48-lead Pb-free Package Available
- ± 50 ps cycle-to-cycle jitter
- 150 ps maximum output-to-output skew
- 200 ps maximum static phase offset window

The MPC9600 is a fully LVCMOS 2.5 V or 3.3 V compatible PLL clock driver. The MPC9600 has the capability to generate clock signals of 50 to 200 MHz from clock sources of 16.67 to 50 MHz. The internal PLL is optimized for this frequency range and does not require external loop filter components. QFB provides an output for the external feedback path to the feedback input FB_IN. The QFB divider ratio is configurable and determines the PLL frequency multiplication factor when QFB is directly connected to FB_IN. The MPC9600 is optimized for minimizing the propagation delay between the clock input and FB_IN.

Three output banks of 7 outputs each bank can be individually configured to divide the VCO frequency by 2 or by 4. Combining the feedback and output divider ratios, the MPC9600 is capable to multiply the input frequency by 2, 3, 4, and 6.

The reference clock is selectable either LVPECL or LVCMOS. The LVPECL reference clock feature allows the designer to use LVPECL fanout buffers for the inner branches of the clock distribution tree. All control inputs accept LVCMOS compatible levels. The outputs provide low impedance LVCMOS outputs capable of driving parallel terminated 50 Ω transmission to $V_{TT} = V_{CC}/2$. For series terminated lines the MPC9600 can drive two lines per output giving the device an effective total fanout of 1:42. With guaranteed maximum output-to-output skew of 150 ps, the MPC9600 PLL clock driver meets the synchronization requirements of the most demanding systems.

The V_{CCA} analog power pin doubles as a PLL bypass select line for test purpose. When the V_{CCA} is driven to GND the reference clock will bypass the PLL.

The device is packaged in a 48-lead LQFP package to provide optimum combination of board density and performance.

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

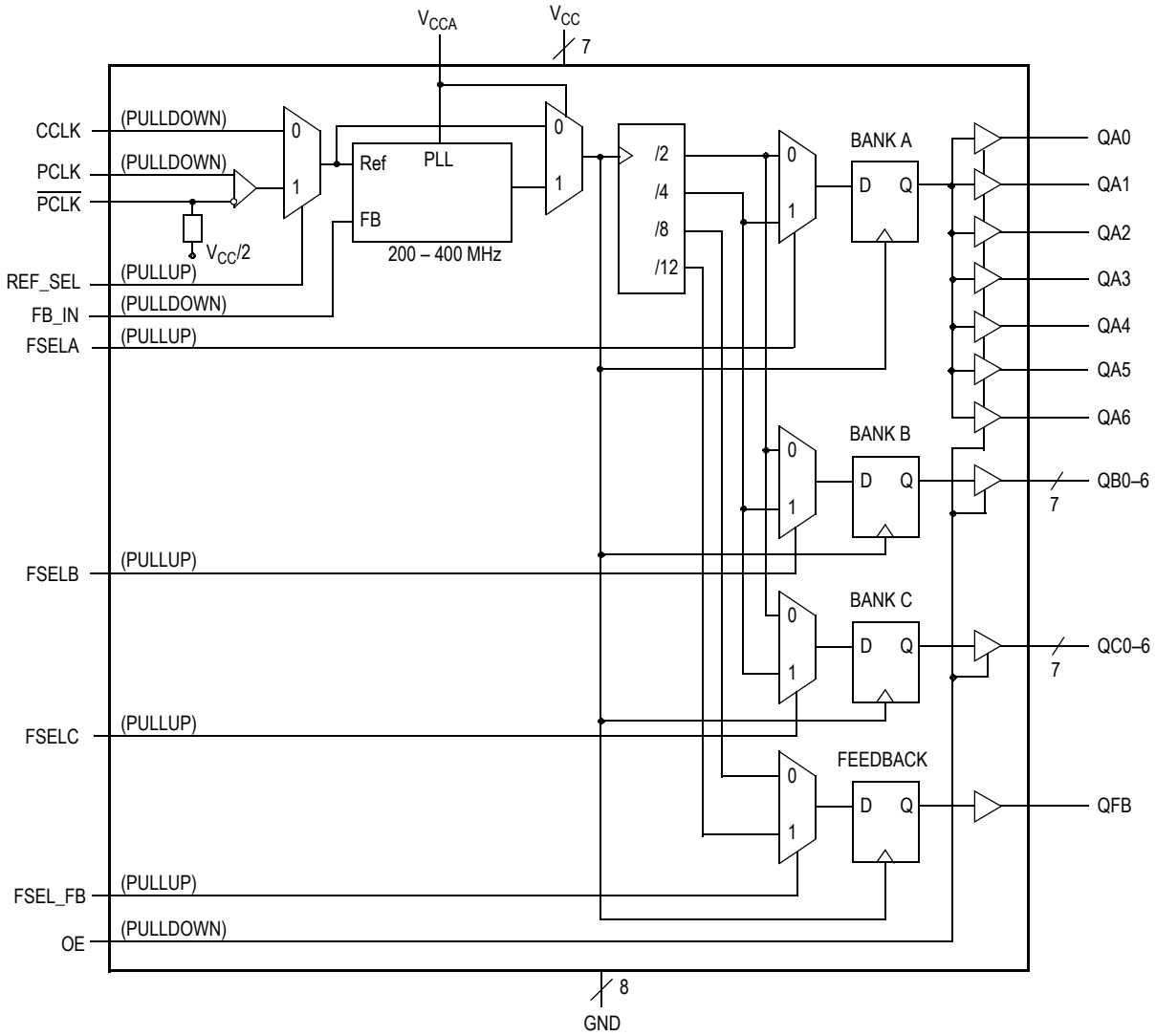


Figure 1. MPC9600 Logic Diagram

Table 1. Pin Configuration – 48 LQFP

Pin	I/O	Type	Description
PCLK, $\overline{\text{PCLK}}$	Input	PECL	Differential reference clock frequency input
CCLK	Input	LVCMOS	Reference clock input
FB_IN	Input	LVCMOS	PLL feedback clock input
QAn	Output	LVCMOS	Bank A outputs
QBn	Output	LVCMOS	Bank B outputs
QCn	Output	LVCMOS	Bank C outputs
QFB	Output	LVCMOS	Differential feedback output
REF_SEL	Input	LVCMOS	Reference clock input select
FSELA	Input	LVCMOS	Selection of bank A output frequency
FSELB	Input	LVCMOS	Selection of bank B output frequency
FSELC	Input	LVCMOS	Selection of bank C output frequency
FSEL_FB	Input	LVCMOS	Selection of feedback frequency
OE	Input	LVCMOS	Output enable
V_{CCA}		Power supply	Analog power supply and PLL bypass. An external V_{CC} filter is recommended for V_{CCA}
V_{CC}		Power supply	Core power supply
GND		Ground	Ground

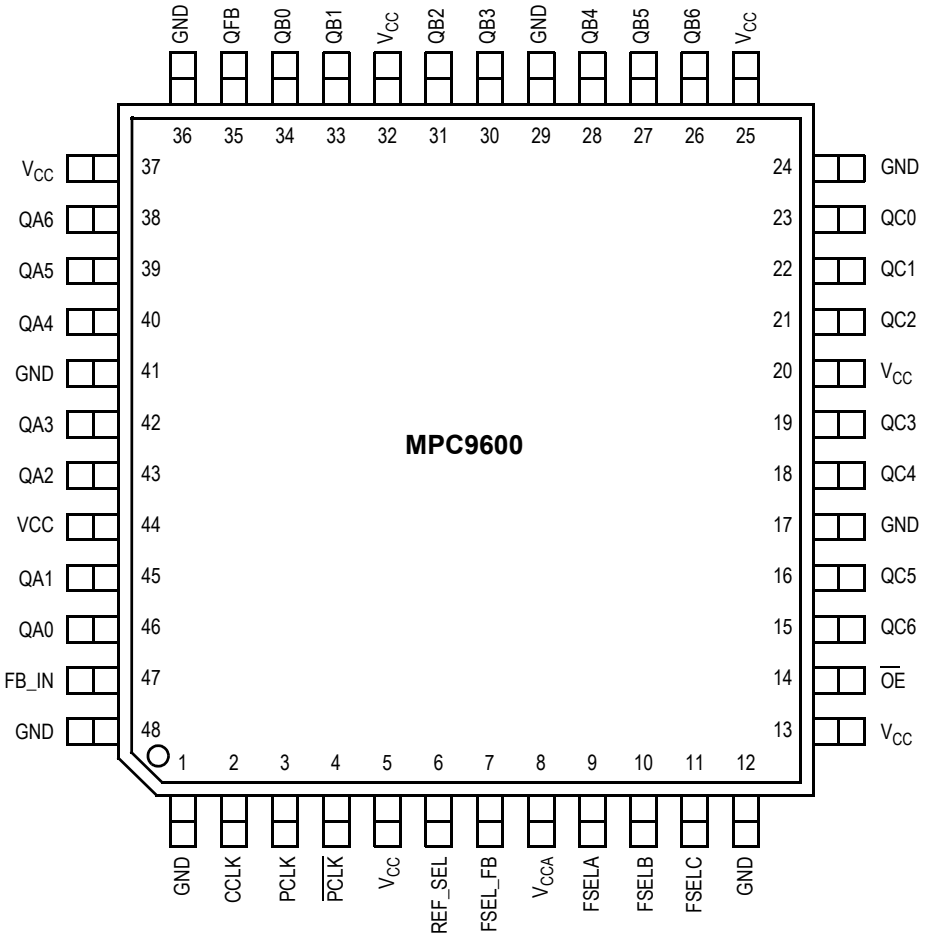


Figure 2. 48-Lead Package Pinout (Top View)

Table 2. Function Table (Controls)

Control Pin	0	1
REF_SEL	CCLK	PCLK
V_{CCA}	PLL Bypass[1]	PLL Power
OE	Outputs Enabled	Outputs Disabled (except QFB)
FSELA	Output Bank A at VCO/2	Output Bank A at VCO/4
FSELB	Output Bank B at VCO/2	Output Bank B at VCO/4
FSELC	Output Bank C at VCO/2	Output Bank C at VCO/4
FSEL_FB	Feedback Output at VCO/8	Feedback Output at VCO/12

1. V_{CCA} = GND, PLL off and bypassed for static test and diagnosis

Table 3. Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	DC Input Current		±20	mA
I_{OUT}	DC Output Current		±50	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	400			V	
HBM	ESD Protection (Human Body Model)	4000			V	
CDM	ESD Protection (Charged Device Model)	1500			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = – 40°C to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage				0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage (DC)	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range (DC)	PCLK, $\overline{PCLK}$	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA[2]
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24mA I_{OL} = 12mA
Z_{OUT}	Output Impedance			14 – 17		W	
I_{IN}	Input Leakage Current				± 150	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current			2.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current				1.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9600 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

Table 6. DC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = – 40°C to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage				0.7	V	LVCMOS
V_{PP}	Peak-to-Peak input voltage (DC)	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range (DC)	PCLK, $\overline{PCLK}$	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage		1.8			V	I_{OH} = –15 mA[2]
V_{OL}	Output Low Voltage				0.6	V	I_{OL} = 15 mA
Z_{OUT}	Output Impedance			17 – 20		W	
I_{IN}	Input Leakage Current				± 150	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current			3.0	5.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current				1.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9600 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.

Table 7. AC Characteristics – 48 LQFP (V_{CC} = 3.3 V ± 5% or V_{CC} = 2.5 V ± 5%, T_A = –40°C to +85°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency					
	÷ 8 feedback (FSEL_FB = 0)	25		50	MHz	PLL locked
	÷ 12 feedback (FSEL_FB = 1)	16.67		33	MHz	PLL locked
	Static test mode (V_{CCA} = GND)	0		500	MHz	V_{CCA} = GND
f_{VCO}	VCO Frequency	200		400	MHz	
f_{MAX}	Maximum Output Frequency					
	÷ 2 outputs (FSELx = 0)	100		200	MHz	PLL locked
	÷ 4 outputs (FSELx = 1)	50		100	MHz	PLL locked
f_{refDC}	Reference Input Duty Cycle	25		75	%	
V_{PP}	Peak-to-Peak Input Voltage PCLK, $\overline{PCLK}$	500		1000	mV	LVPECL
V_{CMR}[2]	Common Mode Range					
	PCLK, $\overline{PCLK}$ (V_{CC} = 3.3 V ± 5%)	1.2		V_{CC} –0.8	V	LVPECL
	PCLK, $\overline{PCLK}$ (V_{CC} = 2.5 V ± 5%)	1.2		V_{CC} –0.6	V	LVPECL
t_r, t_f	CCLK Input Rise/Fall Time			1.0	ns	see Figure 11
$t_{(\varnothing)}$	Propagation Delay (static phase offset)					
	CCLK to FB_IN	–60	+40	+140	ps	PLL locked
	PECL_CLK to FB_IN	+30	+130	+230	ps	PLL locked
$t_{sk(o)}$	Output-to-Output Skew					
	all outputs, single frequency		70	150	ps	Measured at coincident rising edge
	all outputs, multiple frequency		70	150	ps	
	within QAx output bank		30	75	ps	
	within QBx outputs		40	125	ps	
	within QCx outputs		30	75	ps	
DC	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	see Figure 11
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, ZH}$	Output Enable Time			10	ns	
BW	PLL Closed Loop Bandwidth					–3 dB point of PLL transfer characteristic
	÷ 8 feedback (FSEL_FB=0)		1.0 – 10		MHz	
	÷ 12 feedback (FSEL_FB=1)		0.6 – 4.0		MHz	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter[3]					Refer to application section for other configurations
	All outputs in ÷ 2 configuration		40	130	ps	
	All outputs in ÷ 4 configuration		40	180	ps	
$t_{JIT(PER)}$	Period Jitter[3]					Refer to application section for other configurations
	All outputs in ÷ 2 configuration		25	70	ps	
	All outputs in ÷ 4 configuration		20	100	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter (1 σ) V_{CC} = 3.3 V			17[4]	ps	RMS value at f_{VCO} = 400 MHz
	V_{CC} = 2.5 V			15[3]	ps	
t_{LOCK}	Maximum PLL Lock Time			5.0	ms	

1. AC characteristics are applicable over the entire ambient temperature and supply voltage range and are production tested. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
3. Cycle-to-cycle and period jitter depends on output divider configuration.
4. See applications section for max I/O phase jitter versus frequency.

APPLICATIONS INFORMATION

Programming the MPC9600

The MPC9600 clock driver outputs can be configured into several divider modes. Additionally the external feedback of the device allows for flexibility in establishing various input to output frequency relationships. The selectable feedback divider of the three output groups allows the user to configure the device for 1:2, 1:3, 1:4 and 1:6 input:output frequency ratios. The use of even dividers ensure that the output duty cycle is always 50%. Table 8 illustrates the various output configurations, the table describes the outputs using the input clock frequency CLK as a reference.

The feedback divider division settings establish the output relationship, in addition, it must be ensured that the VCO will be stable given the frequency of the outputs desired. The feedback frequency should be used to situate the VCO into a frequency range in which the PLL will be stable. The design of the PLL supports output frequencies from 50 MHz to 200 MHz while the VCO frequency range is specified from 200 MHz to 400 MHz and should not be exceeded for stable operation.

Table 8. Output Frequency Relationship[1] for QFB Connected to FB_IN

Configuration Inputs				Input Frequency Range CLK [MHz]	Output Frequency Ratio and Range		
FSEL_FB	FSELA	FSELB	FSELC		Ratio, QAx [MHz]	Ratio, QBx [MHz]	Ratio, QCx [MHz]
0	0	0	0	25.0–50.0	4•CLK (100–200)	4•CLK (100–200)	4•CLK (100–200)
0	0	0	1		4•CLK (100–200)	4•CLK (100–200)	2•CLK (50.0–100)
0	0	1	0		4•CLK (100–200)	2•CLK (50.0–100)	4•CLK (100–200)
0	0	1	1		4•CLK (100–200)	2•CLK (50.0–100)	2•CLK (50.0–100)
0	1	0	0		2•CLK (50.0–100)	4•CLK (100–200)	4•CLK (100–200)
0	1	0	1		2•CLK (50.0–100)	4•CLK (100–200)	2•CLK (50.0–100)
0	1	1	0		2•CLK (50.0–100)	2•CLK (50.0–100)	4•CLK (100–200)
0	1	1	1		2•CLK (50.0–100)	2•CLK (50.0–100)	2•CLK (50.0–100)
1	0	0	0	16.67–33.33	6•CLK (100–200)	6•CLK (100–200)	6•CLK (100–200)
1	0	0	1		6•CLK (100–200)	6•CLK (100–200)	3•CLK (50.0–100)
1	0	1	0		6•CLK (100–200)	3•CLK (50.0–100)	6•CLK (100–200)
1	0	1	1		6•CLK (100–200)	3•CLK (50.0–100)	3•CLK (50.0–100)
1	1	0	0		3•CLK (50.0–100)	6•CLK (100–200)	6•CLK (100–200)
1	1	0	1		3•CLK (50.0–100)	6•CLK (100–200)	3•CLK (50.0–100)
1	1	1	0		3•CLK (50.0–100)	3•CLK (50.0–100)	6•CLK (100–200)
1	1	1	1		3•CLK (50.0–100)	3•CLK (50.0–100)	3•CLK (50.0–100)

1. Output frequency relationship with respect to input reference frequency CLK. The VCO frequency range is always 200–400.

Table 9. Typical and Maximum Period Jitter Specification

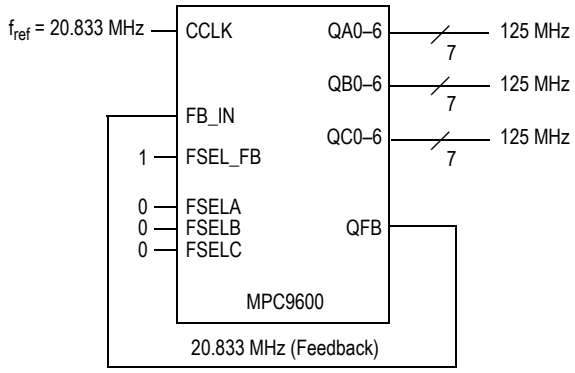
Device Configuration	QA0 to QA6		QB0 to QB6		QC0 to QC6	
	Typ	Max	Typ	Max	Typ	Max
All output banks in ÷ 2 or ÷ 4 divider configuration[1] ÷ 2 (FSELA = 0 and FESLB = 0 and FSELC = 0) ÷ 4 (FSELA = 1 and FESLB = 1 and FSELC = 1)	 25 20	 50 70	 50 50	 70 100	 25 20	 50 70
Mixed ÷ 2/÷ 4 divider configurations[2] for output banks in ÷ 2 divider configurations for output banks in ÷ 4 divider configurations	 80 25	 130 70	 100 60	 150 100	 80 25	 130 70

1. In this configuration, all MPC9600 outputs generate the same clock frequency. See Figure 3 for an example configuration.
2. Multiple frequency generation. Jitter data are specified for each output divider separately. See Figure 7 for an example.

Table 10. Typical and Maximum Cycle-to-Cycle Jitter Specification

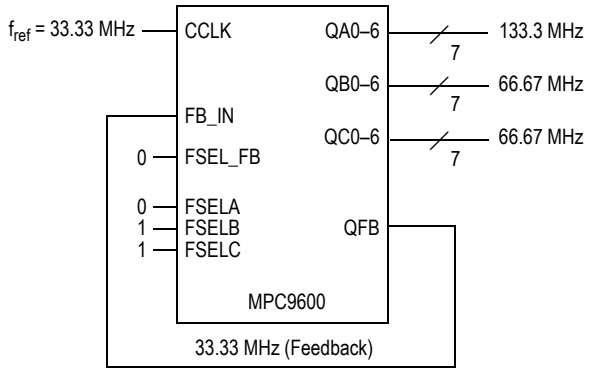
Device Configuration	QA0 to QA6		QB0 to QB6		QC0 to QC6	
	Typ	Max	Typ	Max	Typ	Max
All output banks in ÷ 2 or ÷ 4 divider configuration[1] ÷ 2 (FSELA = 0 and FESLB = 0 and FSELC = 0) ÷ 4 (FSELA = 1 and FESLB = 1 and FSELC = 1)	 40 40	 90 110	 80 120	 130 180	 40 40	 90 110
Mixed ÷2/÷ 4 divider configurations[2] for output banks in ÷ 2 divider configurations for output banks in ÷ 4 divider configurations	 150 30	 250 110	 200 120	 280 180	 150 30	 250 110

1. In this configuration, all MPC9600 outputs generate the same clock frequency.
2. Multiple frequency generation. Jitter data are specified for each output divider separately.



Frequency Range	Min	Max
Input	16.67 MHz	33.33 MHz
QA outputs	100 MHz	200 MHz
QB outputs	100 MHz	200 MHz
QC outputs	100 MHz	200 MHz

Figure 3. Configuration for 126 MHz Clocks



Frequency Range	Min	Max
Input	25 MHz	50 MHz
QA outputs	100 MHz	200 MHz
QB outputs	100 MHz	200 MHz
QC outputs	100 MHz	200 MHz

Figure 4. Configuration for 133.3/66.67 MHz Clocks

Power Supply Filtering

The MPC9600 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9600 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9600. Figure 5 illustrates a typical power supply filter scheme. The MPC9600 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 2.325 V (V_{CC} = 3.3 V or V_{CC} = 2.5 V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 5, must have a resistance of 9–10 Ω (V_{CC} = 2.5 V) to meet the voltage drop criteria.

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 5, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

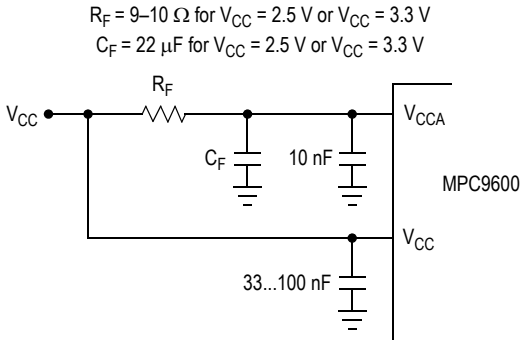


Figure 5. V_{CCA} Power Supply Filter

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9600 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9600 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9600. For these applications the MPC9600 offers a differential LVPECL clock input pair as a PLL reference. This allows for the use of differential LVPECL primary clock distribution devices such as the Motorola MC100ES6111 or MC100ES6226, taking advantage of its superior low-skew performance. Clock trees using LVPECL for clock distribution and the MPC9600 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers.

The external feedback option of the MPC9600 PLL allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge and virtually eliminates the propagation delay through the device.

The remaining insertion delay (skew error) of the MPC9600 in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset (SPO or $t_{(\varnothing)}$), I/O jitter ($t_{JIT(\varnothing)}$, phase or long-term jitter), feedback path delay and the output-to-output skew ($t_{SK(O)}$) relative to the feedback output.

Features Calculation of Part-to-Part Skew

The MPC9600 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs (CCLK or PCLK) of two or more MPC9600 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \bullet CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

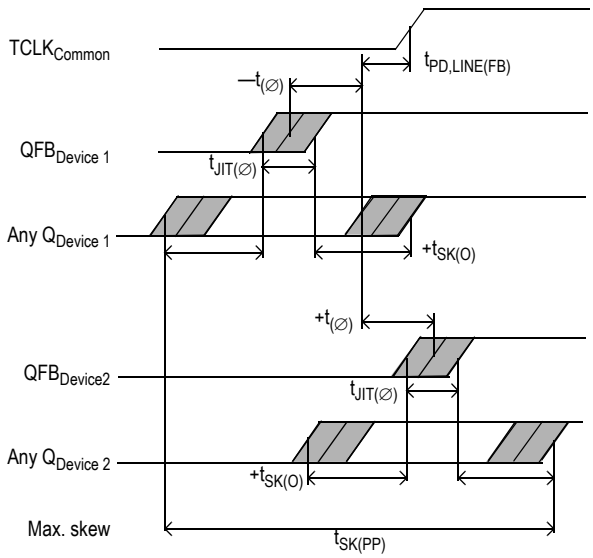


Figure 6. MPC9600 Maximum Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 11.

Table 11. Confidence Factor CF

CF	Probability of Clock Edge Within the Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –261 ps to 341 ps relative to CCLK (V_{CC} = 3.3 V and f_{VCO} = 200 MHz):

$$t_{SK(PP)} = [–60\ ps...140\ ps] + [–150\ ps...150\ ps] + [(17\ ps\ @\ –3)...(17\ ps\ @\ 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–261\ ps...341\ ps] + t_{PD,\ LINE(FB)}$$

Above equation uses the maximum I/O jitter number shown in the AC characteristic table for V_{CC} = 3.3 V (17 ps RMS). I/O jitter is frequency dependant with a maximum at the lowest VCO frequency (200 MHz for the MPC9600). Applications using a higher VCO frequency exhibit less I/O jitter than the AC characteristic limit. The I/O jitter characteristics in Figure 7 can be used to derive a smaller I/O jitter number at the specific VCO frequency, resulting in tighter timing limits in zero-delay mode and for part-to-part skew $t_{SK(PP)}$.

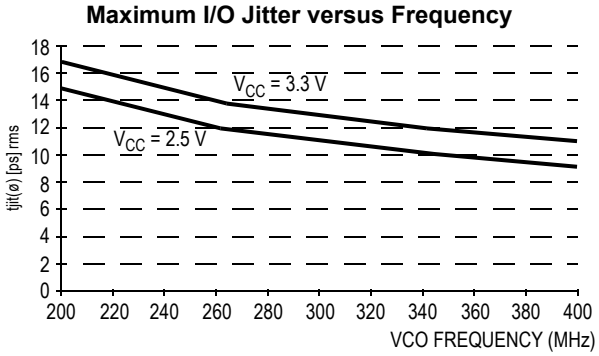


Figure 7. I/O Jitter versus VCO Frequency for V_{CC} = 2.5 V and V_{CC} = 3.3 V

Driving Transmission Lines

The MPC9600 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC} ÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9600 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 8 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9600 clock driver is effectively doubled due to its capability to drive multiple lines.

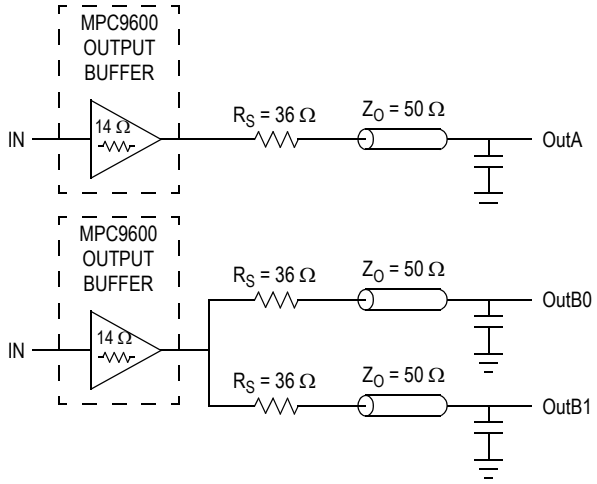


Figure 8. Single versus Dual Transmission Lines

The waveform plots in Figure 9 shows the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9600 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9600. The output waveform in Figure 9 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S\ (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega\ ||\ 50\ \Omega$$
$$R_S = 36\ \Omega\ ||\ 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18 + 17 + 25)$$
$$= 1.31\ V$$

At the load end the voltage will double due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

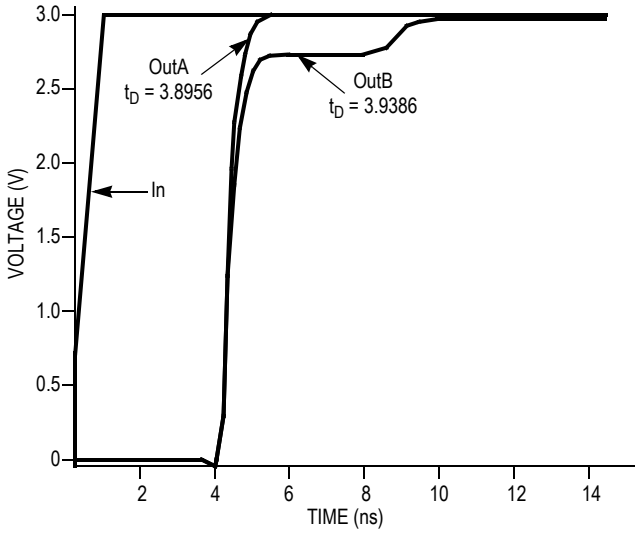
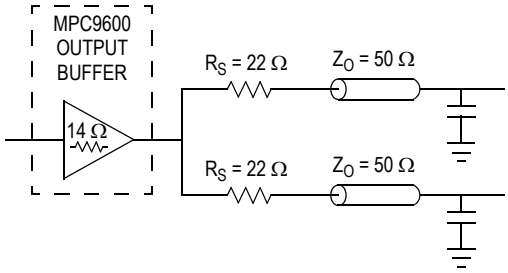


Figure 9. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 10 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



14 Ω + 22 Ω || 22 Ω = 50 Ω || 50 Ω
25 Ω = 25 Ω

Figure 10. Optimized Dual Line Termination

The following figures illustrate the measurement reference for the MPC9600 clock driver circuit.

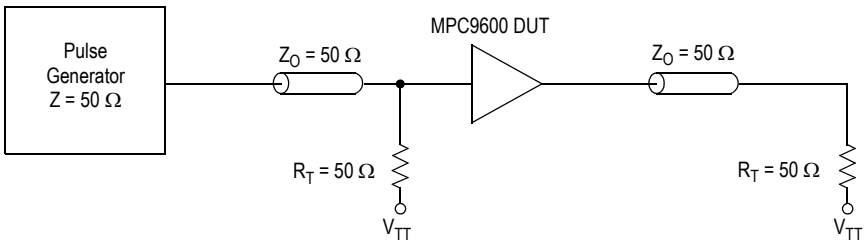


Figure 11. CCLK MPC9600 AC Test Reference

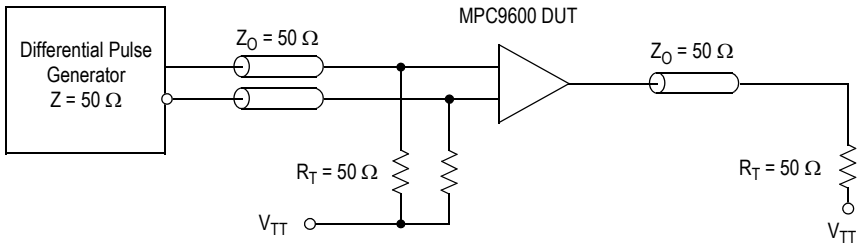


Figure 12. PCLK MPC9600 AC Test Reference

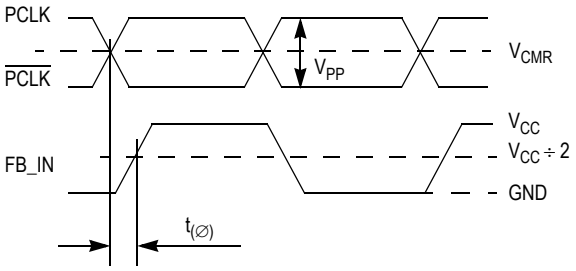


Figure 14. Propagation Delay ($t_{Ø}$, status phase offset) Test Reference

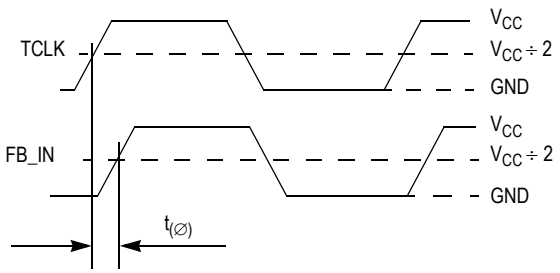
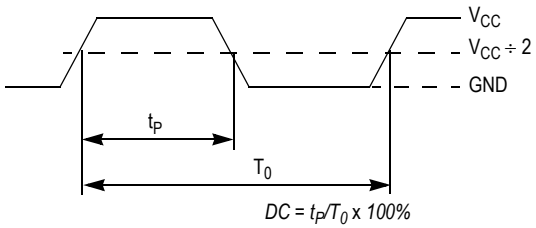
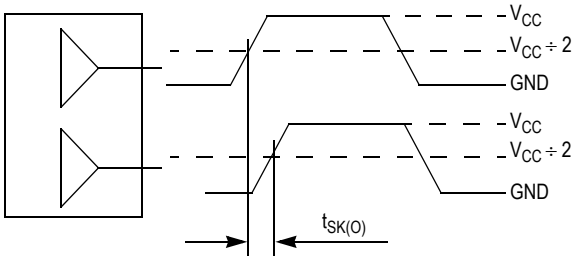


Figure 15. Propagation Delay ($t_{Ø}$) Test Reference



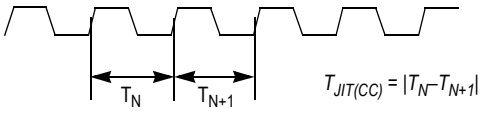
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)



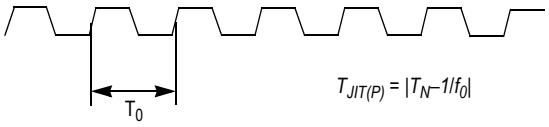
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 17. Output-to-Output Skew $t_{SK(O)}$



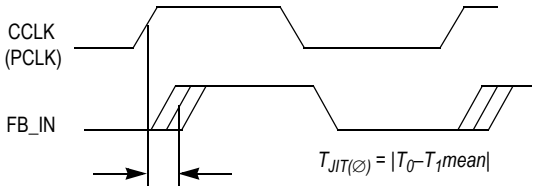
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 18. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 19. Period Jitter



The deviation in T_0 for a controlled edge with respect to a T_0 mean in a random sample of cycles

Figure 20. I/O Jitter

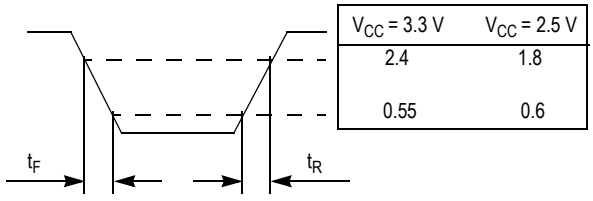


Figure 21. Transition Time Test Reference

3.3V 1:12 LVCMOS PLL Clock Generator

MPC9772

3.3V 1:12 LVCMOS PLL CLOCK GENERATOR

FA SUFFIX
52-LEAD LQFP PACKAGE
CASE 848D-03

The MPC9772 is a 3.3V compatible, 1:12 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance networking, computing and telecom applications. With output frequencies up to 240 MHz and output skews less than 250 ps the device meets the needs of the most demanding clock applications.

Features

- 1:12 PLL based low-voltage clock generator
- 3.3V power supply
- Internal power-on reset
- Generates clock signals up to 240 MHz
- Maximum output skew of 250 ps
- On-chip crystal oscillator clock reference
- Two LVCMOS PLL reference clock inputs
- External PLL feedback supports zero-delay capability
- Various feedback and output dividers (see application section)
- Supports up to three individual generated output clock frequencies
- Synchronous output clock stop circuitry for each individual output for power down support
- Drives up to 24 clock lines
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC972
- 52-lead Pb-free Package Available

Functional Description

The MPC9772 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9772 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC9772 features an extensive level of frequency programmability between the 12 outputs as well as the output to input relationships, for instance 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 5:4, 5:6, 6:1, 8:1, and 8:3.

The QSYNC output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies. This allows for very flexible programming of the input reference versus output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non-binary factor. The MPC9772 also supports the 180° phase shift of one of its output banks with respect to the other output banks. The QSYNC outputs reflects the phase relationship between the QA and QC outputs and can be used for the generation of system baseline timing signals.

The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be individually disabled (stopped in logic low state) by programming the serial CLOCK_STOP interface of the MPC9772. The MPC9772 has an internal power-on reset.

The MPC9772 is fully 3.3V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9772 outputs can drive one or two traces giving the devices an effective fanout of 1:24. The device is pin and function compatible to the MPC972 and is packaged in a 52-lead LQFP package.

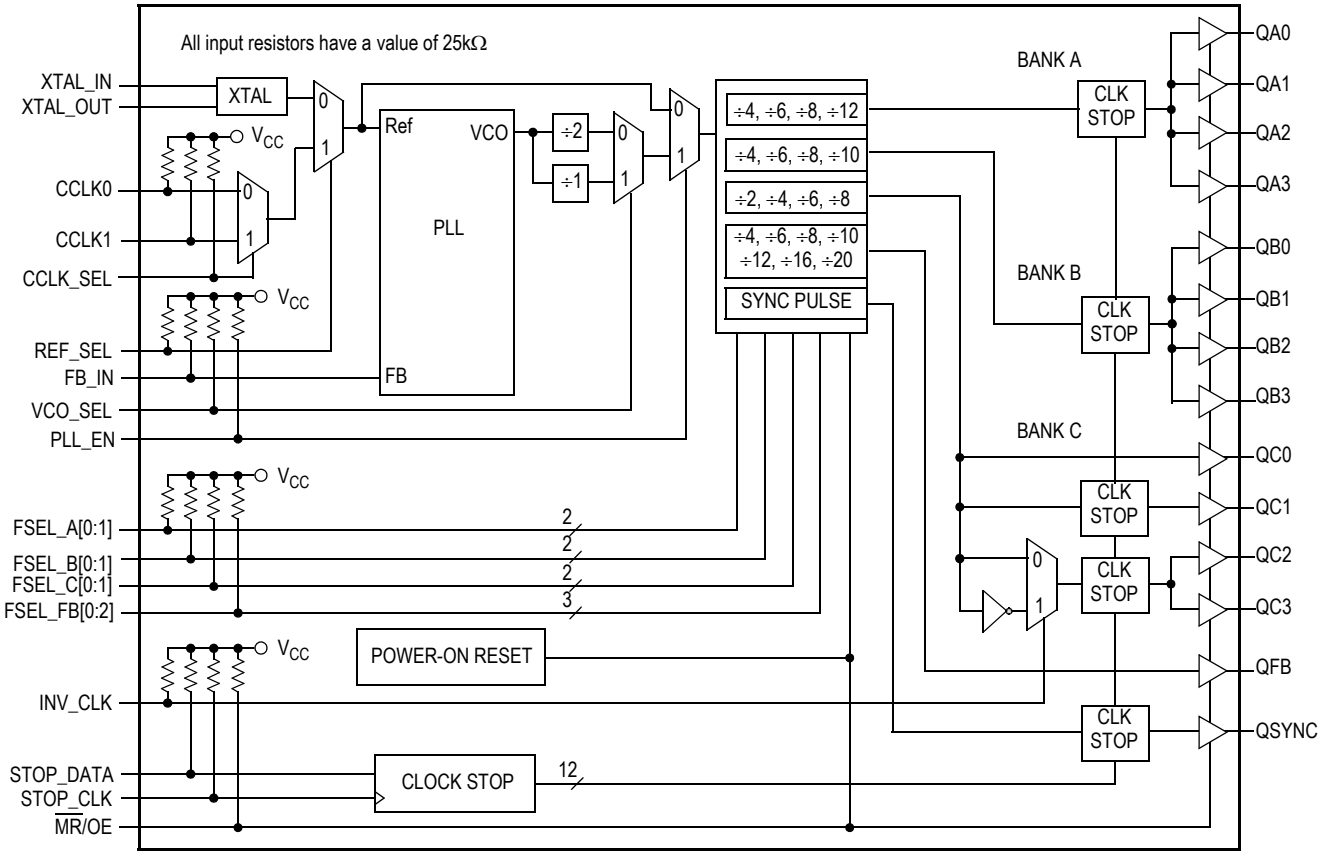


Figure 1. MPC9772 Logic Diagram

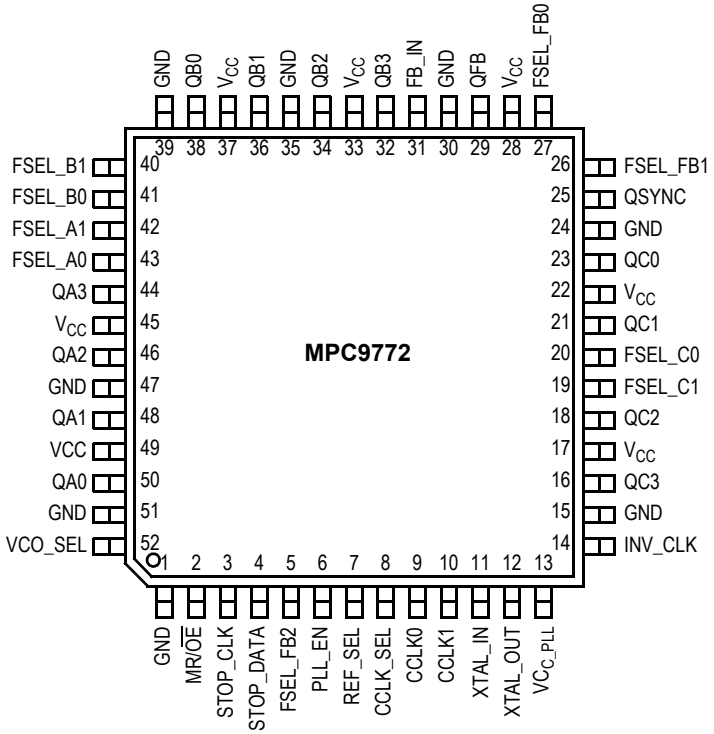


Figure 2. MPC9772 52-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK0	Input	LVCMOS	PLL reference clock
CCLK1	Input	LVCMOS	Alternative PLL reference clock
XTAL_IN, XTAL_OUT		Analog	Crystal oscillator interface
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to an QFB
CCLK_SEL	Input	LVCMOS	LVCMOS clock reference select
REF_SEL	Input	LVCMOS	LVCMOS/PECL reference clock select
VCO_SEL	Input	LVCMOS	VCO operating frequency select
PLL_EN	Input	LVCMOS	PLL enable/PLL bypass mode select
$\overline{MR}$/OE	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
FSEL_A[0:1]	Input	LVCMOS	Frequency divider select for bank A outputs
FSEL_B[0:1]	Input	LVCMOS	Frequency divider select for bank B outputs
FSEL_C[0:1]	Input	LVCMOS	Frequency divider select for bank C outputs
FSEL_FB[0:2]	Input	LVCMOS	Frequency divider select for the QFB output
INV_CLK	Input	LVCMOS	Clock phase selection for outputs QC2 and QC3
STOP_CLK	Input	LVCMOS	Clock input for clock stop circuitry
STOP_DATA	Input	LVCMOS	Configuration data input for clock stop circuitry
QA[0-3]	Output	LVCMOS	Clock outputs (Bank A)
QB[0-3]	Output	LVCMOS	Clock outputs (Bank B)
QC[0-3]	Output	LVCMOS	Clock outputs (Bank C)
QFB	Output	LVCMOS	PLL feedback output. Connect to FB_IN.
QSYNC	Output	LVCMOS	Synchronization pulse output
GND	Supply	Ground	Negative power supply
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table (Configuration Controls)

Control	Default	0	1
REF_SEL	1	Selects CCLKx as the PLL reference clock	Selects the crystal oscillator as the PLL reference clock
CCLK_SEL	1	Selects CCLK0	Selects CCLK1
VCO_SEL	1	Selects VCO÷2. The VCO frequency is scaled by a factor of 2 (low VCO frequency range).	Selects VCO÷1. (high VCO frequency range)
PLL_EN	1	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9772 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
INV_CLK	1	QC2 and QC3 are in phase with QC0 and QC1	QC2 and QC3 are inverted (180° phase shift) with respect to QC0 and QC1
$\overline{MR}$/OE	1	Outputs disabled (high-impedance state) and device is reset. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC9772 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). The device is reset by the internal power-on reset (POR) circuitry during power-up.	Outputs enabled (active)

VCO_SEL, FSEL_A[0:1], FSEL_B[0:1], FSEL_C[0:1], FSEL_FB[0:2] control the operating PLL frequency range and input/output frequency ratios. See Table 3 to Table 6 and the APPLICATIONS INFORMATION for supported frequency ranges and output to input frequency ratios.

Table 3. Output Divider Bank A (N_A)

VCO_SEL	FSEL_A1	FSEL_A0	QA[0:3]
0	0	0	VCO÷8
0	0	1	VCO÷12
0	1	0	VCO÷16
0	1	1	VCO÷24
1	0	0	VCO÷4
1	0	1	VCO÷6
1	1	0	VCO÷8
1	1	1	VCO÷12

Table 4. Output Divider Bank B (N_B)

VCO_SEL	FSEL_B1	FSEL_B0	QB[0:3]
0	0	0	VCO÷8
0	0	1	VCO÷12
0	1	0	VCO÷16
0	1	1	VCO÷20
1	0	0	VCO÷4
1	0	1	VCO÷6
1	1	0	VCO÷8
1	1	1	VCO÷10

Table 5. Output Divider Bank C (N_C)

VCO_SEL	FSEL_C1	FSEL_C0	QC[0:3]
0	0	0	VCO÷4
0	0	1	VCO÷8
0	1	0	VCO÷12
0	1	1	VCO÷16
1	0	0	VCO÷2
1	0	1	VCO÷4
1	1	0	VCO÷6
1	1	1	VCO÷8

Table 6. Output Divider PLL Feedback (M)

VCO_SEL	FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	0	VCO÷8
0	0	0	1	VCO÷12
0	0	1	0	VCO÷16
0	0	1	1	VCO÷20
0	1	0	0	VCO÷16
0	1	0	1	VCO÷24
0	1	1	0	VCO÷32
0	1	1	1	VCO÷40
1	0	0	0	VCO÷4
1	0	0	1	VCO÷6
1	0	1	0	VCO÷8
1	0	1	1	VCO÷10
1	1	0	0	VCO÷8
1	1	0	1	VCO÷12
1	1	1	0	VCO÷16
1	1	1	1	VCO÷20

Table 7. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		12		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 8. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 9. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{CC_PLL}	PLL Supply Voltage	3.0		V_{CC}	V	LVCMOS
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH}=–24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24 mA I_{OL}= 12 mA
Z_{OUT}	Output Impedance		14 – 17		W	
I_{IN}	Input Current[2]			±200	μA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		3.0	5.0	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current			15	mA	All V_{CC} Pins

1. The MPC9772 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
2. Inputs have pull-down resistors affecting the input current.

Table 10. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40° to +85°C)[1, 2]

Symbol	Characteristics		Min	Typ	Max		Unit	Condition
					T_A = 0°C to +70°C	T_A = –40°C to +85°C		
f_{REF}	Input reference frequency	÷4 feedback	50.0		120.0	115.00	MHz	PLL locked
		÷6 feedback	33.3		80.0	76.67	MHz	
		÷8 feedback	25.0		60.0	57.50	MHz	
		÷10 feedback	20.0		48.0	46.00	MHz	
		÷12 feedback	16.6		40.0	38.33	MHz	
		÷16 feedback	12.5		30.0	28.75	MHz	
		÷20 feedback	10.0		24.0	23.00	MHz	
		÷24 feedback	8.33		20.0	19.16	MHz	
		÷32 feedback	6.25		15.0	14.37	MHz	
		÷40 feedback	5.00		12.0	11.50	MHz	
	Input reference frequency in PLL bypass mode[3]				250	250	MHz	PLL bypass
f_{VCO}	VCO frequency range[4]		200		480	460	MHz	
f_{XTAL}	Crystal interface frequency range[4]		10		25		MHz	
f_{MAX}	Output Frequency	÷2 output	100.0		240.0	230.00	MHz	PLL locked
		÷4 output	50.0		120.0	115.00	MHz	
		÷6 output	33.3		80.0	76.67	MHz	
		÷8 output	25.0		60.0	57.50	MHz	
		÷10 output	20.0		48.0	46.00	MHz	
		÷12 output	16.6		40.0	38.33	MHz	
		÷16 output	12.5		30.0	28.75	MHz	
		÷20 output	10.0		24.0	23.00	MHz	
		÷24 output	8.33		20.0	19.16	MHz	
f_{STOP_CLK}	Serial interface clock frequency				20		MHz	
$t_{PW,MIN}$	Input Reference Pulse Width[5]		2.0				ns	
t_R, t_F	CCLKx Input Rise/Fall Time[6]				1.0		ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)[7]							PLL locked
	CCLK to FB_IN	6.25 MHz < f_{REF} < 65.0 MHz	–3		+3		°	
		65.0 MHz < f_{REF} < 125 MHz	–4		+4		°	
		f_{REF}=50 MHz and feedback=÷8	–166		+166		ps	
$t_{SK(O)}$	Output-to-output Skew[8]	within QA outputs			100		ps	
		within QB outputs			100		ps	
		within QC outputs			100		ps	
		all outputs			250		ps	
DC	Output Duty Cycle[9]		(T÷2) – 200	T ÷ 2	(T÷2) + 200		ps	
t_R, t_F	Output Rise/Fall Time		0.1		1.0		ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				8		ns	
$t_{PZL, LZ}$	Output Enable Time				8		ns	
$t_{JIT(CC)}$	Cycle-to-cycle Jitter[10]			150	200		ps	
$t_{JIT(PER)}$	Period Jitter[11]				150		ps	

Table 10. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40° to +85°C)[1, 2] **(Continued)**

Symbol	Characteristics		Min	Typ	Max		Unit	Condition
					T_A = 0°C to +70°C	T_A = –40°C to +85°C		
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)[12]	÷4 feedback			11		ps	(VCO=400 MHz)
		÷6 feedback			86		ps	
		÷8 feedback			13		ps	
		÷10 feedback			88		ps	
		÷12 feedback			16		ps	
		÷16 feedback			19		ps	
		÷20 feedback			21		ps	
		÷24 feedback			22		ps	
		÷32 feedback			27		ps	
		÷40 feedback			30		ps	
BW	PLL closed loop bandwidth[13]	÷4 feedback		1.20 – 3.50			MHz	
		÷6 feedback		0.70 – 2.50			MHz	
		÷8 feedback		0.50 – 1.80			MHz	
		÷10 feedback		0.45 – 1.20			MHz	
		÷12 feedback		0.30 – 1.00			MHz	
		÷16 feedback		0.25 – 0.70			MHz	
		÷20 feedback		0.20 – 0.55			MHz	
		÷24 feedback		0.17 – 0.40			MHz	
		÷32 feedback		0.12 – 0.30			MHz	
		÷40 feedback		0.11 – 0.28			MHz	
t_{LOCK}	Maximum PLL Lock Time				10		ms	

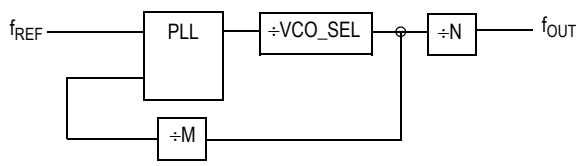
1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. In bypass mode, the MPC9772 divides the input reference clock.
3. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{REF} = f_{VCO} \div (M$ Þ VCO_SEL).
4. The crystal frequency range must both meet the interface frequency range and VCO lock range divided by the feedback divider ratio: $f_{XTAL(min, max)} = f_{VCO(min, max)} \div (M \cdot$ VCO_SEL) and 10 MHz ≤ f_{XTAL} ≤ 25 MHz.
5. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% – DC_{REF, MIN}$.
6. The MPC9772 will operate with input rise/fall times up to 3.0 ns, but the A.C. characteristics, specifically $t_{(\varnothing)}$, $t_{PW,MIN}$, DC and f_{MAX} can only be guaranteed if t_R, t_F are within the specified range.
7. Static phase offset depends on the reference frequency. $t_{(\varnothing)}$ [s] = $t_{(\varnothing)}$ [°] ÷ ($f_{REF} \cdot 360°$).
8. Excluding QSYNC output. See application section for part-to-part skew calculation.
9. Output duty cycle is DC = (0.5 ± 200 ps · f_{OUT}) . 100%. E.g. the DC range at f_{OUT} = 100 MHz is 48%<DC<52%. T = output period.
10. Cycle jitter is valid for all outputs in the same divider configuration. See application section for more details.
11. Period jitter is valid for all outputs in the same divider configuration. See application section for more details.
12. I/O jitter is valid for a VCO frequency of 400 MHz. See application section for I/O jitter vs. VCO frequency.
13. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

MPC9772 Configurations

Configuring the MPC9772 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$



where f_{REF} is the reference frequency of the selected input clock source (CCLKO, CCLK1 or XTAL interface), M is the PLL feedback divider and N is a output divider. The PLL feedback divider is configured by the FSEL_FB[2:0] and the output dividers are individually configured for each output bank by the FSEL_A[1:0], FSEL_B[1:0] and FSEL_C[1:0] inputs.

The reference frequency f_{REF} and the selection of the feedback-divider M is limited by the specified VCO frequency range. f_{REF} and M must be configured to match the VCO frequency range of 200 to 480 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \leq (f_{REF} \cdot VCO\_SEL \cdot M) \leq f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-one or a divide-by-two and can be used to situate the VCO into the specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio.

The output frequency for each bank can be derived from the VCO frequency and output divider:

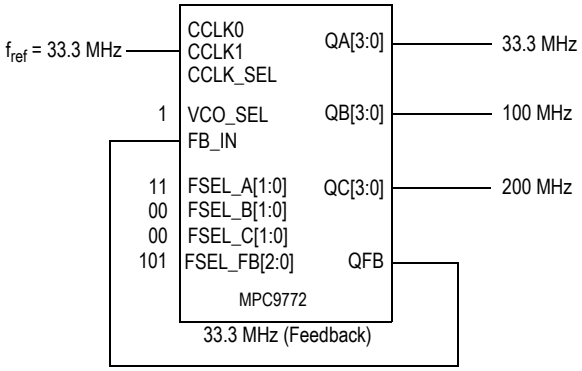
$$f_{QA[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$
$$f_{QB[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$
$$f_{QC[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

Table 11. MPC9772 Divider

Divider	Function	VCO_SEL	Values
M	PLL feedback FSEL_FB[0:3]	÷1	4, 6, 8, 10, 12, 16
		÷2	8, 12, 16, 20, 24, 32, 40
N_A	Bank A Output Divider FSEL_A[0:1]	÷1	4, 6, 8, 12
		÷2	8, 12, 16, 24
N_B	Bank B Output Divider FSEL_B[0:1]	÷1	4, 6, 8, 10
		÷2	8, 12, 16, 20
N_C	Bank C Output Divider FSEL_C[0:1]	÷1	2, 4, 6, 8
		÷2	4, 8, 12, 16

Table 11 shows the various PLL feedback and output dividers and Figure 3. Example Configuration and Figure 4. Example Configuration display example configurations for the MPC9772:

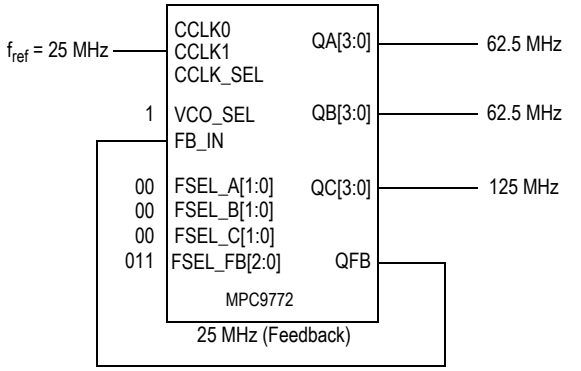
Figure 3. Example Configuration



MPC9772 example configuration (feedback of QFB = 33.3 MHz, f_{VCO}=400 MHz, VCO_SEL=÷1, M=12, N_A=12, N_B=4, N_C=2).

Frequency Range	T_A = 0°C to +70°C	T_A = –40°C to +85°C
Input	16.6 – 40 MHz	16.6 – 38.33 MHz
QA Outputs	16.6 – 40 MHz	16.6 – 38.33 MHz
QA Outputs	50 – 120 MHz	50 – 115 MHz
QC Outputs	100 – 240 MHz	100 – 230 MHz

Figure 4. Example Configuration



MPC9772 example configuration (feedback of QFB = 25 MHz, f_{VCO}=250 MHz, VCO_SEL=÷1, M=10, N_A=4, N_B=4, N_C=2).

Frequency Range	T_A = 0°C to +70°C	T_A = –40°C to +85°C
Input	20 – 48 MHz	20 – 46 MHz
QA Outputs	50 – 120 MHz	50 – 115 MHz
QA Outputs	50 – 120 MHz	50 – 115 MHz
QC Outputs	100 – 240 MHz	100 – 230 MHz

MPC9772 Individual Output Disable (Clock Stop) Circuitry

The individual clock stop (output enable) control of the MPC9772 allows designers, under software control, to implement power management into the clock distribution design. A simple serial interface and a clock stop control logic provides a mechanism through which the MPC9772 clock outputs can be individually stopped in the logic ‘0' state: The clock stop mechanism allows serial loading of a 12-bit serial input register. This register contains one programmable clock stop bit for 12 of the 14 output clocks. The QC0 and QFB outputs cannot be stopped (disabled) with the serial port.

The user can program an output clock to stop (disable) by writing logic ‘0' to the respective stop enable bit. Likewise, the user may programmably enable an output clock by writing logic ‘1' to the respective enable bit. The clock stop logic enables or disables clock outputs during the time when the output would be in normally in logic low state, eliminating the possibility of short or ‘runt' clock pulses.

The user can write to the serial input register through the STOP_DATA input by supplying a logic ‘0' start bit followed serially by 12 NRZ disable/enable bits. The period of each STOP_DATA bit equals the period of the free—running STOP_CLK signal. The STOP_DATA serial transmission should be timed so the MPC9772 can sample each STOP_DATA bit with the rising edge of the free—running STOP_CLK signal. (See Figure 5. Clock Stop Circuit Programming.)

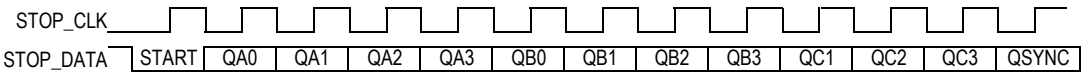


Figure 5. Clock Stop Circuit Programming

SYNC Output Description

The MPC9772 has a system synchronization pulse output QSYNC. In configurations with the output frequency relationships are not integer multiples of each other QSYNC provides a signal for system synchronization purposes. The MPC9772 monitors the relationship between the A bank and the B bank of outputs. The QSYNC output is asserted (logic low) one period in duration and one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse is dependent QA and QC output frequencies: the QSYNC pulse width is equal to the period of the higher of the QA and QC output frequencies. Figure 6. QSYNC Timing Diagram shows various waveforms for the QSYNC output. The QSYNC output is defined for all possible combinations of the bank A and bank C outputs.

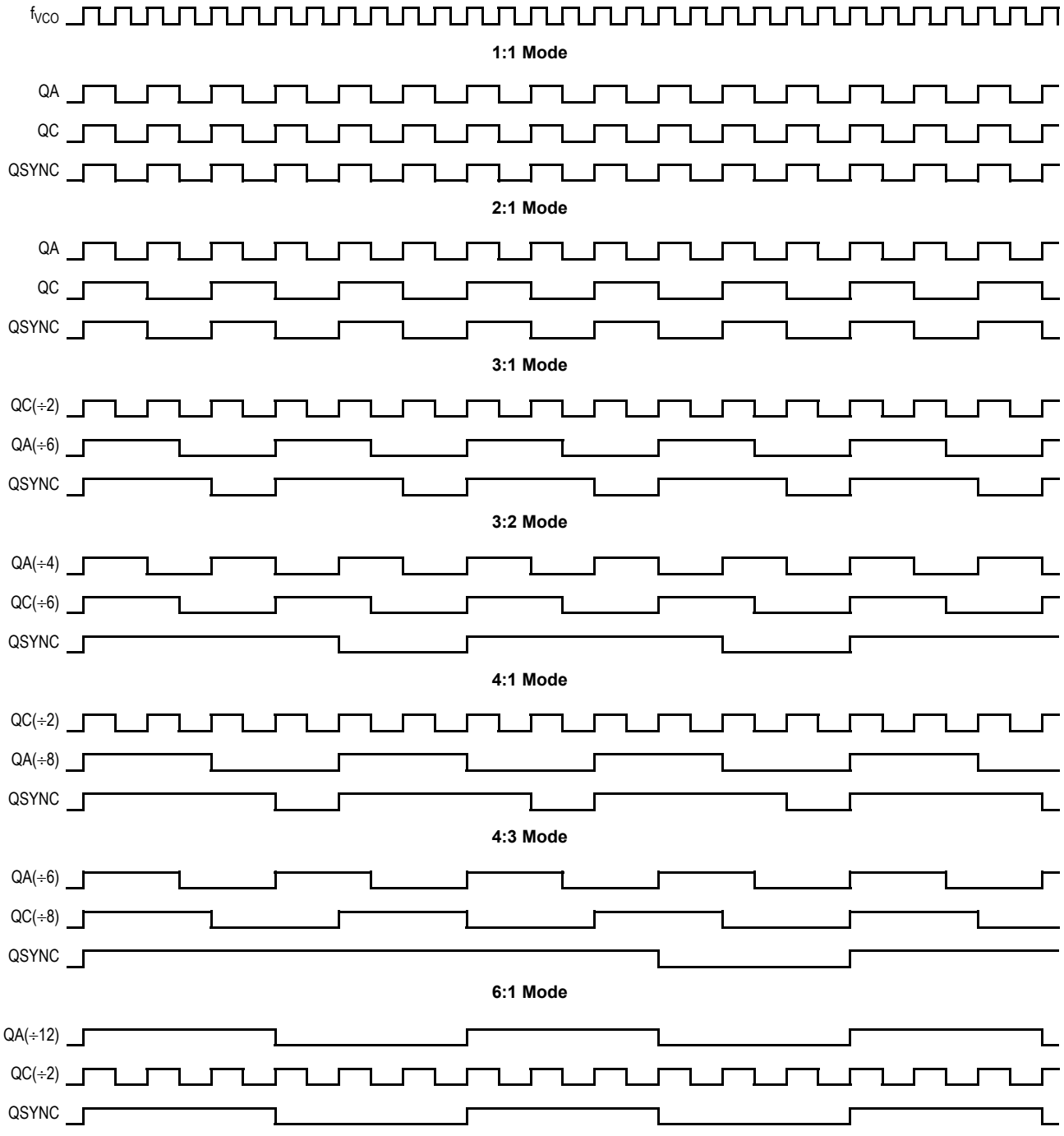


Figure 6. QSYNC Timing Diagram

Power Supply Filtering

The MPC9772 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9772 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA_PLL} pin for the MPC9772. Figure 7. VCC_PLL Power Supply Filter illustrates a typical power supply filter scheme. The MPC9772 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 7. VCC_PLL Power Supply Filter must have a resistance of 5-10Ω to meet the voltage drop criteria.

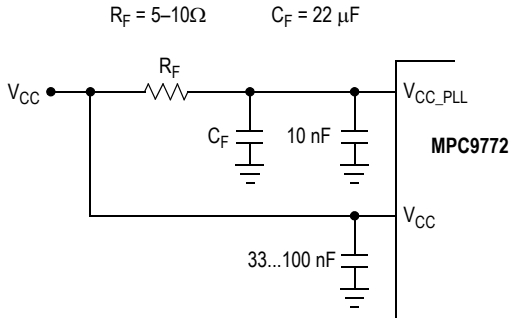


Figure 7. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7. VCC_PLL Power Supply Filter, the filter cut-off frequency is around 4.5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9772 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9772 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9772. Designs using the MPC9772 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9772 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9772 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9772 are connected together, the maximum overall timing uncertainty from the common CCLKx input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

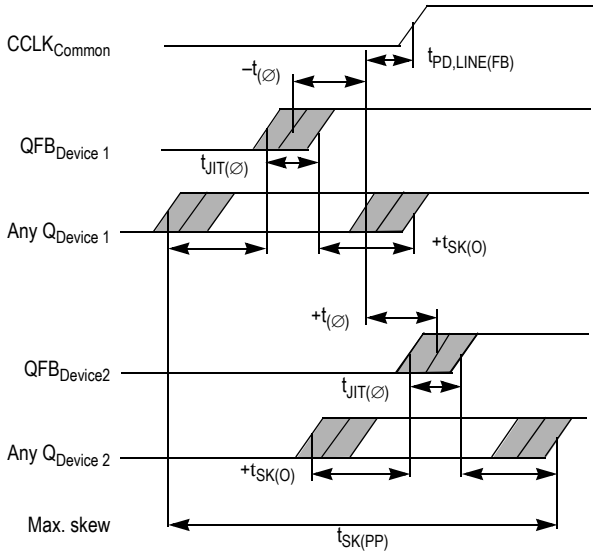


Figure 8. MPC9772 Maximum Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 12. Confidence Factor CF.

Table 12. Confidence Factor CF

CF	Probability of Clock Edge within the Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device.

Due to the frequency dependence of the static phase offset and I/O jitter, using Figure 9. MPC9772 I/O Jitter to Figure 11. MPC9772 I/O Jitter to predict a maximum I/O jitter and the specified $t_{(\varnothing)}$ parameter relative to the input reference frequency results in a precise timing performance analysis.

In the following example calculation an I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from the common input reference clock to any output of –455 ps to +455 ps relative to CCLK (PLL feedback = ÷8, reference frequency = 50 MHz, VCO frequency = 400 MHz, I/O jitter = 13 ps rms max., static phase offset $t_{(\varnothing)}$ = ± 166 ps):

$t_{SK(PP)}$ = *[-166ps...166ps] + [-250ps...250ps] + [(13ps @ –3)...(13ps @ 3)] +* $t_{PD, LINE(FB)}$

$t_{SK(PP)}$ = *[-455ps...455ps]* + $t_{PD, LINE(FB)}$

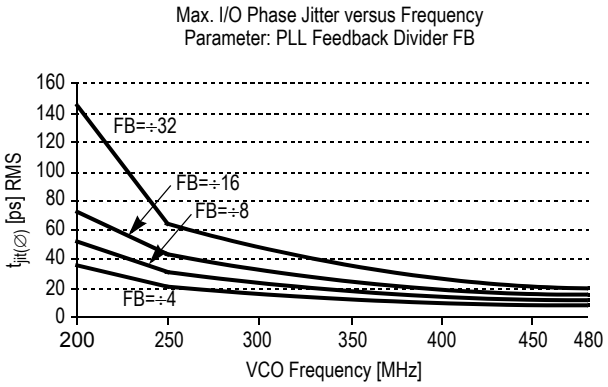


Figure 9. MPC9772 I/O Jitter

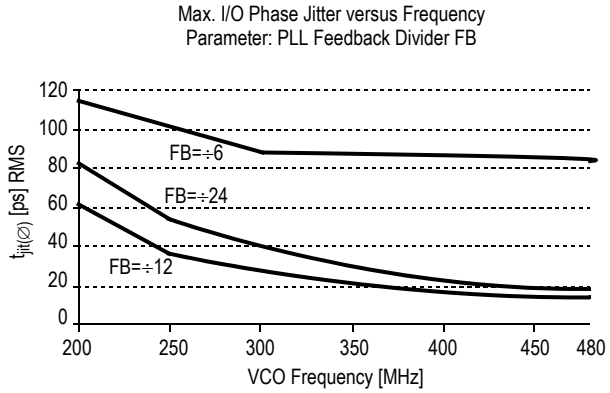


Figure 10. MPC9772 I/O Jitter

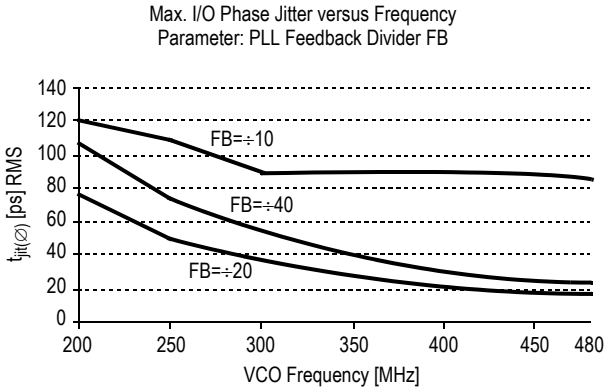


Figure 11. MPC9772 I/O Jitter

Driving Transmission Lines

The MPC9772 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9772 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 12. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9772 clock driver is effectively doubled due to its capability to drive multiple lines.

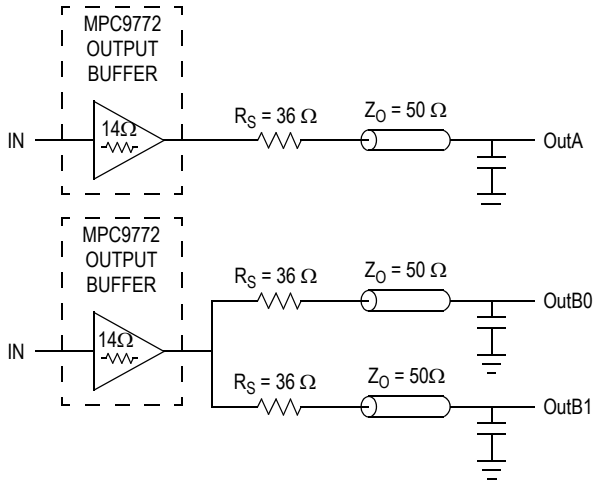


Figure 12. Single versus Dual Transmission Lines

The waveform plots in Figure 13. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9772 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9772. The output waveform in Figure 13. Single versus Dual Waveforms shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 (25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

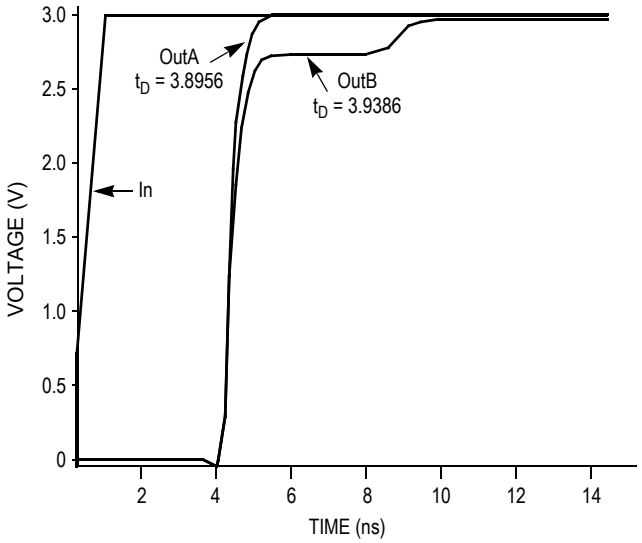
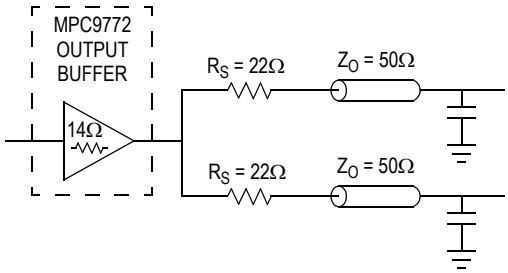


Figure 13. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 14. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

Figure 14. Optimized Dual Line Termination

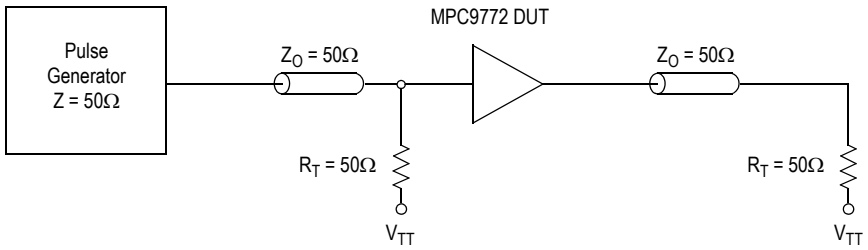
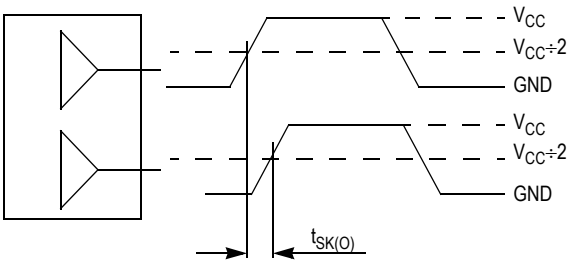


Figure 15. CCLK MPC9772 AC Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 16. Output-to-Output Skew $t_{SK(O)}$

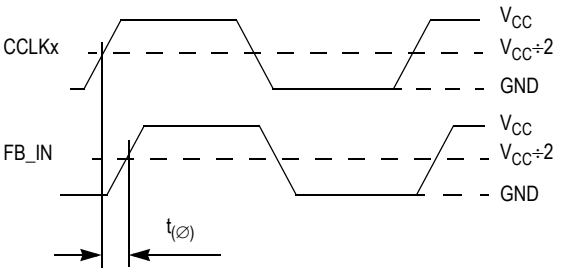
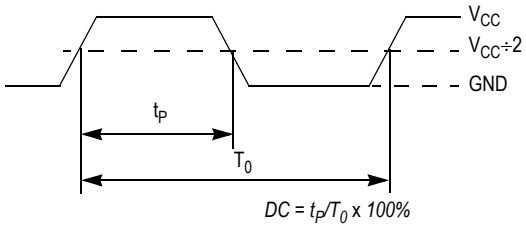
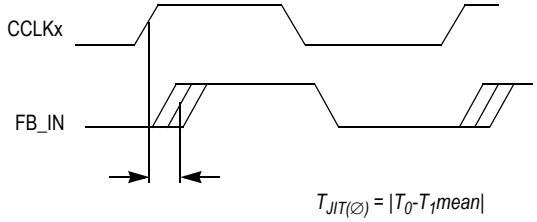


Figure 17. Propagation Delay ($t_{(\varnothing)}$, Static Phase Offset) Test Reference



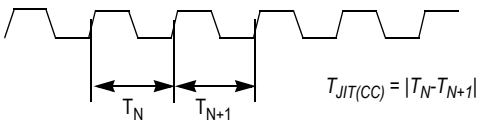
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 18. Output Duty Cycle (DC)



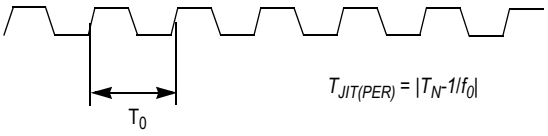
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 19. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 20. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 21. Period Jitter

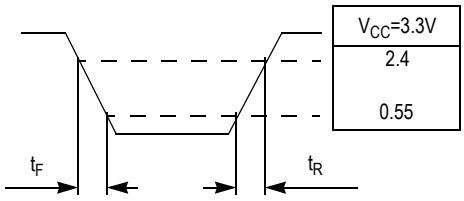


Figure 22. Output Transition Time Test Reference

Order number: MPC9773
Rev 4, 08/2004

3.3 V 1:12 LVCMOS PLL Clock Generator

MPC9773

3.3 V 1:12 LVCMOS PLL CLOCK GENERATOR

FA SUFFIX
52-LEAD LQFP PACKAGE
CASE 848D-03

The MPC9773 is a 3.3 V compatible, 1:12 PLL based clock generator targeted for high-performance low-skew clock distribution in mid-range to high-performance networking, computing, and telecom applications. With output frequencies up to 240 MHz and output skews less than 250 ps the device meets the needs of the most demanding clock applications.

Features

- 1:12 PLL based low-voltage clock generator
- 3.3 V power supply
- Internal power-on reset
- Generates clock signals up to 240 MHz
- Maximum output skew of 250 ps
- Differential PECL reference clock input
- Two LVCMOS PLL reference clock inputs
- External PLL feedback supports zero-delay capability
- Various feedback and output dividers (refer to Application Section)
- Supports up to three individual generated output clock frequencies
- Synchronous output clock stop circuitry for each individual output for power down support
- Drives up to 24 clock lines
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC973
- 52-lead Pb-free Package Available

Functional Description

The MPC9773 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9773 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC9773 features an extensive level of frequency programmability between the 12 outputs as well as the output to input relationships, for instance 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 5:4, 5:6, 6:1, 8:1 and 8:3.

The QSYNC output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies. This allows for very flexible programming of the input reference versus output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non-binary factor. The MPC9773 also supports the 180° phase shift of one of its output banks with respect to the other output banks. The QSYNC outputs reflects the phase relationship between the QA and QC outputs and can be used for the generation of system baseline timing signals.

The REF_SEL pin selects the LVPECL or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be individually disabled (stopped in logic low state) by programming the serial CLOCK_STOP interface of the MPC9773. The MPC9773 has an internal power-on reset.

The MPC9773 is fully 3.3 V compatible and requires no external loop filter components. All inputs (except PCLK) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9773 outputs can drive one or two traces giving the devices an effective fanout of 1:24. The device is pin and function compatible to the MPC973 and is packaged in a 52-lead LQFP package.

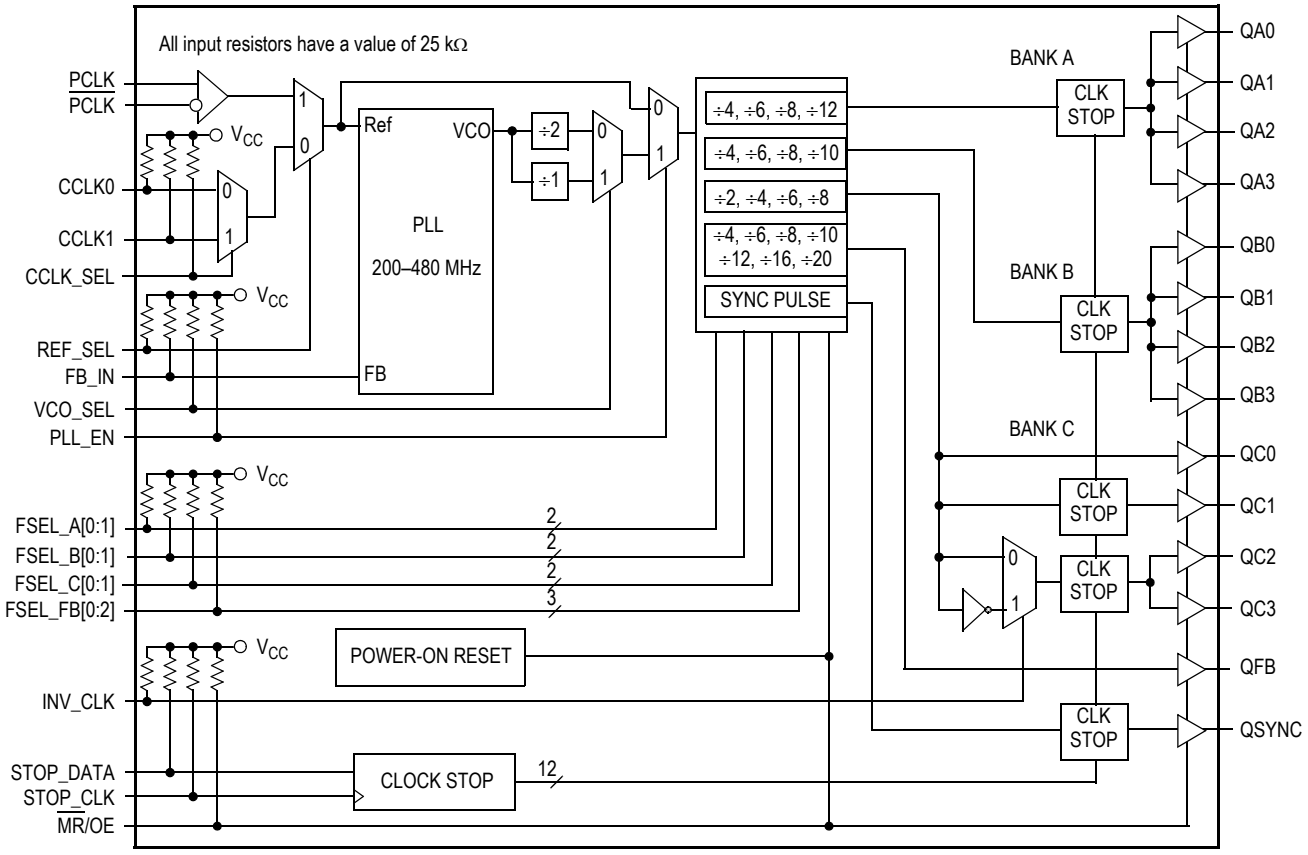


Figure 1. MPC9773 Logic Diagram

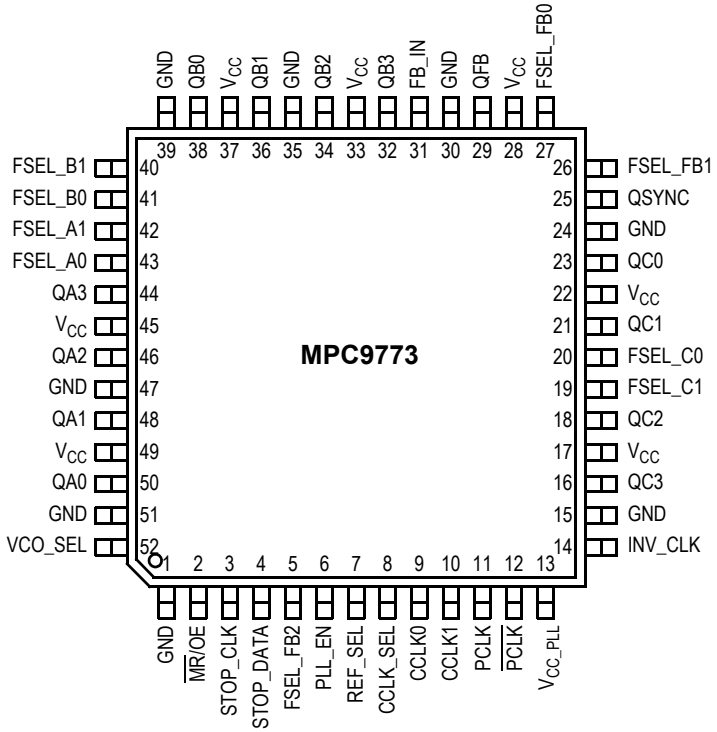


Figure 2. MPC9773 52-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK0	Input	LVCMOS	PLL reference clock
CCLK1	Input	LVCMOS	Alternative PLL reference clock
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	Differential LVPECL reference clock
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to an QFB
CCLK_SEL	Input	LVCMOS	LVCMOS clock reference select
REF_SEL	Input	LVCMOS	LVCMOS/PECL reference clock select
VCO_SEL	Input	LVCMOS	VCO operating frequency select
PLL_EN	Input	LVCMOS	PLL enable/PLL bypass mode select
$\overline{\text{MR}}$/OE	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
FSEL_A[0:1]	Input	LVCMOS	Frequency divider select for bank A outputs
FSEL_B[0:1]	Input	LVCMOS	Frequency divider select for bank B outputs
FSEL_C[0:1]	Input	LVCMOS	Frequency divider select for bank C outputs
FSEL_FB[0:2]	Input	LVCMOS	Frequency divider select for the QFB output
INV_CLK	Input	LVCMOS	Clock phase selection for outputs QC2 and QC3
STOP_CLK	Input	LVCMOS	Clock input for clock stop circuitry
STOP_DATA	Input	LVCMOS	Configuration data input for clock stop circuitry
QA[0-3]	Output	LVCMOS	Clock outputs (Bank A)
QB[0-3]	Output	LVCMOS	Clock outputs (Bank B)
QC[0-3]	Output	LVCMOS	Clock outputs (Bank C)
QFB	Output	LVCMOS	PLL feedback output. Connect to FB_IN.
QSYNC	Output	LVCMOS	Synchronization pulse output
GND	Supply	Ground	Negative power supply
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please refer to applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table (Configuration Controls)

Control	Default	0	1
REF_SEL	1	Selects CCLKx as the PLL reference clock	Selects the LVPECL inputs as the PLL reference clock
CCLK_SEL	1	Selects CCLK0	Selects CCLK1
VCO_SEL	1	Selects VCO ÷ 2. The VCO frequency is scaled by a factor of 2 (low VCO frequency range).	Selects VCO ÷ 1 (high VCO frequency range)
PLL_EN	1	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9773 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
INV_CLK	1	QC2 and QC3 are in phase with QC0 and QC1	QC2 and QC3 are inverted (180° phase shift) with respect to QC0 and QC1
$\overline{\text{MR}}$/OE	1	Outputs disabled (high-impedance state) and device is reset. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC9773 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). The device is reset by the internal power-on reset (POR) circuitry during power-up.	Outputs enabled (active)

VCO_SEL, FSEL_A[0:1], FSEL_B[0:1], FSEL_C[0:1], FSEL_FB[0:2] control the operating PLL frequency range and input/output frequency ratios. See Table 3 to Table 6 and the Applications Section for supported frequency ranges and output to input frequency ratios.

Table 3. Output Divider Bank A (N_A)

VCO_SEL	FSEL_A1	FSEL_A0	QA[0:3]
0	0	0	VCO ÷ 8
0	0	1	VCO ÷ 12
0	1	0	VCO ÷ 16
0	1	1	VCO ÷ 24
1	0	0	VCO ÷ 4
1	0	1	VCO ÷ 6
1	1	0	VCO ÷ 8
1	1	1	VCO ÷ 12

Table 4. Output Divider Bank (N_B)

VCO_SEL	FSEL_B1	FSEL_B0	QB[0:3]
0	0	0	VCO ÷ 8
0	0	1	VCO ÷ 12
0	1	0	VCO ÷ 16
0	1	1	VCO ÷ 20
1	0	0	VCO ÷ 4
1	0	1	VCO ÷ 6
1	1	0	VCO ÷ 8
1	1	1	VCO ÷ 10

Table 5. Ouput Divider Bank (N_C)

VCO_SEL	FSEL_C1	FSEL_C0	QC[0:3]
0	0	0	VCO ÷ 4
0	0	1	VCO ÷ 8
0	1	0	VCO ÷ 12
0	1	1	VCO ÷ 16
1	0	0	VCO ÷ 2
1	0	1	VCO ÷ 4
1	1	0	VCO ÷ 6
1	1	1	VCO ÷ 8

Table 6. Output Divider PLL Feedback (M)

VCO_SEL	FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	0	VCO ÷ 8
0	0	0	1	VCO ÷ 12
0	0	1	0	VCO ÷ 16
0	0	1	1	VCO ÷ 20
0	1	0	0	VCO ÷ 16
0	1	0	1	VCO ÷ 24
0	1	1	0	VCO ÷ 32
0	1	1	1	VCO ÷ 40
1	0	0	0	VCO ÷ 4
1	0	0	1	VCO ÷ 6
1	0	1	0	VCO ÷ 8
1	0	1	1	VCO ÷ 10
1	1	0	0	VCO ÷ 8
1	1	0	1	VCO ÷ 12
1	1	1	0	VCO ÷ 16
1	1	1	1	VCO ÷ 20

Table 7. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		12		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 8. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 9. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{CC_PLL}	PLL Supply Voltage		3.0		V_{CC}	V	LVCMOS
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage				0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK, $\overline{PCLK}$	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA[2]
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance			14 – 17		Ω	
I_{IN}	Input Current[3]				±200	μA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current			8.0	13.5	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current				35	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9773 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
3. Inputs have pull-down resistors affecting the input current.

Table 10. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)[1, 2]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Reference Frequency	÷ 4 feedback	50.0		120.0	MHz	PLL locked
		÷ 6 feedback	33.3		80.0	MHz	
		÷ 8 feedback	25.0		60.0	MHz	
		÷ 10 feedback	20.0		48.0	MHz	
		÷ 12 feedback	16.6		40.0	MHz	
		÷ 16 feedback	12.5		30.0	MHz	
		÷ 20 feedback	10.0		24.0	MHz	PLL bypass
		÷ 24 feedback	8.33		20.0	MHz	
		÷ 32 feedback	6.25		15.0	MHz	
		÷ 40 feedback	5.00		12.0	MHz	
	Input Reference Frequency in PLL Bypass Mode				250	MHz	
f_{VCO}	VCO Frequency Range[3]		200		480	MHz	
f_{MAX}	Output Frequency	÷ 2 output	100.0		240.0	MHz	PLL locked
		÷ 4 output	50.0		120.0	MHz	
		÷ 6 output	33.3		80.0	MHz	
		÷ 8 output	25.0		60.0	MHz	
		÷ 10 output	20.0		48.0	MHz	
		÷ 12 output	16.6		40.0	MHz	
		÷ 16 output	12.5		30.0	MHz	
		÷ 20 output	10.0		24.0	MHz	
		÷ 24 output	8.33		20.0	MHz	
f_{STOP_CLK}	Serial Interface Clock Frequency				20	MHz	
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	400		1000	mV	LVPECL
V_{CMR}[4]	Common Mode Range	PCLK, $\overline{PCLK}$	1.2		V_{CC} – 0.9	V	LVPECL
$t_{PW,MIN}$	Input Reference Pulse Width[4]		2.0			ns	
t_R, t_F	CCLKx Input Rise/Fall Time[5]				1.0	ns	0.8 to 2.0 V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)[6]						PLL locked
	6.25 MHz < f_{REF} < 65.0 MHz		–3		+3	°	
	65.0 MHz < f_{REF} < 125 MHz		–4		+4	°	
	f_{REF} = 50 MHz and feedback = ÷8		–166		+166	ps	
$t_{SK(O)}$	Output-to-Output Skew[7]	within QA outputs			100	ps	
		within QB outputs			100	ps	
		within QC outputs			100	ps	
		all outputs			250	ps	
DC	Output Duty Cycle[8]		(T÷2) –200	T÷2	(T÷2) +200	ps	
t_R, t_F	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time				8.0	ns	
$t_{PZL, LZ}$	Output Enable Time				8.0	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter[9]			150	200	ps	
$t_{JIT(PER)}$	Period Jitter[10]				150	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)[11]	÷ 4 feedback			11	ps	(VCO = 400 MHz)
		÷ 6 feedback			86	ps	
		÷ 8 feedback			13	ps	
		÷ 10 feedback			88	ps	
		÷ 12 feedback			16	ps	
		÷ 16 feedback			19	ps	
		÷ 20 feedback			21	ps	
		÷ 24 feedback			22	ps	
		÷ 32 feedback			27	ps	
		÷ 40 feedback			30	ps	

Table 10. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)[1, 2]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
BW	PLL Closed Loop Bandwidth[12]	÷ 4 feedback		1.20 – 3.50		MHz	
		÷ 6 feedback		0.70 – 2.50		MHz	
		÷ 8 feedback		0.50 – 1.80		MHz	
		÷ 10 feedback		0.45 – 1.20		MHz	
		÷ 12 feedback		0.30 – 1.00		MHz	
		÷ 16 feedback		0.25 – 0.70		MHz	
		÷ 20 feedback		0.20 – 0.55		MHz	
		÷ 24 feedback		0.17 – 0.40		MHz	
		÷ 32 feedback		0.12 – 0.30		MHz	
		÷ 40 feedback		0.11 – 0.28		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

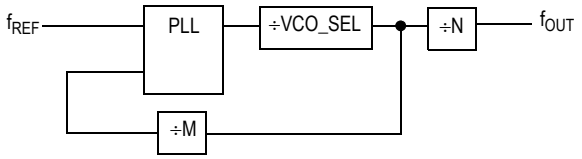
1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. The input reference frequency must match the VCO lock range divided by the feedback divider ratio: $f_{REF} = f_{VCO} \div (M \cdot VCO\_SEL)$.
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
4. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% – DC_{REF,MIN}$.
5. The MPC9773 will operate with input rise/fall times up to 3.0 ns, but the A.C. characteristics, specifically $t_{(\varnothing)}$, $t_{PW,MIN}$, DC and f_{MAX} can only be guaranteed if t_R, t_F are within the specified range.
6. CCLKx or PCLK to FB_IN. Static phase offset depends on the reference frequency. $t_{(\varnothing)}$ [s] = $t_{(\varnothing)}$ [°] ÷ ($f_{REF} \cdot 360°$).
7. Excluding QSYNC output. Refer to application section for part-to-part skew calculation.
8. Output duty cycle is DC = (0.5 ± 200 ps · f_{OUT}) . 100%. E.g., the DC range at f_{OUT} = 100 MHz is 48% < DC < 52%. T = output period.
9. Cycle jitter is valid for all outputs in the same divider configuration. Refer to APPLICATIONS INFORMATION for more details.
10. Period jitter is valid for all outputs in the same divider configuration. Refer to APPLICATIONS INFORMATION for more details.
11. I/O jitter is valid for a VCO frequency of 400 MHz. Refer to APPLICATIONS INFORMATION for I/O jitter vs. VCO frequency.
12. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

MPC9773 Configurations

Configuring the MPC9773 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$



where f_{REF} is the reference frequency of the selected input clock source (CCLKO, CCLK1 or PCLK), M is the PLL feedback divider and N is a output divider. The PLL feedback divider is configured by the FSEL_FB[2:0] and the output dividers are individually configured for each output bank by the FSEL_A[1:0], FSEL_B[1:0] and FSEL_C[1:0] inputs.

The reference frequency f_{REF} and the selection of the feedback-divider M is limited by the specified VCO frequency range. f_{REF} and M must be configured to match the VCO frequency range of 200 to 480 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \leq (f_{REF} \cdot VCO\_SEL \cdot M) \leq f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-one or a divide-by-two and can be used to situate the VCO into the specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio.

The output frequency for each bank can be derived from the VCO frequency and output divider:

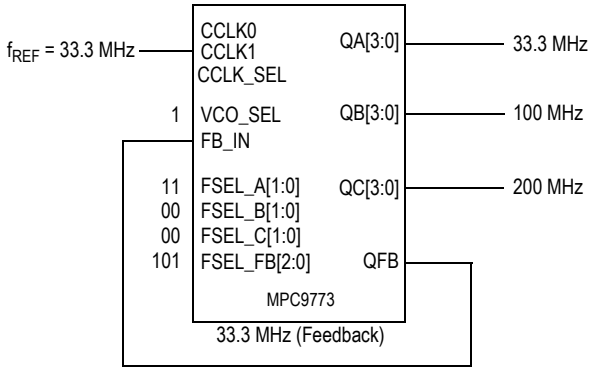
$$f_{QA[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$
$$f_{QB[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$
$$f_{QC[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

Table 11. MPC9773 Divider

Divider	Function	VCO_SEL	Values
M	PLL Feedback FSEL_FB[0:3]	÷1	4, 6, 8, 10, 12, 16
		÷2	8, 12, 16, 20, 24, 32, 40
N_A	Bank A Output Divider FSEL_A[0:1]	÷1	4, 6, 8, 12
		÷2	8, 12, 16, 24
N_B	Bank B Output Divider FSEL_B[0:1]	÷1	4, 6, 8, 10
		÷2	8, 12, 16, 20
N_C	Bank C Output Divider FSEL_C[0:1]	÷1	2, 4, 6, 8
		÷2	4, 8, 12, 16

Table 11 shows the various PLL feedback and output dividers and Figure 3 and Figure 4 display example configurations for the MPC9773.

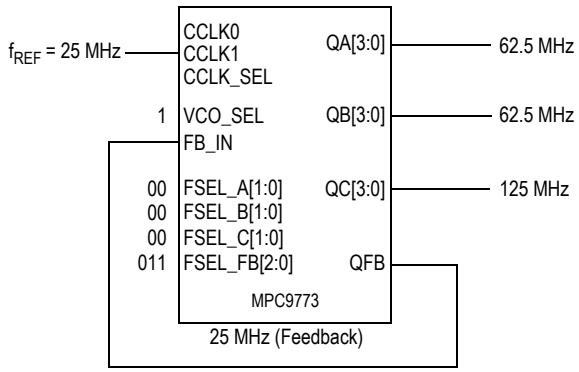
Figure 3. Example Configuration



MPC9773 example configuration (feedback of QFB = 33.3 MHz, f_{VCO} = 400 MHz, VCO_SEL = ÷1, M = 12, N_A = 12, N_B = 4, N_C = 2).

Frequency Range	Min	Max
Input	16.6 MHz	40 MHz
QA outputs	16.6 MHz	40 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

Figure 4. Example Configuration



MPC9773 example configuration (feedback of QFB = 25 MHz, f_{VCO} = 250 MHz, VCO_SEL = ÷1, M = 10, N_A = 4, N_B = 4, N_C = 2).

Frequency Range	Min	Max
Input	20 MHz	48 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	240 MHz

MPC9773 Individual Output Disable (Clock Stop) Circuitry

The individual clock stop (output enable) control of the MPC9773 allows designers, under software control, to implement power management into the clock distribution design. A simple serial interface and a clock stop control logic provides a mechanism through which the MPC9773 clock outputs can be individually stopped in the logic ‘0' state: The clock stop mechanism allows serial loading of a 12-bit serial input register. This register contains one programmable clock stop bit for 12 of the 14 output clocks. The QC0 and QFB outputs cannot be stopped (disabled) with the serial port.

The user can program an output clock to stop (disable) by writing logic ‘0' to the respective stop enable bit. Likewise, the user may programmably enable an output clock by writing logic ‘1' to the respective enable bit. The clock stop logic enables or disables clock outputs during the time when the output would be in normally in logic low state, eliminating the possibility of short or ‘runt' clock pulses.

The user can write to the serial input register through the STOP_DATA input by supplying a logic ‘0' start bit followed serially by 12 NRZ disable/enable bits. The period of each STOP_DATA bit equals the period of the free-running STOP_CLK signal. The STOP_DATA serial transmission should be timed so the MPC9773 can sample each STOP_DATA bit with the rising edge of the free-running STOP_CLK signal. (See Figure 5.)

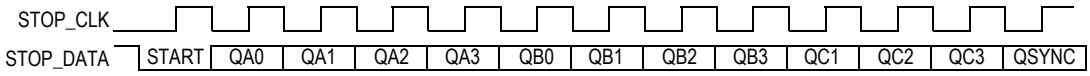


Figure 5. Clock Stop Circuit Programing

SYNC Output Description

The MPC9773 has a system synchronization pulse output QSYNC. In configurations with the output frequency relationships are not integer multiples of each other QSYNC provides a signal for system synchronization purposes. The MPC9773 monitors the relationship between the A bank and the B bank of outputs. The QSYNC output is asserted (logic low) one period in duration and one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse is dependent QA and QC output frequencies: the QSYNC pulse width is equal to the period of the higher of the QA and QC output frequencies. Figure 6 shows various waveforms for the QSYNC output. The QSYNC output is defined for all possible combinations of the bank A and bank C outputs.

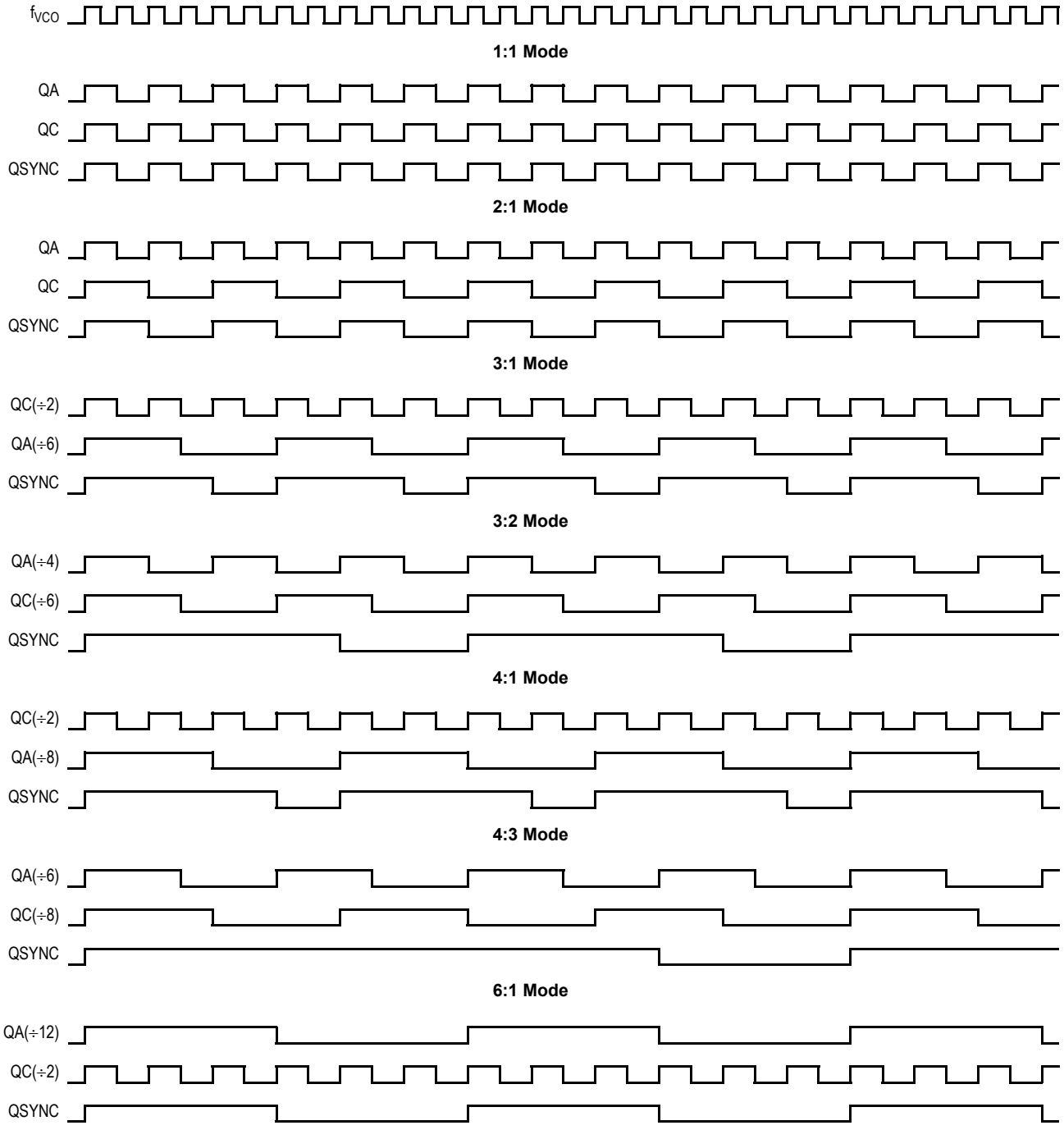


Figure 6. QSYNC Timing Diagram

Power Supply Filtering

The MPC9773 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9773 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA_PLL} pin for the MPC9773. Figure 7 illustrates a typical power supply filter scheme. The MPC9773 frequency and phase stability is most susceptible to noise with spectral content in the 100-kHz to 20-MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 8 mA (13.5 mA maximum), assuming that a minimum of 3.0 V must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 7 must have a resistance of 5–10 Ω to meet the voltage drop criteria.

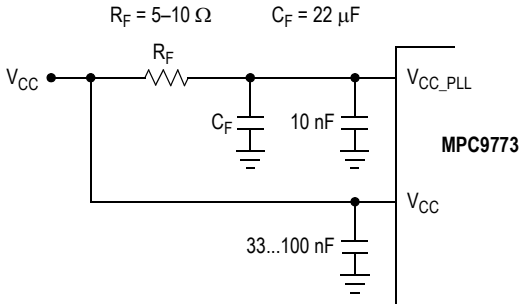


Figure 7. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7, the filter cut-off frequency is around 4.5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9773 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9773 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9773. Designs using the MPC9773 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9773 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9773 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9773 are connected together, the maximum overall timing uncertainty from the common CCLKx input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} * CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay, and I/O (phase) jitter:

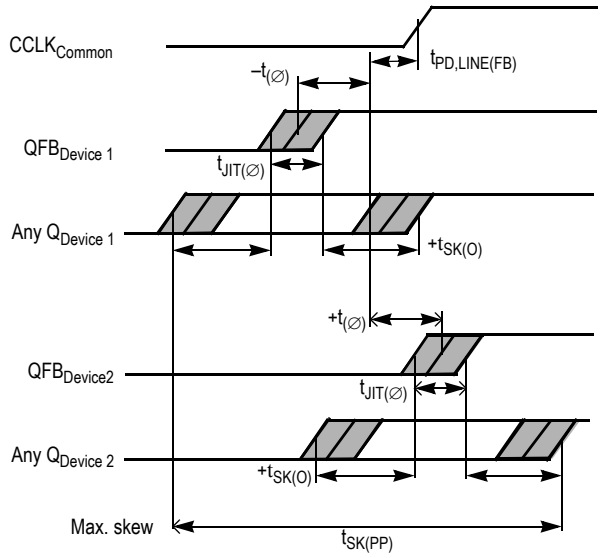


Figure 8. MPC9773 Maximum Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 12.

Table 12. Confidence Factor CF

CF	Probability of Clock Edge within the Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device.

Due to the frequency dependence of the static phase offset and I/O jitter, using Figure 9 to Figure 11 to predict a maximum I/O jitter and the specified $t_{(\varnothing)}$ parameter relative to the input reference frequency results in a precise timing performance analysis.

In the following example calculation an I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst-case timing uncertainty from the common input reference clock to any output of –455 ps to +455 ps relative to CCLK (PLL feedback = ÷8, reference frequency = 50 MHz, VCO frequency = 400 MHz, I/O jitter = 13 ps RMS max., static phase offset $t_{(\varnothing)}$ = ± 166 ps):

$$t_{SK(PP)} = [–166ps...166ps] + [–250ps...250ps] + [(13ps \cdot –3)...(13ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–455ps...455ps] + t_{PD,\ LINE(FB)}$$

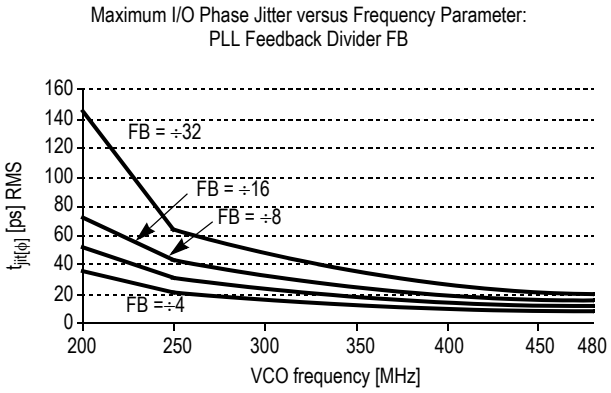


Figure 9. MPC9772 I/O Jitter

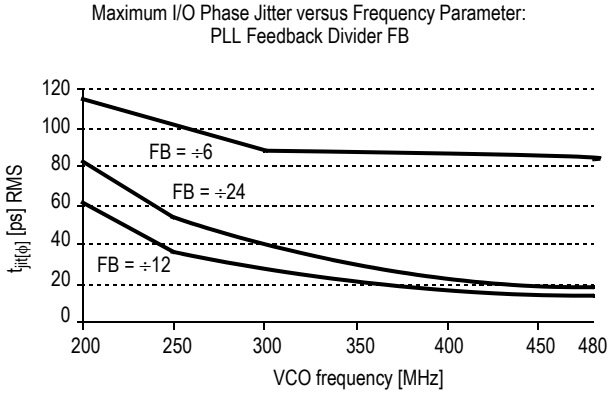


Figure 10. MPC9772 I/O Jitter

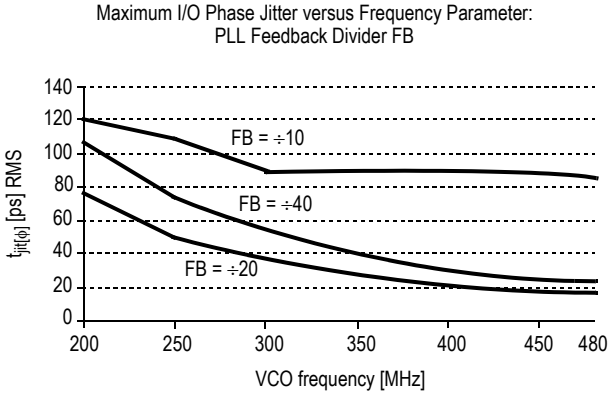


Figure 11. MPC9772 I/O Jitter

Driving Transmission Lines

The MPC9773 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high-performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50-Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9773 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 12 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9773 clock driver is effectively doubled due to its capability to drive multiple lines.

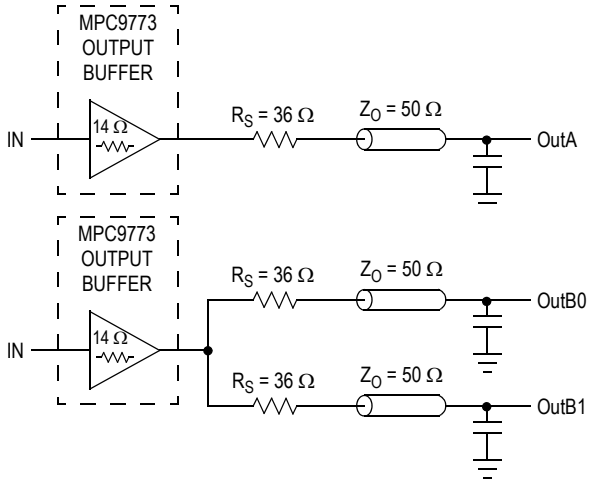


Figure 12. Single versus Dual Transmission Lines

The waveform plots in Figure 13 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9773 output buffer is more than sufficient to drive 50-Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9773. The output waveform in Figure 13 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36-Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$
$Z_0 = 50\ \Omega \parallel 50\ \Omega$
$R_S = 36\ \Omega \parallel 36\ \Omega$
$R_0 = 14\ \Omega$
$V_L = 3.0\ (25 \div (18+17+25)$
$= 1.31\ V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

1. Final skew data pending specification.

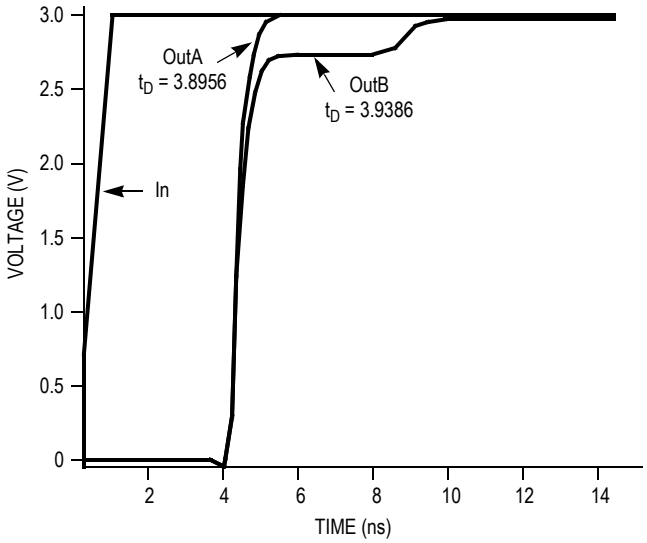
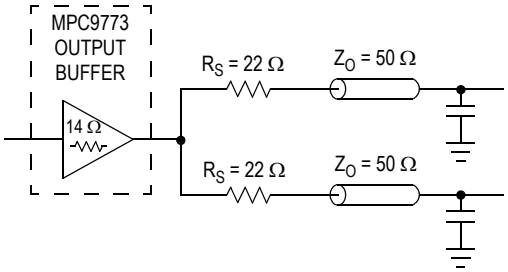


Figure 13. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 14 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\ \Omega + 22\ \Omega \parallel 22\ \Omega = 50\ \Omega \parallel 50\ \Omega$
$25\ \Omega = 25\ \Omega$

Figure 14. Optimized Dual Line Termination

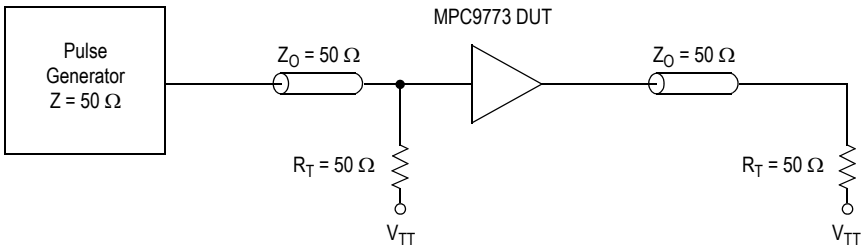


Figure 15. CCLK MPC9773 AC Test Reference

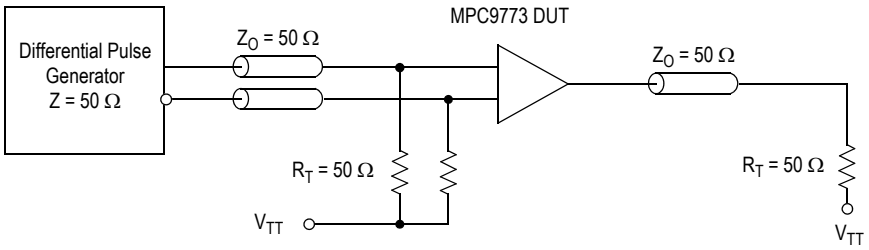
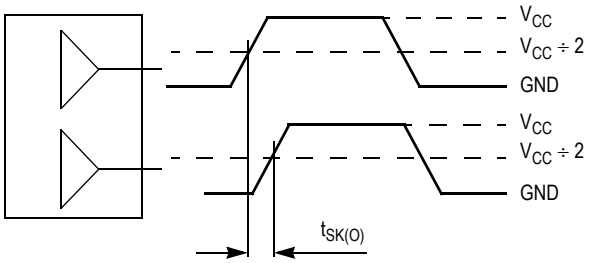


Figure 16. PCLK MPC9773 AC Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 17. Output-to-Output Skew $t_{SK(O)}$

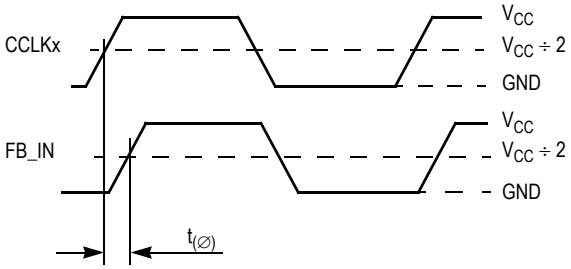
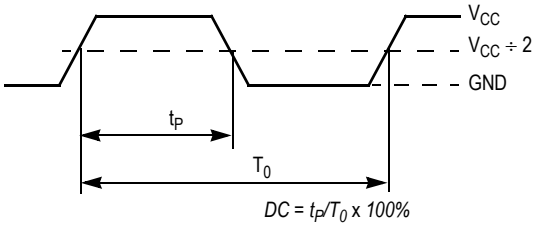
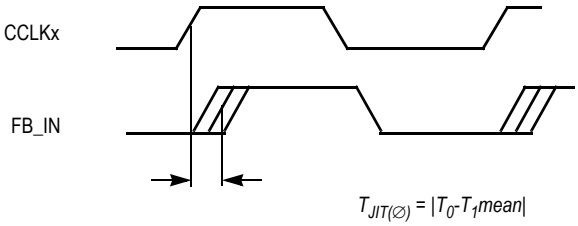


Figure 18. Propagation Delay ($t_{(\varnormal)}$, Static Phase Offset) Test Reference



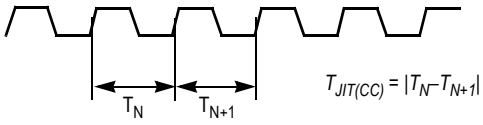
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 19. Output Duty Cycle (DC)



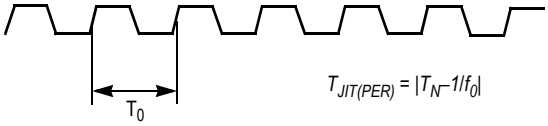
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 20. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 21. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 22. Period Jitter

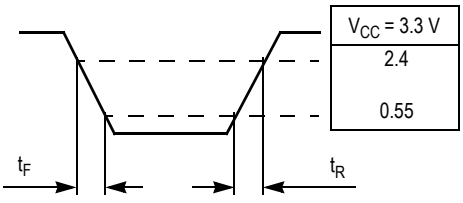


Figure 23. Output Transition Time Test Reference

Order number: MPC97H73
Rev 1, 08/2004

3.3V 1:12 LVCMOS PLL Clock Generator

MPC97H73

3.3V 1:12 LVCMOS PLL CLOCK GENERATOR

FA SUFFIX
52 LEAD LQFP PACKAGE
CASE 848D-03

The MPC97H73 is a 3.3V compatible, 1:12 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance networking, computing and telecom applications. With output frequencies up to 240 MHz and output skews less than 250 ps the device meets the needs of the most demanding clock applications.

Features

- 1:12 PLL based low-voltage clock generator
- 3.3V power supply
- Internal power-on reset
- Generates clock signals up to 240 MHz
- Maximum output skew of 250 ps
- Differential PECL reference clock input
- Two LVCMOS PLL reference clock inputs
- External PLL feedback supports zero-delay capability
- Various feedback and output dividers (see application section)
- Supports up to three individual generated output clock frequencies
- Synchronous output clock stop circuitry for each individual output for power down support
- Drives up to 24 clock lines
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC973
- 52-lead Pb-free Package Available

Functional Description

The MPC97H73 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC97H73 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC97H73 features an extensive level of frequency programmability between the 12 outputs as well as the output to input relationships, for instance 1:1, 2:1, 3:1, 3:2, 4:1, 4:3, 5:1, 5:2, 5:3, 5:4, 5:6, 6:1, 8:1, and 8:3.

The QSYNC output will indicate when the coincident rising edges of the above relationships will occur. The selectability of the feedback frequency is independent of the output frequencies. This allows for very flexible programming of the input reference versus output frequency relationship. The output frequencies can be either odd or even multiples of the input reference. In addition the output frequency can be less than the input frequency for applications where a frequency needs to be reduced by a non—binary factor. The MPC97H73 also supports the 180° phase shift of one of its output banks with respect to the other output banks. The QSYNC outputs reflects the phase relationship between the QA and QC outputs and can be used for the generation of system baseline timing signals.

The REF_SEL pin selects the LVPECL or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The outputs can be individually disabled (stopped in logic low state) by programming the serial CLOCK_STOP interface of the MPC97H73. The MPC97H73 has an internal power-on reset.

The MPC97H73 is fully 3.3V compatible and requires no external loop filter components. All inputs (except PCLK) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC97H73 outputs can drive one or two traces giving the devices an effective fanout of 1:24. The device is pin and function compatible to the MPC973 and is packaged in a 52-lead LQFP package.

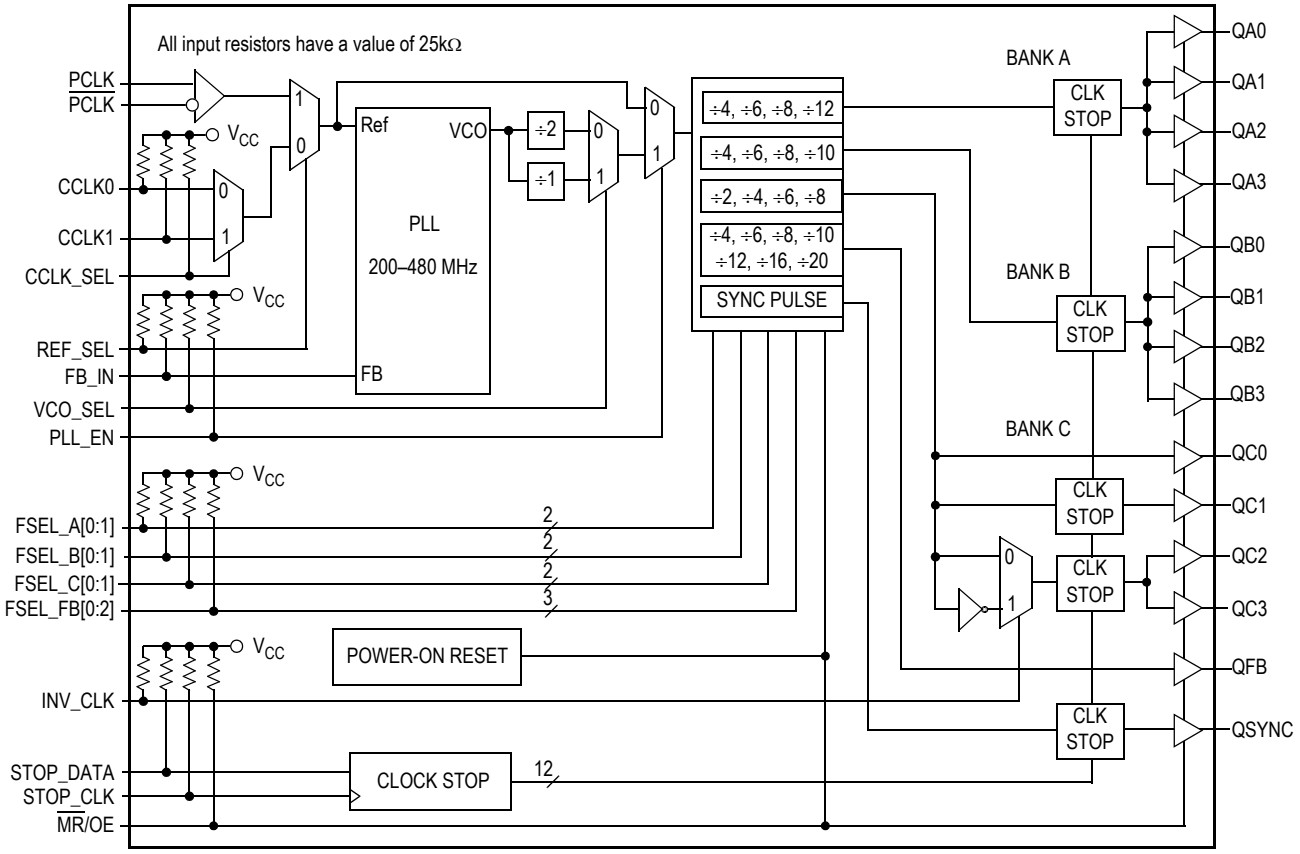


Figure 1. MPC97H73 Logic Diagram

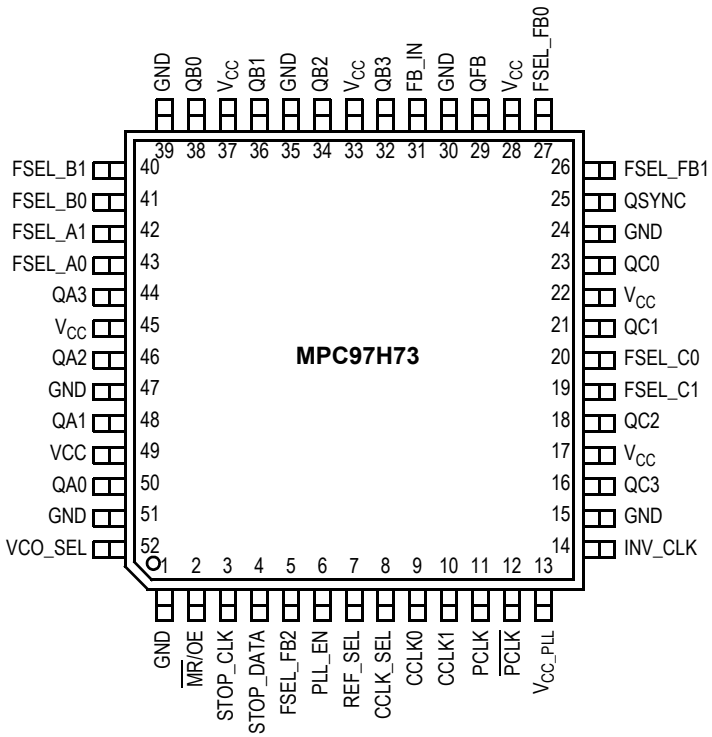


Figure 2. MPC97H73 52-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK0	Input	LVCMOS	PLL reference clock
CCLK1	Input	LVCMOS	Alternative PLL reference clock
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	Differential LVPECL reference clock
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to an QFB
CCLK_SEL	Input	LVCMOS	LVCMOS clock reference select
REF_SEL	Input	LVCMOS	LVCMOS/PECL reference clock select
VCO_SEL	Input	LVCMOS	VCO operating frequency select
PLL_EN	Input	LVCMOS	PLL enable/PLL bypass mode select
$\overline{\text{MR}}$/OE	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
FSEL_A[0:1]	Input	LVCMOS	Frequency divider select for bank A outputs
FSEL_B[0:1]	Input	LVCMOS	Frequency divider select for bank B outputs
FSEL_C[0:1]	Input	LVCMOS	Frequency divider select for bank C outputs
FSEL_FB[0:2]	Input	LVCMOS	Frequency divider select for the QFB output
INV_CLK	Input	LVCMOS	Clock phase selection for outputs QC2 and QC3
STOP_CLK	Input	LVCMOS	Clock input for clock stop circuitry
STOP_DATA	Input	LVCMOS	Configuration data input for clock stop circuitry
QA[0-3]	Output	LVCMOS	Clock outputs (Bank A)
QB[0-3]	Output	LVCMOS	Clock outputs (Bank B)
QC[0-3]	Output	LVCMOS	Clock outputs (Bank C)
QFB	Output	LVCMOS	PLL feedback output. Connect to FB_IN.
QSYNC	Output	LVCMOS	Synchronization pulse output
GND	Supply	Ground	Negative power supply
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table (Configuration Controls)

Control	Default	0	1
REF_SEL	1	Selects CCLKx as the PLL reference clock	Selects the LVPECL inputs as the PLL reference clock
CCLK_SEL	1	Selects CCLK0	Selects CCLK1
VCO_SEL	1	Selects VCO÷2. The VCO frequency is scaled by a factor of 2 (low VCO frequency range).	Selects VCO÷1. (high VCO frequency range)
PLL_EN	1	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC97H73 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
INV_CLK	1	QC2 and QC3 are in phase with QC0 and QC1	QC2 and QC3 are inverted (180° phase shift) with respect to QC0 and QC1
$\overline{\text{MR}}$/OE	1	Outputs disabled (high-impedance state) and device is reset. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC97H73 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). The device is reset by the internal power-on reset (POR) circuitry during power-up.	Outputs enabled (active)

VCO_SEL, FSEL_A[0:1], FSEL_B[0:1], FSEL_C[0:1], FSEL_FB[0:2] control the operating PLL frequency range and input/output frequency ratios. See Table 3 to Table 6 and the APPLICATIONS INFORMATION for supported frequency ranges and output to input frequency ratios.

Table 3. Output Divider Bank A (N_A)

VCO_SEL	FSEL_A1	FSEL_A0	QA[0:3]
0	0	0	VCO÷8
0	0	1	VCO÷12
0	1	0	VCO÷16
0	1	1	VCO÷24
1	0	0	VCO÷4
1	0	1	VCO÷6
1	1	0	VCO÷8
1	1	1	VCO÷12

Table 4. Output Divider Bank B (N_B)

VCO_SEL	FSEL_B1	FSEL_B0	QB[0:3]
0	0	0	VCO÷8
0	0	1	VCO÷12
0	1	0	VCO÷16
0	1	1	VCO÷20
1	0	0	VCO÷4
1	0	1	VCO÷6
1	1	0	VCO÷8
1	1	1	VCO÷10

Table 5. Output Divider Bank C (N_C)

VCO_SEL	FSEL_C1	FSEL_C0	QC[0:3]
0	0	0	VCO÷4
0	0	1	VCO÷8
0	1	0	VCO÷12
0	1	1	VCO÷16
1	0	0	VCO÷2
1	0	1	VCO÷4
1	1	0	VCO÷6
1	1	1	VCO÷8

Table 6. Output Divider PLL Feedback (M)

VCO_SEL	FSEL_FB2	FSEL_FB1	FSEL_FB0	QFB
0	0	0	0	VCO÷8
0	0	0	1	VCO÷12
0	0	1	0	VCO÷16
0	0	1	1	VCO÷20
0	1	0	0	VCO÷16
0	1	0	1	VCO÷24
0	1	1	0	VCO÷32
0	1	1	1	VCO÷40
1	0	0	0	VCO÷4
1	0	0	1	VCO÷6
1	0	1	0	VCO÷8
1	0	1	1	VCO÷10
1	1	0	0	VCO÷8
1	1	0	1	VCO÷12
1	1	1	0	VCO÷16
1	1	1	1	VCO÷20

Table 7. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		12		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 8. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 9. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0° to 70°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{CC_PLL}	PLL Supply Voltage		3.0		V_{CC}	V	LVCMOS
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage				0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK, $\overline{PCLK}$	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH}=–24 mA[2]
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL}= 24 mA I_{OL}= 12 mA
Z_{OUT}	Output Impedance			8 – 11		Ω	
I_{IN}	Input Current[3]				±200	µA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current			8.0	13.5	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current				35	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC97H73 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
3. Inputs have pull-down resistors affecting the input current.

Table 10. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0° to +70°C)[1] [2]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Reference Frequency	÷4 feedback	50.0		120.0	MHz	PLL locked
		÷6 feedback	33.3		80.0	MHz	
		÷8 feedback	25.0		60.0	MHz	
		÷10 feedback	20.0		48.0	MHz	
		÷12 feedback	16.6		40.0	MHz	
		÷16 feedback	12.5		30.0	MHz	
		÷20 feedback	10.0		24.0	MHz	
		÷24 feedback	8.33		20.0	MHz	
		÷32 feedback	6.25		15.0	MHz	
		÷40 feedback	5.00		12.0	MHz	
	Input Reference Frequency in PLL Bypass Mode				250	MHz	PLL bypass
f_{VCO}	VCO Frequency Range[3]		200		480	MHz	
f_{MAX}	Output Frequency	÷2 output	100.0		240.0	MHz	PLL locked
		÷4 output	50.0		120.0	MHz	
		÷6 output	33.3		80.0	MHz	
		÷8 output	25.0		60.0	MHz	
		÷10 output	20.0		48.0	MHz	
		÷12 output	16.6		40.0	MHz	
		÷16 output	12.5		30.0	MHz	
		÷20 output	10.0		24.0	MHz	
		÷24 output	8.33		20.0	MHz	
f_{STOP_CLK}	Serial Interface Clock Frequency				20	MHz	
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	400		1000	mV	LVPECL
V_{CMR}	Common Mode Range	PCLK, $\overline{PCLK}$	1.2		V_{CC}–0.9	V	LVPECL
$t_{PW,MIN}$	Input Reference Pulse Width[4]		2.0			ns	
t_R, t_F	CCLKx Input Rise/Fall Time[5]				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)[6]						PLL locked
	6.25 MHz < f_{REF} < 65.0 MHz		–3		+3	°	
	65.0 MHz < f_{REF} < 125 MHz		–4		+4	°	
	f_{REF}=50 MHz and feedback=÷8		–166		+166	ps	
$t_{SK(O)}$	Output-to-Output Skew[7]	within QA outputs			100	ps	
		within QB outputs			100	ps	
		within QC outputs			100	ps	
		all outputs			250	ps	
DC	Output Duty Cycle[8]		(T÷2) - 200	T÷2	(T÷2) +200	ps	
t_R, t_F	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				8.0	ns	
$t_{PZL, LZ}$	Output Enable Time				8.0	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle jitter[9]			150	200	ps	
$t_{JIT(PER)}$	Period Jitter[10]				150	ps	

Table 10. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0° to +70°C)[1] [2] **(Continued)**

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)[11]	÷4 feedback			11	ps	(VCO=400 MHz)
		÷6 feedback			86	ps	
		÷8 feedback			13	ps	
		÷10 feedback			88	ps	
		÷12 feedback			16	ps	
		÷16 feedback			19	ps	
		÷20 feedback			21	ps	
		÷24 feedback			22	ps	
		÷32 feedback			27	ps	
		÷40 feedback			30	ps	
BW	PLL Closed Loop Bandwidth[12]	÷4 feedback		1.20 – 3.50		MHz	
		÷6 feedback		0.70 – 2.50		MHz	
		÷8 feedback		0.50 – 1.80		MHz	
		÷10 feedback		0.45 – 1.20		MHz	
		÷12 feedback		0.30 – 1.00		MHz	
		÷16 feedback		0.25 – 0.70		MHz	
		÷20 feedback		0.20 – 0.55		MHz	
		÷24 feedback		0.17 – 0.40		MHz	
		÷32 feedback		0.12 – 0.30		MHz	
		÷40 feedback		0.11 – 0.28		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

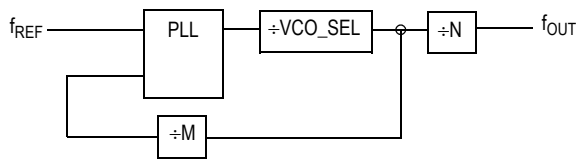
1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. The input reference frequency must match the VCO lock range divided by the feedback divider ratio: $f_{REF} = f_{VCO} \div (M \cdot VCO\_SEL)$.
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
4. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% - DC_{REF,\ MIN}$.
5. The MPC97H73 will operate with input rise/fall times up to 3.0 ns, but the A.C. characteristics, specifically $t_{(\varnothing)}$, $t_{PW,MIN}$, DC and f_{MAX} can only be guaranteed if t_R, t_F are within the specified range.
6. CCLKx or PCLK to FB_IN. Static phase offset depends on the reference frequency. $t_{(\varnothing)}$ [s] = $t_{(\varnothing)}$ [°] ÷ ($f_{REF} \cdot 360°$).
7. Excluding QSYNC output. See application section for part-to-part skew calculation.
8. Output duty cycle is DC = (0.5 ± 200 ps · f_{OUT}) . 100%. E.g. the DC range at f_{OUT}=100MHz is 48%<DC<52%. T = output period.
9. Cycle jitter is valid for all outputs in the same divider configuration. See APPLICATIONS INFORMATION for more details.
10. Period jitter is valid for all outputs in the same divider configuration. See APPLICATIONS INFORMATION for more details.
11. I/O jitter is valid for a VCO frequency of 400 MHz. See APPLICATIONS INFORMATION for I/O jitter vs. VCO frequency.
12. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

MPC97H73 Configurations

Configuring the MPC97H73 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$



where f_{REF} is the reference frequency of the selected input clock source (CCLKO, CCLK1 or PCLK), M is the PLL feedback divider and N is a output divider. The PLL feedback divider is configured by the FSEL_FB[2:0] and the output dividers are individually configured for each output bank by the FSEL_A[1:0], FSEL_B[1:0] and FSEL_C[1:0] inputs.

The reference frequency f_{REF} and the selection of the feedback-divider M is limited by the specified VCO frequency range. f_{REF} and M must be configured to match the VCO frequency range of 200 to 480 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \leq (f_{REF} \cdot VCO\_SEL \cdot M) \leq f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-one or a divide-by-two and can be used to situate the VCO into the specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio.

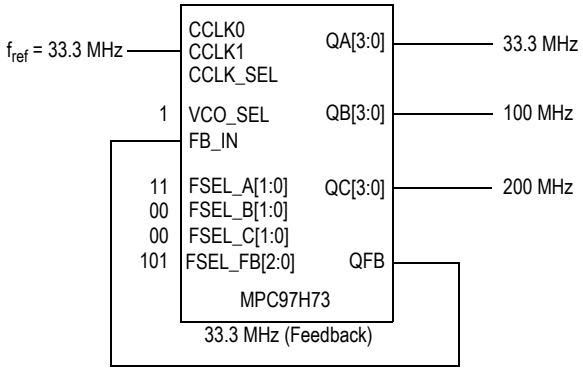
The output frequency for each bank can be derived from the VCO frequency and output divider:

$$f_{QA[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$
$$f_{QB[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$
$$f_{QC[0:3]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

Table 11. MPC97H73 Divider

Divider	Function	VCO_SEL	Values
M	PLL feedback FSEL_FB[0:3]	÷1	4, 6, 8, 10, 12, 16
		÷2	8, 12, 16, 20, 24, 32, 40
N_A	Bank A Output Divider FSEL_A[0:1]	÷1	4, 6, 8, 12
		÷2	8, 12, 16, 24
N_B	Bank B Output Divider FSEL_B[0:1]	÷1	4, 6, 8, 10
		÷2	8, 12, 16, 20
N_C	Bank C Output Divider FSEL_C[0:1]	÷1	2, 4, 6, 8
		÷2	4, 8, 12, 16

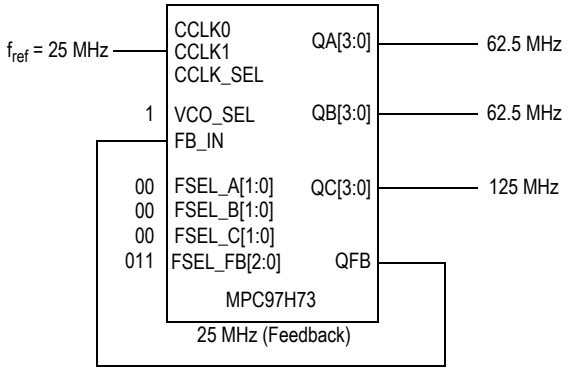
Table 11 shows the various PLL feedback and output dividers and Figure 3. Example Configuration and Figure 4. Example Configuration display example configurations for the MPC97H73:



MPC97H73 example configuration (feedback of QFB = 33.3 MHz, f_{VCO}=400 MHz, VCO_SEL=÷1, M=12, N_A=12, N_B=4, N_C=2).

Frequency Range	Min	Max
Input	16.6 MHz	40 MHz
QA Outputs	16.6 MHz	40 MHz
QA Outputs	50 MHz	120 MHz
QC Outputs	100 MHz	240 MHz

Figure 3. Example Configuration



MPC97H73 example configuration (feedback of QFB = 25 MHz, f_{VCO}=250 MHz, VCO_SEL=÷1, M=10, N_A=4, N_B=4, N_C=2).

Frequency Range	Min	Max
Input	20 MHz	48 MHz
QA Outputs	50 MHz	120 MHz
QA Outputs	50 MHz	120 MHz
QC Outputs	100 MHz	240 MHz

Figure 4. Example Configuration

MPC97H73 Individual Output Disable (Clock Stop) Circuitry

The individual clock stop (output enable) control of the MPC97H73 allows designers, under software control, to implement power management into the clock distribution design. A simple serial interface and a clock stop control logic provides a mechanism through which the MPC97H73 clock outputs can be individually stopped in the logic ‘0' state: The clock stop mechanism allows serial loading of a 12-bit serial input register. This register contains one programmable clock stop bit for 12 of the 14 output clocks. The QC0 and QFB outputs cannot be stopped (disabled) with the serial port.

The user can program an output clock to stop (disable) by writing logic ‘0' to the respective stop enable bit. Likewise, the user may programmably enable an output clock by writing logic ‘1' to the respective enable bit. The clock stop logic enables or disables clock outputs during the time when the output would be in normally in logic low state, eliminating the possibility of short or ‘runt' clock pulses.

The user can write to the serial input register through the STOP_DATA input by supplying a logic ‘0' start bit followed serially by 12 NRZ disable/enable bits. The period of each STOP_DATA bit equals the period of the free-running STOP_CLK signal. The STOP_DATA serial transmission should be timed so the MPC97H73 can sample each STOP_DATA bit with the rising edge of the free-running STOP_CLK signal. (See Figure 5. Clock Stop Circuit Programming.)

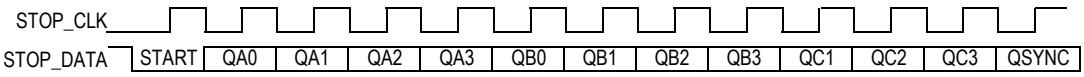


Figure 5. Clock Stop Circuit Programming

SYNC Output Description

The MPC97H73 has a system synchronization pulse output QSYNC. In configurations with the output frequency relationships are not integer multiples of each other QSYNC provides a signal for system synchronization purposes. The MPC97H73 monitors the relationship between the A bank and the B bank of outputs. The QSYNC output is asserted (logic low) one period in duration and one period prior to the coincident rising edges of the QA and QC outputs. The duration and the placement of the pulse is dependent QA and QC output frequencies: the QSYNC pulse width is equal to the period of the higher of the QA and QC output frequencies. Figure 6. QSYNC Timing Diagram shows various waveforms for the QSYNC output. The QSYNC output is defined for all possible combinations of the bank A and bank C outputs.

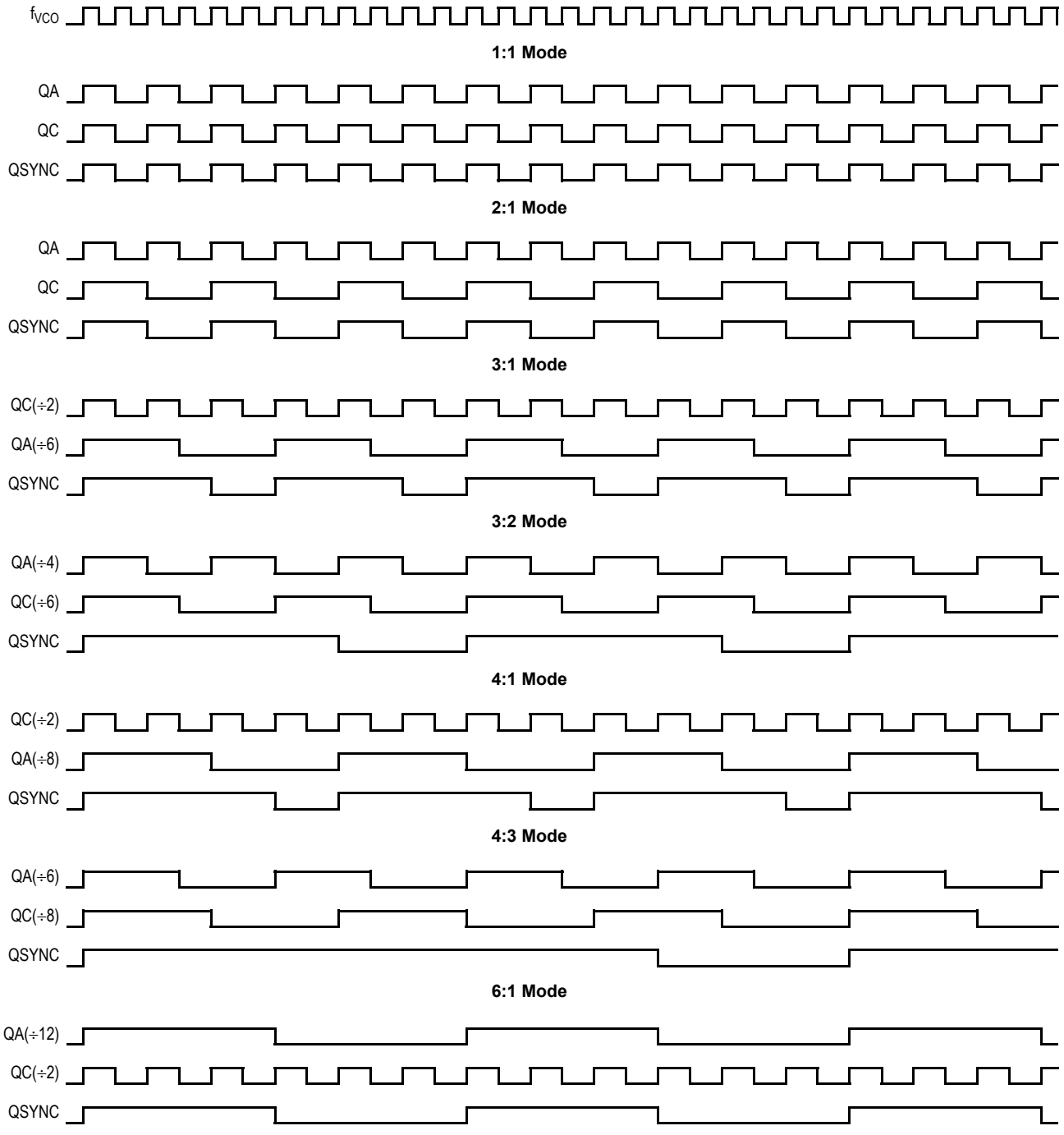


Figure 6. QSYNC Timing Diagram

Power Supply Filtering

The MPC97H73 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC97H73 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA_PLL} pin for the MPC97H73. Figure 7. VCC_PLL Power Supply Filter illustrates a typical power supply filter scheme. The MPC97H73 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 7. VCC_PLL Power Supply Filter must have a resistance of 5-10Ω to meet the voltage drop criteria.

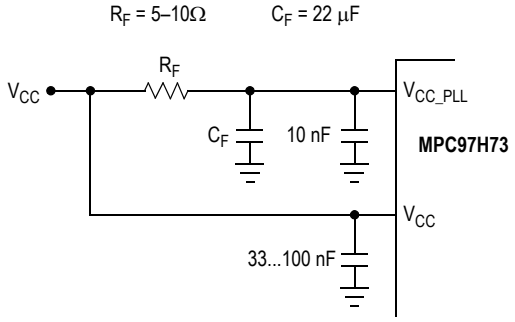


Figure 7. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 7. VCC_PLL Power Supply Filter, the filter cut-off frequency is around 4.5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC97H73 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC97H73 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC97H73. Designs using the MPC97H73 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC97H73 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC97H73 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC97H73 are connected together, the maximum overall timing uncertainty from the common CCLKx input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

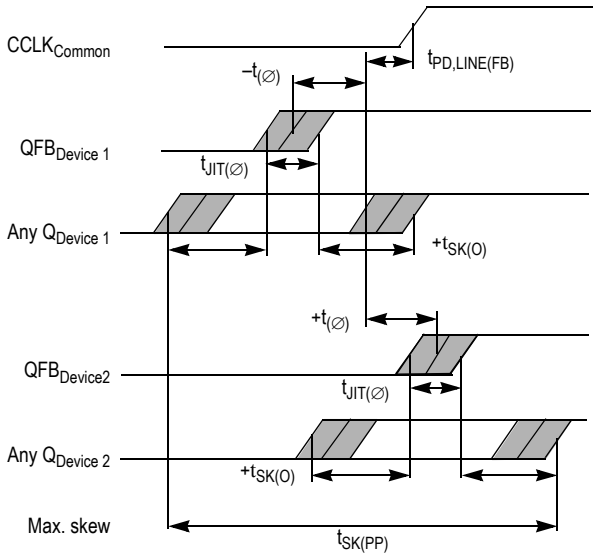


Figure 8. MPC97H73 Maximum Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 12.

Table 12. Confidence Factor CF

CF	Probability of Clock Edge within the Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device.

Due to the frequency dependence of the static phase offset and I/O jitter, using Figure 9. MPC97H73 I/O Jitter to Figure 11. MPC97H73 I/O Jitter to predict a maximum I/O jitter and the specified $t_{(\varnothing)}$ parameter relative to the input reference frequency results in a precise timing performance analysis.

In the following example calculation an I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from the common input reference clock to any output of –455 ps to +455 ps relative to CCLK (PLL feedback = ÷8, reference frequency = 50 MHz, VCO frequency = 400 MHz, I/O jitter = 13 ps rms max., static phase offset $t_{(\varnothing)}$ = ± 166 ps):

$t_{SK(PP)}$ = *[-166ps...166ps] + [-250ps...250ps] + [(13ps @ –3)...(13ps @ 3)] + $t_{PD, LINE(FB)}$*

$t_{SK(PP)}$ = *[-455ps...455ps] + $t_{PD, LINE(FB)}$*

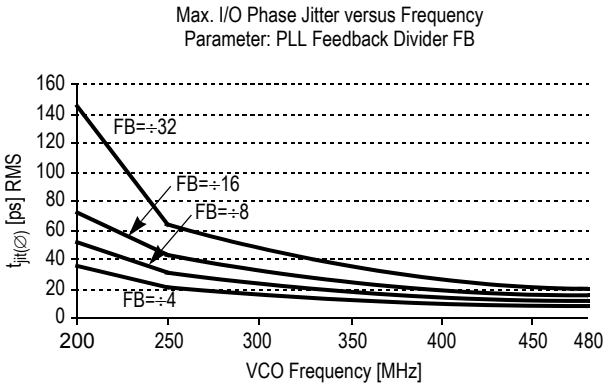


Figure 9. MPC97H73 I/O Jitter

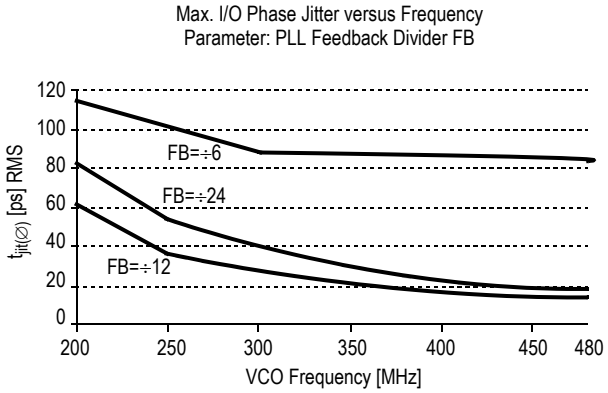


Figure 10. MPC97H73 I/O Jitter

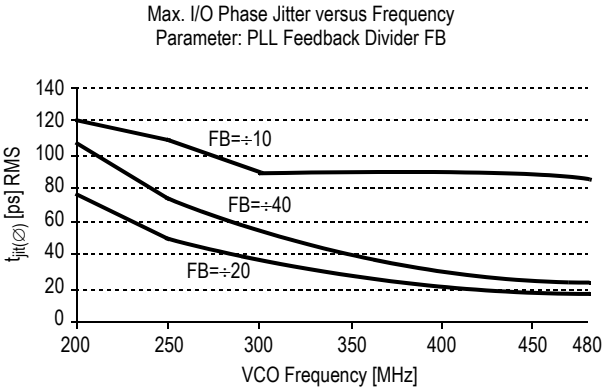


Figure 11. MPC97H73 I/O Jitter

Driving Transmission Lines

The MPC97H73 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC97H73 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 12. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC97H73 clock driver is effectively doubled due to its capability to drive multiple lines.

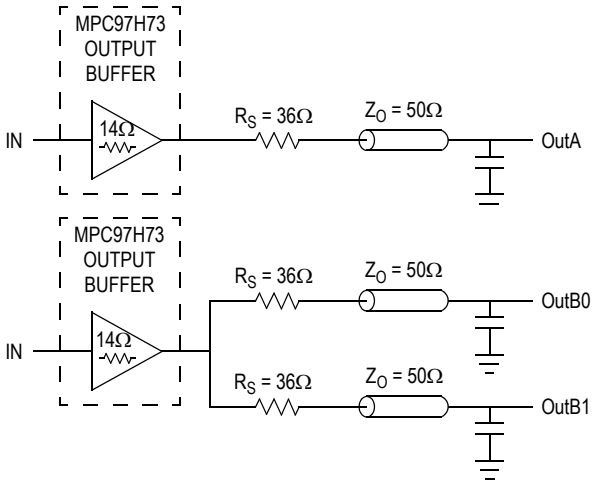


Figure 12. Single versus Dual Transmission Lines

The waveform plots in Figure 13. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC97H73 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC97H73. The output waveform in Figure 13. Single versus Dual Waveforms shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 (25 \div (18+17+25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

1. Final skew data pending specification

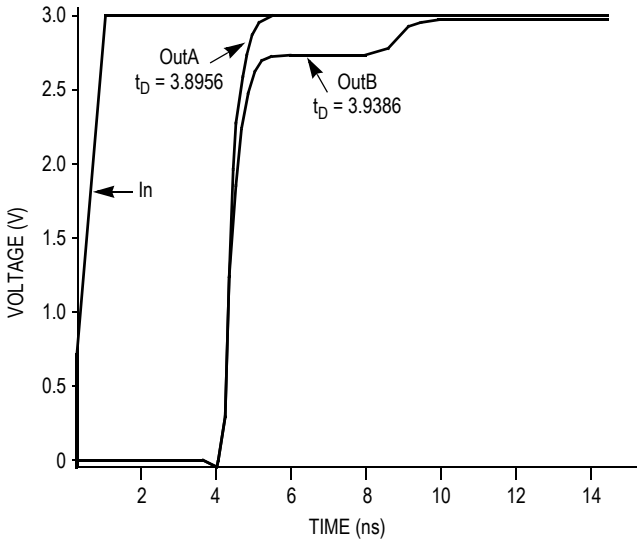
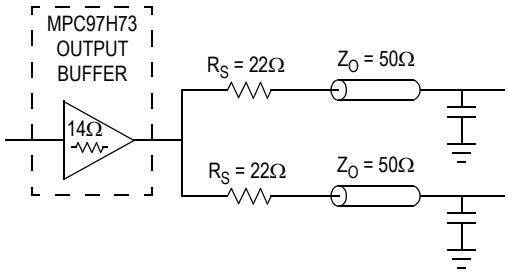


Figure 13. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 14. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$
$25\Omega = 25\Omega$

Figure 14. Optimized Dual Line Termination

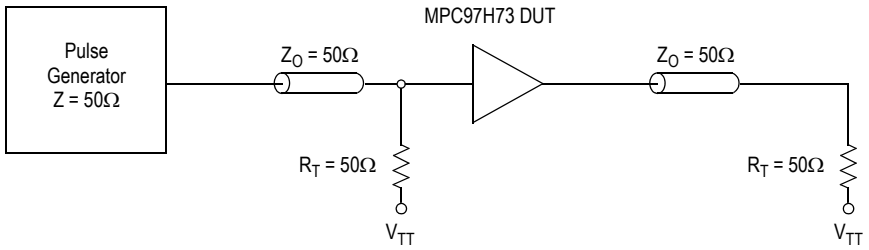


Figure 15. CCLK MPC97H73 AC Test Reference

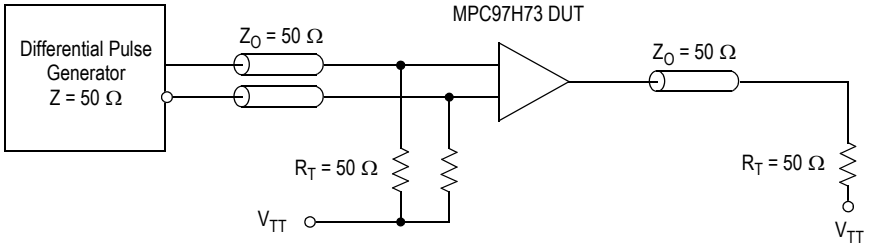
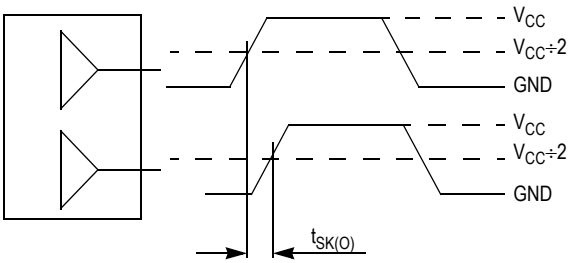


Figure 16. PCLK MPC97H73 AC Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 16. Output-to-Output Skew $t_{SK(O)}$

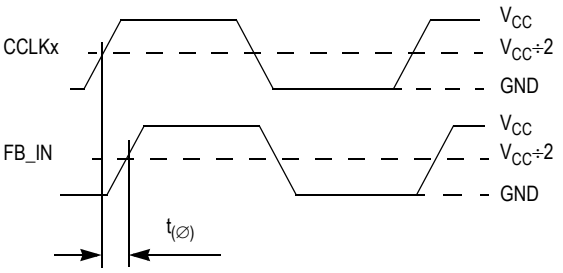
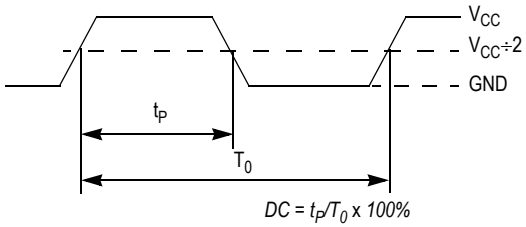
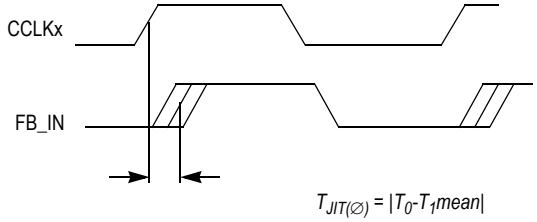


Figure 17. Propagation Delay ($t_{(\varnothing)}$, Static Phase Offset) Test Reference



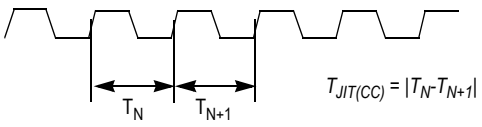
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 18. Output Duty Cycle (DC)



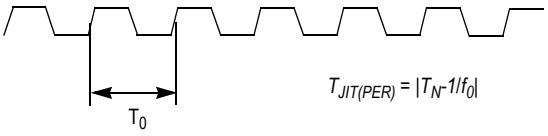
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 19. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 20. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 21. Period Jitter

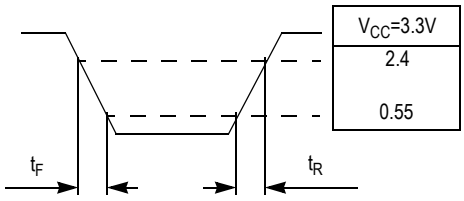


Figure 22. Output Transition Time Test Reference

Order number: MPC9774
Rev 3, 08/2004

3.3 V 1:14 LVCMOS PLL Clock Generator

MPC9774

3.3 V 1:14 LVCMOS PLL CLOCK GENERATOR

FA SUFFIX
52-LEAD LQFP PACKAGE
CASE 848D-03

The MPC9774 is a 3.3V compatible, 1:14 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance networking, computing and telecom applications. With output frequencies up to 125 MHz and output skews less than 175 ps the device meets the needs of the most demanding clock applications.

Features

- 1:14 PLL based low-voltage clock generator
- 3.3 V power supply
- Internal power-on reset
- Generates clock signals up to 125 MHz
- Maximum output skew of 175 ps
- Two LVCMOS PLL reference clock inputs
- External PLL feedback supports zero-delay capability
- Various feedback and output dividers (see APPLICATIONS INFORMATION)
- Supports up to three individual generated output clock frequencies
- Drives up to 28 clock lines
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC974
- 52-lead Pb-free Package Available

Functional Description

The MPC9774 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9774 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range.

The MPC9774 features frequency programmability between the three output banks outputs as well as the output to input relationships. Output frequency ratios of 1:1, 2:1, 3:1, 3:2 and 3:2:1 can be realized. Additionally, the device supports a separate configurable feedback output which allows for a wide variety of input/output frequency multiplication alternatives. The VCO_SEL pin provides an extended PLL input reference frequency range.

The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The MPC9774 has an internal power-on reset.

The MPC9774 is fully 3.3 V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9774 outputs can drive one or two traces giving the devices an effective fanout of 1:12. The device is pin and function compatible to the MPC974 and is packaged in a 52-lead LQFP package.

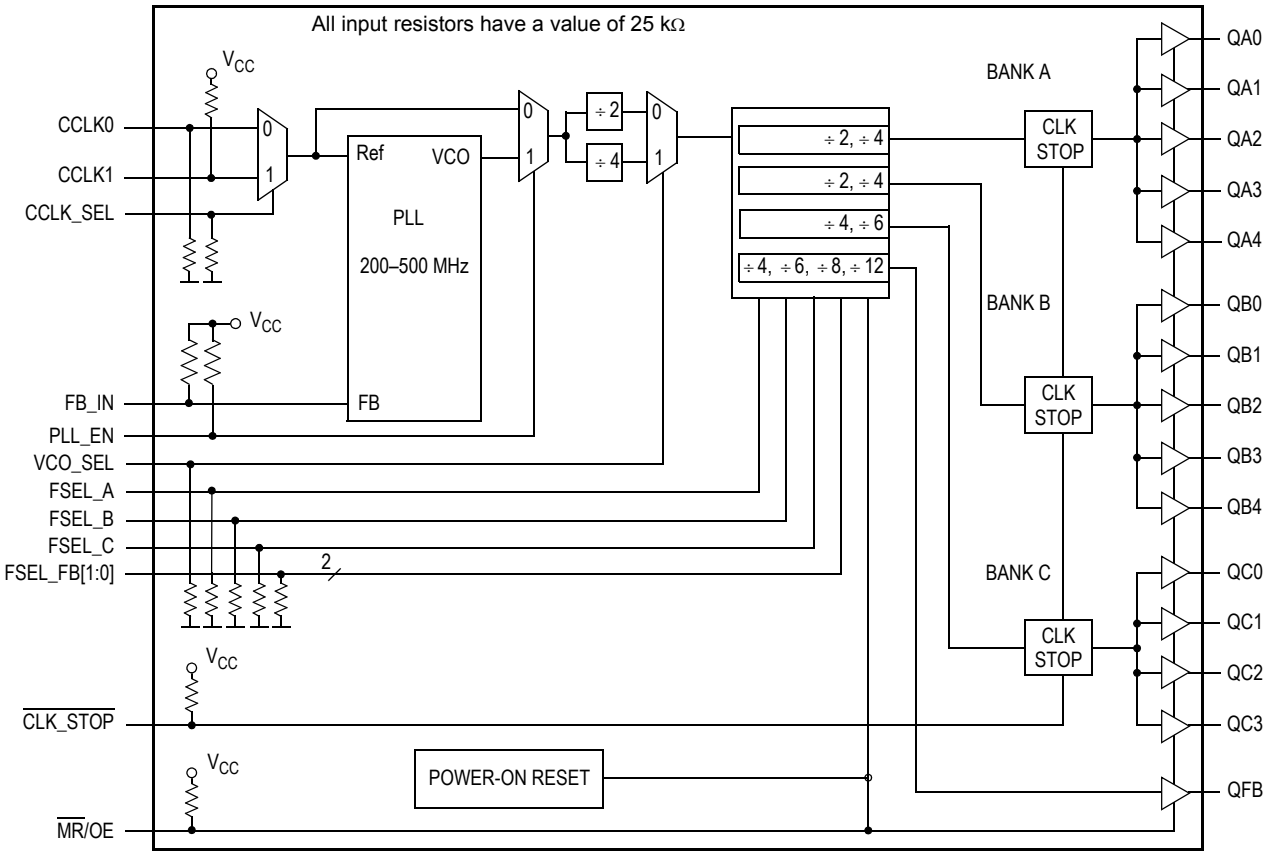


Figure 1. MPC9774 Logic Diagram

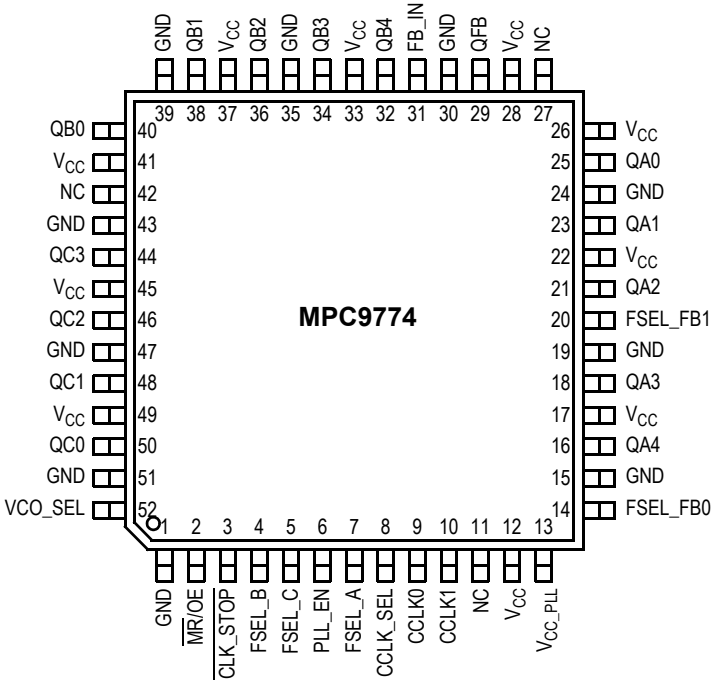


Figure 2. MPC9774 52-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK0	Input	LVCMOS	PLL reference clock
CCLK1	Input	LVCMOS	Alternative PLL reference clock
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to QFB
CCLK_SEL	Input	LVCMOS	LVCMOS clock reference select
VCO_SEL	Input	LVCMOS	VCO operating frequency select
PLL_EN	Input	LVCMOS	PLL enable/PLL bypass mode select
$\overline{\text{MR}}$/OE	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
$\overline{\text{CLK\_STOP}}$	Input	LVCMOS	Output enable/clock stop (logic low state)
FSEL_A	Input	LVCMOS	Frequency divider select for bank A outputs
FSEL_B	Input	LVCMOS	Frequency divider select for bank B outputs
FSEL_C	Input	LVCMOS	Frequency divider select for bank C outputs
FSEL_FB[1:0]	Input	LVCMOS	Frequency divider select for the QFB output
QA[4:0]	Output	LVCMOS	Clock outputs (Bank A)
QB[4:0]	Output	LVCMOS	Clock outputs (Bank B)
QC[3:0]	Output	LVCMOS	Clock outputs (Bank C)
QFB	Output	LVCMOS	PLL feedback output. Connect to FB_IN.
GND	Supply	Ground	Negative power supply
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin $V_{CC\_PLL.}$ Please see applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table (Configuration Controls)

Control	Default	0	1
CCLK_SEL	0	Selects CCLK0 as PLL references signal input	Selects CCKL1 as PLL reference signal input
VCO_SEL	0	Selects VCO ÷ 2. The VCO frequency is scaled by a factor of 2 (high input frequency range)	Selects VCO ÷ 4. The VCO frequency is scaled by a factor of 4 (low input frequency range).
PLL_EN	1	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9774 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
$\overline{\text{CLK\_STOP}}$	1	QA, QB an QC outputs disabled in logic low state. QFB is not affected by $\overline{\text{CLK\_STOP}}$. $\overline{\text{CLK\_STOP}}$ deassertion may cause the initial output clock pulse to be distorted.	Outputs enabled (active)
$\overline{\text{MR}}$/OE	1	Outputs disabled (high-impedance state) and reset of the device. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC9774 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). The device is reset by the internal power-on reset (POR) circuitry during power-up.	Outputs enabled (active)

VCO_SEL, FSEL_A, FSEL_B, FSEL_C and FSEL_FB[1:0] control the operating PLL frequency range and input/output frequency ratios. See Table 3 and Table 4 for the device frequency configuration.

Table 3. Function Table (Output Dividers Bank A, B, and C)

VCO_SEL	FSEL_A	QA[4:0]	VCO_SEL	FSEL_B	QB[4:0]	VCO_SEL	FSEL_C	QC[3:0]
0	0	VCO ÷ 4	0	0	VCO ÷ 4	0	0	VCO ÷ 8
0	1	VCO ÷ 8	0	1	VCO ÷ 8	0	1	VCO ÷ 12
1	0	VCO ÷ 8	1	0	VCO ÷ 8	1	0	VCO ÷ 16
1	1	VCO ÷ 16	1	1	VCO ÷ 16	1	1	VCO ÷ 24

Table 4. Function Table (QFB)

VCO_SEL	FSEL_B1	FSEL_B0	QFB
0	0	0	VCO ÷ 8
0	0	1	VCO ÷ 16
0	1	0	VCO ÷ 12
0	1	1	VCO ÷ 24
1	0	0	VCO ÷ 16
1	0	1	VCO ÷ 32
1	1	0	VCO ÷ 24
1	1	1	VCO ÷ 48

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} ÷ 2		V	
MM	ESD protection (Machine Model)	200			V	
HBM	ESD protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		12		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 6. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 7. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{CC_PLL}	PLL Supply Voltage	3.02		V_{CC}	V	LVCMOS
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance		14 – 17		Ω	
I_{IN}	Input Current[2]			±200	μA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		5.0	7.5	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current			8.0	mA	All V_{CC} Pins

1. The MPC9774 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
2. Inputs have pull-down or pull-up resistors affecting the input current.

Table 8. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Reference Frequency	÷ 8 feedback	25.0		62.5	MHz	PLL locked
		÷ 12 feedback	16.6		41.6	MHz	
		÷ 16 feedback	12.5		31.25	MHz	
		÷ 24 feedback	8.33		20.83	MHz	
		÷ 32 feedback	6.25		15.625	MHz	PLL bypass
		÷ 48 feedback	4.16		10.41	MHz	
	Input Reference Frequency in PLL Bypass Mode[2]				250	MHz	
f_{VCO}	VCO Frequency Range[3]		200		500	MHz	
f_{MAX}	Output Frequency	÷ 4 output	50.0		125.0	MHz	PLL locked
		÷ 8 output	25.0		62.5	MHz	
		÷ 12 output	16.6		41.6	MHz	
		÷ 16 output	12.5		31.25	MHz	
		÷ 24 output	8.33		20.83	MHz	
$t_{PW,MIN}$	Input Reference Pulse Width[4]		2.0			ns	
t_R, t_F	CCLKx Input Rise/Fall Time				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)[5] CCLKx to FB_IN (FB = ÷ 8 and f_{REF} = 50 MHz)		–250		+100	ps	PLL locked
$t_{SK(O)}$	Output-to-Output Skew[6]	within QA bank			100	ps	
		within QB bank			125	ps	
		within QC bank			100	ps	
		any output			175	ps	
DC	Output Duty Cycle		47	50	53	%	
t_R, t_F	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
t_{PZL}	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter[7]				90	ps	
$t_{JIT(PER)}$	Period Jitter[6]				90	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)[8]	FB = ÷ 8			15	ps	
		FB = ÷ 12			49	ps	
		FB = ÷ 16			18	ps	
		FB = ÷ 24			22	ps	
		FB = ÷ 32			26	ps	
		FB = ÷ 48			34	ps	
BW	PLL Closed Loop Bandwidth[9]	FB = ÷ 8		0.50 – 1.80		MHz	
		FB = ÷ 12		0.30 – 1.00		MHz	
		FB = ÷ 16		0.25 – 0.70		MHZ	
		FB = ÷ 24		0.17 – 0.40		MHz	
		FB = ÷ 32		0.12 – 0.30		MHz	
		FB = ÷ 48		0.07 – 0.20		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

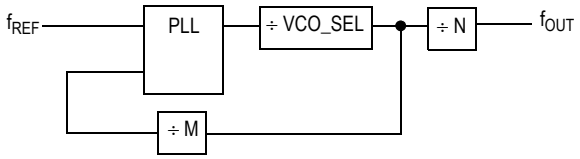
1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. In bypass mode, the MPC9774 divides the input reference clock.
3. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio (FB): $f_{REF} = f_{VCO} \div (M \cdot VCO\_SEL)$.
4. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% – DC_{REF,MIN}$. E.g. at f_{REF} = 62.5 MHz the input duty cycle range is 12.5% < DC < 87.5%.
5. Static phase offset depends on the reference frequency: $t_{(\varnothing)} = +50 \text{ ps} \pm (1 \div (120 \cdot f_{REF}))$ for any reference frequency.
6. Refer to Application section for part-to-part skew calculation.
7. Valid for all outputs at the same frequency.
8. I/O jitter for f_{VCO} = 400 MHz. Refer to APPLICATIONS INFORMATION for I/O jitter at other frequencies and for a jitter calculation for confidence factors other than 1 σ.
9. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

MPC9774 Configurations

Configuring the MPC9774 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \cdot M \div N$$



where f_{REF} is the reference frequency of the selected input clock source (CCLK0 or CCLK1), M is the PLL feedback divider and N is a output divider. M is configured by the FSEL_FB[0:1] and N is individually configured for each output bank by the FSEL_A, FSEL_B and FSEL_C inputs.

The reference frequency f_{REF} and the selection of the feedback-divider M is limited by the specified VCO frequency range. f_{REF} and M must be configured to match the VCO frequency range of 200 to 500 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \leq (f_{REF} \cdot VCO\_SEL \cdot M) \leq f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-two or a divide-by-four and can be used to situate the VCO into the specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio. The output frequency for each bank can be derived from the VCO frequency and output divider:

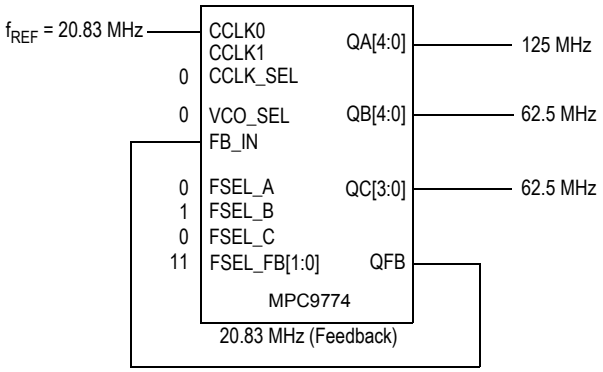
$$f_{QA[4:0]} = f_{VCO} \div (VCO\_SEL \cdot N_A)$$
$$f_{QB[4:0]} = f_{VCO} \div (VCO\_SEL \cdot N_B)$$
$$f_{QC[3:0]} = f_{VCO} \div (VCO\_SEL \cdot N_C)$$

Table 9. MPC9774 Divider

Divider	Function	VCO_SEL	Values
M	PLL Feedback FSEL_FB[0:1]	÷ 2	8, 12, 16, 24
		÷ 4	16, 24, 32, 48
N_A	Bank A Output Divider FSEL_A	÷ 2	4, 8
		÷ 4	8, 16
N_B	Bank B Output Divider FSEL_B	÷ 2	4, 8
		÷ 4	8, 16
N_C	Bank C Output Divider FSEL_C	÷ 2	8, 12
		÷ 4	16, 24

Table 9 shows the various PLL feedback and output dividers. The output dividers for the three output banks allow the user to configure the outputs into 1:1, 2:1, 3:2, and 3:2:1 frequency ratios. Figure 3 and Figure 4 display example configurations for the MPC9774.

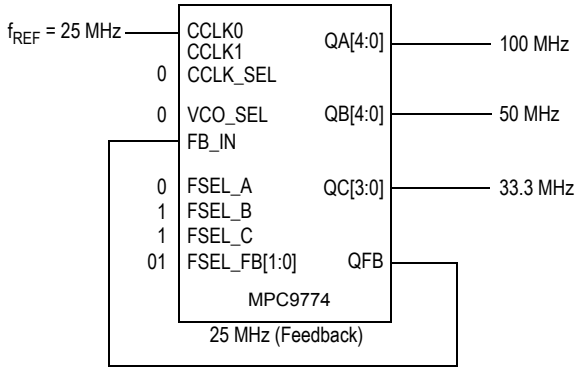
Figure 3. Example Configuration



MPC9774 example configuration (feedback of QFB = 20.83 MHz, VCO_SEL = ÷ 2, M = 12, N_A = 2, N_B = 4, N_C = 4, f_{VCO} = 500 MHz).

Frequency Range	Min	Max
Input	8.33 MHz	20.83 MHz
QA outputs	50 MHz	125 MHz
QB outputs	25 MHz	62.5 MHz
QC outputs	25 MHz	62.5 MHz

Figure 4. Example Configuration



MPC9774 example configuration (feedback of QFB = 25 MHz, VCO_SEL = ÷ 2, M = 8, N_A = 2, N_B = 4, N_C = 6, f_{VCO} = 400 MHz).

Frequency Range	Min	Max
Input	20 MHz	48 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	200 MHz

Using the MPC9774 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9774. Designs using the MPC9774 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback of the MPC9774 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9774 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9774 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

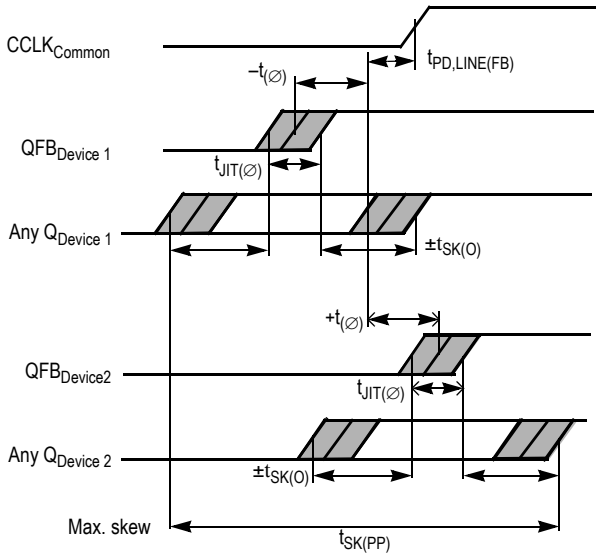


Figure 5. MPC9774 Maximum Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device.

Table 10. Confidence Factor CF

CF	Probability of Clock Edge within the Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

Due to the frequency dependence of the static phase offset and I/O jitter, using Figure 6 and Figure 7 to predict a maximum I/O jitter and the specified $t_{(\varnothing)}$ parameter relative to the input reference frequency results in a precise timing performance analysis.

In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from the common input reference clock to any output of –470 ps to +320 ps relative to CCLK (PLL feedback = ÷ 8, reference frequency = 50 MHz, VCO frequency = 400 MHz, I/O jitter = 15 ps RMS max., static phase offset $t_{(\varnothing)}$ = –250 ps to +100 ps):

$$t_{SK(PP)} = [–250\ ps...+100\ ps] + [-175\ ps...175\ ps] + [(15\ ps \bullet –3)...(15\ ps \bullet 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–470\ ps...+320\ ps] + t_{PD,\ LINE(FB)}$$

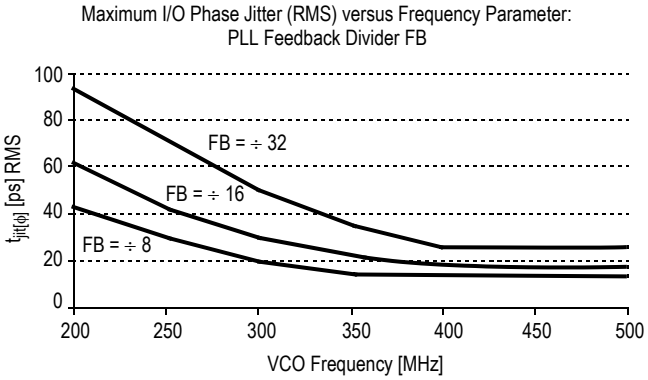


Figure 6. MPC9774 I/O Jitter

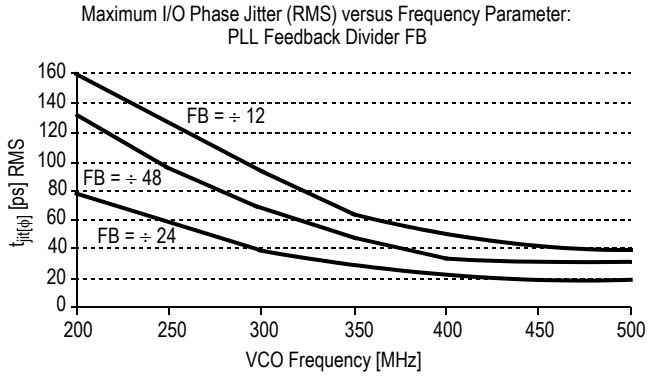


Figure 7. MPC9774 I/O Jitter

Driving Transmission Lines

The MPC9774 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9774 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 8 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9774 clock driver is effectively doubled due to its capability to drive multiple lines.

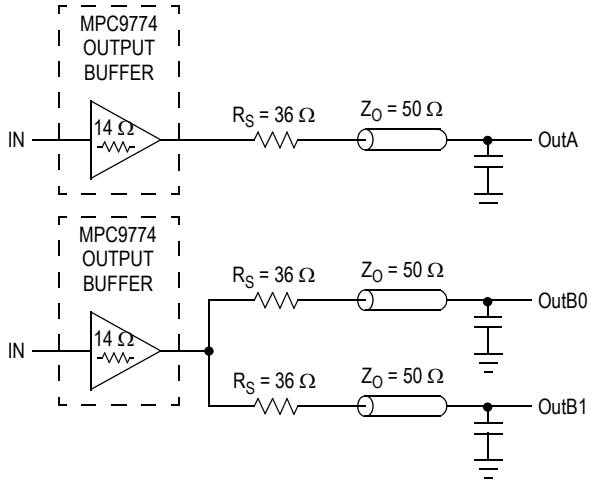


Figure 8. Single versus Dual Transmission Lines

The waveform plots in Figure 9 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9774 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9774. The output waveform in Figure 9 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$
$Z_0 = 50\ \Omega \parallel 50\ \Omega$
$R_S = 36\ \Omega \parallel 36\ \Omega$
$R_0 = 14\ \Omega$
$V_L = 3.0\ (25 \div (18 + 17 + 25)$
$= 1.31$ V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

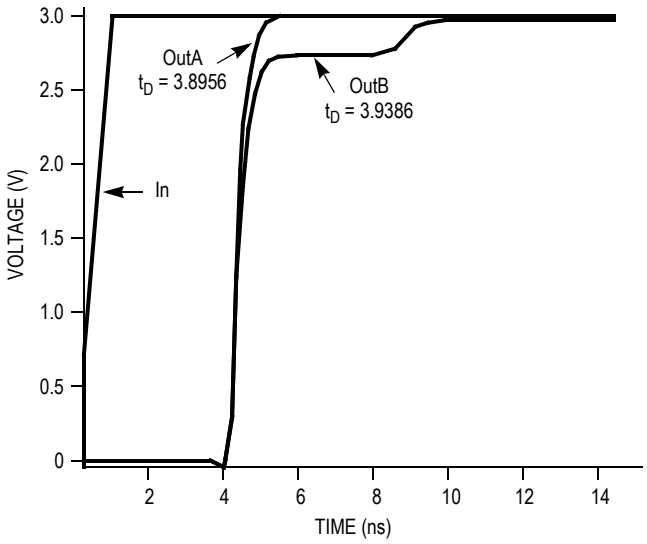
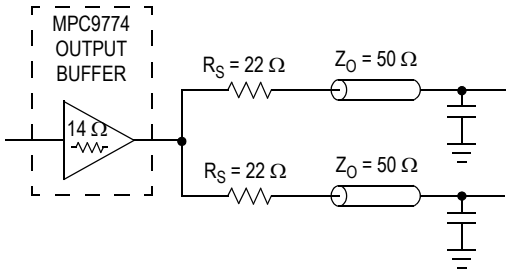


Figure 9. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 10 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\ \Omega + 22\ \Omega \parallel 22\ \Omega = 50\ \Omega \parallel 50\ \Omega$
$25\ \Omega = 25\ \Omega$

Figure 10. Optimized Dual Line Termination

Power Supply Filtering

The MPC9774 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9774 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9774. Figure 11 illustrates a typical power supply filter scheme. The MPC9774 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 5 mA (7.5 mA maximum), assuming that a minimum of 3.02 V (V_{CC_PLL}, min) must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 11 must have a resistance of 5–15 Ω to meet the voltage drop criteria.

The minimum values for RF and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example, RC filter shown in Figure 11, the filter cut-off frequency is around 3–5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

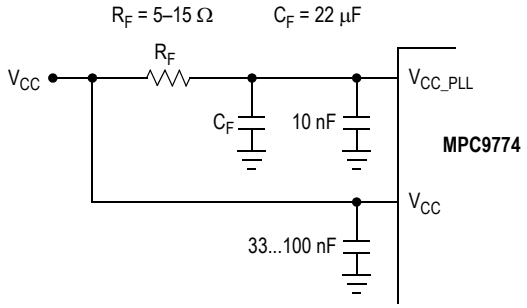


Figure 11. V_{CC_PLL} Power Supply Filter

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9774 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

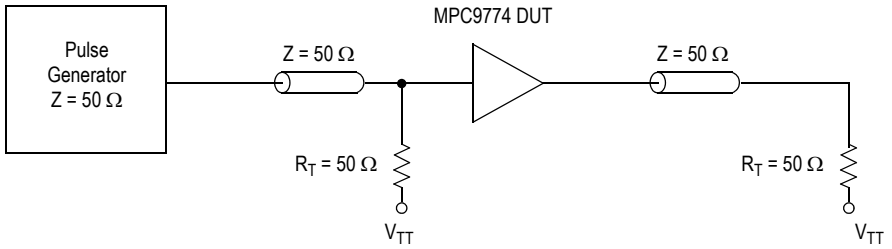
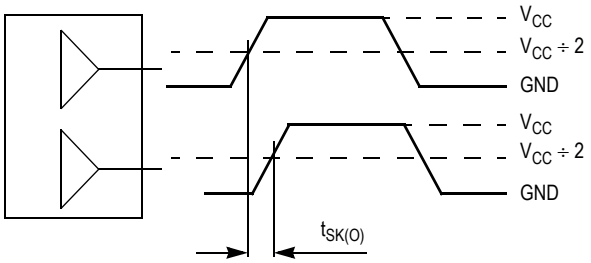


Figure 12. CCLK MPC9774 AC Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 13. Output-to-Output Skew $t_{SK(O)}$

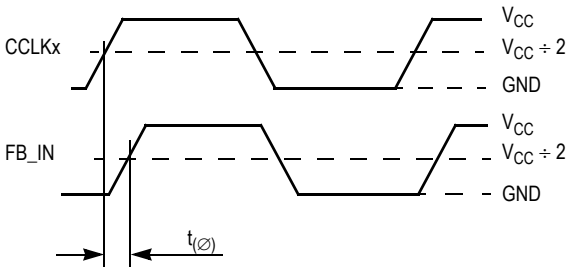
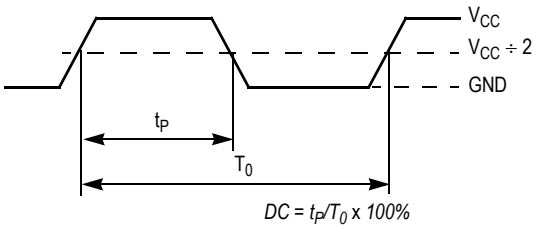
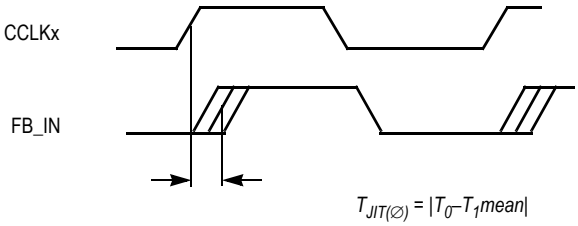


Figure 14. Propagation Delay ($t_{(\varnormal)}$, Static Phase Offset) Test Reference



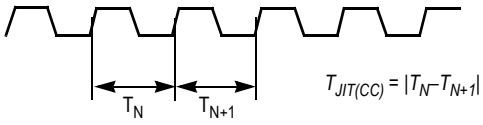
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 15. Output Duty Cycle (DC)



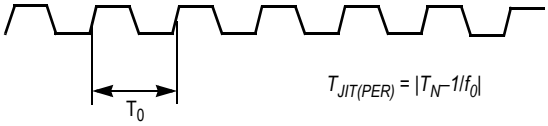
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 16. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 17. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 18. Period Jitter

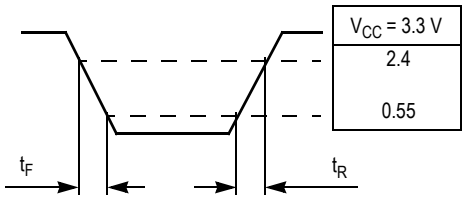


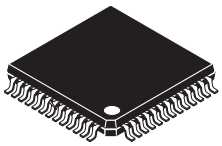
Figure 19. Output Transition Time Test Reference

Order number: MPC97H74
Rev 3, 08/2004

3.3 V 1:14 LVCMOS PLL Clock Generator

MPC97H74

3.3 V 1:14 LVCMOS PLL CLOCK GENERATOR



FA SUFFIX
52-LEAD LQFP PACKAGE
CASE 848D-03

The MPC97H74 is a 3.3 V compatible, 1:14 PLL based clock generator targeted for high performance low-skew clock distribution in mid-range to high-performance networking, computing and telecom applications. With output frequencies up to 125 MHz and output skews less than 175 ps the device meets the needs of the most demanding clock applications.

Features

- 1:14 PLL based low-voltage clock generator
- 3.3 V power supply
- Internal power-on reset
- Generates clock signals up to 125 MHz
- Maximum output skew of 175 ps
- Two LVCMOS PLL reference clock inputs
- External PLL feedback supports zero-delay capability
- Various feedback and output dividers (see application section)
- Supports up to three individual generated output clock frequencies
- Drives up to 28 clock lines
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC974
- 52-lead Pb-free Package Available

Functional Description

The MPC97H74 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC97H74 requires the connection of the PLL feedback output QFB to feedback input FB_IN to close the PLL feedback path. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range.

The MPC97H74 features frequency programmability between the three output bank outputs as well as the output to input relationships. Output frequency ratios of 1:1, 2:1, 3:1, 3:2, and 3:2:1 can be realized. Additionally, the device supports a separate configurable feedback output which allows for a wide variety of input/output frequency multiplication alternatives. The VCO_SEL pin provides an extended PLL input reference frequency range.

The REF_SEL pin selects the internal crystal oscillator or the LVCMOS compatible inputs as the reference clock signal. Two alternative LVCMOS compatible clock inputs are provided for clock redundancy support. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The MPC97H74 has an internal power-on reset.

The MPC97H74 is fully 3.3 V compatible and requires no external loop filter components. All inputs (except XTAL) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC97H74 outputs can drive one or two traces giving the devices an effective fanout of 1:28. The device is pin and function compatible to the MPC974 and is packaged in a 52-lead LQFP package.

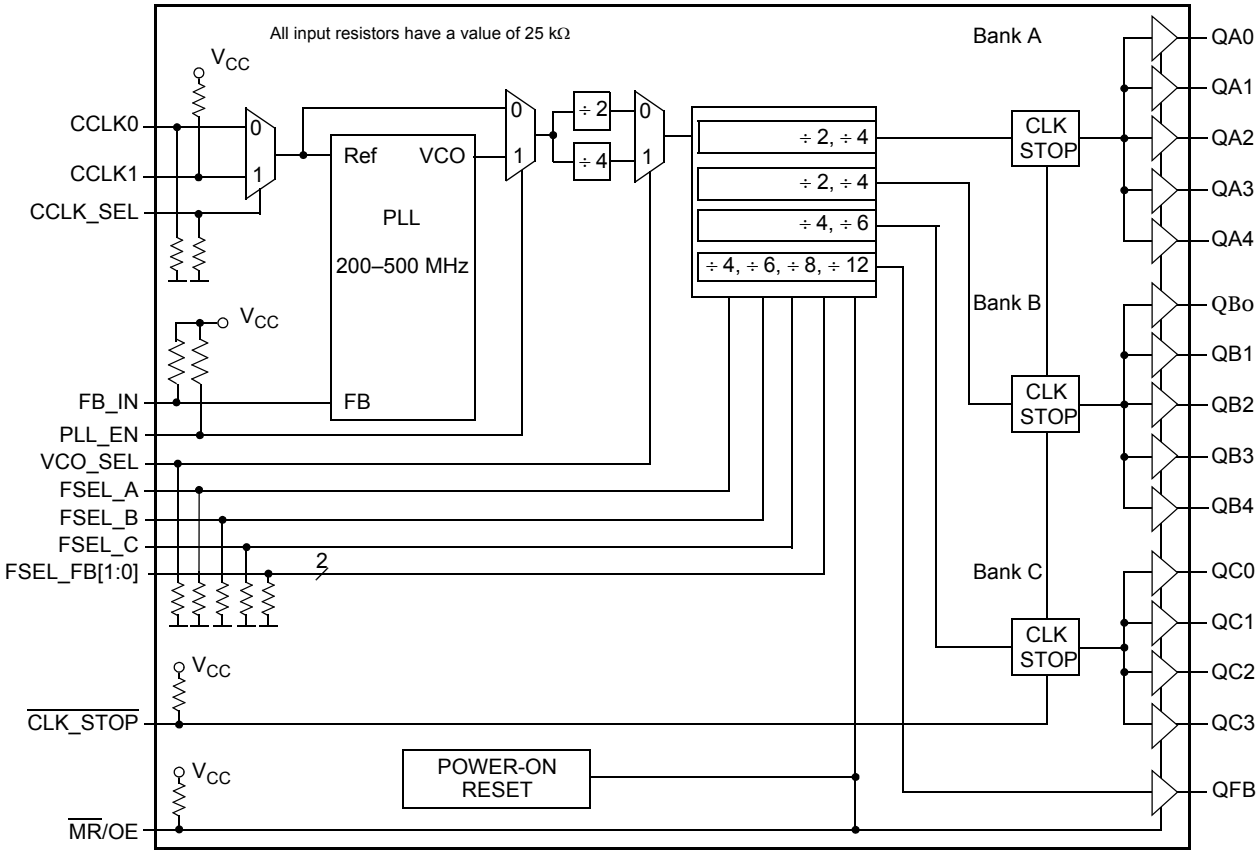


Figure 1. MPC97H74 Logic Diagram

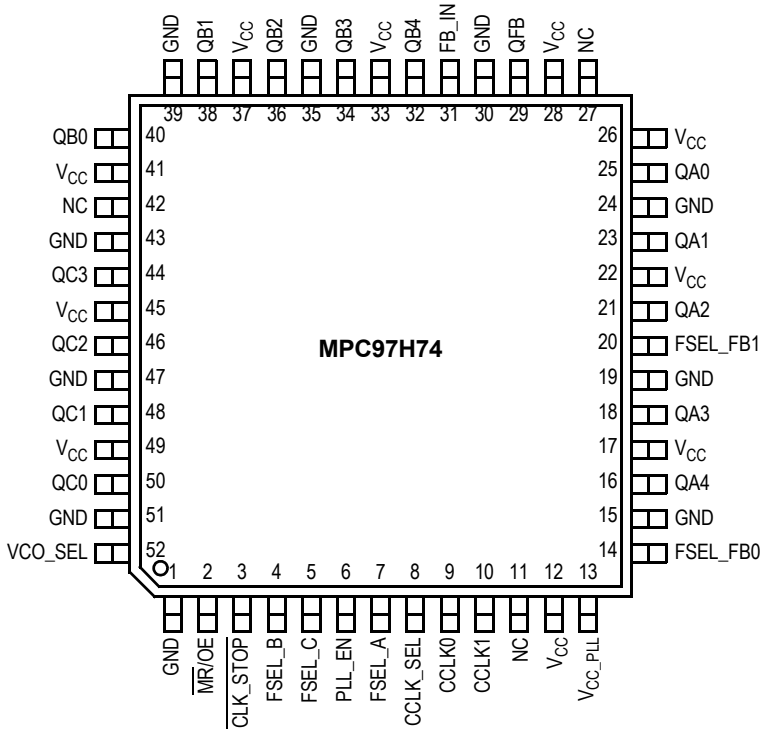


Figure 2. MPC97H74 52-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK0	Input	LVCMOS	PLL reference clock
CCLK1	Input	LVCMOS	Alternative PLL reference clock
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to QFB
CCLK_SEL	Input	LVCMOS	LVCMOS clock reference select
VCO_SEL	Input	LVCMOS	VCO operating frequency select
PLL_EN	Input	LVCMOS	PLL enable/PLL bypass mode select
$\overline{MR}$/OE	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
CLK_STOP	Input	LVCMOS	Output enable/clock stop (logic low state)
FSEL_A	Input	LVCMOS	Frequency divider select for bank A outputs
FSEL_B	Input	LVCMOS	Frequency divider select for bank B outputs
FSEL_C	Input	LVCMOS	Frequency divider select for bank C outputs
FSEL_FB[1:0]	Input	LVCMOS	Frequency divider select for the QFB output
QA[4:0]	Output	LVCMOS	Clock outputs (bank A)
QB[4:0]	Output	LVCMOS	Clock outputs (bank B)
QC[3:0]	Output	LVCMOS	Clock outputs (bank C)
QFB	Output	LVCMOS	PLL feedback output. Connect to FB_IN.
GND	Supply	Ground	Negative power supply
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin $V_{CC\_PLL.}$ Please see applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table (MPC97H74 Configuration Controls)

Control	Default	0	1
CCLK_SEL	0	Selects CCLK0 as PLL reference signal input	Selects CCKL1 as PLL reference signal input
VCO_SEL	0	Selects VCO ÷ 2. The VCO frequency is scaled by a factor of 2 (high input frequency range)	Selects VCO ÷ 4. The VCO frequency is scaled by a factor of 4 (low input frequency range).
PLL_EN	1	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC97H74 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
CLK_STOP	1	QA, QB an QC outputs disabled in logic low state. QFB is not affected by $\overline{CLK\_STOP}$. $\overline{CLK\_STOP}$ deassertion may cause the initial output clock pulse to be distorted.	Outputs enabled (active)
$\overline{MR}$/OE	1	Outputs disabled (high-impedance state) and reset of the device. During reset/output disable the PLL feedback loop is open and the internal VCO is tied to its lowest frequency. The MPC97H74 requires reset after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than one reference clock cycle (CCLKx). The device is reset by the internal power-on reset (POR) circuitry during power-up.	Outputs enabled (active)

VCO_SEL, FSEL_A, FSEL_B, FSEL_C and FSEL_FB[1:0] control the operating PLL frequency range and input/output frequency ratios. Refer to Table 3 and Table 4 for the device frequency configuration.

Table 3. Function Table (Output Dividers Bank A, B, and C)

VCO_SEL	FSEL_A	QA[4:0]	VCO_SEL	FSEL_B	QB[4:0]	VCO_SEL	FSEL_C	QC[3:0]
0	0	VCO ÷ 4	0	0	VCO ÷ 4	0	0	VCO ÷ 8
0	1	VCO ÷ 8	0	1	VCO ÷ 8	0	1	VCO ÷ 12
1	0	VCO ÷ 8	1	0	VCO ÷ 8	1	0	VCO ÷ 16
1	1	VCO ÷ 16	1	1	VCO ÷ 16	1	1	VCO ÷ 24

Table 4. Function Table (QFB)

VCO_SEL	FSEL_B1	FSEL_B0	QFB
0	0	0	VCO ÷ 8
0	0	1	VCO ÷ 16
0	1	0	VCO ÷ 12
0	1	1	VCO ÷ 24
1	0	0	VCO ÷ 16
1	0	1	VCO ÷ 32
1	1	0	VCO ÷ 24
1	1	1	VCO ÷ 48

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} ÷ 2		V	
MM	ESD protection (Machine Model)	200			V	
HBM	ESD protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		12		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 6. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 7. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{CC_PLL}	PLL Supply Voltage	3.02		V_{CC}	V	LVCMOS
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance		8 – 11		Ω	
I_{IN}	Input Current[2]			±200	μA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		5.0	7.5	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current			8.0	mA	All V_{CC} Pins

1. The MPC97H74 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
2. Inputs have pull-down or pull-up resistors affecting the input current.

Table 8. AC CHARACTERISTICS (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Reference Frequency	÷ 8 feedback	25.0		62.5	MHz	PLL locked
		÷ 12 feedback	16.6		41.6	MHz	
		÷ 16 feedback	12.5		31.25	MHz	
		÷ 24 feedback	8.33		20.83	MHz	
		÷ 32 feedback	6.25		15.625	MHz	
		÷ 48 feedback	4.16		10.41	MHz	
	Input Reference Frequency in PLL Bypass Mode[2]				250	MHz	PLL bypass
f_{VCO}	VCO Frequency Range[3]		200		500	MHz	
f_{MAX}	Output Frequency	÷ 4 output	50.0		125.0	MHz	PLL locked
		÷ 8 output	25.0		62.5	MHz	
		÷ 12 output	16.6		41.6	MHz	
		÷ 16 output	12.5		31.25	MHz	
		÷ 24 output	8.33		20.83	MHz	
$t_{PW,MIN}$	Input Reference Pulse Width[4]		2.0			ns	
t_R, t_F	CCLKx Input Rise/Fall Time				1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)[5] CCLKx to FB_IN (FB = ÷ 8 and f_{REF} = 50 MHz)		–250		+100	ps	PLL locked
$t_{SK(O)}$	Output-to-output Skew[6]	within QA bank			100	ps	
		within QB bank			125	ps	
		within QC bank			100	ps	
		any output			175	ps	
DC	Output Duty Cycle		47	50	53	%	
t_R, t_F	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
t_{PZL}	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle Jitter[7]				90	ps	
$t_{JIT(PER)}$	Period Jitter[6]				90	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)[8]	FB = ÷ 8			15	ps	
		FB = ÷ 12			49	ps	
		FB = ÷ 16			18	ps	
		FB = ÷24			22	ps	
		FB = ÷ 32			26	ps	
		FB = ÷ 48			34	ps	
BW	PLL Closed Loop Bandwidth[9]	FB = ÷ 8		0.50 - 1.80		MHz	
		FB = ÷ 12		0.30 - 1.00		MHz	
		FB = ÷ 16		0.25 - 0.70		MHZ	
		FB = ÷ 24		0.17 - 0.40		MHz	
		FB = ÷ 32		0.12 - 0.30		MHz	
		FB = ÷ 48		0.07 - 0.20		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

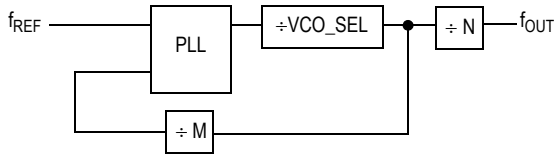
1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. In bypass mode, the MPC97H74 divides the input reference clock.
3. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio (FB): $f_{REF} = f_{VCO} \div (M \times VCO\_SEL)$.
4. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \times f_{REF} \times 100\%$ and $DC_{REF,MAX} = 100\% – DC_{REF,\ MIN}$. E.g. at f_{REF} = 62.5 MHz the input duty cycle range is 12.5% < DC < 87.5%.
5. Static phase offset depends on the reference frequency: $t_{(\varnothing)}$ = +50 ps ± (1 ÷ (120 × f_{REF})) for any reference frequency.
6. Refer to Application section for part-to-part skew calculation.
7. Valid for all outputs at the same fequency.
8. I/O jitter for f_{VCO} = 400 MHz. Refer to APPLICATIONS INFORMATION for I/O jitter at other frequencies and for a jitter calculation for confidence factors other than 1 σ.
9. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

MPC97H74 Configurations

Configuring the MPC97H74 amounts to properly configuring the internal dividers to produce the desired output frequencies. The output frequency can be represented by this formula:

$$f_{OUT} = f_{REF} \times M \div N$$



where f_{REF} is the reference frequency of the selected input clock source (CCLKO or CCLK1), M is the PLL feedback divider and N is a output divider. M is configured by the FSEL_FB[0:1] and N is individually configured for each output bank by the FSEL_A, FSEL_B and FSEL_C inputs.

The reference frequency f_{REF} and the selection of the feedback-divider M is limited by the specified VCO frequency range. f_{REF} and M must be configured to match the VCO frequency range of 200 to 500 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \le (f_{REF} \times VCO\_SEL \times M) \le f_{VCO,MAX}$$

The PLL post-divider VCO_SEL is either a divide-by-two or a divide-by-four and can be used to situate the VCO into the specified frequency range. This divider is controlled by the VCO_SEL pin. VCO_SEL effectively extends the usable input frequency range while it has no effect on the output to reference frequency ratio. The output frequency for each bank can be derived from the VCO frequency and the output divider:

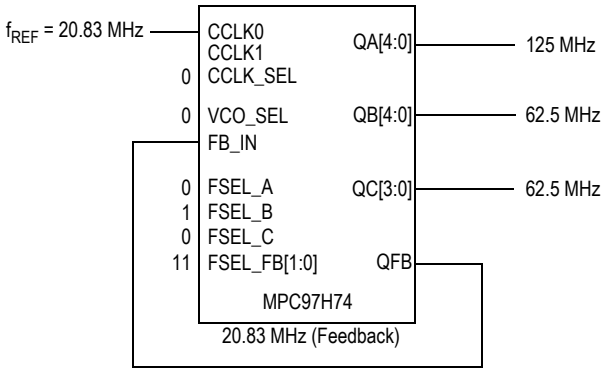
$$f_{QA[4:0]} = f_{VCO} \div (VCO\_SEL \times N_A)$$
$$f_{QB[4:0]} = f_{VCO} \div (VCO\_SEL \times N_B)$$
$$f_{QC[3:0]} = f_{VCO} \div (VCO\_SEL \times N_C)$$

Table 9MPC97H74 Dividers

Divider	Function	VCO_SEL	Values
M	PLL feedback FSEL_FB[0:1]	÷ 2	8, 12, 16, 24
		÷ 4	16, 24, 32, 48
N_A	Bank A Output Divider FSEL_A	÷ 2	4, 8
		÷ 4	8, 16
N_B	Bank B Output Divider FSEL_B	÷ 2	4, 8
		÷ 4	8, 16
N_C	Bank C Output Divider FSEL_C	÷ 2	8, 12
		÷ 4	16, 24

Table 9 shows the various PLL feedback and output dividers. The output dividers for the three output banks allow the user to configure the outputs into 1:1, 2:1, 3:2, and 3:2:1 frequency ratios. Figure 3 and Figure 4 display example configurations for the MPC97H74:

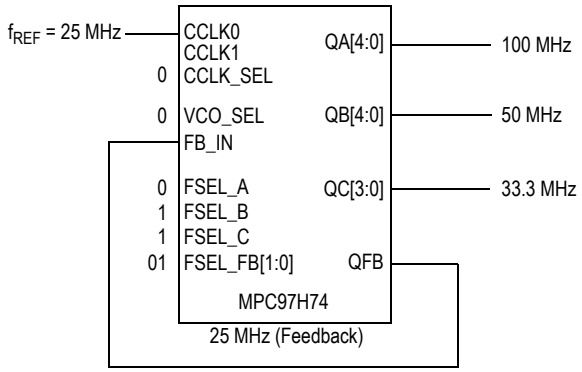
Figure 3. Example Configuration



MPC97H74 example configuration (feedback of QFB = 20.83 MHz, VCO_SEL = ÷ 2, M = 12, N_A = 2, N_B = 4, N_C = 4, f_{VCO} = 500 MHz).

Frequency Range	Min	Max
Input	8.33 MHz	20.83 MHz
QA outputs	50 MHz	125 MHz
QB outputs	25 MHz	62.5 MHz
QC outputs	25 MHz	62.5 MHz

Figure 4. Example Configuration



MPC97H74 example configuration (feedback of QFB = 25 MHz, VCO_SEL = ÷ 2, M = 8, N_A = 2, N_B = 4, N_C = 6, f_{VCO} = 400 MHz).

Frequency Range	Min	Max
Input	20 MHz	48 MHz
QA outputs	50 MHz	120 MHz
QB outputs	50 MHz	120 MHz
QC outputs	100 MHz	200 MHz

Using the MPC97H74 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC97H74. Designs using the MPC97H74 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback of the MPC97H74 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC97H74 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC97H74 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \times CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

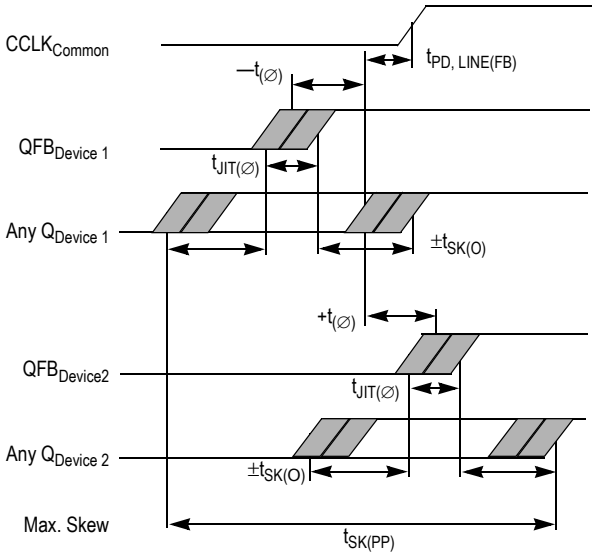


Figure 5. MPC97H74 Max. Device-to-Device Skew

Due to the statistical nature of I/O jitter a rms value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 10.

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device.

Table 10. Confidence Factor CF

CF	Probability of Clock Edge Within The Distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

Due to the frequency dependence of the static phase offset and I/O jitter, using Figure 6. MPC97H74 I/O Jitter and Figure 7. MPC97H74 I/O Jitter to predict a maximum I/O jitter and the specified $t_{(\varnothing)}$ parameter relative to the input reference frequency results in a precise timing performance analysis.

In the following example calculation a I/O jitter confidence factor of 99.7 percent (± 3 σ) is assumed, resulting in a worst case timing uncertainty from the common input reference clock to any output of –470 ps to +320 ps relative to CCLK (PLL feedback = ÷8, reference frequency = 50 MHz, VCO frequency = 400 MHz, I/O jitter = 15 ps rms max., static phase offset $t_{(\varnothing)}$ = –250 ps to +100 ps):

$$t_{SK(PP)} = [–250\ ps...+100\ ps] + [–175\ ps...175\ ps] + [(15\ ps \times –3)...(15\ ps \times 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–470\ ps...+320\ ps] + t_{PD,\ LINE(FB)}$$

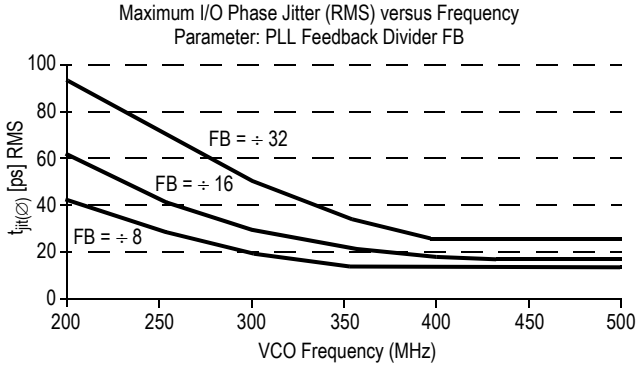


Figure 6. MPC97H74 I/O Jitter

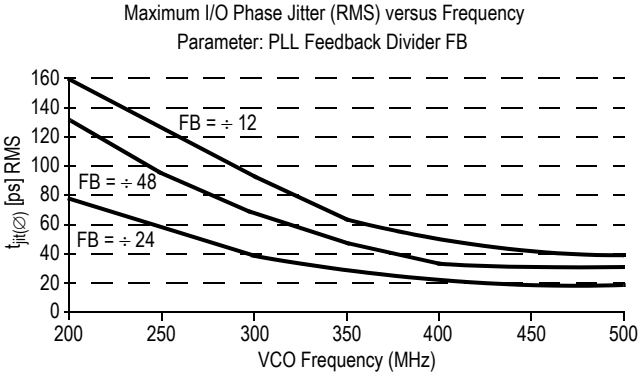


Figure 7. MPC97H74 I/O Jitter

Driving Transmission Lines

The MPC97H74 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC} divided by 2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC97H74 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 8. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC97H74 clock driver is effectively doubled due to its capability to drive multiple lines.

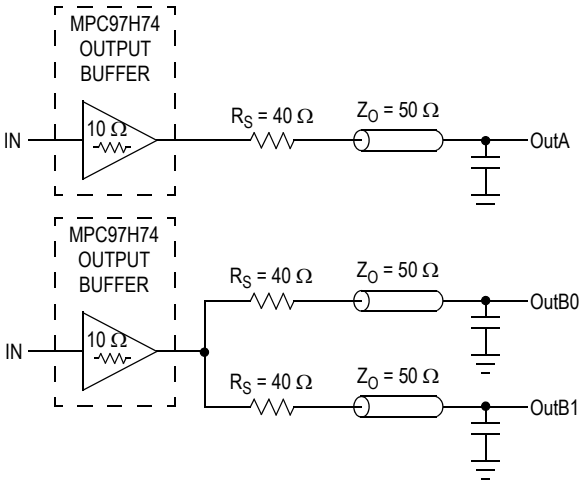


Figure 8. Single versus Dual Transmission Lines

The waveform plots in Figure 9. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC97H74 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC97H74. The output waveform in Figure 9. Single versus Dual Waveforms shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 40 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$
$Z_0 = 50\ \Omega \parallel 50\ \Omega$
$R_S = 40\ \Omega \parallel 40\ \Omega$
$R_0 = 10\ \Omega$
$V_L = 3.0 (25 \div (20 + 10 + 25)$
$= 1.36\ V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.7 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

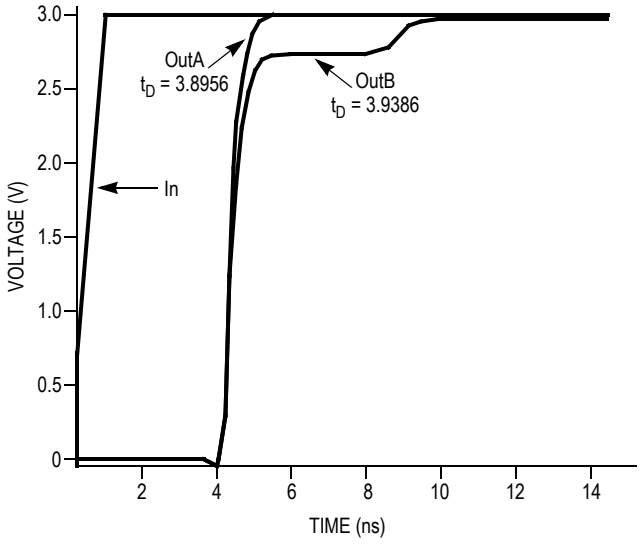
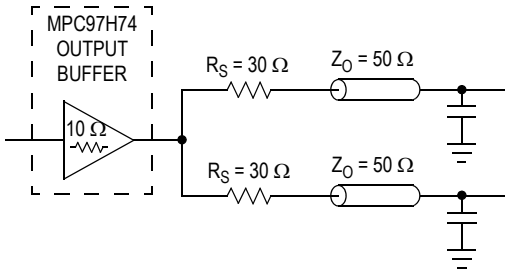


Figure 9. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 10. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



10 Ω + 30 Ω || 30 Ω = 50 Ω || 50 Ω
25 Ω = 25 Ω

Figure 10. Optimized Dual Line Termination

Power Supply Filtering

The MPC97H74 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC97H74 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device.The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC97H74. Figure 11. V_{CC_PLL} Power Supply Filter illustrates a typical power supply filter scheme. The MPC97H74 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the ICC_PLL current (the current sourced through the V_{CC_PLL} pin) is typically 5 mA (7.5 mA maximum), assuming that a minimum of 3.02 V (V_{CC_PLL}, minimum) must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 11. V_{CC_PLL} Power Supply Filter must have a resistance of 5 – 15 Ω to meet the voltage drop criteria.

The minimum values for RF and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 11. V_{CC_PLL} Power Supply Filter, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

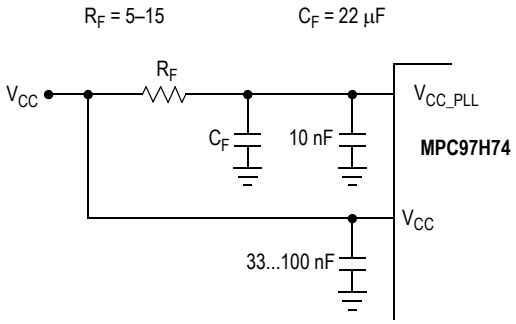


Figure 11. V_{CC_PLL} Power Supply Filter

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC97H74 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

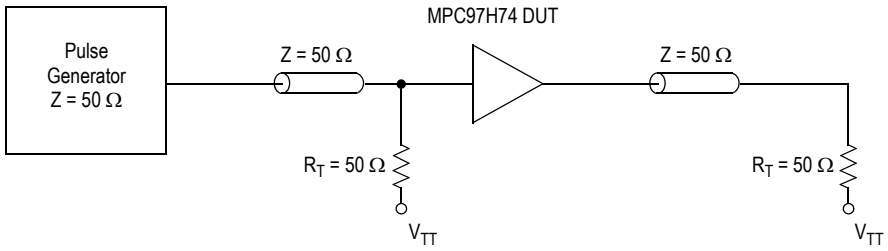
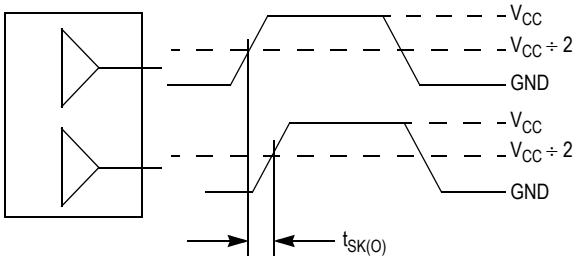


Figure 12. CCLK MPC97H74 AC Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 13. Output-to-Output Skew $t_{SK(O)}$

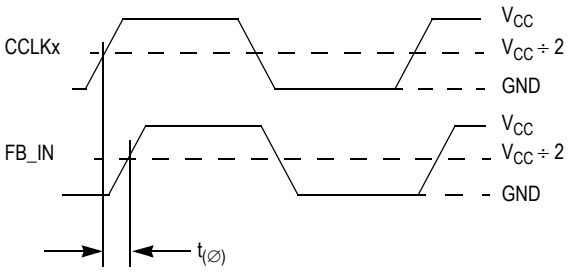
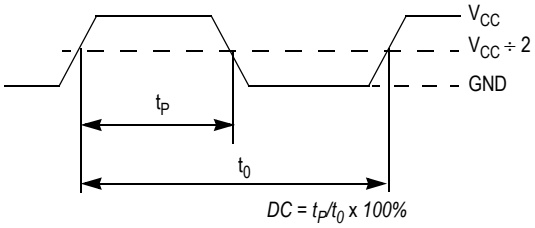
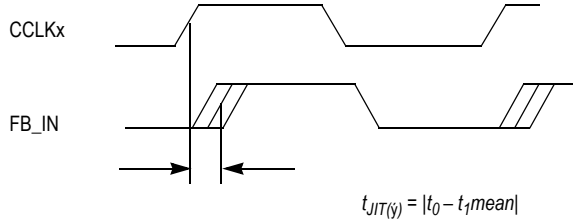


Figure 14. Propagation Delay ($t_{(\varnothing)}$, Static Phase Offset) Test Reference



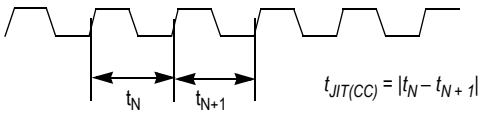
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 15. Output Duty Cycle (DC)



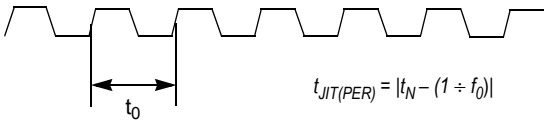
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 16. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 17. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 18. Period Jitter

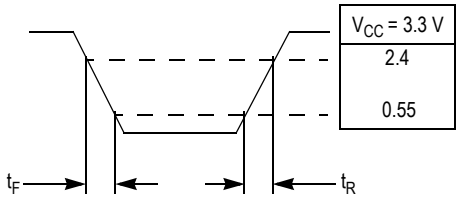


Figure 19. Output Transition Time Test Reference

Order number: MPC992
Rev 2, 08/2001

Low Voltage PECL PLL Clock Driver

MPC992

LOW VOLTAGE PLL CLOCK DRIVER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC992 is a 3.3V compatible, PLL based PECL clock generator and distributor. The fully differential design ensures optimum skew and PLL jitter performance. The performance of the device makes the MPC992 ideal for workstations, main frame computer, telecommunication and instrumentation applications. The device offers a crystal oscillator or a differential PECL reference clock input to provide flexibility in the reference clock interface. All of the control signals to the MPC992 are LVTTL compatible inputs.

Features

- Fully Integrated PLL
- Output Frequency of up to 400MHz
- PECL Clock Inputs and Outputs
- Operates from a 3.3V V_{CC} Supply
- Output Frequency Configurable
- 32-Lead TQFP Packaging
- ±25ps Cycle-Cycle Jitter

Functional Description

The MPC992 offers two banks of outputs which can be configured into four different relationships. The output banks can be configured into 2:1, 3:1, 3:2 and 5:2 ratios to provide a wide variety of potential frequency outputs.
In addition to these two banks of outputs a synchronization output is also offered. The SYNC output will provide information as to the time when the two output banks will transition positively in phase. This information can be important when the odd ratios are used as it provides for a baseline point in the system timing. The SYNC output will pulse high for one Qa clock period, centered on the rising Qa clock edge four edges prior to the Qb synchronous edge. The relationship is illustrated in the timing diagrams in the data sheet.

The MPC992 offers several features to aid in system debug and test. The PECL reference input pins can be interfaced to a test signal and the PLL can be bypassed to allow the designer to drive the MPC992 outputs directly. This allows for single stepping in a system functional debug mode. In addition an overriding reset is provided which will force all of the Q outputs LOW upon assertion.

The MPC992 is packaged in a 32-lead TQFP package to optimize both performance and board density.

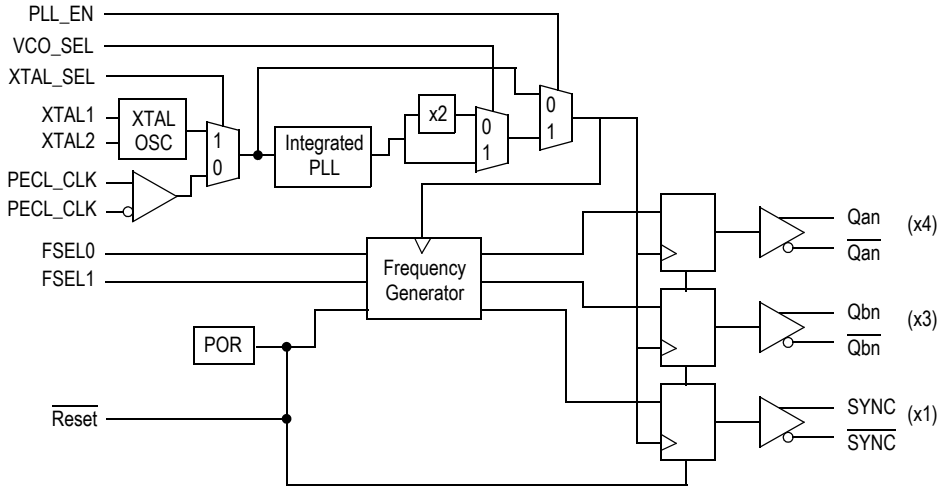


Figure 1. MPC992 Logic Diagram

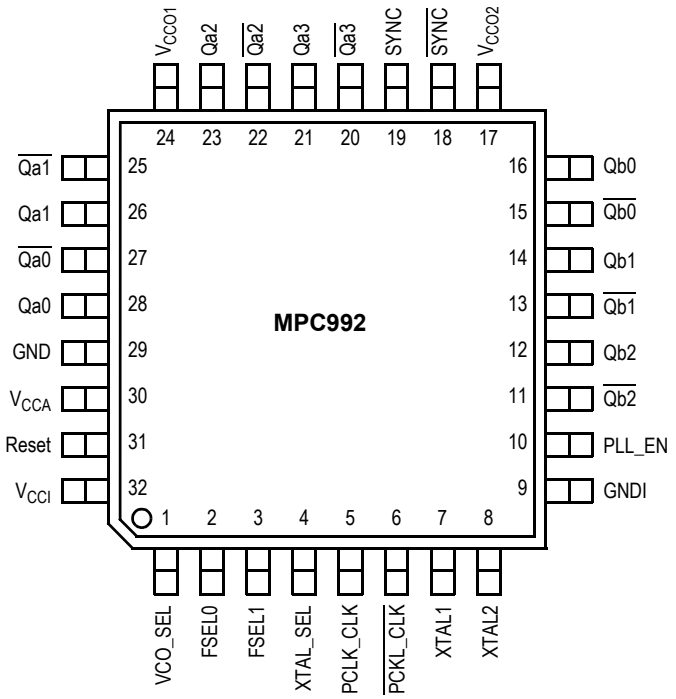


Figure 2. MPC992 32-Lead Package Pinout (Top View)

Table 1. Function Table 1

FSEL0	FSEL1	Qa	Qb	Feedback	Ratio
0	0	VCO/4	VCO/6	VCO/24	3:2
0	1	VCO/2	VCO/4	VCO/16	2:1
1	0	VCO/4	VCO/10	VCO/40	5:2
1	1	VCO/2	VCO/6	VCO/24	3:1

Table 2. Input vs Output Frequency

FSEL0	FSEL1	Qa	Qb	Internal Feedback
0	0	6 (f_{ref})	4 (f_{ref})	f_{ref}
0	1	8 (f_{ref})	4 (f_{ref})	f_{ref}
1	0	10 (f_{ref})	4 (f_{ref})	f_{ref}
1	1	12 (f_{ref})	4 (f_{ref})	f_{ref}

Table 3. Function Table 2

Control Signal	Logic '0'	Logic '1'
Reset	Outputs Enabled	Outputs Disabled
XTAL_SEL	PECL REF	XTAL REF
PLL_EN	Disabled	Enabled
VCO_SEL	High Frequency	Low Frequency

Table 4. Pin Description

Pin Name	Function
VCO_SEL	VCO range select pin (Int Pullup)
PLL_EN	PLL bypass select pin (Int Pullup)
XTAL_SEL	Input reference source select pin (Int Pullup)
XTAL1:2	Crystal interface pins for the internal oscillator
PECL_CLK	True PECL reference clock input (Int Pulldown)
$\overline{\text{PECL\_CLK}}$	Compliment PECL reference clock input (Int Pullup)
FSELn	Internal divider select pins (Int Pullup)
RESET	Internal flip-flop reset, true outputs go LOW (Int Pulldown)

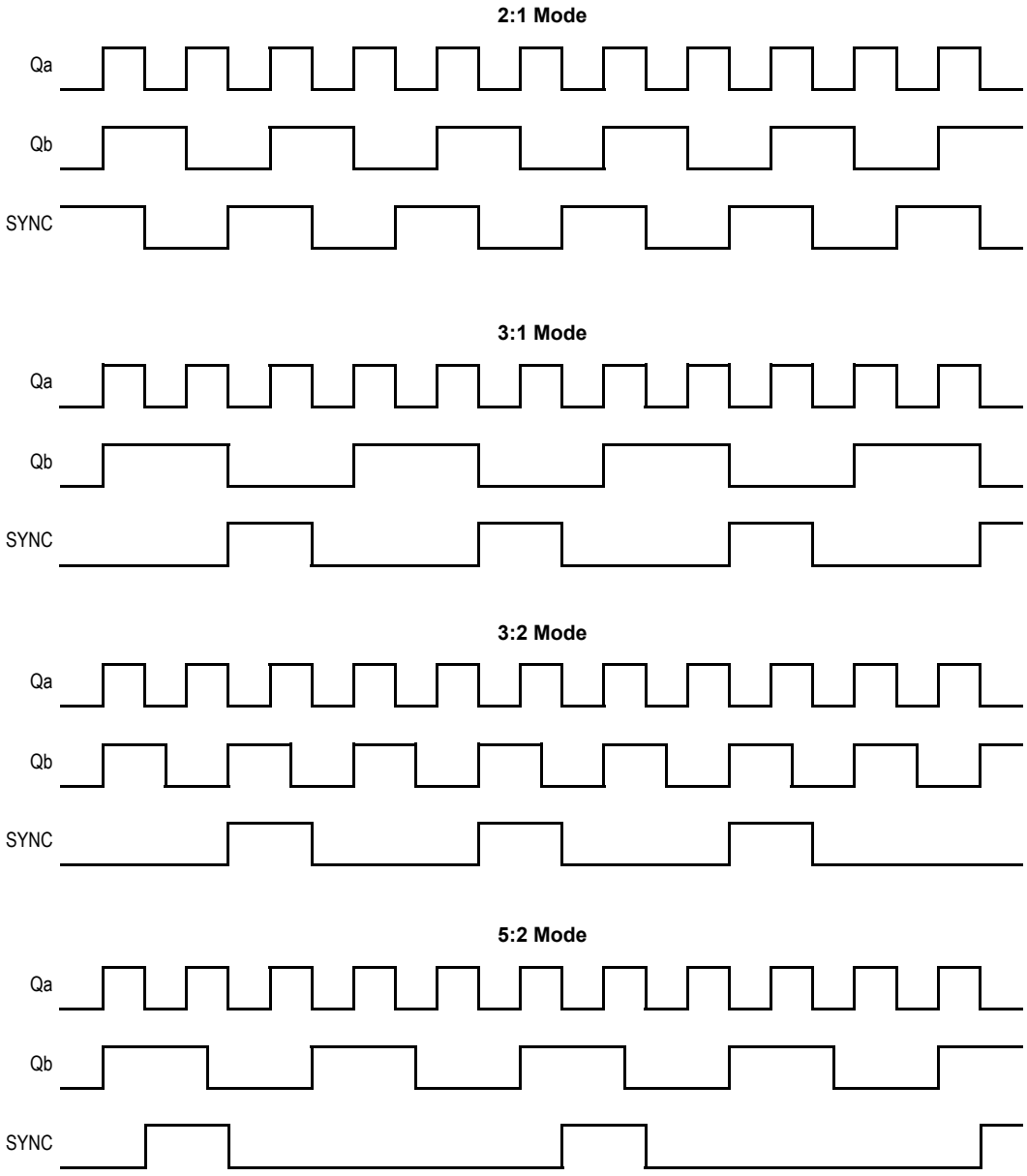


Figure 3. Output Waveforms

Table 5. Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	4.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{OUT}	Output Current Continuous Surge		50 100	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (T_A = 0° to 70°C, V_{CC} = 3.3V ± 5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	PECL_CLK[1] Other	2.15 2.0		2.4 V_{CC}	V	V_{CC} = 3.3V
V_{IL}	Input LOW Voltage	PECL_CLK[1] Other	1.5 0		1.8 0.8	V	V_{CC} = 3.3V
V_{OH}	Output HIGH Voltage[1]		1.8		2.4	V	V_{CC} = 3.3V
V_{OL}	Output LOW Voltage[1]		1.2		1.7	V	V_{CC} = 3.3V
I_{IN}	Input Current		–120		120	μA	
I_{CCI}	Maximum Quiescent Supply Current			130	150	mA	
I_{CCA}	Maximum PLL Supply Current			15	20	mA	

1. DC levels will vary 1:1 with V_{CC}.

Table 7. AC Characteristics (T_A = 0° to 70°C, V_{CC} = 3.3V ± 5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
t_r, t_f	Output Rise/Fall Time		200		850	ps	20% to 80%
t_{pw1}	Output Duty Cycle		49		51	%	
t_{pw2}	SYNC Output Duty Cycle		0.95		1.05	%	PCLK Period
f_{ref}	Input Reference Frequency	XTAL FREF	10 Note[1]		20 Note[1]	MHz	
t_{os}	Output-to-Output Skew	Qa, Qb Qa (–) to SYNC (+)			100 300	ps	
f_{VCO}	PLL VCO Lock Range		200 400		440 750	MHz	VCO_SEL = 1 VCO_SEL = 0
f_{max}	Maximum Output Frequency	Qa (÷2) Qa,Qb (÷4) Qb (÷6) Qb (÷10)			375 187.5 125 75	MHz	Note[2]
t_{jitter}	Cycle-to-Cycle Jitter (Peak-to-Peak)			±25	±50	ps	Note[3]
t_{lock}	Maximum PLL Lock Time				10	ms	

1. ECLK and XTAL input reference limited by the feedback divide and the guaranteed VCO lock range.
2. At 400MHz the output swing will be less than the nominal value.
3. Guaranteed by characterization.

APPLICATIONS INFORMATION

Using the On-Board Crystal Oscillator

The MPC992 features an on-board crystal oscillator to allow for seed clock generation as well as final distribution. The on-board oscillator is completely self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC992 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit as opposed to the more common parallel resonant circuit, this eliminates the need for large on-board capacitors. Because the design is a series resonant design, for optimum frequency accuracy a series resonant crystal should be used (see specification table below). Unfortunately most off the shelf crystals are characterized in a parallel resonant mode. However a parallel resonant crystal is physically no different than a series resonant crystal, a parallel resonant crystal is simply a crystal which has been characterized in its parallel resonant mode. Therefore in the majority of cases a parallel specified crystal can be used with the MPC992 with just a minor frequency error due to the actual series resonant frequency of the parallel resonant specified crystal. Typically a parallel specified crystal used in a series resonant mode will exhibit an oscillatory frequency a few hundred ppm lower than the specified value. For most processor implementations a few hundred ppm translates into kHz inaccuracies, a level which does not represent a major issue.

Figure 4 shows an optional series capacitor in the crystal oscillator interface. The on-board oscillator introduces a small phase shift in the overall loop which causes the oscillator to operate at a frequency slightly slower than the specified crystal. The series capacitor is used to compensate the loop and allow the oscillator to function at the specified crystal frequency. If a 100ppm type error is not important, the capacitor can be left off the PCB. For more detailed information, order Motorola Application Note AN1579/D.

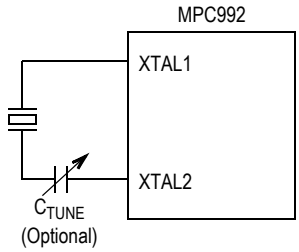


Figure 4. Recommended Crystal Interface

Table 8. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance*
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150ppm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω max
Correlation Drive Level	100μΩ
Aging	5ppm/Yr (First 3 Years)

Power Supply Filtering

The MPC992 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC992 provides separate power supplies for the digital circuitry (V_{CCI}) and the internal PLL (V_{CCA}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC992.

Figure 5 illustrates a typical power supply filter scheme. The MPC992 is most susceptible to noise with spectral content in the 10kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC992. From the data sheet the I_{VCCA} current (the current sourced through the V_{CCA} pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the V_{CCA} pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 5 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

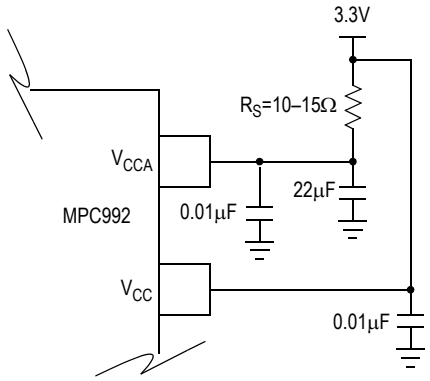


Figure 5. Power Supply Filter

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000μH choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the V_{CCA} pin a low DC resistance inductor is required (less than 15Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MPC992 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. The important aspect of the layout for the MPC992 is low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC992 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

No active signal lines should pass below the crystal interface to the MPC992. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. In addition, the crystal interface circuitry will be adversely affected by activity on the PECL_CLK inputs. Therefore, it is recommended that the PECL input signals be static when the crystal oscillator circuitry is being used.

Although the MPC992 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

3.3V Differential ECL/PECL PLL Clock Generator

MPC9992

3.3V DIFFERENTIAL ECL/PECL CLOCK GENERATOR

FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A-03

The MPC9992 is a 3.3 V compatible, PLL based PECL clock driver. Using SiGe technology and a fully differential design ensures optimum skew and PLL jitter performance. The performance of the MPC9992 makes the device ideal for workstation, mainframe computer and telecommunication applications. With output frequencies up to 400 MHz and output skews less than 100 ps the device meets the needs of the most demanding clock applications. The MPC9992 offers a differential PECL input and a crystal oscillator interface. All control signals are LVCMOS compatible.

Features

- 7 differential outputs, PLL based clock generator
- SiGe technology supports minimum output skew (max. 100 ps)
- Supports up to two generated output clock frequencies with a maximum clock frequency up to 400 MHz
- Selectable crystal oscillator interface and PECL compatible clock input
- SYNC pulse generation
- PECL compatible differential clock inputs and outputs
- Single 3.3V (PECL) supply
- Ambient temperature range 0°C to +70°C
- Standard 32 lead LQFP package
- Pin and function compatible to the MPC992
- 32-lead Pb-free Package Available

Functional Description

The MPC9992 utilizes PLL technology to frequency lock its outputs onto an input reference clock. The reference clock frequency and the divider for the feedback path determine the VCO frequency. Both must be selected to match the VCO frequency range. The MPC9992 features frequency programmability between the three output banks outputs as well as the output to input relationships. Output frequency ratios of 2:1, 3:1, 3:2 and 5:2 can be realized. The two banks of outputs and the feedback frequency divider can be programmed by the FSEL[2:0] pins of the device. The VCO_SEL pin provides an extended PLL input reference frequency range.

The SYNC pulse generator monitors the phase relationship between the QA[3:0] and QB[2:0] output banks. The SYNC generator output signals the coincident edges of the two output banks. This feature is useful for non binary relationships between output frequencies.

The REF_SEL pin selects the differential PECL compatible input pair or crystal oscillator interface as the reference clock signal. The PLL_EN control selects the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is routed directly to the output dividers bypassing the PLL. The PLL bypass is fully static and the minimum clock frequency specification and all other PLL characteristics do not apply.

The MPC9992 requires an external reset signal for start-up and for PLL recovery in case the reference input is interrupted. Assertion of the reset signal forces all outputs to the logic low state.

The MPC9992 is fully 3.3V compatible and requires no external loop filter components. The differential clock input (PCLK) is PECL compatible and all control inputs accept LVCMOS compatible signals while the outputs provide PECL compatible levels with the capability to drive terminated 50 Ω transmission lines.

The device is pin and function compatible to the MPC992 and is packaged in a 32-lead LQFP package.

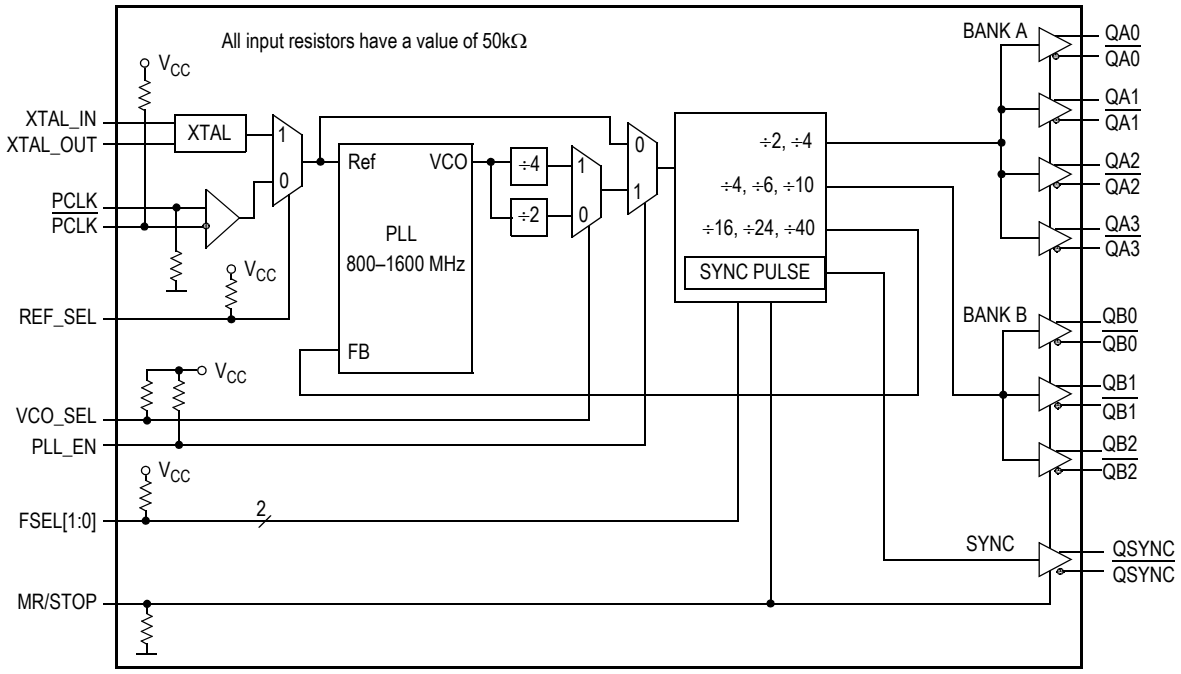


Figure 1. MPC9992 Logic Diagram

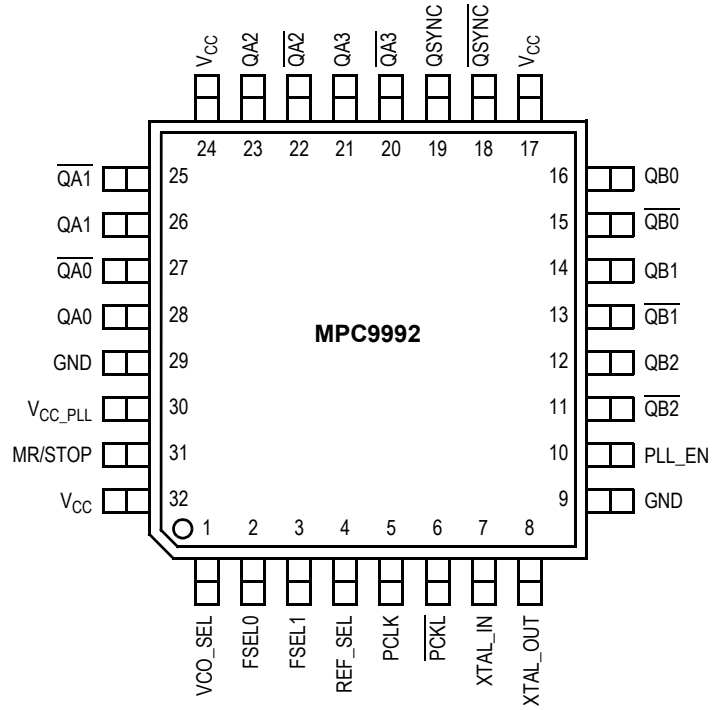


Figure 2. MPC9992 32-Lead Package Pinout (Top View)

Table 1. MPC9992 PLL Configurations

VCO_SEL	FSEL_0	FSEL_1	f_{REF} (MHz)	QA[3:0] (N_A)	QB[2:0] (N_B)	Frequency Ratio QA to QB	Internal Feedback (M · VCO_SEL)
0	0	0	16.6–33.3	VCO÷8 (6 · f_{REF})	VCO÷12 (4 · f_{REF})	3÷2	VCO÷48
0	0	1	25–50	VCO÷4 (8 · f_{REF})	VCO÷8 (4 · f_{REF})	2÷1	VCO÷32
0	1	0	10–20	VCO÷8 (10 · f_{REF})	VCO÷20 (4 · f_{REF})	5÷2	VCO÷80
0	1	1	16.6–33.3	VCO÷4 (12 · f_{REF})	VCO÷12 (4 · f_{REF})	3÷1	VCO÷48
1	0	0	8.3–16.6	VCO÷16 (6 · f_{REF})	VCO÷24 (4 · f_{REF})	3÷2	VCO÷96
1	0	1	12.5–25	VCO÷8 (8 · f_{REF})	VCO÷16 (4 · f_{REF})	2÷1	VCO÷64
1	1	0	5–10	VCO÷16 (10 · f_{REF})	VCO÷40 (4 · f_{REF})	5÷2	VCO÷160
1	1	1	8.3–16.6	VCO÷8 (12 · f_{REF})	VCO÷24 (4 · f_{REF})	3÷1	VCO÷96

Table 2. Function Table (Configuration Controls)

Control	Default	0	1
REF_SEL	1	Selects PCLK, $\overline{\text{PCLK}}$ as PLL references signal input	Selects the crystal oscillator as PLL reference signal input
VCO_SEL	1	Selects VCO÷2. The VCO frequency is scaled by a factor of 2 (high input frequency range)	Selects VCO÷4. The VCO frequency is scaled by a factor of 4 (low input frequency range).
PLL_EN	1	Test mode with the PLL bypassed. The reference clock is substituted for the internal VCO output. MPC9992 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Normal operation mode with PLL enabled.
MR/STOP	0	Normal operation	Reset of the device and output disable (output clock stop). The outputs are stopped in logic low state: Qx=L, $\overline{\text{Q}}$x=H. The minimum reset period should be greater than one reference clock cycle.

VCO_SEL and FSEL[1:0] control the operating PLL frequency range and input/output frequency ratios. See Table 1 for the device frequency configuration.

Table 3. Pin Configuration

Pin	I/O	Type	Function
PCLK, $\overline{\text{PCLK}}$	Input	PECL	Differential reference clock signal input
XTAL_IN, XTAL_OUT		Analog	Crystal oscillator interface
VCO_SEL	Input	LVCMOS	VCO operating frequency select
PLL_EN	Input	LVCMOS	PLL Enable/Bypass mode select
REF_SEL	Input	LVCMOS	PLL reference signal input select
MR/STOP	Input	LVCMOS	Device reset and output clock disable (stop in logic low state)
FSEL[1:0]	Input	LVCMOS	Output and PLL feedback frequency divider select
QA[0-3], $\overline{\text{QA[0–3]}}$	Output	PECL	Differential clock outputs (bank A)
QB[0-2], $\overline{\text{QB[0–2]}}$	Output	PECL	Differential clock outputs (bank B)
QSYNC, $\overline{\text{QSYNC}}$	Output	PECL	Differential clock outputs (bank C)
GND	Supply	GND	Negative power supply
V_{CC}	Supply	V_{CC}	Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see applications section for details

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine Model)	175			V	
HBM	ESD Protection (Human Body Model)	2000			V	
CDM	ESD Protection (Charged Device Model)	1000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T_J	Operating Junction Temperature[1] (continuous operation) MTBF = 9.1 years	0		110	°C	

1. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9992 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9992 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 6. DC Characteristics (V_{CC} = 3.3V ± 5%, GND = 0V, T_A = 0°C to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential PECL Clock Inputs (PCLK, $\overline{PCLK}$)[1]						
V_{PP}	AC Differential Input Voltage[2]	0.2		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[3]	1.0		V_{CC}-0.3	V	Differential operation
I_{IN}	Input Current[4]			±120	µA	V_{IN} = V_{CC} or GND
LVCMOS Control Inputs (VCO_SEL, PLL_EN, MR/STOP, REF_SEL, FSEL[1:0])						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[4]			±120	µA	V_{IN} = V_{CC} or GND
PECL Clock Outputs (QA[3:0], $\overline{QA[3:0]}$, QB[2:0], $\overline{QB[2:0]}$, QSYNC, $\overline{QSYNC}$)						
V_{OH}	Output High Voltage	V_{CC}–1.025		V_{CC}–0.880	V	I_{OH} = –30 mA
V_{OL}	Output Low Voltage	V_{CC}–1.920		V_{CC}–1.620	V	I_{OL} = –5 mA
Supply Current and Voltage						
V_{CC_PLL}	PLL Supply Voltage	2.955		V_{CC}	V	V_{CC_PLL} pin
I_{CC_PLL}	Maximum PLL Supply Current		9.0	12	mA	V_{CC_PLL} pin
I_{GND}[5]	Maximum Supply Current		80	110	mA	GND pins

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
3. Inputs have pull-down resistors affecting the input current.
4. Equivalent to a termination of 50Ω to V_{TT}.
5. Does not include output drive current which is dependant on output termination methods.

Table 7. AC Characteristics (V_{CC} = 3.3V ± 5%, GND = 0V, T_A = 0°C to +70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency	÷32 feedback	25.0		50.0	MHz	PLL locked
		÷48 feedback	16.67		33.3	MHz	
		÷64 feedback	12.5		25.0	MHz	
		÷80 feedback	10.0		20.0	MHz	
		÷96 feedback	8.33		16.67	MHz	
		÷160 feedback	5.0		10.0	MHz	
	Input Reference Frequency in PLL Bypass Mode[2]				400	MHz	PLL bypass
f_{XTAL}	Crystal Interface Frequency Range[3]		10		20	MHz	
f_{VCO}	VCO Frequency Range[4]		800		1600	MHz	
f_{MAX}	Output Frequency	÷4 output	200.0		400.0	MHz	PLL locked
		÷8 output	100.0		200.0	MHz	
		÷12 output	66.6		133.3	MHz	
		÷16 output	50.0		100.0	MHz	
		÷20 output	40.0		80.0	MHz	
		÷24 output	33.3		66.6	MHz	
		÷48 output	16.6		33.3	MHz	
V_{PP}	Differential Input Voltage[5] (peak-to-peak)		0.3		1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[6]	(PCLK)	1.2		V_{CC}–0.3	V	
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak)	(PCLK)	0.6	0.8		V	
$t_{PW,MIN}$	Input Reference Pulse Width[7]		2.0			ns	
$t_{sk(O)}$	Output-to-Output Skew				100	ps	
DC	Output Duty Cycle[8]		48	50	52	%	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter[9]			30	79	ps	
$t_{JIT(PER)}$	Period Jitter[9]			43	106	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter[9]	RMS (1 σ)[10]		86	212	ps	
BW	PLL Closed Loop Bandwidth[11]	÷32 feedback		0.60-1.5		MHz	
		÷48 feedback		0.40-1.2		MHz	
		÷64 feedback		0.30-1.0		MHz	
		÷80 feedback		0.30-0.8		MHz	
		÷96 feedback		0.20-0.7		MHz	
		÷160 feedback		0.15-0.4		MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	
t_r, t_f	Output Rise/Fall Time		0.05		1.0	ns	20% to 80%

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. In bypass mode, the MPC9992 divides the input reference clock.
3. The crystal frequency range must both meet the interface frequency range and VCO lock range divided by the feedback divider ratio: $f_{XTAL(min, max)} = f_{VCO(min, max)} \div (M \cdot VCO\_SEL)$ and 10 MHz ≤ f_{XTAL} ≤ 20 MHz.
4. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = f_{VCO} \div (M \cdot VCO\_SEL)$
5. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics.
6. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification.
7. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% – DC_{REF, MIN.}$ E.g. at f_{REF} = 50 MHz the input duty cycle range is 10% < DC < 90%.
8. Output duty cycle for QAx and QBx outputs. The pulse width for the QSYNC output is equal to one QAx output period $t_{QA} \pm 5\%$.
9. Jitter data is valid f_{ref} = 25 MHz.
10. See application section for a jitter calculation for other confidence factors than 1 σ.
11. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

SYNC Output Description

The MPC9992 has a system synchronization pulse output QSYNC. In configurations with the output frequency relationships are not integer multiples of each other QSYNC provides a signal for system synchronization purposes. The MPC9992 monitors the relationship between the A bank and the B bank of outputs. The QSYNC output is asserted (logic high) one QA period in duration. The placement of the pulse is dependent on the QA and QB output frequencies ratio. Figure 3 shows the waveforms for the QSYNC output. The QSYNC output is defined for all possible combinations of the bank A and bank B outputs.

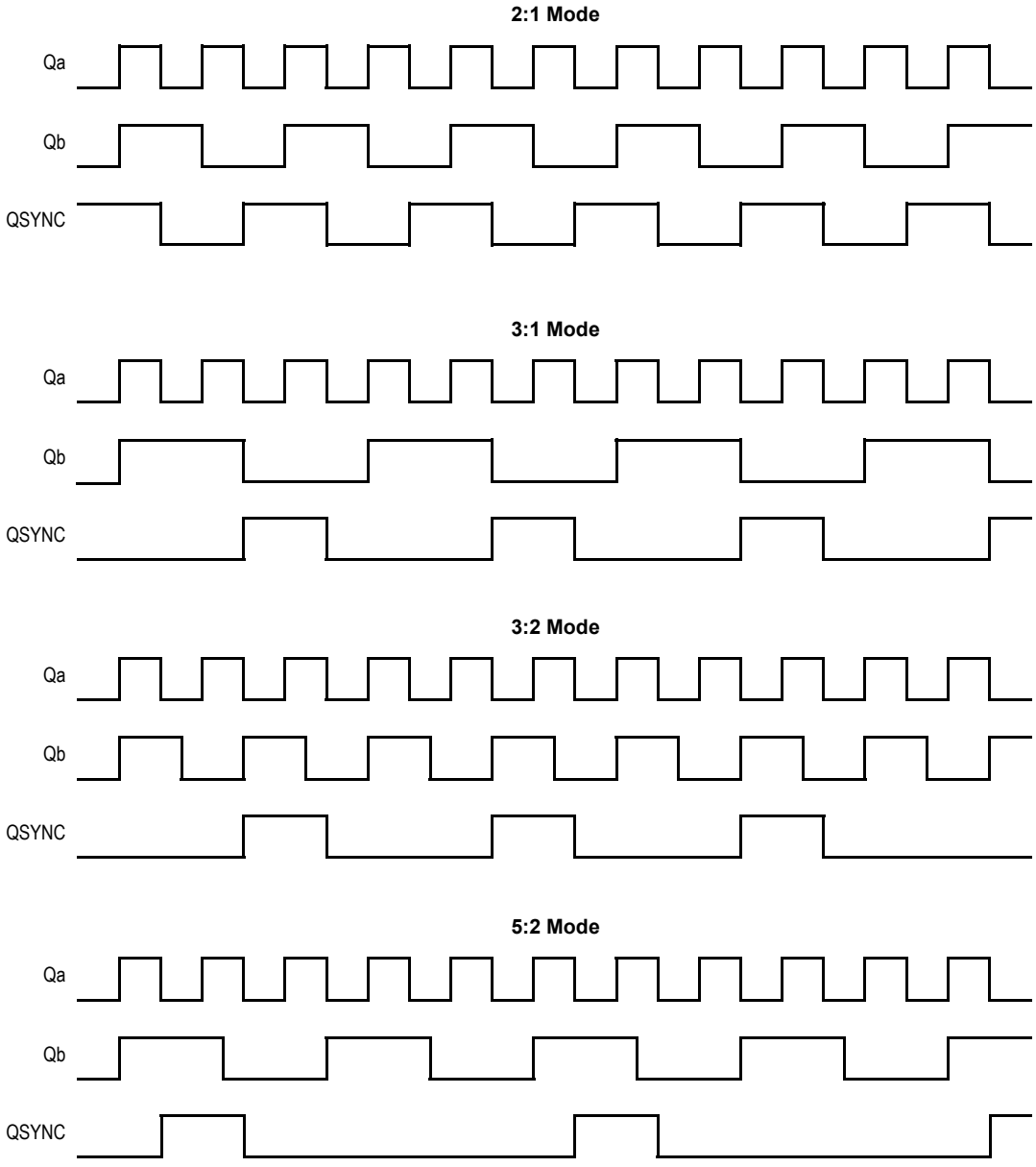


Figure 3. QSYNC Timing Diagram

Power Supply Filtering

The MPC9992 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9992 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9992. Figure 4 illustrates a typical power supply filter scheme. The MPC9992 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 9 mA (12 mA maximum), assuming that a minimum of 2.955V must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 4 must have a resistance of 10-15Ω to meet the voltage drop criteria.

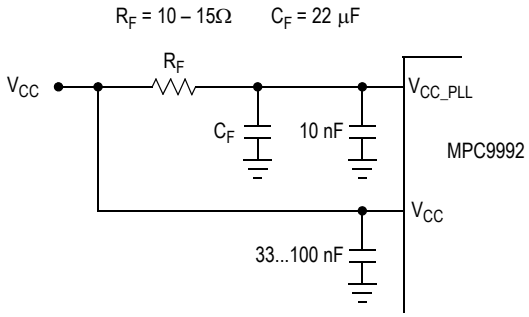


Figure 4. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 4, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9992 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

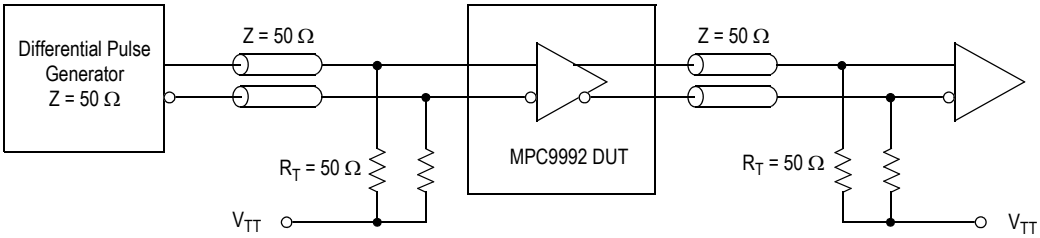


Figure 5. MPC9992 AC Test Reference

Chapter Three
QUICCClock Generator Data Sheets

QUICCClock Generator Device Index

Order number: MPC9817
Rev 0, 07/2004

Advance Information

Clock Generator for PowerQUICC and PowerPC Microprocessors and Microcontrollers

MPC9817

MICROPROCESSOR CLOCK GENERATOR

SD SUFFIX
20 SSOP PACKAGE
CASE 1461-01

The MPC9817 is a PLL-based clock generator specifically designed for Motorola Microprocessor and Microcontroller applications including the PowerPC and PowerQUICC. This device generates the microprocessor input clock and other microprocessor system and bus clocks at any one of four output frequencies. These frequencies include the popular 33- and 66-MHz PCI bus frequencies. The device offers five low-skew clock outputs plus three reference outputs. The clock input reference is 25 MHz and may be derived from an external source or by the addition of a 25-MHz crystal to the on-chip crystal oscillator. The extended temperature range of the MPC9817 supports telecommunication and networking requirements.

Features

- 5 LVCMOS outputs for processor and other system circuitry
- 3 Buffered 25-MHz reference clock outputs
- Crystal oscillator or external reference input
- 25-MHz input reference frequency
- Selectable output frequencies include: 25, 33, 50, or 66 MHz
- Low cycle-to-cycle and period jitter
- Package: 20-lead SSOP
- 3.3-V supply
- Supports computing, networking, and telecommunications applications
- Ambient temperature range: –40°C to +85°C

Functional Description

The MPC9817 uses a PLL with a 25-MHz input reference frequency to generate a single bank of five configurable LVCMOS output clocks. The output frequency of this bank is configurable to either 25, 33, 50, or 66 MHz by two FSEL pins. The 25-MHz reference may be either an external frequency source or a 25-MHz crystal. The 25-MHz crystal is directly connected to the XTAL_IN and XTAL_OUT pins with no additional components required. An external reference may be applied to the XTAL_IN pin with the XTAL_OUT pin left floating. The input reference, whether provided by a crystal or an external input, is also directly buffered to a second bank of three LVCMOS outputs. These outputs may be used as the clock source for processor I/O applications such as an Ethernet PHY. When FSEL0 and FSEL1 are both configured low, the QA outputs are directly fed from the input reference providing a total of eight low-skew 25-MHz outputs. For all other combinations of FSEL0 and FSEL1 the single-ended LVCMOS outputs provide five low-skew outputs for use in driving a microprocessor or microcontroller clock input as well as other system components.

The MPC9817 is packaged in a 20-lead SSOP package.

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

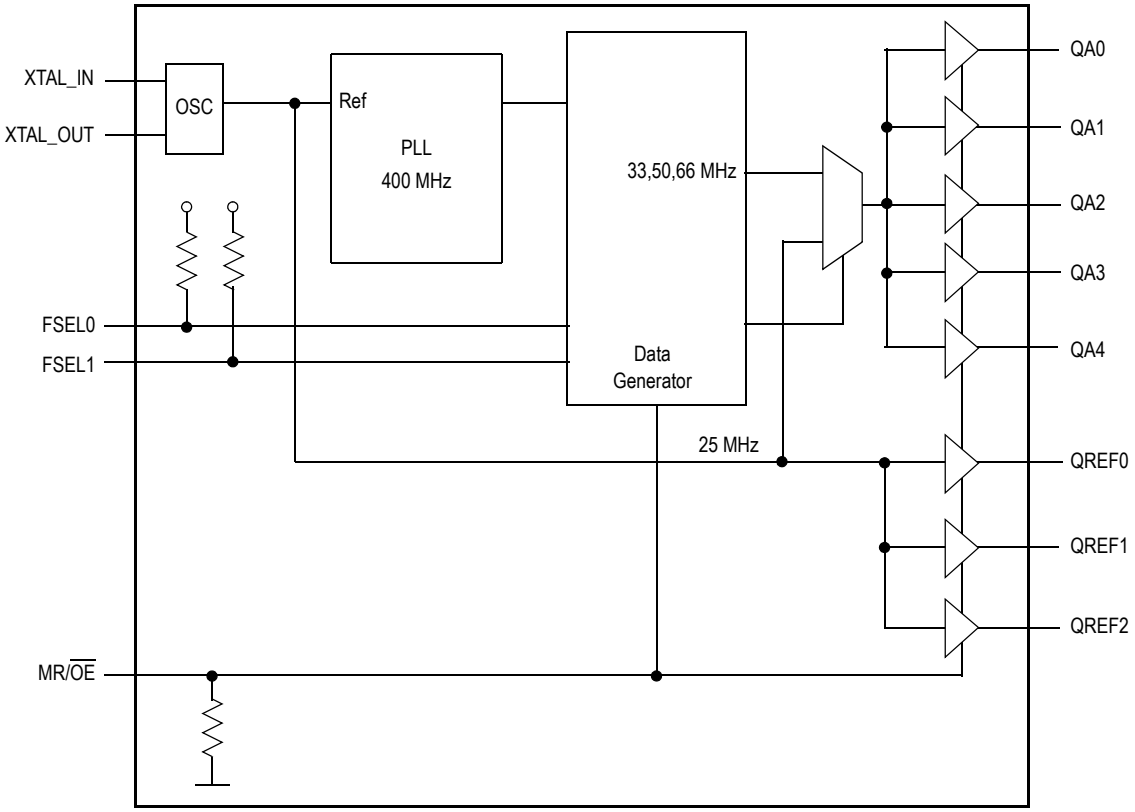


Figure 1. MPC9817 Logic Diagram

Table 1. Pin Configuration

Pin	I/O	Type	Function
QA0, QA1, QA2, QA3, QA4	Output	LVCMOS	Clock Outputs
QREF0, QREF1, QREF2	Output	LVCMOS	Reference Output (25 MHz)
XTAL_IN	Input	LVCMOS	Crystal Oscillator Input Pin
XTAL_OUT	Output	LVCMOS	Crystal Oscillator Output Pin
FSEL0, FSEL1	Input	LVCMOS	Configures Bank A Clock Output Frequency (pull-up)
MR/$\overline{OE}$	Input	LVCMOS	Enables All Outputs (pull-down)
V_{DD}	—	—	3.3-V Supply
GND	—	—	Ground

Table 2. Function Table

Control	Default	00	01	10	11
FSEL0,FSEL1	11	25 MHz fed directly from reference input, PLL disabled	33 MHz	50 MHz	66 MHz

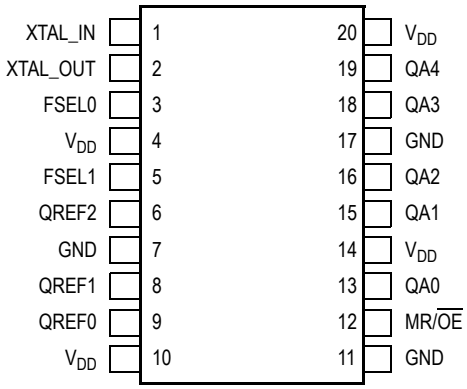


Figure 2. MPC9817 20-Lead SSOP Package Pinout (Top View)

MPC9817 OPERATION

Crystal Oscillator

The MPC9817 features a fully integrated Pierce oscillator to minimize system implementation costs. Other than the addition of a 25-MHz crystal, no external components are required.The crystal selection should be: 25 MHz, parallel resonant type with a load specification of C_L = 20 pF.

The crystal should be located as close to the MPC9817 XTAL_IN and XTAL_OUT pins as possible to avoid any board level parasitic.

Power Supply Bypassing

The MPC9817 should have all V_{DD} pins bypassed with 0.01 capacitors and a minimum of one 1.0 capacitor for the overall package. All capacitors should be located as close to the SSOP pins as possible.

External Clock Source

An external reference source of 25 MHz may be applied to the XTAL_IN pin. In this mode of operation, the XTAL_OUT pin should be left floating.

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{DD}	Supply Voltage	–0.3	3.8	V	
I_{IN}	DC Input Current	—	±20	mA	
I_{OUT}	DC Output Current	—	±75	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage	—	$V_{DD} \div 2$	—	V	
MM	ESD Protection (machine model)	200	—	—	V	
HBM	ESD Protection (human body model)	2000	—	—	V	
LU	Latch-Up Immunity	200	—	—	ma	
C_{IN}	Input Capacitance	—	4	—	pF	Inputs
θ_{JC}	Thermal Resistance (junction-to-ambient, junction-to-board, junction-to-case)	—	TBD	—	°C/W	
T_C	Ambient Temperature	–40		85	°C	

Table 5. DC Characteristics (V_{DD} = 3.3 V ± 5%, T_A= –40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage (XTAL_IN)	2.4	—	V_{DD} + 0.3	V	Input threshold = $V_{DD}/2$
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	—	—	0.8	V	LVCMOS
I_{IN}	Input Current[1]	—	—	150	μA	$V_{IN} = V_{DDL}$ or GND
V_{OH}	Output High Voltage	2.4	—	—	V	I_{OH} = –24 mA
V_{OL}	Output Low Voltage	—	—	0.4	V	I_{OL} = 24 mA
Z_{OUT}	Output Impedance	—	14	—	Ω	
I_{DD}	Maximum Quiescent Supply Current	—	TBD	TBD	mA	V_{DD} pins

1. Inputs have pull-down resistors affecting the input current.

Table 6. AC Characteristics[1] [2] (V_{DD} = 3.3 V ± 5%, T_A= –40°C to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
Input and Output Timing Specification							
f_{ref}	Input Reference Frequency	25 MHz Input XTAL Input	TBD TBD	25 25	TBD TBD	MHz MHz	
f_{VCO}	VCO Frequency Range		—	400	—	MHz	
f_{MCX}	Output Frequency (QAx)	FSEL0, FSEL1 = 00 FSEL0, FSEL1 = 01 FSEL0, FSEL1 = 10 FSEL0, FSEL1 = 11 Output Frequency (QREFx)		25 33 50 66 25	— — — — —	MHz MHz MHz MHz MHz	PLL locked
f_{refPW}	Reference Input Pulse Width		TBD	—	—	ps	
DC	Output Duty Cycle		47.5	50	52.5	%	
f_{out}	Output Frequency Accuracy	Crystal[3] External Reference	TBD 0	— —	TBD 0	ppm ppm	
PLL Specifications							
BW	PLL Closed Loop Bandwidth[4]			500		kHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	
Skew and Jitter Specifications							
$t_{sk(O)}$	Output-to-Output Skew (within a bank)			TBD	100	ps	
$t_{sk(O)}$	Output-to-Output Skew (between bank A and bank Ref)			TBD	200		FSEL0, FSEL1 = 00
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter				150	ps	
$t_{JIT(PER)}$	Period Jitter				175	ps	
$t_{JIT(Ø)}$	I/O Phase Jitter				TBD	ps	
t_r, t_f	Output Rise/Fall Time				1	ns	20% to 80%

1. AC characteristics are design targets and pending characterization
2. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}
3. Based upon recommended crystal specifications as outlined in operation section
4. –3 dB point of PLL transfer characteristics

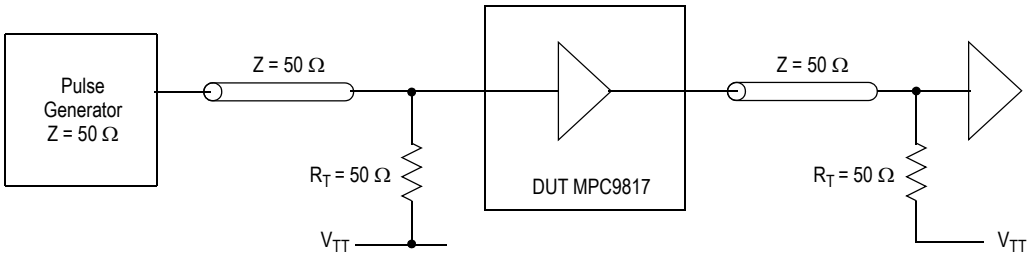


Figure 3. MPC9817 AC Test Reference (LVCMOS Outputs)

Table 7. MPC9817 Pin List

Pin	Description
1	XTAL_IN
2	XTAL_OUT
3	FSEL0
4	V_{DD}
5	FSEL1
6	QREF2
7	GND
8	QREF1
9	QREF0
10	V_{DD}

Pin	Description
11	GND
12	MR/$\overline{OE}$
13	QA0
14	V_{DD}
15	QA1
16	QA2
17	GND
18	QA3
19	QA4
20	V_{DD}

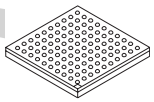
Order number: MPC9850
Rev 3, 07/2004

Preliminary Information

MPC9850

Clock Generator for PowerQUICC III

MICROPROCESSOR CLOCK GENERATOR



VF SUFFIX
VM SUFFIX (Pb-FREE)
100 MAPBGA PACKAGE
CASE 1462-01

The MPC9850 is a PLL based clock generator specifically designed for Motorola Microprocessor And Microcontroller applications including the PowerQUICC III. This device generates a microprocessor input clock plus the 500 MHz Rapid I/O clock. The microprocessor clock is selectable in output frequency to any of the commonly used microprocessor input and bus frequencies. The Rapid I/O outputs are LVDS compatible. The device offers eight low skew clock outputs organized into two output banks, each configurable to support different clock frequencies. The extended temperature range of the MPC9850 supports telecommunication and networking requirements.

Features

- 8 LVCMOS outputs for processor and other circuitry
- 2 differential LVDS outputs for Rapid I/O interface
- Crystal oscillator or external reference input
- 25 or 33 MHz Input reference frequency
- Selectable output frequencies include = 200, 166, 133,125, 111, 100, 83, 66, 50, 33 or 16 MHz
- Buffered reference clock output
- Rapid I/O (LVDS) Output = 500, 250 or 125 MHz
- Low cycle-to-cycle and period jitter
- 100-lead PBGA package
- 100-lead Pb-free Package Available
- 3.3V supply with 3.3V or 2.5V output LVCMOS drive
- Supports computing, networking, telecommunications applications
- Ambient temperature range –40°C to +85°C

Functional Description

The MPC9850 uses either a 25 or 33 MHz reference frequency to generate 8 LVCMOS output clocks, of which, the frequency is selectable from 16 MHz to 200 MHz. The reference is applied to the input of a PLL and multiplied to 2 GHz. Output dividers, divide this frequency by 10, 12, 15, 16, 18, 20, 24, 30, 40, 60 or 120 to produce output frequencies of 200, 166, 133, 125, 111, 100, 83 66 50 33 or 16 MHz. The single-ended LVCMOS outputs are divided into two banks of 4 low skew outputs each, for use in driving a microprocessor or microcontroller clock input as well as other system components. The 2 GHz PLL output frequency is also divided to produce a 125, 250 or 500 MHz clock output for Rapid I/O applications such as found on the PowerQUICC III communications processor. The input reference, either crystal or external input is also buffered to a separate output that my be used as the clock source for a Gigabit Ethernet PHY if desired.

The reference clock may be provided by either an external clock input of 25 MHz or 33 MHz. An internal oscillator requiring a 25 MHz crystal for frequency control may also be used. The external clock source my be applied to either of two clock inputs and selected via the CLK_SEL control input. Both single ended LVCMOS and differential LVPECL inputs are available. The crystal oscillator or external clock input is selected via the input pin of REF_SEL. Other than the crystal, no external components are required for crystal oscillator operation. The REF_33MHz configuration pins is used to select between a 33 and 25 MHz input frequency.

The MPC9850 is packaged in a 100 lead MAPBGA package to optimize both performance and board density.

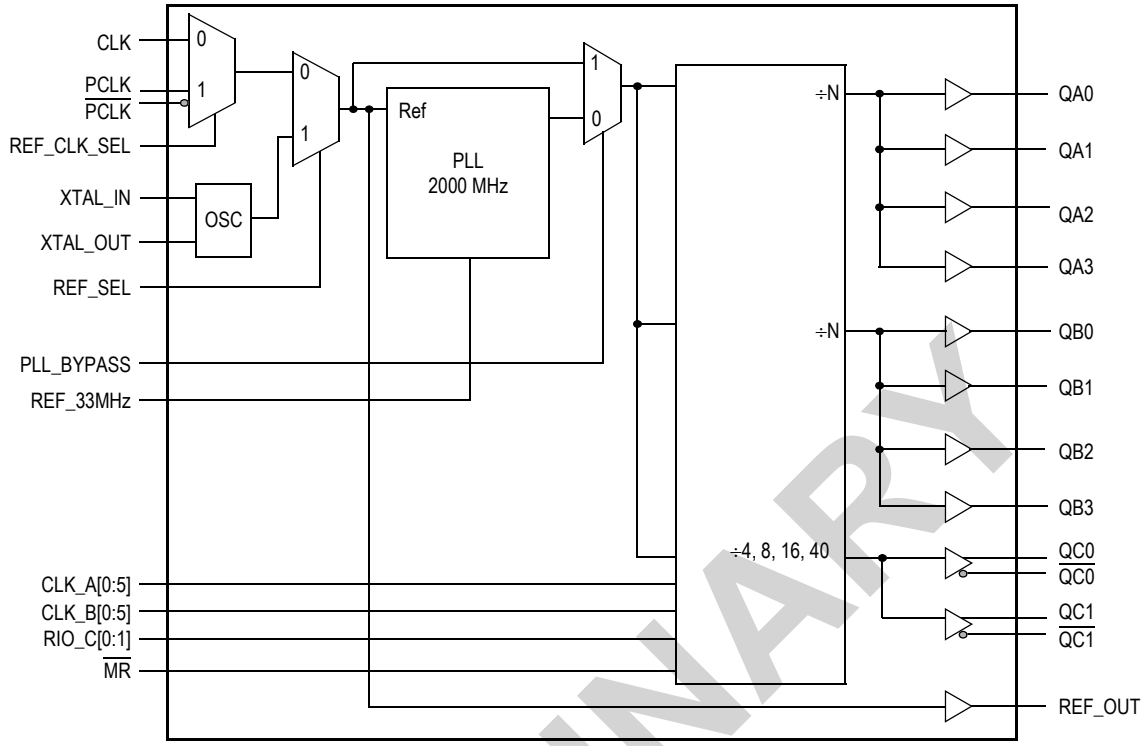


Figure 1. MPC9850 Logic Diagram

Table 1. Pin Configurations

Pin	I/O	Type	Function	Supply	Active/State
CLK	Input	LVCMOS	PLL Reference Clock Input (pull-down)	V_{DD}	
PCLK, $\overline{PCLK}$	Input	LVPECL	PLL Reference Clock Input (PCLK - pull-down, $\overline{PCLK}$ - pull-up and pull-down)	V_{DD}	
QA0, QA1, QA2, QA3	Output	LVCMOS	Bank A Outputs	V_{DDOA}	
QB0, QB1, QB2, QB3	Output	LVCMOS	Bank B Outputs	V_{DDOB}	
QC0, QC1, $\overline{QC0}$, $\overline{QC1}$	Output	LVDS	Bank C Outputs	V_{DDOC}	
REF_OUT	Output	LVCMOS	Reference Output (25 MHz or 33 MHz)	V_{DD}	
XTAL_IN	Input	LVCMOS	Crystal Oscillator Input Pin	V_{DD}	
XTAL_OUT	Output	LVCMOS	Crystal Oscillator Output Pin	V_{DD}	
REF_CLK_SEL	Input	LVCMOS	Select between CLK and PCLK Input (pull-down)	V_{DD}	High
REF_SEL	Input	LVCMOS	Select between External Input and Crystal Oscillator Input (pull-down)	V_{DD}	High
REF_33MHz	Input	LVCMOS	Selects 33MHz Input (pull-down)	V_{DD}	High
$\overline{MR}$	Input	LVCMOS	Master Reset (pull-up)	V_{DD}	Low
PLL_BYPASS	Input	LVCMOS	Select PLL or static test mode (pull-down)	V_{DD}	High
CLK_A[0:5][1]	Input	LVCMOS	Configures Bank A clock output frequency (pull-up)	V_{DD}	High
CLK_B[0:5][2]	Input	LVCMOS	Configures Bank B clock output frequency (pull-up)	V_{DD}	High
RIO_C [0:1]	Input	LVCMOS	Configures Bank C clock output frequency (pull-down)	V_{DD}	
V_{DD}			3.3 V Supply		
V_{DDA}			Analog Supply		
V_{DDOA}			Supply for Output Bank A		
V_{DDOB}			Supply for Output Bank B		
GND			Ground		

1. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb)
2. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb)
   PowerPC bit ordering (bit 0 = msb, bit 1 = lsb)

Table 2. Function Table

Control	Default	0	1
REF_CLK_SEL	0	CLK	PCLK
REF_SEL	0	CLK or PCLK	XTAL
PLL_BYPASS	0	Normal	Bypass
REF_33MHz	0	Selects 25 MHz Reference	Selects 33 MHz Reference
$\overline{MR}$	1	Reset	Normal

CLK_A, CLK_B, and RIO_C control output frequencies. See Table 3 and Table 4 for specific device configuration

Table 3. Output Configurations (Banks A & B)

CLK_x[0:5][1]	CLK_x[0] (msb)	CLK_x[1]	CLK_x[2]	CLK_x[3]	CLK_x[4]	CLK_x[5] (lsb)	N	Frequency (MHz)
111111	1	1	1	1	1	1	126	15.87
111100	1	1	1	1	0	0	120	16.67
101000	1	0	1	0	0	0	80	25.00
011110	0	1	1	1	1	0	60	33.33
010100	0	1	0	1	0	0	40	50.00
001111	0	0	1	1	1	1	30	66.67
001100	0	0	1	1	0	0	24	83.33
001010	0	0	1	0	1	0	20	100.00
001001	0	0	1	0	0	1	18	111.11
001000	0	0	1	0	0	0	16	125.00
000111	0	0	0	1	1	1	15	133.33
000110	0	0	0	1	1	0	12	166.67
000101	0	0	0	1	0	1	10	200.00
000100	0	0	0	1	0	0	8[2]	250

1. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb)
2. Minimum value for N

Table 4. Output Configurations (Bank C)

RIO_C[0:1]	Frequency (MHz)
00	50 (test output)
01	125
10	250
11	500

OPERATION INFORMATION

Output Frequency Configuration

The MPC9850 was designed to provide the commonly used frequencies in PowerQUICC, PowerPC and other microprocessor systems. Table 3 lists the configuration values that will generate those common frequencies. The MPC9850 can generate numerous other frequencies that may be useful in specific applications. The output frequency (f_{out}) of either Bank A or Bank B may be calculated by the following equation.

$$f_{out} = 2000 / N$$

where f_{out} is in MHz and N = 2 * CLK_x[0:5]

This calculation is valid for all values of N from 8 to 126. Note that N = 15 is a modified case of the configuration inputs CLK_x[0:5]. To achieve N = 15 CLK_x[0:5] is configured to 00111 or 7.

Crystal Input Operation

TBD

Power-Up and $\overline{MR}$ Operation

Figure 2 defines the release time and the minimum pulse length for $\overline{MR}$ pin. The $\overline{MR}$ release time is based upon the power supply being stable and within V_{DD} specifications. See Table 11 for actual parameter values. The MPC9850 may be configured after release of reset and the outputs will be stable for use after lock indication is obtained.

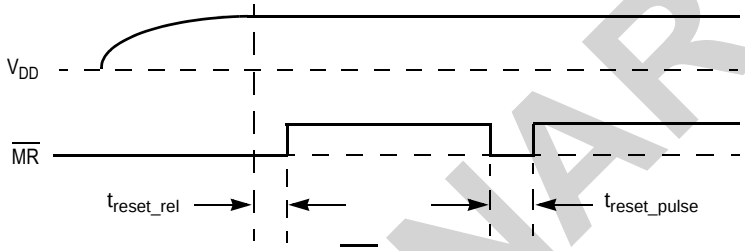


Figure 2. $\overline{MR}$ Operation

Power Supply Bypassing

The MPC9850 is a mixed analog/digital product. The architecture of the MPC9850 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{DD} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

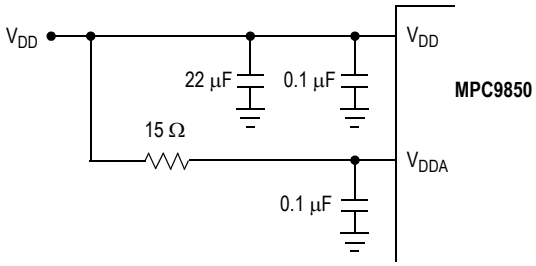


Figure 3. V_{CC} Power Supply Bypass

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{DD}	Supply Voltage (core)	–0.3	3.8	V	
V_{DDA}	Supply Voltage (Analog Supply Voltage)	–0.3	V_{DD}	V	
V_{DDOA}	Supply Voltage (LVCMOS output for Bank A)	–0.3	V_{DD}	V	
V_{DDOB}	Supply Voltage (LVCMOS output for Bank B)	–0.3	V_{DD}		
V_{IN}	DC Input Voltage	–0.3	V_{DD}+0.3	V	
V_{OUT}	DC Output Voltage[2]	–0.3	V_{DDx}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.
2. V_{DDx} references power supply pin associated with specific output pin.

Table 6. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{DD} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
CDM	ESD Protection (Charged Device Model)	500			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4		pF	Inputs
C_{PD}	Power Dissipation Capacitance		10		pF	Per Output
θ_{JC}	Thermal Resistance (junction-to-ambient)		54.5		°C/W	Air Flow = 0
T_A	Ambient Temperature	–40		85	°C	

Table 7. DC Characteristics (T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Supply Current for V_{DD} = 3.3 V ± 5%, V_{DDOA} = 3.3 V ± 5%, = V_{DDOB} = 3.3 V ± 5%						
$I_{DD} + I_{DDA} + I_{DDOC}$	Maximum Quiescent Supply Current (Core)		100		mA	$V_{DD} + V_{DDA} + V_{DDOC}$ pins
I_{DDA}	Maximum Quiescent Supply Current (Analog Supply)		15		mA	V_{DDIN} pins
I_{DDOA}	Maximum Bank A Supply Current		50		mA	V_{DDOA} pins
I_{DDOB}	Maximum Bank B Supply Current		50		mA	V_{DDOB} pins
Supply Current for V_{DD} = 3.3 V ± 5%, V_{DDOA} = 2.5 V ± 5%, V_{DDOB} = 2.5 V ± 5%						
$I_{DD} + I_{DDA} + I_{DDOC}$	Maximum Quiescent Supply Current (Core)		100		mA	$V_{DD} + V_{DDA} + V_{DDOC}$ pins
I_{DDA}	Maximum Quiescent Supply Current (Analog Supply)		15		mA	V_{DDIN} pins
I_{DDOA}	Maximum Bank A Supply Current		40		mA	V_{DDOA} pins
I_{DDOB}	Maximum Bank B Supply Current		40		mA	V_{DDOA} and V_{DDOB} pins

Table 8. LVDS DC Characteristics (T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential LVDS clock outputs (QC0, $\overline{QC0}$ and QC1, $\overline{QC1}$) for V_{DD} = 3.3 V ± 5% and V_{DDOC} = 3.3 V ± 5%						
V_{PP}	Output Differential Voltage[1] (peak-to-peak) (LVDS)	250		400	mV	
V_{OS}	Output Offset Voltage (LVDS)	1125		1275	mV	

1. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.

Table 9. LVPECL DC Characteristics (T_A = –40°C to 85°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential LVPECL clock inputs (CLK1, $\overline{CLK1}$) for V_{DD} = 3.3 V ± 0.5%						
V_{PP}	Differential Voltage[2] (peak-to-peak) (LVPECL)	250			mV	
V_{CMR}	Differential Input Crosspoint Voltage[3] (LVPECL)	1.0		V_{DD} – 0.6	V	

1. AC characteristics are design targets and pending characterization.
2. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.

Table 10. LVCMOS I/O DC Characteristics (T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS for V_{DD} = 3.3 V ± 5%						
V_{IH}	Input High Voltage	2.0		V_{DD} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[1]			200	μA	V_{IN} = V_{DDL} or GND
LVCMOS for V_{DD} = 3.3 V ± 5%, V_{DDOA} = 3.3 V ± 5%, V_{DDOB} = 3.3 V ± 5%						
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 24 mA
Z_{OUT}	Output Impedance		14 – 17		Ω	
LVCMOS for V_{DD} = 3.3 V ± 5%, V_{DDOA} = 2.5 V ± 5%, V_{DDOB} = 2.5 V ± 5%						
V_{OH}	Output High Voltage	1.9			V	I_{OH} = –15 mA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 15 mA
Z_{OUT}	Output Impedance		18 – 22		Ω	

1. Inputs have pull-down resistors affecting the input current.

Table 11. AC Characteristics (V_{DD} = 3.3 V ± 5%, V_{DDOA} = 3.3 V ± 5%, V_{DDOB} = 3.3 V ± 5%, T_A = –40°C to +85°C)[1] [2]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Input and Output Timing Specification						
f_{ref}	Input Reference Frequency (25 MHz input) Input Reference Frequency (33 MHz input) XTAL Input Input Reference Frequency in PLL Bypass Mode[3]		25 33 25	 250	MHz MHz MHz MHz	 PLL bypass
f_{VCO}	VCO Frequency Range[4]		2000		MHz	
f_{MCX}	Output Frequency Bank A Output Bank B output Bank C output	15.87 15.87 50		200 200 500	MHz MHz MHz	PLL locked
f_{refPW}	Reference Input Pulse Width	2			ns	
f_{refCcc}	Input Frequency Accuracy			100	ppm	
t_r, t_f	Output Rise/Fall Time	150		500	ns	20% to 80%
DC	Output Duty Cycle	47.5 45	50 50	52.5 55	%	3.3 V operation 2.5 V operation
PLL Specifications						
BW	PLL Closed Loop Bandwidth[5]			1	MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	
t_{reset_ref}	MR Hold Time on Power Up	10			ns	
t_{reset_pulse}	MR Hold Time	10			ns	
Skew and Jitter Specifications						
$t_{sk(O)}$	Output-to-Output Skew (within a bank)		50		ps	
$t_{sk(O)}$	Output-to-Output Skew (across banks A and B)		100		ps	V_{DDOA} = 3.3 V V_{DDOB} = 3.3 V
$t_{JIT(CC)}$	Cycle-to-cycle jitter		100 80		ps	Bank A and B Back C
$t_{JIT(PER)}$	Period Jitter		100 80		ps	Bank A and B Back C
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)		15 15		ps	Bank A and B Back C

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. In bypass mode, the MPC9850 divides the input reference clock.
4. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = (f_{VCO} \div M) \cdot N$.
5. –3 dB point of PLL transfer characteristics.

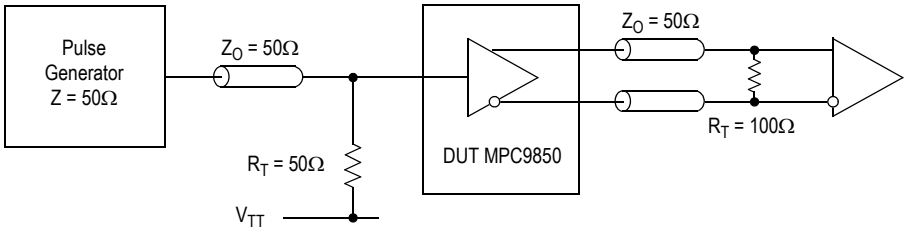


Figure 4. MPC9850 AC Test Reference (LVDS Outputs)

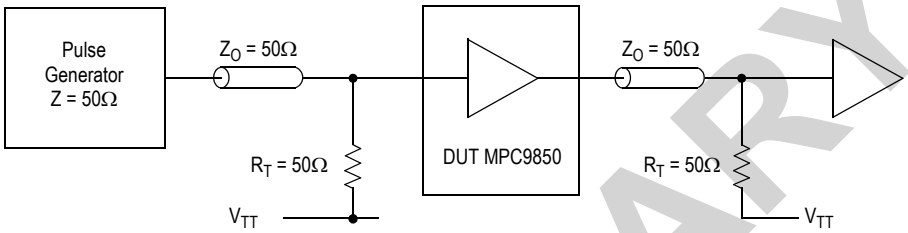


Figure 5. MPC9850 AC Test Reference (LVCMOS Outputs)

Table 12. MPC9850 Pin Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10
A	V_{DDOA}	V_{DDOA}	CLKA[1]	CLKA[3]	CLKA[5]	V_{DD}	QA1	QA2	V_{DDOA}	V_{DDOA}
B	V_{DDOA}	V_{DDOA}	CLKA[0]	CLKA[2]	CLKA[4]	QA0	V_{DDOA}	QA3	V_{DDOA}	V_{DDOA}
C	RSVD	RSVD	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	REF_OUT
D	V_{DDA}	V_{DDA}	V_{DD}	GND	GND	GND	GND	V_{DD}	$\overline{QC0}$	QC0
E	REF_SEL	CLK	V_{DD}	GND	GND	GND	GND	V_{DD}	V_{DDOC}	GND
F	PCLK	$\overline{PCLK}$	V_{DD}	GND	GND	GND	GND	V_{DD}	$\overline{QC1}$	QC1
G	REF_CLK_SEL	REF_33MHz	V_{DD}	GND	GND	GND	GND	V_{DD}	PLL_BYPASS	$\overline{MR}$
H	XTAL_IN	XTAL_OUT	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	RIO_C[1]	RIO_C[0]
J	V_{DDOB}	V_{DDOB}	CLKB[0]	CLKB[2]	CLKB[4]	QB0	V_{DDOB}	QB3	V_{DDOB}	V_{DDOB}
K	V_{DDOB}	V_{DDOB}	CLKB[1]	CLKB[3]	CLKB[5]	V_{DD}	QB1	QB2	V_{DDOB}	V_{DDOB}

Table 13. MPC9850 Pin List

Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA
V_{DDOA}	A1	RSVD[1]	C1	REF_SEL	E1	REF_CLK_SEL	G1	V_{DDOB}	J1
V_{DDOA}	A2	RSVD[1]	C2	CLK	E2	REF_33MHz	G2	V_{DDOB}	J2
CLKA[1]	A3	V_{DD}	C3	V_{DD}	E3	V_{DD}	G3	CLKB[0]	J3
CLKA[3]	A4	V_{DD}	C4	GND	E4	GND	G4	CLKB[2]	J4
CLKA[5]	A5	V_{DD}	C5	GND	E5	GND	G5	CLKB[4]	J5
V_{DD}	A6	V_{DD}	C6	GND	E6	GND	G6	QB0	J6
QA1	A7	V_{DD}	C7	GND	E7	GND	G7	V_{DDOB}	J7
QA2	A8	V_{DD}	C8	V_{DD}	E8	V_{DD}	G8	QB3	J8
V_{DDOA}	A9	V_{DD}	C9	V_{DDOC}	E9	PLL_BYPASS	G9	V_{DDOB}	J9
V_{DDOA}	A10	REF_OUT	C10	GND	E10	$\overline{MR}$	G10	V_{DDOB}	J10
V_{DDOA}	B1	V_{DDA}	D1	PCLK	F1	XTAL_IN	H1	V_{DDOB}	K1
V_{DDOA}	B2	V_{DDA}	D2	$\overline{PCLK}$	F2	XTAL_OUT	H2	V_{DDOB}	K2
CLKA[0]	B3	V_{DD}	D3	V_{DD}	F3	V_{DD}	H3	CLKB[1]	K3
CLKA[2]	B4	GND	D4	GND	F4	V_{DD}	H4	CLKB[3]	K4
CLKA[4]	B5	GND	D5	GND	F5	V_{DD}	H5	CLKB[5]	K5
QA0	B6	GND	D6	GND	F6	V_{DD}	H6	V_{DD}	K6
V_{DDOA}	B7	GND	D7	GND	F7	V_{DD}	H7	QB1	K7
QA3	B8	V_{DD}	D8	V_{DD}	F8	V_{DD}	H8	QB2	K8
V_{DDOA}	B9	$\overline{QC0}$	D9	$\overline{QC1}$	F9	RIO_C[1]	H9	V_{DDOB}	K9
V_{DDOA}	B10	QC0	D10	QC1	F10	RIO_C[0]	H10	V_{DDOB}	K10

1. RSVD pins must be left open.

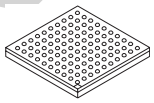
Order number: MPC9855
Rev 1, 07/2004

Preliminary Information

MPC9855

Clock Generator for PowerQUICC and PowerPC Microprocessors

MICROPROCESSOR CLOCK GENERATOR



VF SUFFIX
VM SUFFIX (Pb-FREE)
100 MAPBGA PACKAGE
CASE 1462-01

The MPC9855 is a PLL based clock generator specifically designed for Motorola Microprocessor and Microcontroller applications including the PowerPC and PowerQUICC. This device generates a microprocessor input clock. The microprocessor clock is selectable in output frequency to any of the commonly used microprocessor input and bus frequencies. The device offers eight low skew clock outputs in two banks, each configurable to support different clock frequencies. The extended temperature range of the MPC9855 supports telecommunication and networking requirements.

Features

- 8 LVCMOS outputs for processor and other circuitry
- Crystal oscillator or external reference input
- 25 or 33 MHz Input reference frequency
- Selectable output frequencies include = 200, 166, 133,125, 111, 100, 83, 66, 50, 33, or 16 MHz
- Buffered reference clock output (2 copies)
- Low cycle-to-cycle and period jitter
- 100-lead PBGA package
- 100-lead Pb-free Package Available
- 3.3 V supply with 3.3 V or 2.5 V LVCMOS output supplies
- Supports computing, networking, telecommunications applications
- Ambient temperature range –40°C to +85°C
- 100-lead PBGA package
- 100-lead Pb-free Package Available

Functional Description

The MPC9855 uses either a 25 or 33 MHz reference frequency to generate 8 LVCMOS output clocks, of which, the frequency is selectable from 16 MHz to 200 MHz. The reference is applied to the input of a PLL and multiplied to 2 GHz. Output dividers, divide this frequency by 10, 12, 15, 16, 18, 20, 24, 30, 40, 60, or 120 to produce output frequencies of 200, 166, 133, 125, 111, 100, 83, 66, 50, 33, or 16 MHz. The single-ended LVCMOS outputs provide 8 low skew outputs for use in driving a microprocessor or microcontroller clock input as well as other system components. The input reference, either crystal or external input is also buffered to a separate dual outputs that my be used as the clock source for a Ethernet PHY if desired.

The reference clock may be provided by either an external clock input of 25 or 33 MHz. An internal oscillator requiring a 25 MHz crystal for frequency control may also be used. The external clock source my be applied to either of two clock inputs and selected via the CLK_SEL control input. Both single ended LVCMOS and differential LVPECL inputs are available. The crystal oscillator or external clock input is selected via the input pin of XTAL_SEL. Other than the crystal, no external components are required for crystal oscillator operation. The REF_33 MHz configuration pin is used to select between a 33 and 25 MHz input frequency.

The MPC9855 is packaged in a 100 lead MAPBGA package to optimize both performance and board density.

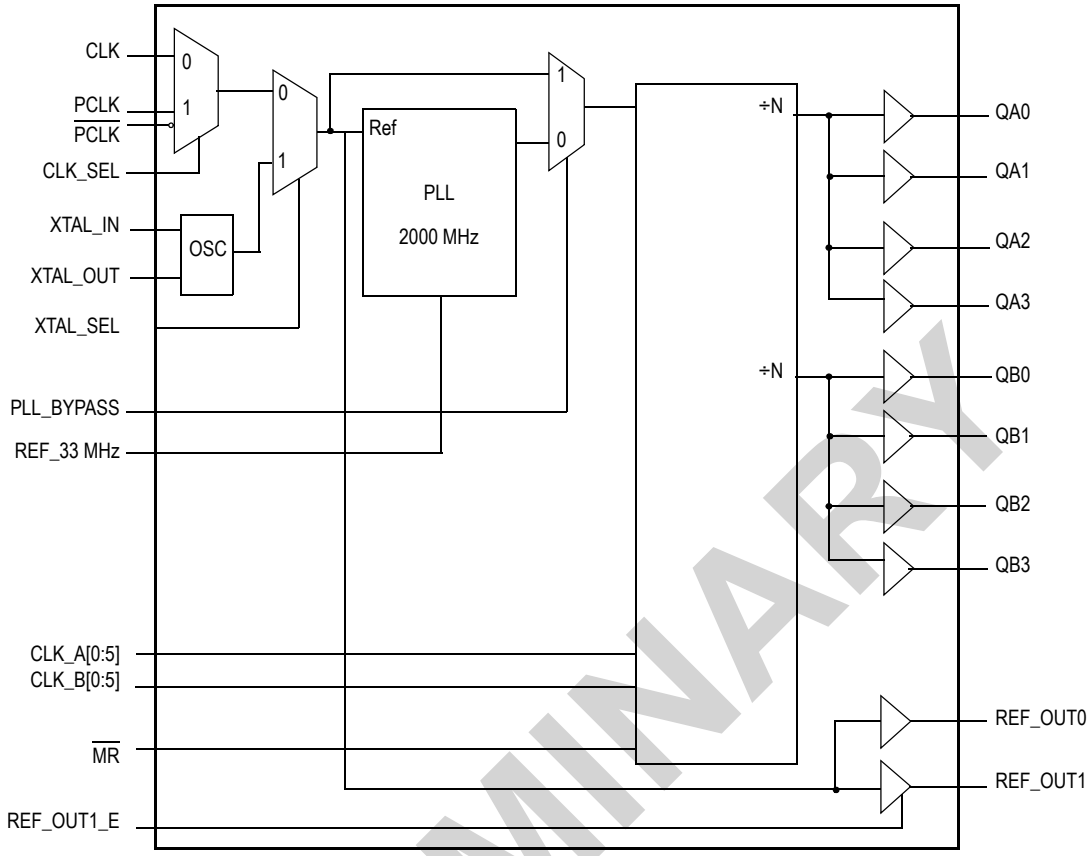


Figure 1. MPC9855 Logic Diagram

Table 1. Pin Configurations

Pin	I/O	Type	Function	Supply	Active/State
CLK	Input	LVCMOS	PLL reference clock input (pull-down)	V_{DD}	—
PCLK, $\overline{PCLK}$	Input	LVPECL	PLL reference clock input (PCLK — pull-down, $\overline{PCLK}$ — pull-up and pull-down)	V_{DD}	—
QA0, QA1, QA2, QA3 QB0, QB1, QB2, QB3	Output	LVCMOS	Clock Outputs	V_{DDOA}	—
REF_OUT0 REF_OUT1	Output	LVCMOS	Reference Output (25 MHz or 33 MHz)	V_{DD}	—
XTAL_IN	Input	LVCMOS	Crystal Oscillator Input Pin	V_{DD}	—
XTAL_OUT	Output	LVCMOS	Crystal Oscillator Output Pin	V_{DD}	—
CLK_SEL	Input	LVCMOS	Select between CLK and PCLK input (pull-down)	V_{DD}	High
XTAL_SEL	Input	LVCMOS	Select between External Input and Crystal Oscillator Input (pull-down)	V_{DD}	High
REF_33 MHz	Input	LVCMOS	Selects 33MHz input (pull-down)	V_{DD}	High
REF_OUT1_E	Input	LVCMOS	Enables REF_OUT! output (pull-down)	V_{DD}	High
$\overline{MR}$	Input	LVCMOS	Master Reset (pull-up)	V_{DD}	Low
PLL_BYPASS	Input	LVCMOS	Select PLL or static test mode (pull-up)	V_{DD}	High
CLK_A[0:5][1]	Input	LVCMOS	Configures Bank A clock output frequency (pull-up)	V_{DD}	—
CLK_**B**[0:5][1]	Input	LVCMOS	Configures Bank B clock output frequency (pull-up)	V_{DD}	—
V_{DD}	—	—	3.3 V Supply	—	—
V_{DDA}	—	—	Analog Supply	—	—
V_{DDOA}	—	—	Output Supply — Bank A	—	—
V_{DDOB}	—	—	Output Supply — Bank B	—	—
GND	—	—	Ground	—	—

1. Power PC bit ordering (bit 0 = msb, bit 5 = lsb).

Table 2. Function Table

Control	Default	0	1
CLK_SEL	0	CLK	PCLK
XTAL_SEL	0	CLKx	XTAL
PLL_BYPASS	0	Normal	Bypass
REF_OUT1_E	0	Disables REF_OUT1	Enables REF_OUT1
REF_33 MHz	0	Selects 25 MHz Reference	Selects 33 MHz Reference
$\overline{MR}$	1	Reset	Normal

CLK_A and CLK_B control output frequencies. Refer to Table 3 for specific device configuration

Table 3. Output Configurations (Banks A & B)

CLK_x[0:5][1]	CLK_x[0] (msb)	CLK_x[1]	CLK_x[2]	CLK_x[3]	CLK_x[4]	CLK_x[5] (lsb)	N	Frequency (MHz)
111111	1	1	1	1	1	1	126	15.87
111100	1	1	1	1	0	0	120	16.67
101000	1	0	1	0	0	0	80	25.00
011110	0	1	1	1	1	0	60	33.33
010100	0	1	0	1	0	0	40	50.00
001111	0	0	1	1	1	1	30	66.67
001100	0	0	1	1	0	0	24	83.33
001010	0	0	1	0	1	0	20	100.00
001001	0	0	1	0	0	1	18	111.11
001000	0	0	1	0	0	0	16	125.00
000111	0	0	0	1	1	1	15	133.33
000110	0	0	0	1	1	0	12	166.67
000101	0	0	0	1	0	1	10	200.00
000100	0	0	0	1	0	0	8^2	250

1. PowerPC bit ordering (bit 0 = msb, bit 5 = lsb)
2. Minimum value for N.

OPERATION INFORMATION

Output Frequency Configuration

The MPC9855 was designed to provide the commonly used frequencies in PowerQUICC, PowerPC and other microprocessor systems. Table 3 lists the configuration values that will generate those common frequencies. The MPC9855 can generate numerous other frequencies that may be useful in specific applications. The output frequency (f_{out}) may be calculated by the following equation.

$$f_{out} = 2000 / N$$

where f_{out} is in MHz and N = 2 * CLK_x[0:5]

This calculation is valid for all values of N from 8 to 126. Note that N = 15 is a modified case of the configuration inputs CLK_x[0:5]. To achieve N = 15 CLK_x[0:5] is configured to 00111 or 7.

Crystal Input Operation

TBD

Power-Up and $\overline{MR}$ Operation

Figure 2 defines the release time and the minimum pulse length for $\overline{MR}$ pin. The $\overline{MR}$ release time is based upon the power supply being stable and within V_{DD} specifications. See Table 10 for actual parameter values. The MPC9855 may be configured after release of reset and the outputs will be stable for use after lock indication is obtained.

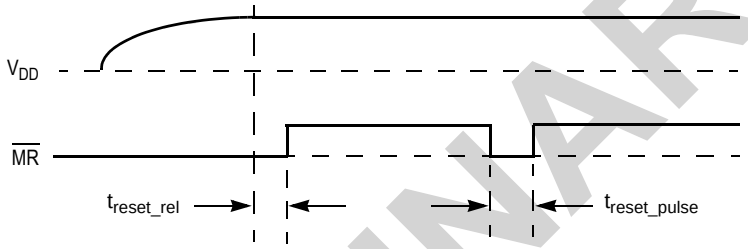


Figure 2. $\overline{MR}$ Operation

Power Supply Bypassing

The MPC9855 is a mixed analog/digital product. The architecture of the XC9855 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{DD} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

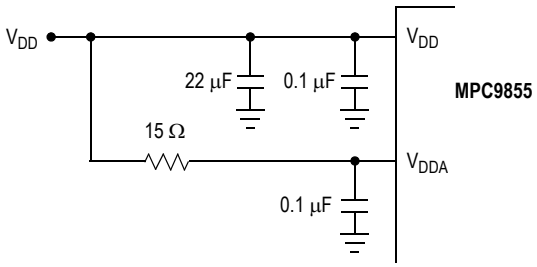


Figure 3. V_{CC} Power Supply Bypass

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{DD}	Supply Voltage (core)	–0.3	3.8	V	
V_{DDA}	Supply Voltage (Analog Supply Voltage)	–0.3	V_{DD}	V	
V_{DDOA}	Supply Voltage (LVCMOS output for Bank A)	–0.3	V_{DD}	V	
V_{DDOB}	Supply Voltage (LVCMOS output for Bank B)	–0.3	V_{DD}		
V_{IN}	DC Input Voltage	–0.3	V_{DD}+0.3	V	
V_{OUT}	DC Output Voltage[2]	–0.3	V_{DDx}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.
2. V_{DDx} references power supply pin associated with specific output pin.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{DD} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
CDM	ESD Protection (Charged Device Model)	500			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4		pF	Inputs
C_{PD}	Power Dissipation Capacitance		10		pF	Per Output
θ_{JC}	Thermal Resistance (junction-to-ambient)		54.5		°C/W	Air Flow = 0
T_A	Ambient Temperature	–40		85	°C	

Table 6. DC Characteristics (T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Supply Current for V_{DD} = 3.3 V ± 5%, V_{DDOA} = 3.3 V ± 5%, = V_{DDOB} = 3.3 V ± 5%						
I_{DD} + I_{DDA} + I_{DDOC}	Maximum Quiescent Supply Current (Core)		100		mA	V_{DD} + V_{DDA} + V_{DDOC} pins
I_{DDA}	Maximum Quiescent Supply Current (Analog Supply)		15		mA	V_{DDIN} pins
I_{DDOA}	Maximum Bank A Supply Current		50		mA	V_{DDOA} pins
I_{DDOB}	Maximum Bank B Supply Current		50		mA	V_{DDOB} pins
Supply Current for V_{DD} = 3.3 V ± 5%, V_{DDOA} = 2.5 V ± 5%, V_{DDOB} = 2.5 V ± 5%						
I_{DD} + I_{DDA} + I_{DDOC}	Maximum Quiescent Supply Current (Core)		100		mA	V_{DD} + V_{DDA} + V_{DDOC} pins
I_{DDA}	Maximum Quiescent Supply Current (Analog Supply)		15		mA	V_{DDIN} pins
I_{DDOA}	Maximum Bank A Supply Current		40		mA	V_{DDOA} pins
I_{DDOB}	Maximum Bank B Supply Current		40		mA	V_{DDOA} and V_{DDOB} pins

Table 7. LVPECL DC Characteristics (T_A = –40°C to 85°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential LVPECL clock inputs (CLK1, $\overline{CLK1}$) for V_{DD} = 3.3 V ± 0.5%						
V_{PP}	Differential Voltage[2] (peak-to-peak) (LVPECL)	250			mV	
V_{CMR}	Differential Input Crosspoint Voltage[3] (LVPECL)	1.0		V_{DD} – 0.6	V	

1. AC characteristics are design targets and pending characterization.
2. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.

Table 8. LVCMOS I/O DC Characteristics (T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS for V_{DD} = 3.3 V ± 5%						
V_{IH}	Input High Voltage	2.0		V_{DD} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[1]			200	μA	V_{IN} = V_{DDL} or GND
LVCMOS for V_{DD} = 3.3 V ± 5%, V_{DDOA} = 3.3 V ± 5%, V_{DDOB} = 3.3 V ± 5%						
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 24 mA
Z_{OUT}	Output Impedance		14 – 17		Ω	
LVCMOS for V_{DD} = 3.3 V ± 5%, V_{DDOA} = 2.5 V ± 5%, V_{DDOB} = 2.5 V ± 5%						
V_{OH}	Output High Voltage	1.9			V	I_{OH} = –15 mA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 15 mA
Z_{OUT}	Output Impedance		18 – 22		Ω	

1. Inputs have pull-down resistors affecting the input current.

Table 9. AC Characteristics (V_{DD} = 3.3 V ± 5%, V_{DDOA} = 3.3 V ± 5%, V_{DDOB} = 3.3 V ± 5%, T_A = –40°C to +85°C)[1] [2]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Input and Output Timing Specification						
f_{ref}	Input Reference Frequency (25 MHz input) Input Reference Frequency (33 MHz input) XTAL Input Input Reference Frequency in PLL Bypass Mode[3]		25 33 25	 250	MHz MHz MHz MHz	 PLL bypass
f_{VCO}	VCO Frequency Range[4]		2000		MHz	
f_{MCX}	Output Frequency Bank A output Bank B output Bank C output	15.87 15.87 50		200 200 500	MHz MHz MHz	PLL locked
f_{refPW}	Reference Input Pulse Width	2			ns	
f_{refCcc}	Input Frequency Accuracy			100	ppm	
t_r, t_f	Output Rise/Fall Time	150		500	ns	20% to 80%
DC	Output Duty Cycle	47.5 45	50 50	52.5 55	%	3.3 V operation 2.5 V operation
PLL Specifications						
BW	PLL Closed Loop Bandwidth[5]			1	MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	
t_{reset_ref}	MR Hold Time on Power Up	10			ns	
t_{reset_pulse}	MR Hold Time	10			ns	
Skew and Jitter Specifications						
$t_{sk(O)}$	Output-to-Output Skew (within a bank)		50		ps	
$t_{sk(O)}$	Output-to-Output Skew (across banks A and B)		100		ps	V_{DDOA} = 3.3 V V_{DDOB} = 3.3 V
$t_{JIT(CC)}$	Cycle-to-cycle jitter		100 80		ps	Bank A and B Back C
$t_{JIT(PER)}$	Period Jitter		100 80		ps	Bank A and B Back C
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1 σ)		15 15		ps	Bank A and B Back C

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. In bypass mode, the MPC9855 divides the input reference clock.
4. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{ref} = (f_{VCO} \div M) \cdot N$.
5. –3 dB point of PLL transfer characteristics.

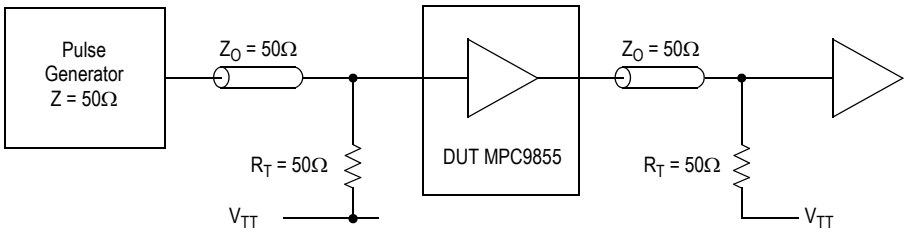


Figure 4. MPC9855 AC Test Reference (LVCMOS Outputs)

Table 10. MPC9855 Pin Diagram (Top View)

	1	2	3	4	5	6	7	8	9	10
A	V_{DDOA}	V_{DDOA}	CLKA[1]	CLKA[3]	CLKA[5]	V_{DD}	QA1	QA2	V_{DDOA}	V_{DDOA}
B	V_{DDOA}	V_{DDOA}	CLKA[0]	CLKA[2]	CLKA[4]	QA0	V_{DDOA}	QA3	V_{DDOA}	V_{DDOA}
C	RSVD	RSVD	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	REF_OUT[0]
D	V_{DDA}	V_{DDA}	V_{DD}	GND	GND	GND	GND	V_{DD}	RSVD	REF_OUT[1]
E	XTAL_SEL	CLK	V_{DD}	GND	GND	GND	GND	V_{DD}	V_{DD}	GND
F	PCLK	$\overline{PCLK}$	V_{DD}	GND	GND	GND	GND	V_{DD}	RSVD	RSVD
G	CLK_SEL	REF_33MHz	V_{DD}	GND	GND	GND	GND	V_{DD}	PLL_BYPASS	MR
H	XTAL_IN	XTAL_OUT	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	RSVD	REF_OUT1E
J	V_{DDOB}	V_{DDOB}	CLKB[0]	CLKB[2]	CLKB[4]	QB0	V_{DDOB}	QB3	V_{DDOB}	V_{DDOB}
K	V_{DDOB}	V_{DDOB}	CLKB[1]	CLKB[3]	CLKB[5]	V_{DD}	QB1	QB2	V_{DDOB}	V_{DDOB}

Table 11. MPC9855 Pin List

Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA	Signal	100 Pin MAPBGA
V_{DDOA}	A1	RSVD	C1	XTAL_SEL	E1	CLK_SEL	G1	V_{DDOB}	J1
V_{DDOA}	A2	RSVD	C2	CLK	E2	REF_33MHz	G2	V_{DDOB}	J2
CLKA[1]	A3	V_{DD}	C3	V_{DD}	E3	V_{DD}	G3	CLKB[0]	J3
CLKA[3]	A4	V_{DD}	C4	GND	E4	GND	G4	CLKB[2]	J4
CLKA[5]	A5	V_{DD}	C5	GND	E5	GND	G5	CLKB[4]	J5
V_{DD}	A6	V_{DD}	C6	GND	E6	GND	G6	QB0	J6
QA1	A7	V_{DD}	C7	GND	E7	GND	G7	V_{DDOB}	J7
QA2	A8	V_{DD}	C8	V_{DD}	E8	V_{DD}	G8	QB3	J8
V_{DDOA}	A9	V_{DD}	C9	V_{DD}	E9	PLL_BYPASS	G9	V_{DDOB}	J9
V_{DDOA}	A10	REF_OUT[0]	C10	GND	E10	$\overline{MR}$	G10	V_{DDOB}	J10
V_{DDOA}	B1	V_{DDA}	D1	PCLK	F1	XTAL_IN	H1	V_{DDOB}	K1
V_{DDOA}	B2	V_{DDA}	D2	$\overline{PCLK}$	F2	XTAL_OUT	H2	V_{DDOB}	K2
CLKA[0]	B3	V_{DD}	D3	V_{DD}	F3	V_{DD}	H3	CLKB[1]	K3
CLKA[2]	B4	GND	D4	GND	F4	V_{DD}	H4	CLKB[3]	K4
CLKA[4]	B5	GND	D5	GND	F5	V_{DD}	H5	CLKB[5]	K5
QA0	B6	GND	D6	GND	F6	V_{DD}	H6	V_{DD}	K6
V_{DDOA}	B7	GND	D7	GND	F7	V_{DD}	H7	QB1	K7
QA3	B8	V_{DD}	D8	V_{DD}	F8	V_{DD}	H8	QB2	K8
V_{DDOA}	B9	RSVD	D9	RSVD	F9	RSVD	H9	V_{DDOB}	K9
V_{DDOA}	B10	REF_OUT[1]	D10	RSVD	F10	REF_OUT1E	H10	V_{DDOB}	K10

Chapter Four
Failover or Redundant Clock Data Sheets

Failover or Redundant Clock Device Index

Order number: MPC9892
Rev 0, 12/2002

Product Preview

MPC9892

Intelligent Dynamic Clock Switch (IDCS) PLL Clock Driver

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC9892 is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two differential LVPECL clock signals from which it generates 5 new differential LVPECL clock outputs. Two of the output pairs regenerate the input signals frequency and phase while the other three pairs generate 4x, phase aligned clock outputs. External PLL feedback is used to also provide zero delay buffer performance.

Features

- Fully Integrated PLL
- Intelligent Dynamic Clock Switch
- LVPECL Clock Outputs
- LVCMOS Control I/O
- 3.3 V Operation
- 32-Lead LQFP Packaging
- SiGe technology supports near-zero output skew

Functional Description

The MPC9892 Intelligent Dynamic Clock Switch (IDCS) circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP_BAD for that CLK will be latched (H). If that CLK is the primary clock, the IDCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated. (See Application Information section).

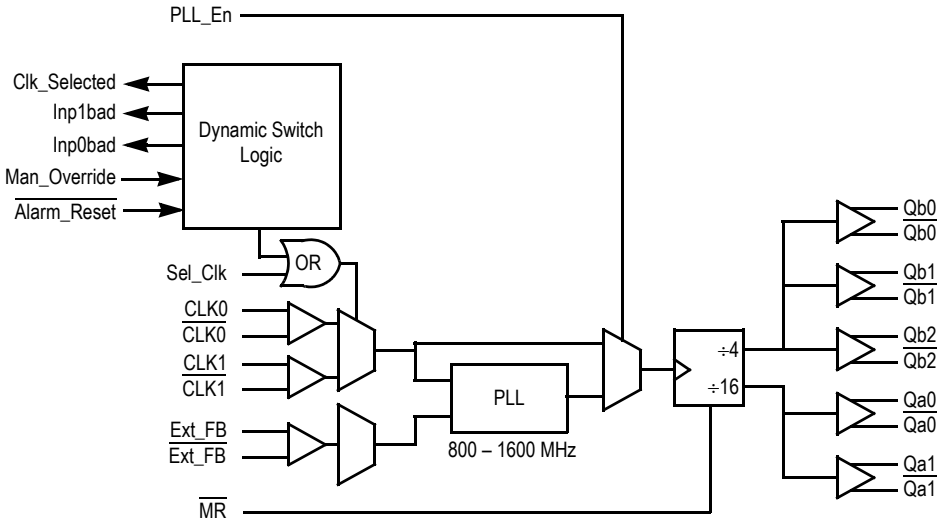


Figure 1. Block Diagram

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

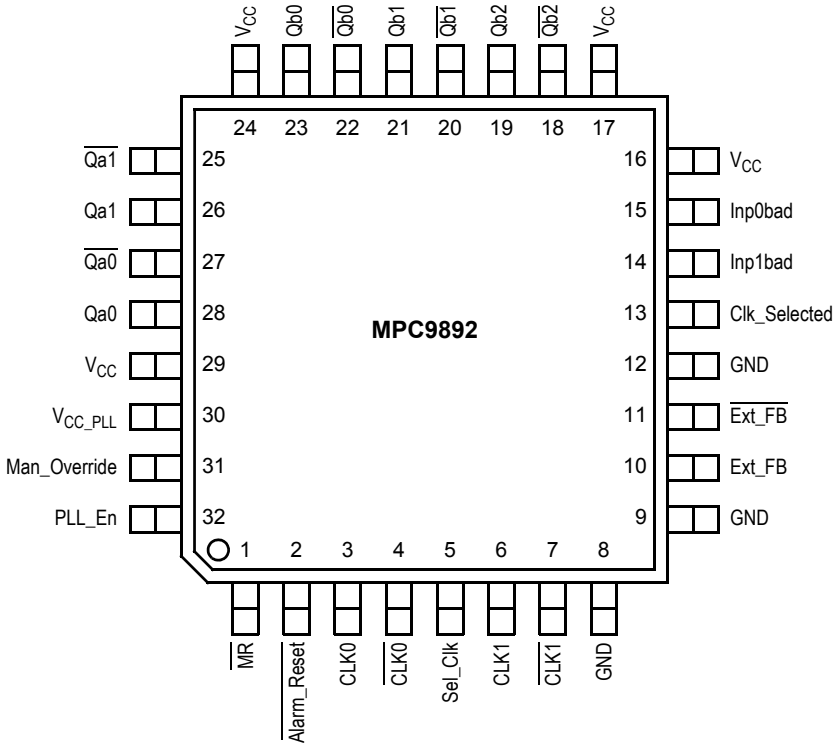


Figure 2. 32-Lead Pinout (Top View)

Table 1. Pin Descriptions

Pin Name	I/O	Pin Definition
CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	LVPECL Input LVPECL Input	Differential PLL clock reference (CLK0 pulldown, $\overline{\text{CLK0}}$ pullup) Differential PLL clock reference (CLK1 pulldown, $\overline{\text{CLK1}}$ pullup)
Ext_FB, $\overline{\text{Ext\_FB}}$	LVPECL Input	Differential PLL feedback clock (Ext_FB pulldown, $\overline{\text{Ext\_FB}}$ pullup)
Qa0:1, $\overline{\text{Qa0:1}}$	LVPECL Output	Differential 1x output pairs
Qb0:2, $\overline{\text{Qb0:2}}$	LVPECL Output	Differential 4x output pairs
Inp0bad	LVCMOS Output	Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Inp1bad	LVCMOS Output	Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Clk_Selected	LVCMOS Output	‘0' if clock 0 is selected, ‘1' if clock 1 is selected
$\overline{\text{Alarm\_Reset}}$	LVCMOS Input	‘0' will reset the input bad flags and align Clk_Selected with Sel_Clk. The input is “one-shotted” (50 kΩ pullup)
Sel_Clk	LVCMOS Input	‘0' selects CLK0, ‘1' selects CLK1 (50 kΩ pulldown)
Manual_Override	LVCMOS Input	‘1' disables internal clock switch circuitry (50 kΩ pulldown)
PLL_En	LVCMOS Input	‘0' bypasses selected input reference around the phase-locked loop (50 kΩ pullup)
$\overline{\text{MR}}$	LVCMOS Input	‘0' resets the internal dividers forcing Q outputs LOW. Asynchronous to the clock (50 kΩ pullup)
V_{CCA}	Power Supply	PLL power supply
V_{CC}	Power Supply	Digital power supply
GNDA	Power Supply	PLL
GND	Power Supply	Digital ground

Table 2. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine model)	TBD			V	
HBM	ESD Protection (Human body model)	TBD			V	
CDM	ESD Protection (Charged device model	TBD			V	
LU	Latch-up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient		83.1	86.0	°C/W	Natural convection
	JESD 51-3, single layer test board		73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board					
			59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
	Operating junction temperature[1] (continuous operation) MTBF = 9.1 years			110	°C	

1. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6226 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6226 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 4. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = -40° to +85°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs ($\overline{OE}$, FSEL0, FSEL1, MR)						
V_{IL}	Input Voltage Low			0.8	V	
V_{IH}	Input Voltage High	2.0			V	
I_{IN}	Input Current[2]			±TBD	μA	V_{IN} = V_{CC} or V_{IN} = GND
LVPECL clock inputs (CLK, $\overline{CLK}$)[3]						
V_{PP}	AC Differential Input Voltage[4]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[5]	1.0		V_{CC}–0.3	V	Differential operation
V_{IH}	Input High Voltage	TBD		TBD		
V_{IL}	Input Low Voltage	TBD		TBD		
I_{IN}	Input Current			±TBD	μA	V_{IN} = TBD or V_{IN} = TBD
LVPECL clock outputs (QA0-4, $\overline{QA0\text{-}4}$, QB0-4, $\overline{QB0\text{-}4}$)						
V_{OH}	Output High Voltage	TBD	V_{CC}–1.005	TBD	V	Termination 50 Ω to V_{TT}
V_{OL}	Output Low Voltage	TBD	V_{CC}–1.705	TBD	V	Termination 50 Ω to V_{TT}
I_{CC}	Maximum Power Supply V_{CC} pins			TBD	mA	
I_{CCA}	Maximum PLL Power Supply V_{CC_PLL} pin			TBD	mA	

1. AC characterisitics are design targets and pending characterization.
2. Input have internal pullup/pulldown resistors which affect the input current.
3. Clock inputs driven by LVPECL compatible signals.
4. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristic.
5. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 5. AC Characteristics (T_A = -40°C to 85°C, V_{CC} = 3.3 V ± 5%)[1]

Symbol	Parameter	Min	Typ	Max	Unit
f_{VCO}	PLL VCO Lock Range	800		1600	MHz
t_{pwi}	Input Pulse Width	25		75	%
t_{pd}	Propagation Delay[2] CLKn to Q (Bypass) CLKn to Ext_FB (Locked[3])			TBD TBD	ns ps
V_{PP}	Differential Input Voltage (peak-to-peak)		0.3	1.3	V
V_{CMR}	Differential Input Crosspoint Voltage			V_{CC}-0.3	V
t_r/t_f	Output Rise/Fall Time			TBD	ps
t_{skew}	Output Skew Within Bank All Outputs			35 50	ps
Δ_{pe}	Maximum Phase Error Deviation			TBD[4] TBD[5]	ps
$\Delta_{per/cycle}$	Rate of Change of Periods 75 MHz Output[2, 4] 300 MHz Output[2, 4] 75 MHz Output[2, 4] 300 MHz Output[2, 4]		20 10 200 100	50 25 400 200	ps/cycle
t_{pw}	Output Duty Cycle	45		55	%
t_{jitter}	Cycle-to-Cycle Jitter, Standard Deviation (RMS)[2]			20	ps
t_{lock}	Maximum PLL Lock Time			10	ms

1. PECL output termination is 50 ohms to V_{CC} – 2.0 V.
2. Guaranteed, not production tested.
3. Static phase offset between the selected reference clock and the feedback signal.
4. Specification holds for a clock switch between two signals no greater than 400 ps out of phase. Delta period change per cycle is averaged over the clock switch excursion. (See Applications Information for more detail)
5. Specification holds for a clock switch between two signals no greater than $\pm\pi$ out of phase. Delta period change per cycle is averaged over the clock switch excursion.

APPLICATIONS INFORMATION

The MPC9892 is a dual clock PLL with on-chip Intelligent Dynamic Clock Switch (IDCS) circuitry.

Definitions

primary clock: The input CLK selected by Sel_Clk.
secondary clock: The input CLK NOT selected by Sel_Clk.
PLL reference signal: The CLK selected as the PLL reference signal by Sel_Clk or IDCS. (IDCS can override Sel_Clk).

Status Functions

Clk_Selected: Clk_Selected (L) indicates CLK0 is selected as the PLL reference signal. Clk_Selected (H) indicates CLK1 is selected as the PLL reference signal.
INP_BAD: Latched (H) when it's CLK is stuck (H) or (L) for at least one Ext_FB period (Pos to Pos or Neg to Neg). Cleared (L) on assertion of Alarm_Reset.

Control Functions

Sel_Clk: Sel_Clk (L) selects CLK0 as the primary clock. Sel_Clk (H) selects CLK1 as the primary clock.
Alarm_Reset: Asserted by a negative edge. Generates a one-shot reset pulse that clears INPUT_BAD latches and Clk_Selected latch.
PLL_En: While (L), the PLL reference signal is substituted for the VCO output.
MR: While (L), internal dividers are held in reset which holds all Q outputs LOW.

Man Override (H)

(IDCS is disabled, PLL functions normally). PLL reference signal (as indicated by Clk_Selected) will always be the CLK selected by Sel_Clk. The status function INP_BAD is active in Man Override (H) and (L).

Man Override (L)

(IDCS is enabled, PLL functions enhanced). The first CLK to fail will latch it's INP_BAD (H) status flag and select the other input as the Clk_Selected for the PLL reference clock. Once latched, the Clk_Selected and INP_BAD remain latched until assertion of Alarm_Reset which clears all latches (INP_BADs are cleared and Clk_Selected = Sel_Clk). NOTE: If both CLKs are bad when Alarm_Reset is asserted, both INP_BADs will be latched (H) after one Ext_FB period and Clk_Selected will be latched (L) indicating CLK0 is the PLL reference signal. While neither INP_BAD is latched (H), the Clk_Selected can be freely changed with Sel_Clk. Whenever a CLK switch occurs, (manually or by IDCS), following the next negative edge of the newly selected PLL reference signal, the next positive edge pair of Ext_FB and the newly selected PLL reference signal will slew to alignment.

To calculate the overall uncertainty between the input CLKs and the outputs from multiple MPC9892's, the following procedure should be used. Assuming that the input CLKs to all MPC9892's are exactly in phase, the total uncertainty will be the sum of the static phase offset, max I/O jitter, and output to output skew.

During a dynamic switch, the output phase between two devices may be increased for a short period of time. If the two input CLKs are 400 ps out of phase, a dynamic switch of an MPC9892 will result in an instantaneous phase change of 400 ps to the PLL reference signal without a corresponding change in the output phase (due to the limited response of the PLL). As a result, the I/O phase of a device, undergoing this switch, will initially be 400 ps and diminish as the PLL slews to its new phase alignment. This transient timing issue should be considered when analyzing the overall skew budget of a system.

Hot Insertion and Withdrawal

In PECL applications, a powered up driver will experience a low impedance path through an MPC9892 input to its powered down VCC pins. In this case, a 100 ohm series resistance should be used in front of the input pins to limit the driver current. The resistor will have minimal impact on the rise and fall times of the input signals.

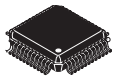
Acquiring Frequency Lock

1. While the MPC9892 is receiving a valid CLK signal, assert Man_Override HIGH.
2. The PLL will phase and frequency lock within the specified lock time.
3. Apply a HIGH to LOW transition to Alarm_Reset to reset Input Bad flags.
4. De-assert Man_Override LOW to enable Intelligent Dynamic Clock Switch mode.

3.3V 1:10 LVCMOS PLL Clock Generator

MPC9893

LOW VOLTAGE
2.5V AND 3.3V IDCS AND
PLL CLOCK GENERATOR



FA SUFFIX
48-LEAD LQFP PACKAGE
CASE 932-03

The MPC9893 is a 2.5V and 3.3V compatible, PLL based intelligent dynamic clock switch and generator specifically designed for redundant clock distribution systems. The device receives two LVCMOS clock signals and generates 12 phase aligned output clocks. The MPC9893 is able to detect a failing reference clock signal and to dynamically switch to a redundant clock signal. The switch from the failing clock to the redundant clock occurs without interruption of the output clock signal (output clock slews to alignment). The phase bump typically caused by a clock failure is eliminated.

The device offers 12 low skew clock outputs organized into two output banks, each configurable to support the different clock frequencies.

The extended temperature range of the MPC9893 supports telecommunication and networking requirements. The device employs a fully differential PLL design to minimize jitter.

Features

- 12-output LVCMOS PLL clock generator
- 2.5V and 3.3V compatible
- IDCS - on-chip intelligent dynamic clock switch
- Automatically detects clock failure
- Smooth output phase transition during clock failover switch
- 7.5 – 200 MHz output frequency range
- LVCMOS compatible inputs and outputs
- External feedback enables zero-delay configurations
- Supports networking, telecommunications and computer applications
- Output enable/disable and static test mode (PLL bypass)
- Low skew characteristics: maximum 50 ps output-to-output (within bank)
- 48-lead LQFP package
- 48-lead Pb-free package available
- Ambient operating temperature range of -40 to 85°C

Functional Description

The MPC9893 is a 3.3V or 2.5V compatible PLL clock driver and clock generator. The clock generator uses a fully integrated PLL to generate clock signals from redundant clock sources. The PLL multiplies the input reference clock signal by one, two, three, four or eight. The frequency-multiplied clock drives six bank A outputs. Six bank B outputs can run at either the same frequency than bank A or at half of the bank A frequency. Therefore, bank B outputs additionally support the frequency multiplication of the input reference clock by 3÷2 and 1÷2. Bank A and bank B outputs are phase-aligned(1). Due to the external PLL feedback, the clock signals of both output banks are also phase-aligned[1] to the selected input reference clock, providing virtually zero-delay capability. The integrated IDCS continuously monitors both clock inputs and indicates a clock failure individually for each clock input. When a false clock signal is detected, the MPC9893 switches to the redundant clock input, forcing the PLL to slowly slew to alignment and not produce any phase bumps at the outputs. Both clock inputs are interchangeable, also supporting the switch to a failed clock that was restored. The MPC9893 also provides a manual mode that allows for user-controlled clock switches.

The PLL bypass of the MPC9893 disables the IDCS and PLL-related specifications do not apply. In PLL bypass mode, the MPC9893 is fully static in order to distribute low-frequency clocks for system test and diagnosis. Outputs of the MPC9893 can be disabled (high-impedance tristate) to isolate the device from the system. Applying output disable also resets the MPC9893. On power-up this reset function needs to be applied for correct operation of the circuitry. Please see the application section for power-on sequence recommendations.

The device is packaged in a 7x7 mm^2 48-lead LQFP package.

1. At coincident rising edges.

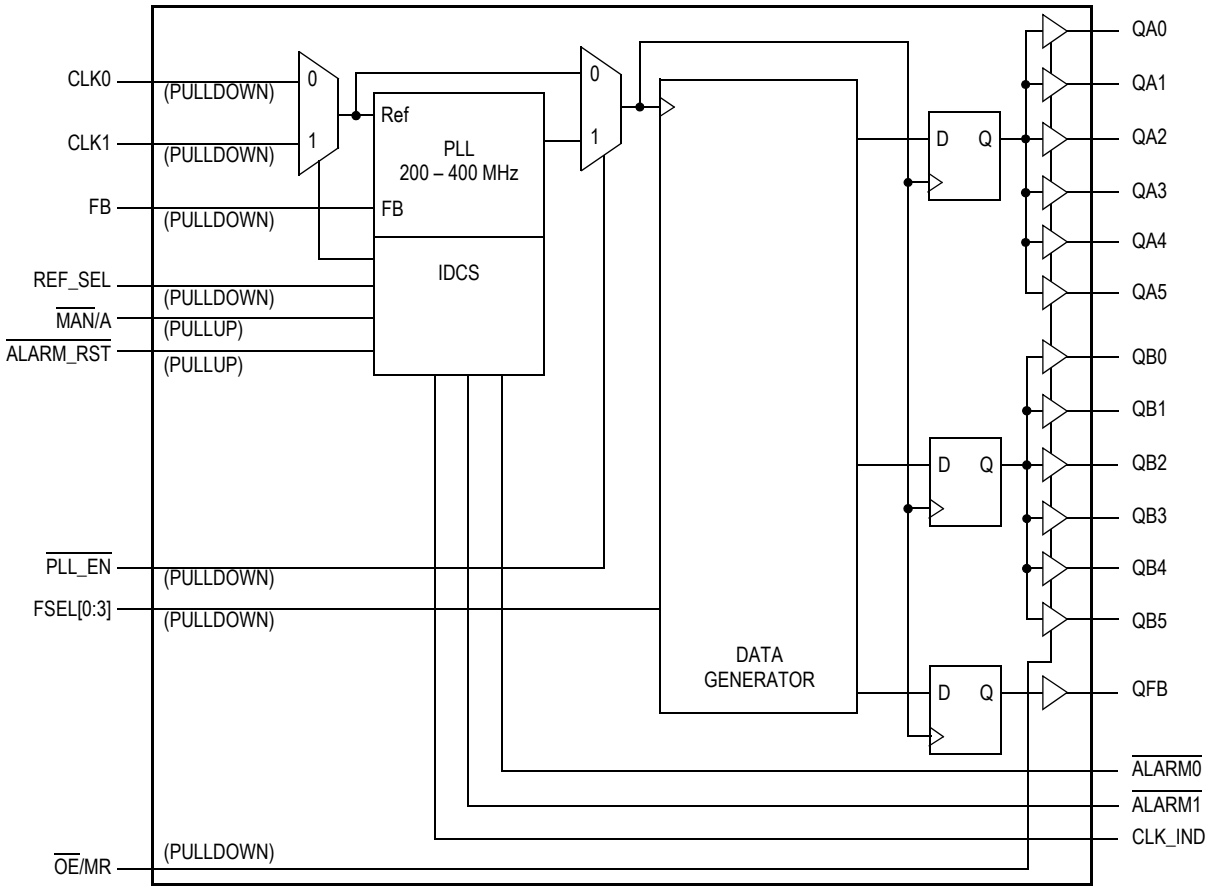
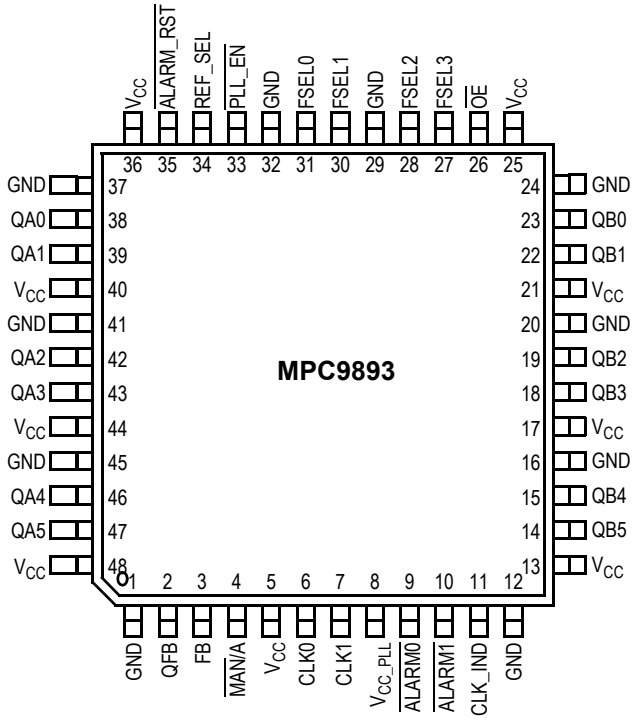


Figure 1. MPC9893 Logic Diagram



It is recommended to use an external RC filter for the analog power supply pin V_{CC_PPL}. Please see application section for details.

Figure 2. MPC9893 48-Lead Pinout (Top View)

Table 1. Pin Configurations

Number	Name	Type	Description
CLK0, CLK1	Input	LVCMOS	PLL reference clock inputs
FB	Input	LVCMOS	PLL feedback signal input, connect directly to QFB output
REF_SEL	Input	LVCMOS	Selects the primary reference clock
$\overline{\text{MAN}}$/A	Input	LVCMOS	Selects automatic switch mode or manual reference clock selection
$\overline{\text{ALARM\_RST}}$	Input	LVCMOS	Reset of alarm flags and selected reference clock
$\overline{\text{PLL\_EN}}$	Input	LVCMOS	Select PLL or static test mode
FSEL[0:3]	Input	LVCMOS	Clock frequency selection and configuration of clock divider modes
$\overline{\text{OE}}$/MR	Input	LVCMOS	Output enable/disable and device reset
QA[0:5]	Output	LVCMOS	Bank A clock outputs
QB[0:5]	Output	LVCMOS	Bank B clock outputs
QFB	Output	LVCMOS	Clock feedback output. QFB must be connected to FB for correct operation
$\overline{\text{ALARM0}}$	Output	LVCMOS	Indicates clock failure on CLK0
$\overline{\text{ALARM1}}$	Output	LVCMOS	Indicates clock failure on CLK1
CLK_IND	Output	LVCMOS	Indicates currently selected input reference clock
GND	Supply	Ground	Negative power supply
V_{CC_PLL}	Supply	V_{CC}	Positive power supply for the PLL (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see the application section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
Inputs			
$\overline{\text{PLL\_EN}}$	0	PLL enabled. The input to output frequency relationship is that according to Table 3 if the PLL is frequency locked.	PLL bypassed and IDCS disabled. The VCO output is replaced by the reference clock signal fref. The MPC9893 is in manual mode.
$\overline{\text{MAN}}$/A	1	Manual clock switch mode. **IDCS disabled**. Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled.	Automatic clock switch mode. **IDCS enabled**. Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled. IDCS overrides REF_SEL on a clock failure. IDCS operation requires $\overline{\text{PLL\_EN}}$ = 0.
$\overline{\text{ALARM\_RST}}$	1	$\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$ and CLK_IND flags are reset: $\overline{\text{ALARM0}}$=H, $\overline{\text{ALARM1}}$=H and CLK_IND=REF_SEL. $\overline{\text{ALARM\_RST}}$ is a one-shot function.	$\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$ and CLK_IND active
REF_SEL	0	Selects CLK0 as the primary clock source	Selects CLK1 as the secondary clock source
FSEL[0:3]	0000	See Table 3	
$\overline{\text{OE}}$/MR	0	Outputs enabled (active)	Outputs disabled (high impedance tristate), reset of data generators and output dividers. The MPC9893 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CLK0,1). $\overline{\text{OE}}$/MR does not tristate the QFB output.
Outputs ($\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$, CLK_IND are valid if PLL is locked)			
$\overline{\text{ALARM0}}$		CLK0 failure	
$\overline{\text{ALARM1}}$		CLK1 failure	
CLK_IND		CLK0 is the reference clock	CLK1 is the reference clock

Table 3. Clock Frequency Configuration

Name	FSEL0	FSEL1	FSEL2	FSEL3	f_{REF} range [MHz]	QAx		QBx		QFB	FB[1]
						Ratio	f_{QAX} [MHz]	Ratio	f_{QBX}[MHz]		
M8	0	0	0	0	15–25	f_{REF} * 8	120–200	f_{REF} * 8	120–200	f_{REF}	16
M82	0	0	0	1				f_{REF} * 4	60–100		
M4	0	0	1	0	30–50	f_{REF} * 4	120–200	f_{REF} * 4	120–200	f_{REF}	8
M42	0	0	1	1				f_{REF} * 2	60–100		
M3	0	1	0	0	40–66.6	f_{REF} * 3	120–200	f_{REF} * 3	120–200	f_{REF}	6
M32	0	1	0	1				f_{REF} * 3 ÷ 2	60–100		
M2M	0	1	1	0	30–50	f_{REF} * 2	60–100	f_{REF} * 2	60–100	f_{REF}	8
M22M	0	1	1	1				f_{REF}	30–50		
M2H	1	0	0	0	60–100	f_{REF} * 2	120–200	f_{REF} * 2	120–200	f_{REF}	4
M22H	1	0	0	1				f_{REF}	60–100		
M1L	1	0	1	0	15–25	f_{REF}	15–25	f_{REF}	15–25	f_{REF}	16
M12L	1	0	1	1				f_{REF} ÷ 2	7.5–12.5		
M1M	1	1	0	0	30–50	f_{REF}	30–50	f_{REF}	30–50	f_{REF}	8
M12M	1	1	0	1				f_{REF} ÷ 2	15–25		
M1H	1	1	1	0	60–100	f_{REF}	60–100.0	f_{REF}	60–100	f_{REF}	4
M12H	1	1	1	1				f_{REF} ÷ 2	30–50		

1. FB: Internal PLL feedback divider

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} ÷ 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
CDM	ESD Protection (Charged Device Model)	1500			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH}=–24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL}= 24 mA I_{OL}= 12 mA
Z_{OUT}	Output Impedance		14–17		Ω	
I_{IN}	Input Current			±200	μA	V_{IN}=V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CC_PLL} Pin
I_{CC}	Maximum Quiescent Supply Current			4.0	mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage		V_{CC}÷2		V	

1. The MPC9893 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

Table 7. DC Characteristics (V_{CC} = 2.5V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.8			V	I_{OH}=–15 mA[1]
V_{OL}	Output Low Voltage			0.6	V	I_{OL}= 15 mA
Z_{OUT}	Output Impedance		17–20		Ω	
I_{IN}	Input Current			±200	μA	V_{IN}=V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CC_PLL} Pin
I_{CC}	Maximum Quiescent Supply Current			4.0	mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage		V_{CC}÷2		V	

1. The MPC9893 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50W series terminated transmission lines per output.

Table 8. AC Characteristics (V_{CC} = 3.3V ± 5% or V_{CC} = 2.5V ± 5%, T_A = –40° to 85°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency					PLL locked
	FSEL=000x	15.0		25.0	MHz	
	FSEL=001x	30.0		50.0	MHz	
	FSEL=010x	40.0		66.6	MHz	
	FSEL=011x	30.0		50.0	MHz	
	FSEL=100x	60.0		100.0	MHz	
	FSEL=101x	15.0		12.5	MHz	
	FSEL=110x	30.0		50.0	MHz	
	FSEL=111x	60.0		100.0	MHz	
f_{MAX}	Maximum Output Frequency					PLL locked
	FSEL=000x	60.0		200.0	MHz	
	FSEL=001x	60.0		200.0	MHz	
	FSEL=010x	60.0		200.0	MHz	
	FSEL=011x	30.0		100.0	MHz	
	FSEL=100x	60.0		200.0	MHz	
	FSEL=101x	7.5		25.0	MHz	
	FSEL=110x	15.0		50.0	MHz	
	FSEL=111x	30.0		100.0	MHz	
f_{refDC}	Reference Input Duty Cycle	40		60	%	
t_r, t_f	CLK0, 1 Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset, CLKx to FB)					PLL locked
	V_{CC}=3.3V±5% and FSEL[0:2]=111	–60		+50	ps	
	V_{CC}=3.3V±5%	–200		+100	ps	
	V_{CC}=2.5V±5% and FSEL[0:2]=111	–125		+25	ps	
	V_{CC}=2.5V±5%	–400		+100	ps	
Δ t	Rate of Period Change (phase slew rate)					Failover switch
	QAx outputs			150	ps/cycle	
	QBx outputs (FSEL=xxx0)			150		
	QBx outputs (FSEL=xxx1)			300		
$t_{sk(O)}$	Output-to-Output Skew[2] (within bank)			150	ps	
	(bank-to-bank)			100	ps	
	(any output to QFB)			125	ps	
DC_O	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter[3] FSEL3=0			225	ps	See applications section
	FSEL3=1			425	ps	
$t_{JIT(PER)}$	Period Jitter[c] FSEL3=0			150	ps	See applications section
	FSEL3=1			250	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter[4]					See applications section
	FB=4: FSEL[0:2]=100 or 111 RMS (1 σ)			40	ps	
	FB=6: FSEL[0:2]=010 RMS (1 σ)			50	ps	
	FB=8: FSEL[0:2]=001, 011, or 110 RMS (1 σ)			55	ps	
	FB=16: FSEL[0:2]=000 or 101 RMS (1 σ)			70	ps	
BW	PLL Closed Loop Bandwidth[5] FSEL=111x		0.8-4.0		MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. See application section for part-to-part skew calculation.
3. Cycle-to-cycle and period jitter depend on the VCO frequency and output configuration. See the application section.
4. I/O jitter depends on the VCO frequency and internal PLL feedback divider FB. See <st-blue>APPLICATIONS INFORMATION for more information and for the calculation for other confidence factors than 1σ.
5. –3dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Definitions

IDCS: Intelligent Dynamic Clock Switch. The IDCS monitors both primary and secondary clock signals. Upon a failure of the primary clock signal, the IDCS switches to a valid secondary clock signal and status flags are set.

Reference clock signal fref: The clock signal that is selected by the IDCS or REF_SEL as the input reference to the PLL.

Manual mode: The reference clock frequency is selected by REF_SEL.

Automatic mode: The reference clock frequency is determined by the internal IDCS logic.

Primary clock: The input clock signal selected by REF_SEL. The primary clock may or may not be the reference clock, depending on switch mode and IDCS status.

Secondary clock: The input clock signal not selected by REF_SEL

Selected clock: The CLK_IND flag indicates the reference clock signal: CLK_IND = 0 indicates CLK0 is the clock reference signal, CLK_IND =1 indicates CLK1 is the reference clock signal.

Clock failure: A valid clock signal that is stuck (high or low) for at least one input clock period. The primary clock and the secondary clock is monitored for failure. Valid clock signals must be within the AC and DC specification for the input reference clock. A loss of clock is detected if as well as the loss of both clocks. In the case of both clocks lost, the MPC9893 will set the alarm flags and the PLL will stall. The MPC9893 does not monitor and detect changes in the input frequency.

Automatic Mode and IDCS Commanded Clock Switch

$\overline{\text{MAN}}$/A = 1, IDCS enabled: Both primary and secondary clocks are monitored. The first clock failure is reported by its $\overline{\text{ALARMx}}$ status flag (clock failure is indicated by a logic low). The $\overline{\text{ALARMx}}$ status is flag latched and remains latched until reset by assertion of $\overline{\text{ALARM\_RST}}$.

If the clock failure occurs on the primary clock, the IDCS attempts to switch to the secondary clock. The secondary clock signal needs to be valid for a successful switch. Upon a successful switch, CLK_IND indicates the reference clock, which may now be different as that originally selected by REF_SEL.

Manual Mode

$\overline{\text{MAN}}$/A = 0, IDCS disabled: PLL functions normally and both clocks are monitored. The reference clock signal will always be the clock signal selected by REF_SEL and will be indicated by CLK_IND.

Clock Output Transition

A clock switch, either in automatic or manual mode, follows the next negative edge of the newly selected reference clock signal. The feedback and newly selected reference clock edge will start to slew to alignment at the next positive edge of both signals. Output runt pulses are eliminated.

Reset

$\overline{\text{ALARM\_RST}}$ is asserted by a negative edge. It generates a one-shot reset pulse that clears both $\overline{\text{ALARMx}}$ latches and the CLK_IND latch. If both CLK0 and CLK1 are invalid or fail when $\overline{\text{ALARM\_RST}}$ is asserted, both $\overline{\text{ALARMx}}$ flags will be latched after one FB signal period and CLK_IND will be latched (L) indicating CLK0 is the reference signal. While neither $\overline{\text{ALARMx}}$ flag is latched ($\overline{\text{ALARMx}}$ = H), the CLK_IND can be freely changed with REF_SEL.

$\overline{\text{OE}}$/MR: Reset the data generator and output disable. Does not reset the IDCS flags.

Acquiring Frequency Lock at Startup

1. On startup, $\overline{\text{OE}}$/MR must be asserted to reset the output dividers. The IDCS should be disabled ($\overline{\text{MAN}}$/A=0) during startup to select the manual mode and the primary clock.
2. The PLL will attempt to gain lock if the primary clock is present on startup. PLL lock requires the specified lock time.
3. Applying a high to low transition to $\overline{\text{ALARM\_RST}}$ will clear the alarm flags.
4. Enable the IDCS ($\overline{\text{MAN}}$/A=1) to enable to IDCS.

Power Supply Filtering

The MPC9893 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the $V_{CC\_PLL\ (PLL)}$ power supply impacts the device characteristics, for instance I/O jitter. The MPC9893 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9893. Figure 3 illustrates a typical power supply filter scheme. The MPC9893 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 2 mA (5 mA maximum), assuming that a minimum of 2.325V (V_{CC}=3.3V or V_{CC}=2.5V) must be maintained on the V_{CC_PLL} pin. The resistor R_F shown in Figure 3 must have a resistance of 9-10Ω to meet the voltage drop criteria.

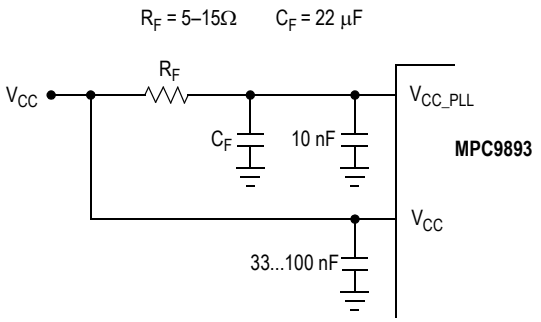


Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9893 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9893 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9893. Designs using the MPC9893 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9893 clock driver allows for its use as a zero delay buffer. The the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9893 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9893 are connected together, the maximum overall timing uncertainty from the common CLK0 or CLK1 input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of four components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

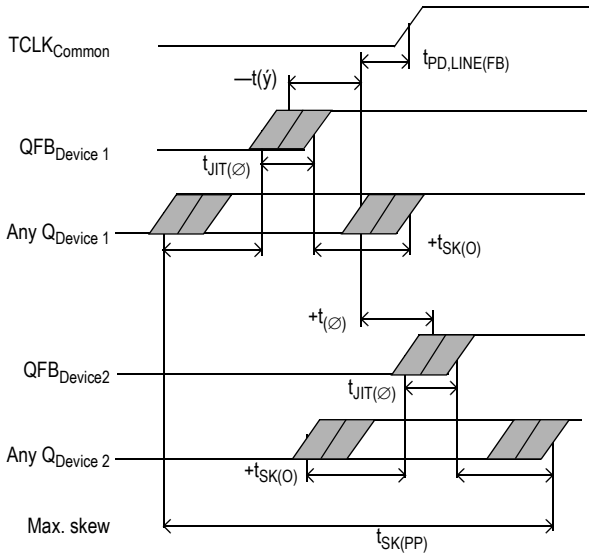


Figure 4. MPC9893 Max. Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 9.

Table 9. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from the common clock input to any MPC9893 output of –275 ps to +265 ps relative to the reference clock input CLK0/1:

$t_{SK(PP)}$ = *[–60ps...50ps] + [-125ps...125ps] + [(30ps · –3)...(30ps · 3)] +* $t_{PD,\ LINE(FB)}$

$t_{SK(PP)}$ = *[–275ps...265ps]* + $t_{PD,\ LINE(FB)}$

Example configuration: f_{ref}=100 MHz, V_{CC}=3.3V
f_{VCO}=400 MHz, FSEL[0:2]=111

The I/O (Phase) jitter of the MPC9893 depends on the internal VCO frequency and the PLL feedback divider configuration. A high internal VCO frequency and a low PLL feedback divider result in lower I/O jitter than the jitter limits in the AC characteristics (Table 8). When calculating the part-to-part skew, Table 10 should be used to determine the actual VCO frequency, then use Figure 5 to determine the maximum I/O jitter for the specific VCO frequency and divider configuration. In above example calculation, the internal VCO frequency of 400 MHz corresponds to a maximum I/O jitter of 30 ps (RMS).

Table 10. Internal VCO Frequency f_{VCO}

MPC9893 Configuration	f_{VCO}	PLL Feedback Divider FB
M1H, M12H, M2H, M22H	4 * f_{ref}	4
M3, M32	6 * f_{ref}	6
M1M, M12M, M2M, M22M, M4, M42	8 * f_{ref}	8
M1L, M12L, M8, M82	16 * f_{ref}	16

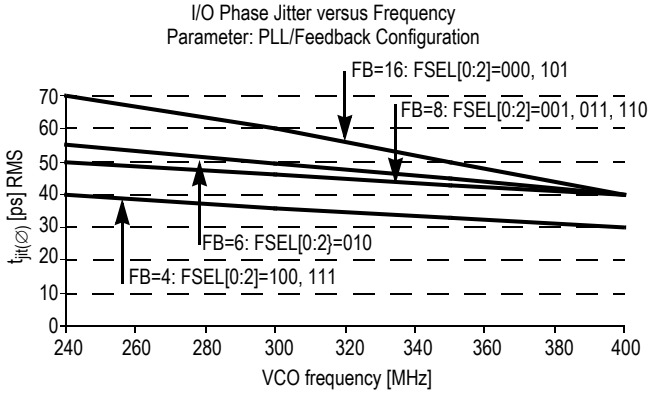


Figure 5. Max. I/O Phase Jitter versus VCO Frequency

The cycle-to-cycle jitter and period jitter of the MPC9893 depend on the output configuration and on the frequency of the internal VCO. Using the outputs of bank A and bank B at the same frequency (FSEL3=0) results in a lower jitter than the split output frequency configuration (FSEL3=1). The jitter also decreases with an increasing internal VCO frequency. Figure 5 to Figure 7 represent the maximum jitter of the MPC9893.

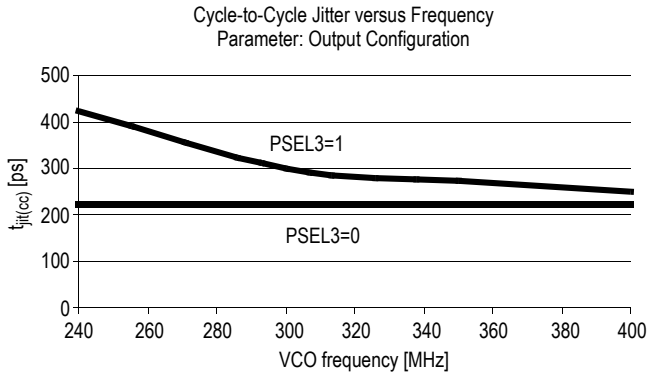


Figure 6. Max. Cycle-to-Cycle Jitter versus VCO Frequency

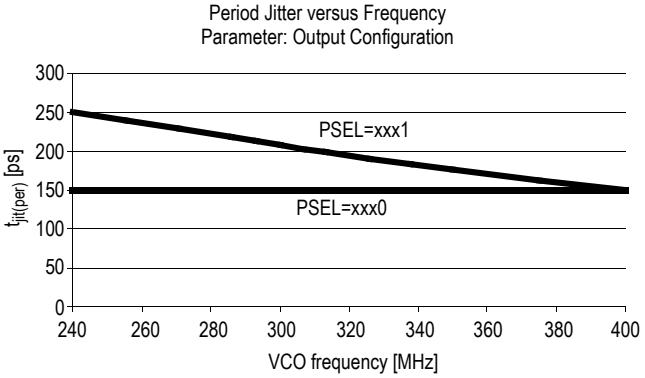


Figure 7. Max. Period Jitter versus VCO Frequency

Driving Transmission Lines

The MPC9893 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9893 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 8 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9893 clock driver is effectively doubled due to its capability to drive multiple lines.

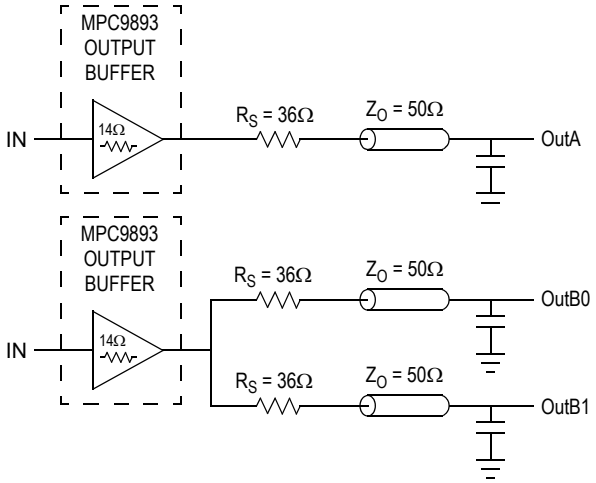


Figure 8. Single versus Dual Transmission Lines

The waveform plots in Figure 9 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9893 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9893. The output waveform in Figure 9 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$

$Z_0 = 50\Omega \parallel 50\Omega$

$R_S = 36\Omega \parallel 36\Omega$

$R_0 = 14\Omega$

$V_L = 3.0 (25 \div (18+17+25)$

$= 1.31V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

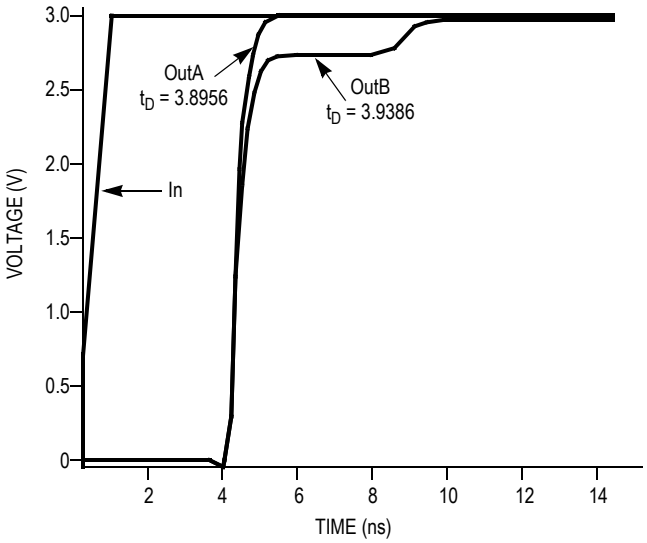
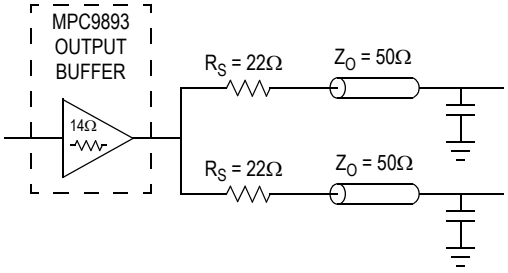


Figure 9. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 10 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$

$25\Omega = 25\Omega$

Figure 10. Optimized Dual Line Termination

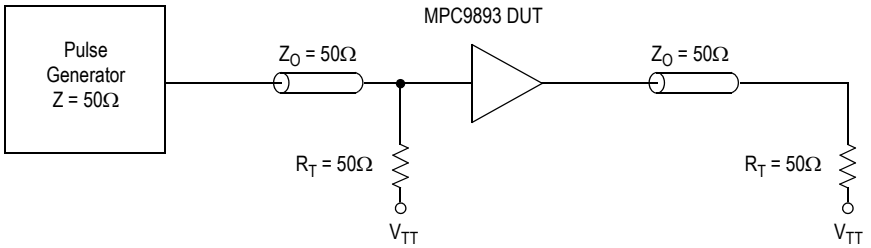
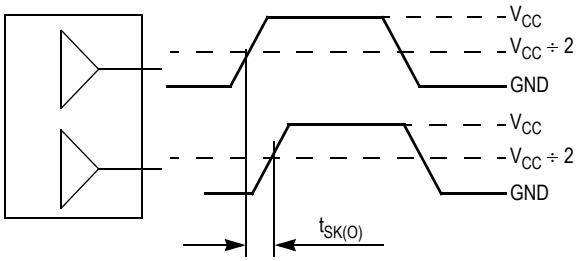


Figure 11. CLK0, CLK1 MPC9893 AC Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 12. Output-to-Output Skew $t_{SK(O)}$

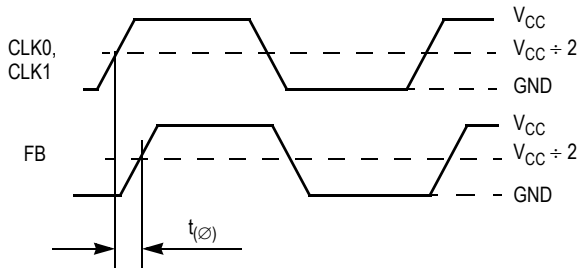
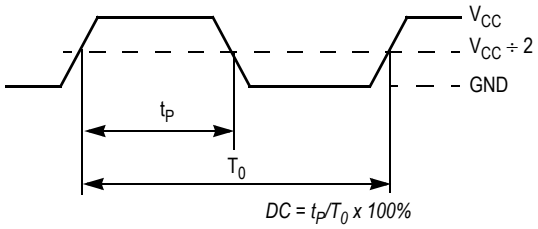
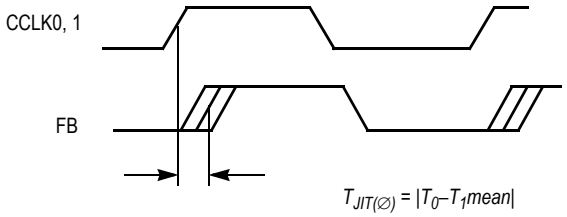


Figure 13. Propagation Delay ($t_{(\varnothing)}$, static phase offset) Test Reference



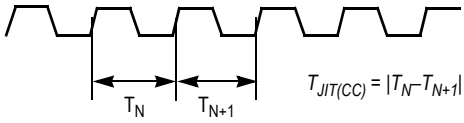
The time from the PLL controlled edge to the noncontrolled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 14. Output Duty Cycle (DC)



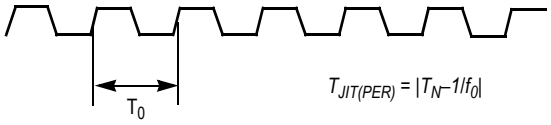
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 15. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 16. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 17. Period Jitter

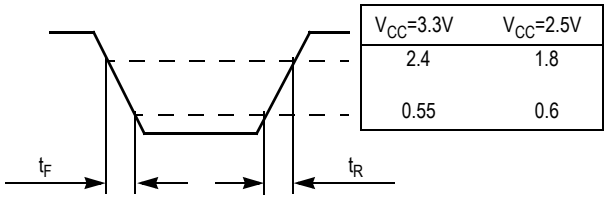


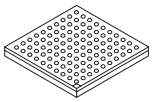
Figure 18. Output Transition Time Test Reference

Preliminary Information

Quad Input Redundant IDCS Clock Generator

MPC9894

QUAD INPUT REDUNDANT IDCS CLOCK GENERATOR



VF SUFFIX
100-LEAD MAPBGA PACKAGE
CASE 1462-01

The MPC9894 is a differential input and output, PLL-based Intelligent Dynamic Clock Switch (IDCS) and clock generator specifically designed for redundant clock distribution systems. The device receives up to four LVPECL clock signals and generates eight phase-aligned output clocks. The MPC9894 is able to detect failing clock signals and to dynamically switch to a redundant clock signal. The switch from the failing clock to the redundant clock occurs without interruption of the output clock signal (output clock slews to alignment). The phase bump typically caused by a clock failure is eliminated. The device offers eight low-skew clock outputs organized into four output banks, each configurable to support the different clock frequencies. The extended temperature range of the MPC9894 supports telecommunication and networking requirements.

Features

- 8 differential LVPECL output pairs
- Quad-redundancy reference clock inputs
- IDCS-on-chip intelligent dynamic clock switch
- Smooth output phase transition during clock failover switch/*
- Automatically detects clock failures
- Clock activity monitor
- Clock qualifier inputs
- Manual clock select and automatic switch modes
- 21.25 – 340 MHz output frequency range
- Specified frequency and phase slew rate on clock switch
- LVCMOS compatible control inputs and outputs
- External feedback enables zero-delay configurations
- Output enable/disable and static test mode (PLL bypass)
- Low-skew characteristics: maximum 50 ps[1] output-to-output
- I^2C interface for device configuration
- Low cycle-to-cycle and period jitter
- IEEE 1149.1 JTAG Interface
- 100-ball MAPBGA package
- Supports 2.5 V or 3.3 V supplies with 2.5 V and 3.3 V I/O
- Junction temperature range –40°C to +110°C

Functional Description

The MPC9894 is a quad differential redundant input clock generator. The device contains logic for clock failure detection and auto switching for clock redundant applications. The generator uses a fully integrated PLL to generate clock signals from any one of four redundant clock sources. The PLL multiplies the frequency of the input reference clock by one, two, four, eight or divides the reference clock by two or four. The frequency-multiplied clock signal drives four banks of two differential outputs. Each bank allows an individual frequency-divider configuration. All outputs are phase-aligned[2] to each other. Due to the external PLL feedback, the clock signals of all outputs are also phase-aligned[2] to the selected input reference clock, providing virtually zero-delay capability.

The integrated IDCS continuously monitors all four clock inputs and indicates a clock failure for each clock input. When a false clock signal is detected on the active clock, the MPC9894 switches to a redundant clock input, forcing the PLL to slowly slew to alignment and not produce any phase bumps at the outputs. The MPC9894 also provides a manual mode that allows for user-controlled clock switches.

The device is packaged in a 11x11 mm^2 100-ball MAPBGA package.

1. Final specification subject to change.
2. At coincident rising edges.

DEVICE DESCRIPTION

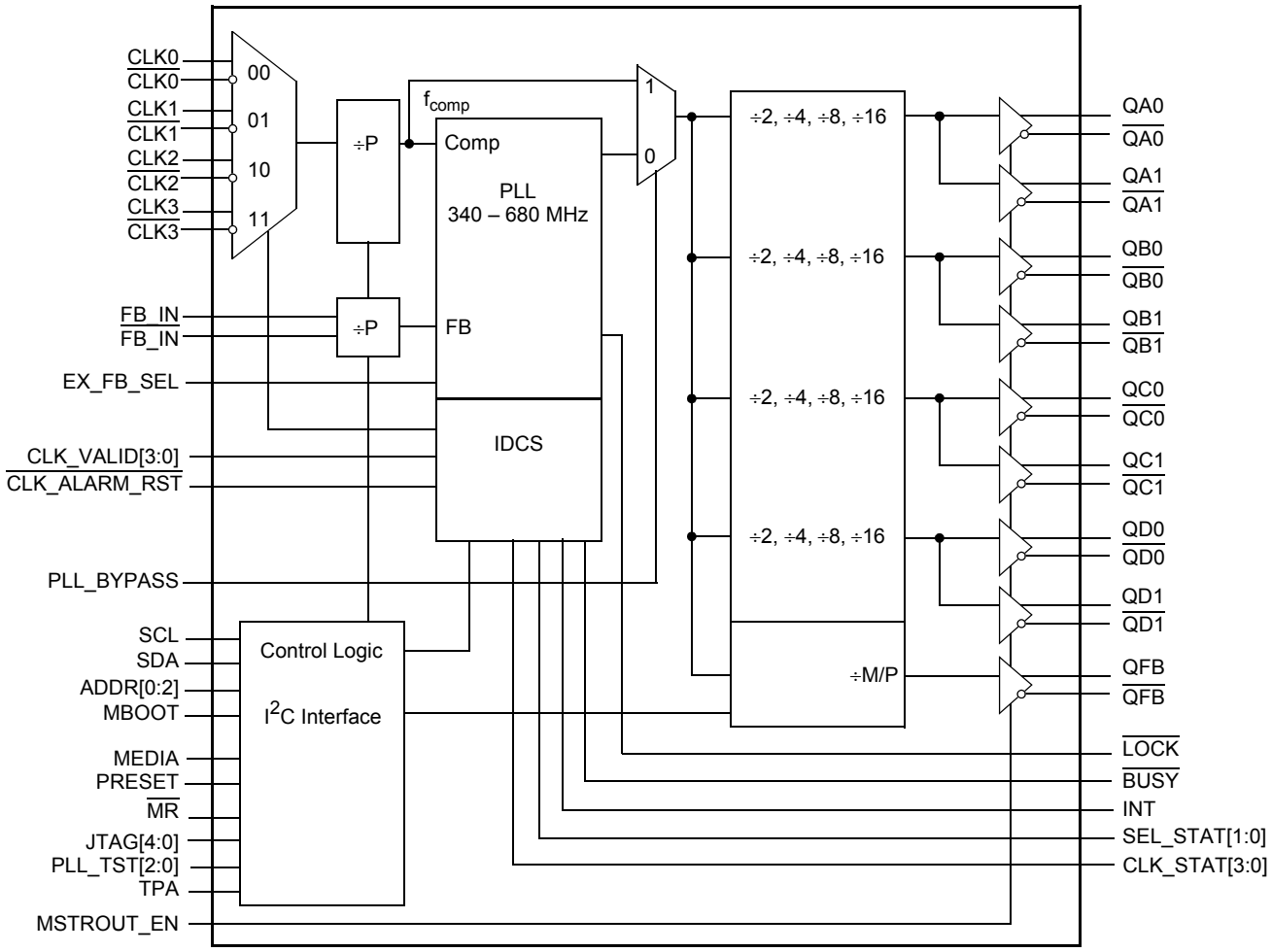


Figure 1MPC9894 Block Diagram

Table 1. Pin Configurations

Pin	I/O	Type	Function	Supply	Active State
Clock Inputs and Outputs					
CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$ CLK2, $\overline{\text{CLK2}}$ CLK3, $\overline{\text{CLK3}}$	Input	LVPECL	PLL reference clock inputs (differential) (internal pulldown)	V_{DDIC}	—
FB_IN, $\overline{\text{FB\_IN}}$	Input	LVPECL	PLL feedback signal input (differential). When configured for external feedback, the QFB output should be connected to FB_IN. (internal pulldown)	V_{DDIC}	—
QA[1:0], $\overline{\text{QA[1:0]}}$	Output	LVPECL	Bank A differential outputs	V_{DDAB}	—
QB[1:0], $\overline{\text{QB[1:0]}}$	Output	LVPECL	Bank B differential outputs	V_{DDAB}	—
QC[1:0], $\overline{\text{QC[1:0]}}$	Output	LVPECL	Bank C differential outputs	V_{DDCD}	—
QD[1:0], $\overline{\text{QD[1:0]}}$	Output	LVPECL	Bank D differential outputs	V_{DDCD}	—
QFB, $\overline{\text{QFB}}$	Output	LVPECL	Differential PLL feedback output. QFB must be connected to FB_IN for correct operation	V_{DDCD}	—

Table 1. Pin Configurations (Continued)

Pin	I/O	Type	Function	Supply	Active State
Control Inputs and Outputs					
EX_FB_SEL	Input	LVCMOS	Selects between external feedback and internal feedback	V_{DD}	high
CLK_VALID[3:0][1]	Input	LVCMOS	Validates the clock inputs CLK0 to CLK3 (internal pullup)	V_{DD}	high
$\overline{\text{CLK\_ALARM\_RST}}$	Input	LVCMOS	Reset of all four alarm status flags and clock selection status flag (internal pullup)	V_{DD}	low
PLL_BYPASS	Input	LVCMOS	Select static test mode (internal pulldown)	V_{DD}	high
MEDIA	Input	LVCMOS	Output impedance control	V_{DD}	high
$\overline{\text{MR}}$	Input	LVCMOS	Device reset (internal pullup)	V_{DD}	low
$\overline{\text{LOCK}}$	Output	LVCMOS	PLL lock indicator	V_{DD}	low
CLK_STAT[3:0]	Output	LVCMOS	Clock input status indicator	V_{DD}	high
SEL_STAT[1:0]	Output	LVCMOS	Reference clock selection indicator	V_{DD}	high
$\overline{\text{BUSY}}$	Output	LVCMOS	IDCS switching activity indicator	V_{DD}	low
MBOOT	Input	LVCMOS	Activates I^2C boot sequence (internal pulldown)	V_{DD}	high
PRESET	Input	LVCMOS	Enables Preset configuration of configuration registers on release of $\overline{\text{MR}}$ (internal pulldown)	V_{DD}	high
$\overline{\text{INT}}$	Output	OD	Indicate any status IDCS change	V_{DD}	low
MSTROUT_EN	Input	LVCMOS	Master Enable for all Outputs (internal pulldown)	V_{DD}	high
SEL_2P5V	Input	LVCMOS	Device core power supply selection for VDD and VDDA	V_{DD}	high
I^2C Interface					
SCL	I/O	OD	I^2C interface control, clock	V_{DD}	—
SDA	I/O	OD	I^2C interface control, data	V_{DD}	—
ADDR[2:0]	Input	LVCMOS	I^2C interface address lines (10K pullup)	V_{DD}	high
IEEE 1149.1 and Test					
TMS	Input	LVCMOS	JTAG test mode select(10K pullup)	V_{DDIC}	—
TDI	Input	LVCMOS	JTAG test data input(10K pullup)	V_{DDIC}	—
TDO	Output	LVCMOS	JTAG test data output	V_{DDIC}	—
TCK	Input	LVCMOS	JTAG test clock	V_{DDIC}	—
$\overline{\text{TRST}}$	Input	LVCMOS	JTAG test reset(10K pullup)	V_{DDIC}	—
PLL_TEST[2:0]	Input	LVCMOS	PLL_TEST pins (factory use only, MUST BE CONNECTED TO GND)	N/A	—
TPA	Output	LVCMOS	PLL Analog test pin (factory use only, MUST BE CONNECT TO GND)	V_{DDA}	—
Power and Ground					
GND	Supply	Ground	Negative power supply	—	—
V_{DD}	Supply	—	Positive power supply for the device core, output status and control inputs. (3.3 V or 2.5 V)	—	—
V_{DDAB}	Supply	—	Supply voltage for output banks A and B (QA0 through QB1) (3.3 V or 2.5 V)	—	—
V_{DDCD}	Supply	—	Supply voltage for output banks C and D (QC0 through QD1) and QFB (3.3 V or 2.5 V)	—	—
V_{DDIC}	Supply	—	Supply voltage for differential inputs clock inputs CLK0 to CLK3 and FB_IN (3.3 V or 2.5 V)	—	—
V_{DDA}	Supply	—	Clean supply for analog portions of the PLL (This voltage is derived via a RC filter from the V_{DD} supply)	—	—

1. bit order = msb to lsb.

Table 2. Function Table

Control	Default	0	1
Control Inputs			
PLL_BYPASS	0	PLL enabled. The input to output frequency relationship is according to Table 9 if the PLL is frequency locked.	PLL bypassed and IDCS disabled. The VCO output is replaced by the reference clock signal f_{REF}. This is considered to be a test mode and clock monitoring and clock switching are disabled during this operation.
CLK_VALID[3:0]	0	The associated clock input is considered to be invalid and usable	The associated clock input is considered to be a valid usable clock input
$\overline{\text{CLK\_ALARM\_RST}}$	1	CLK_STAT[3:0] and SEL_STAT[1:0] flags are reset: CLK_STAT[3:0] = 0000 and SEL_STAT[1:0] = 00. $\overline{\text{CLK\_ALARM\_RST}}$ is a one-shot function.	CLK_STAT[3:0] and SEL_STAT[1:0] flags are active
$\overline{\text{MR}}$	1	Reset of data generators and output dividers. The MPC9894 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles	Outputs enabled (active)
MBOOT	0	I^2C read/write mode	I^2C boot mode
PRESET	0	Normal Operation	Uses Configuration Register PRESET values on $\overline{\text{MR}}$
EX_FB_SEL	0	Selects internal feedback path	Selects external feedback path
MEDIA	0	Low output impedance (QA0 to QD1 and QFB)	50 Ω output impedance (QA0 to QD1 and QFB)
SEL_2P5V	0	Selects 3.3 V for core V_{DD}	Selects 2.5 V for core V_{DD}
MSTROUT_EN		All outputs disabled (synchronous with clock being low)	All outputs enabled
Control Outputs			
$\overline{\text{LOCK}}$[1]		PLL is locked	PLL is unlocked
$\overline{\text{BUSY}}$[1]		The IDCS has initiated a clock switch.	No clock switch currently performed
$\overline{\text{INT}}$		IDCS status has changed (indicates an assertion of CLK_STAT[3:0] or deassertion of $\overline{\text{LOCK}}$)	No status change
CLK_STAT[3:0]		Associated clock input not valid	Associated clock input valid
SEL_STAT[1:0]		Encoded value refer to Table 7	Encoded value refer to Table 7

1. The combined pins of $\overline{\text{LOCK}}$ = 1 and $\overline{\text{BUSY}}$ = 0 are used to indicate a catastrophic failure. Refer to PLL Out-of-Lock Conditions.

OPERATING INFORMATION

Basic Functional Description

The MPC9894 is a quad-redundancy IDCS clock generator. The redundancy feature allows automatic switching from the reference clock source to a secondary clock source on detection of a failed reference clock. The MPC9894 will detect and report a missing clock on any of its four inputs. Based upon the current IDCS mode setting and the qualifier input pins, the MPC9894 will switch to the next qualified secondary clock.

The input clock sources, CLK0, CLK1, CLK2, and CLK3, are assumed to be the same frequency(1) but non-phase-related sources. When a clock switch occurs, the phase alignment to the new clock source will occur over an extended time period, eliminating runt clock output pulses. The maximum rate of phase change is specified in the AC parameter Delta Period per Cycle($^{\Delta}_{PER/CYC}$). The device uses a fully integrated PLL to generate clock signals from redundant clock sources. The PLL multiplies the input reference clock signal by a variety of values, including 0.25, 0.5, 1, 2, 4 or 8. For a complete list refer to Table 9. The frequency multiplied clock signal drives four independent output banks. Each output bank is phase-aligned to the input reference clock phase, providing virtually zero-delay capability(2).

The configuration of the MPC9894 series of clock generators is performed through either the I^2C interface or by the preset configuration mode. The I^2C interface uses a 2 pin interface to transmit clock and data to and from a series of configuration and status registers in the MPC9894.

Definitions

IDCS:

Intelligent Dynamic Clock Switch. The IDCS monitors the clock inputs CLK0, CLK1, CLK2, and CLK3. Upon a failure of the reference clock signal, the IDCS switches to a qualified secondary clock signal and the status flags are set.

Reference clock signal:

The input clock signal that is selected by the IDCS or IDCS_MODE[2:0] as the input reference to the PLL.

Primary clock:

The input clock signal selected by IDCS_MODE[2:0]. The primary clock may or may not be the reference clock, depending on IDCS mode and IDCS status.

Secondary clock:

The input clock signal which will be selected by the IDCS upon an automatic clock switch.

Tertiary, Quaternary clocks:

The input clock signals that will be selected by the IDCS, in turn, after the current secondary clock. This clock selection is based upon a round robin rotational sequence

Manual IDCS mode:

The reference clock input is selected by IDCS_MODE[0xx].

Automatic IDCS mode:

The reference clock signal is determined by the IDCS.

Selected clock:

The SEL_STAT[1:0] flags indicate the reference clock signal.

Qualified clock:

The corresponding CLK_VALID[3:0] signal is logic high, the associated CLK_STAT status bit is logic high and no clock failure is present.

Bit Ordering:

The bit ordering convention used in this document for both pin and register documentation is NAME[7:0] where bit 7 is the most significant bit and 0 is the least significant bit.

1. Refer to Table 39 for clock frequency specification
2. Using external feedback

DEVICE CONFIGURATION

I²C Configuration and I²C Addressing

The MPC9894 is configured via a series of 8-bit registers. The bits in these registers allow a wide range of control over the operation of the MPC9894 clock generator. These registers are accessed via an I²C interface through which a 7-bit address is sent from the I²C master to select the specific I²C slave device being accessed. The address for this clock driver is found in the first of the MPC9894 I2C registers. The format of this address has a fixed most-significant four bits of binary 1101 while the least-significant 3 address bits are read from the 3 ADDR pins. This provides the capability to configure up to 8 clock devices on a single I²C interface.

In addition, activation of the MBOOT pin on power-up or reset initiates an automatic boot sequence allowing the clock generators to be initialized from an I²C compatible EEPROM. In this case the MPC9894 becomes an I²C master and the configuration bits are filled by the information from the first 6 bytes of the EEPROM. This allows the clock to be configured without a controlling I²C bus master if desired. The PRESET pin allows the device to be configured without a I²C bus master.

The detailed register descriptions are found in the section, I²C Interface and configuration/status register.

IDCS MODE Configuration

Three register bits are used to configure the MPC9894 in either an automatic clock switch mode or into a manual clock select mode. The three mode select bits are defined in Table 3

IDCS modes 000 through 011 allow manual selection between the four clock sources. IDCS modes 100 through 111 enable the automatic mode of the IDCS.

Table 3. MPC9894 IDCS Configuration

IDCS_MODE [2:0]	Description	Primary Clock	Secondary Clock[1]	Tertiary Clock	Quaternary Clock
000	Manual	CLK0	n/a	n/a	n/a
001		CLK1	n/a	n/a	n/a
010		CLK2	n/a	n/a	n/a
011		CLK3	n/a	n/a	n/a
100	Automatic	CLK0	CLK1	CLK2	CLK3
101		CLK1	CLK2	CLK3	CLK0
110		CLK2	CLK3	CLK0	CLK1
111		CLK3	CLK0	CLK1	CLK2

1. For CLK_VALID[3:0] = 1111 and input clock validity

Automatic IDCS Mode

In the automatic mode, the clock failure detection is enabled and the IDCS overwrites the selected clock on a clock failure. The IDCS operation requires PLL_BYPASS = 0 and IDCS_MODE[2] = 1. The reference clock is handled in a round robin method based upon clock validity and the qualification input CLK_VALID[3:0]: The qualification input is obtained from the four input pins, CLK_VALID[3:0]. If any of the CLK_VALID pins are low the associated clock input will be considered “unqualified” and thus not selected as a reference clock. Alternatively, if a clock input does not have a valid clock signal, it will not be selected and the next qualified and valid clock is selected as the reference clock.

For example, if IDCS_MODE[2:0] = 100 (the IDCS is in automatic mode), CLK_VALID[3:0] = 1111 and CLK0, CLK1, CLK2, and CLK3 have valid input clock signals then CLK0 is the primary clock and CLK1 is the secondary clock. The IDCS selects the primary clock as the reference clock and the PLL will phase-lock the clock outputs to the CLK0 input. Upon the failure of CLK0 the IDCS will select CLK1 as the reference clock and initiate a switch, making CLK1 the reference clock and CLK2 the secondary clock. If CLK1 fails, the IDCS will switch to CLK2, etc.

A de-asserted CLK_VALID[] pin disables the associated clock input as secondary clock. The associated clock input cannot be selected by the IDCS as secondary clock signal. For instance, if CLK0 is the primary clock and CLK_VALID[3:0] = 1101, the IDCS will select CLK2 upon a clock failure of CLK0 (CLK1 is disabled by the CLK_VALID1 input, allowing external logic to control the IDCS switch logic). If a clock is the reference clock signal and its associated CLK_VALID signal is switched from ‘valid' to ‘invalid', the IDCS initiates a clock input switch, selecting the next available clock input (secondary clock).

An invalid clock(1) signal triggers the associated clock status output (CLK_STAT[3:0]), independent of the primary and reference clock. These pins go set on a clock failure and remain set (sticky) until the CLK_ALARM_RST pin or the individual alarm reset bits (ALARM_RST[3:0]) are asserted. The CLK_STAT[3:0] outputs are mirrored in the device register 4 for I²C bus access.

After each successful IDCS-commanded switch, the primary clock as set by IDCS_MODE[1xx] is no longer the reference clock. The user may reset the IDCS flags by asserting the individual ALARM_RST[3:0] bits after each IDCS-commanded switch. Activation of ALARM_RST[3:0] does not change the reference clock. A user-commanded change of the primary clock in automatic mode requires a write command to the IDCS_MODE[2:0] = 0xx bits (the primary clock and SEL_STAT[1:0] can be freely changed by setting IDCS_MODE[2:0] = 1xx). If the reference clock is not the primary clock, a write command to IDCS_MODE[2:0] = 1xx will cause the PLL to lock on the primary clock, given the new primary clock is a qualified clock.

1. See Clock Failure Detection.

Table 4. Input Clock Qualifier and Status Flag

Input Clock	Associated Input Qualifier[1]	Associated Input Clock Status Flag	
		Pin	Register location
CLK0	CLK_VALID0	CLK_STAT0	Device register 5, bit 3
CLK1	CLK_VALID1	CLK_STAT1	Device register 5, bit 4
CLK2	CLK_VALID2	CLK_STAT2	Device register 5, bit 5
CLK3	CLK_VALID3	CLK_STAT3	Device register 5, bit 6

1. The input qualifier logic can be enabled or disabled by setting the QUAL_EN bit in register 3.

Table 5. Input Clock Status CLK_STAT[3:0]

CLK_STAT[]	Description
0	Clock input failure
1	Clock input signal valid

Table 6. Clock Input Qualifier CLK_VALID[3:0]

CLK_VALID[]	Associated Input Clock
0	Not qualified and will not be selected
1	Qualified

The SEL_STAT[1:0] pins indicate which of the four input clocks is the current reference clock. In the automatic mode and In the case of the reference clock failure, the SEL_STAT flag will indicate a reference clock different from the original primary clock selected by IDCS_MODE[2:0]. The CLK_STAT outputs are mirrored in register 5, bits 1:0 for I^2C bus access.

Table 7. SEL_STAT[1:0]

SEL_STAT[1:0]	Selected clock input
00	CLK0
01	CLK1
10	CLK2
11	CLK3

If all four clock inputs are not qualified the VCO will slew to its lowest frequency. This condition will be indicated by the $\overline{\text{LOCK}}$ pin being de-asserted. The MPC9894 will remain in this state until an input clock is restored and the device is reset via the $\overline{\text{MR}}$ pin.

Clock Failure Detection

The MPC9894 clock failure detection is performed using an input clock amplitude check combined with an activity detector. The following conditions will trigger a failed clock status (CLK_STATn = 0) on any qualified clock (CLK_VALIDn = 1). These conditions are:

1. Either or both CLKx, $\overline{\text{CLKx}}$ are disconnected from the input clock source and open.
2. CLKx and $\overline{\text{CLKx}}$ are shorted together
3. Either or both CLKx or $\overline{\text{CLKx}}$ are shorted to GND
4. Both CLKx and $\overline{\text{CLKx}}$ are shorted to a power supply
5. Amplitude of CLKx or $\overline{\text{CLKx}}$ is less than $V_{PP, OK}$ (refer to AC specification, Table 39)

In addition, the currently selected clock is checked by a phase-frequency detector after the input divider (P). This is triggered by a phase step of $mae_{(\varnothing)}$. This phase detector will issue a failed clock status (CLK_STATn = 0) within 'P' clock cycles.

The IDCS does not detect changes of the reference frequency or the reference frequency being out of the specified input frequency range. This includes errors such as reference frequency drift due to crystal aging etc.

Clearing of IDCS Alarm Flags

The input clock status flags are set by a clock failure and remain set until manually cleared (sticky). Clearing can be done by either of two methods. All status flags can be cleared by the package pin, $\overline{\text{CLK\_ALARM\_RST}}$. Or individual status flags can be cleared via register bits, ALARM_RST[3:0]. The $\overline{\text{CLK\_ALARM\_RST}}$ pin is activated by a negative edge on the pin. This clears all CLK_STAT[3:0] flags and returns the IDCS to the primary clock source. The SEL_STAT[1:0]-selected clock indicator now reflects the IDCS_MODE[2:0] setting.

By using ALARM_RST[3:0] (register 2) individual CLK_STAT[3:0] bits are cleared by writing a logic 0 to the individual bit in this register. It is important to note that this action does not return the IDCS to the primary clock.

IDCS Manual Mode

The manual request IDCS mode is selected by IDCS_MODE[2:0] = 0xx. The PLL functions normally and all four inputs clocks are monitored. The reference clock will always be the clock signal selected by IDCS_MODE[1:0] and will be indicated by SEL_STAT[1:0]. A manual-requested clock switch (by changing the IDCS_MODE[0xx] signal) will only be executed if the new clock is valid. The SEL_STAT[1:0] pins/bits should be checked after the manual request to ensure the clock switch occurred.

Interrupt Operation

The MPC9894 pin, $\overline{\text{INT}}$, may be used to interrupt a microprocessor or microcontroller. This open drain output pin goes active or low on any of the following occurrences

1. A clock failure as indicated by any of bits 6 thru 3 being set in the status register
2. A out-of-lock condition for the PLL as indicated by either the $\overline{\text{LOCK}}$ pin or bit 2 of the status register.

The interrupted processor would then use the I^2C interface to read the status register (bit 7) to determine if this MPC9894 generated the interrupt. If the interrupt was caused by this MC9894, the status register would then be analyzed to determine the reason for the interrupt and then the appropriate action taken.

In order for interrupts to occur, the INT_E bit must be set in the Device Configuration and Output Clock Enable Register. Once the interrupt flag has been set, reading of the Status Register clears the INT flag.

Clock Operation on Power-Up

On or after power-up, the MPC9894 must be reset via the $\overline{\text{MR}}$ pin. The MPC9894 may be powered-up in either of three configurations. These configurations are selected by the PRESET pin and MBOOT pin.

If PRESET is low, on release of the $\overline{\text{MR}}$ pin, the MPC9894 powers up in a benign mode with all clock outputs disabled. The device is ready to be and must be programmed via the I^2C interface prior to operation.

If the PRESET pin is high on the release of the $\overline{\text{MR}}$ pin, the MPC9894 powers up in a run state. In this case the IDCS is configured for automatic mode, CLK0 to be the primary clock, a divide by 2 on clock bank A and B outputs, a divide by 8 on clock C and D outputs, all clock output banks enabled and interrupts enabled. If using the preset mode, then at least one of the clock inputs must have the correct input frequency prior to $\overline{\text{MR}}$ going high.

Later in this document, tables defining the I^2C interface registers describe both configurations. The default (reset) information is for the normal reset operation, while the default (preset) information describes the values for each configuration bit on activation of the PRESET pin. In order to return the MPC9894 to either the preset or reset configuration the $\overline{\text{MR}}$ pin must be activated.

Refer to the <st-blue>Boot Mode for a description of the MBOOT pin.

PLL Feedback

The MPC9894 may be operated with either an internal or an external PLL feedback path. The selection of internal vs. external feedback is made with the pin, EX_FB_SEL. If external feedback is desired, the EX_FB_SEL pin should be connected to V_{DD} and a connection from QFB/$\overline{\text{QFB}}$ to FB_IN/$\overline{\text{FB\_IN}}$ must be made. External feedback provides a known relationship between the clock input and the feedback input for phase synchronization of output clock signals to the clock input. If this phase synchronization is not required, the MPC9894 may be configured for internal feedback by the connection of EX_FB_SEL to ground. In this configuration, the connection from the feedback output to the feedback input is not required. The feedback output may be used as a separate output to produce a reference clock output.

PLL Out-of-Lock Conditions

The $\overline{\text{LOCK}}$ pin and associated status bit indicates the lock state of the PLL. After power-up and prior to writing configuration data to the control registers, an out-of-lock condition will be indicated by $\overline{\text{LOCK}}$ = 1. If a valid clock is available and proper configuration data is written to the control registers, $\overline{\text{LOCK}}$ will then indicate the PLL is in a locked condition with $\overline{\text{LOCK}}$ = 0.

The combination of $\overline{\text{LOCK}}$ = 1 and $\overline{\text{BUSY}}$ = 0 is used to indicate a catastrophic failure of the PLL. This condition will occur on the following:

1. All input clocks have failed or no clock is present.
2. External feedback has been selected with the EX_FB_SEL pin and an external feedback signal is not present on the FB_IN/$\overline{\text{FB\_IN}}$ inputs. It should be noted that if this condition occurs during the initial PLL lock acquisition the PLL will produce a clock that is locked to the internal feedback path. However, the catastrophic failure status of $\overline{\text{LOCK}}$ = 1 and $\overline{\text{BUSY}}$ = 0 will occur.

Recovery from the catastrophic failure condition requires repairing the cause of the failure, followed by a master reset to be issued to the MPC9894.

CLOCK OUTPUT TRANSITION

An MPC9894 clock switch, either in IDCS manual or IDCS automatic mode, follows the next positive edge of the newly selected reference clock signal. The positive edge of the feedback clock and the newly selected reference clock edge will start to slew to alignment by adjusting the feedback edge placement a small amount of time in each clock cycle. Figure 2. Clock Switch shows a failed primary input clock with the MPC9894 switching to and aligning to the secondary clock. This small amount of additional time in each clock cycle will ensure that the output clock does not have any large phase changes or frequency changes in a short period of time. The alignment will be to either 1) the closest edge, either forward or backward or 2) toward the lagging clock edge. The maximum rate of period change is specified in the AC parameter tables with the parameter of $^{\Delta}_{PER/CYC}$. This parameter implies that the output clock edge will never change more than the specified amount in any one cycle.

The busy signal is used to indicate that the MPC9894 is in the process of slewing to the new input clock alignment. The signal is accessed thru the $\overline{BUSY}$ pin and goes set upon a clock switch. The pin is reset once the phase realignment is completed. During the period that $\overline{BUSY}$ is active, the configuration register of the MPC9894 should not be written with new configuration data.

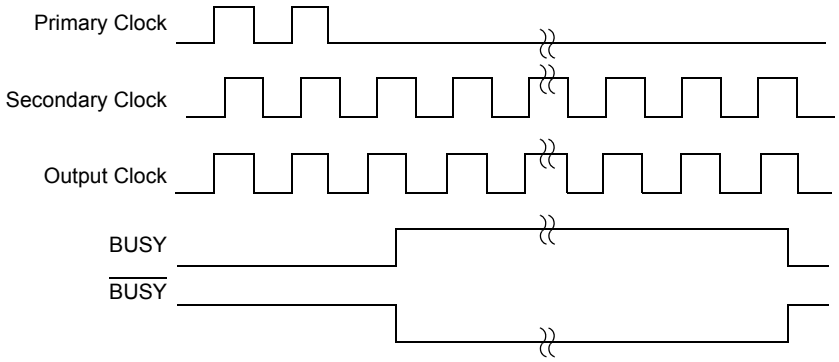


Figure 2. Clock Switch

For example, if the current input clock of 62.5 MHz and the secondary clock are 180 degrees out of phase then the minimum clock transition time can be calculated by

$$t_{cycle} = 1 \div f_{cycle} = 1 \div 62.5\ MHz = 16\ ns$$

Therefore 180 degree clock difference is

$$t_{cycle} \div 2 = 8\ ns$$

Assuming a $^{\Delta}_{PER/CYC}$ of 40 ps, then

$$8ns \div 40\ ps/cycle = 200\ cycles.$$

This is the minimum number of cycles that will be required for the alignment to the new clock. The alignment to the new clock phase may occur slower than this but never faster.

The alignment on clock failure is selectable between either 1) the closest edge, either forward or backward or 2) toward the lagging clock edge. The selection of the alignment method is selected in the Slew_Control bit (bit 5) of the Device Configuration and Output Enable Register. This selection allows the user to select the alignment method that best suits the application. The characteristics and subsequent advantages and disadvantages of each method are described as follows.

1. Slew to closest edge
   a. The alignment is either forward toward the lagging edge or backward toward the leading edge.
   b. The alignment to the closest edge ensures re-alignment to the new clock input in the minimum time.
   c. In applications where the input clocks are closely aligned, there is no ambiguity on the direction of clock slew.
   d. The clock output frequency will either increase or decrease based on direction of clock slew.
2. Slew to lagging edge
   a. The output frequency always decreases. Thus the clock frequency never violates a maximum frequency specification in the user system.
   b. When input clocks are closely aligned (within SPO + jitter) the MPC9894 may align to the closest edge or to the lagging edge. In the case of multiple MPC9894s with equivalent clock inputs one MPC9894 may align in one direction while an other MPC9894 may align to the opposite direction.

If default values for the Slew_Control is not the configuration desired then the reconfiguration of the slew method should be perform soon after power-up and the configuration should remain fixed from that point.

INPUT AND OUTPUT FREQUENCY CONFIGURATION

Configuring the MPC9894 input and output frequencies requires programming the internal PLL input, feedback and output dividers. The output frequency is represented by the following formula:

$$f_{OUT} = [(f_{REF} \div P) \cdot M] \div N$$

where f_{REF} is the reference frequency of the selected input clock source (reference input), M is the PLL feedback divider and N is an output divider. The PLL input divider P, the feedback divider M and the output divider are configured by the device registers 1 and 4. The MPC9894 has four output banks (Bank A, B, C, and D) and each output bank can be configured individually as shown in Table 8.

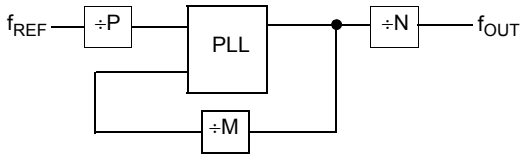


Figure 3. PLL Frequency Calculation

Table 8. Configuration of PLL P, M and N Frequency Dividers

Divider	Available Values	Configuration Through
PLL Input Divider (P)	÷1, ÷2, ÷3, ÷4, ÷5, ÷6	Input_FB_Div[3:0], Register 4, bit 3:0
PLL Feedback Divider (M)	÷8, ÷12, ÷16	
PLL Output Divider, Bank A (N_A)	÷2, ÷4, ÷8, ÷16	FSEL_B[1:0], Register 1, bit 7:6
PLL Output Divider, Bank B (N_B)	÷2, ÷4, ÷8, ÷16	FSEL_B[1:0], Register 1, bit 5:4
PLL Output Divider, Bank C (N_C)	÷2, ÷4, ÷8, ÷16	FSEL_C[1:0], Register 1, bit 3:2
PLL Output Divider, Bank D (N_D)	÷2, ÷4, ÷8, ÷16	FSEL_D[1:0], Register 1, bit 1:0

The reference frequency f_{REF} and the selection of the PLL input divider (P) and feedback-divider (M) is limited by the specified VCO frequency range. f_{REF}, P and M must be configured to match the VCO frequency range of 340 to 680 MHz in order to achieve stable PLL operation:

$$f_{VCO,MIN} \le (f_{REF} \div P \cdot M) \le f_{VCO,MAX}$$

The PLL input divider (P) can be used to situate the VCO in the specified frequency range. The PLL input divider effectively extends the usable input frequency range.

The output frequency for each bank can be derived from the VCO frequency and output divider (N):

$$f_{QA}[1:0] = f_{VCO} \div N_A$$
$$f_{QB}[1:0] = f_{VCO} \div N_B$$
$$f_{QC}[1:0] = f_{VCO} \div N_C$$
$$f_{QD}[1:0] = f_{VCO} \div N_D$$

Table 9 illustrates the possible input clock frequency configurations of the MPC9894. Note that the VCO lock range is always 340 MHz to 680 MHz, setting lower and upper boundaries for the frequency range of the device.

Table 9. Input and Output Frequency Ranges

Input_FB_Div[3:0]	P	M	f_{REF} range MHz	Output frequency for any bank A, B, C or D (FSEL_x) and ratio to f_{REF}			
				N = 2	N = 4	N = 8	N = 16
0	÷1	÷16	21.25 – 42.5	8·f_{REF}	4·f_{REF}	2·f_{REF}	f_{REF}
1	÷1	÷12	28.33 – 56.67	6·f_{REF}	3·f_{REF}	1.5·f_{REF}	0.75·f_{REF}
2	÷2	÷12	56.66 – 113.34	3·f_{REF}	1.5·f_{REF}	0.75·f_{REF}	0.375·f_{REF}
3	÷1	÷8	42.5 – 85.0	4·f_{REF}	2·f_{REF}	1·f_{REF}	0.5·f_{REF}
4	÷2	÷16	42.5 – 85.0	4·f_{REF}	2·f_{REF}	1·f_{REF}	0.5·f_{REF}
5	reserved						
6	÷2	÷8	85.0 – 170.0	2·f_{REF}	1·f_{REF}	0.5·f_{REF}	0.125·f_{REF}
7	÷3	÷12	85.0 – 170.0	2·f_{REF}	1·f_{REF}	0.5·f_{REF}	0.125·f_{REF}
8	÷4	÷16	85.0 – 170.0	2·f_{REF}	1·f_{REF}	0.5·f_{REF}	0.125·f_{REF}
9	reserved						
10	÷4	÷12	113.32 – 226.64	1.5·f_{REF}	0.75·f_{REF}	0.375·f_{REF}	0.1875·f_{REF}
11	reserved						
12	reserved						
13	reserved						
14	4	÷8	170.0 – 340.0	1·f_{REF}	0.5·f_{REF}	0.25·f_{REF}	0.125·f_{REF}
15	6	÷12	170.0 – 340.0	1·f_{REF}	0.5·f_{REF}	0.25·f_{REF}	0.125·f_{REF}

I²C INTERFACE AND CONFIGURATION/STATUS REGISTERS

The following tables summarize the bit configurations for the registers accessible via the I²C interface. The register values are read or written over the I²C interface by the I²C Master. This sequence starts with the I²C start command, followed by the I²C device address and read/write byte. This is then followed by the address of the register that is to be accessed. In the case of a write, the register address byte is followed by the data to be written to that register. In the case of a read, the device will then respond with the data from that register. At the conclusion of the transfer an I²C Stop command is issued by the Master to terminate the transfer. For a complete description of the I²C protocol refer to the v2.1 I²C specification.

Table 10 lists the registers that are accessible via the I²C interface.

Table 10. I²C Registers

Address	Register
0x00	Table 11. Slave Address (Register 0 — Read Only)
0x01	Table 12. Output Configuration Register (Register 1 — Read/Write)
0x02	Table 14. Mode Configuration and Alarm Reset Register (Register 2 — Read/Write)
0x03	Table 17. Device Configuration and Output Clock Enable Register (Register 3 — Read/Write)
0x04	Table 22. Input and Feedback Divider Configuration Register (Register 4 — Read/Write)
0x05	Table 24. Status Register (Register 5 — Read Only)
0x06	Table 25. Output Power-Up Register (Register 6 — Read/Write)
0x07	Table 27. Feedback Power-Up Register (Register 7 — Read/Write)

Boot Mode

When the I²C boot mode is activated on power-up or reset via the MBOOT pin, the entire set of writable configuration registers are written with a 6-byte sequence. This sequence starts with the Output Configuration Register, and is followed by the Mode Configuration and Alarm Reset Register, the Device Configuration and Output Clock Enable Register, the Input and Feedback Divider Configuration Register, the Output Power-Up Register and the Feedback Power-Up Register. This equates to the register sequence of 1, 2, 3, 4, 6, 7. This sequence starts with the start command, the device select and read/write(write) byte, followed by the beginning byte address for reading from the EEPROM. This is then followed by the start command, device select and read/write (read) and four current address read bytes. The device address is the binary 7-bit value of 1010000. This I²C sequence is compatible with industry standard I²C bus EEPROMs such as STMicroelectronics M24C01, or equivalent.

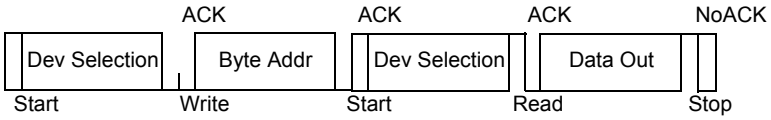


Figure 4. Boot Mode Random Access Read

Slave Address Register

The Slave Address register contains the I²C address that is used to determine if the data on the I²C interface is addressed to this device. The seven-bit address is determined with the fixed value of binary 1101 followed by variable bits that are obtained from the three address pins. The three input pins allow for 8 different addresses for a given clock generator, allowing up to 8 clock generators to be addressed on a single I²C interface.

Table 11. Slave Address (Register 0 — Read Only)

Bit	7	6	5	4	3	2	1	0
Description	not used	ADDR_6	ADD_R5	ADDR_4	ADDR_3	ADDR_2 read from ADDR[2] pin	ADDR_1 read from ADR[1] pin	ADDR_0 read from ADDR[0] pin
Reset default		1	1	0	1			
Preset default		1	1	0	1			

Output Configuration Register

The output configuration register is divided into four, 2 bit-groups with each group selecting the divide ratio for output banks A through bank D, refer to Table 12. For each bank, four output divider settings (÷2, ÷4, ÷8, ÷16) are available, refer to Table 12.

Table 12. Output Configuration Register (Register 1 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	FSEL_A[1:0]		FSEL_B[1:0]		FSEL_C[1:0]		FSEL_D[1:0]	
Reset default	0	0	0	0	0	0	0	0
Preset default	0	0	0	0	1	0	1	0

Table 13. PLL Output Divider N (FSEL_A to FSEL_D)

FSEL_x[1:0]	Value
00	÷2
01	÷4
10	÷8
11	÷16

Mode Configuration Register

The mode configuration register, refer to Table 14, is a read/write register and contains the fields for mode selection as well as alarm reset.

The mode of the MPC9894 may be changed by writing the three least significant Mode Configuration Register bits to the desired value. The current idcs mode of the MPC9894 may be obtained by reading this register.

The alarm reset bits, found in bit positions 6 thru 3, may be used to individually reset the status flags of register 5. Each of these flag bits are associated with the four clock inputs pins and indicate a failed clock input. Clearing of a clock status flag is performed by writing a logic 1 to the individual bit (or bits if more than one flag is to be cleared). Care should be taken to insure that the idcs mode information is written to the proper value when resetting the clock status bits. The four alarm reset bits always read as a logic 0. If a clock input status flag is cleared and the clock input is still in a failed state, the status flag will go set within 4 clock cycles after being cleared.

Table 14. Mode Configuration and Alarm Reset Register (Register 2 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	not used	ALARM_RST[3:0] (Refer to Table 15)				IDCS_MODE[2:0] (Refer to Table 16)		
Reset default	n/a	n/a	n/a	n/a	n/a	0	1	1
Preset default	n/a	n/a	n/a	n/a	n/a	1	0	0

Table 15. Individual Reset of CLK_STAT[x] Bits

ALARM_RST[x]	Description
0	No action
1	The status flag CLK_STAT[x] is cleared by setting of this bit. (bit always reads as zero)

Table 16. MPC9894 IDCS Configuration[1]

IDCS_MODE [2:0]	Description	Primary clock	Secondary clock[2]	Tertiary clock[b]	Quaternary clock[b]
000	Manual	CLK0	n/a	n/a	n/a
001		CLK1	n/a	n/a	n/a
010		CLK2	n/a	n/a	n/a
011		CLK3	n/a	n/a	n/a
100	Automatic	CLK0	CLK1	CLK2	CLK3
101		CLK1	CLK2	CLK3	CLK0
110		CLK2	CLK3	CLK0	CLK1
111		CLK3	CLK0	CLK1	CLK2

1. This is a repeat of Table 8.
2. For CLK_VALID[3:0] = 1111 and input clock validity.

Device Configuration and Output Enable Register

The Device Configuration and Output Enable Register is used to individually enable or disable each bank of outputs. Output banks are enabled by setting the corresponding bit to a logic 1 and disabled by setting the bit to a logic 0 as described in Table 21. Output Clock Stop/Enable. The disable logic sets the outputs of the addressed bank synchronously to logic low state (Qx[] = 0 and $\overline{Qx[]}$ = 1). The clock output enable/stop bits can be set asynchronous to any clock signal without the risk of generating of runt pulses. The PLL feedback output QFB cannot be disabled when MPC9894 is configured for external feedback.

The Device Configuration Register, bit 6, QUAL_EN is used to enable or disable all clock input qualifier pins. Asserting this bit enables the Clock Qualifier Input Pins CLK_VALID[3:0]. Deasserting this bit disables these pins such that inputs on CLK_VALID[3:0] are ignored.

The INT_E bit, in bit position 7, is used to enable or disable interrupts from occurring on the INT pin. The setting of the interrupt flag (bit 7 of the Status Register) is unaffected by this bit.

Table 17. Device Configuration and Output Clock Enable Register (Register 3 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	INT_E	QUAL_EN	Slew_Control	Enable_QFB	ENABLE_QA	ENABLE_QB	ENABLE_QC	ENABLE_QD
Reset default	0	0	0	0	0	0	0	0
Preset default	1	1	0	0	1	1	1	1

Table 18. Interrupt Signal ($\overline{INT}$) Enable INT_E

INT_E	Description
0	Interrupt signal $\overline{INT}$ is disabled
1	Interrupt signal $\overline{INT}$ is enabled

Table 19. Input Clock Qualifier Enable QUAL_EN

QUAL_EN	Description
0	CLK_VALID[3:0] are disabled (clock qualifier signals are disabled)
1	CLK_VALID[3:0] are enabled (clocks can be qualified)

Table 20. Slew Control

Slew_Control	Description
0	Clock slew direction on clock switch is toward the closest edge
1	Clock slew direction on clock switch is toward the lagging edge

Table 21. Output Clock Stop/Enable

ENABLE_Qx	Description
0	Output bank x is disabled (clock stop in logic low state)
1	Output bank x is enabled

Input and Feedback Divider Configuration Register

Table 22. Input and Feedback Divider Configuration Register (Register 4 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Reserved	Reserved	Reserved	Input_FB_Div[3:0]			
Reset default	n/a	n/a	n/a	n/a	0	0	0	0
Preset default	n/a	n/a	n/a	n/a	0	0	1	1

The Input and Feedback Divider Configuration Register is used to select the input divider value and the feedback divider values. The four bits for Input_FB_Div allow 16 combinations of input and feedback divider ratios. Some input and output frequency ranges may overlap allowing a choice of PLL closed loop bandwidths. This selection may be useful when PLL devices are cascaded.

Table 23. Input_FB_Div[3:0]

Input_FB_Div[3:0]	Input Divider (P)	Feedback Divider (M)
0000	1	16
0001	1	12
0010	2	12
0011	1	8
0100	2	16
0101	reserved	
0110	2	8
0111	3	12
1000	4	16
1001	reserved	
1010	4	12
1011	reserved	
1100	reserved	
1101	reserved	
1110	4	8
1111	6	12

Device Status Register

The Device Status Register contains a copy of the status SEL_STAT[1:0], $\overline{\text{LOCK}}$ and CLK_STAT[3:0] pins. In addition, bit 7 is an INT flag bit, which is used to indicate a setting of a bit in the CLK_STAT[3:0], a clearing of the $\overline{\text{LOCK}}$ bit and a change in the value of the SEL_STAT[1:0] bits.

The CLK_STAT[3:0] bits are sticky and remain set until manually reset through the Mode Configuration Register.

The setting of the register INT bit is reflected on the interrupt pin only if interrupts are enabled. Enabling interrupts is done by the setting of the INT_E bit which is located in the Device Configuration Register. Reading of the Status Register clears the INT flag.

Table 24. Status Register (Register 5 — Read Only)

Bit	7	6	5	4	3	2	1	0
Description	INT Inverse of $\overline{\text{INT}}$ signal	CLK_STAT[3:0] Status of CLK3, CLK2, CLK1 and CLK0 (sticky) Copy of CLK_STAT[3:0] signal				LOCK Inverse of $\overline{\text{LOCK}}$ signal	SEL_STAT[1:0] Copy of SEL_STAT[1:0] signal	

Output Power-Up Register

The Output Power-Up Register configures each of the 8 LVPECL outputs for either power-up or a power-down state. The use of these bits allows power consumption to be reduced when all of the clock outputs are not used. Placing an output in the power-down condition is not synchronous with the clock edges.

Table 25. Output Power-Up Register (Register 6 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	PWR_QD1	PWR_QD0	PWR_QC1	PWR_QC0	PWR_QB1	PWR_QB01	PWR_QA1	PWR_QA0
Reset Default	0	0	0	0	0	0	0	0
Preset Default	1	1	1	1	1	1	1	1

Table 26. Clock Output Power-Up Bits

PWR_Qxx	Description
0	Output Power-Down
1	Output Power-Up

Feedback Power-Up Register

The Feedback Power-Up register bit 0 is used to configure the MPC9894 feedback output in either a power-up state or a power-down state. Note this register bit is valid for internal feedback configuration only. When external feedback is selected QFB is always enabled and in a power-up state. The remaining bits of this register are unused and read as a logic 0.

Table 27. Feedback Power-Up Register (Register 7 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description								PWR_QFB
Reset Default								0
Preset Default								1

Table 28. Feedback Output Power-Up Bit

PWR_QFB	Description
0	Feedback Output Power-Down
1	Feedback Output Power-Up

IEEE STD.1149.1(JTAG)

This section describes the IEEE Std. 1149.1 compliant Test Access Port (TAP) and Boundary Scan Architecture implementation in the MPC9894. Special private instructions are provided to assist in production test control. These instructions combined with control of the test mode inputs and the use of shared inputs and outputs provide for full production test mode access and control.

Test Access Port Interface Signals

Table 29 lists the TAP interface signals and their descriptions.

Table 29. TAP Interface Signals

Signal Name	Description	Function	Direction	Active State
TCK	Test Clock	Test logic clock.	Input	—
TMS	Test Mode Select	TAP mode control input.	Input	—
TDI	Test Data In	Serial test instruction/data input.	Input	—
TRST_B	Test Reset Bar	Asynchronous test controller reset.	Input	—
TDO	Test Data Out	Serial test instruction/data output.	Output	—

Instruction Register

Table 30. Instruction Register

Bit Position	4	3	2	1	0
Field	IR				
Capture-IR Value	0	0	0	0	1

Instructions

Table 31 lists the public instructions provided in the implementation and their instruction codes. Public instructions are accessible by the customer for board test and may also be used for production chip test.

Table 31. TAP Controller Public Instructions

Instruction	Code	Enabled Serial Test Data Path
BYPASS	11111	Bypass Register
CLAMP	01100	Bypass Register
EXTEST	00000	Boundary Scan Register
HIGHZ	01001	Bypass Register
IDCODE	00001	ID Register
SAMPLE	00010	Boundary Scan Register

Boundary-Scan Register

A full description of the boundary scan register may be found in the BSDL file.

Device Identification Register (0x0281D01D)

Table 32. Device Identification Register

Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Field	Version				Part Number																Manufacturer ID											
Value	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	0	1	1	1	0	1

POWER SUPPLY CONFIGURATION

The MPC9894 operates from either a 3.3 V or 2.5 V voltage supply for the device core. The pin SEL_2P5V is used to logically indicate the core supply voltage. This selection is done by setting the pin to a logic 1 for 2.5 V or logic 0 for 3.3 V operation.

The input and output supply voltage may be set for either 3.3 V or 2.5 V and can be individually set for inputs and banks of outputs. Table 33. Power Supply Configuration lists the supply pins and what pin or group of pins are associated with each supply. Note, that for output skew and SPO specifications to be valid the input, feedback input and output, and the output bank must all be at the same voltage level.

Table 33. Power Supply Configuration

Supply Voltage	Description	Value
V_{DD}	Positive power supply for the device core, output status and control inputs. (3.3 V or 2.5 V)	3.3 V or 2.5 V
V_{DDAB}	Supply voltage for output banks A and B (QA0 through QB1)	3.3 V or 2.5 V
V_{DDCD}	Supply voltage for output banks A and B (QC0 through QD1) and QFB	3.3 V or 2.5 V
V_{DDIC}[1]	Supply voltage for differential inputs clock inputs CLK0 to CLK3 and FB_IN	3.3 V or 2.5 V
V_{DDA}	Clean supply for Analog portions of the PLL (This voltage is derived via an RC filter from the V_{DD} supply)	Derived from V_{DD}

1. V_{DDIC} (Supply of FB_IN) must be equal to V_{DDCD} (Supply of QFB) to ensure the SPO specification is met.

Power Supply Sequencing and $\overline{MR}$ Operation

Figure 5 defines the release time and the minimum pulse length for $\overline{MR}$ pin. The $\overline{MR}$ release time is based upon the power supply being stable and within V_{DD} specifications. Refer to Table 39 for actual parameter values. The MPC9894 may be configured after release of reset and the outputs will be stable for use after lock indication is obtained.

V_{DD} must ramp up prior to or concurrent with the other power supply pins. It is recommended that the maximum slew rate for the V_{DD} supply not exceed 0.5 V/ms.

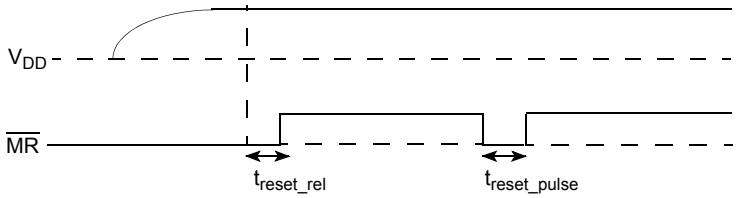


Figure 5. MR Operation

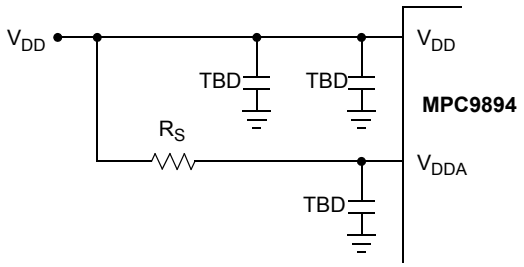


Figure 6. V_{CC} Power Supply Bypass

Power Supply Bypassing

The MPC9894 is a mixed analog/digital product. The differential architecture of the MPC9894 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

Clock Outputs

The MPC9894 clock outputs are differential LVPECL voltage compatible. The outputs are designed to drive a single 50 Ω impedance load that is properly terminated. The media pin is used to select between either of two output termination techniques.

Selection of media = 0 sets all of the outputs to drive up to 50 Ω parallel terminated (to V_{TT}) transmission lines. With media = 1 the outputs are designed to drive 50 Ω transmission line terminated with a single 100 differential load resistor. See Figure 7 and Figure 8 for diagrams of each of these termination techniques. Note, that the traditional output pulldown resistors for emitter follower biasing are not required for the MPC9894. If external feedback is used, the QFB output must be terminated with the same technique as selected with the media pin. Once a termination technique is chosen, that technique must be used for all MPC9894 outputs to guarantee output skew timing.

The recommended termination technique is media = 1. This provides a simpler termination method and also reduces overall power consumption of the MPC9894. Unused outputs may be powered-down via the Output Power-Up and Feedback Power-Up registers to conserve power. If external feedback is selected the programming of the PWR_QFB bit is ignored.

Table 34. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{DD}	Supply Voltage (core)	–0.3	4.0	V	
$V_{DDAB, CD}$	Supply Voltage (differential outputs)	–0.3	4.0	V	
V_{DDIC}	Supply Voltage (differential inputs)	–0.3	4.0	V	
V_{DDA}	Supply Voltage (Analog Supply Voltage)	–0.3	V_{DD}	V	
V_{IN}	DC Input Voltage[2]	–0.3	V_{DDx}+0.3	V	
V_{OUT}	DC Output Voltage[3]	–0.3	V_{DDx}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.
2. V_{DDx} references power supply pin associated with specific input pin.
3. V_{DDx} references power supply pin associated with specific output pin.

Table 35. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage (LVPECL)		V_{DD} – 2		V	LVPECL outputs
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
CDM	ESD Protection (Charged Device Model)	500			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		TBD		pF	Inputs
θ_{JC}	Thermal Resistance (junction-to-ambient, junction-to-board, junction-to-case)		TBD		°C/W	
T_J	Junction Temperature[1]	–40		110	°C	

1. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (Refer to Application Note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9894 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9894 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 36. DC Characteristics (T_J = –40°C to +110°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Supply Current for V_{DD} = 2.5 V±5% and $V_{DDAB,CD}$ = 2.5 V±5%						
I_{DD}	Maximum Quiescent Supply Current (core)		TBD	TBD	mA	V_{DD} pins
$I_{DDAB, CD}$[2]	Maximum Quiescent Supply Current, outputs terminated 50 Ω to V_{TT}		TBD	TBD	mA	V_{DDAB} and V_{DDCD} pins
I_{DDA}	Maximum Supply Current (Analog Supply)		TBD	TBD	mA	V_{DDA} pin
I_{DDIC}	Maximum Quiescent Supply Current (I/O)		TBD	TBD	mA	V_{DDIC} pins
Supply Current for V_{DD} = 3.3 V±5% and $V_{DDAB,CD}$ = 3.3 V±5% or $V_{DDAB,CD}$ = 2.5 V±5%						
I_{DD}	Maximum Quiescent Supply Current (core)		TBD	TBD	mA	V_{DD} pins
$I_{DDAB, CD}$[3]	Maximum Quiescent Supply Current, outputs terminated 50 Ω to V_{TT}		TBD	TBD	mA	V_{DDAB} and V_{DDCD} pins
I_{DDA}	Maximum Supply Current (Analog Supply)		TBD	TBD	mA	V_{DDIN} pins
I_{DDIC}	Maximum Quiescent Supply Current (I/O)		TBD	TBD	mA	V_{DDIC} pins

1. DC characteristics are design targets and pending characterization.
2. $I_{DDAB, CD}$ includes current through the output resistors (all outputs terminated to V_{TT}).
3. $I_{DDAB, CD}$ includes current through the output resistors (all outputs terminated to V_{TT}).

Table 37. PECL DC Characteristics (T_J = –40°C to +110°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Differential PECL clock inputs (CLKx, $\overline{CLKx}$ and FB_IN, $\overline{FB\_IN}$)[2] for V_{DDIC} = 3.3 V ±5% or V_{DDIC} = 2.5 V ±5%						
V_{PKPK}	AC Differential Input Voltage[3]	0.2		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[4]	1.25		V_{DD}–0.3	V	Differential operation
I_{IN}	Input Current[1]			±100	μA	V_{PP} = 0.8 V and V_{CMR} = V_{DDL}–0.7 V
Differential PECL clock outputs (QA0 to QD1 and QFB) for $V_{DDAB,CD}$ = 3.3 V ±5% or $V_{DDAB,CD}$ = 2.5 V ±5%						
V_{OH}	Output High Voltage	TBD	$V_{DDAB,CD}$–1.0	TBD	V	Termination 50 Ω to V_{TT}
V_{OL}	Output Low Voltage	TBD	$V_{DDAB,CD}$–1.7	TBD	V	Termination 50 Ω to V_{TT}
Z_{OUT}	Output Impedance MEDIA = 0 MEDIA = 1		TBD 50		Ω Ω	See Figure 7 See Figure 8

1. DC characteristics are design targets and pending characterization.
2. Clock inputs driven by PECL compatible signals.
3. V_{PKPK} is the minimum differential input voltage swing required to maintain AC characteristics.
4. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 38. LVCMOS I/O DC Characteristics (T_J = –40°C to +110°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Single-ended LVCMOS inputs for V_{DD} = 3.3 V ±5%						
V_{IH}	Input High Voltage	2.0		V_{DD} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –6 mA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 6 mA
Z_{OUT}	Output Impedance	40		62	Ω	
I_{IN}	Input Current[2]			10	μA	V_{IN} = V_{DDL} or GND
Single-ended LVCMOS inputs for V_{DD} = 2.5 V ±5%						
V_{IH}	Input High Voltage	1.7		V_{DD} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.9			V	I_{OH} = -6 mA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 6 mA
Z_{OUT}	Output Impedance	45		70	Ω	
I_{IN}	Input Current[2]			10	μA	V_{IN} = V_{DDL} or GND

1. DC characteristics are design targets and pending characterization.
2. Inputs have pull-down resistors affecting the input current.

Table 39. AC Characteristics (T_J = –40°C to +110°C)[1] [2]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{DD} = 3.3 V ±5%, $V_{DDAB,CD,IC}$ = 3.3 V ±5% or $V_{DDAB,CD,IC}$ = 2.5 V ±5%						
Input and output timing specification						
f_{REF}	Input reference frequency	21.25 28.33 56.66 42.5 85.0 113.32 170		42.5 56.67 113.34 85 170 226.68 340	MHz MHz MHz MHz MHz MHz MHz	Input_FB_Div[3:0] = 0 Input_FB_Div[3:0] = 1 Input_FB_Div[3:0] = 2 Input_FB_Div[3:0] = 3,4 Input_FB_Div[3:0] = 6,7,8 Input_FB_Div[3:0] = 10 Input_FB_Div[3:0] = 14,15
	Input reference frequency in PLL bypass mode[3]			TBD	MHz	PLL bypass
f_{VCO}	VCO frequency range[4]	340		680	MHz	
f_{MAX}	Output Frequency ÷2 output ÷4 output ÷8 output ÷16 output	170.0 85.0 42.5 21.25		340.0 170.0 85.0 42.5	MHz MHz MHz MHz	PLL locked
f_{REFDC}	Reference Input Duty Cycle	40		60	%	
f_{REFacc}	Input Frequency Accuracy[5]			500	ppm	
$mae_{(\varnothing)}$	Misaligned Edge Specification	±600		±1600	ps	
t_r, t_f	Output Rise/Fall Time			800	ps	20% to 80%
DC	Output duty cycle	47.5	50	52.5	%	
f_{I2C}	I^2C frequency range			100	kHz	
Differential input and output voltages						
V_{PP}	Differential input voltage[6] (peak-to-peak) (PECL)			1.3	V	
$V_{PP, OK}$	Differential input voltage[7] (peak-to-peak) (PECL)	TBD			V	
$V_{PP, NOK}$	Differential input voltage[8] (peak-to-peak) (PECL)			TBD	V	
$V_{O(P-P)}$	Differential output voltage (peak-to-peak) (PECL)	TBD	0.8		V	
PLL and IDCS specifications						
$t_{(\varnothing)}$	Propagation Delay (static phase offset) CLKX, $\overline{CLKX}$ to FB_IN, $\overline{FB\_IN}$	 -100		+100	ps	PLL locked with external feedback selected
$t_{sk(O)}$	Output-to-output Skew within a bank[9] Output-to-output Skew across a bank[9]			50 TBD	ps	
$^{\Delta}$PER/CYC	Rate of change of period[10] ÷2 output ÷4 output ÷8 output ÷16 output			+40 +80 +120 +160	ps	slew_control = 1
$^{\Delta}$PER/CYC	Rate of change of period[11] ÷2 output ÷4 output ÷8 output ÷16 output			±40 ±80 ±120 ±160	ps	slew_control = 0
Jitter and bandwidth specifications						
$t_{JIT(CC)}$	Cycle-to-cycle jitterRMS (1 σ)			10	ps	
$t_{JIT(PER)}$	Period JitterRMS (1 σ)		TBD		ps	
$t_{JIT(ý)}$	I/O Phase JitterRMS (1 σ)		TBD		ps	
BW	PLL closed loop bandwidth[12]		TBD		kHz	

Table 39. AC Characteristics (T_J = –40°C to +110°C)[1] [2] (Continued)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{DD} = 3.3 V ±5%, $V_{DDAB,CD,IC}$ = 3.3 V ±5% or $V_{DDAB,CD,IC}$ = 2.5 V ±5%						
$\overline{MR}$ and PLL Lock						
t_{LOCK}	Maximum PLL Lock Time			10	µs	
t_{reset_ref}	$\overline{MR}$ hold time on power up	2			ps	
t_{reset_pulse}	$\overline{MR}$ hold time	100			ns	

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
3. In bypass mode, the MPC9894 divides the input reference clock.
4. The input reference frequency must match the VCO lock range divided by the total feedback divider ratio: $f_{REF} = (f_{VCO} \div M) \cdot N$.
5. All Input Clock frequencies must be within this value to guarantee smooth phase transition on input clock switch.
6. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
7. $V_{PP, OK}$ is the minimum differential input voltage swing required for a valid clock signal. Above $V_{PP, OK}$ the input will be detected as a good clock (see IDCS).
8. $V_{PP, NOK}$ is the maximum differential input voltage swing for a guaranteed bad clock. Below $V_{PP, NOK}$ the input will be detected as a failed clock (see IDCS).
9. $V_{DDAB} = V_{DDCD}$
10. Rate of period change is the maximum change of the clock output signal period T per cycle on a IDCS commanded switch.
11. Rate of period change is the maximum change of the clock output signal period T per cycle on a IDCS commanded switch.
12. –3 dB point of PLL transfer characteristics.

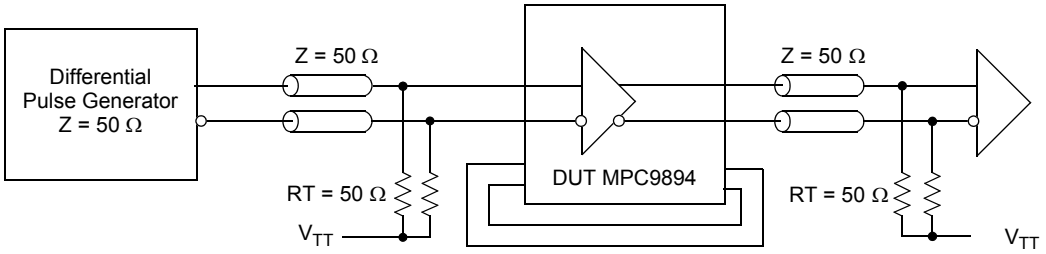


Figure 7. MPC9894 AC Test Reference (Media = 0)

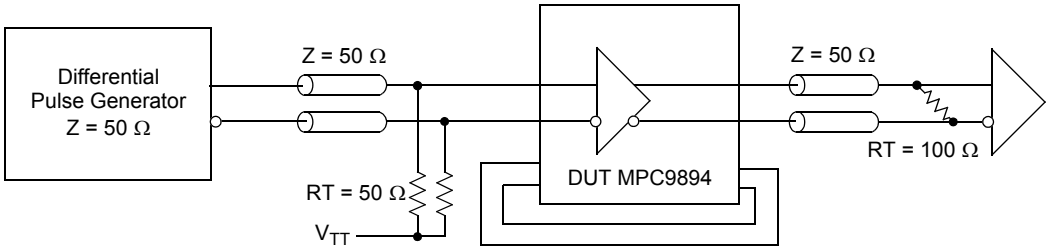


Figure 8 . MPC9894 AC Test Reference (Media = 1)

MPC9894 Pin and Package

Table 40. MPC9894 Pin Listing

Signal Name	Description	Direction	Type	Active State	Supply	Pin
CLK0	Clock0 Positive Input	Input	LVPECL	—	V_{DDIC}	D1
$\overline{\text{CLK0}}$	Clock0 Negative Input	Input	LVPECL	—	V_{DDIC}	D2
CLK1	Clock1 Positive Input	Input	LVPECL	—	V_{DDIC}	E3
$\overline{\text{CLK1}}$	Clock1 Negative Input	Input	LVPECL	—	V_{DDIC}	E2
CLK2	Clock2 Positive Input	Input	LVPECL	—	V_{DDIC}	F3
$\overline{\text{CLK2}}$	Clock2 Negative Input	Input	LVPECL	—	V_{DDIC}	F2
CLK3	Clock3 Positive Input	Input	LVPECL	—	V_{DDIC}	G1
$\overline{\text{CLK3}}$	Clock3 Negative Input	Input	LVPECL	—	V_{DDIC}	G2
FB_IN	Feedback Clock Positive Input	Input	LVPECL	—	V_{DDIC}	C1
$\overline{\text{FB\_IN}}$	Feedback Clock Negative Input	Input	LVPECL	—	V_{DDIC}	C2
QA0	Positive Differential Clock Output	Output	LVPECL	—	V_{DDAB}	K4
$\overline{\text{QA0}}$	Negative Differential Clock Output	Output	LVPECL	—	V_{DDAB}	J4
QA1	Positive Differential Clock Output	Output	LVPECL	—	V_{DDAB}	K5
$\overline{\text{QA1}}$	Negative Differential Clock Output	Output	LVPECL	—	V_{DDAB}	J5
QB0	Positive Differential Clock Output	Output	LVPECL	—	V_{DDAB}	K7
$\overline{\text{QB0}}$	Negative Differential Clock Output	Output	LVPECL	—	V_{DDAB}	J7
QB1	Positive Differential Clock Output	Output	LVPECL	—	V_{DDAB}	K6
$\overline{\text{QB1}}$	Negative Differential Clock Output	Output	LVPECL	—	V_{DDAB}	J6
QC0	Positive Differential Clock Output	Output	LVPECL	—	V_{DDCD}	A7
$\overline{\text{QC0}}$	Negative Differential Clock Output	Output	LVPECL	—	V_{DDCD}	B7
QC1	Positive Differential Clock Output	Output	LVPECL	—	V_{DDCD}	A6
$\overline{\text{QC1}}$	Negative Differential Clock Output	Output	LVPECL	—	V_{DDCD}	B6
QD0	Positive Differential Clock Output	Output	LVPECL	—	V_{DDCD}	A4
$\overline{\text{QD0}}$	Negative Differential Clock Output	Output	LVPECL	—	V_{DDCD}	B4
QD1	Positive Differential Clock Output	Output	LVPECL	—	V_{DDCD}	A5
$\overline{\text{QD1}}$	Negative Differential Clock Output	Output	LVPECL	—	V_{DDCD}	B5
QFB	Positive Differential Clock Output	Output	LVPECL	—	V_{DDCD}	A3
$\overline{\text{QFB}}$	Negative Differential Clock Output	Output	LVPECL	—	V_{DDCD}	B3
CLK_VALID3	Qualifier for clock input CLK3	Input	LVCMOS	High	V_{DD}	F10
CLK_VALID2	Qualifier for clock input CLK2	Input	LVCMOS	High	V_{DD}	E10
CLK_VALID1	Qualifier for clock input CLK1	Input	LVCMOS	High	V_{DD}	E9
CLK_VALID0	Qualifier for clock input CLK0	Input	LVCMOS	High	V_{DD}	E8
$\overline{\text{CLK\_ALARM\_RST}}$	Reset of all four alarm status flags and clock selection status flag	Input	LVCMOS	Low	V_{DD}	F8
PLL_BYPASS	Select PLL of static test mode	Input	LVCMOS	High	V_{DD}	F9
MEDIA	Output impedance control (high = 50 Ω)	Input	LVCMOS	High	V_{DD}	E7
SCL	I^2C Interface Control, Clock	I/O	LVCMOS	—	V_{DD}	C9
SDA	I^2C Interface Control, Data	I/O	LVCMOS	—	V_{DD}	C10

Table 40. MPC9894 Pin Listing (Continued)

Signal Name	Description	Direction	Type	Active State	Supply	Pin
ADDR2	I^2C Interface Control, Address 2 (MSB)	Input	LVCMOS	—	V_{DD}	A9
ADDR1	I^2C Interface Control, Address 1	Input	LVCMOS	—	V_{DD}	B8
ADDR0	I^2C Interface Control, Address 1 (LSB)	Input	LVCMOS	—	V_{DD}	A8
$\overline{MR}$	Device Master Reset	Input	LVCMOS	Low	V_{DD}	D10
$\overline{LOCK}$	PLL Lock Indicator	Output	LVCMOS	Low	V_{DD}	G10
CLK_STAT3	Input CLK3 status indicator	Output	LVCMOS	High	V_{DD}	H9
CLK_STAT2	Input CLK2 status indicator	Output	LVCMOS	High	V_{DD}	H10
CLK_STAT1	Input CLK1 status indicator	Output	LVCMOS	High	V_{DD}	G8
CLK_STAT0	Input CLK0 status indicator	Output	LVCMOS	High	V_{DD}	G9
SEL_STAT1	Reference Clock Selection Indicator (MSB)	Output	LVCMOS	High	V_{DD}	K8
SEL_STAT0	Reference Clock Selection Indicator (LSB)	Output	LVCMOS	High	V_{DD}	J8
$\overline{BUSY}$	IDCS switch activity indicator	Output	LVCMOS	High	V_{DD}	J10
MBOOT	Activates I^2C Boot Sequence	Input	LVCMOS	High	V_{DD}	D8
$\overline{INT}$	Indicates any status IDCS change	Output	OD	n/a	V_{DD}	D9
PRESET	Sets preset state	Input	LVCMOS	High	V_{DD}	H7
TMS	JTAG Test Mode Select	Input	LVCMOS	High	V_{DDIC}	D3
TDI	JTAG Test Data Input	Input	LVCMOS	—	V_{DDIC}	H1
$\overline{TRST}$	JTAG Test Reset Bar	Input	LVCMOS	Low	V_{DD}	H2
TCK	JTAG Test Clock	Input	LVCMOS	—	V_{DDIC}	G3
TDO	JTAG Test Data Out	Output	LVCMOS	—	V_{DDIC}	J3
SEL_2P5V	Indicate core VDD level, (high = 2.5V, low = 3.3V)	Input	LVCMOS	—	V_{DD}	D7
MSTROUT_EN	Enable all outputs in sync	Input	LVCMOS	High	V_{DD}	K9
PLL_TEST2	PLL Test Bit 2	Input	LVCMOS	—	V_{DDAB}	H4
PLL_TEST1	PLL Test Bit 1	Input	LVCMOS	—	V_{DDAB}	G5
PLL_TEST0	PLL Test Bit 0 (LSB)	Input	LVCMOS	—	V_{DDCD}	D5
TPA	PLL Analog Test Pin	Output	Analog	—	V_{DDA}	E4
EX_FB_SEL	Select feedback mode (high = external)	Input	LVCMOS	—	V_{DD}	C7
V_{DD}	Control Input, Status Output and Core Supply	Power	—	—	V_{DD}	A10, B9, C3, C8, G7, H8, J9, K10
V_{DDA}	Analog Supply	Power	—	—	V_{DDA}	E1
V_{DDAB}	Supply for A and B bank outputs	Power	—	—	V_{DDAB}	H6, J2, K2
V_{DDCD}	Supply for C and D bank outputs	Power	—	—	V_{DDCD}	A1, C4, C6
V_{DDIC}	Supply for input clocks	Power	—	—	V_{DDIC}	B2, H3, K1
GND	Control Input, Status Output and Core Ground	Ground	—	—	GND	A2, B1, B10, C5, D4, D6, E5, E6, F1, F4, F5, F6, F7, G4, G6, H5, J1, K3

Table 41. MPC9894 PIN DIAGRAM

	1	2	3	4	5	6	7	8	9	10
A	V_{DDC}	GND	QFB	QD0	QD1	QC1	QC0	ADDR0	ADDR2	V_{DD}
B	GND	V_{DDIC}	$\overline{QFB}$	$\overline{QD0}$	$\overline{QD1}$	$\overline{QC1}$	$\overline{QC0}$	ADDR1	V_{DD}	GND
C	FB_IN	$\overline{FB\_IN}$	V_{DD}	V_{DDCD}	GND	V_{DDCD}	EX_FB_SEL	V_{DD}	SCL	SDA
D	CLK0	$\overline{CLK0}$	TMS	GND	PLL_TEST0	GND	SEL_2P5V	MBOOT	$\overline{INT}$	$\overline{MR}$
E	V_{DDA}	$\overline{CLK1}$	CLK1	TPA	GND	GND	MEDIA	CLK_ VALID0	CLK_ VALID1	CLK_ VALID2
F	GND	$\overline{CLK2}$	CLK2	GND	GND	GND	GND	$\overline{CLK\_ALARM\_RST}$	PLL_ BYPASS	CLK_ VALID3
G	CLK3	$\overline{CLK3}$	TCK	GND	PLL_TEST1	GND	V_{DD}	CLK_ STAT1	CLK_ STAT0	$\overline{LOCK}$
H	TDI	$\overline{TRST}$	VDDIC	PLL_TEST2	GND	V_{DDAB}	PRESET	V_{DD}	CLK_ STAT3	CLK_ STAT2
J	GND	V_{DDAB}	TDO	$\overline{QA0}$	$\overline{QA1}$	$\overline{QB1}$	$\overline{QB0}$	SEL_STAT0	V_{DD}	$\overline{BUSY}$
K	V_{DDIC}	V_{DDAB}	GND	QA0	QA1	QB1	QB0	SEL_ STAT1	MSTROUT _EN	V_{DD}

MPC9894 PROGRAMMING MODEL

Table 42. Slave Address (Register 0 — Read Only)

Bit	7	6	5	4	3	2	1	0
Description	not used	ADDR_6	ADD_R5	ADDR_4	ADDR_3	ADDR_2 read from ADDR[2] pin	ADDR_1 read from ADR[1] pin	ADDR_0 read from ADDR[0] pin
Reset default		x (TBD)	x (TBD)	x (TBD)	x (TBD)			
Preset default		x (TBD)	x (TBD)	x (TBD)	x (TBD)			

Table 43. Output Configuration Register (Register 1 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	FSEL_A[1:0]		FSEL_B[1:0]		FSEL_C[1:0]		FSEL_D[1:0]	
Reset default	0	0	0	0	0	0	0	0
Preset default	0	0	0	0	1	0	1	0

Table 44. Mode Configuration and Alarm Reset Register (Register 2 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	not used	ALARM_RST[3:0] (See Table 15)				IDCS_MODE[2:0] (See Table 16)		
Reset default	n/a	n/a	n/a	n/a	n/a	0	1	1
Preset default	n/a	n/a	n/a	n/a	n/a	1	0	0

Table 45. Device Configuration and Output Clock Enable Register (Register 3 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	INT_E	QUAL_EN	Slew_Control	Enable_QFB	ENABLE_QA	ENABLE_QB	ENABLE_QC	ENABLE_QD
Reset default	0	0	0	0	0	0	0	0
Preset default	1	1	0	0	1	1	1	1

Table 46I. nput and Feedback Divider Configuration Register (Register 4 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	Reserved	Reserved	Reserved	Reserved	Input_FB_Div[3:0]			
Reset default	n/a	n/a	n/a	n/a	0	0	0	0
Preset default	n/a	n/a	n/a	n/a	0	0	1	1

Table 47. Status Register (Register 5 — Read Only)

Bit	7	6	5	4	3	2	1	0
Description	INT Inverse of $\overline{\text{INT}}$ signal	CLK_STAT[3:0] Status of CLK3, CLK2, CLK1 and CLK0 (sticky) Copy of CLK_STAT[3:0] signal				LOCK Inverse of $\overline{\text{LOCK}}$ signal	SEL_STAT[1:0] Copy of SEL_STAT[1:0] signal	

Table 48. Output Power-Up Register (Register 6 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description	PWR_QD1	PWR_QD0	PWR_QC1	PWR_QC0	PWR_QB1	PWR_QB01	PWR_QA1	PWR_QA0
Reset Default	0	0	0	0	0	0	0	0
Preset Default	1	1	1	1	1	1	1	1

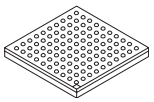
Table 49. Feedback Power-Up Register (Register 7 — Read/Write)

Bit	7	6	5	4	3	2	1	0
Description								PWR_QFB
Reset Default								0
Preset Default								1

Low Voltage PLL Intelligent Dynamic Clock (IDCS) Switch

MPC9895

3.3V IDCS AND PLL CLOCK GENERATOR



VF SUFFIX
100-LEAD MAPBGA PACKAGE
CASE 1462-01

The MPC9895 is a 3.3V compatible, PLL based intelligent dynamic clock switch and generator specifically designed for redundant clock distribution systems. The device receives two LVCMOS clock signals and generates 12 phase aligned output clocks. The MPC9895 is able to detect a failing reference clock signal and to dynamically switch to a redundant clock signal. The switch from the failing clock to the redundant clock occurs without interruption of the output clock signal (output clock slews to alignment). The phase bump typically caused by a clock failure is eliminated.

The device offers 12 low skew clock outputs organized into two output banks.

The extended temperature range of the MPC9895 supports telecommunication and networking requirements. The device employs a fully differential PLL design to minimize jitter.

Features

- 12 output LVCMOS PLL clock generator
- 3.3V compatible
- IDCS – on-chip intelligent dynamic clock switch
- Automatically detects clock failure
- Smooth output phase transition during clock failover switch
- 50 – 200 MHz output frequency range
- LVCMOS compatible inputs and outputs
- External feedback enables zero-delay configurations
- Supports networking, telecommunications and computer applications
- Output enable/disable and static test mode (PLL bypass)
- Low skew characteristics: maximum 150 ps(1) output-to-output
- 100 ball MAPBGA package, 1 mm ball pitch
- Ambient temperature range –40°C to +85°C

Functional Description

The MPC9895 is a 3.3V compatible PLL clock driver and clock generator. The clock generator uses a fully integrated PLL to generate clock signals from redundant clock sources. The PLL multiplies the input reference clock signal by 4, 8, 16 or 32. The frequency-multiplied clock drives six bank A outputs and six bank B outputs. Bank A and bank B outputs are phase-aligned. Due to the external PLL feedback, the clock signals of both output banks are also phase-aligned to the selected input reference clock, providing virtually zero-delay capability. The integrated IDCS continuously monitors both clock inputs and indicates a clock failure individually for each clock input. When a false clock signal is detected, the MPC9895 switches to the redundant clock input, forcing the PLL to slowly slew to alignment and not produce any phase bumps at the outputs. Both clock inputs are interchangeable. The automatic switch operation to a restored (fixed) clock signal is also supported. The MPC9895 also provides a manual mode that allows for user-controlled clock switches.

The PLL bypass of the MPC9895 disables the IDCS and PLL-related PLL specifications do not apply. In PLL bypass mode, the MPC9895 is fully static in order to distribute low-frequency clocks for system test and diagnosis. Outputs of the MPC9895 can be disabled (high-impedance state) to isolate the device from the system. Applying output disable also resets the MPC9895. On power-up this reset function needs to be applied for correct operation of the circuitry. Please see <st-blue>APPLICATIONS INFORMATION for power-on sequence recommendations.

The device is packaged in 100-ball MAPBGA package.

1. Final specification subject to change

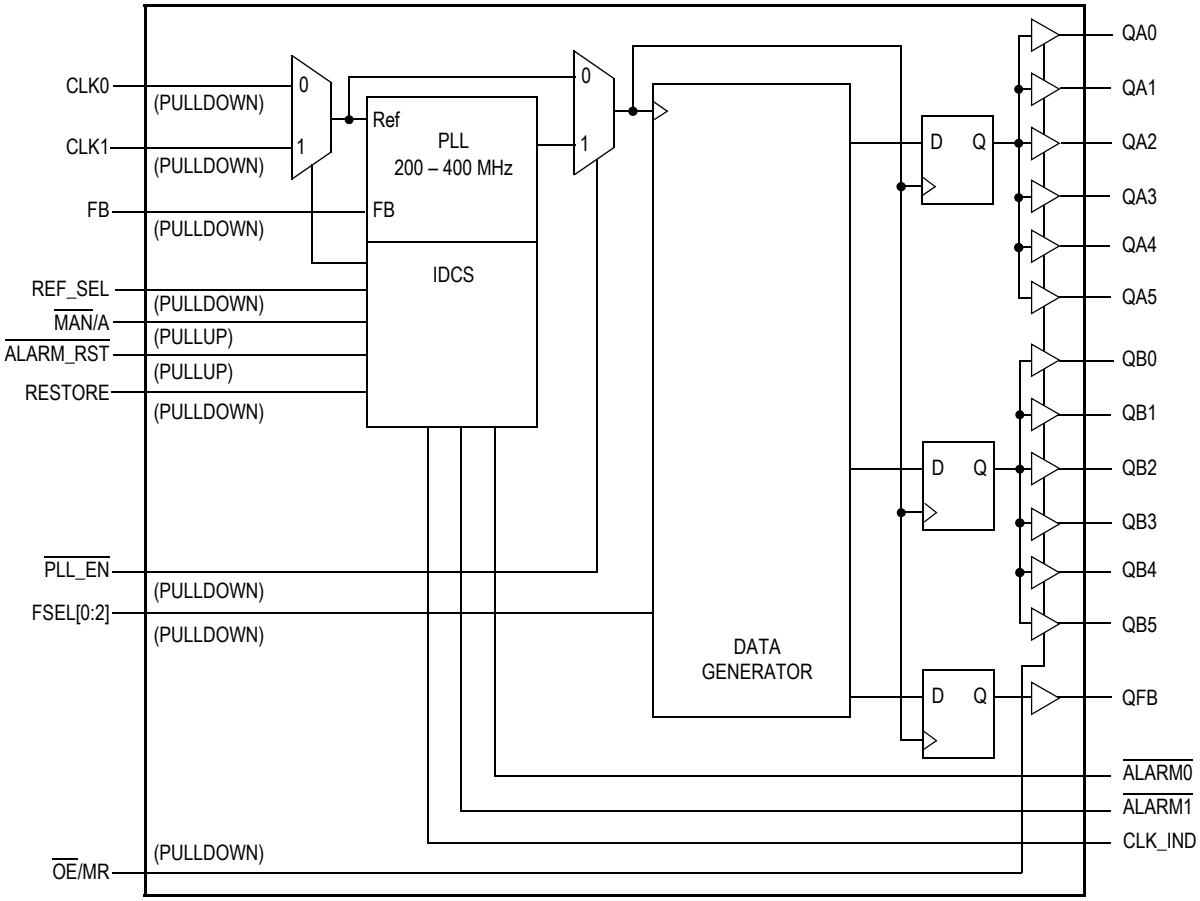


Figure 1. MPC9895 Logic Diagram

Table 1. Signal Configurations

Signal	I/O	Type	Function
CLK0, CLK1	Input	LVCMOS	PLL reference clock inputs
FB	Input	LVCMOS	PLL feedback signal input, connect directly to QFB output
REF_SEL	Input	LVCMOS	Selects the primary reference clock
MAN/A	Input	LVCMOS	Selects switch mode and alarm flag reset
ALARM_RST	Input	LVCMOS	Reset of alarm flags and selected reference clock indicator
RESTORE	Input	LVCMOS	Selects the automatic restore mode
PLL_EN	Input	LVCMOS	Selects PLL or static test mode
FSEL[0:2]	Input	LVCMOS	Clock frequency selection and configuration of clock divider modes
OE/MR	Input	LVCMOS	Output enable/disable, device reset
QA[0:5]	Output	LVCMOS	Bank A clock outputs
QB[0:5]	Output	LVCMOS	Bank B clock outputs
QFB	Output	LVCMOS	Clock feedback output. QFB must be connected to FB for correct operation
ALARM0	Output	LVCMOS	Indicates clock failure on CLK0
ALARM1	Output	LVCMOS	Indicates clock failure on CLK1
CLK_IND	Output	LVCMOS	Indicates currently selected input reference clock
GND	Supply	Ground	Negative power supply
V_{CC_PLL}	Supply	V_{CC}	Positive power supply for the PLL (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see <st-blue>APPLICATIONS INFORMATION for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
Inputs			
$\overline{\text{PLL\_EN}}$	0	PLL enabled. The input to output frequency relationship is according to Table 3 if the PLL is frequency locked.	PLL bypassed and IDCS disabled. The VCO output is replaced by the reference clock signal fref. The MPC9895 is in manual mode.
$\overline{\text{MAN}}$/A	1	Manual clock switch mode. **IDCS disabled**. Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled. Low-to-high transition: $\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$ and CLK_IND flags are reset: $\overline{\text{ALARM0}}$=H, $\overline{\text{ALARM1}}$=H and CLK_IND=REF_SEL.	Automatic clock switch mode. **IDCS enabled**. Clock failure detection and output flags ALARM0, ALARM1, CLK_IND are enabled. IDCS overrides REF_SEL on a clock failure. IDCS operation requires $\overline{\text{PLL\_EN}}$ = 0.
$\overline{\text{ALARM\_RST}}$	1	$\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$ and CLK_IND flags are reset: $\overline{\text{ALARM0}}$=H, $\overline{\text{ALARM1}}$=H and CLK_IND=REF_SEL. $\overline{\text{ALARM\_RST}}$ is an one-shot function.	$\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$ and CLK_IND active
RESTORE	0	RESTORE operation is disabled	The IDCS attempts to automatically restore the primary clock source defined by REF_SEL. This operation requires $\overline{\text{PLL\_EN}}$ = 0 and $\overline{\text{MAN}}$/A=1
REF_SEL	0	Selects CLK0 as the primary clock source	Selects CLK1 as the primary clock source
FSEL[0:2]	00	See Table 3	
$\overline{\text{OE}}$/MR	0	Outputs enabled (active)	Logic 1: Outputs disabled (high impedance state), reset of data generators and output dividers. The MPC9895 requires reset at power-up and after any loss of PLL lock. Loss of PLL lock may occur when the external feedback path is interrupted. The length of the reset pulse should be greater than two reference clock cycles (CLK0,1). $\overline{\text{OE}}$/MR does not affect the QFB output.
Outputs ($\overline{\text{ALARM0}}$, $\overline{\text{ALARM1}}$, CLK_IND are valid if PLL is locked)			
$\overline{\text{ALARM0}}$		CLKO failure	
$\overline{\text{ALARM1}}$		CLK1 failure	
CLK_IND		CLKO is the primary clock, CLK1 is the secondary clock	CLK1 is the primary clock, CLK0 is the secondary clock

Table 3. Clock Frequency Configuration

Name	FSEL0	FSEL1	FSEL2	f_{REF} range [MHz]	QAx and QBx		QFB	M	N
					Ratio	f_{QAX} [MHz]			
M16H	0	0	0	6.25–12.5	$f_{REF} \cdot 16$	100–200	f_{REF}	32	2
M8L	0	1	0	6.25–12.5	$f_{REF} \cdot 8$	50–100	f_{REF}	32	4
M32	1	0	0	3.125–6.25	$f_{REF} \cdot 32$	100–200	f_{REF}	64	2
M16L	1	1	0	3.125–6.25	$f_{REF} \cdot 16$	50–100	f_{REF}	64	4
M8H	0	0	1	12.5–25.0	$f_{REF} \cdot 8$	100–200	f_{REF}	16	2
M4	0	1	1	12.5–25.0	$f_{REF} \cdot 4$	50–100	f_{REF}	16	4
	1	0	1	n/a					
	1	1	1	n/a					

Table 4. 100 Ball MAPBGA Signal Alignment[1]

Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball	Signal	Ball
$\overline{\text{MAN}}$/A	A1	FB	C1	CLK1	E1	V_{CC_PLL}	G1	$\overline{\text{ALARM1}}$	J1
QA5	A2	GND	C2	V_{CC}	E2	GND	G2	V_{CC}	J2
QA4	A3	V_{CC}	C3	V_{CC}	E3	V_{CC}	G3	GND	J3
GND	A4	V_{CC}	C4	GND	E4	GND	G4	V_{CC}	J4
QA3	A5	V_{CC}	C5	GND	E5	GND	G5	V_{CC}	J5
QA2	A6	V_{CC}	C6	GND	E6	GND	G6	GND	J6
V_{CC}	A7	V_{CC}	C7	GND	E7	GND	G7	GND	J7
QA1	A8	V_{CC}	C8	VCC	E8	V_{CC}	G8	V_{CC}	J8
QA0	A9	V_{CC}	C9	GND	E9	GND	G9	V_{CC}	J9
GND	A10	REF_SEL	C10	FSEL0	E10	FSEL2	G10	$\overline{\text{OE}}$/MR	J10
QFB	B1	CLK0	D1	V_{CC_PLL}	F1	$\overline{\text{ALARM0}}$	H1	CLK_IND	K1
V_{CC}	B2	V_{CC}	D2	GND	F2	GND	H2	QB5	K2
GND	B3	V_{CC}	D3	V_{CC}	F3	V_{CC}	H3	QB4	K3
V_{CC}	B4	GND	D4	GND	F4	V_{CC}	H4	GND	K4
V_{CC}	B5	GND	D5	GND	F5	V_{CC}	H5	QB3	K5
GND	B6	GND	D6	GND	F6	V_{CC}	H6	QB2	K6
GND	B7	GND	D7	GND	F7	V_{CC}	H7	V_{CC}	K7
V_{CC}	B8	V_{CC}	D8	V_{CC}	F8	V_{CC}	H8	QB1	K8
V_{CC}	B9	GND	D9	GND	F9	V_{CC}	H9	QB0	K9
$\overline{\text{ALARM\_RST}}$	B10	$\overline{\text{PLL\_EN}}$	D10	FSEL1	F10	RESTORE	H10	GND	K10

1. See Figure 14. MAPBGA Pin Configurations (Bottom View).

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 6. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 7. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance		14–17		Ω	
I_{IN}	Input Current			±200	µA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		2	5	mA	V_{CC_PLL} balls
I_{CC}	Maximum Quiescent Supply Current			4	mA	All V_{CC} balls
V_{TT}	Output Termination Voltage		V_{CC} ÷ 2		V	

1. The MPC9895 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50W series terminated transmission lines.

Table 8. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40°C to +85°C)[1 2]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency					PLL locked
	FSEL= 000	6.25		12.5	MHz	
	FSEL= 010	6.26		12.5	MHz	
	FSEL= 100	3.125		6.25	MHz	
	FSEL= 110	3.125		6.25	MHz	
	FSEL= 001	12.5		25.0	MHz	
	FSEL= 011	12.5		25.0	MHZ	
f_{MAX}	Maximum Output Frequency					PLL locked
	FSEL= 000	100		200	MHz	
	FSEL= 010	50		100	MHz	
	FSEL= 100	100		200	MHz	
	FSEL= 110	50		100	MHz	
	FSEL= 001	100		200	MHz	
	FSEL= 011	50		100	MHz	
f_{refDC}	Reference Input Duty Cycle	40		60	%	
t_r, t_f	CLK0, 1 Input Rise/Fall Time			1.0	ns	0.8 to 2.0V
$t_{(\varnothing)}$	Propagation Delay (static phase offset, CLKx to FB)		±3		ns	PLL locked
Δ t	Rate of Period Change (phase slew rate) FSEL=x0x		150		ps/cycle	$\overline{MAN}$/A = 1
	FSEL=x1x		300			$\overline{MAN}$/A = 1
N_F	IDCS Switch Delay[3]	1			T	
N_R	IDCS Restore Delay[4]	64			T	
$t_{sk(O)}$	Output-to-Output Skew[5] (within bank)			50	ps	
	(bank-to-bank)			100	ps	
DC_O	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.55 to 2.4V
$t_{PLZ, HZ}$	Output Disable Time			10	ns	
$t_{PZL, LZ}$	Output Enable Time			10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle jitter			100	ps	
$t_{JIT(PER)}$	Period Jitter			TBD	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter		±2		ns	
BW	PLL Closed Loop Bandwidth[6] FSEL=0x		TBD		MHz	
	FSEL=1x		TBD		MHz	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

1. All AC characteristics are design targets and subject to change upon characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. Number of input clock cycles for clock failure detection. T = period of the feedback clock signal.
4. Number of consecutive, valid clock cycles of an input clock signal. T = period of the feedback clock signal.
5. See application section for part-to-part skew calculation.
6. –3dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Definitions

IDCS: Intelligent Dynamic Clock Switch. The IDCS monitors both primary and secondary clock signals. Upon a failure of the primary clock signal, the IDCS switches to a valid secondary clock signal and status flags are set.

Reference clock signal fref: The clock signal that is selected by the IDCS or REF_SEL as the input reference to the PLL.

Manual mode: The reference clock frequency is selected by REF_SEL.

Automatic mode: The reference clock frequency is selected by the internal IDCS logic.

Primary clock: The input clock signal selected by REF_SEL. The primary clock may or may not be the reference clock, depending on switch mode and IDCS status.

Secondary clock: The input clock signal not selected by REF_SEL

Selected clock: The CLK_IND flag indicates the reference clock signal: CLK_IND = 0 indicates CLK0 is the clock reference signal, CLK_IND =1 indicates CLK1 is the reference clock signal.

Clock failure: A valid clock signal that is stuck (high or low) for at least one input clock period (N_F>1). The primary clock and the secondary clock is monitored for failure. Valid clock signals must be within the AC and DC specification for the input reference clock. A loss of clock is detected if as well as the loss of both clocks. In the case of both clocks are lost, the MPC9895 will set the alarm flags and the VCO will run at its lowest frequency. The PLL will not be locked. The MPC9895 has to be reset by $\overline{OE}$/MR to recover from this situation, it is recommended to re-apply the startup sequence and to use the manual mode ($\overline{MAN}$/A=0) to select the primary clock.

The MPC9895 does not monitor and detect changes in the input frequency.

Automatic Mode and IDCS Commanded Clock Switch

$\overline{MAN}$/A = 1, IDCS enabled: Both primary and secondary clocks are monitored. The first clock failure is reported by its $\overline{ALARMx}$ status flag (clock failure is indicated by a logic low). The $\overline{ALARMx}$ status is flag latched and remains latched until reset by assertion of $\overline{ALARM\_RST}$ (if RESTORE=0) or the input clock is fixed (if RESTORE=1).

If the clock failure occurs on the primary clock, the IDCS attempts to switch to the secondary clock. The secondary clock signal needs to be valid for a successful switch. CLK_IND indicates the reference clock signal. Upon a successful switch, CLK_IND indicates the reference clock, which may now be different as that originally selected by REF_SEL.

Clock Restore Operation

If the RESTORE input is asserted (RESTORE=1, $\overline{MAN}$/A = 1) the IDCS attempts to restore the primary clock after a clock failure. After a successful IDCS-commanded clock switch, REF_SEL is not equal to CLK_IND. The IDCS continues to monitor the primary and secondary clock. If the primary clock becomes valid for at least 64 consecutive cycles (N_R>64), the IDCS attempts to switch back to the primary clock (restore the primary clock).

Upon a successful clock restore operation, the primary clock is the reference clock, CLK_IND will be equal to REF_SEL and the $\overline{ALARMx}$ flags are cleared.

If REF_SEL is equal to the CLK_IND flag (no clock failure occurred) the IDCS does not change the selected input clock. Deassertion of RESTORE disables the clock restore option and the clock selection must be reset manually.

Manual Mode

$\overline{MAN}$/A = 0, IDCS disabled: PLL functions normally and both clocks are monitored. The reference clock signal will always be the clock signal selected by REF_SEL and will be indicated by CLK_IND. The clock restore feature is disabled in manual mode.

Clock Output Transition

A clock switch, either in automatic or manual mode, follows the next negative edge of the newly selected reference clock signal. The feedback and newly selected reference clock edge will start to slew to alignment at the next positive edge of both signals. Output runt pulses are eliminated.

Reset

$\overline{ALARM\_RST}$ is asserted by a negative edge. It generates a one-shot reset pulse that clears both $\overline{ALARMx}$ latches and the CLK_IND latch. If both CLK0 and CLK1 are invalid or fail when $\overline{ALARM\_RST}$ is asserted, both $\overline{ALARMx}$ flags will be latched after one FB signal period and CLK_IND will be latched (L) indicating CLK0 is the reference signal. While neither $\overline{ALARMx}$ flag is latched ($\overline{ALARMx}$ = H), the CLK_IND can be freely changed with REF_SEL.

$\overline{OE}$/MR: Reset the data generator and output disable.

$\overline{MAN}$/A: The rising edge of $\overline{OE}$/MR resets $\overline{ALARMx}$ and CLK_IND as $\overline{ALARM\_RST}$ does.

Acquiring Frequency Lock (startup sequence)

1. On startup, $\overline{OE}$/MR must be asserted to reset the output dividers. The IDCS should be disabled ($\overline{MAN}$/A=0) and RESTORE should be logic low (disable restore option) during startup. REF_SEL selects the primary clock.
2. Release $\overline{OE}$/MR and the PLL will attempt to gain lock if the primary clock is present. PLL lock requires the specified lock time.
3. Enable the IDCS automatic mode ($\overline{MAN}$/A=1). The rising edge of the $\overline{MAN}$/A signal clears the alarm flags and CLK_IND. The IDCS will now report clock failures by asserting $\overline{ALARMx}$ flags.
4. Enable the restore option (RESTORE=1) if needed.

Power Supply Filtering

The MPC9895 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} (PLL) power supply impacts the device

characteristics, for instance I/O jitter. The MPC9895 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9895. Figure 2 illustrates a typical power supply filter scheme. The MPC9895 frequency and phase stability is most susceptible to noise with spectral content in the 100kHz to 20MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 3 mA (5 mA maximum), assuming that a minimum of 3.0V must be maintained on the VCC_PLL pin. The resistor R_F shown in Figure 2 must have a resistance of 9-10Ω to meet the voltage drop criteria.

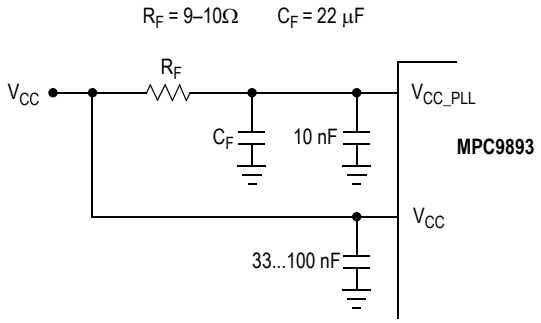


Figure 2. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 2, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9895 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC9895 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9895 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9895 clock driver is effectively doubled due to its capability to drive multiple lines.

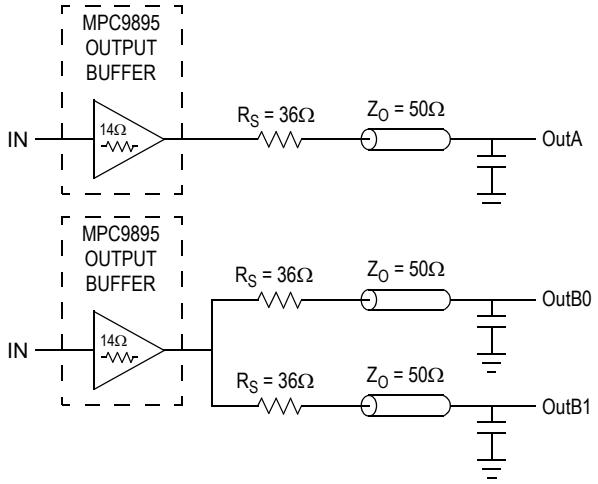


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9895 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9895. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus

the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S+R_0 +Z_0))$

$Z_0 = 50\Omega \parallel 50\Omega$

$R_S = 36\Omega \parallel 36\Omega$

$R_0 = 14\Omega$

$V_L = 3.0 (25 \div (18+17+25)$

$= 1.31V$

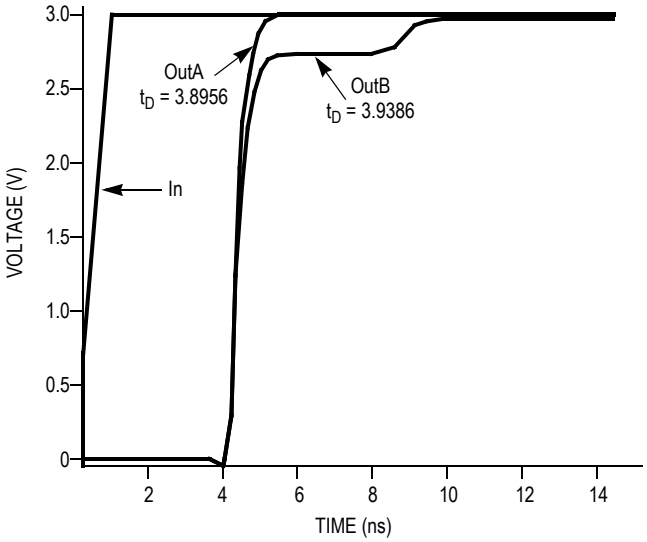
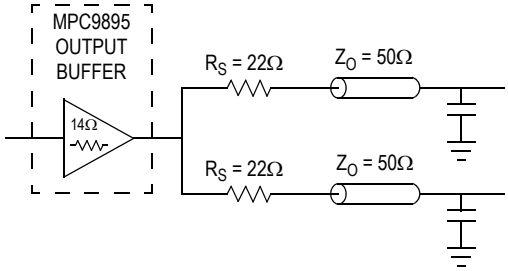


Figure 4. Single versus Dual Waveforms

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\Omega + 22\Omega \parallel 22\Omega = 50\Omega \parallel 50\Omega$

$25\Omega = 25\Omega$

Figure 5. Optimized Dual Line Termination

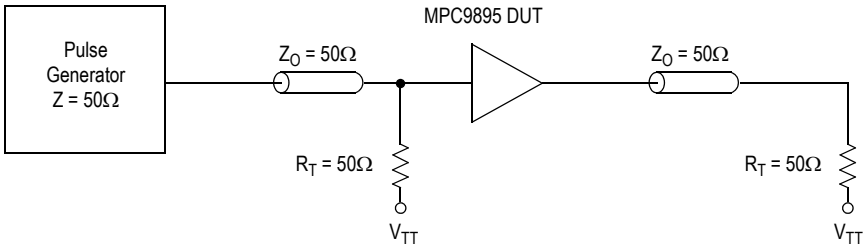
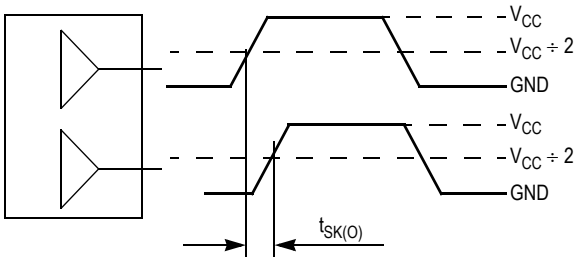


Figure 6. CLK0, CLK1 MPC9895 AC Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 7. Output-to-Output Skew $t_{SK(O)}$

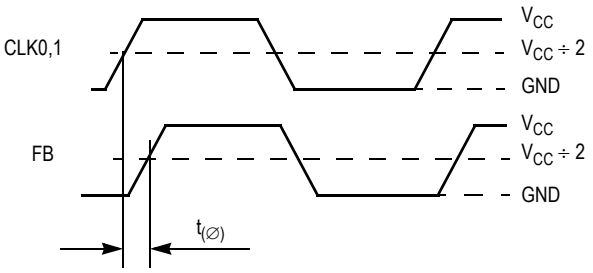
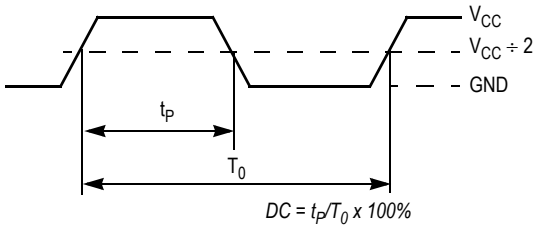
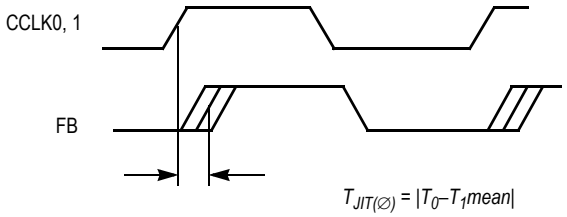


Figure 8. Propagation Delay ($t_{(\varnothing)}$, static phase offset) Test Reference



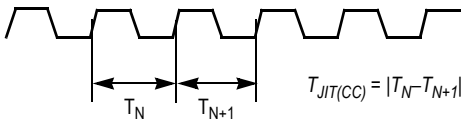
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 9. Output Duty Cycle (DC)



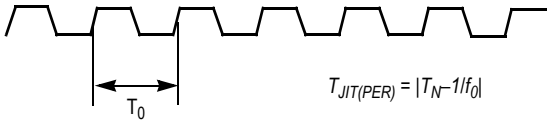
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 10. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 11. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 12. Period Jitter

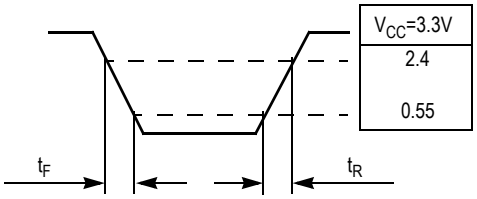


Figure 13. Output Transition Time Test Reference

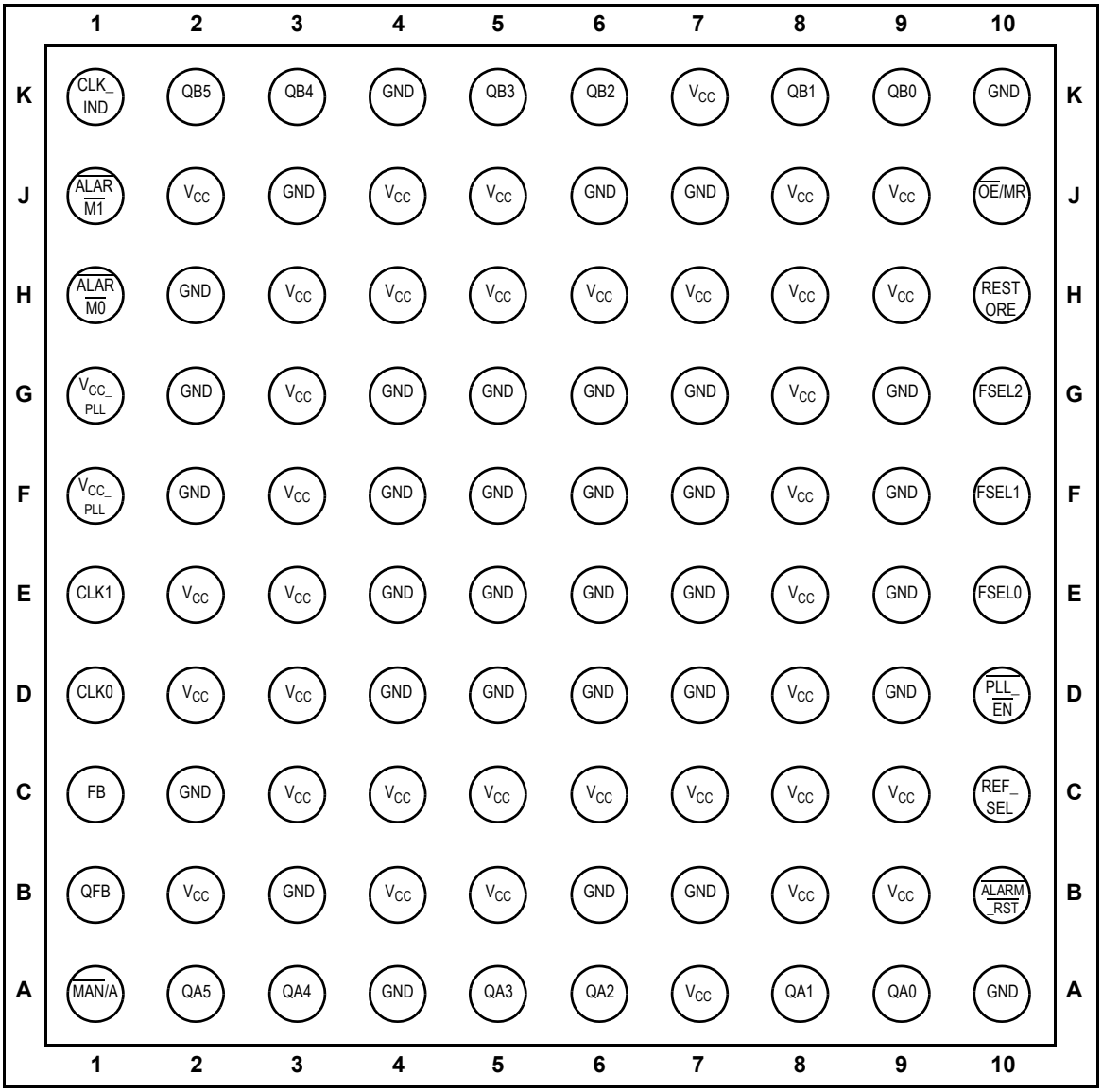


Figure 14. MAPBGA Pin Configurations (Bottom View)

Order number: MPC9993
Rev 2, 08/2004

Intelligent Dynamic Clock Switch (IDCS) PLL Clock Driver

MPC9993

INTELLIGENT DYNAMIC CLOCK SWITCH PLL CLOCK DRIVER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC9993 is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two differential LVPECL clock signals from which it generates 5 new differential LVPECL clock outputs. Two of the output pairs regenerate the input signals frequency and phase while the other three pairs generate 2x, phase aligned clock outputs.

Features

- Fully Integrated PLL
- Intelligent Dynamic Clock Switch
- LVPECL Clock Outputs
- LVCMOS Control I/O
- 3.3V Operation
- 32-Lead LQFP Packaging
- 32-Lead Pb-Free Package Available

Functional Description

The MPC9993 Intelligent Dynamic Clock Switch (IDCS) circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP_BAD for that CLK will be latched (H). If that CLK is the primary clock, the IDCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated. (See Application Information section).

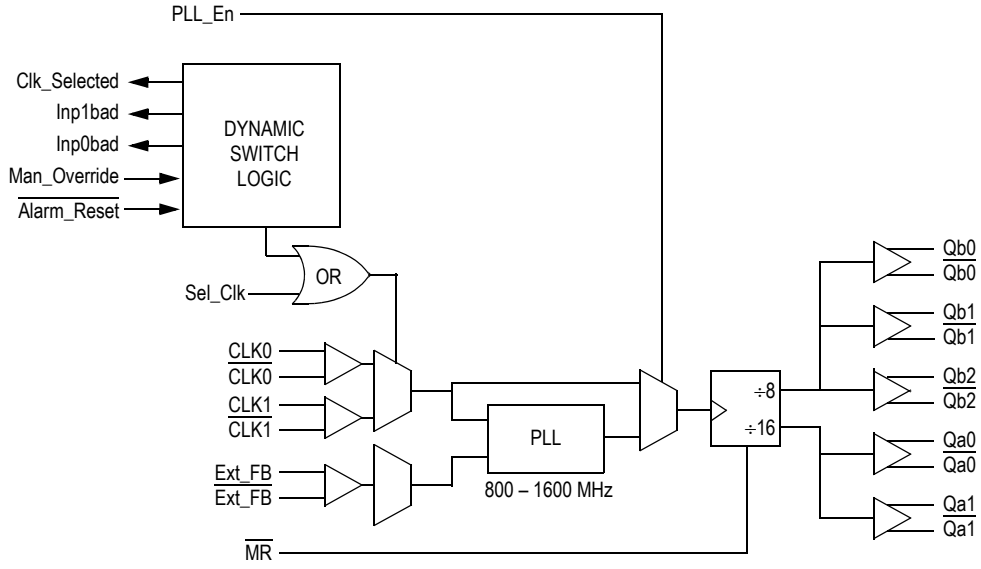


Figure 1. Block Diagram

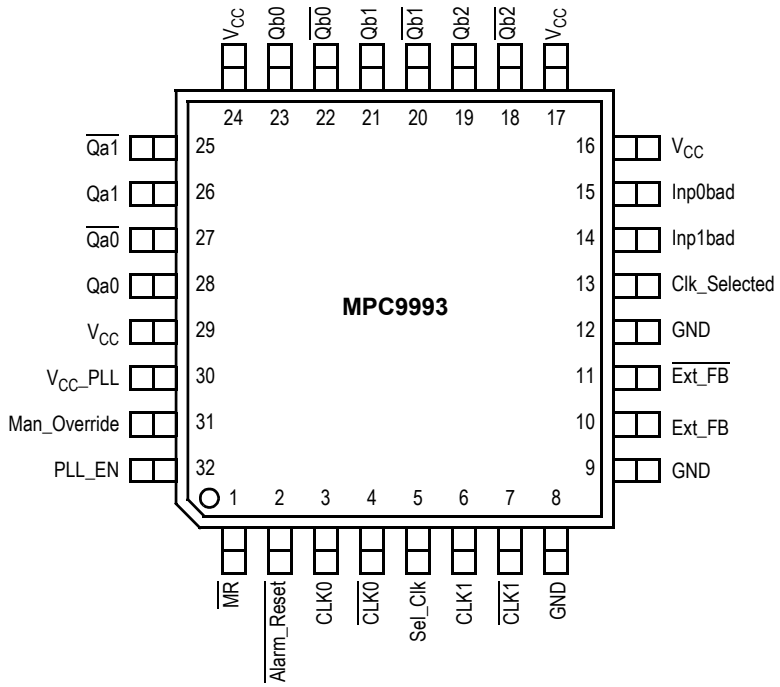


Figure 2. 32-Lead Pinout (Top View)

Table 1. Pin Descriptions

Pin Name	I/O	Pin Definition
CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	LVPECL Input LVPECL Input	Differential PLL clock reference (CLK0 pulldown, $\overline{\text{CLK0}}$ pullup) Differential PLL clock reference (CLK1 pulldown, $\overline{\text{CLK1}}$ pullup)
Ext_FB, $\overline{\text{Ext\_FB}}$	LVPECL Input	Differential PLL feedback clock (Ext_FB pulldown, $\overline{\text{Ext\_FB}}$ pullup)
Qa0:1, $\overline{\text{Qa0:1}}$	LVPECL Output	Differential 1x output pairs
Qb0:2, $\overline{\text{Qb0:2}}$	LVPECL Output	Differential 2x output pairs
Inp0bad	LVCMOS Output	Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Inp1bad	LVCMOS Output	Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Clk_Selected	LVCMOS Output	‘0' if clock 0 is selected, ‘1' if clock 1 is selected
Alarm_Reset	LVCMOS Input	‘0' will reset the input bad flags and align Clk_Selected with Sel_Clk. The input is “one-shotted” (50kΩ pullup)
Sel_Clk	LVCMOS Input	‘0' selects CLK0, ‘1' selects CLK1 (50kΩ pulldown)
Manual_Override	LVCMOS Input	‘1' disables internal clock switch circuitry (50kΩ pulldown)
PLL_En	LVCMOS Input	‘0' bypasses selected input reference around the phase-locked loop (50kΩ pullup)
$\overline{\text{MR}}$	LVCMOS Input	‘0' resets the internal dividers forcing Q outputs LOW. Asynchronous to the clock (50kΩ pullup)
V_{CCA}	Power Supply	PLL power supply
V_{CC}	Power Supply	Digital power supply
GNDA	Power Supply	PLL ground
GND	Power Supply	Digital ground

Table 2. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine model)	175			V	
HBM	ESD Protection (Human body model)	1500			V	
CDM	ESD Protection (Charged device model	1000			V	
LU	Latch-up Immunity	100			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T_J	Operating Junction Temperature[1] (continuous operation) MTBF = 9.1 years			110	°C	

1. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC9993 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC9993 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 4. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = – 40° to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs ($\overline{MR}$, PLL_En, Sel_Clk, Man_Override, $\overline{Alarm\_Reset}$)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IN}	Input Current[1]			±100	μA	V_{IN} = V_{CC} or GND
LVCMOS control outputs (Clk_selected, Inp0bad, Inp1bad)						
V_{OH}	Output High Voltage	2.0			V	I_{OH} = –24 mA
V_{OL}	Output Low Voltage			0.55	V	I_{OL} = 24 mA
LVPECL clock inputs (CLK0, CLK1, Ext_FB)[2]						
V_{PP}	DC Differential Input Voltage[3]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[4]	V_{CC} –1.8		V_{CC} –0.3	V	Differential operation
I_{IN}	Input Current[1]			±100	μA	V_{IN} = V_{CC} or GND
LVPECL clock outputs (QA[1:0], QB[2:0])						
V_{OH}	Output High Voltage	V_{CC} –1.20	V_{CC} –0.95	V_{CC} –0.70	V	Termination 50Ω to V_{TT}
V_{OL}	Output Low Voltage	V_{CC} –1.90	V_{CC} –1.75	V_{CC} –1.45	V	Termination 50Ω to V_{TT}
Supply Current						
I_{GND}	Maximum Power Supply Current			180	mA	GND Pins
I_{CC_PLL}	Maximum PLL Supply Current			15	mA	V_{CC_PLL} Pin

1. Inputs have internal pull-up/pull-down resistors affecting the input current.
2. Clock inputs driven by differential LVPECL compatible signals.
3. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics.
4. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 5. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40°C to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency	÷16 feedback	50		100	MHz	PLL locked
f_{VCO}	VCO Frequency Range[2]	÷16 feedback	800		1600	MHz	
f_{MAX}	Output Frequency	QA[1:0] QB[2:0]	50 100		100 200	MHz MHz	PLL locked
f_{refDC}	Reference Input Duty Cycle		25		75	%	
$t_{(\varnothing)}$	Propagation Delay	SPO, static phase offset[3] CLK0, CLK1 to any Q	-2.0 0.9		+2.0 1.8	ns ns	PLL_EN=1 PLL_EN=0
V_{PP}	Differential Input Voltage[4]	(peak-to-peak)	0.25		1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[5]		V_{CC}-1.7		V_{CC}-0.3	V	
$t_{sk(O)}$	Output-to-Output Skew	within QA[2:0] or QB[1:0] within device			50 80	ps ps	
$\Delta_{per/cycle}$	Rate of Change of Period	QA[1:0][6] QB[2:0][6] QA[1:0][7] QB[2:0][7]		20 10 200 100	50 25 400 200	ps ps ps ps	
DC	Output Duty Cycle		45	50	55	%	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	RMS (1 σ)			47	ps	
t_{LOCK}	Maximum PLL Lock Time				10	ms	
t_r, t_f	Output Rise/Fall Time		0.05		0.70	ns	20% to 80%

1. AC characteristics apply for parallel output termination of 50Ω to V_{CC} – 2V.
2. The input reference frequency must match the VCO lock range divided by the feedback divider ratio (FB): $f_{ref} = f_{VCO} \div FB$.
3. CLK0, CLK1 to Ext_FB.
4. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including SPO and device-to-device skew. Applicable to CLK0, CLK1 and Ext_FB.
5. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the SPO, device and part-to-part skew. Applicable to CLK0, CLK1 and Ext_FB.
6. Specification holds for a clock switch between two input signals (CLK0, CLK1) no greater than 400 ps out of phase. Delta period change per cycle is averaged over the clock switch excursion.
7. Specification holds for a clock switch between two input signals (CLK0, CLK1) at any phase difference (±180°). Delta period change per cycle is averaged over the clock switch excursion.

APPLICATIONS INFORMATION

The MPC9993 is a dual clock PLL with on-chip Intelligent Dynamic Clock Switch (IDCS) circuitry.

Definitions

primary clock: The input CLK selected by Sel_Clk.

secondary clock: The input CLK NOT selected by Sel_Clk.

PLL reference signal: The CLK selected as the PLL reference signal by Sel_Clk or IDCS. (IDCS can override Sel_Clk).

Status Functions

Clk_Selected: Clk_Selected (L) indicates CLK0 is selected as the PLL reference signal. Clk_Selected (H) indicates CLK1 is selected as the PLL reference signal.

INP_BAD: Latched (H) when it's CLK is stuck (H) or (L) for at least one Ext_FB period (Pos to Pos or Neg to Neg). Cleared (L) on assertion of Alarm_Reset.

Control Functions

Sel_Clk: Sel_Clk (L) selects CLK0 as the primary clock. Sel_Clk (H) selects CLK1 as the primary clock.

Alarm_Reset: Asserted by a negative edge. Generates a one-shot reset pulse that clears INPUT_BAD latches and Clk_Selected latch.

PLL_En: While (L), the PLL reference signal is substituted for the VCO output.

MR: While (L), internal dividers are held in reset which holds all Q outputs LOW.

Man Override (H)

(IDCS is disabled, PLL functions normally). PLL reference signal (as indicated by Clk_Selected) will always be the CLK selected by Sel_Clk. The status function INP_BAD is active in Man Override (H) and (L).

Man Override (L)

(IDCS is enabled, PLL functions enhanced). The first CLK to fail will latch it's INP_BAD (H) status flag and select the other input as the Clk_Selected for the PLL reference clock. Once latched, the Clk_Selected and INP_BAD remain latched until assertion of Alarm_Reset which clears all latches (INP_BADs are cleared and Clk_Selected = Sel_Clk). NOTE: If both CLKs are bad when Alarm_Reset is asserted, both INP_BADs will be latched (H) after one Ext_FB period and Clk_Selected will be latched (L) indicating CLK0 is the PLL reference signal. While neither INP_BAD is latched (H), the Clk_Selected can be freely changed with Sel_Clk. Whenever a CLK switch occurs, (manually or by IDCS), following the next negative edge of the newly selected PLL reference signal, the next positive edge pair of Ext_FB and the newly selected PLL reference signal will slew to alignment.

To calculate the overall uncertainty between the input CLKs and the outputs from multiple MPC9993's, the following procedure should be used. Assuming that the input CLKs to all MPC9993's are exactly in phase, the total uncertainty will be the sum of the static phase offset, max I/O jitter, and output to output skew.

During a dynamic switch, the output phase between two devices may be increased for a short period of time. If the two input CLKs are 400ps out of phase, a dynamic switch of an MPC9993 will result in an instantaneous phase change of 400ps to the PLL reference signal without a corresponding change in the output phase (due to the limited response of the PLL). As a result, the I/O phase of a device, undergoing this switch, will initially be 400ps and diminish as the PLL slews to its new phase alignment. This transient timing issue should be considered when analyzing the overall skew budget of a system.

Hot insertion and withdrawal

In PECL applications, a powered up driver will experience a low impedance path through an MPC9993 input to its powered down VCC pins. In this case, a 100 ohm series resistance should be used in front of the input pins to limit the driver current. The resistor will have minimal impact on the rise and fall times of the input signals.

Acquiring Frequency Lock

1. While the MPC9993 is receiving a valid CLK signal, assert Man_Override HIGH.
2. The PLL will phase and frequency lock within the specified lock time.
3. Apply a HIGH to LOW transition to Alarm_Reset to reset Input Bad flags.
4. De-assert Man_Override LOW to enable Intelligent Dynamic Clock Switch mode.

Intelligent Dynamic Clock Switch (IDCS) PLL Clock Driver

MPC99J93

INTELLIGENT DYNAMIC CLOCK SWITCH PLL CLOCK DRIVER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC99J93 is a PLL clock driver designed specifically for redundant clock tree designs. The device receives two differential LVPECL clock signals from which it generates 5 new differential LVPECL clock outputs. Two of the output pairs regenerate the input signals frequency and phase while the other three pairs generate 2x, phase aligned clock outputs.

Features

- Fully Integrated PLL
- Intelligent Dynamic Clock Switch
- LVPECL Clock Outputs
- LVCMOS Control I/O
- 3.3V Operation
- 32-Lead LQFP Packaging
- 32-Lead Pb-Free Package Available

Functional Description

The MPC99J93 Intelligent Dynamic Clock Switch (IDCS) circuit continuously monitors both input CLK signals. Upon detection of a failure (CLK stuck HIGH or LOW for at least 1 period), the INP_BAD for that CLK will be latched (H). If that CLK is the primary clock, the IDCS will switch to the good secondary clock and phase/frequency alignment will occur with minimal output phase disturbance. The typical phase bump caused by a failed clock is eliminated. (See Application Information section).

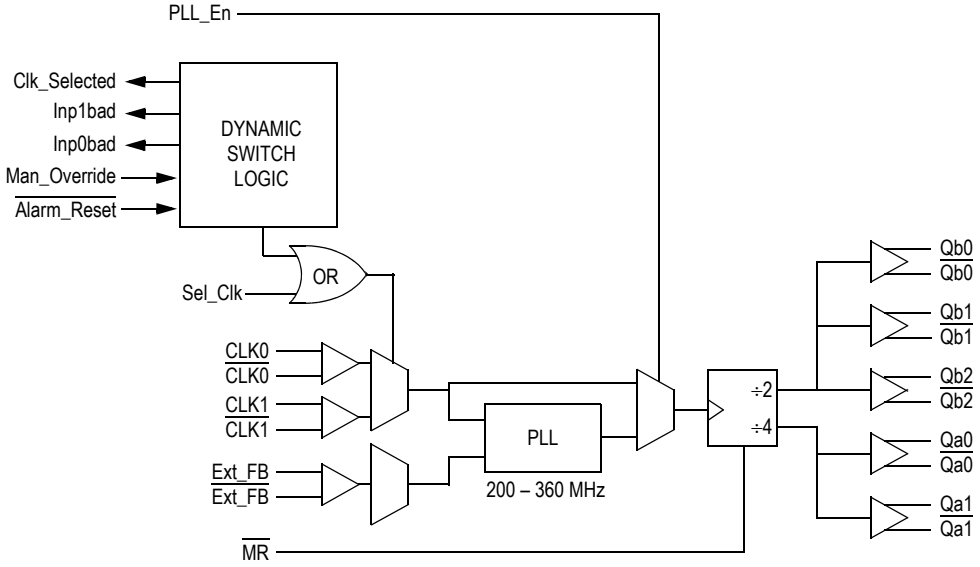


Figure 1. Block Diagram

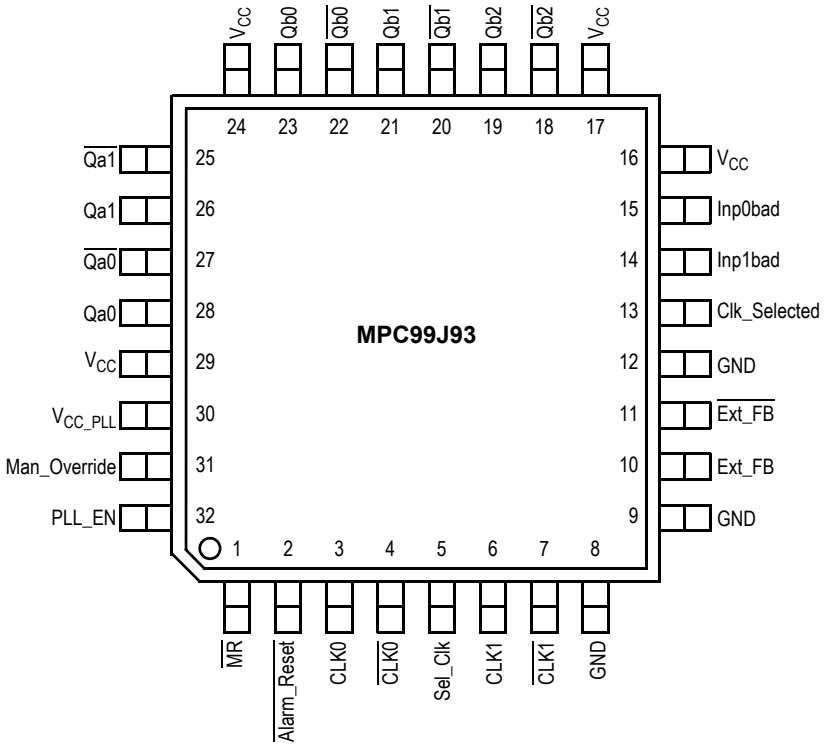


Figure 2. Pinout: 32-Lead Pinout (Top View)

Table 1. Pin Descriptions

Pin Name	I/O	Pin Definition
CLK0, $\overline{\text{CLK0}}$ CLK1, $\overline{\text{CLK1}}$	LVPECL Input LVPECL Input	Differential PLL clock reference (CLK0 pulldown, $\overline{\text{CLK0}}$ pullup) Differential PLL clock reference (CLK1 pulldown, $\overline{\text{CLK1}}$ pullup)
Ext_FB, $\overline{\text{Ext\_FB}}$	LVPECL Input	Differential PLL feedback clock (Ext_FB pulldown, $\overline{\text{Ext\_FB}}$ pullup)
Qa0:1, $\overline{\text{Qa0:1}}$	LVPECL Output	Differential 1x output pairs. Connect one QAx pair to Ext_FB.
Qb0:2, $\overline{\text{Qb0:2}}$	LVPECL Output	Differential 2x output pairs
Inp0bad	LVCMOS Output	Indicates detection of a bad input reference clock 0 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Inp1bad	LVCMOS Output	Indicates detection of a bad input reference clock 1 with respect to the feedback signal. The output is active HIGH and will remain HIGH until the alarm reset is asserted
Clk_Selected	LVCMOS Output	‘0' if clock 0 is selected, ‘1' if clock 1 is selected
$\overline{\text{Alarm\_Reset}}$	LVCMOS Input	‘0' will reset the input bad flags and align Clk_Selected with Sel_Clk. The input is “one-shotted” (50kΩ pullup)
Sel_Clk	LVCMOS Input	‘0' selects CLK0, ‘1' selects CLK1 (50kΩ pulldown)
Manual_Override	LVCMOS Input	‘1' disables internal clock switch circuitry (50kΩ pulldown)
PLL_En	LVCMOS Input	‘0' bypasses selected input reference around the phase-locked loop (50kΩ pullup)
$\overline{\text{MR}}$	LVCMOS Input	‘0' resets the internal dividers forcing Q outputs LOW. Asynchronous to the clock (50kΩ pullup)
V_{CCA}	Power Supply	PLL power supply
V_{CC}	Power Supply	Digital power supply
GNDA	Power Supply	PLL ground
GND	Power Supply	Digital ground

Table 2. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine model)	175			V	
HBM	ESD Protection (Human body model)	1500			V	
CDM	ESD Protection (Charged device model	1000			V	
LU	Latch-up Immunity	100			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T_J	Operating Junction Temperature[1] (continuous operation) MTBF = 9.1 years			110	°C	

1. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MPC99J93 to be used in applications requiring industrial temperature range. It is recommended that users of the MPC99J93 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 4. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40° to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs ($\overline{MR}$, PLL_En, Sel_Clk, Man_Override, $\overline{Alarm\_Reset}$)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}	Input Low Voltage			0.8	V	
I_{IN}	Input Current[1]			±100	μA	V_{IN}=V_{CC} or GND
LVCMOS Control Outputs (Clk_selected, Inp0bad, Inp1bad)						
V_{OH}	Output High Voltage	2.0			V	I_{OH}=-24 mA
V_{OL}	Output Low Voltage			0.55	V	I_{OL}= 24 mA
LVPECL Clock Inputs (CLK0, CLK1, Ext_FB)[2]						
V_{PP}	DC Differential Input Voltage[3]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[4]	V_{CC}–1.8		V_{CC}–0.3	V	Differential operation
I_{IN}	Input Current[1]			±100	μA	V_{IN}=V_{CC} or GND
LVPECL Clock Outputs (QA[1:0], QB[2:0])						
V_{OH}	Output High Voltage	V_{CC}–1.20	V_{CC}–0.95	V_{CC}–0.70	V	Termination 50Ω to V_{TT}
V_{OL}	Output Low Voltage	V_{CC}–1.90	V_{CC}–1.75	V_{CC}–1.45	V	Termination 50Ω to V_{TT}
Supply Current						
I_{GND}	Maximum Power Supply Current			180	mA	GND pins
I_{CC_PLL}	Maximum PLL Supply Current			15	mA	V_{CC_PLL} pin

1. Inputs have internal pull-up/pull-down resistors affecting the input current.
2. Clock inputs driven by differential LVPECL compatible signals.
3. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics.
4. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 5. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40°C to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Reference Frequency	÷4 feedback	50		90	MHz	PLL locked
f_{VCO}	VCO Frequency Range[2]	÷4 feedback	200		360	MHz	
f_{MAX}	Output Frequency	QA[1:0] QB[2:0]	50 100		90 180	MHz MHz	PLL locked
f_{refDC}	Reference Input Duty Cycle		25		75	%	
$t_{(\varnothing)}$	Propagation Delay	SPO, static phase offset[3] CLK0, CLK1 to any Q	–0.15 0.9		+0.17 1.8	ns ns	PLL_EN=1 PLL_EN=0
V_{PP}	Differential Input Voltage[4]	(peak-to-peak)	0.25		1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[5]		V_{CC}–1.7		V_{CC}–0.3	V	
$t_{sk(O)}$	Output-to-Output Skew	within QA[2:0] or QB[1:0] within device			50 80	ps ps	
$\Delta_{per/cycle}$	Rate of Change of Period	QA[1:0][6] QB[2:0][6] QA[1:0][7] QB[2:0][7]		20 10 200 100	50 25 400 200	ps ps ps ps	
DC	Output Duty Cycle		45	50	55	%	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	RMS (1 σ)		25		ps	
t_{LOCK}	Maximum PLL Lock Time				10	ms	
t_r, t_f	Output Rise/Fall Time		0.05		0.70	ns	20% to 80%

1. AC characteristics apply for parallel output termination of 50Ω to V_{CC} – 2V.
2. The input reference frequency must match the VCO lock range divided by the feedback divider ratio (FB): $f_{ref} = f_{VCO} \div FB$.
3. CLK0, CLK1 to Ext_FB.
4. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including SPO and device-to-device skew. Applicable to CLK0, CLK1 and Ext_FB.
5. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the SPO, device and part-to-part skew. Applicable to CLK0, CLK1 and Ext_FB.
6. Specification holds for a clock switch between two input signals (CLK0, CLK1) no greater than 400 ps out of phase. Delta period change per cycle is averaged over the clock switch excursion.
7. Specification holds for a clock switch between two input signals (CLK0, CLK1) at any phase difference (±180°). Delta period change per cycle is averaged over the clock switch excursion.

APPLICATIONS INFORMATION

The MPC99J93 is a dual clock PLL with on-chip Intelligent Dynamic Clock Switch (IDCS) circuitry.

Definitions

primary clock: The input CLK selected by Sel_Clk.
secondary clock: The input CLK NOT selected by Sel_Clk.
PLL reference signal: The CLK selected as the PLL reference signal by Sel_Clk or IDCS. (IDCS can override Sel_Clk).

Status Functions

Clk_Selected: Clk_Selected (L) indicates CLK0 is selected as the PLL reference signal. Clk_Selected (H) indicates CLK1 is selected as the PLL reference signal.
INP_BAD: Latched (H) when it's CLK is stuck (H) or (L) for at least one Ext_FB period (Pos to Pos or Neg to Neg). Cleared (L) on assertion of Alarm_Reset.

Control Functions

Sel_Clk: Sel_Clk (L) selects CLK0 as the primary clock. Sel_Clk (H) selects CLK1 as the primary clock.
Alarm_Reset: Asserted by a negative edge. Generates a one-shot reset pulse that clears INPUT_BAD latches and Clk_Selected latch.
PLL_En: While (L), the PLL reference signal is substituted for the VCO output.
MR: While (L), internal dividers are held in reset which holds all Q outputs LOW.

Man Override (H)

(IDCS is disabled, PLL functions normally). PLL reference signal (as indicated by Clk_Selected) will always be the CLK selected by Sel_Clk. The status function INP_BAD is active in Man Override (H) and (L).

Man Override (L)

(IDCS is enabled, PLL functions enhanced). The first CLK to fail will latch it's INP_BAD (H) status flag and select the other input as the Clk_Selected for the PLL reference clock. Once latched, the Clk_Selected and INP_BAD remain latched until assertion of Alarm_Reset which clears all latches (INP_BADs are cleared and Clk_Selected = Sel_Clk). NOTE: If both CLKs are bad when Alarm_Reset is asserted, both INP_BADs will be latched (H) after one Ext_FB period and Clk_Selected will be latched (L) indicating CLK0 is the PLL reference signal. While neither INP_BAD is latched (H), the Clk_Selected can be freely changed with Sel_Clk. Whenever a CLK switch occurs, (manually or by IDCS), following the next negative edge of the newly selected PLL reference signal, the next positive edge pair of Ext_FB and the newly selected PLL reference signal will slew to alignment.

To calculate the overall uncertainty between the input CLKs and the outputs from multiple MPC99J93's, the following procedure should be used. Assuming that the input CLKs to all MPC9993's are exactly in phase, the total uncertainty will be the sum of the static phase offset, max I/O jitter, and output to output skew.

During a dynamic switch, the output phase between two devices may be increased for a short period of time. If the two input CLKs are 400ps out of phase, a dynamic switch of an MPC99J93 will result in an instantaneous phase change of 400ps to the PLL reference signal without a corresponding change in the output phase (due to the limited response of the PLL). As a result, the I/O phase of a device, undergoing this switch, will initially be 400ps and diminish as the PLL slews to its new phase alignment. This transient timing issue should be considered when analyzing the overall skew budget of a system.

Hot insertion and withdrawal

In PECL applications, a powered up driver will experience a low impedance path through an MPC99J93 input to its powered down V_{CC} pins. In this case, a 100 ohm series resistance should be used in front of the input pins to limit the driver current. The resistor will have minimal impact on the rise and fall times of the input signals.

Acquiring Frequency Lock

1. While the MPC99J93 is receiving a valid CLK signal, assert Man_Override HIGH.
2. The PLL will phase and frequency lock within the specified lock time.
3. Apply a HIGH to LOW transition to Alarm_Reset to reset Input Bad flags.
4. De-assert Man_Override LOW to enable Intelligent Dynamic Clock Switch mode.

Chapter Five
Clock Synthesizer Data Sheets

Clock Synthesizer Device Index

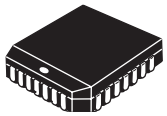
Order number: MC12429
Rev 7, 06/2001

High Frequency Clock Synthesizer

MC12429

HIGH FREQUENCY PLL CLOCK SYNTHESIZER

The MC12429 is a general purpose synthesized clock source. Its internal VCO will operate over a range of frequencies from 200 to 400MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4, or 8. With the output configured to divide the VCO frequency by 1, and with a 16.000MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1MHz steps. The PLL loop filter is fully integrated so that no external components are required. The output frequency is configured using a parallel or serial interface.



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776-022

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

Features

- 25 to 400MHz Differential PECL Outputs
- ±25 ps Peak-to-Peak Output Jitter
- Fully Integrated Phase-Locked Loop
- Minimal Frequency Over-Shoot
- Synthesized Architecture
- Serial 3-Wire Interface
- Parallel Interface for Power-Up
- Quartz Crystal Interface
- 28-Lead PLCC and 32-Lead LQFP Packages
- Operates from 3.3V or 5.0V Power Supply

Functional Description

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 16 before being sent to the phase detector. With a 16MHz crystal, this provides a reference frequency of 1MHz. Although this data sheet illustrates functionality only for a 16MHz crystal, any crystal in the 10–25MHz range can be used.

The VCO within the PLL operates over a range of 200 to 400MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

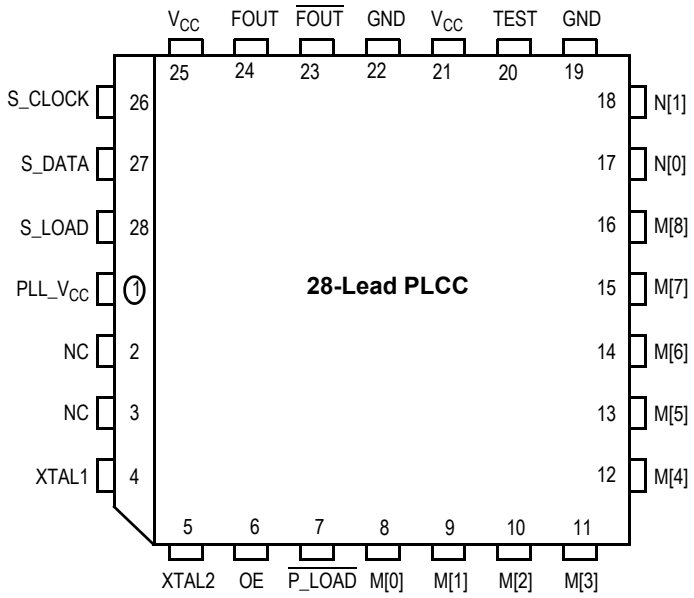
The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider (N divider) is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50 percent duty cycle.

The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated in 50Ω to V_{CC} – 2.0V. The positive reference for the output driver and the internal logic is separated from the power supply for the phase-locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. On the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.



N[1:0]	Output Division
0 0	1
0 1	2
1 0	4
1 1	8

Figure 1. 28-Lead (Top View)

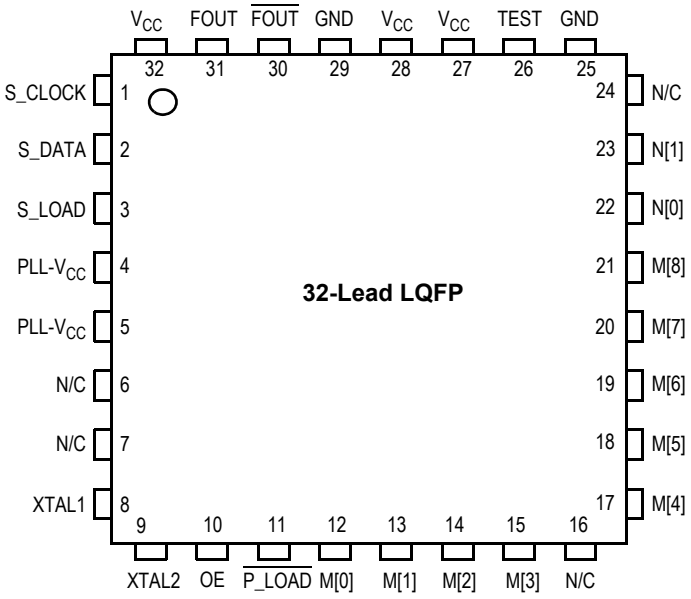


Figure 2. 32-Lead Pinout (Top View)

Table 1. Pin Descriptions

Pin	Function
Inputs	
XTAL1, XTAL2	These pins form an oscillator when connected to an external series-resonant crystal.
S_LOAD (Int. Pulldown)	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.
S_DATA (Int. Pulldown)	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK (Int. Pulldown)	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
$\overline{\text{P\_LOAD}}$ (Int. Pullup)	This pin loads the configuration latches with the contents of the parallel inputs.The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation. $\overline{\text{P\_LOAD}}$ is state sensitive.
M[8:0] (Int. Pullup)	These pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$. M[8] is the MSB, M[0] is the LSB.
N[1:0] (Int. Pullup)	These pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$.
OE (Int. Pullup)	Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation on the F_{OUT} output.
Outputs	
FOUT, $\overline{\text{FOUT}}$	These differential positive-referenced ECL signals (PECL) are the output of the synthesizer.
TEST	The function of this output is determined by the serial configuration bits T[2:0].
Power	
V_{CC}	This is the positive supply for the internal logic and the output buffer of the chip, and is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}). Current drain through $V_{CC} \approx$ 85mA.
PLL_V_{CC}	This is the positive supply for the PLL, and should be as noise-free as possible for low-jitter operation. This supply is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}). Current drain through PLL_$V_{CC} \approx$ 15mA.
GND	These pins are the negative supply for the chip and are normally all connected to ground.

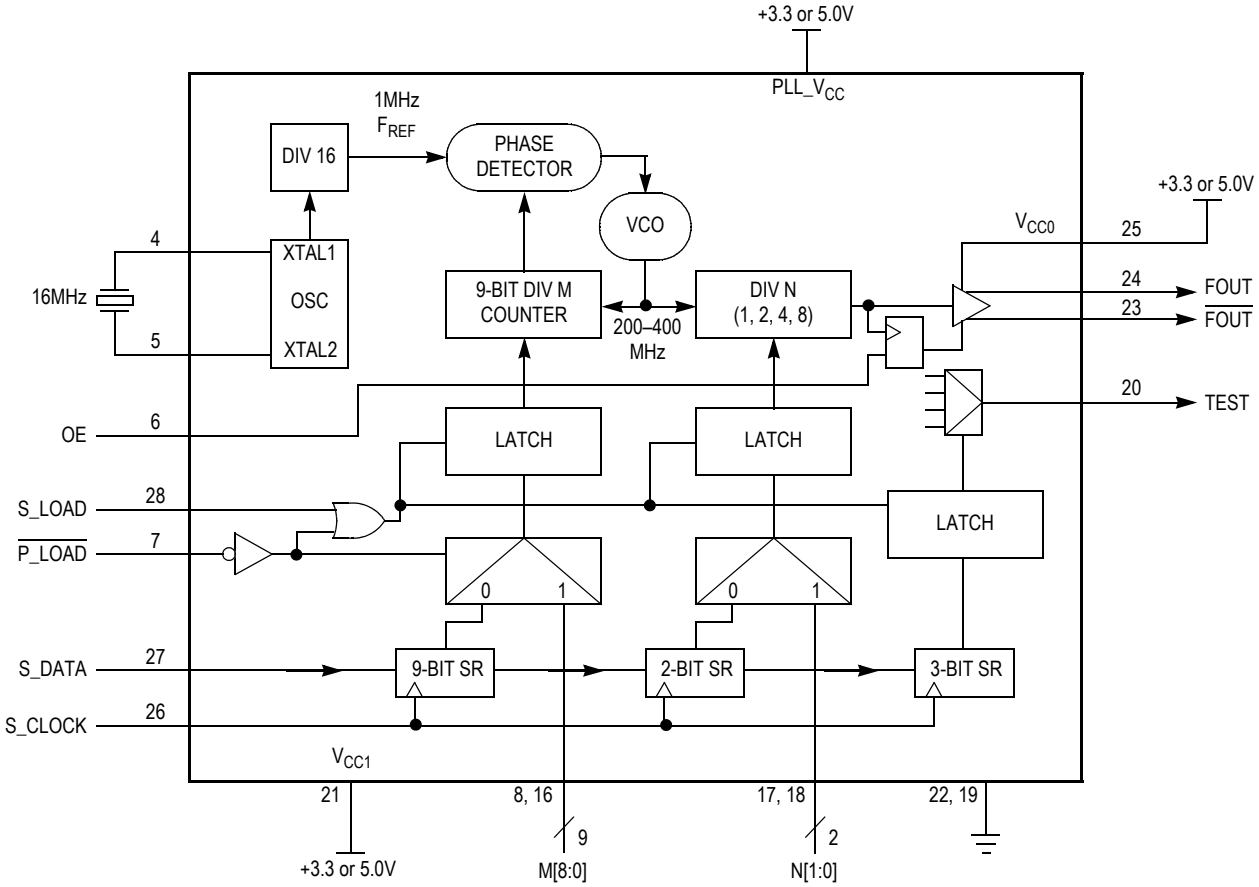


Figure 3. MC12429 Block Diagram (28-Lead PLCC Pinout)

PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = (F_{XTAL} \div 16) \times M \div N \quad (1)$$

Where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$ for a 16MHz input reference.

Assuming that a 16MHz reference frequency is used the above equation reduces to:

$$FOUT = M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

Table 2. Output Frequency Range

N	FOUT	Output Frequency Range
1	M	200 – 400 MHz
2	M / 2	100 – 200 MHz
4	M / 4	50 – 100 MHz
8	M / 8	25 – 50 MHz

From these ranges the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example if an output frequency of 131MHz was desired the following steps would be taken to identify the appropriate M and N values. 131MHz falls within the frequency range set by an N value of 2 so N [1:0] = 01. For N = 2 FOUT = M ÷ 2 and M = 2 x FOUT. Therefore M = 131 x 2 = 262, so M[8:0] = 100000110. Following this same procedure a user can generate any whole frequency desired between 25 and 400MHz. Note that for N > 2 fractional values of FOUT can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to FXTAL ÷ 16 ÷ N.

For input reference frequencies other than 16MHz the set of appropriate equations can be deduced from equation 1. For computer applications another useful frequency base would be 16.666MHz. From this reference one can generate a family of output frequencies at multiples of the 33.333MHz PCI clock. As an example to generate a 133.333MHz clock from a 16.666MHz reference the following M and N values would be used:

$$FOUT = 16.666 \div 16 \times M \div N = 1.0416 \times M \div N$$

Let N = 2, M = 133.3333 ÷ 1.0416 x 2 = 256

The value for M falls within the constraints set for PLL stability, therefore N[1:0] = 01 and M[8:0] = 10000000. If the value for M fell outside of the valid range a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MC12429 synthesizer.

M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the CMOS output may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1 and T0 control bits are preset to '000' when P_LOAD is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12429 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MC12429 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 5 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 250MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 125MHz as the minimum divide ratio of the N counter is 2. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

T2	**T1**	**T0**	**TEST** (Pin 20)
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	FREF
0	1	1	M COUNTER OUT
1	0	0	FOUT
1	0	1	LOW
1	1	0	MCNT
1	1	1	FOUT/4

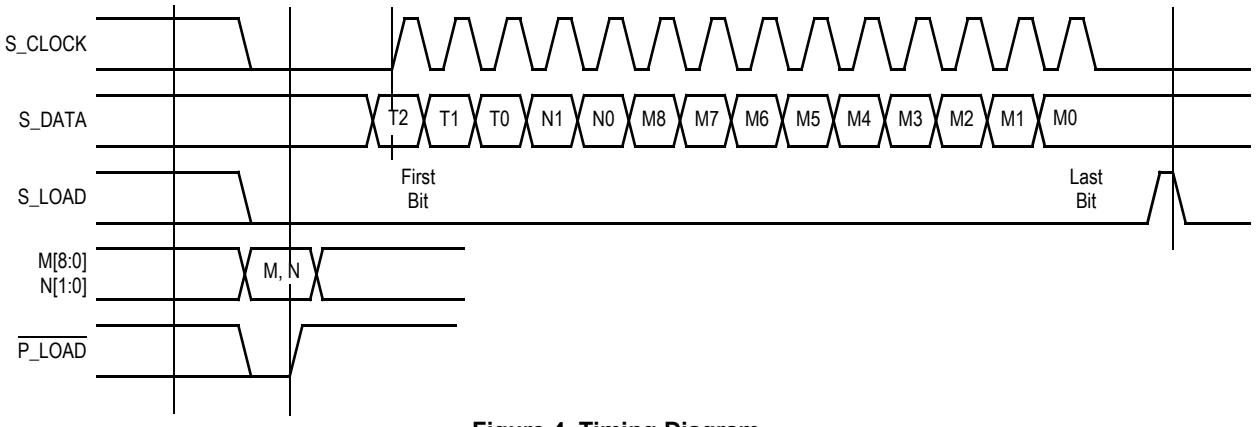
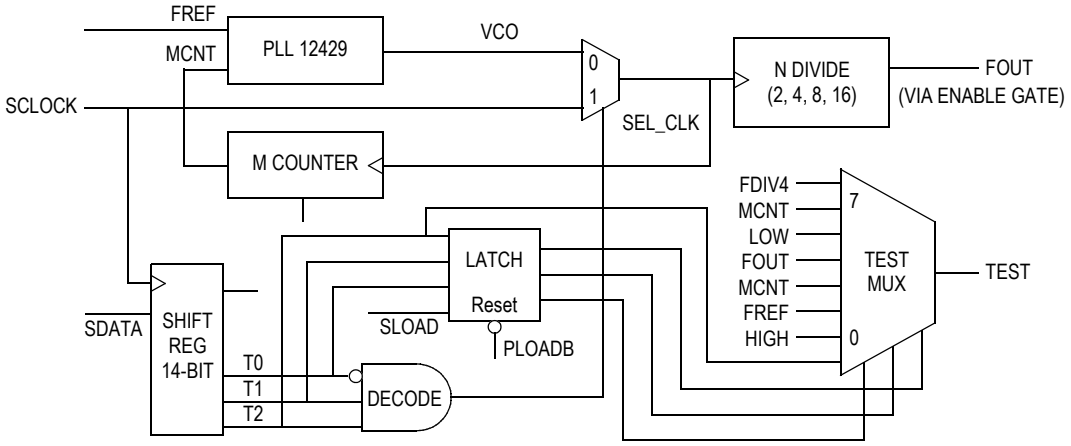


Figure 4. Timing Diagram



- T2=T1=1, T0=0: Test Mode (PLL bypass)
- SCLOCK is selected, MCNT is on TEST output, SCLOCK DIVIDE BY N is on FOUT pin

PLOADB acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

Figure 5. Serial Test Clock Block Diagram (PLL bypass)

Table 3. DC Characteristics (V_{CC} = 3.3V ±5%)

Symbol	Characteristic	0°C			25°C			70°C				Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	
V_{IH}	Input HIGH Voltage	2.2			2.2			2.2			V	
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V	
I_{IN}	Input Current			1.0			1.0			1.0	mA	
V_{OH}	Output HIGH Voltage TEST	2.5			2.5			2.5			V	I_{OH} = –0.8mA
V_{OL}	Output LOW Voltage TEST			0.4			0.4			0.4	V	I_{OL} = 0.8mA
V_{OH}	Output HIGH Voltage[1] FOUT, $\overline{FOUT}$	2.28		2.60	2.32		2.49	2.38		2.565	V	V_{CCO} = 3.3V[2]
V_{OL}	Output LOW Voltage[1] FOUT, $\overline{FOUT}$	1.35		1.67	1.35		1.67	1.35		1.70	V	V_{CCO} = 3.3V[2]
I_{CC}	Power Supply Current V_{CC} PLL_V_{CC}		85 15	100 20		85 15	100 20		85 15	100 20	mA	

1. 50Ω to V_{CC} – 2.0V termination.
2. Output levels will vary 1:1 with V_{CC0} variation.

Table 4. DC Characteristics (V_{CC} = 5.0V ±5%)

Symbol	Characteristic	0°C			25°C			70°C				Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit	
V_{IH}	Input HIGH Voltage	3.5			3.5			3.5			V	
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V	
I_{IN}	Input Current			1.0			1.0			1.0	mA	
V_{OH}	Output HIGH Voltage TEST	2.5			2.5			2.5			V	I_{OH} = –0.8mA
V_{OL}	Output LOW Voltage TEST			0.4			0.4			0.4	V	I_{OL} = 0.8mA
V_{OH}	Output HIGH Voltage[1] FOUT, $\overline{FOUT}$	3.98		4.30	4.02		4.19	4.08		4.265	V	V_{CCO} = 5.0V[2]
V_{OL}	Output LOW Voltage[1] FOUT, $\overline{FOUT}$	3.05		3.37	3.05		3.37	3.05		3.40	V	V_{CCO} = 5.0V[2]
I_{CC}	Power Supply Current V_{CC} PLL_V_{CC}		85 15	100 20		85 15	100 20		85 15	100 20	mA	

1. 50Ω to V_{CC} – 2.0V termination.
2. Output levels will vary 1:1 with V_{CC0} variation.

Table 5. AC Characteristics (T_A = 0° to 70°C, V_{CC} = 3.3V to 5.0V ±5%)

Symbol	Characteristic		Min	Max	Unit	Condition
F_{MAXI}	Maximum Input Frequency	S_CLOCK Xtal Oscillator	 10	10 20	MHz	Note 1
F_{MAXO}	Maximum Output Frequency	VCO (Internal) FOUT	200 25	400 400	MHz	Note 2
t_{LOCK}	Maximum PLL Lock Time			10	ms	
t_{jitter}	Period Deviation (Peak-to-Peak)			±25	ps	Note 2, See Applications Section
t_s	Setup Time	S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20 20 20		ns	
t_h	Hold Time	S_DATA to S_CLOCK M, N to P_LOAD	20 20		ns	
tpw_{MIN}	Minimum Pulse Width	S_LOAD P_LOAD	50 50		ns	Note 2
t_r, t_f	Output Rise/Fall	FOUT	300	800	ps	20%-80%, Note 2

1. 10MHz is the maximum frequency to load the feedback divide registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.
2. 50Ω to V_{CC} – 2.0V pulldown.

APPLICATIONS INFORMATION

Using the On-Board Crystal Oscillator

The MC12429 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MC12429 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the xtal terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1KΩ.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MC12429 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 6 below specifies the performance requirements of the crystals to be used with the MC12429.

Table 6. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance[1]
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

1. See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MC12429 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12429 provides separate power supplies for the digital ciruitry (V_{CC}) and the internal PLL (PLL_V_{CC}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a

controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_V_{CC} pin for the MC12429.

Figure 6 illustrates a typical power supply filter scheme. The MC12429 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_V_{CC} pin of the MC12429. From the data sheet the I_{PLL_VCC} current (the current sourced through the PLL_V_{CC} pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_V_{CC} pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 6 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

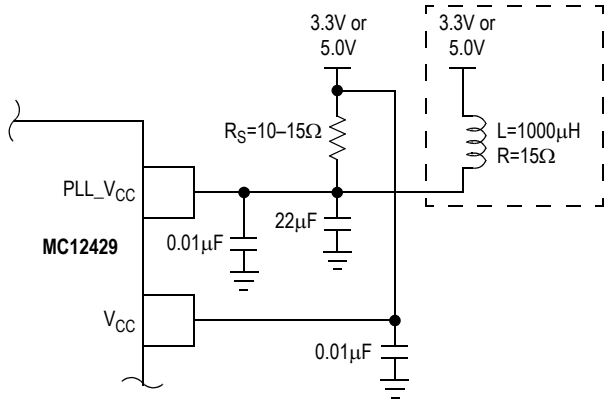


Figure 6. Power Supply Filter

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. Figure 6 shows a 1000μH choke, this value choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_V_{CC} pin a low DC resistance inductor is required (less than 15Ω). Generally the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12429 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 7 shows a representative board layout for the MC12429. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 7 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12429 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

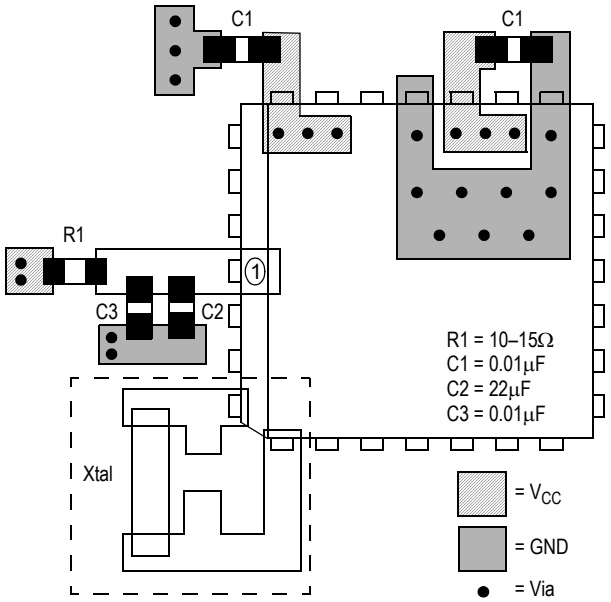


Figure 7. PCB Board Layout for MC12429 (28 PLCC)

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Note the provisions for placing a resistor across the crystal oscillator terminals as discussed in the crystal oscillator section of this data sheet.

Although the MC12429 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Jitter Performance of the MC12429

The MC12429 exhibits long term and cycle-to-cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

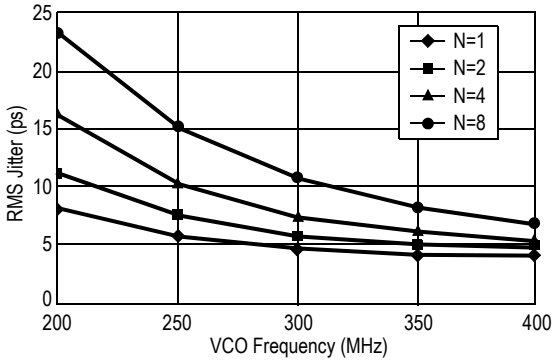


Figure 8. RMS PLL Jitter versus VCO Frequency

Figure 8 illustrates the RMS jitter performance of the MC12429 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data.

The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. All of the jitter data reported on the MC12429 was collected in this manner.

Figure 9 shows the jitter as a function of the output frequency. For the 12429 this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ±25ps peak-to-peak long term period jitter. The graph shows that for output frequencies from 87.5 to 400MHz the jitter falls within the ±25ps peak-to-peak specification. The general trend is that as the output frequency is decreased the output edge jitter will increase.

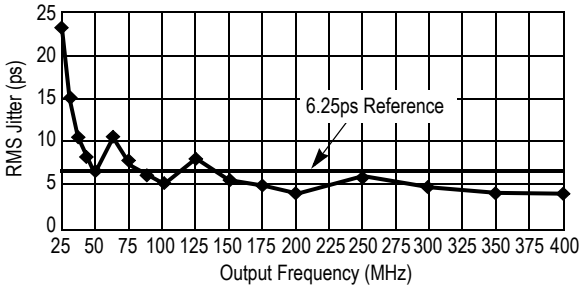


Figure 9. RMS Jitter versus Output Frequency

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

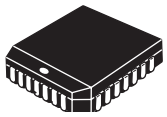
Order number: MC12430
Rev 6, 08/2004

High Frequency Clock Synthesizer

MC12430

(See Upgrade Product — MPC9230)

HIGH FREQUENCY PLL CLOCK SYNTHESIZER



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776-02

FA SUFFIX
32-LEAD TQFP PACKAGE
CASE 873A-03

The MC12430 is a general purpose synthesized clock source. Its internal VCO will operate over a range of frequencies from 400 to 800 MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4 or 8. With the output configured to divide the VCO frequency by 2, and with a 16.000 MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 1 MHz steps. The PLL loop filter is fully integrated so that no external components are required. The synthesizer output frequency is configured using a parallel or serial interface.

Features

- 50 to 800 MHz Differential PECL Outputs
- ±25 ps Peak-to-Peak Output Jitter
- Fully Integrated Phase-Locked Loop
- Minimal Frequency Over-Shoot
- Synthesized Architecture
- Serial 3-Wire Interface
- Parallel Interface for Power-Up
- Quartz Crystal Interface
- 28-Lead PLCC and 32-Lead LQFP Packages
- Operates from 3.3 V or 5.0V Power Supply

Functional Description

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 16 before being sent to the phase detector. With a 16 MHz crystal, this provides a reference frequency of 1 MHz. Although this data sheet illustrates functionality only for a 16 MHz crystal, any crystal in the 10-20 MHz range can be used.

The VCO within the PLL operates over a range of 400 to 800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be M x 2 times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

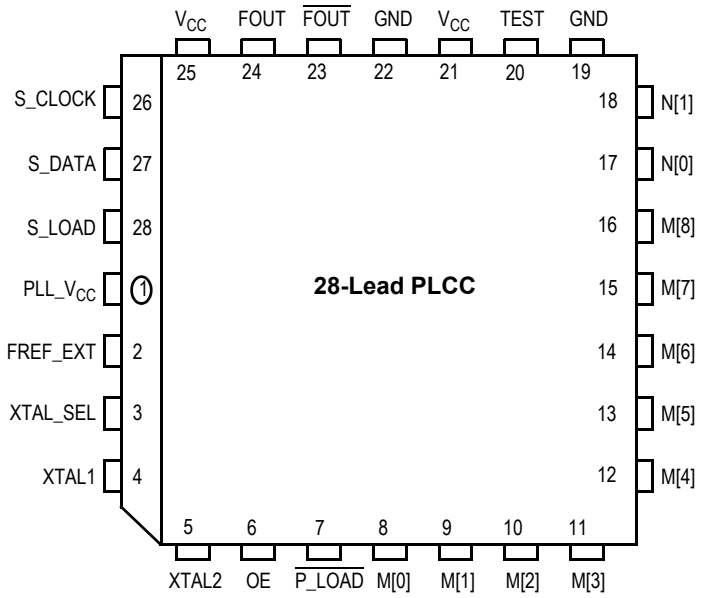
The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider (N divider) is configured through either the serial or the parallel interfaces and can provide one of four division ratios (1, 2, 4 or 8). This divider extends performance of the part while providing a 50 percent duty cycle.

The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated in 50Ω to V_{CC} – 2.0 V. The positive reference for the output driver and the internal logic is separated from the power supply for the phase-locked loop to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. On the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information.

The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. See the programming section for more information.



N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	1

INPUT	0	1
XTEL_SEL	FREF_EXT	XTAL
OE	Disabled	Enabled

Figure 1. 28-Lead Pinout (Top View)

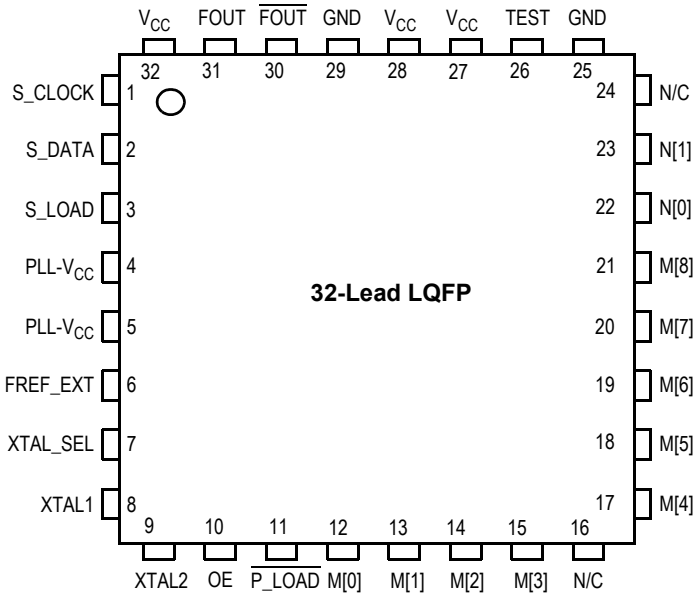


Figure 2. 32-Lead Pinout (Top View)

Table 1. Pin Descriptions

Pin Name		Function
Inputs		
XTAL1, XTAL2		These pins form an oscillator when connected to an external series-resonant crystal.
S_LOAD	(Int. Pulldown)	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.
S_DATA	(Int. Pulldown)	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK	(Int. Pulldown)	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
$\overline{\text{P\_LOAD}}$	(Int. Pullup)	This pin loads the configuration latches with the contents of the parallel inputs.The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation. $\overline{\text{P\_LOAD}}$ is state sensitive.
M[8:0]	(Int. Pullup)	These pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$. M[8] is the MSB, M[0] is the LSB.
N[1:0]	(Int. Pullup)	These pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$.
OE	(Int. Pullup)	Active HIGH Output Enable. The Enable is synchronous to eliminate possibility of runt pulse generation on the F_{OUT} output.
Outputs		
FOUT, $\overline{\text{FOUT}}$		These differential positive-referenced ECL signals (PECL) are the output of the synthesizer.
TEST		The function of this output is determined by the serial configuration bits T[2:0]. The output is single-ended ECL.
Power		
V_{CC}		This is the positive supply for the internal logic and the output buffer of the chip, and is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}). Current drain through $V_{CC} \approx$ 85mA.
PLL_V_{CC}		This is the positive supply for the PLL, and should be as noise-free as possible for low-jitter operation. This supply is connected to +3.3V or 5.0V (V_{CC} = PLL_V_{CC}). Current drain through PLL_$V_{CC} \approx$ 15mA.
GND		These pins are the negative supply for the chip and are normally all connected to ground.
Other		
FREF_EXT	(Int. Pulldown)	LVCMOS/CMOS input which can be used as the PLL reference.
XTAL_SEL	(Int. Pullup)	LVCMOS/CMOS input that selects between the crystal and the FREF_EXT source for the PLL reference signal. A HIGH selects the crystal input.

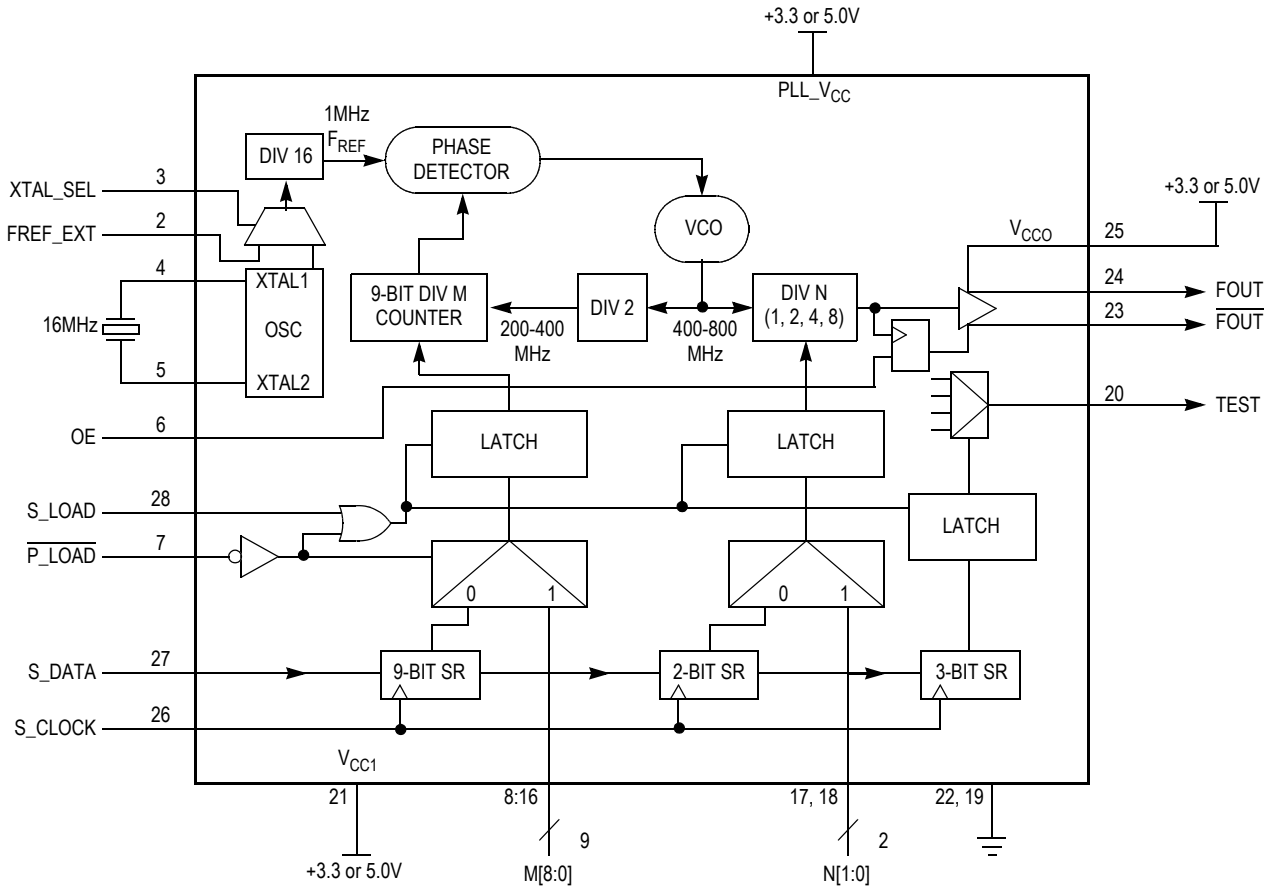


Figure 3. MC12430 Block Diagram (28-Lead PLCC Pinout)

PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = (F_{XTAL} \div 16) \times M \times 2 \div N \quad (1)$$

Where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $200 \leq M \leq 400$ for any input reference.

Assuming that a 16MHz reference frequency is used the above equation reduces to:

$$FOUT = 2 \times M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

Table 2. Output Frequency Range

N	FOUT	Output Frequency Range
1	2 x M	400 – 800 MHz
2	M	200 – 400 MHz
4	M ÷ 2	100 – 200 MHz
8	M ÷ 4	50 – 100 MHz

From these ranges the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example if an output frequency of 131 MHz was desired the following steps would be taken to identify the appropriate M and N values. 131 MHz falls within the frequency range set by an N value of 4 so N [1:0] = 01. For N = 4 FOUT = M ÷ 2 and M = 2 x FOUT. Therefore, M = 131 x 2 = 262, so M[8:0] = 100000110. Following this same procedure a user can generate any whole frequency desired between 50 and 800MHz. Note that for N > 2 fractional values of FOUT can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to FXTAL ÷ 8 ÷ N.

For input reference frequencies other than 16MHz, the set of appropriate equations can be deduced from equation 1. For computer applications another useful frequency base would be 16.666MHz. From this reference one can generate a family of output frequencies at multiples of the 33.333MHz PCI clock. As an example to generate a 133.333MHz clock from a 16.666MHz reference the following M and N values would be used:

FOUT = 16.666 ÷ 16 x M x 2 ÷ N = 1.04166 x M x 2 ÷ N

Let N = 4, M = 133.3333 ÷ 1.04166 x 2 = 256

The value for M falls within the constraints set for PLL stability, therefore N[1:0] = 01 and M[8:0} = 10000000. If the value for M fell outside of the valid range a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port, the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register, the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MC12430 synthesizer.

M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. The T2, T1 and T0 control bits are preset to '000' when P_LOAD is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12430 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MC12430 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 5 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 250MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 250MHz as the minimum divide ratio of the N counter is 1. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

T2	T1	T0	**Test** (Pin 20)
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	FREF
0	1	1	M COUNTER OUT/2
1	0	0	FOUT
1	0	1	LOW
1	1	0	M COUNTER/2 in PLL Bypass Mode
1	1	1	FOUT/4

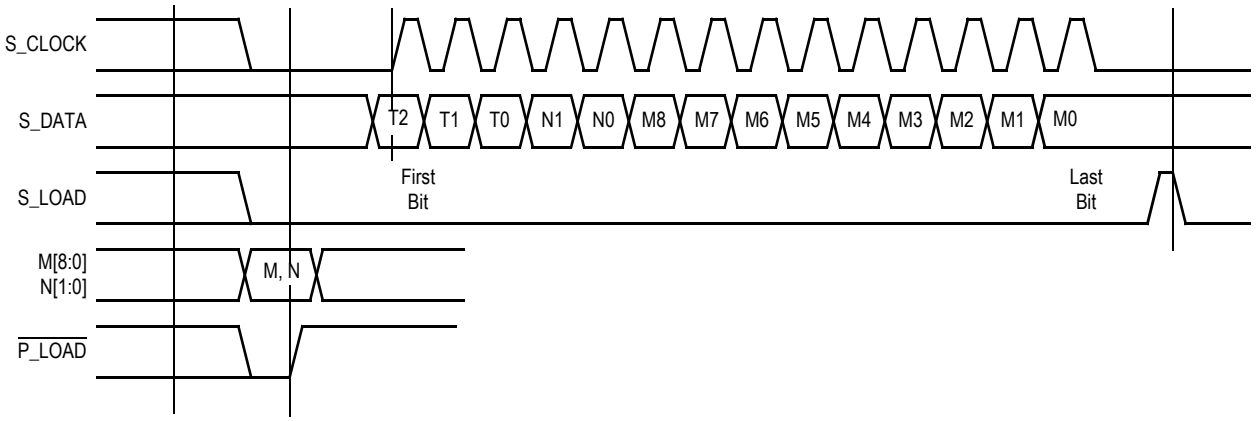
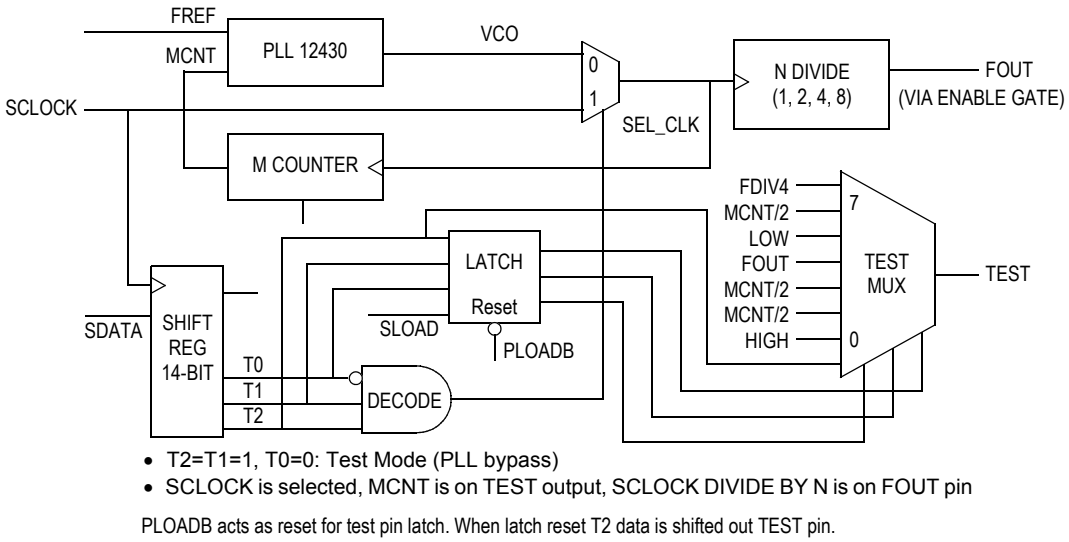


Figure 4. Timing Diagram



- T2=T1=1, T0=0: Test Mode (PLL bypass)
- SCLOCK is selected, MCNT is on TEST output, SCLOCK DIVIDE BY N is on FOUT pin

PLOADB acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

Figure 5. Serial Test Clock Block Diagram

Table 3. DC Characteristics (V_{CC} = 3.3V ±5%)

Symbol	Characteristic	0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH}	Input HIGH Voltage	2.2			2.2			2.2			V	
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V	
I_{IN}	Input Current			1.0			1.0			1.0	mA	
V_{OH}	Output HIGH Voltage TEST	2.5			2.5			2.5			V	I_{OH} = –0.8mA
V_{OL}	Output LOW Voltage TEST			0.4			0.4			0.4	V	I_{OL} = 0.8mA
V_{OH}	Output HIGH Voltage[1] FOUT, $\overline{FOUT}$	2.28		2.60	2.32		2.49	2.38		2.565	V	V_{CCO} = 3.3V[2,3]
V_{OL}	Output LOW Voltage[1] FOUT, $\overline{FOUT}$	1.35		1.67	1.35		1.67	1.35		1.70	V	V_{CCO} = 3.3V[2,3]
I_{CC}	Power Supply Current V_{CC} PLL_V_{CC}		90 15	110 20		90 15	110 20		90 15	100 20	mA	

1. See APPLICATIONS INFORMATION for output level versus frequency information.
2. Output levels will vary 1:1 with V_{CC0} variation.
3. 50Ω to V_{CC} – 2.0V termination.

Table 4. DC Characteristics (V_{CC} = 5.0V ±5%)

Symbol	Characteristic	0°C			25°C			70°C			Unit	Condition
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH}	Input HIGH Voltage	3.5			3.5			3.5			V	
V_{IL}	Input LOW Voltage			0.8			0.8			0.8	V	
I_{IN}	Input Current			1.0			1.0			1.0	mA	
V_{OH}	Output HIGH Voltage TEST	2.5			2.5			2.5			V	I_{OH} = –0.8mA
V_{OL}	Output LOW Voltage TEST			0.4			0.4			0.4	V	I_{OL} = 0.8mA
V_{OH}	Output HIGH Voltage[1] FOUT, $\overline{FOUT}$	3.98		4.30	4.02		4.19	4.08		4.265	V	V_{CCO} = 5.0V[2,3]
V_{OL}	Output LOW Voltage[1] FOUT, $\overline{FOUT}$	3.05		3.37	3.05		3.37	3.05		3.40	V	V_{CCO} = 5.0V[2,3]
I_{CC}	Power Supply Current V_{CC} PLL_V_{CC}		90 15	110 20		90 15	110 20		90 15	100 20	mA	

1. See APPLICATIONS INFORMATION for output level versus frequency information.
2. Output levels will vary 1:1 with V_{CC0} variation.
3. 50Ω to V_{CC} – 2.0V termination.

Table 5. AC Characteristics (T_A = 0° to 70°C, V_{CC} = 3.3V to 5.0V ±5%)

Symbol	Characteristic		Min	Max	Unit	Condition
F_{MAXI}	Maximum Input Frequency	S_CLOCK Xtal Oscillator FREF_EXT	 10 10	10 20 Note[1]	MHz	Note [2]
F_{MAXO}	Maximum Output Frequency	VCO (Internal) FOUT	400 –50	800 800	MHz	Note [3]
t_{LOCK}	Maximum PLL Lock Time			10	ms	
t_{jitter}	Period Deviation (Peak-to-Peak)[4]			±25 ±65	ps	N = 2, 4, 8: Note[3] N = 1; Note[3]
t_s	Setup Time	S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20 20 20		ns	
t_h	Hold Time	S_DATA to S_CLOCK M, N to P_LOAD	20 20		ns	
tpw_{MIN}	Minimum Pulse Width	S_LOAD P_LOAD	50 50		ns	
t_r, t_f	Output Rise/Fall	FOUT	300	800	ps	20%-80%, Note[3]

1. Maximum frequency on FREF_EXT is a function of the internal M counter limitations. The phase detector can handle up to 100MHz on the input, but the M counter must remain in the valid range of 200 ≤ M ≤ 400. See the Programming Interface section on page 4 of this data sheet for more details.
2. 10MHz is the maximum frequency to load the feedback divide registers. S_CLOCK can be switched at higher frequencies when used as a test clock in TEST_MODE 6.
3. 50Ω to V_{CC} – 2.0V pulldown.
4. See APPLICATIONS INFORMATION for additional information.

APPLICATIONS INFORMATION

Using the On-Board Crystal Oscillator

The MC12430 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MC12430 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately, most crystals are characterized in a parallel resonant mode. Fortunately, there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result, a parallel resonant crystal can be used with the MC12430 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application, this level of inaccuracy is immaterial. Table 1 below specifies the performance requirements of the crystals to be used with the MC12430.

Table 6. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance[1]
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

1. See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MC12430 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12430 provides separate power supplies for the digital ciruitry (V_{CC}) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MC12430.

Figure 6 illustrates a typical power supply filter scheme. The MC12430 is most susceptible to noise with spectral content in the 1KHz to 1MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_VCC pin of the MC12430. From the data sheet, the I_{PLL_VCC} current (the current sourced through the PLL_VCC pin) is typically 15mA (20mA maximum), assuming that a minimum of 3.0V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3V V_{CC} supply is used. The resistor shown in Figure 6 must have a resistance of 10–15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20KHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

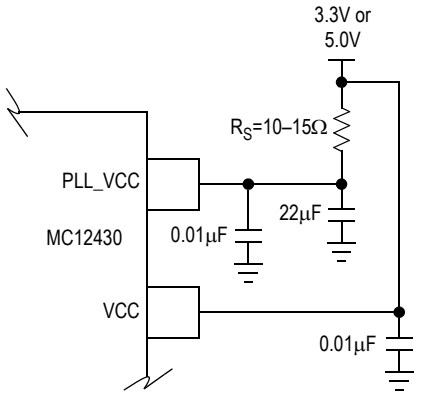


Figure 6. Power Supply Filter

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000μH choke will show a significant impedance at 10KHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin a low DC resistance inductor is required (less than 15Ω). Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12430 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 7 shows a representative board layout for the MC12430. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 7 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12430 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

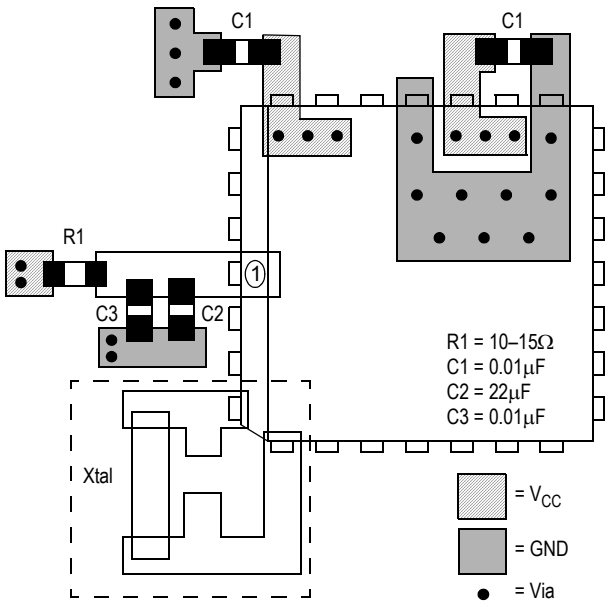


Figure 7. PCB Board Layout for MC12430 (28 PLCC)

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator.

Although the MC12430 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded

due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Jitter Performance of the MC12430

The MC12430 exhibits long term and cycle-to-cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

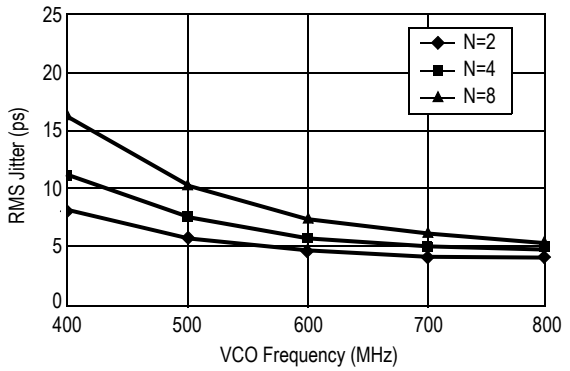


Figure 8. RMS PLL Jitter versus VCO Frequency

Figure 8 illustrates the RMS jitter performance of the MC12430 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data.

The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. The oscillator cannot collect adjacent pulses, rather it collects pulses from a very large sample of pulses.

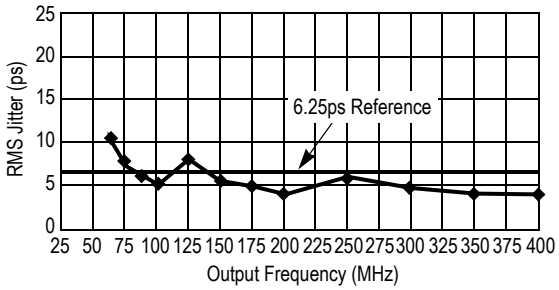


Figure 9. RMS Jitter versus Output Frequency

Figure 9 shows the jitter as a function of the output frequency. For the MC12430 this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ±25ps peak-to-peak long term period jitter. The graph shows that for output frequencies from 87.5 to 400MHz the jitter falls within the ±25ps peak-to-peak specification. The general trend is that as the output frequency is decreased the output edge jitter will increase.

The jitter data from Figure 8 and Figure 9 do not include the performance of the MC12430 when the output is in the divide by 1 mode. In divide by one mode, the MC12430 output jitter distribution is bimodal. Since a bimodal distribution cannot be accurately represented with an rms value, peak-to-peak values of jitter for the divide by one mode are presented.

Figure 10 shows the peak-to-peak jitter of the 12430 output in divide by one mode as a function of output frequency. Notice that as with the other modes the jitter improves with increasing frequency. The ±65 ps shown in the data sheet table represents a conservative value of jitter, especially for the higher VCO, and thus output frequencies.

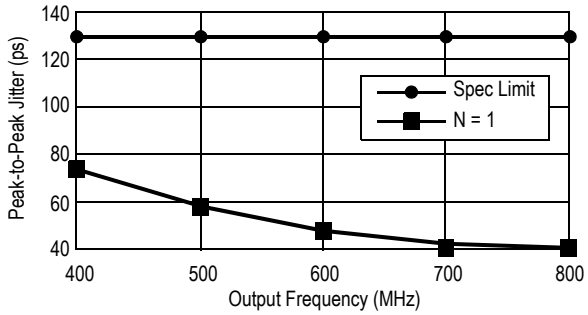


Figure 10. Peak-to-Peak Jitter versus Output Frequency

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

Output Voltage Swing vs Frequency

In the divide by one mode, the output rise and fall times will limit the peak to peak output voltage swing. For a 400 MHz output, the peak to peak swing of the 12430 output will be approximately 700 mV. This swing will gradually degrade as the output frequency increases, at 800 MHz the output swing will be reduced to approximately 500 mV. For a worst case analysis, it would be safe to assume that the 12430 output will always generate at least a 500mV output swing. Note that most high speed ECL receivers require only a few hundred millivolt input swings for reliable operation. As a result, the output generated by the 12430 will, under all conditions, be sufficient for clocking standard ECL devices. Note that if a larger swing is required the MC12430 could drive a clock fanout buffer like the MC100EP111.

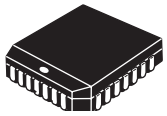
Order number: MC12439
Rev 6, 09/2001

High Frequency Clock Synthesizer

MC12439

HIGH FREQUENCY PLL CLOCK SYNTHESIZER

The MC12439 is a general purpose synthesized clock source. Its internal VCO will operate over a range of frequencies from 400 to 800 MHz. The differential PECL output can be configured to be the VCO frequency divided by 1, 2, 4, or 8. With the output configured to divide the VCO frequency by 1, and with a 16.66 MHz external quartz crystal used to provide the reference frequency, the output frequency can be specified in 16.66 MHz steps. The output frequency is configured using a parallel or serial interface.



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776-02

Features

- 50 to 800 MHz Differential PECL Outputs
- ±25 ps Typical Peak-to-Peak Output Jitter
- Minimal Frequency Over-Shoot
- Synthesized Architecture
- Serial 3-Wire Interface
- Parallel Interface for Power-Up
- Quartz Crystal Interface
- 28-Lead PLCC Package
- Operates from 3.3 V or 5.0 V Power Supply

Functional Description

The internal oscillator uses the external quartz crystal as the basis of its frequency reference. The output of the reference oscillator is divided by 2 before being sent to the phase detector. With a 16.66 MHz crystal, this provides a reference frequency of 8.33 MHz. Although this data sheet illustrates functionality only for a 16 MHz and 16.66 MHz crystal, any crystal in the 10-20 MHz range can be used. In addition to the crystal, an LVCMOS input can also be used as the PLL reference. The reference is selected via the XTAL_SEL input pin.

The VCO within the PLL operates over a range of 400 to 800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The output of this loop divider is also applied to the phase detector.

The phase detector and loop filter attempt to force the VCO output frequency to be 2 x M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve loop lock.

The output of the VCO is also passed through an output divider before being sent to the PECL output driver. This output divider is configured through either the serial or the parallel interfaces and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50 percent duty cycle.

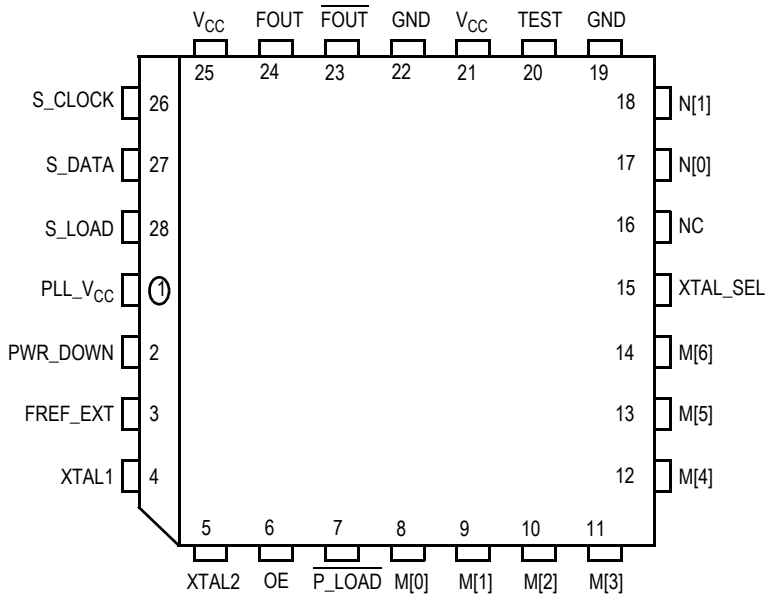
The output driver is driven differentially from the output divider and is capable of driving a pair of transmission lines terminated in 50 Ω to V_{CC} – 2.0 V.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. Normally, on system reset, the $\overline{\text{P\_LOAD}}$ input is held LOW until sometime after power becomes valid. On the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs to reduce component count in the application of the chip.

The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See PROGRAMMING INTERFACE for more information.

The TEST output reflects various internal node values and is controlled by the T[2:0] bits in the serial data stream. See PROGRAMMING INTERFACE for more information.

The PWR_DOWN pin, when asserted, will synchronously divide the FOUT by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de-assertion of the PWR_DOWN pin, the FOUT input will step back up to its programmed frequency in four discrete increments.



N[1:0]	Output Division
0 0	2
0 1	4
1 0	8
1 1	1

Input	0	1
PWR_DOWN	FOUT	FOUT/16
XTAL_SEL	FREF_EXT	XTAL
OE	Disabled	Enabled

Figure 1. 28-Lead Pinout (Top View)

Table 1. Pin Descriptions

Pin Name	Type	Function
Inputs		
XTAL1, XTAL2	—	These pins form an oscillator when connected to an external series-resonant crystal.
S_LOAD	Int. Pulldown	This pin loads the configuration latches with the contents of the shift registers. The latches will be transparent when this signal is HIGH, thus the data must be stable on the HIGH-to-LOW transition of S_LOAD for proper operation.
S_DATA	Int. Pulldown	This pin acts as the data input to the serial configuration shift registers.
S_CLOCK	Int. Pulldown	This pin serves to clock the serial configuration shift registers. Data from S_DATA is sampled on the rising edge.
$\overline{\text{P\_LOAD}}$	Int. Pullup	This pin loads the configuration latches with the contents of the parallel inputs.The latches will be transparent when this signal is LOW, thus the parallel data must be stable on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$ for proper operation.
M[6:0]	Int. Pullup	These pins are used to configure the PLL loop divider. They are sampled on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$. M[6] is the MSB, M[0] is the LSB.
N[1:0]	Int. Pullup	These pins are used to configure the output divider modulus. They are sampled on the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$. $\overline{\text{P\_LOAD}}$ is state sensitive.
OE	Int. Pullup	Active HIGH Output Enable.
Outputs		
F_{OUT}, $\overline{F_{OUT}}$	—	These differential positive-referenced ECL signals (PECL) are the output of the synthesizer.
TEST	—	The function of this output is determined by the serial configuration bits T[2:0].
Power		
V_{CC}	—	This is the positive supply for the chip, and is connected to +3.3 V or 5.0 V (V_{CC} = PLL_V_{CC}).
PLL_V_{CC}	—	This is the positive supply for the PLL and should be as noise-free as possible for low-jitter operation. This supply is connected to +3.3 V or 5.0 V (V_{CC} = PLL_V_{CC}).
GND	—	These pins are the negative supply for the chip and are normally all connected to ground.
Other		
PWR_DOWN	Int. Pulldown	LVCMOS input that forces the FOUT output to synchronously reduce its frequency by a factor of 16.
FREF_EXT	Int. Pulldown	LVCMOS input which can be used as the PLL reference frequency.
XTAL_SEL	Int. Pullup	LVCMOS input that selects between the XTAL and FREF_EXT PLL reference inputs. A HIGH selects the XTAL input.

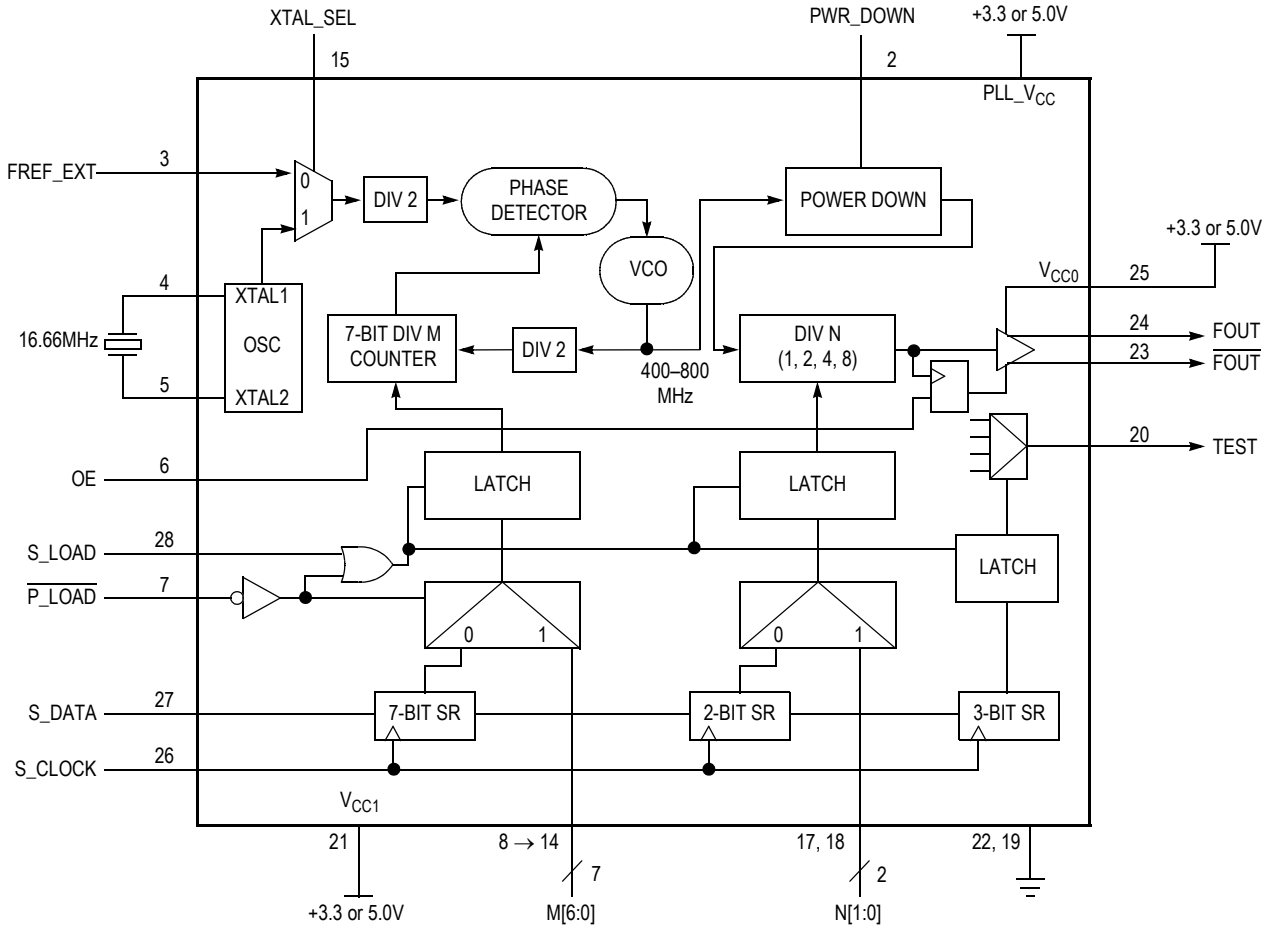


Figure 2. MC12439 Block Diagram

PROGRAMMING INTERFACE

Programming the device amounts to properly configuring the internal dividers to produce the desired frequency at the outputs. The output frequency can by represented by this formula:

$$FOUT = F_{XTAL} \times M \div N \quad (1)$$

Where F_{XTAL} is the crystal frequency, M is the loop divider modulus, and N is the output divider modulus. Note that it is possible to select values of M such that the PLL is unable to achieve loop lock. To avoid this, always make sure that M is selected to be $25 \leq M \leq 50$ for a 16MHz input reference.

For input references other than 16MHz, the valid M values can be calculated from the valid VCO range of 400–800MHz.

Assuming that a 16MHz reference frequency is used, the above equation reduces to:

$$FOUT = 16 \times M \div N$$

Substituting the four values for N (1, 2, 4, 8) yields:

Table 2. Output Frequency Range

N	FOUT	Output Frequency Range
1	16 x M	400 – 800 MHZ
2	8 x M	200 – 400 MHZ
4	4 x M	100 – 200 MHZ
8	2 x M	50 – 100 MHZ

From these ranges, the user will establish the value of N required, then the value of M can be calculated based on the appropriate equation above. For example, if an output frequency of 384MHz was desired, the following steps would be taken to identify the appropriate M and N values. 384 MHz falls within the frequency range set by an N value of 2, so N [1:0] = 00. For N = 2, F_{OUT} = 8M and M = $F_{OUT} \div 8$. Therefore, M = 384 ÷ 8 = 48, so M[8:0] = 0110000.

For input reference frequencies other than 16MHz, the set of appropriate equations can be deduced from equation 1. For computer applications, another useful frequency base would be 16.666MHz. From this reference, one can generate a family of output frequencies at multiples of the 33.333 MHz PCI clock. As an example, to generate a 533.333MHz clock from a 16.666MHz reference, the following M and N values would be used:

FOUT = 16.666 x M ÷ N

Let N = 1, M = 533.333 ÷ 16.666 = 32

The value for M falls within the constraints set for PLL stability ($400 \div 16.666 \leq M \leq 800 \div 16.666$; $24 \leq M \leq 48$), therefore N[1:0] = 11 and M[6:0} = 0100000. If the value for M fell outside of the valid range, a different N value would be selected to try to move M in the appropriate direction.

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW to HIGH transition will latch the information present on the M[6:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW, the input latches will be transparent and any changes on the M[6:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port, the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register, the most significant bit is loaded first (T2, N1 and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 3 illustrates the timing diagram for both a parallel and a serial load of the MC12439 synthesizer.

M[6:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents F_{OUT}, the CMOS output may not be able to toggle fast enough for some of the higher output frequencies. The T2, T1 and T0 control bits are preset to '000' when P_LOAD is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MC12439 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110, the MC12439 is placed in PLL bypass mode. In this mode, the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the F_{OUT} differential pair and the M counter drives the TEST output pin. In this mode, the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clock tree. Figure 4 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level, the input frequency is limited to 250 MHz or less. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 250 MHz as the minimum divide ratio of the N counter is 1. Note that the M counter output on the TEST output will not be a 50% duty cycle due to the way the divider is implemented.

T2	T1	T0	**TEST** (Pin 20)
0	0	0	SHIFT REGISTER OUT
0	0	1	HIGH
0	1	0	FREF
0	1	1	M COUNTER OUT/2
1	0	0	FOUT
1	0	1	LOW
1	1	0	M COUNTER/2 in PLL Bypass Mode
1	1	1	FOUT/4

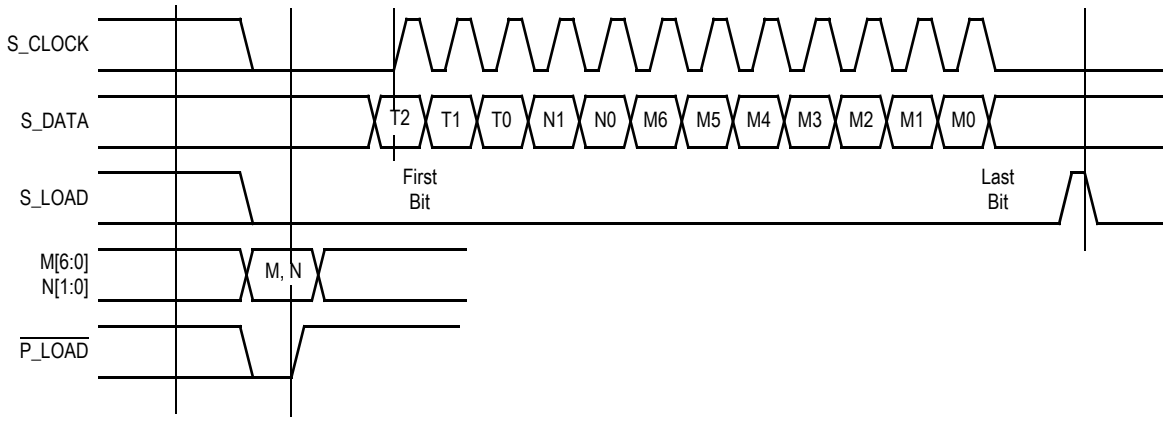
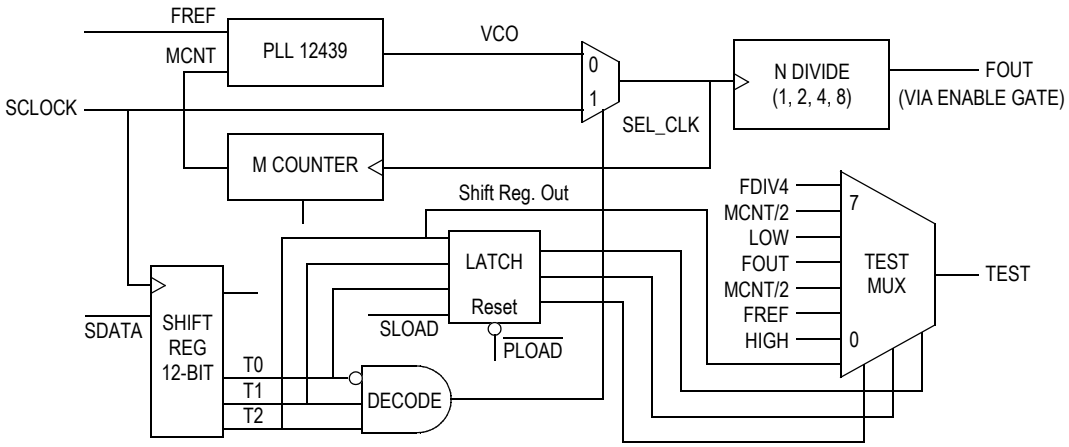


Figure 3. Timing Diagram



- T2=T1=1, T0=0: Test Mode (PLL bypass)
- SCLOCK is selected, MCNT/2 is on TEST output, SCLOCK DIVIDE BY N is on FOUT pin

$\overline{\text{PLOAD}}$ acts as reset for test pin latch. When latch reset T2 data is shifted out TEST pin.

Figure 4. Serial Test Clock Block Diagram

Table 3. DC Characteristics (V_{CC} = 3.3 V ±5%)

Symbol	Characteristic		0°C			25°C			70°C			Unit	Condition
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH}	Input HIGH Voltage		2.0			2.0			2.0			V	
V_{IL}	Input LOW Voltage				0.8			0.8			0.8	V	
I_{IN}	Input Current				1.0			1.0			1.0	mA	
I_{OH}	Output HIGH Current[1]	FOUT, $\overline{\text{FOUT}}$			50			50			50	mA	Continuous
V_{OH}	Output HIGH Voltage	TEST	2.5			2.5			2.5			V	I_{OH} = –0.8mA
V_{OL}	Output LOW Voltage	TEST			0.4			0.4			0.4	V	I_{OL} = 0.8mA
V_{OH}	Output HIGH Voltage[2]	FOUT, $\overline{\text{FOUT}}$	2.28		2.60	2.32		2.49	2.38		2.565	V	V_{CCO} = 3.3V[3 4]
V_{OL}	Output LOW Voltage[2]	FOUT, $\overline{\text{FOUT}}$	1.35		1.67	1.35		1.67	1.35		1.70	V	V_{CCO} = 3.3V[3 4]
I_{CC}	Power Supply Current	V_{CC} PLL_V_{CC}		90 15	110 20		90 15	110 20		90 15	110 20	mA	

1. Maximum I_{OH} spec implies the device can drive 25Ω impedance with the PECL outputs.
2. See APPLICATIONS INFORMATION for output level versus frequency information.
3. Output levels will vary 1:1 with V_{CC} variation.
4. 50Ω to V_{CC} – 2.0V termination.

Table 4. DC Characteristics (V_{CC} = 5.0 V ±5%)

Symbol	Characteristic		0°C			25°C			70°C			Unit	Condition
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V_{IH}	Input HIGH Voltage		3.5			3.5			3.5			V	
V_{IL}	Input LOW Voltage				0.8			0.8			0.8	V	
I_{IN}	Input Current				1.0			1.0			1.0	mA	
I_{OH}	Output HIGH Current[1]	FOUT, $\overline{\text{FOUT}}$			50			50			50	mA	Continuous
V_{OH}	Output HIGH Voltage	TEST	3.8			3.8			3.8			V	I_{OH} = -0.8 mA
V_{OL}	Output LOW Voltage[2]	TEST			0.4			0.4			0.4	V	I_{OL} = 0.8 mA
V_{OH}	Output HIGH Voltage[2]	FOUT, $\overline{\text{FOUT}}$	3.98		4.30	4.02		4.19	4.08		4.265	V	V_{CCO} = 5.0 V[3 4]
V_{OL}	Output LOW Voltage	FOUT, $\overline{\text{FOUT}}$	3.05		3.37	3.05		3.37	3.05		3.40	V	V_{CCO} = 5.0 V[3 4]
I_{CC}	Power Supply Current	V_{CC} PLL_V_{CC}		90 15	110 20		90 15	110 20		90 15	110 20	mA	

1. Maximum I_{OH} spec implies the device can drive 25Ω impedance with the PECL outputs.
2. See APPLICATIONS INFORMATION for output level versus frequency information.
3. Output levels will vary 1:1 with V_{CC0} variation.
4. 50Ω to V_{CC} – 2.0V termination.

Table 5. AC Characteristics (TA = 0 to 70°C; V_{CC} = 3.3 to 5.0V ±5%)

Symbol	Characteristic		Min	Max	Unit	Condition
F_{MAXI}	Maximum Input Frequency	S_CLOCK Xtal Oscillator FREF_EXT	 10 10	10 20 Note[1]	MHz	
F_{MAXO}	Maximum Output Frequency	VCO (Internal) FOUT	400 50	900 800	MHz	Note[2]
t_{LOCK}	Maximum PLL Lock Time		1	10	ms	
t_{jitter}	Period Deviation (Peak-to-Peak)[3]			±25 ±65	ps	N = 2,4,8; Note[2] N = 1; Note[2]
t_s	Setup Time	S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to $\overline{\text{P\_LOAD}}$	20 20 20		ns	
t_h	Hold Time	S_DATA to S_CLOCK M, N to $\overline{\text{P\_LOAD}}$	20 20		ns	
tpw_{MIN}	Minimum Pulse Width	S_LOAD $\overline{\text{P\_LOAD}}$	50 50		ns	Note[2]
t_r, t_f	Output Rise/Fall Time		300	800	ps	Note[2]

1. Maximum frequency on FREF_EXT is a function of the internal M counter limitations. The phase detector can handle up to 100 MHz on the input, but the M counter must remain in the valid range of 25 ≤ M ≤ 50. See PROGRAMMING INTERFACE in this data sheet for more details.
2. 50 Ω to V_{CC} – 2.0 V pulldown.
3. See APPLICATIONS INFORMATION for additional information.

APPLICATIONS INFORMATION

Using the On-Board Crystal Oscillator

The MC12439 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs, the user is advised to mount the crystal as close to the MC12439 as possible to avoid any board level parasitics. To facilitate co-location, surface mount crystals are recommended but not required.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately, most crystals are characterized in a parallel resonant mode. Fortunately, there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result, a parallel resonant crystal can be used with the MC12439 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application, this level of inaccuracy is immaterial. Table 6 below specifies the performance requirements of the crystals to be used with the MC12439.

Table 6. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance[1]
Frequency Tolerance	±75 ppm at 25°C
Frequency/Temperature Stability	±150 pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5-7 pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μW
Aging	5 ppm/Yr (First 3 Years)

1. See accompanying text for series versus parallel resonant discussion.

Power Supply Filtering

The MC12439 is a mixed analog/digital product, and as such, it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MC12439 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (PLL_VCC) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the PLL_VCC pin for the MC12439.

Figure 5 illustrates a typical power supply filter scheme. The MC12439 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the PLL_V_{CC} pin of the MC12439. From the data sheet, the I_{PLL_VCC} current (the current sourced through the PLL_VCC pin) is typically 15mA (20 mA maximum), assuming that a minimum of 3.0 V must be maintained on the PLL_VCC pin very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 5 must have a resistance of 10-15Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

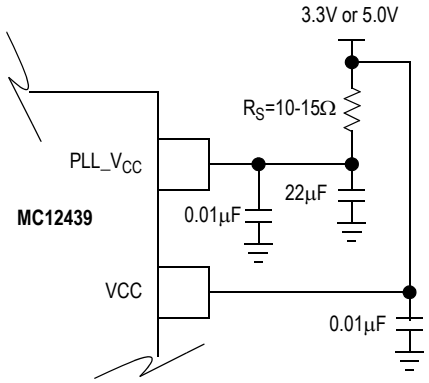


Figure 5. Power Supply Filter

A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the PLL_VCC pin, a low DC resistance inductor is required (less than 15 Ω). Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering.

The MC12439 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MC12439. There exist many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general

purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the 12439 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors.

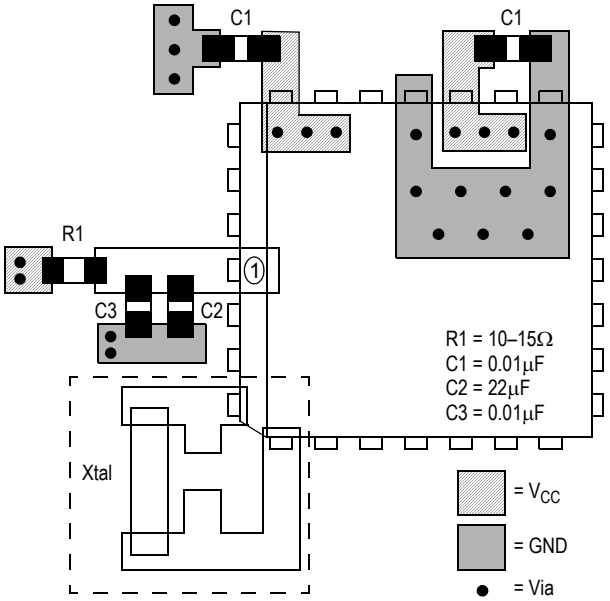


Figure 6. PCB Board Layout for MC12439

Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit, and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator.

Although the MC12439 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Jitter Performance of the MC12439

The MC12439 exhibits long term and cycle-to-cycle jitter which rivals that of SAW based oscillators. This jitter performance comes with the added flexibility one gets with a synthesizer over a fixed frequency oscillator.

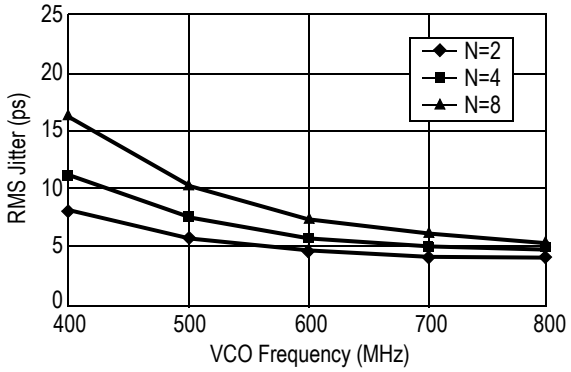


Figure 7. RMS PLL Jitter versus VCO Frequency

Figure 7 illustrates the RMS jitter performance of the MC12439 across its specified VCO frequency range. Note that the jitter is a function of both the output frequency as well as the VCO frequency, however the VCO frequency shows a much stronger dependence. The data presented has not been compensated for trigger jitter, this fact provides a measure of guardband to the reported data.

The typical method of measuring the jitter is to accumulate a large number of cycles, create a histogram of the edge placements and record peak-to-peak as well as standard deviations of the jitter. Care must be taken that the measured edge is the edge immediately following the trigger edge. The oscilloscope cannot collect adjacent pulses, rather it collects pulses from a very large sample of pulses.

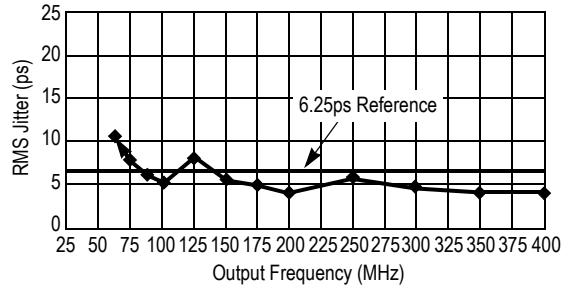


Figure 8. RMS Jitter versus Output Frequency

Figure 8 shows the jitter as a function of the output frequency. For the 12439, this information is probably of more importance. The flat line represents an RMS jitter value that corresponds to an 8 sigma ±25 ps peak-to-peak long term period jitter. The graph shows that for output frequencies from 87.5 to 400 MHz the jitter falls within the ±25 ps peak-to-peak specification. The general trend is that as the output frequency is decreased, the output edge jitter will increase.

The jitter data from Figure 7 does not include the performance of the 12439 when the output is in the divide by 1 mode. In divide by one mode, the MC12439 output jitter distribution is bimodal. Since a bimodal distribution cannot be accurately represented with an rms value, peak-to-peak values of jitter for the divide by one mode are presented.

Figure 9 shows the peak-to-peak jitter of the 12439 output in divide by one mode as a function of output frequency. Notice that as with the other modes, the jitter improves with increasing frequency. The ±65 ps shown in the data sheet table represents a conservative value of jitter, especially for the higher VCO, and thus output frequencies.

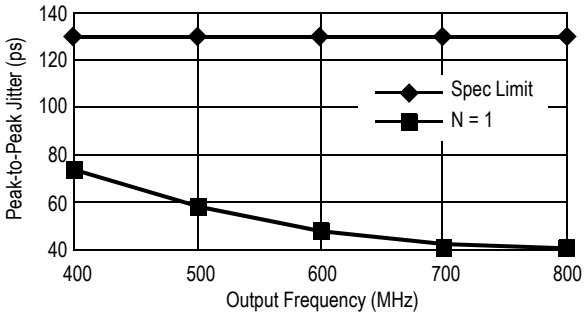


Figure 9. Peak-to-Peak versus Output Frequency

The jitter data presented should provide users with enough information to determine the effect on their overall timing budget. The jitter performance meets the needs of most system designs while adding the flexibility of frequency margining and field upgrades. These features are not available with a fixed frequency SAW oscillator.

Output Voltage Swing vs Frequency

In the divide by one mode, the output rise and fall times will limit the peak to peak output voltage swing. For a 400 MHz output, the peak to peak swing of the 12439 output will be approximately 700 mV. This swing will gradually degrade as the output frequency increases, at 800 MHz the output swing will be reduced to approximately 500 mV. For a worst case analysis, it would be safe to assume that the 12439 output will always generate at least a 400mV output swing. Note that most high speed ECL receivers require only a few hundred millivolt input swings for reliable operation. As a result, the output generated by the 12439 will, under all conditions, be sufficient for clocking standard ECL devices. Note that if a larger swing is desired, the MC12439 could drive the clock fanout buffer MC100EP111.

Order number: MPC9229
Rev 2, 05/2004

400 MHz Low Voltage PECL Clock Synthesizer

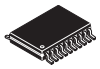
MPC9229

400 MHz LOW VOLTAGE CLOCK SYNTHESIZER

The MPC9229 is a 3.3 V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 25 MHz to 400 MHz and the support of differential PECL output signals the device meets the needs of the most demanding clock applications.

Features

- 25 MHz to 400 MHz synthesized clock output signal
- Differential PECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- 3.3 V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 32-lead LQFP and 20-lead PLCC packaging
- 32-lead and 20-lead Pb-free Package Available
- SiGe Technology
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MC12429



DT SUFFIX
20-LEAD TSSOP PACKAGE
CASE 948E-02

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator is divided by 16 and then multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1600 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be 4·M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1600 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50 Ω to V_{CC} –2.0 V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the $\overline{\text{P\_LOAD}}$ input LOW until power becomes valid. On the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. Refer to the programming section for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output.

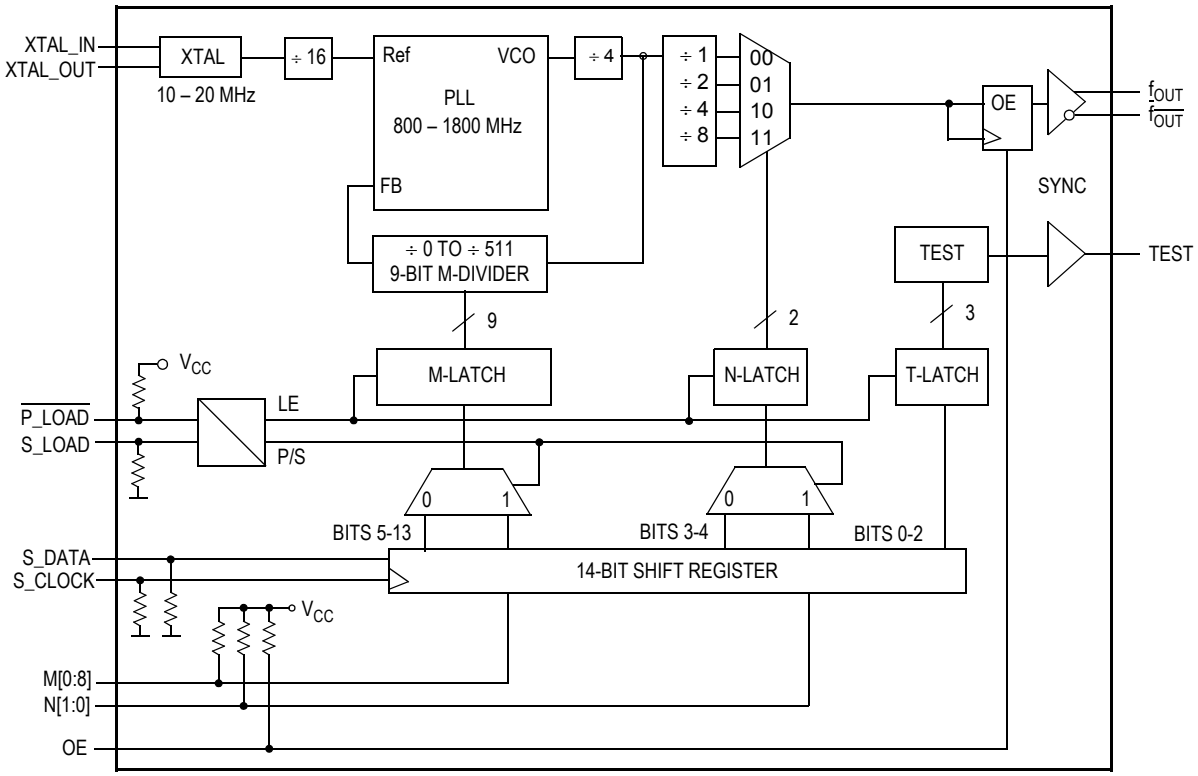


Figure 1. MPC9229 Logic Diagram

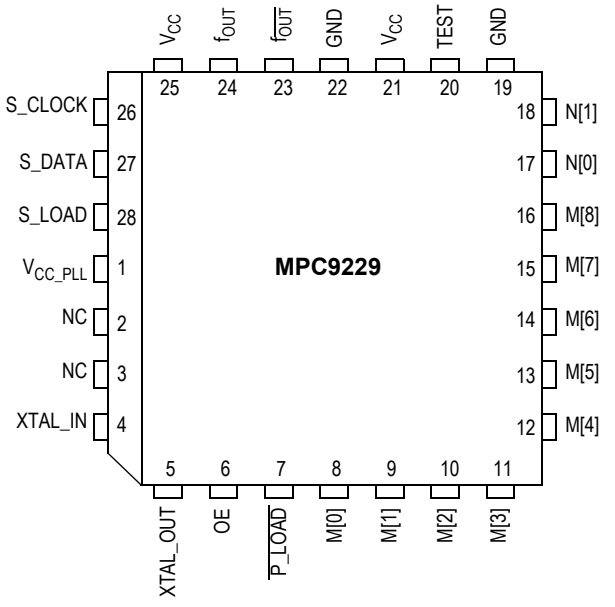


Figure 2. MPC9229 28-Lead PLCC Pinout
(Top View)

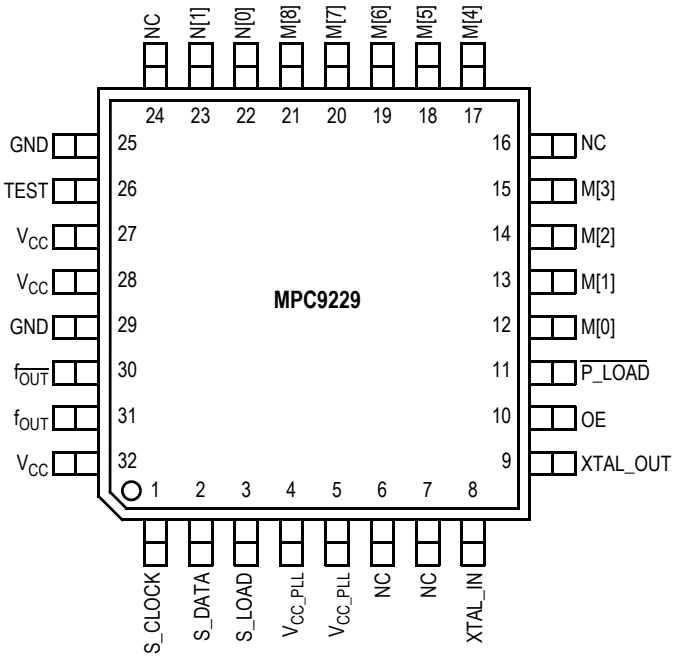


Figure 3. MPC9229 32-Lead LQFP Pinout
(Top View)

Table 1. Pin Configurations

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface.
f_{OUT}, $f_{\overline{OUT}}$	Output		LVPECL	Differential clock output.
TEST	Output		LVCMOS	Test and device diagnosis output.
S_LOAD	Input	0	LVCMOS	Serial configuration control input. This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
P_LOAD	Input	1	LVCMOS	Parallel configuration control input. This input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of P_LOAD. P_LOAD is state sensitive
S_DATA	Input	0	LVCMOS	Serial configuration data input.
S_CLOCK	Input	0	LVCMOS	Serial configuration clock input.
M[0:8]	Input	1	LVCMOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of P_LOAD.
N[1:0]	Input	1	LVCMOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of P_LOAD
OE	Input	1	LVCMOS	Output enable (active high). The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the f_{OUT} output. OE = L low stops f_{OUT} in the logic low state (f_{OUT} = L, $f_{\overline{OUT}}$ = H)
GND	Supply	Supply	Ground	Negative power supply (GND).
V_{CC}	Supply	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation.
V_{CC_PLL}	Supply	Supply	V_{CC}	PLL positive power supply (analog power supply).

Table 2. Output Frequency Range and PII Post-Divider N

N		Output Division	Output Frequency Range
1	**0**		
0	0	1	200 – 400 MHz
0	1	2	100 – 200 MHz
1	0	4	50 – 100 MHz
1	1	8	25 – 50 MHz

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} –2		V	
MM	ESD protection (Machine Model)	200			V	
HBM	ESD protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal resistance junction to ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS control inputs ($\overline{P\_LOAD}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1], OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[1]			±200	μA	V_{IN} = V_{CC} or GND
Differential clock output f_{OUT}[2]						
V_{OH}	Output High Voltage[3]	V_{CC} –1.02		V_{CC} –0.74	V	LVPECL
V_{OL}	Output Low Voltage[3]	V_{CC} –1.95		V_{CC} –1.60	V	LVPECL
Test and diagnosis output TEST						
V_{OH}	Output High Voltage[3]	2.0			V	I_{OH} = –0.8 mA
V_{OL}	Output Low Voltage[3]			0.55	V	I_{OL} = 0.8 mA
Supply current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			100	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50 Ω to V_{TT} = V_{CC} –2 V.
3. The MPC9229 TEST output levels are compatible to the MC12429 output levels.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal interface frequency range		10		20	MHz	
f_{VCO}	VCO frequency range[2]		800		1600	MHz	
f_{MAX}	Output Frequency	N = 00 (÷ 1) N = 01 (÷ 2) N = 10 (÷ 4) N = 11 (÷ 8)	200 100 50 25		400 200 100 50	MHz MHz MHz MHz	
DC	Output duty cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.05		0.3	ns	20% to 80%
f_{S_CLOCK}	Serial interface programming clock frequency[3]		0		10	MHz	
$t_{P,MIN}$	Minimum pulse width	(S_LOAD, $\overline{\text{P\_LOAD}}$)	50			ns	
t_S	Setup Time	S_DATA to S_CLOCK S_CLOCK to $\overline{\text{S\_LOAD}}$ M, N to $\overline{\text{P\_LOAD}}$	20 20 20			ns ns ns	
t_S	Hold Time	S_DATA to S_CLOCK M, N to $\overline{\text{P\_LOAD}}$	20 20			ns ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter	N = 00 (÷ 1) N = 01 (÷ 2) N = 10 (÷ 4) N = 11 (÷ 8)			90 130 160 190	ps ps ps ps	
$t_{JIT(PER)}$	Period Jitter	N = 00 (÷ 1) N = 01 (÷ 2) N = 10 (÷ 4) N = 11 (÷ 8)			70 120 140 170	ps ps ps ps	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M \div 4$.
3. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. Refer to APPLICATIONS INFORMATION for more details.

PROGRAMMING INTERFACE

Programming the MPC9229

Programming the MPC9229 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$f_{OUT} = (f_{XTAL} \div 16) \cdot (4 \cdot M) \div (4 \cdot N) \text{ or} \quad (1)$$

$$f_{OUT} = (f_{XTAL} \div 16) \cdot M \div N \quad (2)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 800 to 1600 MHz in order to achieve stable PLL operation:

$$M_{MIN} = 4 \cdot f_{VCO,MIN} \div f_{XTAL} \text{ and} \quad (3)$$

$$M_{MAX} = 4 \cdot f_{VCO,MAX} \div f_{XTAL} \quad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M = 200 and M = 400. Table 7 shows the usable VCO frequency and M divider range for other example input frequencies. Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$$f_{OUT} = M \div N$$

Table 7. MPC9229 Frequency Operating Range

M	M[8:0]	VCO frequency for a crystal interface frequency of						Output frequency for f_{XTAL} = 16 MHz and for N =			
		10	12	14	16	18	20	1	2	4	16
160	010100000						800				
170	010101010						850				
180	010110100					810	900				
190	010111110					855	950				
200	011001000				800	900	1000	200	100	50	25
210	011010010				840	945	1050	210	105	52.5	26.25
220	011011100				880	990	1100	220	110	55	27.50
230	011100110			805	920	1035	1150	230	115	57.5	28.75
240	011110000			840	960	1080	1200	240	120	60	30
250	011111010			875	100	1125	1250	250	125	62.5	31.25
260	100000100			910	1040	1170	1300	260	130	65	32.50
270	100001110		810	945	1080	1215	1350	270	135	67.5	33.75
280	100011000		840	980	1120	1260	1400	280	140	70	35
290	100100010		870	1015	1160	1305	1450	290	145	72.5	36.25
300	100101100		900	1050	1200	1350	1500	300	150	75	37.5
310	100110110		930	1085	1240	1395	1550	310	155	77.5	38.75
320	101000000	800	960	1120	1280	1440	1600	320	160	80	40
330	101001010	825	990	1155	1320	1485		330	165	82.5	41.25
340	101010100	850	1020	1190	1360	1530		340	170	85	42.5
350	101011110	875	1050	1225	1400	1575		350	175	87.5	43.75
360	101101000	900	1080	1260	1440			360	180	90	45
370	101110010	925	1110	1295	1480			370	185	92.5	46.25
380	101111100	950	1140	1330	1520			380	190	95	47.5
390	110000110	975	1170	1365	1560			390	195	97.5	48.75
400	110010000	1000	1200	1400	1600			400	200	100	50
410	110011010	1025	1230	1435							
420	110100100	1050	1260	1470							
430	110101110	1075	1290	1505							
440	110111000	1100	1320	1540							
450	111000010	1125	1350	1575							
510	111111110	1275	1530								

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 8. Output Frequency Range for f_{XTAL} = 16 MHz

N			f_{OUT}	f_{OUT} Range	f_{OUT} Step
1	0	Value			
0	0	1	M	200 – 400 MHz	1 MHz
0	1	2	M ÷ 2	100 – 200 MHz	500 kHz
1	0	4	M ÷ 4	50 – 100 MHz	250 kHz
1	1	8	M ÷ 8	25 – 50 MHz	125 kHz

Example Frequency Calculation for an 16 MHz Input Frequency

If an output frequency of 131 MHz was desired the following steps would be taken to identify the appropriate M and N values. According to Table 8, 131 MHz falls in the frequency set by an value of 2 so N[1:0] = 01. For N = 2 the output frequency is $f_{OUT} = M \div 2$ and $M = f_{OUT} \times 2$. Therefore M = 2 x 131 = 262, so M[8:0] = 100000110. Following this procedure a user can generate any whole frequency between 25 MHz and 400 MHz. Note than for N > 2 fractional values of can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to:

$$f_{STEP} = f_{XTAL} \div 16 \div N$$

APPLICATIONS INFORMATION

Using the Parallel and Serial Interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW-to-HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW, the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the f_{OUT} output pair. To use the serial port, the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14-bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1, and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH-to-LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC9229 synthesizer. M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the Test and Diagnosis Output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents f_{OUT}, the CMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis. The T2, T1, and T0 control bits are preset to '000' when P_LOAD is LOW so that the PECL f_{OUT} outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin. Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9229 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110, the MPC9229 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the f_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving f_{OUT} directly gives the user more control on the test clocks sent through the clock tree. Figure 6 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level, the input frequency is limited to 200 MHz. This means the fastest the f_{OUT} pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 9. Test and Debug Configuration for TEST

T[2:0]			TEST Output
T2	T1	T0	
0	0	0	14-bit shift register out[1]
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 16$
0	1	1	M-Counter out
1	0	0	f_{OUT}
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	$f_{OUT} \div 4$

1. Clocked out at the rate of S_CLOCK

Table 10. Debug Configuration for PLL Bypass[1]

Output	Configuration
f_{OUT}	S_CLOCK ÷ N
TEST	M-Counter out[2]

1. T[2:0] = 110. AC specifications do not apply in PLL bypass mode
2. Clocked out at the rate of S_CLOCK ÷ (4 · N)

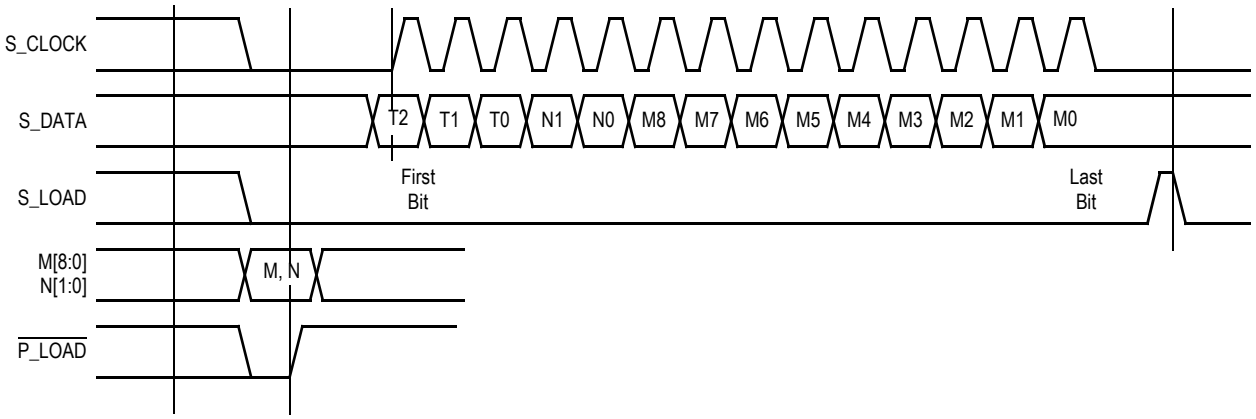


Figure 4. Serial Interface Timing Diagram

Power Supply Filtering

The MPC9229 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device characteristics. The MPC9229 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9229. Figure 5 illustrates a typical power supply filter scheme. The MPC9229 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the MPC9229 pin of the MPC9229. From the data sheet the V_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 5 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the V_{CC_PLL} pin, a low DC resistance inductor is required (less than 15 Ω).

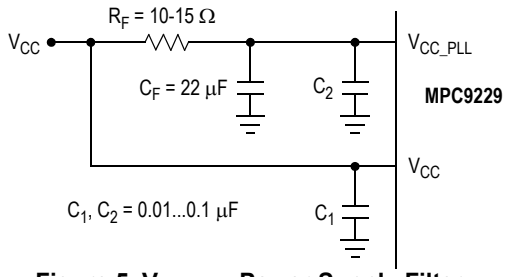


Figure 5. V_{CC_PLL} Power Supply Filter

Layout Recommendations

The MPC9229 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC9229. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC9229 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Although the MPC9229 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential

PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

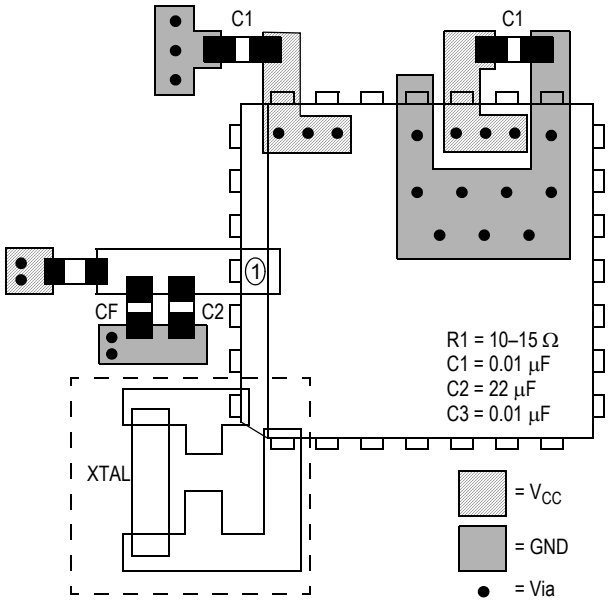


Figure 6. PCB Board Layout Recommendation for the PLCC28 Package

Using the On-Board Crystal Oscillator

The MPC9229 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC9229 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the xtal terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance, it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required, it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1 KΩ.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MPC9229 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 11 below specifies the performance requirements of the crystals to be used with the MPC9229.

Table 11. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance[1]
Frequency Tolerance	±75 ppm at 25°C
Frequency/Temperature Stability	±150 pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5 – 7pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μW
Aging	5 ppm/Yr (First 3 Years)

1. Refer to the accompanying text for series versus parallel resonant discussion.

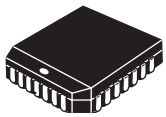
Order number: MPC9230
Rev 4, 07/2004

800 MHz Low Voltage PECL Clock Synthesizer

MPC9230

800 MHz LOW VOLTAGE CLOCK SYNTHESIZER

The MPC9230 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 50 MHz to 800 MHz(1) and the support of differential PECL output signals the device meets the needs of the most demanding clock applications.



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776-02

FA SUFFIX
32-LEAD TQFP PACKAGE
CASE 873A-03

Features

- 50 MHz to 800 MHz[1] synthesized clock output signal
- Differential PECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference clock input
- 3.3V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 32-lead LQFP and 28-lead PLCC packaging
- 32-lead and 28-lead Pb-free package available
- SiGe Technology
- Ambient temperature range -40°C to +85°C
- Pin and function compatible to the MC12430

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator is divided by 16 and then multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1600 MHz.[1] Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be 8·M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1600 MHz[1]). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50Ω to V_{CC} – 2.0V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the P_LOAD input LOW until power becomes valid. On the LOW–to–HIGH transition of P_LOAD, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See the programming section for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output.

1. The VCO frequency range of 800–1600 MHz is available at an ambient temperature range of 0 to 70°C. At –40 to +85°C, the VCO frequency (output frequency) is limited to max. 1500 MHz (750 MHz)

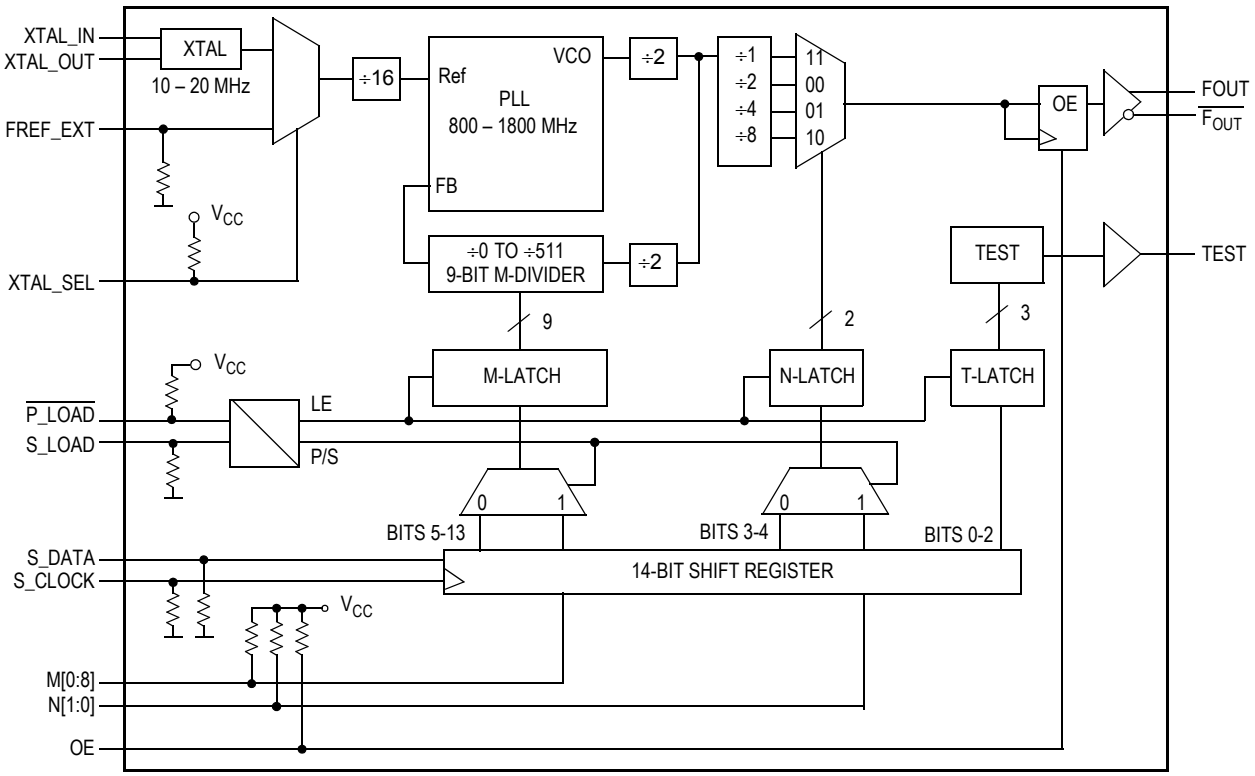


Figure 1. MPC9230 Logic Diagram

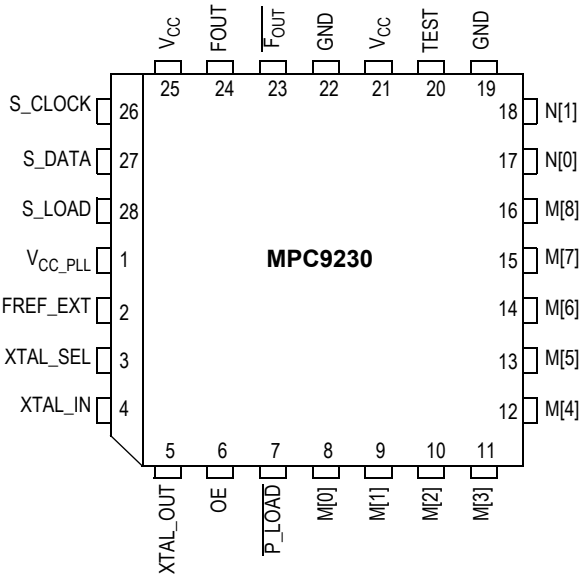


Figure 2. MPC9230 28-Lead PLCC Pinout
(Top View)

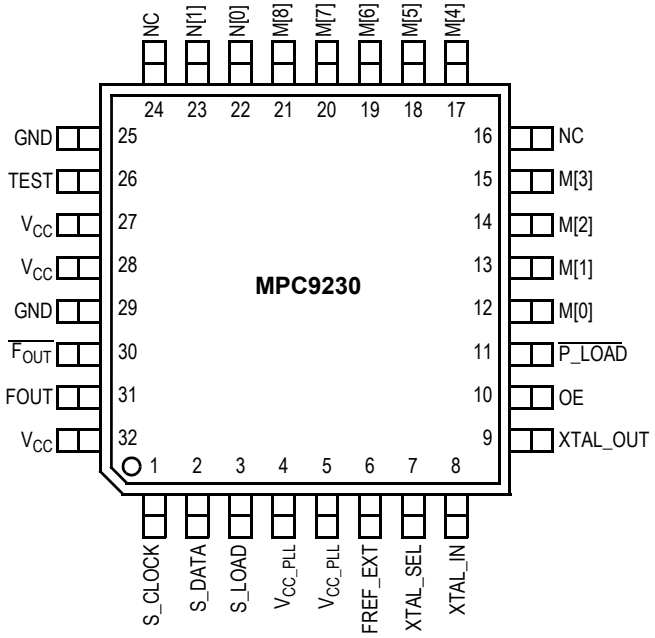


Figure 3. MPC9230 32-Lead Package Pinout
(Top View)

Table 1. Pin Configurations

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface
FREF_EXT	Input	0	LVCMOS	Alternative PLL reference input
F_{OUT}, F_{OUT}	Output		LVPECL	Differential clock output
TEST	Output		LVCMOS	Test and device diagnosis output
XTAL_SEL	Input	1	LVCMOS	PLL reference select input
S_LOAD	Input	0	LVCMOS	Serial configuration control input. This input controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
$\overline{\text{P\_LOAD}}$	Input	1	LVCMOS	Parallel configuration control input. This input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of P_LOAD. P_LOAD is state sensitive.
S_DATA	Input	0	LVCMOS	Serial configuration data input.
S_CLOCK	Input	0	LVCMOS	Serial configuration clock input.
M[0:8]	Input	1	LVCMOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of P_LOAD.
N[1:0]	Input	1	LVCMOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of P_LOAD.
OE	Input	1	LVCMOS	Output enable (active high) The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the F_{OUT} output.
GND	Supply		Ground	Negative power supply (GND).
V_{CC}	Supply		V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation.
V_{CC_PLL}	Supply		V_{CC}	PLL positive power supply (analog power supply).

Table 2. Output Frequency Range and PLL Post-Divider N

N		Output Division	Output Frequency Range for T_A = 0°C to +70°C	Output Frequency Range for T_A = –40°C to +85°C
1	0			
0	0	2	200 – 400 MHz	200 – 375 MHz
0	1	4	100 – 200 MHz	100 – 187.5 MHz
1	0	8	50 – 100 MHz	50 – 93.75 MHz
1	1	1	400 – 800 MHz	400 – 750 MHz

Table 3. Function Table

Input	0	1
XTAL_SEL	FREF_EXT	XTAL interface
OE	Outputs disabled. F_{OUT} is stopped in the logic low state (F_{OUT} = L, F_{OUT} = H)	Outputs enabled

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	4.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs (FREF_EXT, XTAL_SEL, $\overline{\text{P\_LOAD}}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1]. OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[1]			±200	μA	V_{IN} = V_{CC} or GND
Differential Clock Output F_{OUT}[2]						
V_{OH}	Output High Voltage	V_{CC}–1.02		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage	V_{CC}–1.02		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			110	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50Ω to V_{TT} = V_{CC} – 2V.

Table 7. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs (FREF_EXT, XTAL_SEL, $\overline{\text{P\_LOAD}}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1]. OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[1]			±200	μA	V_{IN} = V_{CC} or GND
Differential Clock Output F_{OUT}[2]						
V_{OH}	Output High Voltage	V_{CC}–1.1		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage	V_{CC}–1.95		V_{CC}–1.65	V	LVPECL
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage	V_{CC}–1.1		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage	V_{CC}–1.95		V_{CC}–1.65	V	LVPECL
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			110	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50Ω to V_{TT} = V_{CC} – 2V.

Table 8. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range		10		20	MHz	
f_{REF}	FREF_EXT Reference Frequency Range		10		$(f_{VCO,MAX} \div M) \cdot 4$[2]	MHz	
f_{VCO}	VCO Frequency Range[3]		800		1600	MHz	
f_{MAX}	Output Frequency	N = 11 (÷1) N = 00 (÷2) N = 01 (÷4) N = 10 (÷8)	400 200 100 50		800 400 200 100	MHz MHz MHz MHz	
f_{S_CLOCK}	Serial Interface Programming Clock Frequency[4]		0		10	MHz	
$t_{P,MIN}$	Minimum Pulse Width	(S_LOAD, $\overline{\text{P\_LOAD}}$)	50			ns	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.05		0.3	ns	20% to 80%
t_S	Setup Time	S_DATA to S_CLOCK S_CLOCK to $\overline{\text{S\_LOAD}}$ M, N to $\overline{\text{P\_LOAD}}$	20 20 20			ns ns ns	
t_H	Hold Time	S_DATA to S_CLOCK M, N to $\overline{\text{P\_LOAD}}$	20 20			ns ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	N = 11 (÷1) N = 00 (÷2) N = 01 (÷4) N = 10 (÷8)			80 90 130 160	ps ps ps ps	
$t_{JIT(PER)}$	Period Jitter	N = 11 (÷1) N = 00 (÷2) N = 01 (÷4) N = 10 (÷8)			60 70 120 140	ps ps ps ps	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. The maximum frequency on FREF_EXT is a function of the max. VCO frequency and the M counter. M should be higher than 160 for stable PLL operation.
3. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M \div 4$.
4. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See APPLICATIONS INFORMATION for more details.

Table 9. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40°C to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range		10		20	MHz	
f_{REF}	FREF_EXT Reference Frequency Range		10		$(f_{VCO,MAX} \div M) \cdot 4$[2]	MHz	
f_{VCO}	VCO Frequency Range[3]		800		1500	MHz	
f_{MAX}	Output Frequency	N = 11 (÷1) N = 00 (÷2) N = 01 (÷4) N = 10 (÷8)	400 200 100 50		750.00 375.00 187.50 93.75	MHz MHz MHz MHz	
f_{S_CLOCK}	Serial Interface Programming Clock Frequency[4]		0		10	MHz	
$t_{P,MIN}$	Minimum Pulse Width	(S_LOAD, $\overline{\text{P\_LOAD}}$)	50			ns	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.05		0.3	ns	20% to 80%
t_S	Setup Time	S_DATA to S_CLOCK S_CLOCK to $\overline{\text{S\_LOAD}}$ M, N to $\overline{\text{P\_LOAD}}$	20 20 20			ns ns ns	
t_H	Hold Time	S_DATA to S_CLOCK M, N to $\overline{\text{P\_LOAD}}$	20 20			ns ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	N = 11 (÷1) N = 00 (÷2) N = 01 (÷4) N = 10 (÷8)			80 90 130 160	ps ps ps ps	
$t_{JIT(CC)}$	Period Jitter	N = 11 (÷1) N = 00 (÷2) N = 01 (÷4) N = 10 (÷8)			60 70 120 140	ps ps ps ps	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}
2. The maximum frequency on FREF_EXT is a function of the max. VCO frequency and the M counter. M should be higher than 160 for stable PLL operation
3. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M \div 4$.
4. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See APPLICATIONS INFORMATION for more details.

PROGRAMMING INTERFACE

Programming the MPC9230

Programming the MPC9230 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$F_{OUT} = (f_{XTAL} \div 16) \cdot (4 \cdot M) \div (2 \cdot N) \text{ or} \quad (1)$$

$$F_{OUT} = (f_{XTAL} \div 8) \cdot M \div N \quad (2)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 800 to 1600 MHz in order to achieve stable PLL operation:

$$M_{MIN} = 4 \cdot f_{VCO,MIN} \div f_{XTAL} \text{ and} \quad (3)$$

$$M_{MAX} = 4 \cdot f_{VCO,MAX} \div f_{XTAL} \quad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M=200 and M = 400. Table 10 shows the usable VCO frequency and M divider range for other example input frequencies. Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$$F_{OUT} = 2 \cdot M \div N \quad (5)$$

Table 10. MPC9230 Frequency Operating Range

		VCO frequency for an crystal interface frequency of [MHz]						Output frequency for f_{XTAL}=16 MHz and for N =			
M	M[8:0]	10	12	14	16	18	20	1	2	4	8
160	010100000						800				
170	010101010						850				
180	010110100					810	900				
190	010111110					855	950				
200	011001000				800	900	1000	400	200	100	50
210	011010010				840	945	1050	420	210	105	52.5
220	011011100				880	990	1100	440	220	110	55
230	011100110			805	920	1035	1150	460	230	115	57.5
240	011110000			840	960	1080	1200	480	240	120	60
250	011111010			875	100	1125	1250	500	250	125	62.5
260	100000100			910	1040	1170	1300	520	260	130	65
270	100001110		810	945	1080	1215	1350	540	270	135	67.5
280	100011000		840	980	1120	1260	1400	560	280	140	70
290	100100010		870	1015	1160	1305	1450	580	290	145	72.5
300	100101100		900	1050	1200	1350	1500	600	300	150	75
310	100110110		930	1085	1240	1395	1550[1]	620	310	155	77.5
320	101000000	800	960	1120	1280	1440	1600[1]	640	320	160	80
330	101001010	825	990	1155	1320	1485		660	330	165	82.5
340	101010100	850	1020	1190	1360	1530[1]		680	340	170	85
350	101011110	875	1050	1225	1400	1575[1]		700	350	175	87.5
360	101101000	900	1080	1260	1440			720	360	180	90
370	101110010	925	1110	1295	1480			740	370	185	92.5
380	101111100	950	1140	1330	1520[1]			760[2]	380[2]	190[2]	95[2]
390	110000110	975	1170	1365	1560[1]			780[2]	390[2]	195[2]	97.5[2]
400	110010000	1000	1200	1400	1600[1]			800[2]	400[2]	200[2]	100[2]
410	110011010	1025	1230	1435							
420	110100100	1050	1260	1470							
430	110101110	1075	1290	1505[a]							
440	110111000	1100	1320	1540[a]							
450	111000010	1125	1350	1575[a]							

1. This VCO frequency is only available at the 0°C to +70°C temperature range.
2. This output frequency is only available at the 0°C to +70°C temperature range.

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 11. Output Frequency Range for f_{XTAL} = 16 MHz

N			F_{OUT}	Output Frequency Range for T_A = 0°C to 70°C	Output Frequency Range for T_A = –40°C to 85°C	F_{OUT} Step
1	0	Value				
0	0	2	M	200 – 400 MHz	200 – 375 MHz	1 MHz
0	1	4	M÷2	100 – 200 MHz	100 – 187.5 MHz	500 kHz
1	0	8	M÷4	50 – 100 MHz	50 – 93.75 MHz	250 kHz
1	1	1	2 · M	400 – 800 MHz	400 – 750 MHz	2 MHz

Example Frequency Calculation for an 16 MHz Input Frequency

If an output frequency of 131 MHz was desired the following steps would be taken to identify the appropriate M and N values. According to Table 11, 131 MHz falls in the frequency set by a value of 4 so N[1:0] = 01. For N = 4 the output frequency is $F_{OUT} = M \div 2$ and $M = F_{OUT} \times 2$. Therefore M = 2 x 131 = 262, so M[8:0] = 010000011. Following this procedure a user can generate any whole frequency between 50 MHz and 800 MHz. Note than for N > 2 fractional values of can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to:

$$f_{STEP} = f_{XTAL} \div 8 \div N$$

APPLICATIONS INFORMATION

Using the Parallel and Serial Interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW to HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the F_{OUT} output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC9230 synthesizer. M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the Test and Diagnosis Output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents F_{OUT}, the LVPECL compatible TEST output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis. The T2, T1 and T0 control bits are preset to '000' when P_LOAD is LOW so that the LVPECL compatible F_{OUT} outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin. Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9230 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC9230 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the F_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving F_{OUT} directly gives the user more control on the test clocks sent through the clock tree. Table 12 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the F_{OUT} pin can be toggled via the S_CLOCK is 50 MHz as the divide ratio of the Post-PLL divider is 4 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 12. Test and Debug Configuration for TEST

T[2:0]			TEST Output
T2	T1	T0	
0	0	0	14-bit shift register out[1]
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 16$
0	1	1	M-Counter out
1	0	0	F_{OUT}
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	$F_{OUT} \div 4$

1. Clocked out at this rate of S_CLOCK

Table 13. Debug Configuration for PLL Bypass[1]

Output	Configuration
F_{OUT}	S_CLOCK ÷ N
TEST	M-Counter out[2]

1. T[2:0]=110. AC specifications do not apply in PLL bypass mode
2. Clocked out at the rate of S_CLOCK÷(2·N)

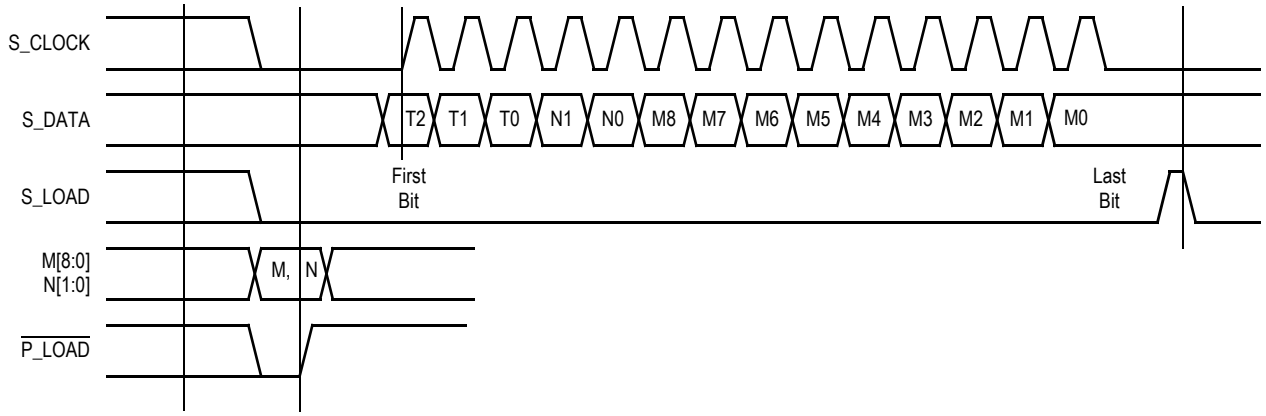


Figure 4. Serial Interface Timing Diagram

Power Supply Filtering

The MPC9230 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device characteristics. The MPC9230 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9230. Figure 5 illustrates a typical power supply filter scheme. The MPC9230 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the MPC9230 pin of the MPC9230. From the data sheet, the V_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 5 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the V_{CC_PLL} pin, a low DC resistance inductor is required (less than 15 Ω).

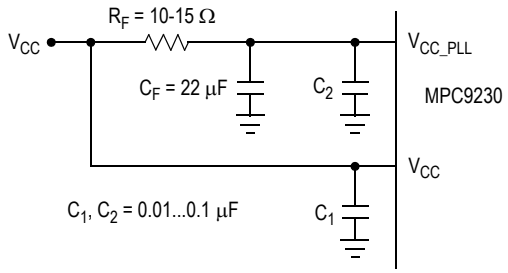


Figure 5. V_{CC_PLL} Power Supply Filter

Layout Recommendations

The MPC9230 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC9230. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC9230 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Although the MPC9230 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential

PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

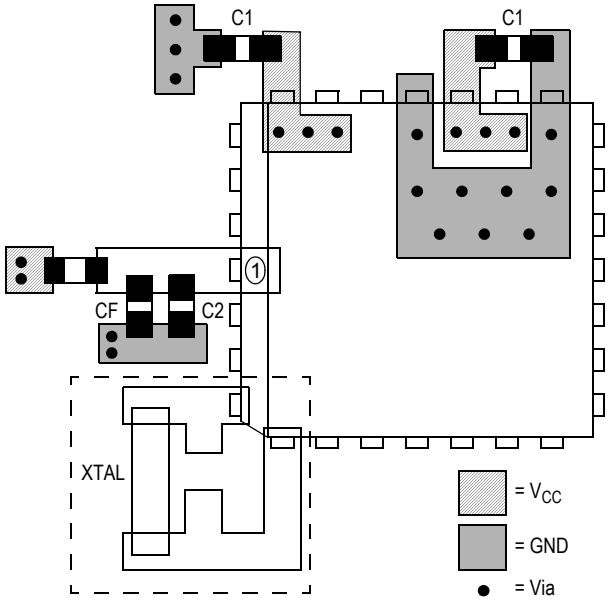


Figure 6. PCB Board Layout Recommendation for the PLCC28 Package

Using the On-Board Crystal Oscillator

The MPC9230 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC9230 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the XTAL terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1 KΩ.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MPC9230 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 14 below specifies the performance requirements of the crystals to be used with the MPC9230.

Table 14. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance[1]
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μΩ
Aging	5ppm/Yr (First 3 Years)

1. See accompanying text for series versus parallel resonant discussion.

Order number: MPC9239
Rev 2, 03/2003

900 MHz Low Voltage LVPECL Clock Synthesizer

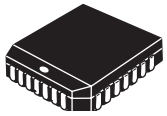
MPC9239

900 MHz LOW VOLTAGE CLOCK SYNTHESIZER

The MPC9239 is a 3.3 V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking, and computing applications. With output frequencies from 3.125 MHz to 900 MHz and the support of differential LVPECL output signals the device meets the needs of the most demanding clock applications.

Features

- 3.125 MHz to 900 MHz synthesized clock output signal
- Differential LVPECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference input
- 3.3 V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 28 PLCC and 32 LQFP packaging
- SiGe Technology
- Ambient temperature range 0°C to + 70°C
- Pin and function compatible to the MC12439



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776-02

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator or external reference clock signal is multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1800 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50 Ω to V_{CC} – 2.0 V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the $\overline{\text{P\_LOAD}}$ input LOW until power becomes valid. On the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating. The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. Refer to PROGRAMMING INTERFACE for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output. The PWR_DOWN pin, when asserted, will synchronously divide the f_{OUT} by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de-assertion of the PWR_DOWN pin, the f_{OUT} input will step back up to its programmed frequency in four discrete increments.

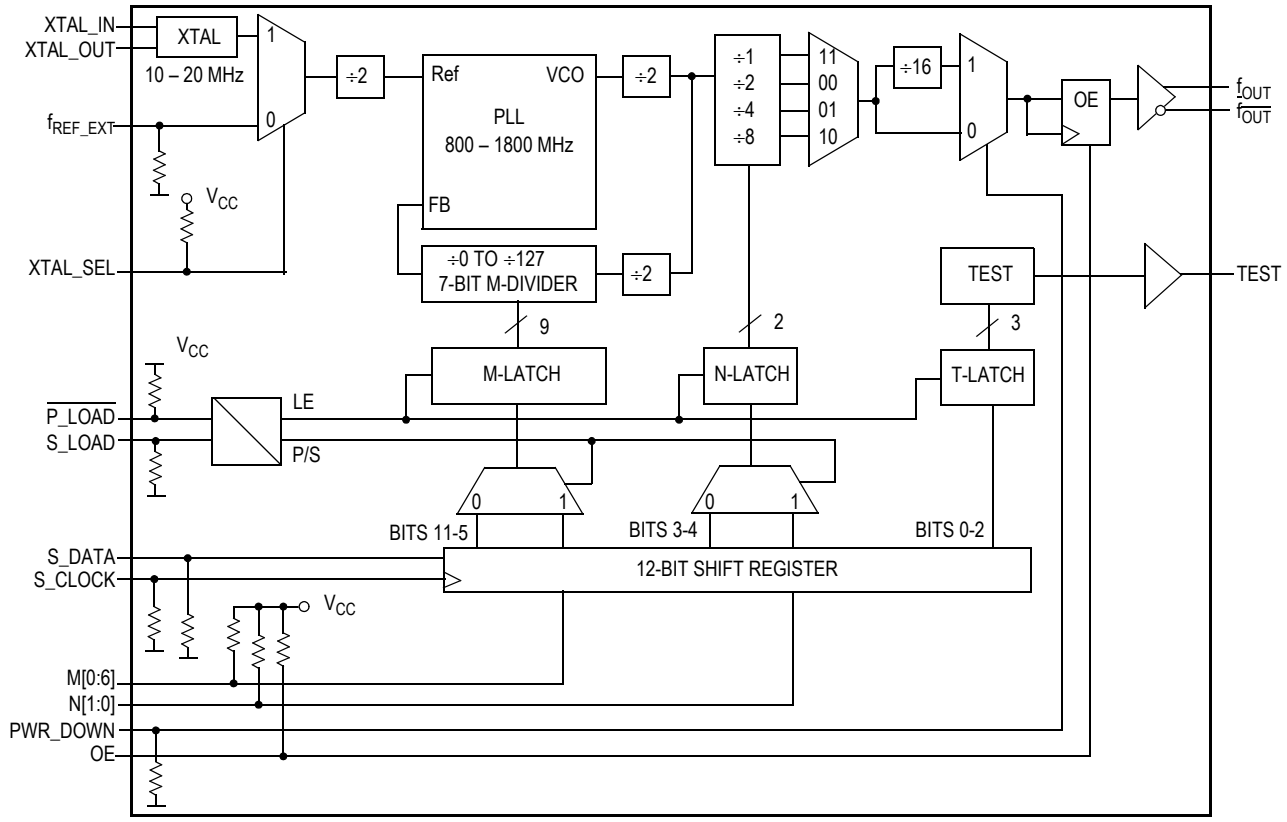


Figure 1. MPC9239 Logic Diagram

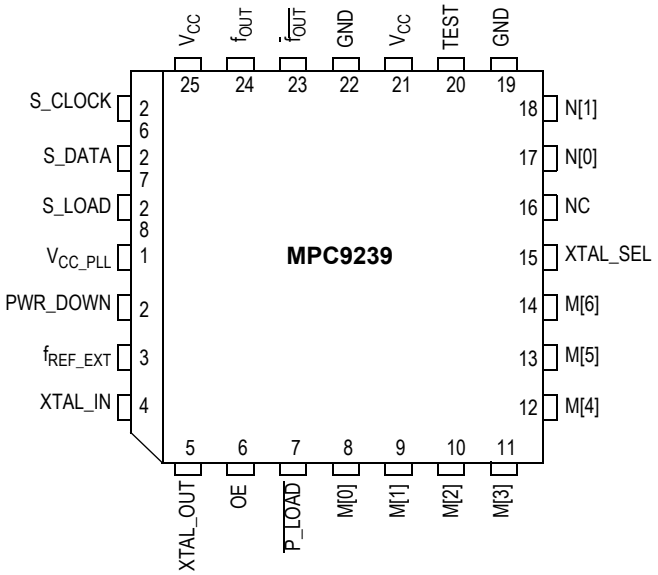


Figure 2. MPC9239 28-Lead PLCC Pinout
(Top View)

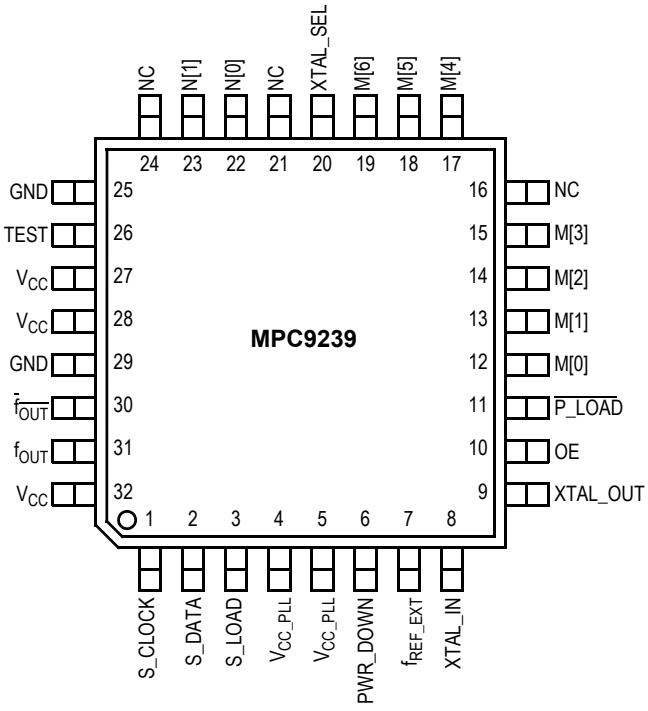


Figure 3. MPC9239 32-Lead LQFP Pinout
(Top View)

Table 1. Pin Configurations

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface.
f_{REF_EXT}	Input	0	LVCMOS	Alternative PLL reference input.
f_{OUT}, $\overline{f_{OUT}}$	Output		LVPECL	Differential clock output.
TEST	Output		LVCMOS	Test and device diagnosis output.
XTAL_SEL	Input	1	LVCMOS	PLL reference select input.
PWR_DOWN	Input	0	LVCMOS	Configuration input for power down mode. Assertion (deassertion) of power down will decrease (increase) the output frequency by a ratio of 16 in 4 discrete steps. PWR_DOWN assertion (deassertion) is synchronous to the input reference clock.
S_LOAD	Input	0	LVCMOS	Serial configuration control input. This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
$\overline{P\_LOAD}$	Input	1	LVCMOS	Parallel configuration control input. this input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of $\overline{P\_LOAD}$. $\overline{P\_LOAD}$ is state sensitive.
S_DATA	Input	0	LVCMOS	Serial configuration data input.
S_CLOCK	Input	0	LVCMOS	Serial configuration clock input.
M[0:6]	Input	1	LVCMOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of $\overline{P\_LOAD}$.
N[1:0]	Input	1	LVCMOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of $\overline{P\_LOAD}$.
OE	Input	1	LVCMOS	Output enable (active high). The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the f_{OUT} output. OE = L low stops f_{OUT} in the logic low stat (f_{OUT} = L, $\overline{f_{OUT}}$ = H).
GND	Supply		Ground	Negative power supply (GND).
V_{CC}	Supply		V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation.
V_{CC_PLL}	Supply		V_{CC}	PLL positive power supply (analog power supply).
NC				Do not connect.

Table 2. Output Frequency Range and PLL Post-Divider N

PWR_DOWN	N		VCO Output Frequency Division	f_{OUT} Frequency Range
	1	0		
0	0	0	2	200 – 450 MHz
0	0	1	4	100 – 225 MHz
0	1	0	8	50 – 112.5 MHz
0	1	1	1	400 – 900 MHz
1	0	0	32	12.5 – 28.125 MHz
1	0	1	64	6.25 – 14.0625 MHz
1	1	0	128	3.125 – 7.03125 MHz
1	1	1	16	25 – 56.25 MHz

Table 3. Function Table

Input	0	1
XTAL_SEL	f_{REF_EXT}	XTAL interface
OE	Outputs disabled. f_{OUT} is stopped in the logic low state (f_{OUT} = L, $\bar{f}_{\overline{OUT}}$ = H)	Outputs enabled
PWR_DOWN	Output divider ÷ 1	Output divider ÷ 16

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs (f_{REF_EXT}, PWR_DOWN, XTAL_SEL, $\overline{P\_LOAD}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1]. OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[1]			±200	µA	V_{IN} = V_{CC} or GND
Differential Clock Output f_{OUT}[2]						
V_{OH}	Output High Voltage[3]	V_{CC}–1.02		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage[3]	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage[3]	2.0			V	I_{OH} = –0.8 mA
V_{OL}	Output Low Voltage[3]			0.55	V	I_{OL} = 0.8 mA
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current		62	100	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50 Ω to V_{TT} = V_{CC} – 2 V.
3. The MPC9239 TEST output levels are compatible to the MC12429 output levels. The MPC9239 is capable of driving 25 Ω loads.

Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range		10		20	MHz	
f_{VCO}	VCO Frequency Range[2]		800		1800	MHz	
f_{MAX}	Output Frequency	N = 11 (÷ 1)	400		900	MHz	PWR_DOWN = 0
		N = 00 (÷ 2)	300		450	MHz	
		N = 01 (÷ 4)	100		225	MHz	
		N = 10 (÷ 8)	50		112.5	MHz	
f_{S_CLOCK}	Serial Interface Programming Clock Frequency[3]		0		10	MHz	
$t_{P,MIN}$	Minimum Pulse Width	(S_LOAD, $\overline{P\_LOAD}$)	50			ns	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.05		0.3	ns	20% to 80%
t_S	Setup Time	S_DATA to S_CLOCK	20			ns	
		S_CLOCK to $\overline{S\_LOAD}$	20			ns	
		M, N to $\overline{P\_LOAD}$	20			ns	
t_S	Hold Time	S_DATA to $\overline{S\_CLOCK}$	20			ns	
		M, N to $\overline{P\_LOAD}$	20			ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	N = 11 (÷ 1)			60	ps	
		N = 00 (÷ 2)			90	ps	
		N = 01 (÷ 4)			120	ps	
		N = 10 (÷ 8)			160	ps	
$t_{JIT(PER)}$	Period Jitter	N = 11 (÷ 1)			40	ps	
		N = 00 (÷ 2)			65	ps	
		N = 01 (÷ 4)			90	ps	
		N = 10 (÷ 8)			120	ps	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot 2 \cdot M$.
3. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. Refer to APPLICATIONS INFORMATION for more details.

Table 8. MPC9239 Frequency Operating Range (in MHz)

M	M[6:0]	VCO frequency for a crystal interface frequency of						Output frequency for f_{XTAL}=16 MHz and for N =			
		10 MHz	12 MHz	14 MHz	16 MHz	18 MHz	20 MHz	1	2	4	8
20	0010100						800				
21	0010101						840				
22	0010110						880				
23	0010111					828	920				
24	0011000					864	960				
25	0011001				800	900	1000	400	200	100	50
26	0011010				832	936	1040	416	208	104	52
27	0011011				864	972	1080	432	216	108	54
28	0011100			812	896	1008	1120	448	224	112	56
29	0011101			840	928	1044	1160	464	232	116	58
30	0011110			875	960	1080	1200	480	240	120	60
31	0011111			868	992	1116	1240	496	248	124	62
32	0100000			896	1024	1152	1280	512	256	128	64
33	0100001			924	1056	1188	1320	528	264	132	66
34	0100010		816	952	1088	1224	1360	544	272	136	68
35	0100011		840	980	1120	1260	1400	560	280	140	70
36	0100100		864	1008	1152	1296	1440	576	288	144	72
37	0100101		888	1036	1184	1332	1480	592	296	148	74
38	0100110		912	1064	1216	1368	1520	608	304	152	76
39	0100111		936	1092	1248	1404	1560	624	312	156	78
40	0101000	800	960	1120	1280	1440	1600	640	320	160	80
41	0101001	820	984	1148	1312	1476	1640	656	328	164	82
42	0101010	840	1008	1176	1344	1512	1680	672	336	168	84
43	0101011	860	1032	1204	1376	1548	1720	688	344	172	86
44	0101100	880	1056	1232	1408	1584	1760	704	352	176	88
45	0101101	900	1080	1260	1440	1620	1800	720	360	180	90
46	0101110	920	1104	1288	1472	1656		736	368	184	92
47	0101111	940	1128	1316	1504	1692		752	376	188	94
48	0110000	960	1152	1344	1536	1728		768	384	192	96
49	0110001	980	1176	1372	1568	1764		784	392	196	98
50	0110010	1000	1200	1400	1600	1800		800	400	200	100
51	0110011	1020	1224	1428	1632			816	408	204	102
52	0110100	1040	1248	1456	1664			832	416	208	104
53	0110101	1060	1272	1484	1696			848	424	212	106
54	0110110	1080	1296	1512	1728			864	432	216	108
55	0110111	1100	1320	1540	1760			880	440	220	110
56	0111000	1120	1344	1568	1792			896	448	224	112
57	0111001	1140	1368	1596							
58	0111010	1160	1392	1624							
59	0111011	1180	1416	1652							
60	0111100	1200	1440	1680							
61	0111101	1220	1488	1736							
62	0111110	1260	1512	1764							
63	0111111	1260	1512	1764							
64	1000000	1280	1536	1792							

PROGRAMMING INTERFACE

Programming the MPC9239

Programming the MPC9239 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$f_{OUT} = (f_{XTAL} \div 2) \cdot (M \cdot 4) \div (N \cdot 2) \text{ or} \quad (1)$$

$$f_{OUT} = f_{XTAL} \cdot M \div N \quad (2)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 800 to 1800 MHz in order to achieve stable PLL operation:

$$M_{MIN} = f_{VCO,MIN} \div (2 \cdot f_{XTAL}) \text{ and} \quad (3)$$

$$M_{MAX} = f_{VCO,MAX} \div (2 \cdot f_{XTAL}) \quad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M = 25 and M = 56. Table 8 shows the usable VCO frequency and M divider range for other example input frequencies.

Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$$f_{OUT} = 16\ M \div N$$

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 9. Output Frequency Range for f_{XTAL} = 10 MHz

N			f_{OUT}	f_{OUT} Range	f_{OUT} Step
1	0	Value			
0	0	2	8·M	200–450 MHz	8 MHz
0	1	4	4·M	100–225 MHz	4 MHz
1	0	8	2·M	50–112.5 MHz	2 MHz
1	1	1	16·M	400–900 MHz	16 MHz

Example Calculation for an 16 MHz Input Frequency

For example, if an output frequency of 384 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 384 MHz falls within the frequency range set by an N value of 2, so N[1:0]=00. For N = 2, f_{OUT} = 8·M, and M = $f_{OUT} \div 8$. Therefore, M = 384 ÷ 8 = 48, so M[6:0] = 0110000. Following this procedure a user can generate any whole frequency between 50 MHz and 900 MHz. The size of the programmable frequency steps will be equal to:

$$f_{STEP} = f_{XTAL} \div N$$

APPLICATIONS INFORMATION

Using the Parallel and Serial Interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW to HIGH transition will latch the information present on the M[6:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[6:0] and N[1:0] inputs will affect the f_{OUT} output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two, and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1, and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC9239 synthesizer.

M[6:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the Test and Diagnosis Output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents f_{OUT}, the LVCMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis.

The T2, T1, and T0 control bits are preset to ‘000' when P_LOAD is LOW so that the PECL f_{OUT} outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9239 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC9239 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the f_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving f_{OUT} directly gives the user more control on the test clocks sent through the clock tree shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the f_{OUT} pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 10. Test and Debug Configuration for TEST

T[2:0]			TEST Output
T2	T1	T0	
0	0	0	12-bit shift register out[1]
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 2$
0	1	1	M-Counter out
1	0	0	f_{OUT}
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	$f_{OUT} \div 4$

1. Clocked out at the rate of S_CLOCK.

Table 11. Debug Configuration for PLL Bypass[1]

Output	Configuration
f_{OUT}	S_CLOCK ÷ N
TEST	M-Counter out[2]

1. T[2:0] = 110. AC specifications do not apply in PLL bypass mode.
2. Clocked out at the rate of S_CLOCK ÷ (2 · N)

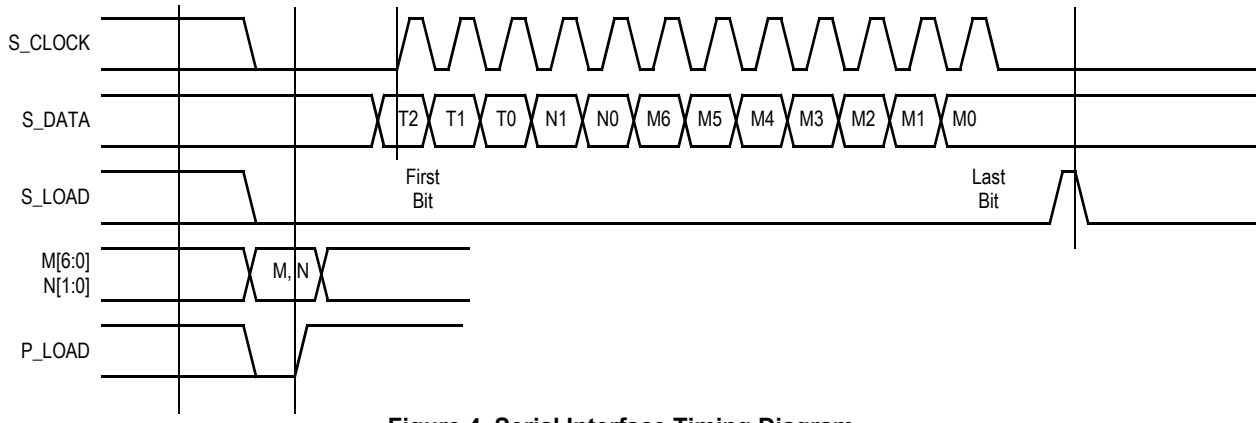


Figure 4. Serial Interface Timing Diagram

Power Supply Filtering

The MPC9239 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device characteristics. The MPC9239 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9239. Figure 5 illustrates a typical power supply filter scheme. The MPC9239 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the MPC9239 pin of the MPC9239. From the data sheet, the V_{CC_PLL}current (the current sourced through the V_{CC_PLL} pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 5 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the V_{CC_PLL} pin, a low DC resistance inductor is required (less than 15 Ω).

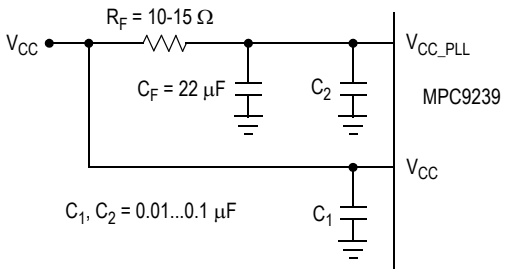


Figure 5. V_{CC_PLL} Power Supply Filter

Layout Recommendations

The MPC9239 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC9239. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC9239 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on—board oscillator. Although the MPC9239 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

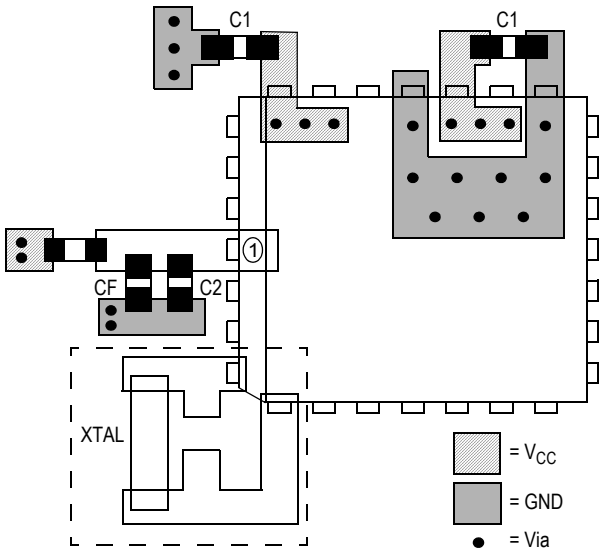


Figure 6. PCB Board Layout Recommendation for the PLCC28 Package

Using the On-Board Crystal Oscillator

The MPC9239 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC9239 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the XTAL terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1KΩ.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MPC9239 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 12 below specifies the performance requirements of the crystals to be used with the MPC9239.

Table 12. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance[1]
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5-7pF
Equivalent Series Resistance (ESR)	50 to 80 Ω
Correlation Drive Level	100 μW
Aging	5ppm/Yr (First 3 Years)

1. See accompanying text for series versus parallel resonant discussion.

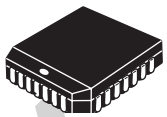
Order number: MPC92429
Rev 1, 08/2004

400 MHz Low Voltage PECL Clock Synthesizer

MPC92429

400 MHz LOW VOLTAGE CLOCK SYNTHESIZER

The MPC9429 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 25 MHz to 400 MHz and the support of differential PECL output signals the device meets the needs of the most demanding clock applications.



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776-02

FA SUFFIX
32-LEAD TQFP PACKAGE
CASE 873A-03

Features

- 25 MHz to 400 MHz synthesized clock output signal
- Differential PECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- 3.3V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 32-lead LQFP and 28-PLCC packaging
- 32-lead Pb-free package available
- SiGe Technology
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MC12429 and MPC9229

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator is divided by 16 and then multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1600 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be 4·M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1600 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50Ω to V_{CC} – 2.0V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the P_LOAD input LOW until power becomes valid. On the LOW-to-HIGH transition of P_LOAD, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See PROGRAMMING INTERFACE for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output.

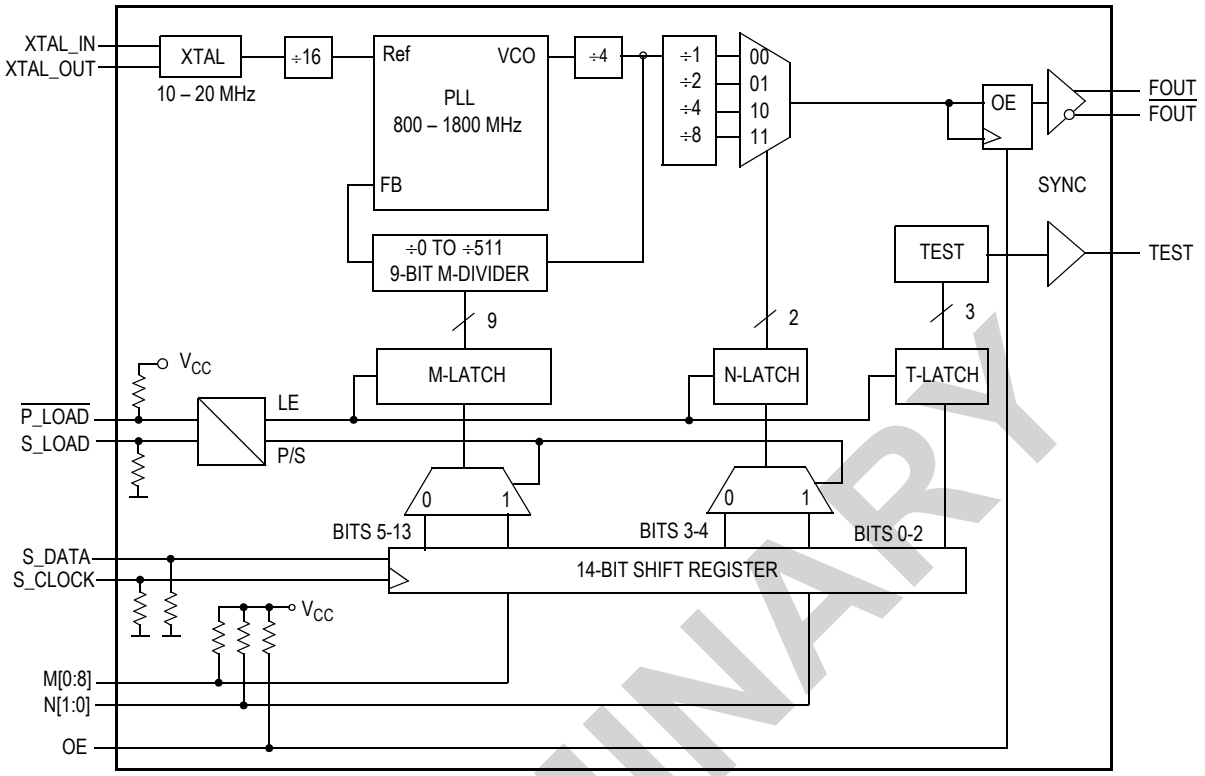


Figure 1. MPC92429 Logic Diagram

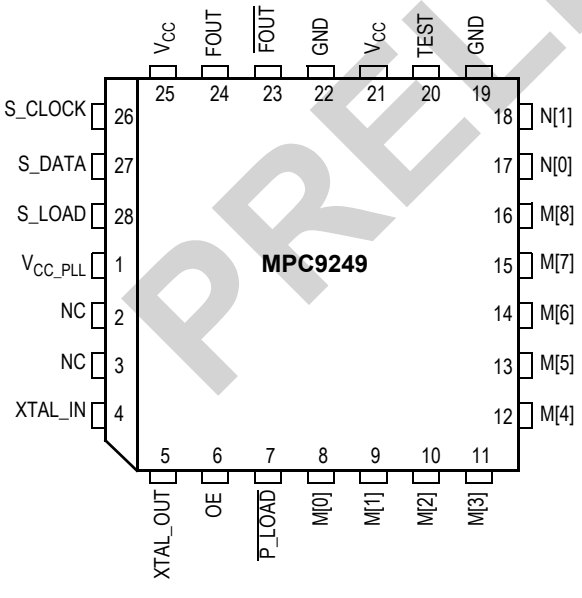


Figure 2. MPC9249 28-Lead PLCC Pinout
(Top View)

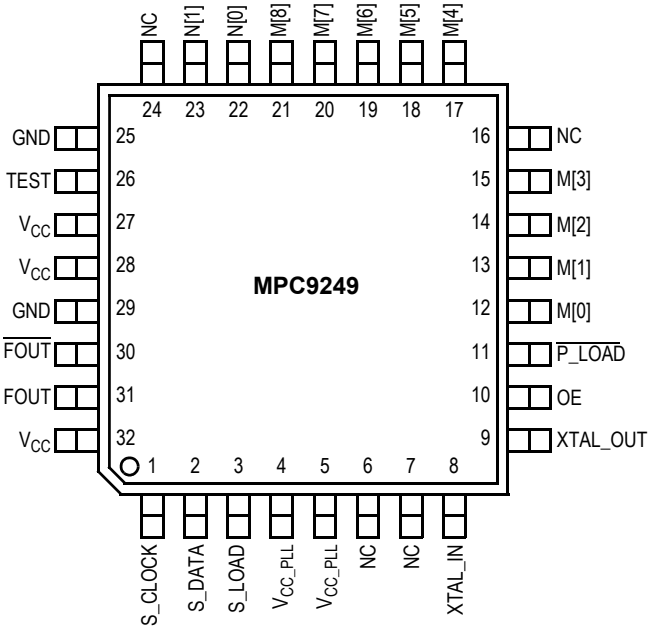


Figure 3. MPC9249 32-Lead Package Pinout
(Top View)

Table 1. Pin Configurations

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface
FOUT, $\overline{\text{FOUT}}$	Output		LVPECL	Differential clock output
TEST	Output		LVCMOS	Test and device diagnosis output
S_LOAD	Input	0	LVCMOS	Serial configuration control input. This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
$\overline{\text{P\_LOAD}}$	Input	1	LVCMOS	Parallel configuration control input. This input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of P_LOAD. P_LOAD is state sensitive
S_DATA	Input	0	LVCMOS	Serial configuration data input.
S_CLOCK	Input	0	LVCMOS	Serial configuration clock input.
M[0:8]	Input	1	LVCMOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of P_LOAD.
N[1:0]	Input	1	LVCMOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of P_LOAD
OE	Input	1	LVCMOS	Output enable (active high) The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the F_{OUT} output. OE = L low stops F_{OUT} in the logic low state (F_{OUT} = L, $\overline{\text{FOUT}}$ = H)
GND	Supply	Supply	Ground	Negative power supply (GND)
V_{CC}	Supply	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation
V_{CC_PLL}	Supply	Supply	V_{CC}	PLL positive power supply (analog power supply)

Table 2. Output Frequency Range and PLL Post-Divider N

N		Output Division	Output Frequency Range
1	**0**		
0	0	1	200 – 400 MHz
0	1	2	100 – 200 MHz
1	0	4	50 – 100 MHz
1	1	8	25 – 50 MHz

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs ($\overline{P\_LOAD}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1]. OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[1]			±200	μA	V_{IN} = V_{CC} or GND
Differential Clock Output F_{OUT}[2]						
V_{OH}	Output High Voltage[3]	V_{CC}–1.02		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage[3]	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage[3]	2.0			V	I_{OH} = –0.8 mA
V_{OL}	Output Low Voltage[3]			0.55	V	I_{OH} = 0.8 mA
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			100	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50Ω to V_{TT} = V_{CC} – 2V.
3. The MPC92429 TEST output levels are compatible to the MC12429 output levels.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range		10		20	MHz	
f_{VCO}	VCO Frequency Range[2]		200		1600	MHz	
f_{MAX}	Output Frequency	N = 00 (÷1) N = 01 (÷2) N = 10 (÷4) N = 11 (÷8)	200 100 50 25		400 200 100 50	MHz MHz MHz MHz	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.05		0.3	ns	20% to 80%
f_{S_CLOCK}	Serial Interface Programming Clock Frequency[3]		0		10	MHz	
$t_{P,MIN}$	Minimum pulse width	(S_LOAD, $\overline{\text{P\_LOAD}}$)	50			ns	
t_S	Setup Time	S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to $\overline{\text{P\_LOAD}}$	20 20 20			ns ns ns	
t_S	Hold Time	S_DATA to S_CLOCK M, N to $\overline{\text{P\_LOAD}}$	20 20			ns ns	
$t_{JIT(CC)}$	Cycle-to-Cycle jitter	N = 00 (÷1) N = 01 (÷2) N = 10 (÷4) N = 11 (÷8)			90 130 160 190	ps ps ps ps	
$t_{JIT(PER)}$	Period Jitter	N = 00 (÷1) N = 01 (÷2) N = 10 (÷4) N = 11 (÷8)			70 120 140 170	ps ps ps ps	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \times M \div 4$.
3. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See APPLICATIONS INFORMATION for more details.

PROGRAMMING INTERFACE

Programming the MPC92429

Programming the MPC92429 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$F_{OUT} = (f_{XTAL} \div 16) \times (M) \div (N) \quad (1)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 200 to 400 MHz in order to achieve stable PLL operation:

$$M_{MIN} = f_{VCO,MIN} \div f_{XTAL} \text{ and} \quad (2)$$

$$M_{MAX} = f_{VCO,MAX} \div f_{XTAL} \quad (3)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M = 200 and M = 400. Table 7 shows the usable VCO frequency and M divider range for other example input frequencies. Assuming that a 16 MHz input frequency is used, equation 1 reduces to:

$$F_{OUT} = M \div N \quad (4)$$

Table 7. MPC9230 Frequency Operating Range

M	M[8:0]	VCO frequency for an crystal interface frequency of						Output frequency for f_{XTAL} = 16 MHz and for N =			
		10	12	14	16	18	20	1	2	4	16
160	010100000						800				
170	010101010						850				
180	010110100					810	900				
190	010111110					855	950				
200	011001000				800	900	1000	200	100	50	25
210	011010010				840	945	1050	210	105	52.5	26.25
220	011011100				880	990	1100	220	110	55	27.50
230	011100110			805	920	1035	1150	230	115	57.5	28.75
240	011110000			840	960	1080	1200	240	120	60	30
250	011111010			875	100	1125	1250	250	125	62.5	31.25
260	100000100			910	1040	1170	1300	260	130	65	32.50
270	100001110		810	945	1080	1215	1350	270	135	67.5	33.75
280	100011000		840	980	1120	1260	1400	280	140	70	35
290	100100010		870	1015	1160	1305	1450	290	145	72.5	36.25
300	100101100		900	1050	1200	1350	1500	300	150	75	37.5
310	100110110		930	1085	1240	1395	1550	310	155	77.5	38.75
320	101000000	800	960	1120	1280	1440	1600	320	160	80	40
330	101001010	825	990	1155	1320	1485		330	165	82.5	41.25
340	101010100	850	1020	1190	1360	1530		340	170	85	42.5
350	101011110	875	1050	1225	1400	1575		350	175	87.5	43.75
360	101101000	900	1080	1260	1440			360	180	90	45
370	101110010	925	1110	1295	1480			370	185	92.5	46.25
380	101111100	950	1140	1330	1520			380	190	95	47.5
390	110000110	975	1170	1365	1560			390	195	97.5	48.75
400	110010000	1000	1200	1400	1600			400	200	100	50
410	110011010	1025	1230	1435							
420	110100100	1050	1260	1470							
430	110101110	1075	1290	1505							
440	110111000	1100	1320	1540							
450	111000010	1125	1350	1575							
510	111111110	1275	1530								

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 8. Output Frequency Range for f_{XTAL} = 16 MHz

N			F_{OUT}	F_{OUT} Range	F_{OUT} Step
1	0	Value			
0	0	1	M	200 – 400 MHz	1 MHz
0	1	2	M÷2	100 – 200 MHz	500 kHz
1	0	4	M÷4	50 – 100 MHz	250 kHz
1	1	8	M÷8	25 – 50 MHz	125 kHz

Example Frequency Calculation for an 16 MHz Input Frequency

If an output frequency of 131 MHz was desired the following steps would be taken to identify the appropriate M and N values. According to Table 8, 131 MHz falls in the frequency set by an value of 2 so N[1:0] = 01. For N = 2 the output frequency is $F_{OUT} = M \div 2$ and $M = F_{OUT} \times 2$. Therefore M = 2 x 131 = 262, so M[8:0] = 100000110. Following this procedure a user can generate any whole frequency between 25 MHz and 400 MHz. Note than for N > 2 fractional values of can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to:

$$f_{STEP} = f_{XTAL} \div 16 \div N \quad (5)$$

APPLICATIONS INFORMATION

Using the Parallel and Serial Interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW-to-HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH-to-LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC9229 synthesizer. M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the Test and Diagnosis Output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents F_{OUT}, the CMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis. The T2, T1 and T0 control bits are preset to '000' when P_LOAD is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin. Most of the signals available on the TEST output pin are useful only for performance verification of the MPC9229 itself. However the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC9229 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the F_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving F_{OUT} directly gives the user more control on the test clocks sent through the clock tree. Figure 6 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the F_{OUT} pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 9. Test and Debug Configuration for TEST

T[2:0]			TEST Output
T2	T1	T0	
0	0	0	14-bit shift register out[1]
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 16$
0	1	1	M-Counter out
1	0	0	FOUT
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	FOUT ÷ 4

1. Clocked out at the rate of S_CLOCK.

Table 10. Debug Configuration for PLL Bypass[1]

Output	Configuration
F_{OUT}	S_CLOCK ÷ N
TEST	M-Counter out[2]

1. T[2:0] = 110. AC specifications do not apply in PLL bypass mode.
2. Clocked out at the rate of S_CLOCK÷(4·N)

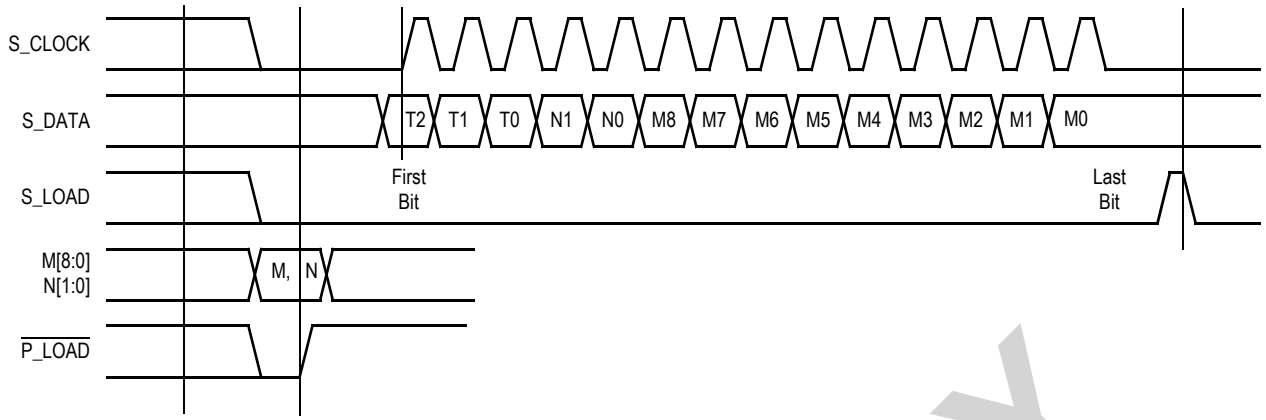


Figure 4. Serial Interface Timing Diagram

Power Supply Filtering

The MPC9229 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device characteristics. The MPC9229 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9229. Figure 5 illustrates a typical power supply filter scheme. The MPC9229 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the MPC9229 pin of the MPC9229. From the data sheet, the V_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 5 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the V_{CC_PLL} pin, a low DC resistance inductor is required (less than 15 Ω).

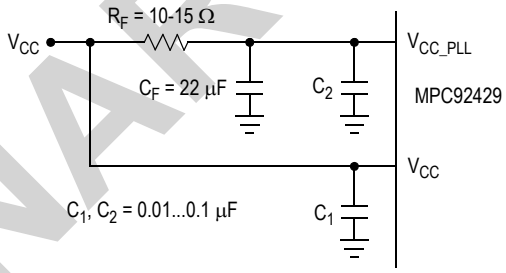


Figure 5. V_{CC_PLL} Power Supply Filter

Layout Recommendations

The MPC9229 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC9229. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC9229 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Although the MPC9229 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential

PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

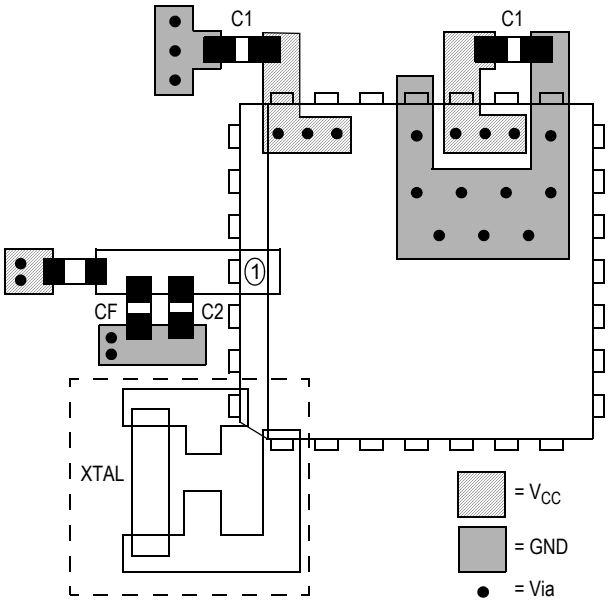


Figure 6. PCB Board Layout Recommendation for the PLCC28 Package

Using the On-Board Crystal Oscillator

The MPC9229 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC9229 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the XTAL terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1KΩ.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MPC9229 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 11 below specifies the performance requirements of the crystals to be used with the MPC9229.

Table 11. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance[1]
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5–7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

1. See accompanying test for series versus parallel resonant discussion.

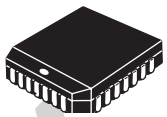
Order number: MPC92430
Rev 1, 08/2004

800 MHz Low Voltage PECL Clock Synthesizer

MPC92430

800 MHz LOW VOLTAGE CLOCK SYNTHESIZER

The MPC92430 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 50 MHz to 800 MHz and the support of differential PECL output signals the device meets the needs of the most demanding clock applications.



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776-02

FA SUFFIX
32-LEAD TQFP PACKAGE
CASE 873A-03

Features

- 50 MHz to 800 MHz synthesized clock output signal
- Differential PECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference clock input
- 3.3V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 32-lead LQFP and 28-PLCC packaging
- 32-lead Pb-free package available
- SiGe Technology
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MC12430 and MPC9230

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator is divided by 16 and then multiplied by the PLL. The VCO within the PLL operates over a range of 400 to 800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be 2·M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (400 to 800 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50Ω to V_{CC} – 2.0V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[8:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the P_LOAD input LOW until power becomes valid. On the LOW-to-HIGH transition of P_LOAD, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[8:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating.

The serial interface centers on a fourteen bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See PROGRAMMING INTERFACE for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output.

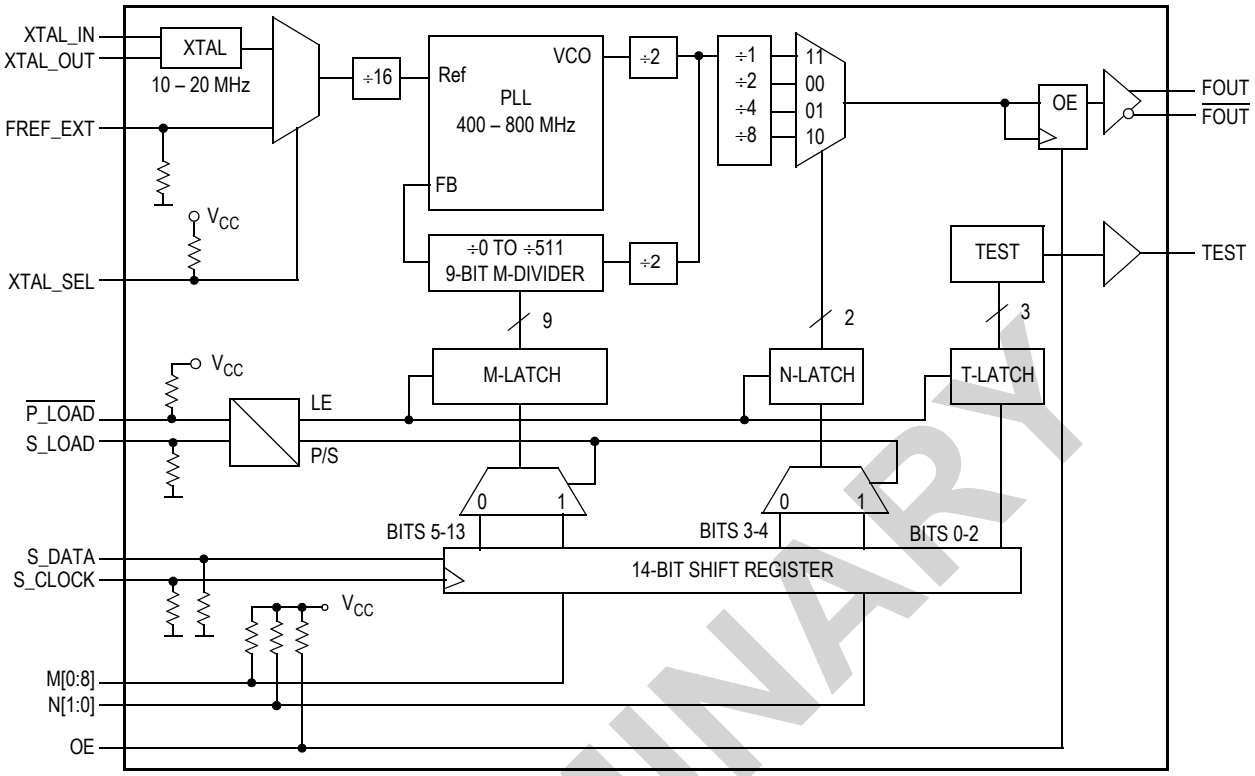


Figure 1. MPC92429 Logic Diagram

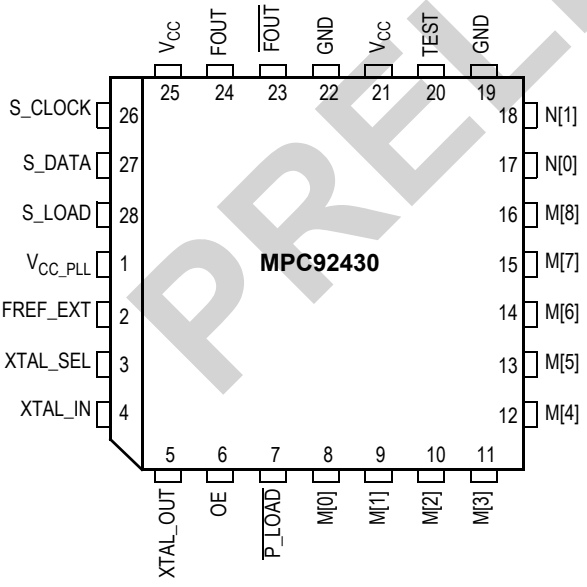


Figure 2. MPC92430 28-Lead PLCC Pinout
(Top View)

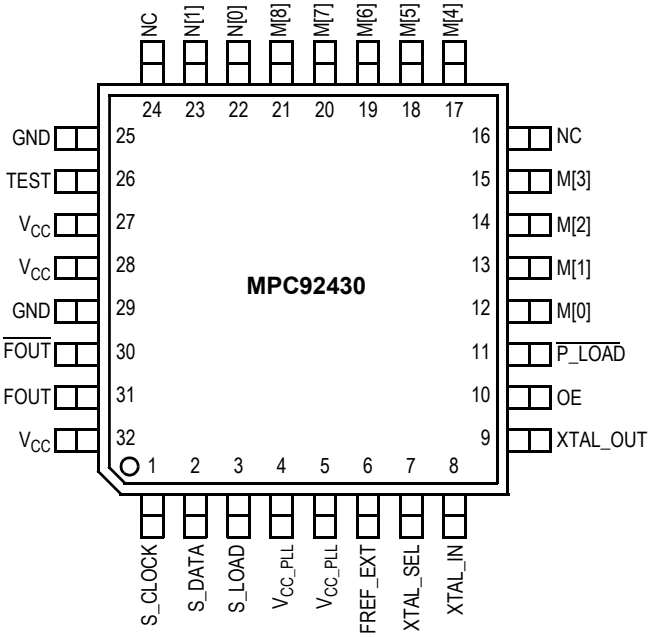


Figure 3. MPC92430 32-Lead Package Pinout
(Top View)

Table 1. Pin Configurations

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface
FREF_EXT	Input	0	LVCMOS	Alternative PLL reference input
FOUT, $\overline{\text{FOUT}}$	Output		LVPECL	Differential clock output
TEST	Output		LVCMOS	Test and device diagnosis output
XTAL_SEL	Input	1	LVCMOS	PLL reference select input
S_LOAD	Input	0	LVCMOS	Serial configuration control input. This input controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
$\overline{\text{P\_LOAD}}$	Input	1	LVCMOS	Parallel configuration control input. This input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of P_LOAD. $\overline{\text{P\_LOAD}}$ is state sensitive
S_DATA	Input	0	LVCMOS	Serial configuration data input.
S_CLOCK	Input	0	LVCMOS	Serial configuration clock input.
M[0:8]	Input	1	LVCMOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
N[1:0]	Input	1	LVCMOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$
OE	Input	1	LVCMOS	Output enable (active high) The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the F_{OUT} output.
GND	Supply	Supply	Ground	Negative power supply (GND)
V_{CC}	Supply	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation
V_{CC_PLL}	Supply	Supply	V_{CC}	PLL positive power supply (analog power supply)

Table 2. Output Frequency Range and PLL Post-Divider N

N		Output Division	Output Frequency Range
1	**0**		
0	0	2	200 – 400 MHz
0	1	4	100 – 200 MHz
1	0	8	50 – 100 MHz
1	1	1	400 – 800 MHz

Table 3. Function Table

Input	0	1
XTAL_SEL	FREF_EXT	XTAL interface
OE	Outputs disabled, FOUT is stopped in the logic low state (FOUT = L, $\overline{\text{FOUT}}$ = H)	Outputs enabled

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs (FREF_EXT, XTAL_SEL, $\overline{\text{P\_LOAD}}$, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1]. OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[1]			±200	µA	V_{IN} = V_{CC} or GND
Differential Clock Output F_{OUT}[2]						
V_{OH}	Output High Voltage	V_{CC}–1.02		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage	V_{CC}–1.02		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			100	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50Ω to V_{TT} = V_{CC} – 2V.

Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range	10		20	MHz	
f_{REF}	FREF_EXT Reference Frequency Range	10		$(f_{VCO,MAX} \div M) \cdot 2$[2]	MHz	
f_{VCO}	VCO Frequency Range[3]	400		800	MHz	
f_{MAX}	Output Frequency N = 11 (÷1) N = 00 (÷2) N = 01 (÷4) N = 10 (÷8)	400 200 100 50		800 400 200 100	MHz MHz MHz MHz	
f_{S_CLOCK}	Serial Interface Programming Clock Frequency[4]	0		10	MHz	
$f_{P,MIN}$	Minimum Pulse Width (S-LOAD, $\overline{\text{P\_LOAD}}$)	50			ns	
DC	Output Duty Cycle	45	50	55	%	
t_r, t_f	Output Rise/Fall Time	0.05		0.3	ns	20% to 80%
t_S	Setup Time S_DATA to S_CLOCK S_CLOCK to $\overline{\text{S\_LOAD}}$ M, N to $\overline{\text{P\_LOAD}}$	20 20 20			ns ns ns	
t_H	Hold Time S_DATA to S_CLOCK M, N to $\overline{\text{P\_LOAD}}$	20 20			ns ns	
$t_{JIT(PER)}$	Period Jitter			25	ps	
t_{LOCK}	Maximum PLL Lock Time			10	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. The maximum frequency of FREF_EXT is a function of the max. VCO frequency and the M counter. M should be higher than 160 for stable PLL operation.
3. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M \div 4$.
4. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See APPLICATIONS INFORMATION for more details.

PROGRAMMING INTERFACE

Programming the MPC92430

Programming the MPC92430 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$f_{OUT} = (f_{XTAL} \div 16) \cdot (2 \cdot M) \div (N) \text{ or} \quad (1)$$

$$f_{OUT} = (f_{XTAL} \div 8) \cdot M \div N \quad (2)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 400 to 800 MHz in order to achieve stable PLL operation:

$$M_{MIN} = 2 \cdot f_{VCO,MIN} \div f_{XTAL} \text{ and} \quad (3)$$

$$M_{MAX} = 2 \cdot f_{VCO,MAX} \div f_{XTAL} \quad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M = 200 and M = 400. Table 8 shows the usable VCO frequency and M divider range for other example input frequencies. Assuming that a 16 MHz input frequency is used, equation "$f_{OUT} = (f_{XTAL} \div 8) \cdot M \div N$ (2)" reduces to:

$$f_{OUT} = 2 \cdot M \div N \quad (5)$$

Table 8. MPC92430 Frequency Operating Range

		VCO frequency for an crystal interface frequency of						Output frequency for f_{XTAL} = 16 MHz and for N =			
M	**M[8:0]**	**10**	**12**	**14**	**16**	**18**	**20**	**1**	**2**	**4**	**8**
160	010100000						800				
170	010101010						850				
180	010110100					810	900				
190	010111110					855	950				
200	011001000				800	900	1000	400	200	100	50
210	011010010				840	945	1050	420	210	105	52.5
220	011011100				880	990	1100	440	220	110	55
230	011100110			805	920	1035	1150	460	230	115	57.5
240	011110000			840	960	1080	1200	480	240	120	60
250	011111010			875	100	1125	1250	500	250	125	62.5
260	100000100			910	1040	1170	1300	520	260	130	65
270	100001110		810	945	1080	1215	1350	540	270	135	67.5
280	100011000		840	980	1120	1260	1400	560	280	140	70
290	100100010		870	1015	1160	1305	1450	580	290	145	72.5
300	100101100		900	1050	1200	1350	1500	600	300	150	75
310	100110110		930	1085	1240	1395	1550	620	310	155	77.5
320	101000000	800	960	1120	1280	1440	1600	640	320	160	80
330	101001010	825	990	1155	1320	1485		660	330	165	82.5
340	101010100	850	1020	1190	1360	1530		680	340	170	85
350	101011110	875	1050	1225	1400	1575		700	350	175	87.5
370	101110010	925	1110	1295	1480			740	370	185	92.5
380	101111100	950	1140	1330	1520			760	380	190	95
390	110000110	975	1170	1365	1560			780	390	195	97.5
400	110010000	1000	1200	1400	1600			800	400	200	100
410	110011010	1025	1230	1435							
420	110100100	1050	1260	1470							
430	110101110	1075	1290	1505							
440	110111000	1100	1320	1540							
450	111000010	1125	1350	1575							
510	111111110	1275	1530								

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 9. Output Frequency Range for f_{XTAL} = 16 MHz

N			F_{OUT}	F_{OUT} Range	F_{OUT} Step
1	0	Value			
0	0	2	M	200 – 400 MHz	1 MHz
0	1	4	M÷2	100 – 200 MHz	500 kHz
1	0	8	M÷4	50 – 100 MHz	250 kHz
1	1	1	2 · M	400 – 800 MHz	2 MHz

Example Frequency Calculation for an 16 MHz Input Frequency

If an output frequency of 131 MHz was desired the following steps would be taken to identify the appropriate M and N values. According to Table 9, 131 MHz falls in the frequency set by a value of 4 so N[1:0] = 01. For N = 4 the output frequency is $F_{OUT} = M \div 2$ and $M = F_{OUT} \times 2$. Therefore, M = 2 x 131 = 262, so M[8:0] = 010000011. Following this procedure a user can generate any whole frequency between 50 MHz and 800 MHz. Note than for N > 2 fractional values of can be realized. The size of the programmable frequency steps (and thus the indicator of the fractional output frequencies achievable) will be equal to:

$$f_{STEP} = f_{XTAL} \div 8 \div N \quad (6)$$

APPLICATIONS INFORMATION

Using the Parallel and Serial Interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW-to-HIGH transition will latch the information present on the M[8:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[8:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 14 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M8). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC92430 synthesizer. M[8:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the Test and Diagnosis Output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents F_{OUT}, the LVPECL compatible TEST output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis. The T2, T1 and T0 control bits are preset to '000' when P_LOAD is LOW so that the LVPECL compatible FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin. Most of the signals available on the TEST output pin are useful only for performance verification of the MPC92430 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC92430 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the F_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving F_{OUT} directly gives the user more control on the test clocks sent through the clock tree. Table 10 shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the F_{OUT} pin can be toggled via the S_CLOCK is 50 MHz as the divide ratio of the Post-PLL divider is 4 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 10. Test and Debug Configuration for TEST

T[2:0]			TEST Output
T2	T1	T0	
0	0	0	14-bit shift register out[1]
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 16$
0	1	1	M-Counter out
1	0	0	FOUT
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	FOUT ÷ 4

1. Clocked at the rate of S_CLOCK

Table 11. Debug Configuration for PLL Bypass[1]

Output	Configuration
F_{OUT}	S_CLOCK ÷ N
TEST	M-Counter out[2]

1. T[2:0]=110. AC specifications do not apply in PLL bypass mode
2. Clocked out at the rate of S_CLOCK÷(2·N)

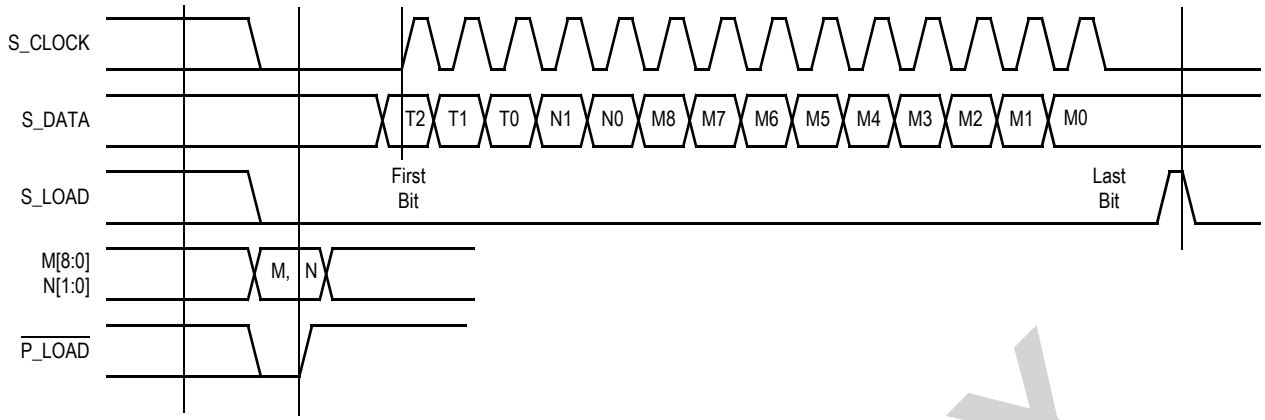


Figure 4. Serial Interface Timing Diagram

Power Supply Filtering

The MPC92430 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device characteristics. The MPC92430 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC92430. Figure 5 illustrates a typical power supply filter scheme. The MPC92430 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the MPC92430 pin of the MPC92430. From the data sheet, the V_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 5 must have a resistance of 10-15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the V_{CC_PLL} pin, a low DC resistance inductor is required (less than 15 Ω).

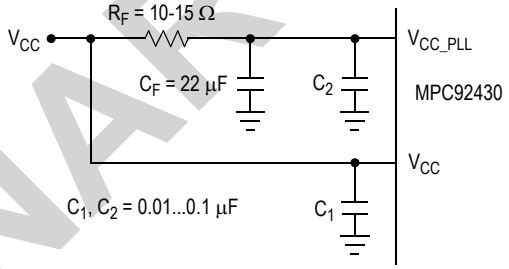


Figure 5. V_{CC_PLL} Power Supply Filter

Layout Recommendations

The MPC92430 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC92430. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between V_{CC} and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC92430 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Although the MPC92430 has several design features to minimize the susceptibility to power supply noise (isolated

power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

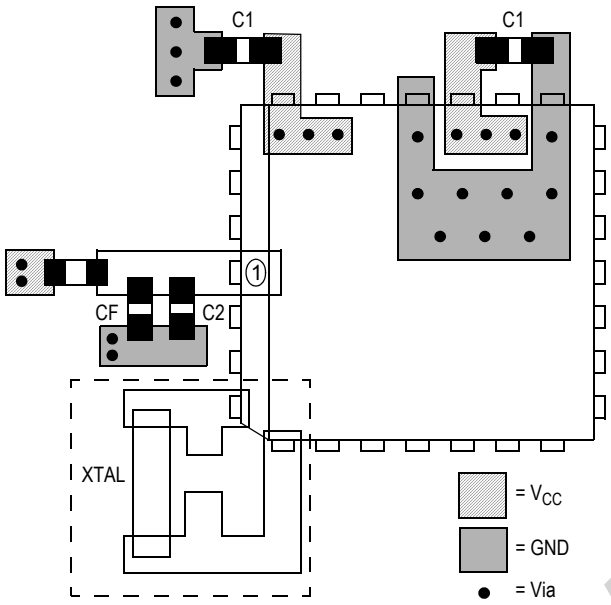


Figure 6. PCB Board Layout Recommendation for the PLCC28 Package

Using the On-Board Crystal Oscillator

The MPC92430 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC92430 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the xtal terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1KΩ.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MPC92430 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 12 below specifies the performance requirements of the crystals to be used with the MPC92430.

Table 12. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance[1]
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5-7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

1. See accompanying text for series versus parallel resonant discussion.

Order number: MPC92432
Rev 1, 08/2004

Product Preview

1360 MHz Dual Output LVPECL Clock Synthesizer

MPC92432

1360 MHz LOW VOLTAGE CLOCK SYNTHESIZER

FA SUFFIX
48-LEAD LQFP PACKAGE
CASE 932-03

The MPC92432 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking, and computing applications. With output frequencies from 21.25 MHz to 1360 MHz and the support of two differential PECL output signals, the device meets the needs of the most demanding clock applications.

Features

- 21.25 MHz to 1360 MHz synthesized clock output signal
- Two differential, LVPECL-compatible high-frequency outputs
- Output frequency programmable through 2-wire I^2C bus or parallel interface
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference clock input
- Synchronous clock stop functionality for both outputs
- LOCK indicator output (LVCMOS)
- LVCMOS compatible control inputs
- Fully integrated PLL
- 3.3-V power supply
- 48-lead LQFP
- SiGe Technology
- Ambient temperature range: –40°C to +85°C

Applications

- Programmable clock source for server, computing, and telecommunication systems
- Frequency margining
- Oscillator replacement

Functional Description

The MPC92432 is a programmable high-frequency clock source (clock synthesizer). The internal PLL generates a high-frequency output signal based on a low-frequency reference signal. The frequency of the output signal is programmable and can be changed on the fly for frequency margining purpose.

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. Alternatively, a LVCMOS compatible clock signal can be used as a PLL reference signal. The frequency of the internal crystal oscillator is divided by a selectable divider and then multiplied by the PLL. The VCO within the PLL operates over a range of 1360 to 2720 MHz. Its output is scaled by a divider that is configured by either the I^2C or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL pre-divider P, the feedback-divider M, and the PLL post-divider N determine the output frequency. The feedback path of the PLL is internal.

The PLL post-divider N is configured through either the I^2C or the parallel interfaces, and can provide one of six division ratios (2, 4, 8, 16, 32, 64). This divider extends the performance of the part while providing a 50% duty cycle. The high-frequency outputs, Q_A and Q_B, are differential and are capable of driving a pair of transmission lines terminated 50 Ω to V_{CC} – 2.0 V. The second high-frequency output, Q_B, can be configured to run at either 1x or 1/2x of the clock frequency or the first output (Q_A). The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: I^2C and parallel. The parallel interface uses the values at the M[9:0], NA[2:0], NB, and P parallel inputs to configure the internal PLL dividers. The parallel programming interface has priority over the serial I^2C interface. The serial interface is I^2C compatible and provides read and write access to the internal PLL configuration registers. The lock state of the PLL is indicated by the LVCMOS-compatible LOCK outputs.

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

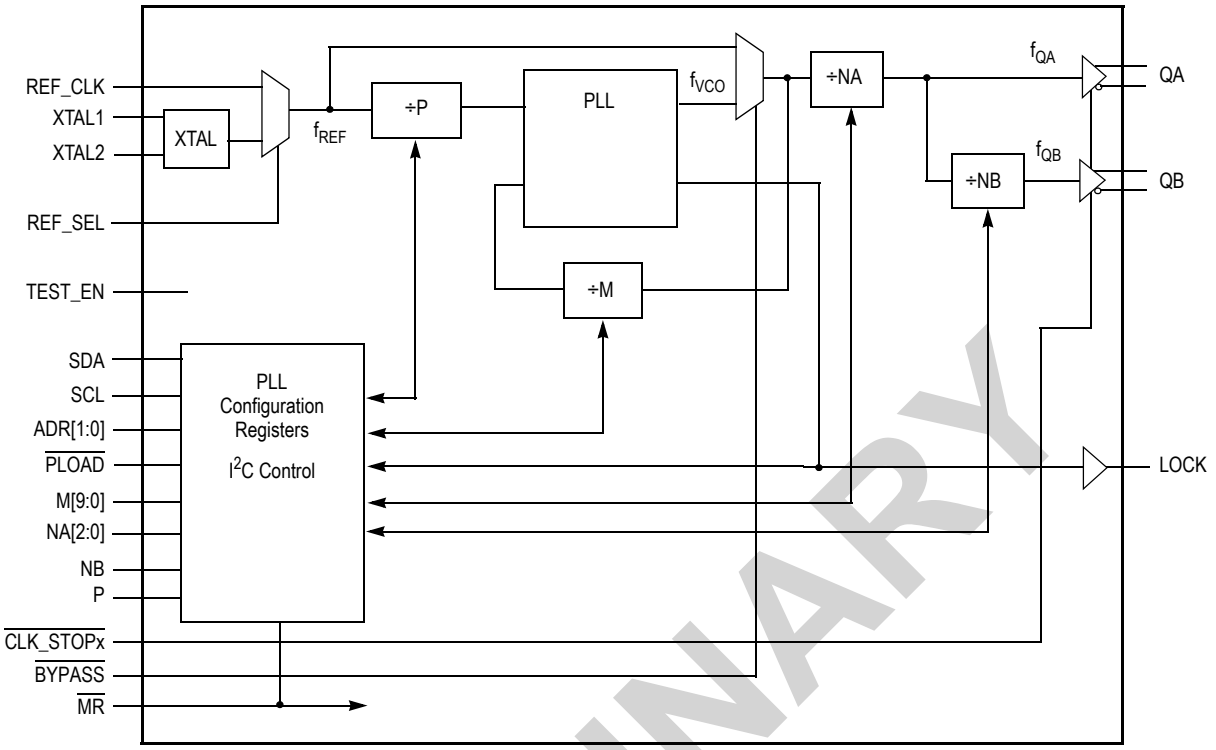
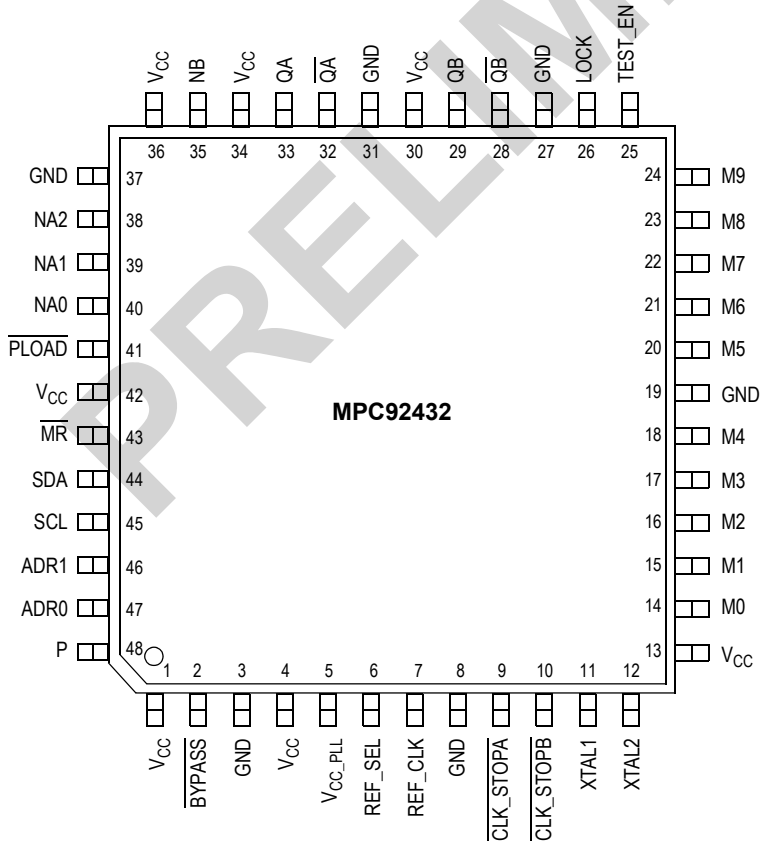


Figure 1. MPC92432 — Generic Logic Diagram



It is recommended to use an external RC filter for the analog V_{CC_PLL} supply pin. Please see the application section for details.

Figure 2. 48-Lead Package Pinout (Top View)

Table 1. Signal Configuration

Pin	I/O	Type	Function
XTAL1, XTAL2	Input	Analog	Crystal oscillator interface
REF_CLK	Input	LVCMOS	PLL external reference input
REF_SEL	Input	LVCMOS	Selects the reference clock input
QA	Output	Differential LVPECL	High frequency clock output
QB	Output	Differential LVPECL	High frequency clock output
LOCK	Output	LVCMOS	PLL lock indicator
M[9:0]	Input	LVCMOS	PLL feedback divider configuration
NA[2:0]	Input	LVCMOS	PLL post-divider configuration for output QA
NB	Input	LVCMOS	PLL post-divider configuration for output QB
P	Input	LVCMOS	PLL pre-divider configuration
$\overline{\text{P\_LOAD}}$	Input	LVCMOS	Selects the programming interface
SDA	I/O	LVCMOS	I^2C data
SCL	Input	LVCMOS	I^2C clock
ADR[1:0]	Input	LVCMOS	Selectable two bits of the I^2C slave address
$\overline{\text{BYPASS}}$	Input	LVCMOS	Selects the static circuit bypass mode
TEST_EN	Input	LVCMOS	Factory test mode enable. This input must be set to logic low level in all applications of the device.
$\overline{\text{CLK\_STOPx}}$	Input	LVCMOS	Output Qx disable in logic low state
$\overline{\text{MR}}$	Input	LVCMOS	Device master reset
GND	Supply	Ground	Negative power supply
V_{CC_PLL}	Supply	V_{CC}	Positive power supply for the PLL (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default[1]	0	1
Inputs			
REF_SEL	1	Selects REF_CLK input as PLL reference clock	Selects the XTAL interface as PLL reference clock
M[9:0]	01 1111 0100b[2]	PLL feedback divider (10-bit) parallel programming interface	
NA[2:0]	010	PLL post-divider parallel programming interface. See Table 9	
NB	0	PLL post-divider parallel programming interface. See Table 10	
P	1	PLL pre-divider parallel programming interface. See Table 8	
$\overline{\text{PLOAD}}$	0	Selects the parallel programming interface. The internal PLL divider settings (M, NA, NB and P) are equal to the setting of the hardware pins. Leaving the M, NA, NB and P pins open (floating) results in a default PLL configuration with f_{OUT} = 250 MHz. See application/programming section.	Selects the serial (I^2C) programming interface. The internal PLL divider settings (M, NA, NB and P) are set and read through the serial interface.
ADR[1:0]	00	Address bit = 0	Address bit = 1
SDA, SCL		See Programming the MPC92432	
$\overline{\text{BYPASS}}$	1	PLL function bypassed $f_{QA}=f_{REF} \div N_A$ and $f_{QB}=f_{REF} \div (N_A \cdot N_B)$	PLL function enabled $f_{QA} = (f_{REF} \div P) \cdot M \div N_A$ and $f_{QB} = (f_{REF} \div P) \cdot M \div (N_A \cdot N_B)$
TEST_EN	0	Application mode. Test mode disabled.	Factory test mode is enabled
$\overline{\text{CLK\_STOPx}}$	1	Output Q*x* is disabled in logic low state. Synchronous disable is only guaranteed if NB = 0.	Output Q*x* is synchronously enabled
$\overline{\text{MR}}$		The device is reset. The output frequency is zero and the outputs are asynchronously forced to logic low state. After releasing reset (upon the rising edge of $\overline{\text{MR}}$ and independent on the state of $\overline{\text{PLOAD}}$), the MPC92432 reads the parallel interface (M, NA, NB and P) to acquire a valid startup frequency configuration. See application/programming section.	The PLL attempts to lock to the reference signal. The t_{LOCK} specification applies.
Outputs			
LOCK		PLL is not locked	PLL is frequency locked

1. Default states are set by internal input pull-up or pull-down resistors of 75 kΩ
2. If f_{REF} = 16 MHz, the default configuration will result in a output frequency of 250 MHz

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage	—	V_{CC} – 2	—	V	
MM	ESD Protection (Machine model)	200	—	—	V	
HBM	ESD Protection (Human body model)	2000	—	—	V	
LU	Latch-Up Immunity	200	—	—	mA	
C_{IN}	Input Capacitance	—	4.0	—	pF	Inputs
θ_{JA}	Thermal Resistance Junction to Ambient JESD 51-3, single layer test board JESD 51-6, 2S2P multilayer test board	—	—	TBD	°C/W	 Natural convection 100 ft/min 200 ft/min 400 ft/min 800 ft/min Natural convection 100 ft/min 200 ft/min 400 ft/min 800 ft/min
θ_{JC}	LQFP 32 Thermal Resistance Junction to Case	—	—	TBD	°C/W	MIL-SPEC 883E Method 1012.1

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current	—	±20	mA	
I_{OUT}	DC Output Current	—	±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_J = –40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs (M[9:0], N[2:0], ADDR[1:0], NB, P, $\overline{\text{CLK\_STOPx}}$, $\overline{\text{BYPASS}}$, $\overline{\text{MR}}$, REF_SEL, TEST_EN, $\overline{\text{PLOAD}}$)						
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	—	—	0.8	V	LVCMOS
I_{IN}	Input Current[1]	—	—	±200	µA	V_{IN} = V_{CC} or GND
I^2C Inputs (SCL, SDA)						
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	—	—	0.8	V	LVCMOS
I_{IN}	Input Current	—	—	±10	µA	
LVCMOS Output (LOCK)						
V_{OH}	Output High Voltage	2.4	—	—	V	I_{OH} = –4 mA
V_{OL}	Output Low Voltage	—	—	0.4	V	I_{OL} = 4 mA
I^2C Open-Drain Output (SDA)						
V_{OL}	Input Low Voltage	—	—	0.4	V	I_{OL} = 4 mA
Differential Clock Output QA, QB[2]						
V_{OH}	Output High Voltage	V_{CC} – 1.05	—	V_{CC} – 0.74	V	LVPECL
V_{OL}	Output Low Voltage	V_{CC} – 1.95	—	V_{CC} – 1.60	V	LVPECL
$V_{O(P-P)}$	Output Peak-to-Peak Voltage	0.5	0.6	1.0	V	
Supply current						
I_{CC_PLL}	Maximum PLL Supply Current	—	—	TBD	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current	—	—	TBD	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50 Ω to V_{TT} = V_{CC} – 2 V

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_J = –40°C to +85°C)[1] [2]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range		15	16	20	MHz	
f_{REF}	FREF_EXT Reference Frequency Range		15	—	20	MHz	
f_{VCO}	VCO Frequency Range[3]		1360	—	2720	MHz	
f_{MAX}	Output Frequency[4]	N= ÷2	680	—	1360	MHz	
		N= ÷4	340	—	680	MHz	
		N= ÷8	170	—	340	MHz	
		N= ÷16	85	—	170	MHz	
		N= ÷32	42.5	—	85	MHz	
		N= ÷64	21.25	—	42.5	MHz	
f_{SCL}	Serial Interface (I^2C) Clock Frequency		0	—	0.4	MHz	
$t_{P,MIN}$	Minimum Pulse Width	($\overline{P\_LOAD}$)	50	—		ns	
DC	Output Duty Cycle		45	50	55	%	
$t_{SK(O)}$	Output-to-Output Skew	Same frequency	—	—	25	ps	
		Different frequency	—	50		ps	
t_r, t_f	Output Rise/Fall Time (QA, QB)		0.05	—	0.3	ns	20% to 80%
t_r, t_f	Output Rise/Fall Time (SDA)		—	—	250	ns	C_L = 400 pF
t_{P_EN}	Output Enable Time ($\overline{CLKSTOPx}$ to QA, QB)		T_{FOUT}	—	2 · T_{FOUT}		T = period of Qx
t_{P_DIS}	Output Enable Time ($\overline{CLKSTOPx}$ to QA, QB)		0.5 · T_{FOUT}	—	1.5 · T_{FOUT}		T = period of Qx
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	N= ÷2	—	—	TBD	ps	
		N= ÷4	—	—	TBD	ps	
		N= ÷8	—	—	25	ps	
		N= ÷16	—	—	25	ps	
		N= ÷32	—	—	TBD	ps	
		N= ÷64	—	—	TBD	ps	
$t_{JIT(CC)}$	Period Jitter (RMS)	f_{OUT} = 250 MHz	—	—	10	ps	
		Any other frequency	—	—	TBD	ps	
t_{LOCK}	Maximum PLL Lock Time		—	—	10	ms	

1. AC specifications are subject to change
2. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}
3. The input frequency f_{XTAL}, the PLL divider M and P must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot M \div P$. The feedback divider M is limited to 170 <= M <= 340 (for P = 2) and 340 <= M <= 680 (for P = 4) for stable PLL operation
4. Output frequency for Q_A, Q_B if N_B=0. With N_B=1 the Q_B output frequency is half of the Q_A output frequency

APPLICATION INFORMATION

Output Frequency Configuration

The MPC92432 is a programmable frequency source (synthesizer) and supports an output frequency range of 21.25 – 1360 MHz. The output frequency f_{OUT} is a function of the reference frequency f_{REF} and the three internal PLL dividers P, M, and N. f_{OUT} can be represented by this formula:

$$f_{OUT} = (f_{REF} \div P) \cdot M \div (N_{A,\ B}) \quad (1)$$

The M, N and P dividers require a configuration by the user to achieve the desired output frequency. The output divider, N_A, determines the achievable output frequency range (see Table 7). The PLL feedback-divider M is the frequency multiplication factor and the main variable for frequency synthesis. For a given reference frequency f_{REF}, the PLL feedback-divider M must be configured to match the specified VCO frequency range in order to achieve a valid PLL configuration:

$$f_{VCO} = (f_{REF} \div P) \cdot M \text{ and} \quad (2)$$

$$1360 \leq f_{VCO} \leq 2720 \quad (3)$$

The output frequency may be changed at any time by changing the value of the PLL feedback divider M. The smallest possible output frequency change is the synthesizer granularity G (difference in f_{OUT} when incrementing or decrementing M). At a given reference frequency, G is a function of the PLL pre-divider P and post-divider N:

$$G = f_{REF} \div (P \cdot N_{A,B}) \quad (4)$$

The N_B divider configuration determines if the output Q_B generates a 1:1 or 2:1 frequency copy of the Q_A output signal. The purpose of the PLL pre-divider P is to situated the PLL into the specified VCO frequency range f_{VCO} (in combination with M). For a given output frequency, P = 4 results in a smaller output frequency granularity G, P = 2 results a larger output frequency granularity G and also increases the PLL bandwidth compared to the P = 2 setting.

The following example illustrates the output frequency range of the MPC92432 using a 16-MHz reference frequency.

Table 7. Frequency Ranges (f_{REF} = 16 MHz)

f_{OUT} (Q_A) [MHz]	N_A	M	P	G [MHz]
680 – 1360	N_A=2	170 – 340	2	4
		340 – 680	4	2
340 – 680	N_A=4	170 – 340	2	2
		340 – 680	4	1
170 – 340	N_A=8	170 – 340	2	1
		340 – 680	4	0.5
85 – 170	N_A=16	170 – 340	2	0.5
		340 – 680	4	0.25
42.5 – 85	N_A=32	170 – 340	2	0.25
		340 – 680	4	0.125
21.25 – 42.5	N_A=64	170 – 340	2	0.125
		340 – 680	4	0.0625

Example Output Frequency Configuration

If a reference frequency of 16 MHz is available, an output frequency at Q_A of 250 MHz and a small frequency granularity is desired, the following steps would be taken to identify the appropriate P, M, and N configuration:

1. Use Table 7 to select the output divider, N_A, that matches the desired output frequency or frequency range. According to Table 7, a target output frequency of 250 MHz falls in the f_{OUT} range of 170 to 340 MHz and requires to set N_A = 8

2. Calculate the VCO frequency $f_{VCO} = f_{OUT} \cdot N_A$, which is 2000 MHz in this example.

3. Determine the PLL feedback divider: M = $f_{VCO} \div P$. The smallest possible output granularity in this example calculation is 500 kHz (set P = 4). M calculates to a value of 2000 ÷ 4 = 500.

4. Configure the MPC92432 with the obtained settings:

   M[9:0] = 0111110100b (binary number for M=500)

   N_A[2:0] = 010 (÷8 divider, see Table 9)

   P = 1 (÷4 divider, see Table 8)

   N_B = 0 ($f_{OUT,\ QB} = f_{OUT,\ QA}$)

5. Use either parallel or serial interface to apply the setting. The I^2C configuration byte for this examples are: PLL_H=01010010b and PLL_L=11110100b. See Table 14 and Table 15 for register maps.

PLL Divider Configuration

Table 8. Pre-PLL Divider P

P	Value
0	$f_{REF} \div 2$
1	$f_{REF} \div 4$

Table 9. Post-PLL Divider N_A

N_{A0}	N_{A1}	N_{A2}	f_{OUT} (Q_A)
0	0	0	$f_{VCO} \div 2$
0	0	1	$f_{VCO} \div 4$
0	1	0	$f_{VCO} \div 8$
0	1	1	$f_{VCO} \div 16$
1	0	0	$f_{VCO} \div 32$
1	0	1	$f_{VCO} \div 64$

Table 10. Post-PLL Divider N_B

N_B	Value
0	$f_{OUT, QB} = f_{OUT, QA}$
1	$f_{OUT, QB} = f_{OUT, QA} \div 2$

Programming the MPC92432

The MPC92432 has a parallel and a serial configuration interface. The purpose of the parallel interface is to directly configure the PLL dividers through hardware pins without the overhead of a serial protocol. At device startup, the device always obtains an initial PLL frequency configuration through the parallel interface. The parallel interface does not support reading the PLL configuration.

The serial interface is I^2C compatible. It allows reading and writing devices settings by accessing internal device registers. The serial interface is designed for host-controller access to the synthesizer frequency settings for instance in frequency-margining applications.

Using the Parallel Interface

The parallel interface supports write-access to the PLL frequency setting directly through 15 configuration pins (P, M[9:0], NA[2:0], and NB). The parallel interface must be enabled by setting $\overline{PLOAD}$ to logic low level. During $\overline{PLOAD}$ = 0, any change of the logical state of the P, M[9:0], NA[2:0], and NB pins will immediately affect the internal PLL divider settings, resulting in a change of the internal VCO-frequency and the output frequency. The parallel interface mode disables the I^2C write-access to the internal registers; however, I^2C read-access to the internal configuration registers is enabled.

Upon startup, when the device reset signal is released (rising edge of the $\overline{MR}$ signal), the device reads its startup configuration through the parallel interface and independent on the state of $\overline{PLOAD}$. It is recommended to provide a valid PLL configuration for startup. If the parallel interface pins are left open, a default PLL configuration will be loaded. After the low-to-high transition of $\overline{PLOAD}$, the configuration pins have no more effect and the configuration registers are made accessible through the serial interface.

Table 11. PLL Feedback-Divider Configuration (M)

Feedback Divider M	9	8	7	6	5	4	3	2	1	0
Pin	M9	M8	M7	M6	M5	M4	M3	M2	M1	M0
Default	0	1	1	1	1	1	0	1	0	0

Table 12. PLL Pre/Post-Divider Configuration (N, P)

Post-D. NA	2	1	0
Pin	NA2	NA1	NA0
Default	0	1	1

Post-D. NB	NB
Pin	NB
Default	0

Pre-D. P	P
Pin	P
Default	1

Using the I^2C Interface

$\overline{PLOAD}$ = 1 enables the programming and monitoring of the internal registers through the I^2C interface. Device register access (write and read) is possible through the 2-wire interface using SDA (configuration data) and SCL (configuration clock) signals. The MPC92432 acts as a slave device at the I^2C bus. For further information on I^2C it is recommended to refer to the I^2C bus specification (version 2.1).

$\overline{PLOAD}$ = 0 disables the I^2C-write-access to the configuration registers and any data written into the register is ignored. However, the MPC92432 is still visible at the I^2C interface and I^2C transfers are acknowledged by the device. Read-access to the internal registers during $\overline{PLOAD}$ = 0 (parallel programming mode) is supported.

Note that the device automatically obtains a configuration using the parallel interface upon the release of the device reset (rising edge of $\overline{MR}$) and independent on the state of $\overline{PLOAD}$. Changing the state of the $\overline{PLOAD}$ input is not supported when the device performs any transactions on the I^2C interface.

Programming Model and Register Set

The synthesizer contains two fully accessible configuration registers (PLL_L and PLL_H) and a write-only command register (CMD). Programming the synthesizer frequency through the I^2C interface requires two steps: 1) writing a valid PLL configuration to the configuration registers and 2) loading the registers into the PLL by an I^2C command. The PLL frequency is affected as a result of the second step.
This two-step procedure can be performed by a single I^2C

transaction or by multiple, independent I^2C transactions. An alternative way to achieve small PLL frequency changes is to use the increment or decrement commands of the synthesizer, which have an immediate effect on the PLL frequency.

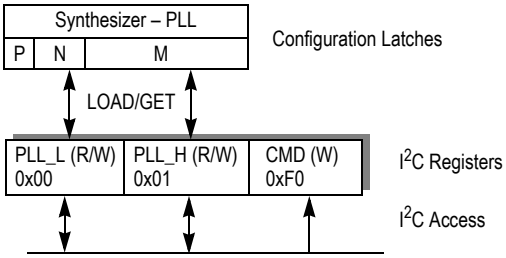


Figure 3. I^2C Mode Register Set

Figure 3 illustrates the synthesizer register set. PLL_L and PLL_H store a PLL configuration and are fully accessible (Read/Write) by the I^2C bus. CMD (Write only) accepts commands (LOAD, GET, INC, DEC) to update registers and for direct PLL frequency changes.

Set the synthesizer frequency:

1) Write the PLL_L and PLL_H registers with a new configuration (see Table 14 and Table 15 for register maps)
2) Write the LOAD command to update the PLL dividers by the current PLL_L, PLL_H content.

Read the synthesizer frequency:

1) Write the GET commands to update the PLL_L, PLL_H registers by the PLL divider setting
2) Read the PLL_L, PLL_H registers through I^2C

Change the synthesizer frequency in small steps:

1) Write the INC or DEC command to change the PLL frequency immediately. Repeat at any time if desired.

LOAD and GET are inverse command to each other. LOAD updates the PLL dividers and GET updates the configuration registers. A fast and convenient way to change the PLL frequency is to use the INC (increment M) and DEC (decrement M) commands of the synthesizer. INC (DEC) directly increments (decrements) the PLL-feedback divider M and immediately changes the PLL frequency by the smallest step G (see Table 7 for the frequency granularity G). The INC and DEC commands are designed for multiple and rapid PLL frequency changes as required in frequency margining applications. INC and DEC do not require the user to update the PLL dividers by the LOAD command, INC and DEC do not update the PLL_L and PLL_H registers either (use LOAD for an initial PLL divider setting and, if desired, use GET to read the PLL configuration). Note that the synthesizer does not check any boundary conditions such as the VCO frequency range. Applying the INC and DEC commands could result in invalid VCO frequencies (VCO frequency beyond lock range).

Register Maps

Table 13. Configuration Registers

Address	Name	Content	Access
0x00	PLL_L	Least significant 8 bits of M	R/W
0x01	PLL_H	Most significant 2 bits of M, P, N_A, N_B, and lock state	R/W
0xF0	CMD	Command register (write only)	W only

Register 0x00 (PLL_L) contains the least significant bits of the PLL feedback divider M.

Table 14. PLL_L (0x00, R/W) Register

Bit	7	6	5	4	3	2	1	0
Name	M7	M6	M5	M4	M3	M2	M1	M0

Register content:
M[7:0] PLL feedback-divider M, bits 7–0

Register 0x01 (PLL_H) contains the two most significant bits of the PLL feedback divider M, four bits to control the PLL post-dividers N and the PLL pre-divider P. The bit 0 in PLL_H register indicates the lock condition of the PLL and is set by the synthesizer automatically. The LOCK state is a copy of the PLL lock signal output (LOCK). A write-access to LOCK has no effect.

Table 15. PLL_H (0x01, R/W) Register

Bit	7	6	5	4	3	2	1	0
Name	M9	M8	NA2	NA1	NA0	NB	P	LOCK

Register content:

M[9:8]	PLL feedback-divider M, bits 9–8
NA[2:0]	PLL post-divider N_A, see Table 9
NB	PLL post-divider N_B, see Table 10
P	PLL pre-divider P, see Table 8
LOCK	Copy of LOCK output signal (read-only)

Note that the LOAD command is required to update the PLL dividers by the content of both PLL_L and PLL_H registers.

Register 0xF0 (CMD) is a write-only command register. The purpose of CMD is to provide a fast way to increase or decrease the PLL frequency and to update the registers. The register accepts four commands, INC (increment M), DEC (decrement M), LOAD and GET (update registers). It is recommended to write the INC, DEC commands only after a valid PLL configuration is achieved. INC and DEC only affect the M-divider of the PLL (PLL feedback). Applying INC and DEC commands can result in a PLL configuration beyond the specified lock range and the PLL may loose lock. The MPC92432 does not verify the validity of any commands such

as LOAD, INC, and DEC. The INC and DEC commands change the PLL feedback divider without updating PLL_L and PLL_H.

Table 16. CMD (0xF0): PLL Command (Write-Only)

Command	Op-Code	Description
INC	xxxx0001b (0x01)	Increase internal PLL frequency M:=M+1
DEC	xxxx0010b (0x02)	Decrease internal PLL frequency M:=M-1
LOAD	xxxx0100b (0x04)	Update the PLL divider config. PLL divider M, N, P:=PLL_L, PLL_H
GET	xxxx1000b (0x08)	Update the configuration registers PLL_L, PLL_H:=PLL divider M, N, P

I^2C — Register Access in Parallel Mode

The MPC92432 supports the configuration of the synthesizer through the parallel interlace ($\overline{PLOAD}$ = 0) and serial interface ($\overline{PLOAD}$ = 1). Register contents and the divider configurations are not changed when the user switches from parallel mode to serial mode. However, when switching from serial mode to parallel mode, the PLL dividers immediately reflect the logical state of the hardware pins M[9:0], NA[2:0], NB, and P.

Applications using the parallel interface to obtain a PLL configuration can use the serial interface to verify the divider settings. In parallel mode ($\overline{PLOAD}$ = 0), the MPC92432 allows read-access to PLL_L and PLL_H through I^2C (if $\overline{PLOAD}$ = 0, the current PLL configuration is stored in PLL_L, PLL_H. The GET command is not necessary and also not supported in parallel mode). After changing from parallel to serial mode ($\overline{PLOAD}$ = 1), the last PLL configuration is still stored in PLL_L, PLL_H. The user now has full write and read access to both configuration registers through the I^2C bus and can change the configuration at any time.

Table 17. PLL Configuration in Parallel and Serial Modes

PLL Configuration	Parallel	Serial (Registers PLL_L, PLL_H)
M[9:0]	Set pins M9–M0	M[9:0] (R/W)

Table 17. PLL Configuration in Parallel and Serial Modes

PLL Configuration	Parallel	Serial (Registers PLL_L, PLL_H)
NA[2:0]	Set pins NA2...NA0	NA[2:0] (R/W)
NB	Set pin NB	NB (R/W)
P	Set bit P in PLL_H	P (R/W)
LOCK status	LOCK pin 26	LOCK (Read only)

Programming the I^2C Interface

Table 18. I^2C Slave Address

Bit	7	6	5	4	3	2	1	0
Value	1	0	1	1	0	Pin ADR1	Pin ADR0	R/W

The 7-bit I^2C slave address of the MPC92432 synthesizer is a combination of a 5-bit fixed addresses and two variable bits which are set by the hardware pins ADR[1:0]. Bit 0 of the MPC92432 slave address is used by the bus controller to select either the read or write mode.'0' indicates a transmission (I^2C-WRITE) to the MPC92432.'1' indicates a request for data (I^2C-READ) from the synthesizer. The hardware pins ADR1 and ADR0 and should be individually set by the user to avoid address conflicts of multiple MPC92432 devices on the same I^2C bus.

Write Mode (R/W = 0)

The configuration registers are written by the bus controller by the initiation of a write transfer with the MPC92432 slave address (first byte), followed by the address of the configuration register (second byte: 0x00, 0x01 or 0xF0), and the configuration data byte (third byte). This transfer may be followed by writing more registers by sending the configuration register address followed by one data byte. Each byte sent by the bus controller is acknowledged by the MPC92432. The transfer ends by a stop bit sent by the bus controller. The number of configuration data bytes and the write sequence are not restricted.

Table 19. Complete Configuration Register Write Transfer

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	8 bits	1 bit	1 bit
Start	Slave address	R/W	ACK	&PLL_H	ACK	Config-Byte 1	ACK	&PLL_L	ACK	Config-Byte 2	ACK	Stop
	10110xx[1]	0		0x01		Data		0x00		Data		
Master	Master	Mast	Slave	Master	Slave	Master	Slave	Master	Slave	Master	Slave	Mast

1. xx = state of ADR1, ADR0 pins

Read Mode (R/W = 1)

The configuration registers are read by the bus controller by the initiation of a read transfer. The MPC92432 supports read transfers immediately after the first byte without a change in the transfer direction. Immediately after the bus controller sends the slave address, the MPC92432 acknowledges and then sends both configuration register PLL_L and PLL_H (back-to-back) to the bus controller. The CMD register cannot be read. In order to read the two synthesizer registers and the current PLL configuration setting, the user can 1) read PLL_L, PLL_H, write the GET command (loads the current configuration into PLL_L, PLL_H) and read PLL_L, PLL_H again. Note that the PLL_L, PLL_H registers and divider settings may not be equivalent after the following cases:

a. Writing the INC command

b. Writing the DEC command

c. Writing PLL_L, PLL_H registers with a new configuration and not writing the LOAD command.

Table 20. Configuration Register Read Transfer

1 bit	7 bits	1 bit	1 bit	8 bits	1 bit	8 bits	1 bit	1 bit
Start	Slave address	R/W	ACK	PLL_L	ACK	PLL_H	ACK	Stop
	10110xx[1]	1		Data		Data		
Master	Master	Mast	Slave	Slave	Mast	Slave	Master	Slave

1. xx = state of ADR1, ADR0 pins

Device Startup

General Device Configuration

It is recommended to reset the MPC92432 during or immediately after the system powers up ($\overline{MR}$ = 0). The device acquires an initial PLL divider configuration through the parallel interface pins M[9:0], NA[2:0], N, and P(1) with the low-to-high transition of $\overline{MR}$(2). PLL frequency lock is achieved within the specified lock time (t_{LOCK}) and is indicated by an assertion of the LOCK signal which completes the startup procedure. It is recommended to disable the outputs ($\overline{CLK\_STOPx}$ = 0) until PLL lock is achieved to suppress output frequency transitions. The output frequency can be reconfigured at any time through either the parallel or the serial interface.

Note that a PLL configuration obtained by the parallel interface can be read through I^2C independent on the current programming mode (parallel or serial). Refer to I2C — Register Access in Parallel Mode for additional information on how to read a PLL startup configuration through the I^2C interface.

Starting-Up Using the Parallel Interface

The simplest way to use the MPC92432 is through the parallel interface. The serial interface pins (SDA, SDL, and ADDR[1:0]) can be left open and $\overline{PLOAD}$ is set to logic low. After the release of $\overline{MR}$ and at any other time the PLL/output frequency configuration is directly set to through the M[9:0], NA[2:0], NB, and P pins.

Start-Up Using the Serial (I^2C) Interface

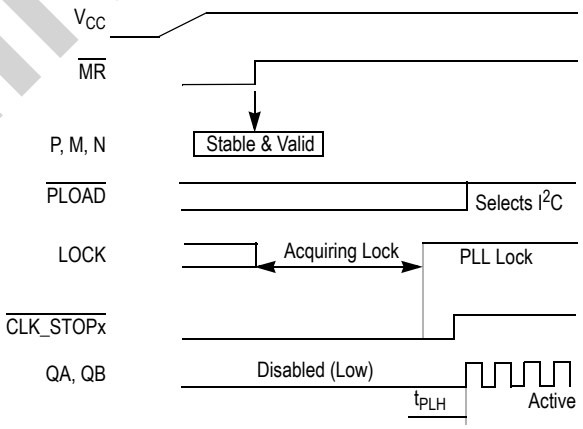


Figure 4. Start-Up Using I^2C Interface

Set $\overline{PLOAD}$ = 1, $\overline{CLK\_STOPx}$ = L and leave the parallel interface pins (M[9:0], NA[2:0], N, and P) open. The PLL dividers are configured by the default configuration at the low-to-high transition of $\overline{MR}$. This initial PLL configuration can be re-programmed to the final VCO frequency at any time through the serial interface. After the PLL achieved lock at the desired VCO frequency, enable the outputs by setting $\overline{CLK\_STOPx}$ = H. PLL lock and re-lock (after any configuration change through M or P) is indicated by LOCK being asserted.

1. The parallel interface pins M[9:0], NA[2:0], N, and P may be left open (floating). In this case the initial PLL configuration will have the default setting of M = 500, P = 1, NA[2:0] = 010, NB = 0, resulting in an internal VCO frequency of 2000 MHz (f_{ref} = 16 MHz) and an output frequency of 250 MHz.
2. The initial PLL configuration is independent on the selected programming mode ($\overline{PLOAD}$ low or high)

LOCK Detect

The LOCK detect circuitry indicates the frequency-lock status of the PLL by setting and resetting the pin LOCK and register bit LOCK simultaneously. The LOCK status is asserted after the PLL acquired frequency lock during the startup and is immediately deasserted when the PLL lost lock, for instance when the reference clock is removed. The PLL may also loose lock when the PLL feedback-divider M or pre-divider P is changed or the DEC/INC command is issued. The PLL may not loose lock as a result of slow reference frequency changes. In any case of loosing LOCK, the PLL attempts to re-lock to the reference frequency. LOCK and re-lock of the PLL is indicated by the LOCK signal after a delay of TBD cycles to prevent signaling temporary PLL locks during frequency transitions.

Output Clock Stop

Asserting $\overline{\text{CLK\_STOPx}}$ will stop the respective output clock in logic low state. The $\overline{\text{CLK\_STOPx}}$ control is internally synchronized to the output clock signal, therefore, enabling and disabling outputs does not produce runt pulses. See Figure 5.The clock stop controls of the QA and QB outputs are independent on each other. If the QB runs at half of the QA output frequency and both outputs are enabled at the same time, the first clock pulse of QA may not appear at the same time of the first QB output. (See Figure 6.) Concident rising edges of QA and QB stay synchronous after the assertion and de-assertion of the CLK_STOPx controls. Asserting $\overline{\text{MR}}$ always resets the output divider to a logic low output state, with the risk of producing an output runt pulse.

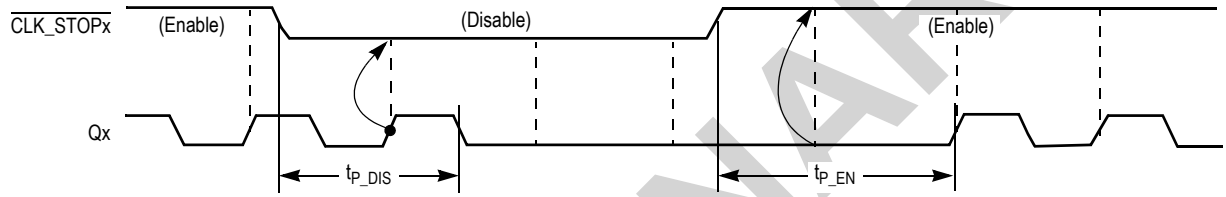


Figure 5. Clock Stop Timing for NB = 0 ($f_{QA} = f_{QB}$)

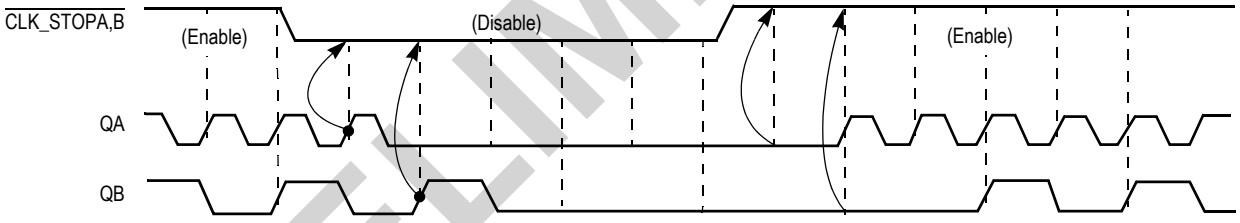


Figure 6. Clock Stop Timing for NB = 1 ($f_{QA} = 2\ f_{QB}$)

Frequency Operating Range

Table 21. MPC92432 Frequency Operating Range for P = 2

		f_{VCO} [MHz] (Parameter: f_{REF} in MHz)				Output Frequency for f_{XTAL} = 16 MHz (Parameter N)					
M	M[9:0]	15	16	18	20	2	4	8	16	32	64
170	0010101010		1360	1530	1700	680	340	170	85	42.50	21.25
180	0010110100		1440	1620	1800	720	360	180	90	45.00	22.50
190	0010111110	1425	1520	1710	1900	760	380	190	95	47.50	23.75
200	0011001000	1500	1600	1800	2000	800	400	200	100	50.00	25.00
210	0011010010	1575	1680	1890	2100	840	420	210	105	52.50	26.25
220	0011011100	1650	1760	1980	2200	880	440	220	110	55.00	27.50
230	0011100110	1725	1840	2070	2300	920	460	230	115	57.50	28.75
240	0011110000	1800	1920	2160	2400	960	480	240	120	60.00	30.00
250	0011111010	1875	2000	2250	2500	1000	500	250	125	62.50	31.25
260	0100000100	1950	2080	2340	2600	1040	520	260	130	65.00	32.50
270	0100001110	2025	2160	2430	2700	1080	540	270	135	67.50	33.75
280	0100011000	2100	2240	2520		1120	560	280	140	70.00	35.00
290	0100100010	2175	2320	2610		1160	580	290	145	72.50	36.25
300	0100101100	2250	2400	2700		1200	600	300	150	75.00	37.50
310	0100110110	2325	2480			1240	620	310	155	77.50	38.75
320	0101000000	2400	2560			1280	640	320	160	80.00	40.00
330	0101001010	2475	2640			1320	660	330	165	82.50	41.25
340	0101010100	2550	2720			1360	680	340	170	85.00	42.50

Table 22. MPC92432 Frequency Operating Range for P = 4

		f_{VCO} [MHz] (Parameter: f_{REF} in MHz)				Output Frequency for f_{XTAL} = 16 MHz (Parameter N)					
M	M[9:0]	15	16	18	20	2	4	8	16	32	64
340	0101010100		1360	1530	1700	680	340	170	85.0	42.50	21.25
350	0101011110		1400	1575	1750	700	350	175	87.5	43.75	21.875
360	0101101000		1440	1620	1800	720	360	180	90.0	45.00	22.50
370	0101110010	1387.5	1480	1665	1850	740	370	185	92.5	46.25	23.125
380	0101111100	1425.0	1520	1710	1900	760	380	190	95.0	47.50	23.75
390	0110000110	1462.5	1560	1755	1950	780	390	195	97.5	48.75	24.375
400	0110010000	1500.0	1600	1800	2000	800	400	200	100.0	50.00	25.00
410	0110110010	1537.5	1640	1845	2050	820	410	205	102.5	51.25	25.625
420	0110100100	1575.0	1680	1890	2100	840	420	210	105.0	52.50	26.25
430	0110101110	1612.5	1720	1935	2150	860	430	215	107.5	53.75	26.875
440	0110111000	1650.0	1760	1980	2200	880	440	220	110.0	55.00	27.50
450	0111000010	1687.5	1800	2025	2250	900	450	225	112.5	56.25	28.125
460	0111001100	1725.0	1840	2070	2300	920	460	230	115.0	57.50	28.75
470	0111010110	1762.5	1880	2115	2350	940	470	235	117.5	58.75	29.375
480	0111100000	1800.0	1920	2160	2400	960	480	240	120.0	60.00	30.00
490	0111101010	1837.5	1960	2205	2450	980	490	245	122.5	61.25	30.626
500	0111110100	1875.0	2000	2250	2500	1000	500	250	125.0	62.50	31.25
510	0111111110	1912.5	2040	2295	2550	1020	510	255	127.5	63.75	31.875
520	1000001000	1950.0	2080	2340	2600	1040	520	260	130.0	65.00	32.50
530	1000010010	1987.5	2120	2475	2650	1060	530	265	132.5	66.25	33.125
540	1000011100	2025.0	2160	2520	2700	1080	540	270	135.0	67.50	33.75
550	1000100110	2062.5	2200	2565		1100	550	285	137.5	68.75	34.375
560	1000110000	2100.0	2240	2610		1120	560	280	140.0	70.00	35.00
570	1000111010	2137.5	2280	2700		1140	570	285	142.5	71.25	35.625
580	1001000100	2175.0	2320			1160	580	290	145.0	72.50	36.25
590	1001001110	2212.5	2360			1180	590	295	147.5	73.75	36.875
600	1001011000	2250.0	2400			1200	600	300	150.0	75.00	37.50
610	1001100010	2287.5	2440			1220	610	305	152.5	76.25	38.125
620	1001101100	2325.0	2480			1240	620	310	155.0	77.50	38.75
630	1001110110	2362.5	2520			1260	630	315	157.5	78.75^	39.375
640	1010000000	2400.0	2560			1280	640	320	160.0	80.00	40.00
650	1010001010	2437.5	2600			1300	650	325	162.5	81.25	40.625
660	0010010100	2475.0	2640			1320	660	330	165	82.5	41.25
670	1010011110	2512.5	2680			1340	670	335	167.5	83.75	41.875
680	1010101000	2550.0	2720			1360	680	340	170	85.00	42.50

V_{CC_PLL} Filter

The MPC92432 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device AC characteristics. The MPC92432 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In digital system environments where it is more difficult to minimize noise on the power supplies a second level of isolation is recommended: a power supply filter on the V_{CC_PLL} pin for the MPC92432.

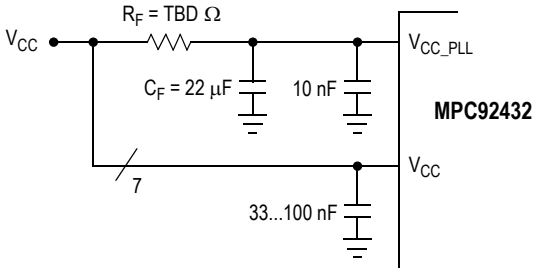


Figure 7. V_{CC_PLL} Power Supply Filter

Figure 7 illustrates a recommended power supply filter scheme.

The MPC9230 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CC_PLL} pin of the .

MPC92432. From the data sheet, the V_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is maximum TBD mA, assuming that a minimum of TBD V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 8 must have a resistance of TBD Ω to meet the voltage drop criteria. The minimum values for R_F and the filter capacitor C_F are defined by the filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above TBD kHz. In the recommended filter shown in Figure 7 the filter cut-off frequency is around 4.5 TBD and the noise attenuation at TBD KHz is better than TBD dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

AC Test Reference and Output Termination

The MPC92432 LVPECL outputs are designed to drive 50 transmission lines and require a DC termination to $V_{TT} = V_{CC} – 2$ V. Figure 8 illustrates the AC test reference for the MPC92432 as used in characterization and test of this circuit. If a separate termination voltage (V_{TT}) is not available, applications may use alternative output termination methods such as shown in Figure 9 and Figure 10.

The high-speed differential output signals of the MPC92432 are incompatible to single-ended LVCMOS signals. In order to use the synthesizer in LVCMOS clock signal environments, the dual-channel translator device MC100ES60T23 provides the necessary level conversion. The MC100ES60T23 has been specifically designed to interface with the MPC92432 and supports clock frequency up to 180 MHz

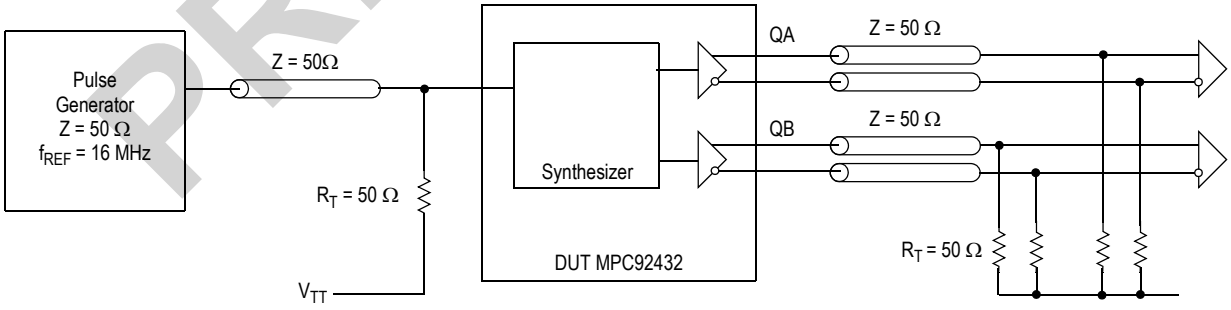


Figure 8. MPC92432 AC Test Reference

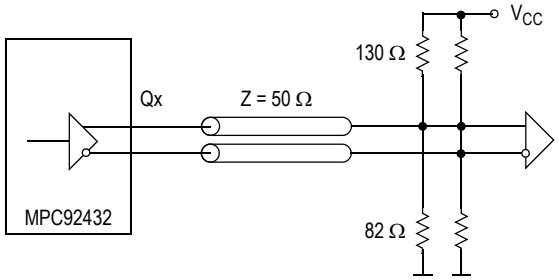


Figure 9. Thevenin Termination

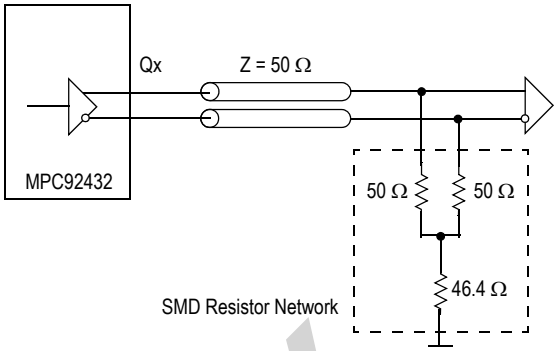


Figure 10. Resistor Network Termination

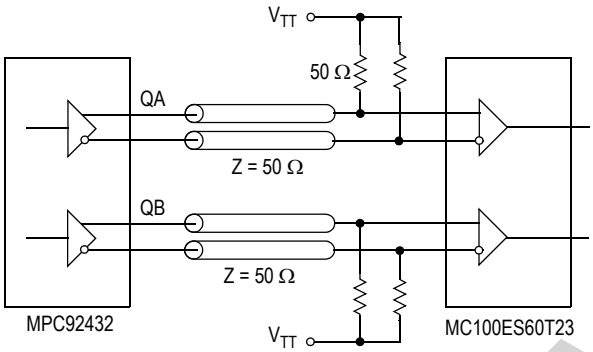


Figure 11. Interfacing with LVCMOS Logic for Frequency < 180 MHz

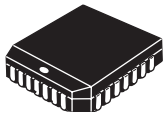
Order number: MPC92439
Rev 1, 08/2004

900 MHz Low Voltage LVPECL Clock Synthesizer

MPC92439

900 MHz LOW VOLTAGE CLOCK SYNTHESIZER

The MPC92439 is a 3.3V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 3.125 MHz to 900 MHz and the support of differential LVPECL output signals the device meets the needs of the most demanding clock applications.



FN SUFFIX
28-LEAD PLCC PACKAGE
CASE 776-02

FA SUFFIX
32-LEAD TQFP PACKAGE
CASE 873A-03

Features

- 3.125 MHz to 900 MHz synthesized clock output signal
- Differential LVPECL output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference input
- 3.3V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 28-PLCC and 32-LQFP packaging
- 32-lead Pb-free package available
- SiGe Technology
- Ambient temperature range 0°C to + 70°C
- Pin and function compatible to the MC12439

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator or external reference clock signal is multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1800 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle. The output driver is driven differentially from the output divider, and is capable of driving a pair of transmission lines terminated 50Ω to V_{CC} – 2.0V. The positive supply voltage for the internal PLL is separated from the power supply for the core logic and output drivers to minimize noise induced jitter.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the P_LOAD input LOW until power becomes valid. On the LOW-to-HIGH transition of P_LOAD, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating. The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See PROGRAMMING INTERFACE for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output. The PWR_DOWN pin, when asserted, will synchronously divide the FOUT by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de-assertion of the PWR_DOWN pin, the FOUT input will step back up to its programmed frequency in four discrete increments.

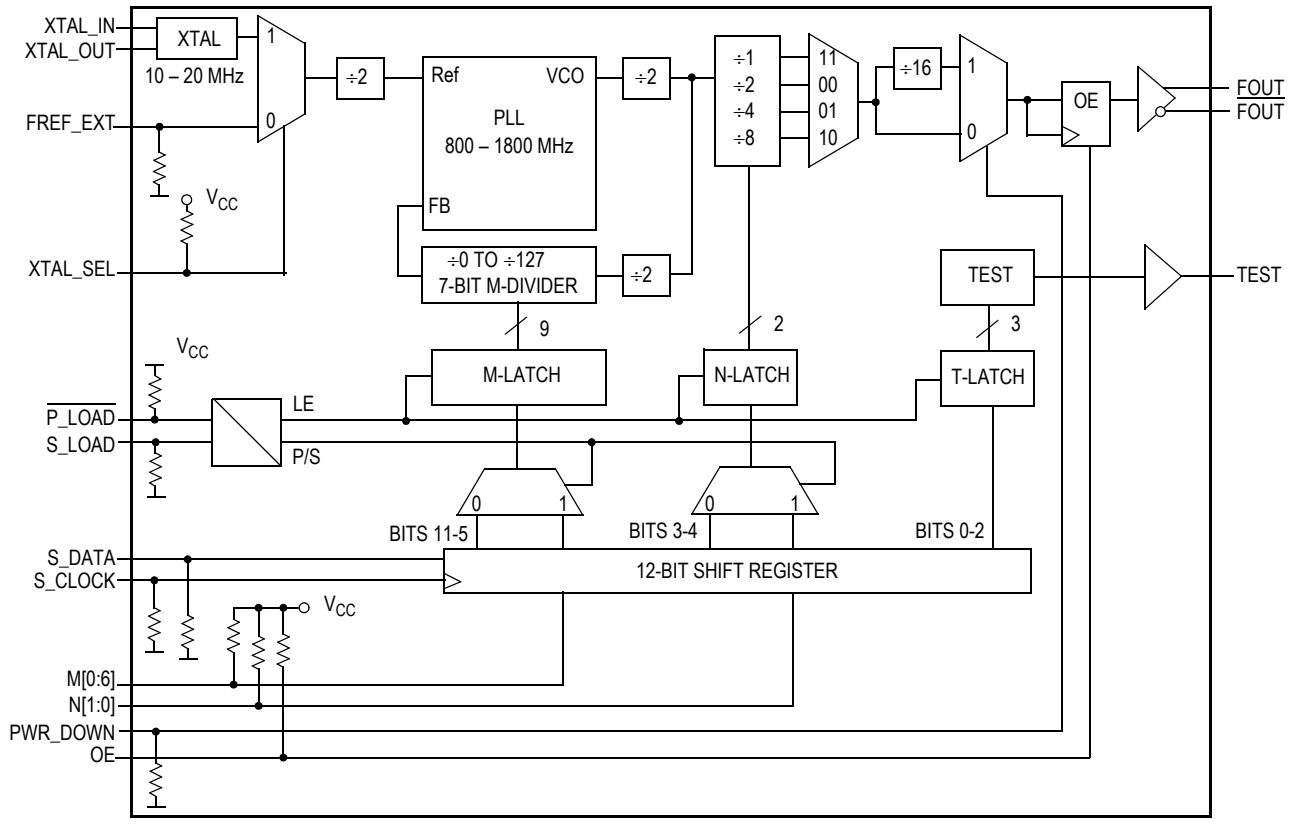


Figure 1. MPC92439 Logic Diagram

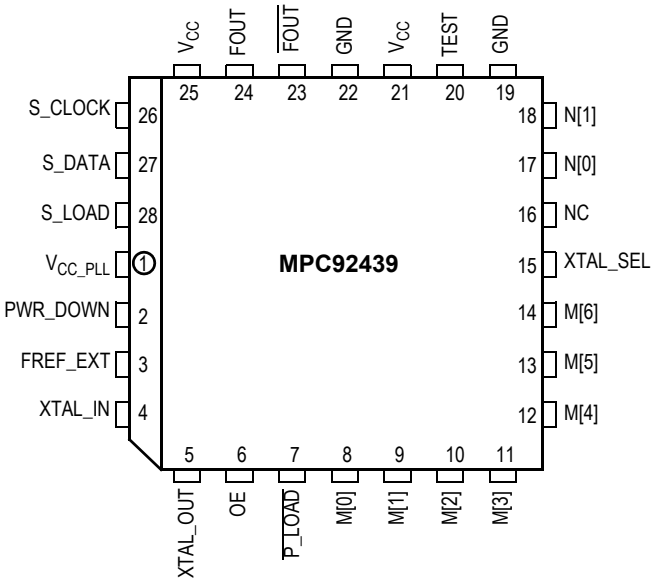


Figure 2. MPC92439 28-Lead PLCC Pinout
(Top View)

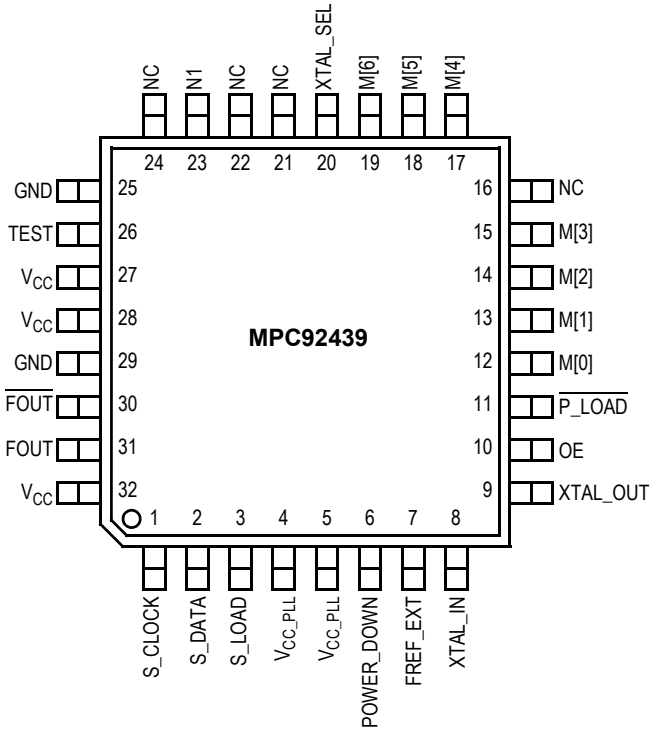


Figure 3. MPC92439 32-Lead Package Pinout
(Top View)

Table 1. Pin Configurations

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface
FREF_EXT	Input	0	LVCMOS	Alternative PLL reference input
FOUT, $\overline{\text{FOUT}}$	Output		LVPECL	Differential clock output
TEST	Output		LVCMOS	Test and device diagnosis output
XTAL_SEL	Input	1	LVCMOS	PLL reference select input
PWR_DOWN	Input	0	LVCMOS	Configuration input for power down mode. Assertion (deassertion) of power down will decrease (increase) the output frequency by a ratio of 16 in 4 discrete steps. PWR_DOWN assertion (deassertion) is synchronous to the input reference clock.
S_LOAD	Input	0	LVCMOS	Serial configuration control input. This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
P_LOAD	Input	1	LVCMOS	Parallel configuration control input. this input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of $\overline{\text{P\_LOAD}}$. $\overline{\text{P\_LOAD}}$ is state sensitive.
S_DATA	Input	0	LVCMOS	Serial configuration data input.
S_CLOCK	Input	0	LVCMOS	Serial configuration clock input.
M[0:6]	Input	1	LVCMOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
N[1:0]	Input	1	LVCMOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of $\overline{\text{P\_LOAD}}$.
OE	Input	1	LVCMOS	Output enable (active high) The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the FOUT output. OE = L low stops FOUT in the logic low state (FOUT = L, $\overline{\text{FOUT}}$ = H).
GND	Supply		Ground	Negative power supply (GND).
V_{CC}	Supply		V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation.
V_{CC_PLL}	Supply		V_{CC}	PLL positive power supply (analog power supply).
NC				Do not connect

Table 2. Output Frequency Range and PLL Post-Divider N

PWR_DOWN	N		VCO Output Frequency Division	FOUT Frequency Range
	1	0		
0	0	0	2	200 – 450 MHz
0	0	1	4	100 – 225 MHz
0	1	0	8	50 – 112.5 MHz
0	1	1	1	400 – 900 MHz
1	0	0	32	12.5 – 28.125 MHz
1	0	1	64	6.25 – 14.0625 MHz
1	1	0	128	3.125 – 7.03125 MHz
1	1	1	16	25 – 56.25 MHz

Table 3. Function Table

Input	0	1
XTAL_SEL	FREF_EXT	XTAL interface
OE	Outputs disabled, FOUT is stopped in the logic low state (FOUT = L, $\overline{FOUT}$ = H)	Outputs enabled
PWR_DOWN	Output divider ÷ 1	Output divider ÷ 16

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	4.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = 0°C to +70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs (FREF_EXT, POWER_DOWN, XTAL_SEL, P_LOAD, S_LOAD, S_DATA, S_CLOCK, M[0:8], N[0:1]. OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[1]			±200	μA	V_{IN} = V_{CC} or GND
Differential Clock Output F_{OUT}[2]						
V_{OH}	Output High Voltage[3]	V_{CC}–1.02		V_{CC}–0.74	V	LVPECL
V_{OL}	Output Low Voltage[3]	V_{CC}–1.95		V_{CC}–1.60	V	LVPECL
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage	2.0			V	I_{OH} = –0.8 mA
V_{OL}	Output Low Voltage			0.55	V	I_{OL} = 0.8 mA
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current		62	110	mA	All V_{CC} Pins

1. Inputs have pull-down resistors affecting the input current.
2. Outputs terminated 50Ω to V_{TT} = V_{CC} – 2V.
3. The MPC92439 FOUT output levels are compatible to the MC12439 output levels. The MPC92439 is capable of driving 25Ω loads.

Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range		10		20	MHz	
f_{VCO}	VCO Frequency Range[2]		800		1800	MHz	
f_{MAX}	Output Frequency	N = 11 (÷1) N = 00 (÷2) N = 01 (÷4) N = 10 (÷8)	400 200 100 50		900 450 225 112.5	MHz MHz MHz MHz	PWWR_DOWN = 0
f_{S_CLOCK}	Serial Interface Programming Clock Frequency[3]		0		10	MHz	
$t_{P,MIN}$	Minimum Pulse Width	(S-LOAD, P_LOAD)	50			ns	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.05		0.3	ns	20% to 80%
t_S	Setup Time	S_DATA to S_CLOCK S_CLOCK to S_LOAD M, N to P_LOAD	20 20 20			ns ns ns	
t_H	Hold Time	S_DATA to S_CLOCK M, N to P_LOAD	20 20			ns ns	
$t_{JIT(PER)}$	Period Jitter				25	ps	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot 2 \cdot M$.
3. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See APPLICATIONS INFORMATION for more details.

Table 8. MPC92439 Frequency Operating Range (In MHz)

M	M[6:0]	VCO frequency for an crystal interface frequency of						Output frequency for f_{XTAL}=16 MHz and for N =			
		10 MHz	12 MHz	14 MHz	16 MHz	18 MHz	20 MHz	1	2	4	8
20	0010100						800				
21	0010101						840				
22	0010110						880				
23	0010111					828	920				
24	0011000					864	960				
25	0011001				800	900	1000	400	200	100	50
26	0011010				832	936	1040	416	208	104	52
27	0011011				864	972	1080	432	216	108	54
28	0011100			812	896	1008	1120	448	224	112	56
29	0011101			840	928	1044	1160	464	232	116	58
30	0011110			875	960	1080	1200	480	240	120	60
31	0011111			868	992	1116	1240	496	248	124	62
32	0100000			896	1024	1152	1280	512	256	128	64
33	0100001			924	1056	1188	1320	528	264	132	66
34	0100010		816	952	1088	1224	1360	544	272	136	68
35	0100011		840	980	1120	1260	1400	560	280	140	70
36	0100100		864	1008	1152	1296	1440	576	288	144	72
37	0100101		888	1036	1184	1332	1480	592	296	148	74
38	0100110		912	1064	1216	1368	1520	608	304	152	76
39	0100111		936	1092	1248	1404	1560	624	312	156	78
40	0101000	800	960	1120	1280	1440	1600	640	320	160	80
41	0101001	820	984	1148	1312	1476	1640	656	328	164	82
42	0101010	840	1008	1176	1344	1512	1680	672	336	168	84
43	0101011	860	1032	1204	1376	1548	1720	688	344	172	86
44	0101100	880	1056	1232	1408	1584	1760	704	352	176	88
45	0101101	900	1080	1260	1440	1620	1800	720	360	180	90
46	0101110	920	1104	1288	1472	1656		736	368	184	92
47	0101111	940	1128	1316	1504	1692		752	376	188	94
48	0110000	960	1152	1344	1536	1728		768	384	192	96
49	0110001	980	1176	1372	1568	1764		784	392	196	98
50	0110010	1000	1200	1400	1600	1800		800	400	200	100
51	0110011	1020	1224	1428	1632			816	408	204	102
52	0110100	1040	1248	1456	1664			832	416	208	104
53	0110101	1060	1272	1484	1696			848	424	212	106
54	0110110	1080	1296	1512	1728			864	432	216	108
55	0110111	1100	1320	1540	1760			880	440	220	110
56	0111000	1120	1344	1568	1792			896	448	224	112
57	0111001	1140	1368	1596							
58	0111010	1160	1392	1624							
59	0111011	1180	1416	1652							
60	0111100	1200	1440	1680							
61	0111101	1220	1488	1736							
62	0111110	1260	1512	1764							
63	0111111	1260	1512	1764							
64	1000000	1280	1536	1792							
...		...	...	...							

PROGRAMMING INTERFACE

Programming the MPC92439

Programming the MPC92439 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$f_{OUT} = (f_{XTAL} \div 2) \cdot (M \cdot 4) \div (N \cdot 2) \text{ or} \quad (1)$$

$$f_{OUT} = f_{XTAL} \cdot M \div N \quad (2)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 800 to 1800 MHz in order to achieve stable PLL operation:

$$M_{MIN} = f_{VCO,MIN} \div (2 \cdot f_{XTAL}) \text{ and} \quad (3)$$

$$M_{MAX} = 2 \cdot f_{VCO,MAX} \div (2 \cdot f_{XTAL}) \quad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M = 25 and M = 56. Table 8 shows the usable VCO frequency and M divider range for other example input frequencies. Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$$f_{OUT} = 16\ M \div N \quad (5)$$

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 9. Output Frequency Range for f_{XTAL} = 16 MHz

N			F_{OUT}	F_{OUT} Range	F_{OUT} Step
1	0	Value			
0	0	2	8·M	200-450 MHz	8 MHz
0	1	4	4·M	100-225 MHz	4 MHz
1	0	8	2·M	50-112.5 MHz	2 MHz
1	1	1	16·M	400-900 MHz	16 MHz

Example Calculation for an 16 MHz Input Frequency

For example, if an output frequency of 384 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 384 MHz falls within the frequency range set by an N value of 2, so N[1:0]=00. For N = 2, FOUT = 8·M and M = FOUT÷8. Therefore, M = 384 ÷ 8 = 48, so M[6:0] = 0110000. Following this procedure a user can generate any whole frequency between 50 MHz and 900 MHz. The size of the programmable frequency steps will be equal to:

$$f_{STEP} = f_{XTAL} \div N \quad (6)$$

APPLICATIONS INFORMATION

Using the Parallel and Serial Interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW to HIGH transition will latch the information present on the M[6:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[6:0] and N[1:0] inputs will affect the FOUT output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two, and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1 and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 4 illustrates the timing diagram for both a parallel and a serial load of the MPC92439 synthesizer.

M[6:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the Test and Diagnosis Output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents FOUT, the LVCMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis.

The T2, T1 and T0 control bits are preset to ‘000' when P_LOAD is LOW so that the PECL FOUT outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MPC92439 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC92439 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the FOUT differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving FOUT directly gives the user more control on the test clocks sent through the clocktree shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the FOUT pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 10. Test and Debug Configuration for TEST

T[2:0]			TEST Output
T2	T1	T0	
0	0	0	12-bit shift register out[1]
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 2$
0	1	1	M-Counter out
1	0	0	FOUT
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	FOUT ÷ 4

1. Clocked out at the rate of S_CLOCK

Table 11. Debug Configuration for PLL Bypass[1]

Output	Configuration
FOUT	S_CLOCK ÷ N
TEST	M-Counter out[2]

1. T[2:0] = 110. AC specifications do not apply in PLL bypass mode
2. Clocked out at the rate of S_CLOCK ÷ (2·N)

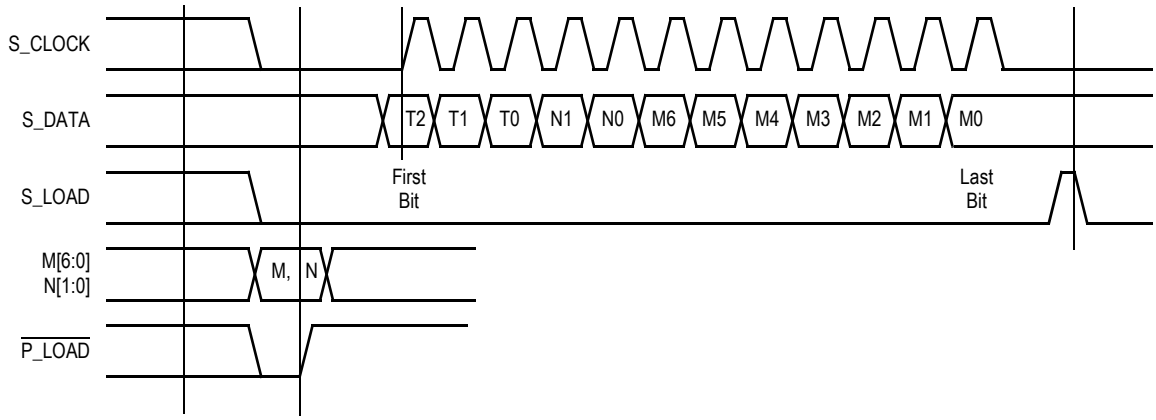


Figure 4. Serial Interface Timing Diagram

Power Supply Filtering

The MPC92439 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CC_PLL} pin impacts the device characteristics. The MPC92439 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC92439. Figure 5 illustrates a typical power supply filter scheme. The MPC92439 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the MPC92439 pin of the MPC92439. From the data sheet, the V_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is maximum 20 mA, assuming that a minimum of 2.835 V must be maintained on the V_{CC_PLL} pin. The resistor shown in Figure 5 must have a resistance of 10–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the V_{CC_PLL} pin, a low DC resistance inductor is required (less than 15 Ω).

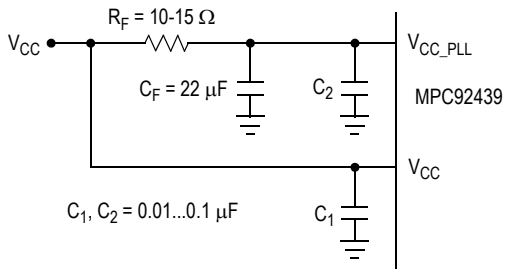


Figure 5. V_{CC_PLL} Power Supply Filter

Layout Recommendations

The MPC92439 provides sub-nanosecond output edge rates and thus a good power supply bypassing scheme is a must. Figure 6 shows a representative board layout for the MPC92439. There exists many different potential board layouts and the one pictured is but one. The important aspect of the layout in Figure 6 is the low impedance connections between VCC and GND for the bypass capacitors. Combining good quality general purpose chip capacitors with good PCB layout techniques will produce effective capacitor resonances at frequencies adequate to supply the instantaneous switching current for the MPC92439 outputs. It is imperative that low inductance chip capacitors are used; it is equally important that the board layout does not introduce back all of the inductance saved by using the leadless capacitors. Thin interconnect traces between the capacitor and the power plane should be avoided and multiple large vias should be used to tie the capacitors to the buried power planes. Fat interconnect and large vias will help to minimize layout induced inductance and thus maximize the series resonant point of the bypass capacitors. Note the dotted lines circling the crystal oscillator connection to the device. The oscillator is a series resonant circuit and the voltage amplitude across the crystal is relatively small. It is imperative that no actively switching signals cross under the crystal as crosstalk energy coupled to these lines could significantly impact the jitter of the device. Special attention should be paid to the layout of the crystal to ensure a stable, jitter free interface between the crystal and the on-board oscillator. Although the MPC92439 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter and bypass schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

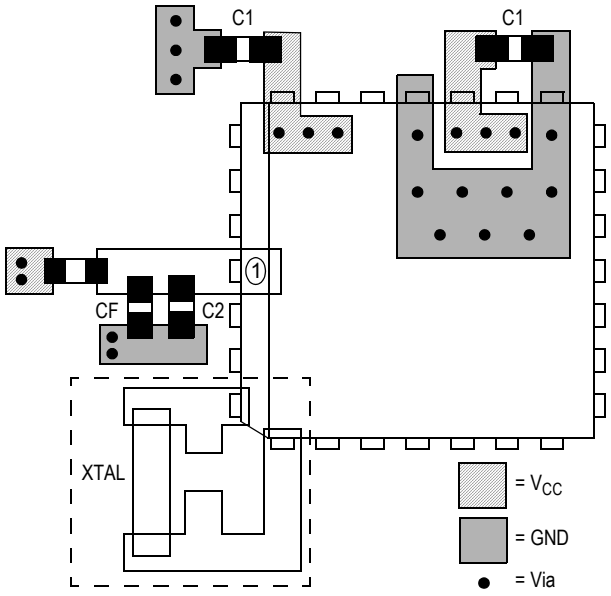


Figure 6. PCB Board Layout Recommendation for the PLCC28 Package

Using the On-Board Crystal Oscillator

The MPC92439 features a fully integrated on-board crystal oscillator to minimize system implementation costs. The oscillator is a series resonant, multivibrator type design as opposed to the more common parallel resonant oscillator design. The series resonant design provides better stability and eliminates the need for large on chip capacitors. The oscillator is totally self contained so that the only external component required is the crystal. As the oscillator is somewhat sensitive to loading on its inputs the user is advised to mount the crystal as close to the MPC92439 as possible to avoid any board level parasitics. To facilitate co-location surface mount crystals are recommended, but not required. Because the series resonant design is affected by capacitive loading on the xtal terminals loading variation introduced by crystals from different vendors could be a potential issue. For crystals with a higher shunt capacitance it may be required to place a resistance across the terminals to suppress the third harmonic. Although typically not required it is a good idea to layout the PCB with the provision of adding this external resistor. The resistor value will typically be between 500 and 1KΩ.

The oscillator circuit is a series resonant circuit and thus for optimum performance a series resonant crystal should be used. Unfortunately most crystals are characterized in a parallel resonant mode. Fortunately there is no physical difference between a series resonant and a parallel resonant crystal. The difference is purely in the way the devices are characterized. As a result a parallel resonant crystal can be used with the MPC92439 with only a minor error in the desired frequency. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified, a few hundred ppm translates to kHz inaccuracies. In a general computer application this level of inaccuracy is immaterial. Table 12 below specifies the performance requirements of the crystals to be used with the MPC92439.

Table 12. Recommended Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Series Resonance[1]
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5-7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

1. See accompanying text for series versus parallel resonant discussion.

Order number: MPC92459
Rev 0, 08/2004

Preliminary Information

900 MHz Low Voltage LVDS Clock Synthesizer

MPC92459

900 MHz LOW VOLTAGE CLOCK SYNTHESIZER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC92459 is a 3.3 V compatible, PLL based clock synthesizer targeted for high performance clock generation in mid-range to high-performance telecom, networking and computing applications. With output frequencies from 50 MHz to 900 MHz and the support of differential LVDS output signals the device meets the needs of the most demanding clock applications.

Features

- 50 MHz to 900 MHz synthesized clock output signal
- Differential LVDS output
- LVCMOS compatible control inputs
- On-chip crystal oscillator for reference frequency generation
- Alternative LVCMOS compatible reference input
- 3.3 V power supply
- Fully integrated PLL
- Minimal frequency overshoot
- Serial 3-wire programming interface
- Parallel programming interface for power-up
- 32 Pin LQFP Package
- SiGe Technology
- Ambient temperature range 0°C to + 70°C

Functional Description

The internal crystal oscillator uses the external quartz crystal as the basis of its frequency reference. The frequency of the internal crystal oscillator or external reference clock signal is multiplied by the PLL. The VCO within the PLL operates over a range of 800 to 1800 MHz. Its output is scaled by a divider that is configured by either the serial or parallel interfaces. The crystal oscillator frequency f_{XTAL}, the PLL feedback-divider M and the PLL post-divider N determine the output frequency.

The feedback path of the PLL is internal. The PLL adjusts the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low) the PLL will not achieve phase lock. The PLL will be stable if the VCO frequency is within the specified VCO frequency range (800 to 1800 MHz). The M-value must be programmed by the serial or parallel interface.

The PLL post-divider N is configured through either the serial or the parallel interfaces, and can provide one of four division ratios (1, 2, 4, or 8). This divider extends performance of the part while providing a 50% duty cycle.

The configuration logic has two sections: serial and parallel. The parallel interface uses the values at the M[6:0] and N[1:0] inputs to configure the internal counters. It is recommended on system reset to hold the $\overline{\text{P\_LOAD}}$ input LOW until power becomes valid. On the LOW-to-HIGH transition of $\overline{\text{P\_LOAD}}$, the parallel inputs are captured. The parallel interface has priority over the serial interface. Internal pullup resistors are provided on the M[6:0] and N[1:0] inputs prevent the LVCMOS compatible control inputs from floating. The serial interface centers on a twelve bit shift register. The shift register shifts once per rising edge of the S_CLOCK input. The serial input S_DATA must meet setup and hold timing as specified in the AC Characteristics section of this document. The configuration latches will capture the value of the shift register on the HIGH-to-LOW edge of the S_LOAD input. See PROGRAMMING INTERFACE for more information. The TEST output reflects various internal node values, and is controlled by the T[2:0] bits in the serial data stream. In order to minimize the PLL jitter, it is recommended to avoid active signal on the TEST output. The PWR_DOWN pin, when asserted, will synchronously divide the f_{OUT} by 16. The power down sequence is clocked by the PLL reference clock, thereby causing the frequency reduction to happen relatively slowly. Upon de-assertion of the PWR_DOWN pin, the f_{OUT} input will step back up to its programmed frequency in four discrete increments.

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

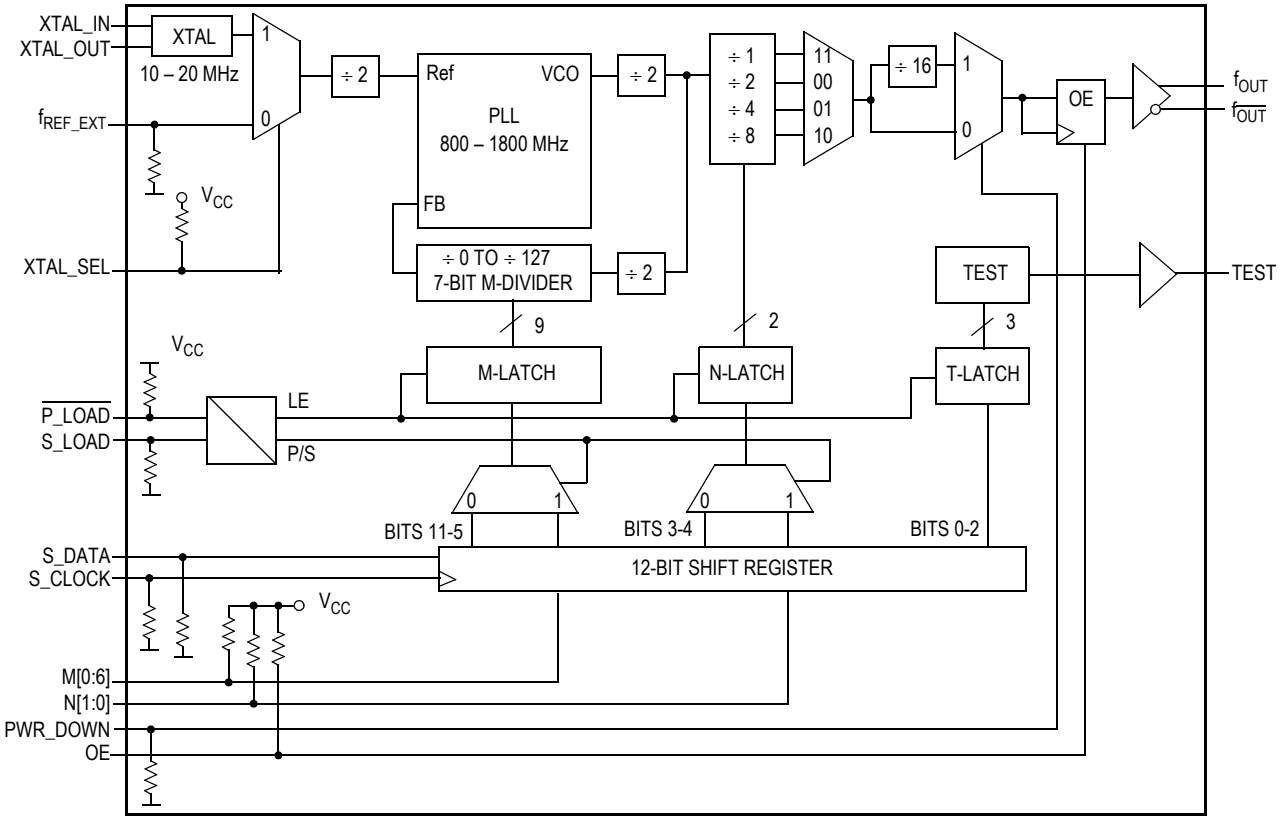


Figure 1. MPC92459 Logic Diagram

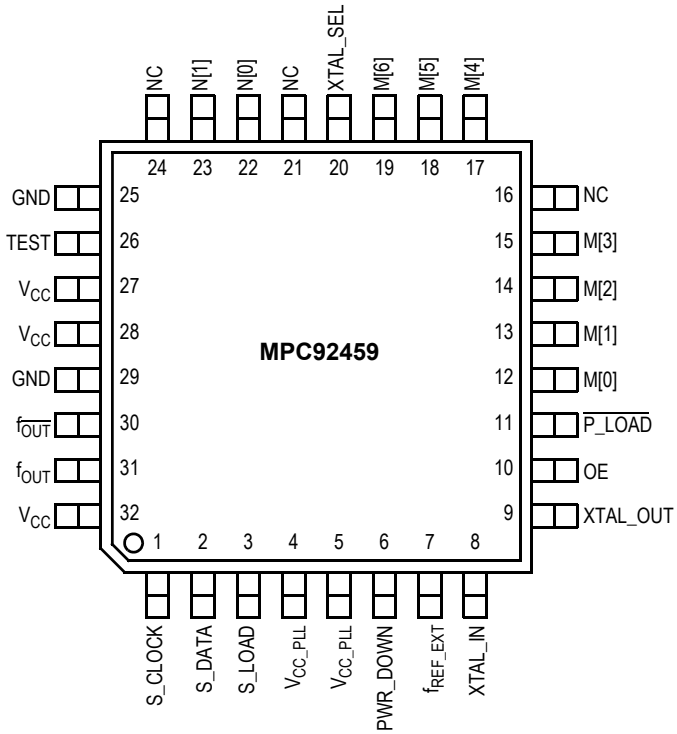


Figure 2. MPC92459 32-Lead LQFP Pinout
(Top View)

Table 1. Pin Configurations

Pin	I/O	Default	Type	Function
XTAL_IN, XTAL_OUT			Analog	Crystal oscillator interface
f_{REF_EXT}	Input	0	LVCMOS	Alternative PLL reference input
f_{OUT}, $f_{\overline{OUT}}$	Output		LVDS	Differential clock output
TEST	Output		LVCMOS	Test and device diagnosis output
XTAL_SEL	Input	1	LVCMOS	PLL reference select input
PWR_DOWN	Input	0	LVCMOS	Configuration input for power down mode. Assertion (deassertion) of power down will decrease (increase) the output frequency by a ratio of 16 in 4 discrete steps. PWR_DOWN assertion (deassertion) is synchronous to the input reference clock.
S_LOAD	Input	0	LVCMOS	Serial configuration control input. This inputs controls the loading of the configuration latches with the contents of the shift register. The latches will be transparent when this signal is high, thus the data must be stable on the high-to-low transition.
P_LOAD	Input	1	LVCMOS	Parallel configuration control input. this input controls the loading of the configuration latches with the content of the parallel inputs (M and N). The latches will be transparent when this signal is low, thus the parallel data must be stable on the low-to-high transition of $\overline{P\_LOAD}$. $\overline{P\_LOAD}$ is state sensitive.
S_DATA	Input	0	LVCMOS	Serial configuration data input.
S_CLOCK	Input	0	LVCMOS	Serial configuration clock input.
M[0:6]	Input	1	LVCMOS	Parallel configuration for PLL feedback divider (M). M is sampled on the low-to-high transition of $\overline{P\_LOAD}$.
N[1:0]	Input	1	LVCMOS	Parallel configuration for Post-PLL divider (N). N is sampled on the low-to-high transition of $\overline{P\_LOAD}$
OE	Input	1	LVCMOS	Output enable (active high) The output enable is synchronous to the output clock to eliminate the possibility of runt pulses on the f_{OUT} output. OE = L low stops f_{OUT} in the logic low state (f_{OUT} = L, $f_{\overline{OUT}}$ = H).
GND	Supply		Ground	Negative power supply (GND).
V_{CC}	Supply		V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation.
V_{CC_PLL}	Supply		V_{CC}	PLL positive power supply (analog power supply).

Table 2. Output Frequency Range and PLL Post-Divider N

PWR_DOWN	N		VCO Output Frequency Division	f_{OUT} Frequency Range
	1	0		
0	0	0	2	200 – 450 MHz
0	0	1	4	100 – 225 MHz
0	1	0	8	50 – 112.5 MHz
0	1	1	1	400 – 900 MHz
1	0	0	32	12.5 – 28.125 MHz
1	0	1	64	6.25 – 14.0625 MHz
1	1	0	128	3.125 – 7.03125 MHz

Table 3. Function Table

Input	0	1
XTAL_SEL	FREF_EXT	XTAL interface
OE	Outputs disabled. f_{OUT} is stopped in the logic low state (f_{OUT} = L, $f_{\overline{OUT}}$ = H)	Outputs enabled
PWR_DOWN	Output divider ÷ 1	Output divider ÷ 16

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
LU	Latch-up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs (f_{REF_EXT}, PWR_DOWN, XTAL_SEL, $\overline{P\_LOAD}$, S_LOAD, S_DATA, S_CLOCK, M[0:6], N[0:1], OE)						
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
I_{IN}	Input Current[2]			±200	µA	V_{IN} = V_{CC} or GND
Differential Clock Output f_{OUT}						
V_{PP}	Output Differential Voltage (peak-to-peak)	250			mV	LVDS
V_{OS}	Output Offset Voltage	1125		1275	mV	LVDS
Test and Diagnosis Output TEST						
V_{OH}	Output High Voltage	2.0			V	I_{OH} =–0.8 mA
V_{OL}	Output Low Voltage			0.55	V	I_{OL} = 0.8 mA
Supply Current						
I_{CC_PLL}	Maximum PLL Supply Current			20	mA	V_{CC_PLL} Pins
I_{CC}	Maximum Supply Current			110	mA	All V_{CC} Pins

1. All AC characteristics are design targets and subject to change upon device characterization.
2. Inputs have pull-down resistors affecting the input current.

Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to +70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{XTAL}	Crystal Interface Frequency Range		10		20	MHz	
f_{VCO}	VCO Frequency Range[2]		800		1800	MHz	
f_{MAX}	Output Frequency	N = 11 (÷ 1) N = 00 (÷ 2) N = 01 (÷ 4) N = 10 (÷ 8)	400 200 100 50		900 450 225 112.5	MHz MHz MHz MHz	PWR_DOWN = 0
f_{S_CLOCK}	Serial Interface Programming Clock Frequency[3]		0		10	MHz	
$t_{P,MIN}$	Minimum Pulse Width	(S_LOAD, $\overline{P\_LOAD}$)	50			ns	
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.05		TBD	ns	20% to 80%
t_S	Setup Time	S_DATA to S_CLOCK S_CLOCK to $\overline{S\_LOAD}$ M, N to $\overline{P\_LOAD}$	20 20 20			ns ns ns	
t_S	Hold Time	S_DATA to $\overline{S\_CLOCK}$ M, N to $\overline{P\_LOAD}$	20 20			ns ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	RMS (1 σ)[4]		TBD	TBD	ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1 σ)			±25	ps	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. All AC characteristics are design targets and subject to change upon device characterization.
2. The input frequency f_{XTAL} and the PLL feedback divider M must match the VCO frequency range: $f_{VCO} = f_{XTAL} \cdot 2 \cdot M$.
3. The frequency of S_CLOCK is limited to 10 MHz in serial programming mode. S_CLOCK can be switched at higher frequencies when used as test clock in test mode 6. See APPLICATIONS INFORMATION for more details.
4. Refer to the application section for a jitter calculation for other confidence factors than 1 σ.

Table 8. MPC92459 Frequency Operating Range (in MHz)

M	M[6:0]	VCO frequency for a crystal interface frequency of						Output frequency for f_{XTAL} = 16 MHz and for N =			
		10 MHz	12 MHz	14 MHz	16 MHz	18 MHz	20 MHz	1	2	4	8
20	0010100						800				
21	0010101						840				
22	0010110						880				
23	0010111					828	920				
24	0011000					864	960				
25	0011001				800	900	1000	400	200	100	50
26	0011010				832	936	1040	416	208	104	52
27	0011011				864	972	1080	432	216	108	54
28	0011100			812	896	1008	1120	448	224	112	56
29	0011101			840	928	1044	1160	464	232	116	58
30	0011110			875	960	1080	1200	480	240	120	60
31	0011111			868	992	1116	1240	496	248	124	62
32	0100000			896	1024	1152	1280	512	256	128	64
33	0100001			924	1056	1188	1320	528	264	132	66
34	0100010		816	952	1088	1224	1360	544	272	136	68
35	0100011		840	980	1120	1260	1400	560	280	140	70
36	0100100		864	1008	1152	1296	1440	576	288	144	72
37	0100101		888	1036	1184	1332	1480	592	296	148	74
38	0100110		912	1064	1216	1368	1520	608	304	152	76
39	0100111		936	1092	1248	1404	1560	624	312	156	78
40	0101000	800	960	1120	1280	1440	1600	640	320	160	80
41	0101001	820	984	1148	1312	1476	1640	656	328	164	82
42	0101010	840	1008	1176	1344	1512	1680	672	336	168	84
43	0101011	860	1032	1204	1376	1548	1720	688	344	172	86
44	0101100	880	1056	1232	1408	1584	1760	704	352	176	88
45	0101101	900	1080	1260	1440	1620	1800	720	360	180	90
46	0101110	920	1104	1288	1472	1656		736	368	184	92
47	0101111	940	1128	1316	1504	1692		752	376	188	94
48	0110000	960	1152	1344	1536	1728		768	384	192	96
49	0110001	980	1176	1372	1568	1764		784	392	196	98
50	0110010	1000	1200	1400	1600	1800		800	400	200	100
51	0110011	1020	1224	1428	1632			816	408	204	102
52	0110100	1040	1248	1456	1664			832	416	208	104
53	0110101	1060	1272	1484	1696			848	424	212	106
54	0110110	1080	1296	1512	1728			864	432	216	108
55	0110111	1100	1320	1540	1760			880	440	220	110
56	0111000	1120	1344	1568	1792			896	448	224	112
57	0111001	1140	1368	1596							
58	0111010	1160	1392	1624							
59	0111011	1180	1416	1652							
60	0111100	1200	1440	1680							
61	0111101	1220	1488	1736							
62	0111110	1260	1512	1764							
63	0111111	1260	1512	1764							
64	1000000	1280	1536	1792							
...		...	...	...							

PROGRAMMING INTERFACE

Programming the MPC92459

Programming the MPC92459 amounts to properly configuring the internal PLL dividers to produce the desired synthesized frequency at the output. The output frequency can be represented by this formula:

$$f_{OUT} = (f_{XTAL} \div 2) \cdot (M \cdot 4) \div (N \cdot 2) \text{ or} \quad (1)$$

$$f_{OUT} = f_{XTAL} \cdot M \div N \quad (2)$$

where f_{XTAL} is the crystal frequency, M is the PLL feedback-divider and N is the PLL post-divider. The input frequency and the selection of the feedback divider M is limited by the VCO-frequency range. f_{XTAL} and M must be configured to match the VCO frequency range of 800 to 1800 MHz in order to achieve stable PLL operation:

$$M_{MIN} = f_{VCO,MIN} \div (2 \cdot f_{XTAL}) \text{ and} \quad (3)$$

$$M_{MAX} = f_{VCO,MAX} \div (2 \cdot f_{XTAL}) \quad (4)$$

For instance, the use of a 16 MHz input frequency requires the configuration of the PLL feedback divider between M = 25 and M = 56. Table 8 shows the usable VCO frequency and M divider range for other example input frequencies.

Assuming that a 16 MHz input frequency is used, equation (2) reduces to:

$$f_{OUT} = 16\ M \div N$$

Substituting N for the four available values for N (1, 2, 4, 8) yields:

Table 9. Output Frequency Range for f_{XTAL} = 16 MHz

N			f_{OUT}	f_{OUT} Range	f_{OUT} Step
1	0	Value			
0	0	2	8 · M	200 – 450 MHz	8 MHz
0	1	4	4 · M	100 – 225 MHz	4 MHz
1	0	8	2 · M	50 – 112.5 MHz	2 MHz
1	1	1	16 · M	400 – 900 MHz	16 MHz

Example Calculation for an 16 MHz Input Frequency

For example, if an output frequency of 384 MHz was desired, the following steps would be taken to identify the appropriate M and N values. 384 MHz falls within the frequency range set by an N value of 2, so N[1:0]=00. For N = 2, $f_{OUT} = 8 \cdot M$ and $M = f_{OUT} \div 8$. Therefore, $M = 384 \div 8 = 48$, so M[6:0] = 0110000. Following this procedure a user can generate any whole frequency between 50 MHz and 900 MHz. The size of the programmable frequency steps will be equal to:

$$f_{STEP} = f_{XTAL} \div N$$

APPLICATIONS INFORMATION

Using the Parallel and Serial Interface

The M and N counters can be loaded either through a parallel or serial interface. The parallel interface is controlled via the P_LOAD signal such that a LOW to HIGH transition will latch the information present on the M[6:0] and N[1:0] inputs into the M and N counters. When the P_LOAD signal is LOW the input latches will be transparent and any changes on the M[6:0] and N[1:0] inputs will affect the f_{OUT} output pair. To use the serial port the S_CLOCK signal samples the information on the S_DATA line and loads it into a 12 bit shift register. Note that the P_LOAD signal must be HIGH for the serial load operation to function. The Test register is loaded with the first three bits, the N register with the next two, and the M register with the final eight bits of the data stream on the S_DATA input. For each register the most significant bit is loaded first (T2, N1, and M6). A pulse on the S_LOAD pin after the shift register is fully loaded will transfer the divide values into the counters. The HIGH to LOW transition on the S_LOAD input will latch the new divide values into the counters. Figure 3 illustrates the timing diagram for both a parallel and a serial load of the MPC92459 synthesizer.

M[6:0] and N[1:0] are normally specified once at power-up through the parallel interface, and then possibly again through the serial interface. This approach allows the application to come up at one frequency and then change or fine-tune the clock as the ability to control the serial interface becomes available.

Using the Test and Diagnosis Output TEST

The TEST output provides visibility for one of the several internal nodes as determined by the T[2:0] bits in the serial configuration stream. It is not configurable through the parallel interface. Although it is possible to select the node that represents f_{OUT}, the LVCMOS output is not able to toggle fast enough for higher output frequencies and should only be used for test and diagnosis.

The T2, T1, and T0 control bits are preset to '000' when P_LOAD is LOW so that the PECL f_{OUT} outputs are as jitter-free as possible. Any active signal on the TEST output pin will have detrimental affects on the jitter of the PECL output pair. In normal operations, jitter specifications are only guaranteed if the TEST output is static. The serial configuration port can be used to select one of the alternate functions for this pin.

Most of the signals available on the TEST output pin are useful only for performance verification of the MPC92459 itself. However, the PLL bypass mode may be of interest at the board level for functional debug. When T[2:0] is set to 110 the MPC92459 is placed in PLL bypass mode. In this mode the S_CLOCK input is fed directly into the M and N dividers. The N divider drives the f_{OUT} differential pair and the M counter drives the TEST output pin. In this mode the S_CLOCK input could be used for low speed board level functional test or debug. Bypassing the PLL and driving f_{OUT} directly gives the user more control on the test clocks sent through the clock tree shows the functional setup of the PLL bypass mode. Because the S_CLOCK is a CMOS level the input frequency is limited to 200 MHz. This means the fastest the f_{OUT} pin can be toggled via the S_CLOCK is 100 MHz as the divide ratio of the Post-PLL divider is 2 (if N = 1). Note that the M counter output on the TEST output will not be a 50% duty cycle.

Table 10. Test and Debug Confutation for TEST

T[2:0]			TEST Output
T2	T1	T0	
0	0	0	12-bit shift register out[1]
0	0	1	Logic 1
0	1	0	$f_{XTAL} \div 2$
0	1	1	M-Counter out
1	0	0	f_{OUT}
1	0	1	Logic 0
1	1	0	M-Counter out in PLL-bypass mode
1	1	1	$f_{OUT} \div 4$

1. Clocked out at the rate of S_CLOCK

Table 11. Debug Configuration for PLL Bypass[1]

Output	Configuration
f_{OUT}	S_CLOCK ÷ N
TEST	M-Counter out[2]

1. T[2:0] = 110. AC specifications do not apply in PLL bypass mode
2. Clocked out at the rate of S_CLOCK ÷ (2 · N)

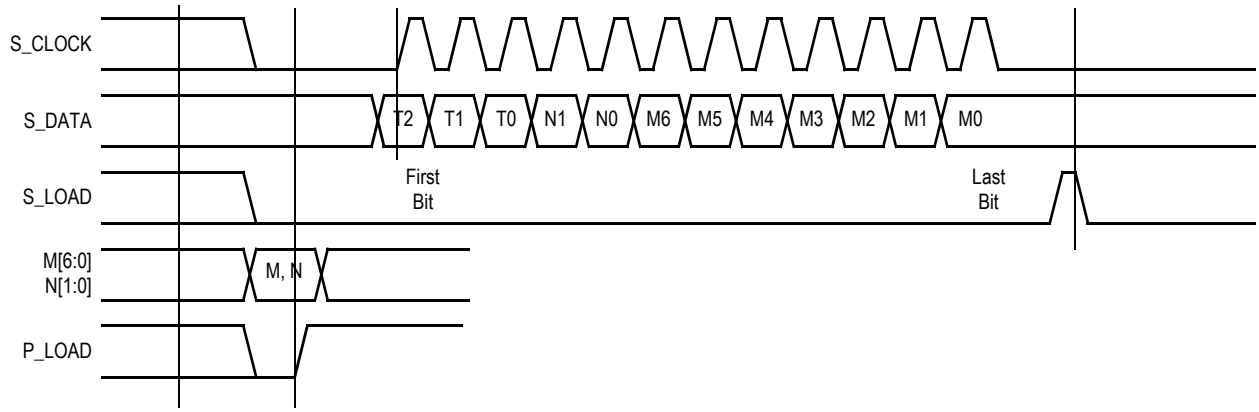


Figure 3. Serial Interface Timing Diagram

Power Supply Filtering

The MPC92459 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC92459 provides separate power supplies for the digital circuitry (V_{CC}) and the internal PLL (V_{CC_PLL}) of the device. The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board, this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC92459. Figure 4 illustrates a typical power supply filter scheme. The MPC92459 is most susceptible to noise with spectral content in the 1 kHz to 1 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the MPC92459 pin of the MPC92459. From the data sheet, the V_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically TBD mA (TBD maximum), assuming that a minimum of 3.135 V must be maintained on the V_{CC_PLL} pin, very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 4 must have a resistance of TBD Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Generally, the resistor/capacitor filter will be cheaper, easier to implement and provide an adequate level of supply filtering. A higher level of attenuation can be achieved by replacing the resistor with an appropriate valued inductor. A 1000 μH choke will show a significant impedance at 10 kHz frequencies and above. Because of the current draw and the voltage that must be maintained on the V_{CC_PLL} pin, a low DC resistance inductor is required (less than TBD Ω).

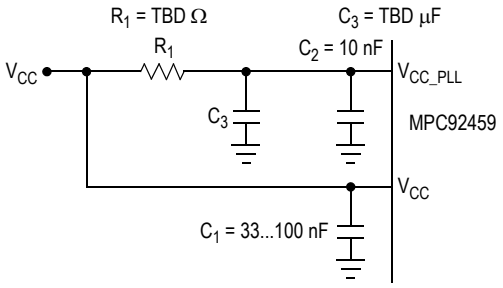


Figure 4. V_{CC_PLL} Power Supply Filter

Order number: MPC926508
Rev 2, 02/2004

Networking Clock Source

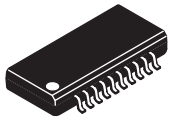
MPC926508

NETWORKING CLOCK SOURCE

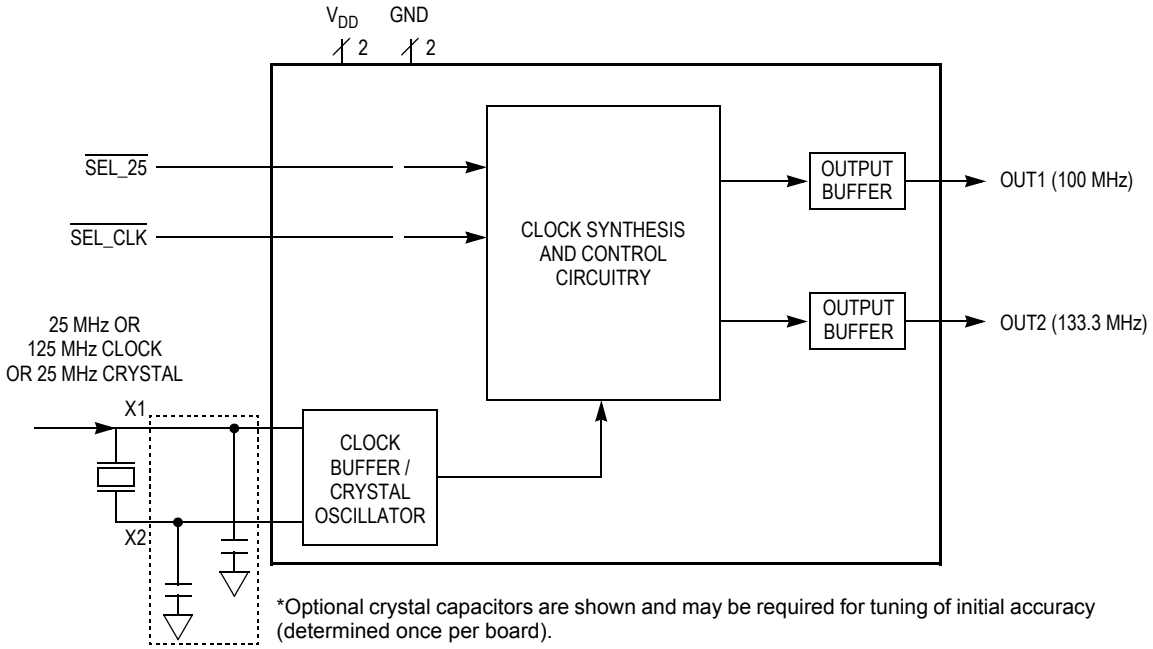
The MPC926508 is a low cost, low jitter, high performance clock synthesizer for networking applications. Using analog Phase-Locked Loop (PLL) techniques, the device accepts an input to produce multiple output clocks for networking chips, PCI devices, SDRAM, and ASICs. The MPC926508 outputs all have 0 ppm synthesis error.

Features

- Packaged in 20 pin narrow (150 mil) SSOP (QSOP)
- 25 or 125 MHz fundamental clock input or 25 MHz crystal input
- Two output clocks
- SDRAM frequencies of 100 and 133 MHz
- Zero ppm synthesis error in all clocks
- Full CMOS output swing with 25 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 3.3 V operating voltage



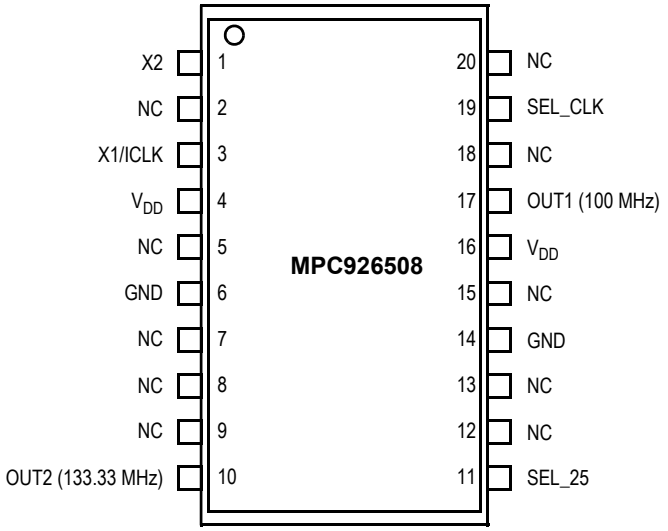
SD SUFFIX
20 LEAD SSOP
CASE 1461-01



*Optional crystal capacitors are shown and may be required for tuning of initial accuracy (determined once per board).

Table 1. Function Table

Control	Default	0	1
SEL_25	1	125	25
SEL_CLK	1	XTAL	REF_CLK



NC = Not Connected

Figure 1. MPC926508 Pin Assignment

Table 2. Pin Description

Number	Name	Type	Description
1	X2	XO	Crystal connection. Connect to a crystal or leave unconnected for a clock input.
2	NC	—	Not Connected
3	X1/ICLK	XI	Crystal connection. Connect to a fundamental crystal or clock input.
4	V_{DD}	P	Connect to +3.3 V. Must be same as other V_{DD}.
5	NC	—	Not Connected
6	GND	P	Connect to ground.
7	NC	—	Not Connected
8	NC	—	Not Connected
9	NC	—	Not Connected
10	OUT1 (133.33 MHz)	O	133.33 MHz Output
11	SEL_25	I	REF_CLK or XTAL Input Selection.
12	NC	—	Not Connected
13	NC	—	Not Connected
14	GND	P	Connect to ground.
15	NC	—	Not Connected
16	V_{DD}	P	Connect to +3.3 V. Must be same as other V_{DD}.
17	OUT2 (100 MHz)	O	100 MHz Output
18	NC	—	Not Connected
19	SEL_CLK	I	25 or 125 MHz REF_CLK Selection.
20	NC	—	Not Connected

Key: XI, XO = crystal connections; I = Input with internal pull-up resistor; O = Output; P = power supply connection.

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{DD}	Supply Voltage			3.9	V	Referenced to GND
	Inputs and Clock Outputs	–0.5		V_{DD} + 0.5	V	Referenced to GND
T_A	Ambient Operating Temperature	0		70	°C	
T_A	Ambient Operating Temperature, I version	–40		85	°C	Industrial temp
T_{SOL}	Soldering Temperature			260	°C	Max of 20 seconds
T_S	Storage Temperature	–65		150	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. DC Characteristics (V_{DD} = 3.3 V ± 10%, T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage X1 pin only all I type inputs	V_{DD}/2 + 1 2	V_{DD}/2		V V	
V_{IL}	Input Low Voltage X1 pin only all I type inputs		V_{DD}/2	V_{DD}/2–1 0.8	V V	
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –25 mA
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 25 mA
V_{OH}	Output High Voltage, CMOS level	V_{DD} – 0.4			V	I_{OH} = –8 mA
I_{DD}	Operating Supply Current		35		mA	No Load
	Short Circuit Current		90		mA	Each Output
	Internal Pull-Up Resistor		200		kΩ	SEL_25, SEL_CLK

Table 5. AC Characteristics (V_{DD} = 3.3 V ± 10%, T_A = –40°C to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{REF}	Input Frequency	12	25	27	MHz	Crystal Oscillator
f_{REF}	Input Frequency		125		MHz	External Input
t_r	Output Clock Rise Time		1		ns	0.8 to 2.0 V
t_f	Output Clock Fall Time		1		ns	2.0 to 0.8 V
DC_O	Output Clock Duty Cycle	40	50	60	%	At V_{DD}/2
	Frequency Error			0	ppm	All clocks
$t_{JIT(CC)}$	Jitter (Cycle-to-Cycle)		300		ps	Variation from mean

APPLICATIONS INFORMATION

External Components

The MPC926508 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01 μF should be connected between each V_{DD} and GND (pins 4 and 6, pins 16, and 14), as close to the MPC926508 as possible. A series termination resistor of 33 Ω may be used for each clock output. The crystal must be connected as close to the chip as possible. The crystal should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation, where C_L is the crystal load capacitance: Crystal caps (pF) = (C_L–6) x 2. So for a crystal with 16 pF load capacitance, two 20 pF caps should be used.

Order number: MPC9994
Rev 1, 03/2001

HSTL Low Voltage Differential Clock

MPC9994

HSTL LOW VOLTAGE DIFFERENTIAL CLOCK SYNTHESIZER FOR 340 – 360 MHz

The MPC9994 is a low voltage 3.3 V, HSTL differential clock synthesizer. The clock is designed to support single and multiple processor systems requiring HSTL differential inputs. The MPC9994 supports two differential HSTL output pairs that may be operated from 340 MHz to 640 MHz.

Features

- 2 clock outputs: (PCLK0 and PCLK1), each fully selectable
- Fully integrated PLL
- Output frequencies from 340 MHz to 640 MHz
- HSTL outputs
- HSTL and LVPECL reference clocks
- 32-lead LQFP packaging

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

Functional Description

The fully integrated Phase Locked Loop multiplies the HSTL_CLK input or the PECL_CLK input frequency to the desired processor clock frequency.

The PLL may be bypassed for test purposes such that the PCLK outputs are fed directly from the HSTL_CLK or PECL_CLK input.

All outputs are HSTL. The PCLK outputs are capable of driving 25 Ω to ground with at least 600 mV p-p signals. The EXTFB_OUT is capable of driving 50 Ω ground with at least a 600 mV p-p signal. For on-chip power reduction, the outputs are powered from 1.8 V external supply. For zero delay applications the buffer can operate with either external or internal feedback.

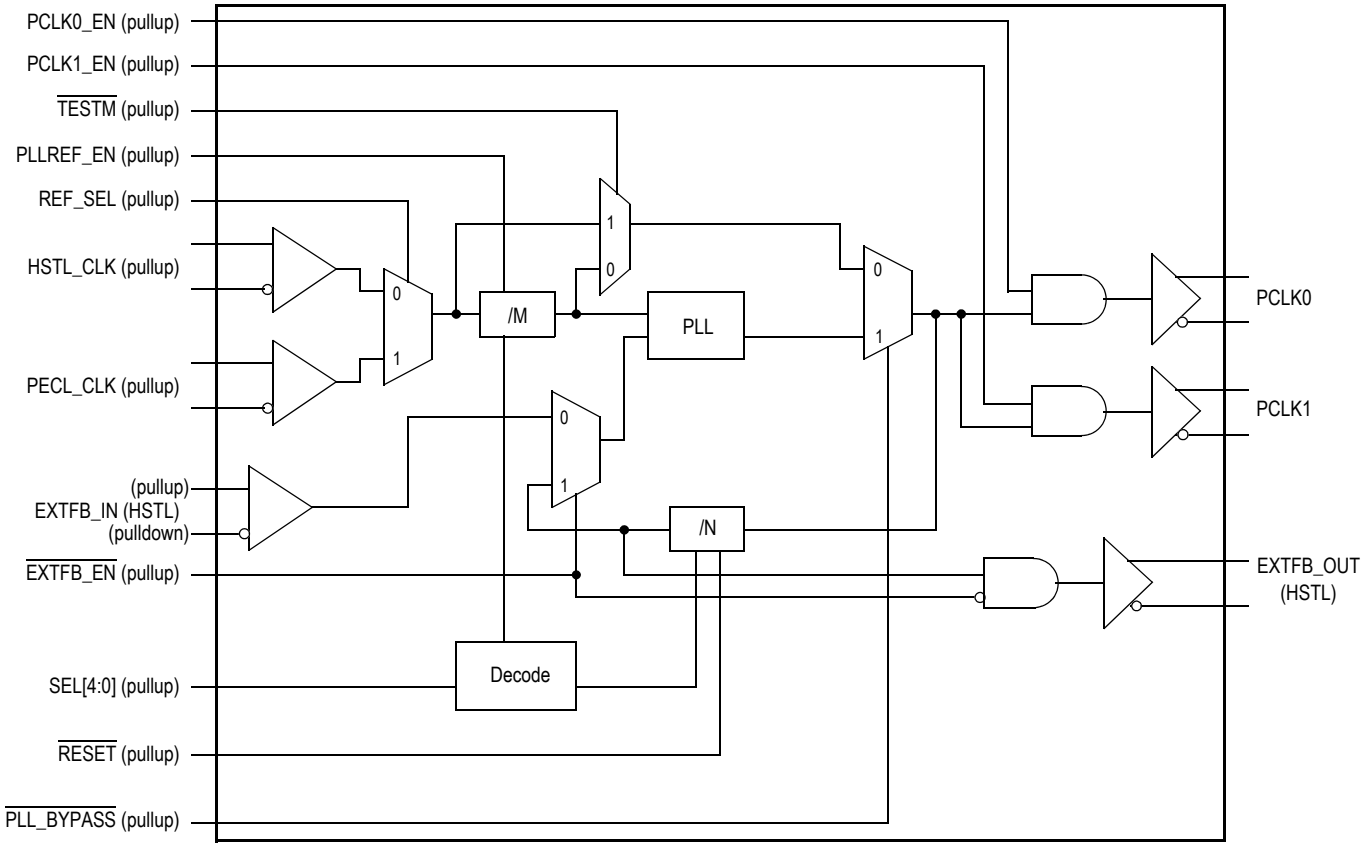


Figure 1. MPC9994 Logic Diagram

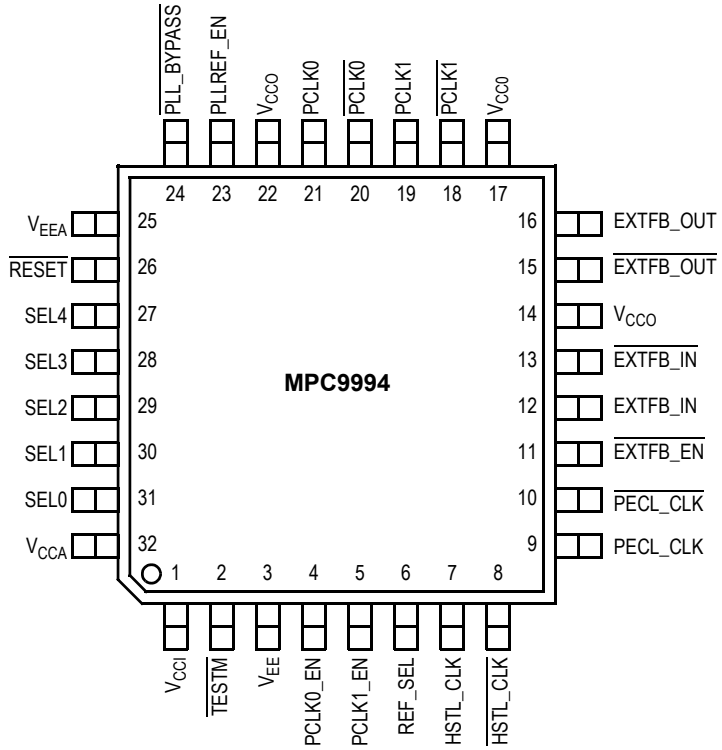


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin #	Pin	I/O Type	Type	Description
1	V_{CCI}	Power	Power Supply	3.3 V
2	TESTM	Input	LVCMOS	M divider test pins
3	V_{EE}	Power (GND)	Ground	Digital GND
4	PCLK0_EN	Input	LVCMOS	PCLK0 enable
5	PCLK1_EN	Input	LVCMOS	PCLK1 enable
6	REF_SEL	Input	LVCMOS	Selects the PLL input reference clock
7	HSTL_CLK	Input	Differential HSTL	PLL reference clock input
8	HSTL_CLK	Input	Differential HSTL	PLL reference clock input
9	PECL_CLK	Input	Differential LVPECL	PLL reference clock input
10	PECL_CLK	Input	Differential LVPECL	PLL reference clock input
11	$\overline{\text{EXTFB\_EN}}$	Input	LVCMOS	External feedback enable
12	EXTFB_IN	Input	Differential HSTL	External feedback input
13	$\overline{\text{EXTFB\_IN}}$	Input	Differential HSTL	External feedback input
14	V_{CCO}	Power	Power Supply	Output buffers power supply
15	$\overline{\text{EXTFB\_OUT}}$	Output	Differential HSTL	External feedback output clock
16	EXTFB_OUT	Output	Differential HSTL	External feedback output clock
17	V_{CCO}	Power	Power Supply	Ouput buffers power supply
18	$\overline{\text{PCLK1}}$	Output	Differential HSTL	Output clock 1
19	PCLK1	Output	Differential HSTL	Output clock 1
20	$\overline{\text{PCLK0}}$	Output	Differential HSTL	Output clock 0
21	PCLK0	Output	Differential HSTL	Output clock 0
22	V_{CCO}	Power	Power Supply	Ouput buffers power supply
23	PLLREF_EN	Input	LVCMOS	PLL reference enable
24	$\overline{\text{PLL\_BYPASS}}$	Input	LVCMOS	Input signal PLL bypass
25	V_{EEA}	Power (GND)	Ground	Analog GND for PLL
26	$\overline{\text{RESET}}$	Input	LVCMOS	PLL bypass reset (for test use)
27	SEL[4]	Input	LVCMOS	Selection of input and feedback frequency
28	SEL[3]	Input	LVCMOS	Selection of input and feedback frequency
29	SEL[2]	Input	LVCMOS	Selection of input and feedback frequency
30	SEL[1]	Input	LVCMOS	Selection of input and feedback frequency
31	SEL[0]	Input	LVCMOS	Selection of input and feedback frequency
32	V_{CCA}	Power	Power Supply	3.3 V filtered for PLL (PLL power supply)

Table 2. Frequency Selection Table

SEL					Input Divide	Feedback Divide
4	3	2	1	0	M	N
0	0	0	0	0	5	16
0	0	0	0	1	5	17
0	0	0	1	0	5	18
0	0	0	1	1	5	19
0	0	1	0	0	5	20
0	0	1	0	1	5	21
0	0	1	1	0	5	22
0	0	1	1	1	5	23
0	1	0	0	0	5	24
0	1	0	0	1	5	25
0	1	0	1	0	5	26
0	1	0	1	1	5	27
0	1	1	0	0	5	28
0	1	1	0	1	5	29
0	1	1	1	0	5	30
0	1	1	1	1	5	31
1	0	0	0	0	5	32
1	0	0	0	1	5	33
1	0	0	1	0	5	34
1	0	0	1	1	5	35
1	0	1	0	0	5	36
1	0	1	0	1	5	37
1	0	1	1	0	5	38
1	0	1	1	1	5	39
1	1	0	0	0	5	40
1	1	0	0	1	5	41
1	1	0	1	0	5	42
1	1	0	1	1	5	43
1	1	1	0	0	5	44
1	1	1	0	1	5	45
1	1	1	1	0	5	46
1	1	1	1	1	5	47

Table 3. Function Table (Controls)

Control Pin	0	1
REF_SEL	HSTL_CLK	PECL_CLK
TESTM	M divider test mode enabled	Reference fed to Bypass mux
PLLREF_EN	Disable the input to the PLL and reset the M divider	Enable the input to the PLL
$\overline{\text{PLL\_BYPASS}}$	Outputs fed by input reference or M divider	Outputs fed by VCO
$\overline{\text{EXTFB\_EN}}$	External feedback enabled	Internal feedback enabled
PCLK0_EN	PCLK0 = low, $\overline{\text{PCLK0}}$ = high	PCLK0 = high, $\overline{\text{PCLK0}}$ = low
PCLK1_EN	PCLK1 = low, $\overline{\text{PCLK1}}$ = high	PCLK1 = high, $\overline{\text{PCLK1}}$ = low
$\overline{\text{RESET}}$	Resets feedback N divider	Feedback enabled
SEL[4:0]	See Table 2.Frequency Selection Table	

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.5	4.4	V	
V_{CCO}	Output Supply Voltage	–0.5	4.4	V	
V_{IN}	Input Voltage	–0.5	VCC + 0.3	V	
I_{IN}	Input Current	–1	1	mA	
T_S	Storage Temperature	–50	150	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics ($V_{CCA} = V_{CCI} = 3.3$ V ± 5%, $V_{CCO} = 1.7$ to 2.1 V, $T_A = 0$ to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
VIH	Input High Voltage	2.0		VCCI	V	LVCMOS
VIL	Input Low Voltage	0.0		0.8	V	LVCMOS
VCMR	Input High Voltage[1]	1		V_{CCI} – 0.3	V	LVPECL
VPP	Input Low Voltage[1]	0.5		1	V	LVPECL[2]
V_{IN}(dc)	DC Input Signal Voltage	–0.3		1.45	V	HSTL[3]
V_{DIF}(dc)	DC Differential Input Voltage	0.4		1.75	V	HSTL[4]
V_{CM}(dc)	DC Common Mode Input Voltage	0.4		1.0	V	HSTL[5]
VOH	Output High Voltage	V_X + 0.3	V_X + 0.5	1.4	V	HSTL[6,1]
VOL	Output Low Voltage	0.0	V_X – 0.5	V_X – 0.3	V	HSTL[6]
ICCI	Core Supply Current			140	mA	
ICCA	PLL Supply Current		15	20	mA	
ICCO	Output Supply Current		150		mA	Note [7]
$Theta_{JA}$	Junction to Ambient Thermal Resistance		53		°C/W	Note [8]

1. DC levels will vary 1:1 with V_{CC}.
2. V_{PP} minimum and maximum required to maintain AC specifications. Actual device function will tolerate minimum V_{PP} of 200 mV.
3. V_{IN} (dc) specifies the maximum allowable dc excursion of each differential input.
4. V_{DIF} (dc) specifies the minimum input differential voltage ($V_{TR} – V_{CP}$) required for switching, where V_{TR} is the “true” input signal and V_{CP} is the “complement” input signal.
5. V_{CM}(dc) specifies the maximum allowable range of input signal crosspoint voltage.
6. V_X is the differential output crosspoint voltage defined in the “AC CHARACTERISTICS” section.
7. 2 PCLK into 25 Ω and 1 EXTFB into 50 Ω.
8. Measured with 1.3 M/s (250 fpm) airflow

Table 6. AC Characteristics (V_{CCA} = V_{CCI} = 3.3 V ± 5%, V_{CCO} = 1.7 to 2.1 V, T_A = 0 to 70°C)

Symbol	Characteristics[1]	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		100 – 125		MHz	
f_{MAX}	Maximum Output Frequency	340		640	MHz	Note[2]
$t_{sk(o)}$	Skew Error (PCLK)			35	ps	Note[3]
$t_{jit(0)}$	Phase jitter (IO jitter)			output period / 2		Note[3]
$t_{jit(cc)}$	Cycle-to-cycle jitter (full period)			5%		Note[3, 4]
$t_{jit(1/2per)}$	Cycle-to-cycle jitter (half period)			6%	Note[4]	Note[3, 5]
V_{DIFout}	Differential Output pk-pk swing	0.6			V	For all HSTL output pairs
V_x	Differential output crosspoint voltage	0.68		0.9	V	For all HSTL output pairs
t_{lock}	Maximum PLL lock time			10	ms	

1. All PCLK outputs are terminated in 25 Ω to ground, EXTFB_OUT is terminated in 50 Ω to ground (applies to all measurements).
2. With PLL active but in bypass mode, f_{ref} Max is limited by input buffer; best performance is expected with PECL input.
3. Measured at differential pair crossover.
4. Reference to full PCLK period.
5. Reference to half PCLK period.

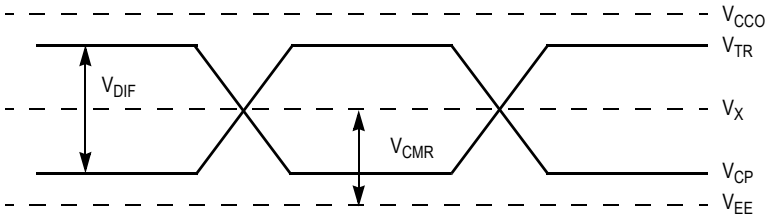


Figure 3. HSTL Differential Input Levels

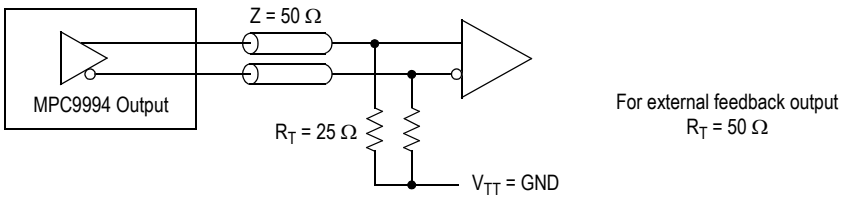


Figure 4. Output Termination and AC Test Reference

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9994 is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC9994 provides separate power supplies for the output buffers (V_{CCO}) and the phase-locked loop (V_{CCA}) of the device.

The purpose of this design technique is to try and isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC9994. Figure 5 illustrates a typical power supply filter scheme. The MPC9994 is most susceptible to noise with spectral content in the 10kHz to 1MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC9994. From the data sheet the I_{VCCA} current (the current sourced through the V_{CCA} pin) is typically 15 mA (20 mA maximum), assuming that a minimum of 3.3 V-5% must be maintained on the V_{CCA} pin. Very little DC voltage drop can be tolerated when a 3.3 V V_{CC} supply is used. The resistor shown in Figure 5 must have a resistance of 5–15 Ω to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. It is recommended that the user start with an 8–10 Ω resistor to avoid potential V_{CC} drop problems and only move to the higher value resistors when a higher level of attenuation is shown to be needed.

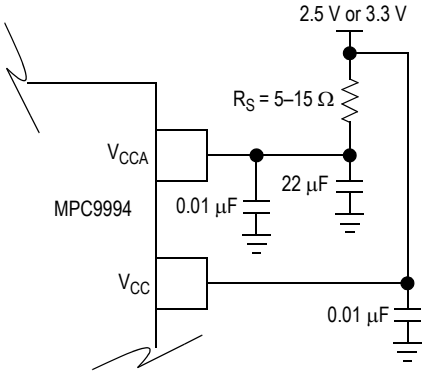


Figure 5. Power Supply Filter

Although the MPC9994 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Chapter Six
Zero-Delay Buffer Data Sheets

Zero-Delay Buffer Device Index

Order number: MPC9608
Rev 3, 08/2004

1:10 LVCMOS Zero Delay Clock Buffer

MPC9608

LOW VOLTAGE 3.3 V LVCMOS 1:10 ZERO-DELAY CLOCK BUFFER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

AC SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC9608 is a 3.3 V compatible, 1:10 PLL based zero-delay buffer. With a very wide frequency range and low output skews the MPC9608 is targeted for high performance and mid-range clock tree designs.

Features

- 1:10 outputs LVCMOS zero-delay buffer
- Single 3.3 V supply
- Supports a clock I/O frequency range of 12.5 to 200 MHz
- Selectable divide-by-two for one output bank
- Synchronous output enable control (CLK_STOP)
- Output tristate control (output high impedance)
- PLL bypass mode for low frequency system test purpose
- Supports networking, telecommunications and computer applications
- Supports a variety of microprocessors and controllers
- Compatible to PowerQuicc I and II
- Ambient Temperature Range -40°C to +85°C
- 32-lead Pb-free Package Available

Functional Description

The MPC9608 uses an internal PLL and an external feedback path to lock its low-skew clock output phase to the reference clock phase, providing virtually zero propagation delay. This enables nested clock designs with near-zero insertion delay. Designs using the MPC9608 as PLL fanout buffer will show significantly lower clock skew than clock distributions developed from traditional fanout buffers. The device offers one reference clock input and two banks of 5 outputs for clock fanout. The input frequency and phase is reproduced by the PLL and provided at the outputs. A selectable frequency divider sets the bank B outputs to generate either an identical copy of the bank A clocks or one half of the bank A clock frequency. Both output banks remain synchronized to the input reference for both bank B configurations.

Outputs are only disabled or enabled when the outputs are already in logic low state (CLK_STOP). For system test and diagnosis, the MPC9608 outputs can also be set to high-impedance state by connecting $\overline{OE}$ to logic high level. Additionally, the device provides a PLL bypass mode for low frequency test purpose. In PLL bypass mode, the minimum frequency and static phase offset specification do not apply.

CLK_STOP and $\overline{OE}$ do not affect the PLL feedback output (QFB) and down stream clocks can be disabled without the internal PLL losing lock.

The MPC9608 is fully 3.3 V compatible and requires no external components for the internal PLL. All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines on the incident edge. For series terminated transmission lines, each of the MPC9608 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

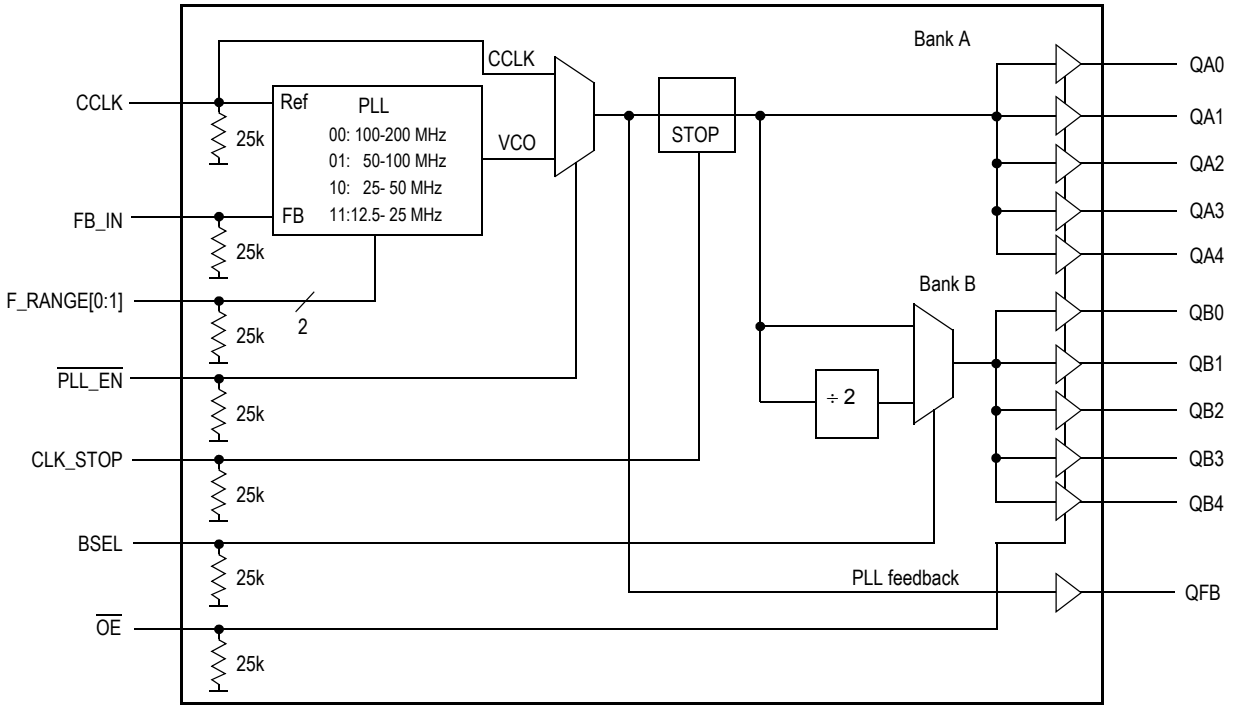


Figure 1. MPC9608 Logic Diagram

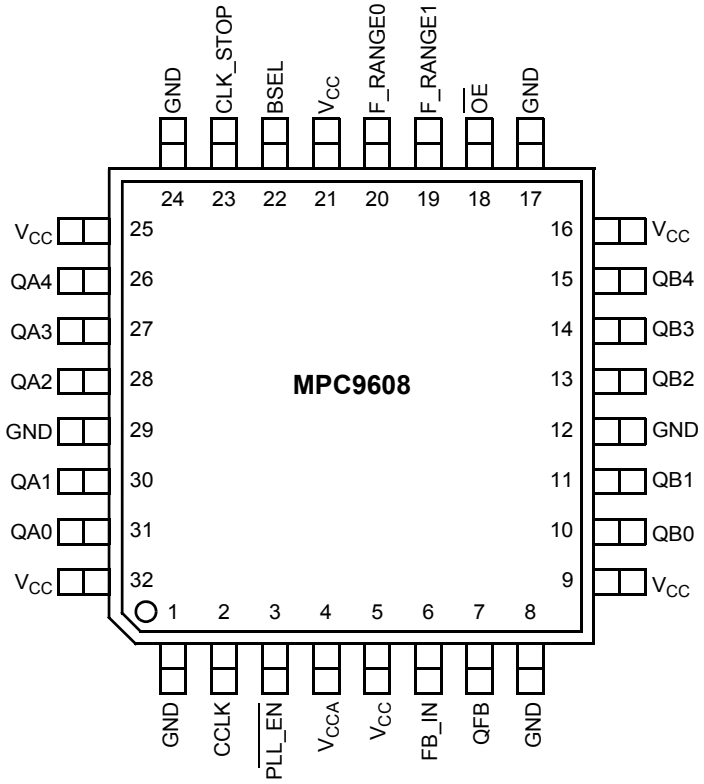


Figure 2. MPC9608 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVCMOS	PLL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to a QFB output
F_RANGE[0:1]	Input	LVCMOS	PLL frequency range select
BSEL	Input	LVCMOS	Frequency divider select for bank B outputs
PLL_EN	Input	LVCMOS	PLL enable/disable
OE	Input	LVCMOS	Output enable/disable (high-impedance tristate)
CLK_STOP	Input	LVCMOS	Synchronous clock enable/stop
QA0-4, QB0-4	Output	LVCMOS	Clock outputs
QFB	Output	LVCMOS	PLL feedback signal output. Connect to FB_IN
GND	Supply	Ground	Negative power supply
V_{CCA}	Supply	V_{CC}	PLL positive power supply (analog power supply). The MPC9608 requires an external RC filter for the analog power supply pin $V_{CCA.}$ Refer to the Applications Information section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
F_RANGE[0:1]	00	PLL frequency range. Refer to Table 3.Clock Frequency Configuration for QFB Connected to FB_INT	
BSEL	0	$f_{QB0-4} = f_{QA0-4}$	$f_{QB0-4} = f_{QA0-4} \div 2$
CLK_STOP	0	Outputs enabled	Outputs synchronously stopped in logic low state
$\overline{OE}$	0	Outputs enabled (active)	Outputs disabled (high-impedance state), independent on CLK_STOP. Applying $\overline{OE}$ = 1 and $\overline{PLL\_EN}$ = 1 resets the device. The PLL feedback output QFB is not affected by $\overline{OE}$.
$\overline{PLL\_EN}$	0	Normal operation mode with PLL enabled.	Test mode with PLL disabled. CCLK is substituted for the internal VCO output. MPC9608 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable. Applying $\overline{OE}$ = 1 and $\overline{PLL\_EN}$ = 1 resets the device.

Table 3. Clock Frequency Configuration for QFB Connected to FB_IN

F_RANGE[0]	F_RANGE[1]	BSEL	f_{REF} (CCLK) range [MHz]	QA0-QA4		QB0-B4		QFB
				Ratio	f_{QA0-4} [MHz]	Ratio	f_{QB0-4} [MHz]	
0	0	0	100.0 – 200.0	f_{REF}	100.0 – 200.0	f_{REF}	100.0 – 200.0	f_{REF}
0	0	1				$f_{REF} \div 2$	50.0 – 25.0	f_{REF}
0	1	0	50.0 – 100.0	f_{REF}	50.0 – 100.0	f_{REF}	50.0 – 100.0	f_{REF}
0	1	1				$f_{REF} \div 2$	25.0 – 50.0	f_{REF}
1	0	0	25.0 – 50.0	f_{REF}	25.0 – 50.0	f_{REF}	25.0 – 50.0	f_{REF}
1	0	1				$f_{REF} \div 2$	12.5 – 25.0	f_{REF}
1	1	0	12.5 – 25.0	f_{REF}	12.5 – 25	f_{REF}	12.5 – 25.0	f_{REF}
1	1	1				$f_{REF} \div 2$	6.25 – 12.5	f_{REF}

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		$V_{CC} \div 2$		V	
MM	ESD protection (Machine model)	200			V	
HBM	ESD protection (Human body model)	2000			V	
LU	Latch-up immunity	200			mA	
C_{PD}	Power dissipation capacitance		10		pF	Per output
C_{IN}	Input capacitance		4.0		pF	Inputs

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	-65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = -40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance		14 – 17		Ω	
I_{IN}	Input Current[2]			±200	μA	V_{IN} = V_{CC} or GND
I_{CCA}	Maximum PLL Supply Current		4.0	8.0	mA	V_{CCA} Pin
I_{CCQ}	Maximum Quiescent Supply Current		1.0	4.0	mA	All V_{CC} Pins

1. The MPC9608 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
2. Inputs have pull-down resistors affecting the input current.

Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = -40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input reference frequency in PLL mode[2]						
		F_RANGE = 00	100		200	MHz	
		F_RANGE = 01	50		100	MHz	
		F_RANGE = 10	25		50	MHz	
		F_RANGE = 11	12.5		25	MHz	
	Input reference frequency in PLL bypass mode[3]		0		200	MHz	
f_{max}	Output Frequency[4]	F_RANGE = 00	100		200	MHz	BSEL = 0
		F_RANGE = 01	50		100	MHz	BSEL = 0
		F_RANGE = 10	25		50	MHz	BSEL = 0
		F_RANGE = 11	12.5		25	MHz	BSEL = 0
$t_{PW, MIN}$	Reference Input Pulse Width[5]		2.0			ns	
t_r, t_f	CCLK Input Rise/Fall Time				1.0	ns	0.8 V to 2.0 V
$t_{(\varnothing)}$	Propagation Delay (SPO) CCLK to FB_IN						
		f_{REF} = 100 MHz and above	-175		+175	ps	PLL Locked
		f_{REF} = 12.5 MHz to 100 MHz	-1.75% of t_{PER}		+1.75% of t_{PER}	ps	
$t_{SK(o)}$	Output-to-Output Skew					ps	
		Within a bank			80		
		Bank-to-bank			100		
		All outputs, including QFB			150		
DC	Output Duty Cycle		45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 V to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-cycle Jitter				150	ps	BSEL = 0
$t_{JIT(PER)}$	Period Jitter				150	ps	BSEL = 0
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1 σ)			125	ps	BSEL = 0
BW	PLL closed loop bandwidth[6]	F_RANGE = 00		7 – 15		MHz	
		F_RANGE = 01		2 – 7		MHz	
		F_RANGE = 10		1 – 3		MHz	
		F_RANGE = 11		0.5 – 1.3		MHz	
t_{LOCK}	Maximum PLL Lock Time			10		ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. PLL mode requires PLL_EN = 0 to enable the PLL and zero-delay operation.
3. In bypass mode, the MPC9608 divides the input reference clock.
4. Applies for bank A and for bank B if BSEL = 0. If BSEL = 1, the minimum and maximum output frequency of bank B is divided by two.
5. Calculation of reference duty cycle limits: $DC_{REF, MIN} = t_{PW,MIN} * f_{REF} *100\%$ and $DC_{REF,MAX} = 100\% – DC_{REF,MIN}$. For example, at f_{REF} = 100 MHz the input duty cycle range is 20% < DC < 80%.
6. -3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC9608 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA} (PLL) power supply impacts the device characteristics, for instance I/O jitter. The MPC9608 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CCA} pin for the MPC9608. Figure 3 illustrates a typical power supply filter scheme. The MPC9608 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 4 mA (8 mA maximum), assuming that a minimum of 3.125 V must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 3 must have a resistance of 9 – 10 Ω (V_{CC} = 3.3 V) to meet the voltage drop criteria.

R_F = 9-10 Ω for V_{CC} = 3.3 V C_F = 1 μF for V_{CC} = 3.3 V

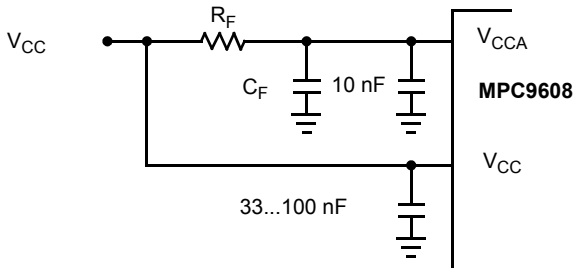


Figure 3. V_{CCA} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 3-5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9608 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL), there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9608 in Zero-delay Applications

Nested clock trees are typical applications for the MPC9608. Designs using the MPC9608, as LVCMOS PLL fanout buffer with zero insertion delay, will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9608 clock driver allows for its use as a zero delay buffer. By using the QFB output as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting in a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9608 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9608 are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consists of 4 components: static phase offset, output skew, feedback board trace delay, and I/O (phase) jitter:

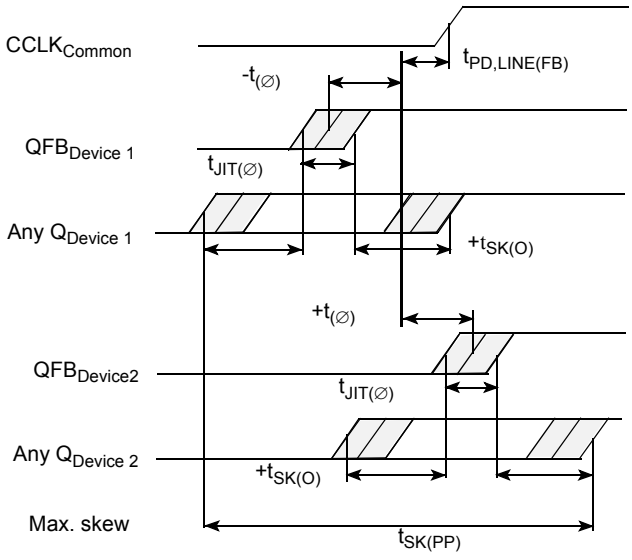


Figure 4. MPC9608 maximum device-to-device skew

Due to the statistical nature of I/O jitter, an RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -295 ps to 295 ps[1] relative to CCLK:

$t_{SK(PP)}$ = *[-100 ps...100 ps] + [-150 ps...150 ps] + [(15 ps · -3)...(15 ps · 3)] +* $t_{PD, LINE(FB)}$

$t_{SK(PP)}$ = *[-295 ps...295 ps]* + $t_{PD, LINE(FB)}$

Driving Transmission Lines

The MPC9608 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9608 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 5 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9608 clock driver is effectively doubled due to its capability to drive multiple lines.

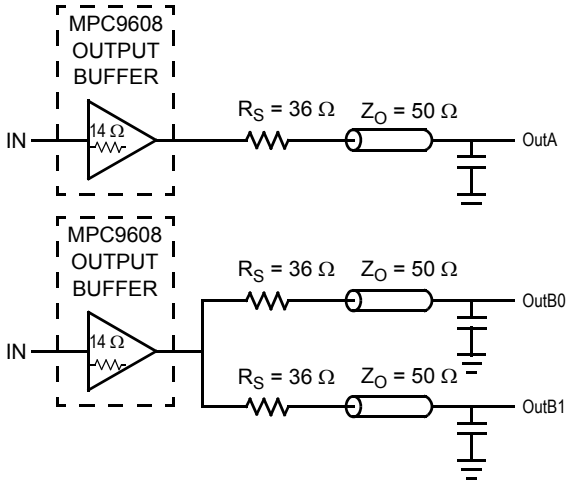


Figure 5. Single versus Dual Transmission Lines

The waveform plots in Figure 6. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9608 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. From the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9608. The output waveform in Figure 6. Single versus Dual Waveforms shows a step in the waveform. This step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$

$Z_0 = 50\ \Omega \parallel 50\ \Omega$

$R_S = 36\ \Omega \parallel 36\ \Omega$

$R_0 = 14\ \Omega$

$V_L = 3.0\ (25 \div (18 + 17 + 25))$

$= 1.31$ V

At the load end the voltage will double to 2.6 V due to the near unity reflection coefficient. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

1. Skew data are designed targets and pending device specifications.

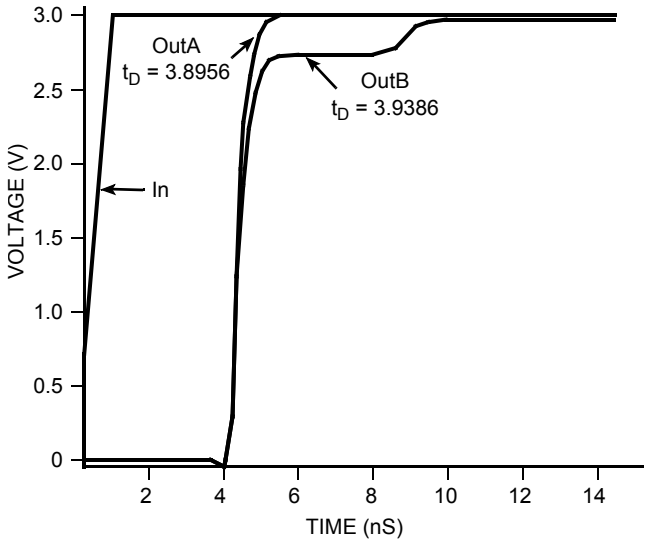


Figure 6. Single versus Dual Waveforms

Since this step is well above the threshold region, it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 7. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

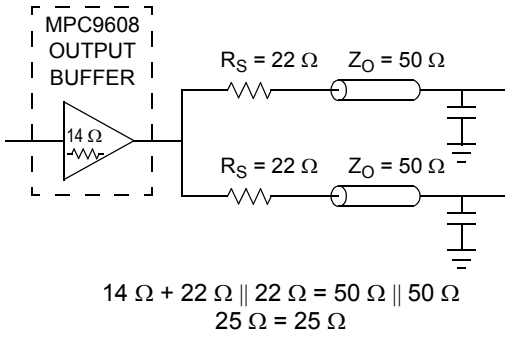


Figure 7. Optimized Dual Line Termination

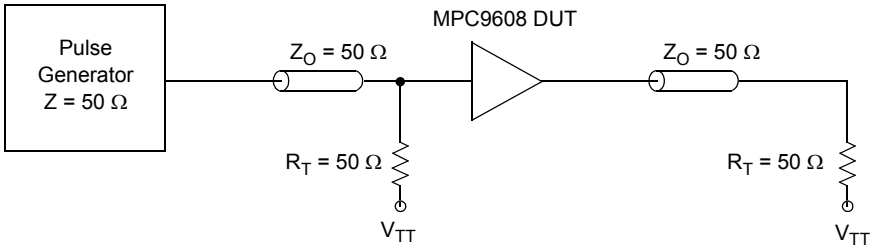
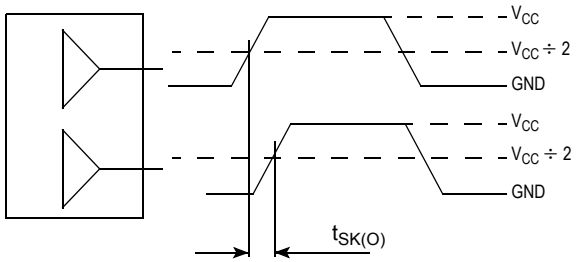


Figure 8. CCLK MPC9608 AC Test Reference for V_{CC} = 3.3 V



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device.

Figure 9. Output-to-Output Skew $t_{SK(O)}$

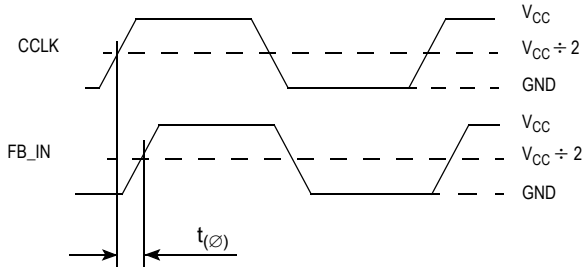
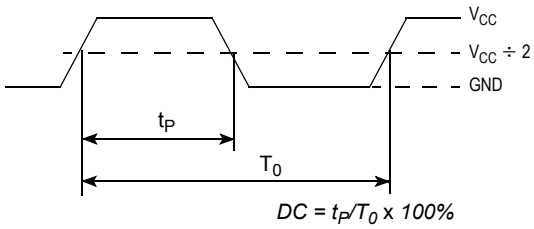
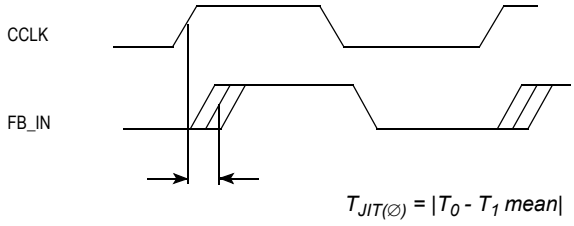


Figure 10. Propagation Delay (t_{PD}, static phase offset) Test Reference



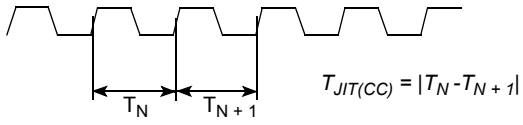
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage.

Figure 11. Output Duty Cycle (DC)



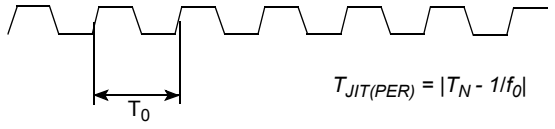
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles.

Figure 12. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs.

Figure 13. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles.

Figure 14. Period Jitter

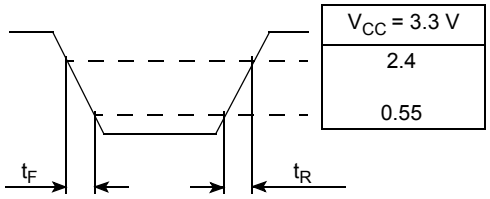


Figure 15. Output Transition Time Test Reference

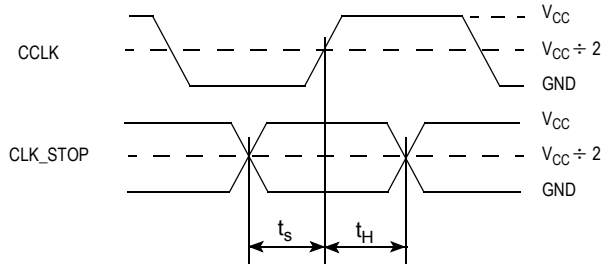


Figure 16. Setup and Hold Time (t_s, t_H) Test Reference

Low Voltage Zero Delay Buffer

MPC961C

LOW VOLTAGE
ZERO DELAY BUFFER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC961 is a 2.5 V or 3.3 V compatible, 1:18 PLL based zero delay buffer. With output frequencies of up to 200 MHz, output skews of 150 ps the device meets the needs of the most demanding clock tree applications.

Features

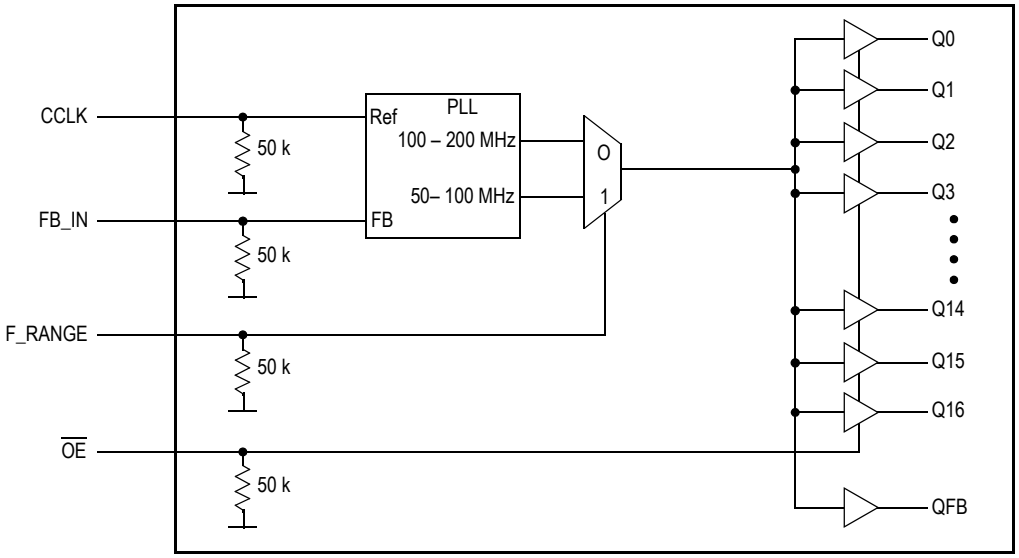
- Fully Integrated PLL
- Up to 200 MHz I/O Frequency
- LVCMOS Outputs
- Outputs Disable in High Impedance
- LVCMOS Reference Clock Options
- LQFP Packaging
- 32-lead Pb-free Package Available
- ±50 ps Cycle-Cycle Jitter
- 150 ps Output Skews

Functional Description

The MPC961 is offered with two different input configurations. The MPC961C offers an LVCMOS reference clock while the MPC961P offers an LVPECL reference clock.

When pulled high the $\overline{OE}$ pin will force all of the outputs (except QFB) into a high impedance state. Because the $\overline{OE}$ pin does not affect the QFB output, down stream clocks can be disabled without the internal PLL losing lock.

The MPC961 is fully 2.5 V or 3.3 V compatible and requires no external loop filter components. All control inputs accept LVCMOS compatible levels and the outputs provide low impedance LVCMOS outputs capable of driving terminated 50 Ω transmission lines. For series terminated lines the MPC961 can drive two lines per output giving the device an effective fanout of 1:36. The device is packaged in a 32 lead LQFP.



The MPC961C requires an external RC filter for the analog power supply pin V_{CCA}. Refer to APPLICATIONS INFORMATION for details.

Figure 1. MPC961C Logic Diagram

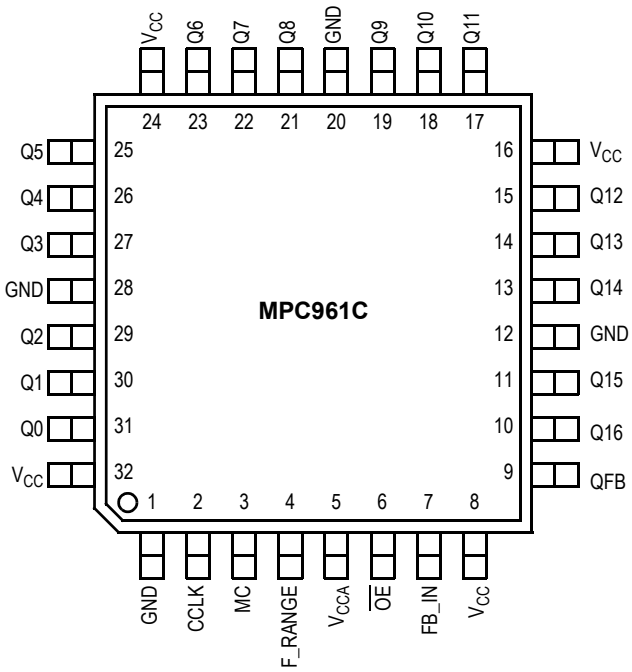


Figure 2. 32-Lead Pinout (Top View)

Table 1. Pin Configurations

Number	Name	Type	Description
CCLK	Input	LVCMOS	PLL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to a QFB output
F_RANGE	Input	LVCMOS	PLL frequency range select
$\overline{OE}$	Input	LVCMOS	Output enable/disable
Q0 – Q16	Output	LVCMOS	Clock outputs
QFB	Output	LVCMOS	PLL feedback signal output, connect to a FB_IN
GND	Supply	Ground	Negative power supply
V_{CCA}	Supply	V_{CC}	PLL positive power supply (analog power supply). The MPC961C requires an external RC filter for the analog power supply pin V_{CCA}. Refer to APPLICATIONS INFORMATION for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core
NC			Not connected

Table 2. Function Table

Control	Default	0	1
F_RANGE	0	PLL high frequency range. MPC961C input reference and output clock frequency range is 100 – 200 MHz	PLL low frequency range. MPC961C input reference and output clock frequency range is 50 – 100 MHz
OE	0	Outputs enabled	Outputs disabled (high-impedance state)

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–40	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input LOW Voltage	–0.3		0.8	V	LVCMOS
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20 mA[1]
V_{OL}	Output LOW Voltage			0.55	V	I_{OL} = 20 mA[1]
Z_{OUT}	Output Impedance		14	20	Ω	
I_{IN}	Input Current			±120	µA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		8.0	10	pF	Per Output
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current				mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage		V_{CC} ÷ 2		V	

1. The MPC961C is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up two 50 Ω series terminated transmission lines.

Table 5. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{MAX}	Maximum Output Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{REFDC}	Reference Input Duty Cycle		25		75	%	
t_r, t_f	TCLK Input Rise/Fall Time				3.0	ns	0.7 to 1.7 V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)	CCLK to FB_IN	–80		120	ps	PLL locked
$t_{sk(O)}$	Output-to-Output Skew[2]			90	150	ps	
DC_O	Output Duty Cycle	F_RANGE = 0 F_RANGE = 1	40 45	50 50	60 55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8 V
$t_{PLZ,HZ}$	Output Disable Time				10	ns	
$t_{PZL,LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	RMS (1σ)[3]			15	ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1σ)		7.0	10	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1σ)			15	ns	
t_{lock}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}
2. Refer to APPLICATIONS INFORMATION for part-to-part skew calculation.
3. Refer to APPLICATIONS INFORMATION for calculation for other confidence factors than 1 σ.

Table 6. DC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input LOW Voltage	–0.3		0.7	V	LVCMOS
V_{OH}	Output HIGH Voltage	1.8			V	I_{OH} = –15 mA[1]
V_{OL}	Output LOW Voltage			0.6	V	I_{OL} = 15 mA[1]
Z_{OUT}	Output Impedance		18	26	W	
I_{IN}	Input Current			±120	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		8.0	10	pF	Per Output
I_{CCA}	Maximum PLL Supply Current		2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current				mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	

1. The MPC961C is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up two 50 Ω series terminated transmission lines.

Table 7. AC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{MAX}	Maximum Output Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{REFDC}	Reference Input Duty Cycle		25		75	%	
t_r, t_f	TCLK Input Rise/Fall Time				3.0	ns	0.7 to 1.7 V
$t_{(\varnothing)}$	Propagation Delay (static phase offset)	CCLK to FB_IN	–80		120	ps	PLL locked
$t_{sk(O)}$	Output-to-Output Skew[2]			90	150	ps	
DC_O	Output Duty Cycle	F_RANGE = 0 F_RANGE = 1	40 45	50 50	60 55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8 V
$t_{PLZ,HZ}$	Output Disable Time				10	ns	
$t_{PZL,LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	RMS (1σ)[3]			15	ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1σ)		7.0	10	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1σ)			15	ns	
t_{lock}	Maximum PLL Lock Time				10	ms	
f_{REF}	Input Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{MAX}	Maximum Output Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. See APPLICATIONS INFORMATION for part-to-part skew calculation.
3. See APPLICATIONS INFORMATION for calculation for other confidence factors than 1 σ.

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC961C is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC961C provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC961C.

Figure 3 illustrates a typical power supply filter scheme. The MPC961C is most susceptible to noise with spectral content in the 10 kHz to 10 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC961C. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 2 mA (5 mA maximum), assuming that a minimum of 2.375 V (V_{CC} = 3.3 V or V_{CC} = 2.5 V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 3 must have a resistance of 270 Ω (V_{CC} = 3.3 V) or 5 to 15 Ω (V_{CC} = 2.5 V) to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

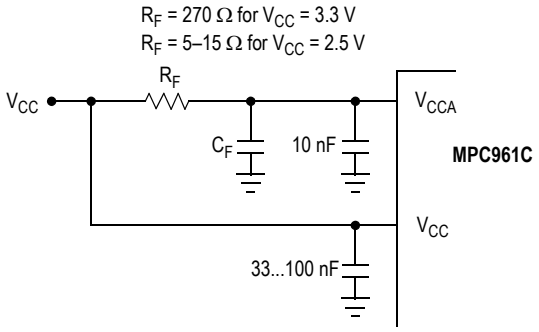


Figure 3. Power Supply Filter

Although the MPC961C has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC961C clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 15 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to the Application Note AN1091.

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC}/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC961C clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC961C clock driver is effectively doubled due to its capability to drive multiple lines.

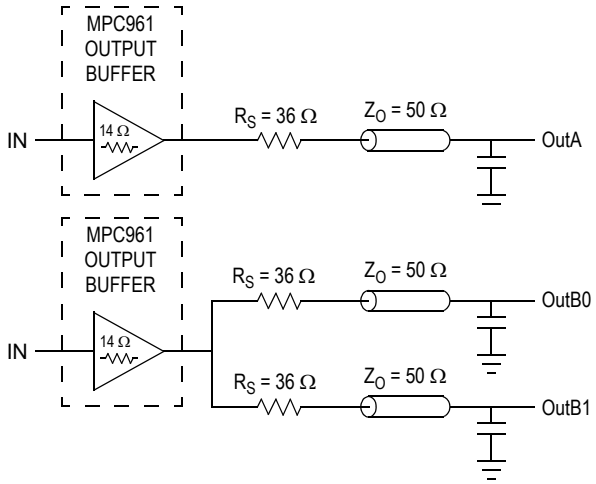


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line verses two lines. In both cases the drive capability of the MPC961C output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC961C. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch

seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$VL = VS (Z_O / (R_S + R_O + Z_O))$
$Z_O = 50\ \Omega \parallel 50\ \Omega$
$R_S = 36\ \Omega \parallel 36\ \Omega$
$R_O = 14\ \Omega$
$VL = 3.0\ (25 / (18 + 14 + 25) = 3.0\ (25 / 57)$
$= 1.31\ V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.62 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

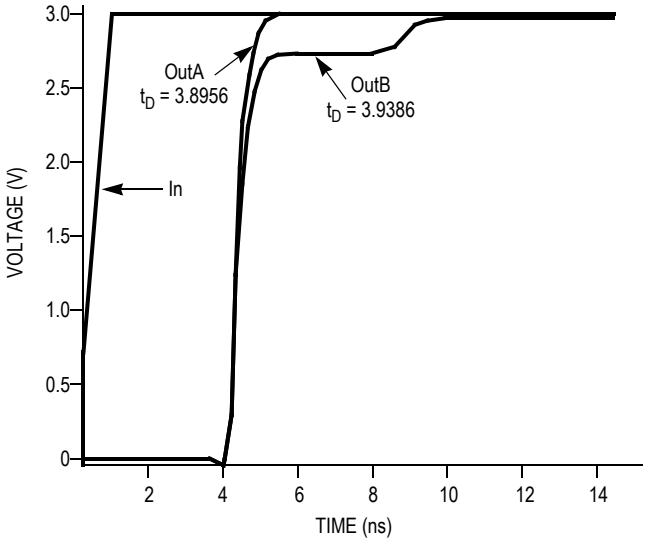
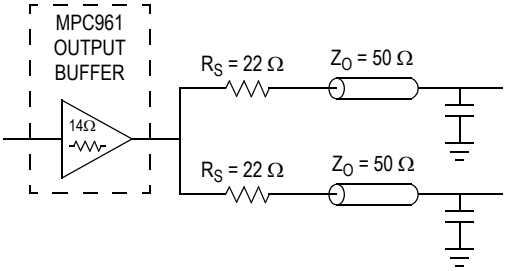


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



14 Ω + 22 Ω || 22 Ω = 50 Ω || 50 Ω
25 Ω = 25 Ω

Figure 6. Optimized Dual Line Termination

SPICE level and IBIS output buffer models are available for engineers who want to simulate their specific interconnect schemes.

Using the MPC961C in Zero-Delay Applications

Nested clock trees are typical applications for the MPC961C. Designs using the MPC961C as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC961C clock driver allows for its use as a zero delay buffer. By using the QFB output as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC961C zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC961C are connected together, the maximum overall timing uncertainty from the common CCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

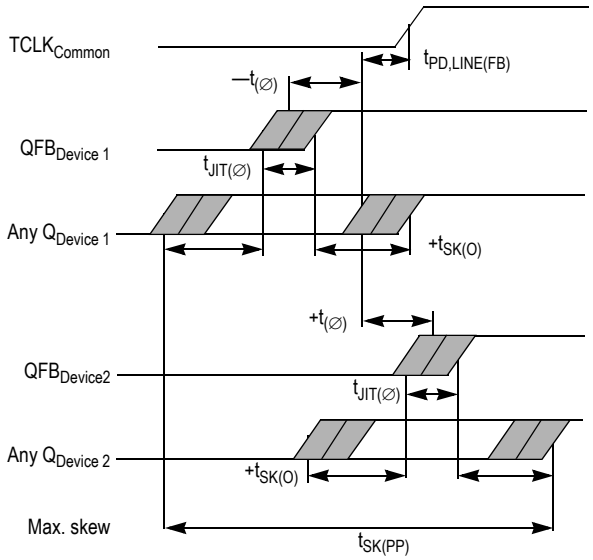


Figure 7. MPC961C Max. Device-to-Device Skew

Due to the statistical nature of I/O jitter a rms value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.Confidence Factor CF.

Table 8. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of -275 ps to 315 ps relative to CCLK:

$t_{SK(PP)}$ = *[-80ps...120ps] + [-150ps...150ps] + [(15ps @ -3)...(15ps @ 3)]* + $t_{PD, LINE(FB)}$

$t_{SK(PP)}$ = *[-275ps...315ps]* + $t_{PD, LINE(FB)}$

Due to the frequency dependence of the I/O jitter, Figure 8 can be used for a more precise timing performance analysis.

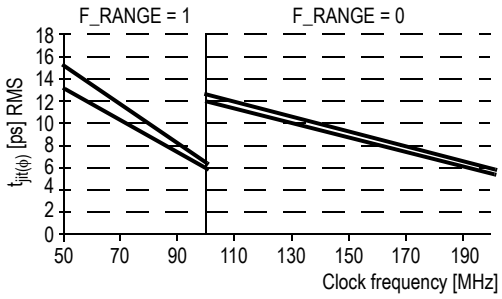


Figure 8. Max. I/O Jitter versus Frequency

Power Consumption of the MPC961C and Thermal Management

The MPC961C AC specification is guaranteed for the entire operating frequency range up to 200 MHz. The MPC961C power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC961C die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability refer to the Application Note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

Table 9. Die Junction Temperature and MTBF

Junction Temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC961C needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC961C is represented in equation 1.

Where I_{CCQ} is the static current consumption of the MPC961C, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 27 in case of the MPC961C). The MPC961C supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL}, I_{OL}, V_{OH}, and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \qquad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \qquad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \qquad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{j,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \qquad \text{Equation 4}$$

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 9.Die Junction Temperature and MTBF, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC961C in a series terminated transmission line system.

Table 10. Thermal Package Impedance of the 32ld LQFP

Convection, LFPM	R_{thja} (1P2S board), K/W
Still air	80
100 lfpm	70
200 lfpm	61
300 lfpm	57
400 lfpm	56
500 lfpm	55

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 9.Die Junction Temperature and MTBF. R_{thja} can be derived from Table 10.Thermal Package Impedance of the 32ld LQFP. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

If the calculated maximum frequency is below 200 MHz, it becomes the upper clock speed limit for the given application conditions. The following two derating charts describe the safe frequency operation range for the MPC961C. The charts were calculated for a maximum tolerable die junction temperature of 110°C, corresponding to an estimated MTBF of 9.1 years, a supply voltage of 3.3 V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made. There are no operating frequency limitations if a 2.5 V power supply or the system specifications allow for a MTBF of 4 years (corresponding to a max. junction temperature of 120°C.

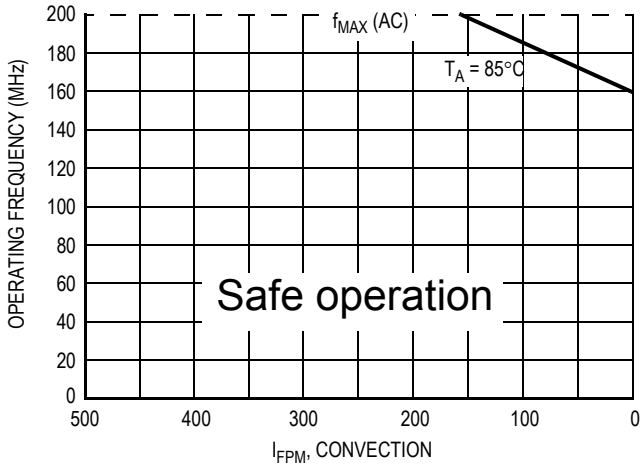


Figure 9. Maximum MPC961C Frequency, V_{CC} = 3.3 V, MTBF 9.1 Years, Driving Series Terminated Transmission Lines

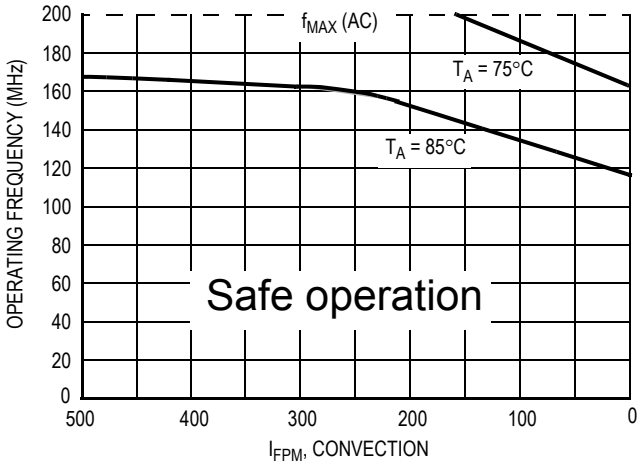


Figure 10. Maximum MPC961C Frequency, V_{CC} = 3.3 V, MTBF 9.1 Years, 4 pF Load per Line

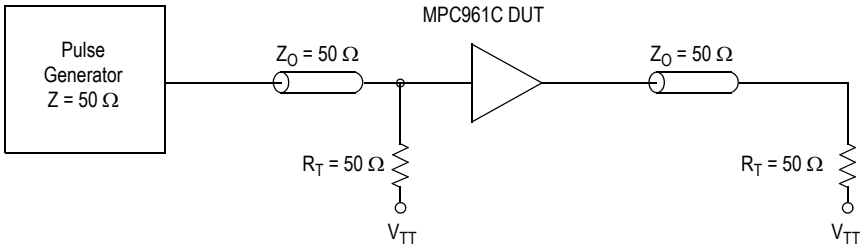
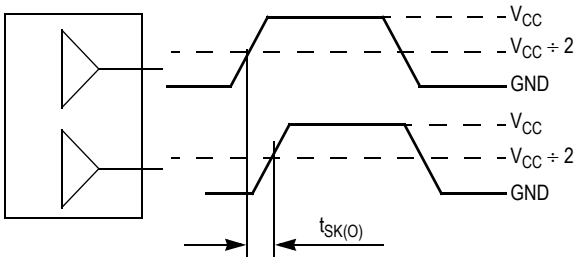


Figure 11. TCLK MPC961C AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 12. Output-to-Output Skew $t_{SK(O)}$

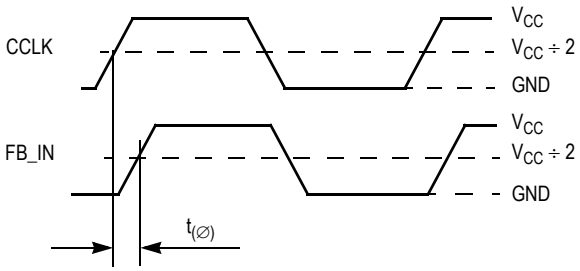
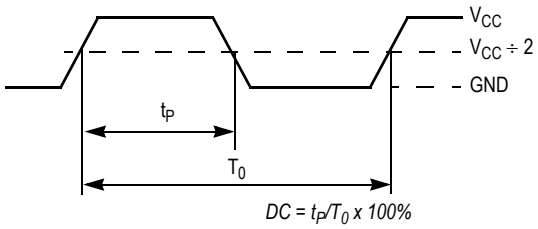
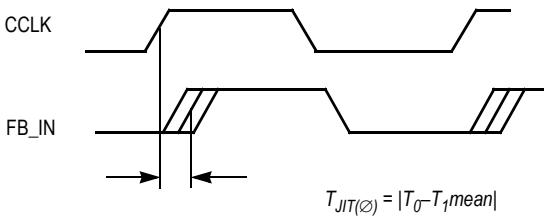


Figure 13. Propagation Delay (t_{PD}, static phase offset) Test Reference



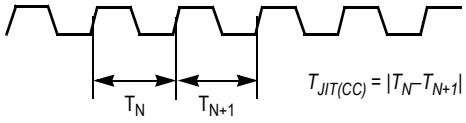
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 14. Output Duty Cycle (DC)



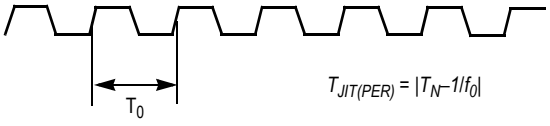
The deviation in t_0 for a controlled edge with respect to a t_0 mean in a random sample of cycles

Figure 15. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 16. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 17. Period Jitter

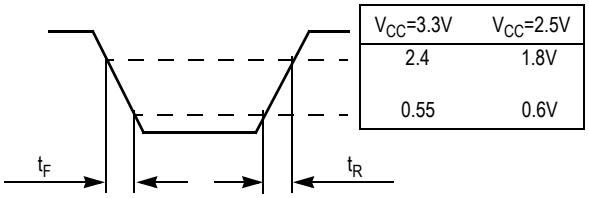


Figure 18. Output Transition Time Test Reference

Low Voltage Zero Delay Buffer

MPC961P

LOW VOLTAGE
ZERO DELAY BUFFER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC961 is a 2.5 V or 3.3 V compatible, 1:18 PLL based zero delay buffer. With output frequencies of up to 200 MHz, output skews of 150 ps the device meets the needs of the most demanding clock tree applications.

Features

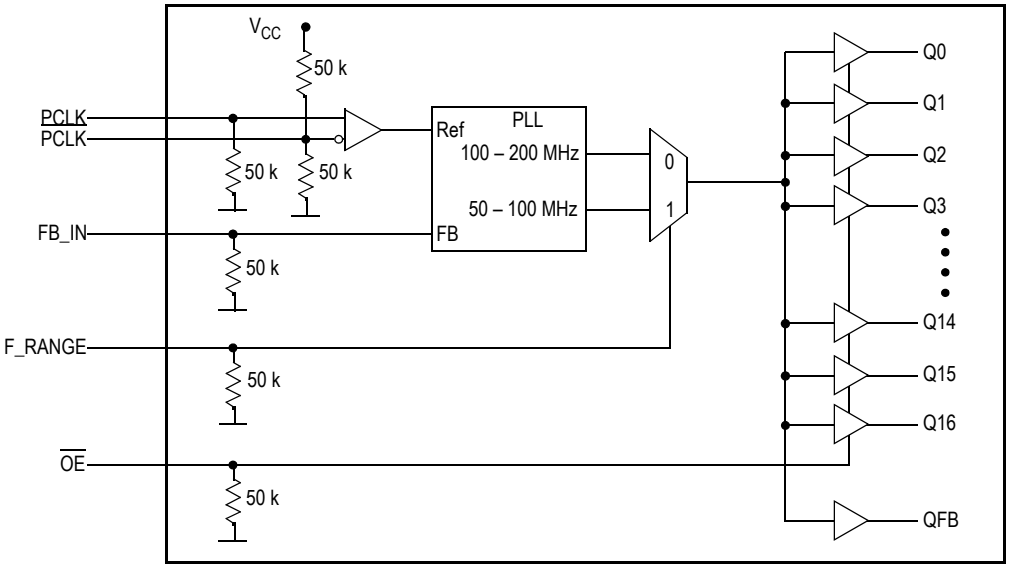
- Fully Integrated PLL
- Up to 200 MHz I/O Frequency
- LVCMOS Outputs
- Outputs Disable in High Impedance
- LVPECL Reference Clock Options
- LQFP Packaging
- 32-lead Pb-free Package Available
- ±50 ps Cycle-Cycle Jitter
- 150 ps Output Skews

Functional Description

The MPC961 is offered with two different input configurations. The MPC961P offers an LVCMOS reference clock while the MPC961P offers an LVPECL reference clock.

When pulled high the $\overline{OE}$ pin will force all of the outputs (except QFB) into a high impedance state. Because the $\overline{OE}$ pin does not affect the QFB output, down stream clocks can be disabled without the internal PLL losing lock.

The MPC961 is fully 2.5 V or 3.3 V compatible and requires no external loop filter components. All control inputs accept LVCMOS compatible levels and the outputs provide low impedance LVCMOS outputs capable of driving terminated 50 Ω transmission lines. For series terminated lines the MPC961 can drive two lines per output giving the device an effective fanout of 1:36. The device is packaged in a 32 lead LQFP package to provide the optimum combination of board density and performance.



The MPC961P requires an external RC filter for the analog power supply pin V_{CCA}. Refer to APPLICATIONS INFORMATION for details.

Figure 1. MPC961P Logic Diagram

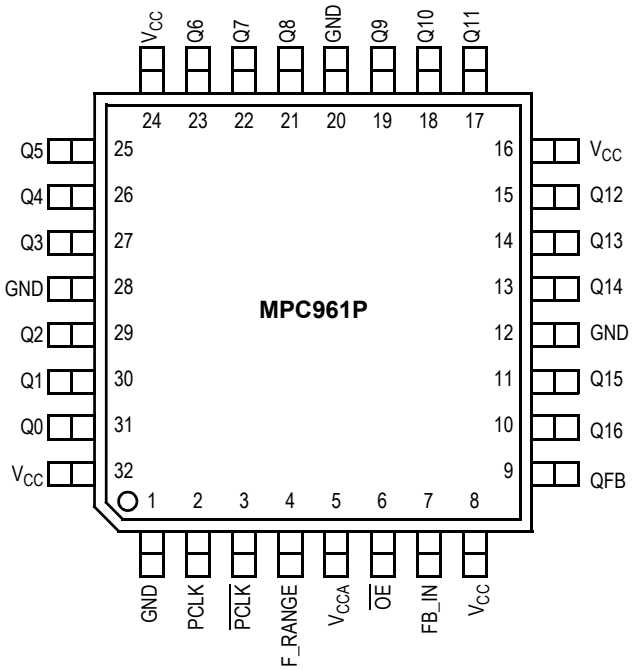


Figure 2. 32-Lead Pinout (Top View)

Table 1. Pin Configurations

Number	Name	Type	Description
PCLK, $\overline{\text{PCLK}}$	Input	LVCMOS	PLL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to a QFB output
F_RANGE	Input	LVCMOS	PLL frequency range select
$\overline{\text{OE}}$	Input	LVCMOS	Output enable/disable
Q0 – Q16	Output	LVCMOS	Clock outputs
QFB	Output	LVCMOS	PLL feedback signal output, connect to a FB_IN
GND	Supply	Ground	Negative power supply
V_{CCA}	Supply	V_{CC}	PLL positive power supply (analog power supply). The MPC961P requires an external RC filter for the analog power supply pin V_{CCA}. Please see applications section for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core

Table 2. Function Table

Control	Default	0	1
F_RANGE	0	PLL high frequency range. MPC961P input reference and output clock frequency range is 100 – 200 MHz	PLL low frequency range. MPC961P input reference and output clock frequency range is 50 – 100 MHz
OE	0	Outputs enabled	Outputs disabled (high-impedance state)

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–40	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input LOW Voltage		–0.3		0.8	V	LVCMOS
V_{PP}	Peak-to-peak input voltage[1]	PECL_CLK, $\overline{\text{PECL\_CLK}}$	500		1000	mV	LVPECL
V_{CMR}	Common Mode Range[2]	PECL_CLK, $\overline{\text{PECL\_CLK}}$	1.2		V_{CC} – 0.8	V	LVPECL
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH} = –20 mA[2]
V_{OL}	Output LOW Voltage				0.55	V	I_{OL} = 20 mA[2]
Z_{OUT}	Output Impedance			14	20	Ω	
I_{IN}	Input Current				±120	µA	
C_{IN}	Input Capacitance			4.0		pF	
C_{PD}	Power Dissipation Capacitance			8.0	10	pF	Per Output
I_{CCA}	Maximum PLL Supply Current			2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current					mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage			V_{CC} ÷ 2		V	

1. Exceeding the specified V_{CMR}/V_{PP} window results in a t_{PD} changes of approximately 250 ps.
2. The MPC961P is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up two 50 Ω series terminated transmission lines.

Table 5. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{MAX}	Maximum Output Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{REFDC}	Reference Input Duty Cycle		25		75	%	
$t_{(\varnothing)}$	Propagation Delay[2] (static phase offset)	PECL_CLK to FB_IN	–80		120	ps	PLL locked
$t_{sk(O)}$	Output-to-Output Skew[3]			90	150	ps	
DC_O	Output Duty Cycle	F_RANGE = 0 F_RANGE = 1	40 45	50 50	60 55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8V
$t_{PLZ,HZ}$	Output Disable Time				10	ns	
$t_{PZL,LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	RMS (1σ)[4]			15	ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1σ)		7.0	10	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter RMS (1σ)	F_RANGE = 0 F_RANGE = 1			0.0015 · T 0.0010 · T	ns	T = Clock Signal Period
t_{lock}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. t_{PD} applies for V_{CMR} = V_{CC} –1.3 V and V_{PP} = 800 mV.
3. Refer to APPLICATIONS INFORMATION for part-to-part skew calculation.
4. Refer to APPLICATIONS INFORMATION for calculation for other confidence factors than 1σ.

Table 6. DC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40° to 85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage		1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input LOW Voltage		–0.3		0.7	V	LVCMOS
V_{PP}	Peak-to-peak input voltage[1]	PECL_CLK, $\overline{\text{PECL\_CLK}}$	500		1000	mV	LVPECL
V_{CMR}	Common Mode Range[a]	PECL_CLK, $\overline{\text{PECL\_CLK}}$	1.2		V_{CC} – 0.7	V	LVPECL
V_{OH}	Output HIGH Voltage		1.8			V	I_{OH} = –15 mA[2]
V_{OL}	Output LOW Voltage				0.6	V	I_{OL} = 15 mA[b]
Z_{OUT}	Output Impedance			18	26	Ω	
I_{IN}	Input Current				±120	μA	
C_{IN}	Input Capacitance			4.0		pF	
C_{PD}	Power Dissipation Capacitance			8.0	10	pF	Per Output
I_{CCA}	Maximum PLL Supply Current			2.0	5.0	mA	V_{CCA} Pin
I_{CC}	Maximum Quiescent Supply Current					mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage			$V_{CC} \div 2$		V	

1. Exceeding the specified V_{CMR}/V_{PP} window results in a t_{PD} changes < 250 ps.
2. The MPC961P is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up two 50 Ω series terminated transmission lines.

Table 7. AC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40° to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{MAX}	Maximum Output Frequency	F_RANGE = 0 F_RANGE = 1	100 50		200 100	MHz	
f_{REFDC}	Reference Input Duty Cycle		25		75	%	
$t_{(\varnothing)}$	Propagation Delay[2] (static phase offset)	CCLK to FB_IN	–50		175	ps	PLL locked
$t_{sk(O)}$	Output-to-Output Skew[3]			90	150	ps	
DC_O	Output Duty Cycle	F_RANGE = 0 F_RANGE = 1	40 45	50 50	60 55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8 V
$t_{PLZ,HZ}$	Output Disable Time				10	ns	
$t_{PZL,LZ}$	Output Enable Time				10	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	RMS (1σ)[4]			15	ps	
$t_{JIT(PER)}$	Period Jitter	RMS (1σ)		7.0	10	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter	RMS (1σ) F_RANGE = 0 F_RANGE = 1			0.0015 · T 0.0010 · T	ns	T = Clock Signal Period
t_{lock}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. t_{PD} applies for $V_{CMR} = V_{CC}$ –1.3 V and V_{PP} = 800 mV.
3. Refer to APPLICATIONS INFORMATION for part-to-part skew calculation.
4. Refer to APPLICATIONS INFORMATION for calculation for other confidence factors than 1σ.

APPLICATIONS INFORMATION

Power Supply Filtering

The MPC961P is a mixed analog/digital product and as such it exhibits some sensitivities that would not necessarily be seen on a fully digital product. Analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. The MPC961P provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a controlled environment such as an evaluation board this level of isolation is sufficient. However, in a digital system environment where it is more difficult to minimize noise on the power supplies, a second level of isolation may be required. The simplest form of isolation is a power supply filter on the V_{CCA} pin for the MPC961P.

Figure 3 illustrates a typical power supply filter scheme. The MPC961P is most susceptible to noise with spectral content in the 10 kHz to 5 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop that will be seen between the V_{CC} supply and the V_{CCA} pin of the MPC961P. From the data sheet the I_{CCA} current (the current sourced through the V_{CCA} pin) is typically 2 mA (5 mA maximum), assuming that a minimum of 2.375 V (V_{CC} = 3.3 V or V_{CC} = 2.5 V) must be maintained on the V_{CCA} pin. The resistor R_F shown in Figure 3 must have a resistance of 270 Ω (V_{CC} = 3.3 V) or 5 to 15 Ω (V_{CC} = 2.5 V) to meet the voltage drop criteria. The RC filter pictured will provide a broadband filter with approximately 100:1 attenuation for noise whose spectral content is above 20 kHz. As the noise frequency crosses the series resonant point of an individual capacitor it's overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL.

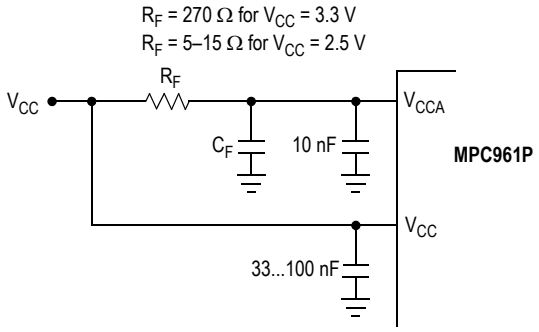


Figure 3. Power Supply Filter

Although the MPC961P has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Driving Transmission Lines

The MPC961P clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 15 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091.

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC}/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC961P clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC961P clock driver is effectively doubled due to its capability to drive multiple lines.

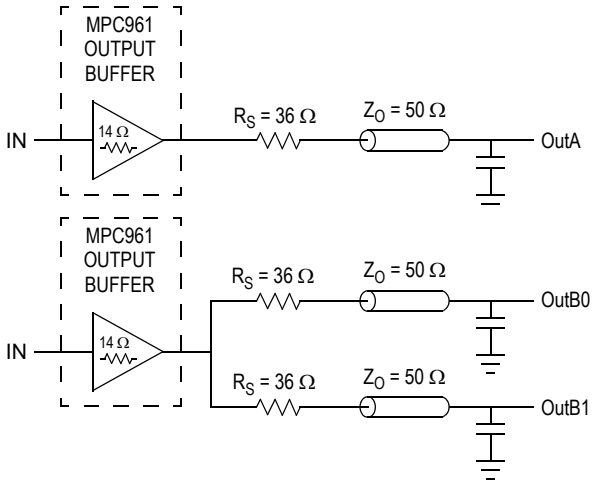


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC961P output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC961P. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen

looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$VL = VS (Z_O / (R_S + R_O + Z_O))$

$Z_O = 50\ \Omega \parallel 50\ \Omega$

$R_S = 36\ \Omega \parallel 36\ \Omega$

$R_O = 14\ \Omega$

$VL = 3.0\ (25 / (18 + 14 + 25) = 3.0\ (25 / 57)$

$= 1.31\ V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.62 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0ns).

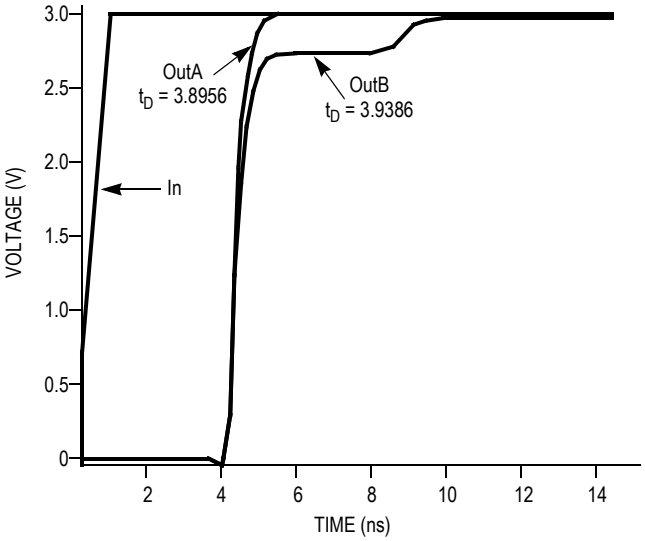
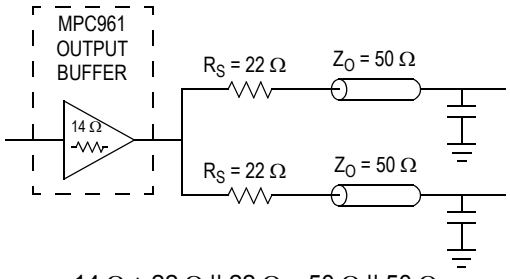


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\ \Omega + 22\ \Omega \parallel 22\ \Omega = 50\ \Omega \parallel 50\ \Omega$

$25\ \Omega = 25\ \Omega$

Figure 6. Optimized Dual Line Termination

SPICE level and IBIS output buffer models are available for engineers who want to simulate their specific interconnect schemes.

Using the MPC961P in Zero-Delay Applications

Nested clock trees are typical applications for the MPC961P. Designs using the MPC961P as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC961P clock driver allows for its use as a zero delay buffer. By using the QFB output as a feedback to the PLL the propagation delay through the device is virtually eliminated. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device. The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC961P zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC961P are connected together, the maximum overall timing uncertainty from the common PCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

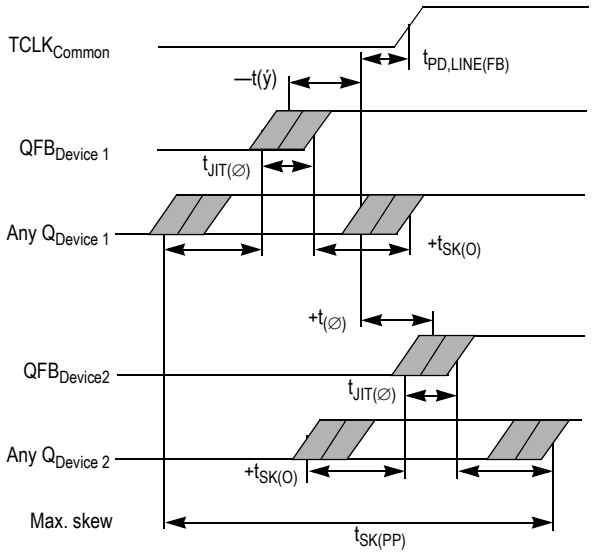


Figure 7. MPC961P Max. Device-to-Device Skew

Due statistical nature of I/O jitter a rms value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.Confidence Factor CF.

Table 8. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –236 ps to 361 ps relative to PCLK (f=125 MHz, V_{CC}=2.5 V):

$t_{SK(PP)}$ = *[-50 ps...175ps] + [-150 ps...150 ps] + [(12ps @ -3)...(12ps @ 3)] +* $t_{PD, LINE(FB)}$

$t_{SK(PP)}$ = *[-236ps...361ps]* + $t_{PD, LINE(FB)}$

Due to the frequency dependence of the I/O jitter, Figure 8 “Max. I/O Jitter versus frequency” can be used for a more precise timing performance analysis.

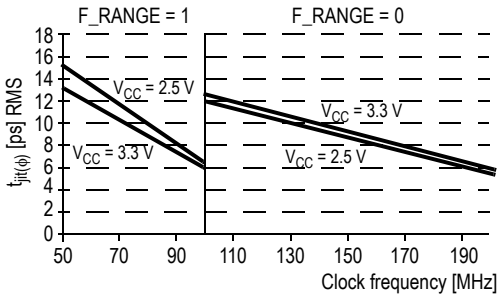


Figure 8. Max. I/O Jitter versus Frequency

Power Consumption of the MPC961P and Thermal Management

The MPC961P AC specification is guaranteed for the entire operating frequency range up to 200 MHz. The MPC961P power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC961P die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability refer to the Application Note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

Table 9. Die Junction Temperature and MTBF

Junction temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC961P needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC961P is represented in equation 1.

Where I_{CCQ} is the static current consumption of the MPC961P, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 27 in case of the MPC961P). The MPC961P supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL}, I_{OL}, V_{OH}, and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \qquad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \qquad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \qquad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{j,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \qquad \text{Equation 4}$$

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 9.Die Junction Temperature and MTBF, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC961P in a series terminated transmission line system.

Table 10. Thermal Package Impedance of the 32ld LQFP

Convection, LFPM	R_{thja} (1P2S board), K/W
Still air	80
100 lfpm	70
200 lfpm	61
300 lfpm	57
400 lfpm	56
500 lfpm	55

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 9.Die Junction Temperature and MTBF. R_{thja} can be derived from Table 10.Thermal Package Impedance of the 32ld LQFP. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

If the calculated maximum frequency is below 200 MHz, it becomes the upper clock speed limit for the given application conditions. The following two derating charts describe the safe frequency operation range for the MPC961P. The charts were calculated for a maximum tolerable die junction temperature of 110°C, corresponding to an estimated MTBF of 9.1 years, a supply voltage of 3.3 V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made. There are no operating frequency limitations if a 2.5 V power supply or the system specifications allow for a MTBF of 4 years (corresponding to a max. junction temperature of 120°C.

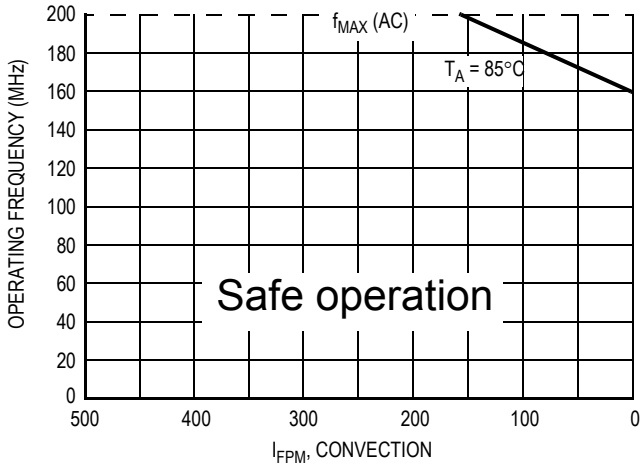


Figure 9. Maximum MPC961P Frequency, V_{CC} = 3.3 V, MTBF 9.1 Years, Driving Series Terminated Transmission Lines

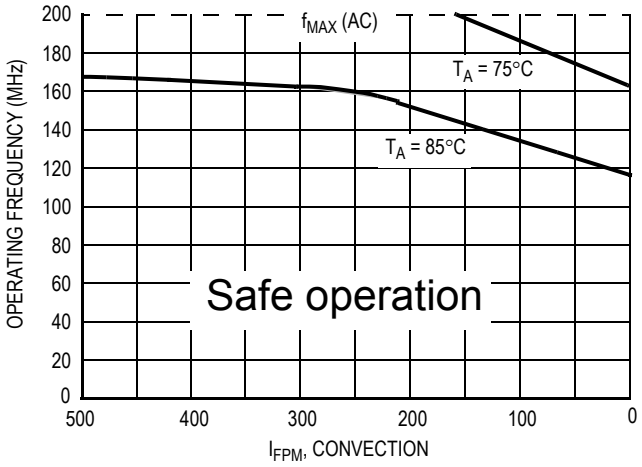


Figure 10. Maximum MPC961P Frequency, V_{CC} = 3.3 V, MTBF 9.1 Years, 4 pF Load per Line

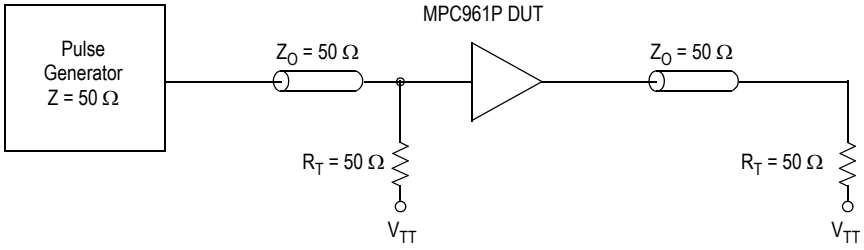


Figure 11. TCLK MPC961P AC Test Reference for V_{CC} = 3.3 V and V_{CC} = 2.5 V

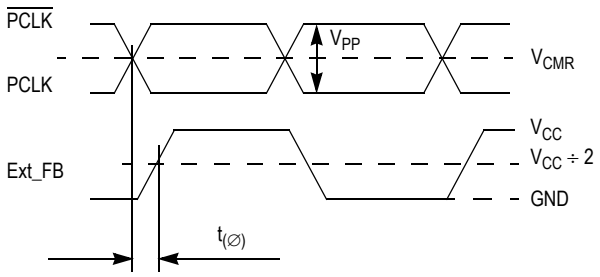


Figure 12. Propagation Delay ($t_{\varnothing}$, static phase offset) Test Reference

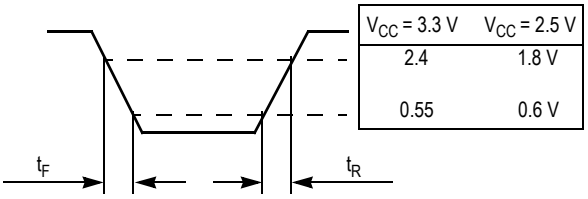
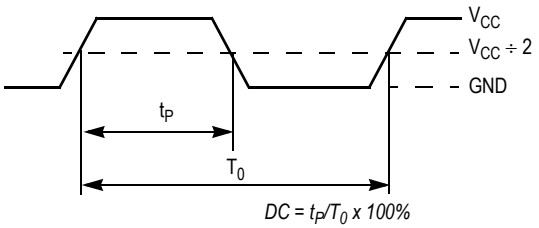
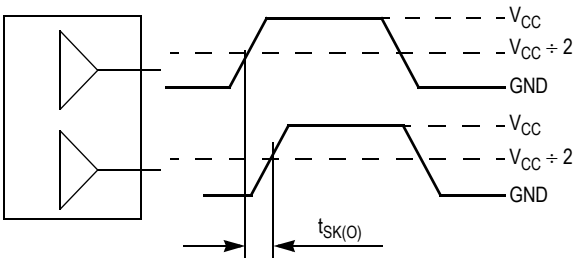


Figure 13. Output Transition Time Test Reference



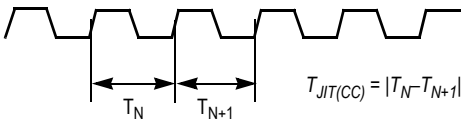
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 14. Output Duty Cycle (DC)



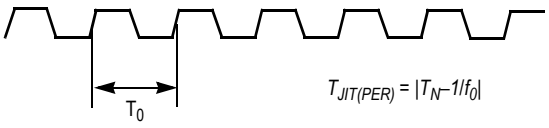
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 15. Output-to-Output Skew $t_{SK(O)}$



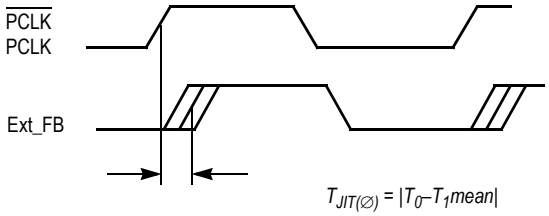
The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 16. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 17. Period Jitter



The deviation in t_0 for a controlled edge with respect to a T_0 mean in a random sample of cycles

Figure 18. I/O Jitter

3.3 V Zero Delay Buffer

MPC962304

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-06

The MPC962304 is a 3.3 V Zero Delay Buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom and other high-performance applications. The MPC962304 uses an internal PLL and an external feedback path to lock its low-skew clock output phase to the reference clock phase, providing virtually zero propagation delay. The input-to-output skew is guaranteed to be less than 250 ps and output-to-output skew is guaranteed to be less than 200 ps.

Features

- 1:4 outputs LVCMOS zero-delay buffer
- Zero input-output propagation delay, adjustable by the capacitive load on FBK input
- Multiple Configurations, See **Table 1. Available MPC962304 Configurations**
- Multiple low-skew outputs
  - 200 ps max output-output skew
  - 500 ps max device-device skew
- Supports a clock I/O frequency range of 10 MHz to 133 MHz
- Low jitter, 200 ps max cycle-cycle
- 8-pin SOIC package
- Single 3.3 V supply
- Ambient temperature range: –40°C to +85°C
- Compatible with the CY2304

Functional Description

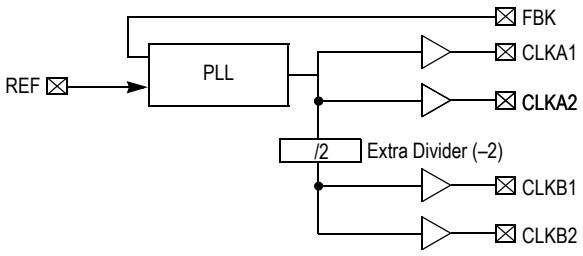
The MPC962304 has two banks of two outputs each. The MPC962304 PLL enters a power down state when there are no rising edges on the REF input. During this state, all of the outputs are in tristate. When the PLL is turned off, there is less than 25 μA of current draw.

Multiple MPC962304 devices can accept and distribute the same input clock throughout the system. In this situation, the difference between the output skews of two devices will be less than 500 ps.

The MPC962304 is offered in two configurations. In the -1 version, the reference frequency is reproduced by the PLL and provided to the outputs.

The MPC962304-2 provides 1/2X and 2X the reference frequency at the output banks.

Block Diagram



Pin Configuration

8-pin SOIC
Top View

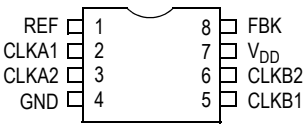


Table 1. Available MPC962304 Configurations

Device	Feedback From	Bank A Frequency	Bank B Frequency
MPC962304-1	Bank A or Bank B	Reference	Reference
MPC962304-2	Bank A	Reference	Reference/2
MPC962304-2	Bank B	2 X Reference	Reference

Table 2. Pin Description

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5 V tolerant input
2	CLKA1[2]	Clock output, Bank A
3	CLKA2[2]	Clock output, Bank A
4	GND	Ground
5	CLKB1[2]	Clock output, Bank B
6	CLKB2[2]	Clock output, Bank B
7	V_{DD}	3.3 V supply
8	FBK	PLL feedback input

1. Weak pull-down.
2. Weak pull-down on all outputs.

Table 3. Maximum Ratings

Characteristics	Value	Unit
Supply Voltage to Ground Potential	–0.5 to +3.9	V
DC Input Voltage (Except REF)	–0.5 to V_{DD}+0.5	V
DC Input Voltage REF	–0.5 to 5.5	V
Storage Temperature	–65 to +150	°C
Junction	150	°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2000	V

Table 4. Operating Conditions for MPC962304-X Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, below 100 MHz		30	pF
	Load Capacitance, from 100 MHz to 133 MHz		15	pF
C_{IN}	Input Capacitance[1]		7	pF

1. Applies to both REF clock and FBK.

Table 5. Electrical Characteristics for MPC962304-X Industrial Temperature Devices[1]

Parameter	Description	Test Conditions	Min	Max.	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0 V		50.0	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	μA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 8 mA (-1, -2)		0.4	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = -8 mA (-1, -2)	2.4		V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		25.0	μA
I_{DD}	Supply Current	Unloaded outputs, 100 MHz, Select inputs at V_{DD} or GND		45.0	mA
		Unloaded outputs, 66-MHz REF (-1, -2)		35.0	mA
		Unloaded outputs, 35-MHz REF (-1, -2)		20.0	mA

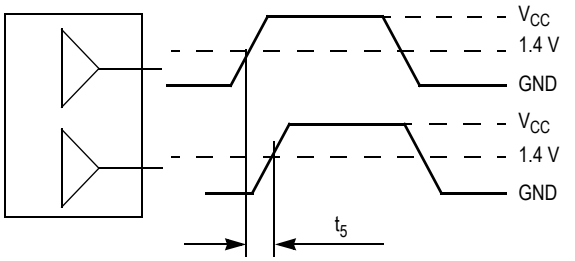
1. All parameters are specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 6. Switching Characteristics for MPC962304-X Industrial Temperature Devices[1]

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30-pF load, all devices	10		100	MHz
	Output Frequency	15-pF load, all devices	10		133.3	MHz
	Duty Cycle[2] = $t_2 \div t_1$ (-1, -2)	Measured at 1.4 V, FOUT = 66.66 MHz 30-pF load	40.0		60.0	%
	Duty Cycle[2] = $t_2 \div t_1$ (-1, -2)	Measured at 1.4 V, FOUT < 50.0 MHz 15-pF load	45.0		55.0	%
t_3	Rise Time[2] (-1, -2)	Measured between 0.8 V and 2.0 V, 30-pF load			2.50	ns
	Rise Time[2] (-1, -2)	Measured between 0.8 V and 2.0 V, 15-pF load			1.50	ns
t_4	Fall Time[2] (-1, -2)	Measured between 0.8 V and 2.0 V, 30-pF load			2.50	ns
	Fall Time[2] (-1, -2)	Measured between 0.8 V and 2.0 V, 15-pF load			1.50	ns
t_5	Output to Output Skew on same Bank (-1, -2)[2]	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (-1)	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (-2)	All outputs equally loaded			400	ps
t_6	Delay, REF Rising Edge to FBK Rising Edge[2]	Measured at $V_{DD}/2$		0	±250	ps
t_7	Device to Device Skew[2]	Measured at $V_{DD}/2$ on the FBK pins of devices		0	500	ps
t_J	Cycle to Cycle Jitter[2] (-1)	Measured at 66.67 MHz, loaded outputs, 15-pF load			180	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load			200	ps
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	ps
t_J	Cycle to Cycle Jitter[2] (-2)	Measured at 66.67 MHz, loaded outputs 30-pF load			400	ps
		Measured at 66.67 MHz, loaded outputs 15-pF load			380	ps
t_{LOCK}	PLL Lock Time[2]	Stable power supply, valid clocks presented on REF and FBK pins			1.0	ms

1. All parameters are specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

APPLICATIONS INFORMATION



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 1. Output-to-Output Skew $t_{SK(O)}$

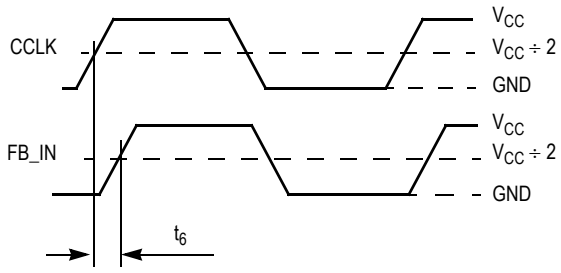
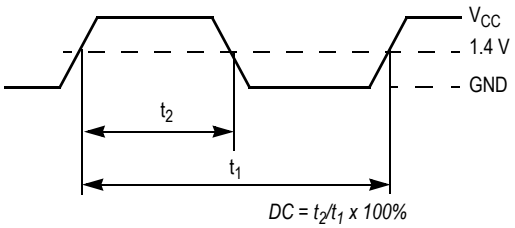


Figure 2. Static Phase Offset Test Reference



The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 3. Output Duty Cycle (DC)

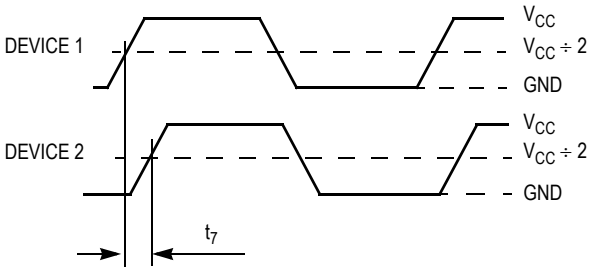
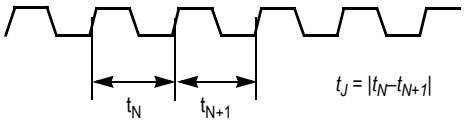


Figure 4. Device-to-Device Skew



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 5. Cycle-to-Cycle Jitter

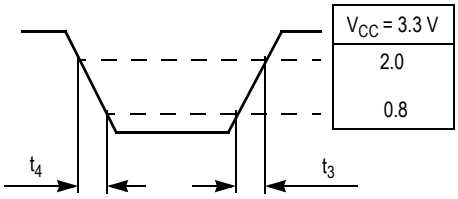
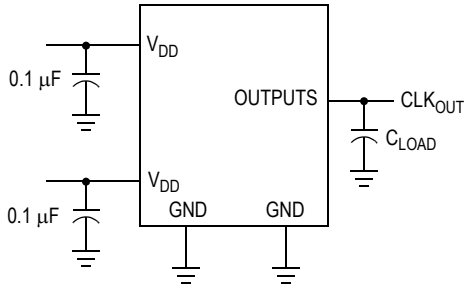


Figure 6. Output Transition Time Test Reference

Test Circuit #1



Test Circuit for all parameters

Ordering Information (Available)

Ordering Code	Package Name	Package Type
MPC962304D-1	D8	8-pin 150-mil SOIC
MPC962304D-1R2	D8	8-pin 150-mil SOIC — Tape and Reel
MPC962304D-2	D8	8-pin 150-mil SOIC
MPC962304D-2R2	D8	8-pin 150-mil SOIC — Tape and Reel

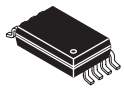
Order number: MPC962305
Rev 5, 08/2004

MPC962305
MPC962309

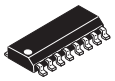
Low-Cost 3.3 V Zero Delay Buffer

The MPC962309 is a zero delay buffer designed to distribute high-speed clocks. Available in a 16-pin SOIC or TSSOP package, the device accepts one reference input and drives nine low-skew clocks. The MPC962305 is the 8-pin version of the MPC962309 which drives five outputs with one reference input. The -1H versions of these devices have higher drive than the -1 devices and can operate up to 100/-133 MHz frequencies. These parts have on-chip PLLs which lock to an input clock presented on the REF pin. The PLL feedback is on-chip and is obtained from the CLOCKOUT pad.

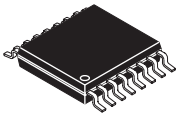
D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-06



DT SUFFIX
8-LEAD TSSOP PACKAGE
CASE 948J-01



D SUFFIX
16-LEAD SOIC PACKAGE
CASE 751B-05



DT SUFFIX
16-LEAD TSSOP PACKAGE
CASE 948F-01

Features

- 1:5 LVCMOS zero-delay buffer (MPC962305)
- 1:9 LVCMOS zero-delay buffer (MPC962309)
- Zero input-output propagation delay
- Multiple low-skew outputs
- 250 ps max output-output skew
- 700 ps max device-device skew
- Supports a clock I/O frequency range of 10 MHz to 133 MHz, compatible with CPU and PCI bus frequencies
- Low jitter, 200 ps max cycle-cycle, and compatible with Pentium® based systems
- Test Mode to bypass PLL (MPC962309 only. See Table 3.Select Input Decoding for MPC962309)
- 8-pin SOIC or 8-pin TSSOP package (MPC962305);16-pin SOIC or 16-pin TSSOP package (MPC962309)
- Single 3.3 V supply
- Ambient temperature range: –40°C to +85°C
- Compatible with the CY2305, CY23S05, CY2309, CY23S09
- Spread spectrum compatible

Functional Description

The MPC962309 has two banks of four outputs each, which can be controlled by the Select Inputs as shown in Table 3.Select Input Decoding for MPC962309. Bank B can be tri-stated if all of the outputs are not required. Select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

The MPC962305 and MPC962309 PLLs enters a power down state when there are no rising edges on the REF input. During this state, all of the outputs are in tristate, the PLL is turned off, and there is less than 25.0 μA of current draw for the device. The PLL shuts down in one additional case as shown in Table 3.Select Input Decoding for MPC962309.

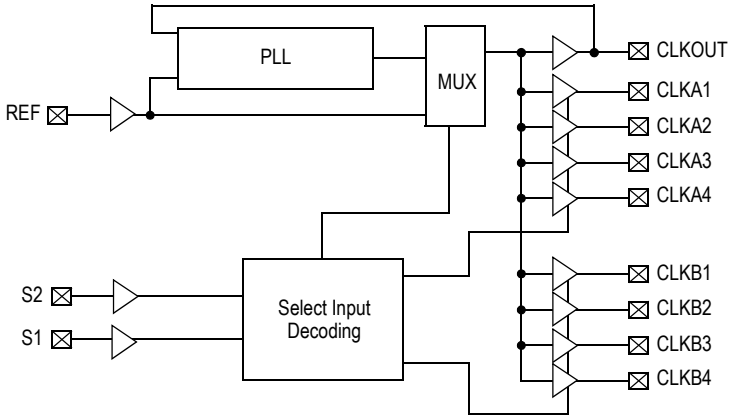
Multiple MPC962305 and MPC962309 devices can accept the same input clock and distribute it throughout the system. In this situation, the difference between the output skews of two devices will be less than 700 ps.

All outputs have less than 200 ps of cycle-cycle jitter. The input-to-output propagation delay on both devices is guaranteed to be less than 350 ps and the output-to-output skew is guaranteed to be less than 250 ps.

The MPC962305 and MPC962309 are available in two/three different configurations, as shown on the ordering information page. The MPC962305-1/MPC962309-1 are the base parts. High drive versions of those devices, MPC962305-1H and MPC962309-1H, are available to provide faster rise and fall times of the base device.

Pentium II is a trademark of Intel Corporation.

Block Diagram



Pin Configuration

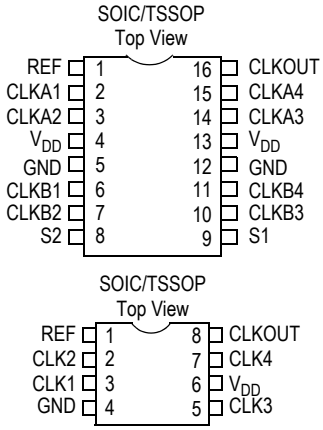


Table 1. Pin Description for MPC962309

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5 V-tolerant input
2	CLKA1[2]	Buffered clock output, Bank A
3	CLKA2[2]	Buffered clock output, Bank A
4	V_{DD}	3.3 V supply
5	GND	Ground
6	CLKB1[2]	Buffered clock output, Bank B
7	CLKB2[2]	Buffered clock output, Bank B
8	S2[3]	Select input, bit 2
9	S1[3]	Select input, bit 1
10	CLKB3[2]	Buffered clock output, Bank B
11	CLKB4[2]	Buffered clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3 V supply
14	CLKA3[2]	Buffered clock output, Bank A
15	CLKA4[2]	Buffered clock output, Bank A
16	CLKOUT[2]	Buffered output, internal feedback on this pin

Table 2. Pin Description for MPC962305

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5 V-tolerant input
2	CLK2[2]	Buffered clock output
3	CLK1[2]	Buffered clock output
4	GND	Ground
5	CLK3[2]	Buffered clock output
6	V_{DD}	3.3 V supply
7	CLK4[2]	Buffered clock output
8	CLKOUT[2]	Buffered clock output, internal feedback on this pin

1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-ups on these inputs.

Table 3. Select Input Decoding for MPC962309

S2	S1	CLOCK A1–A4	CLOCK B1–B4	CLKOUT[1]	Output Source	PLL Shutdown
0	0	Three-State	Three-State	Driven	PLL	N
0	1	Driven	Three-State	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

1. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Table 4. Maximum Ratings

Characteristics	Value	Unit
Supply Voltage to Ground Potential	–0.5 to +3.9	V
DC Input Voltage (Except Ref)	–0.5 to V_{DD}+0.5	V
DC Input Voltage REF	–0.5 to 5.5	V
Storage Temperature	–65 to +150	°C
Junction Temperature	150	°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2000	V

Table 5. Operating Conditions for MPC962305-X and MPC962309-X Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, below 100 MHz		30	pF
C_L	Load Capacitance, from 100 MHz to 133 MHz		10	pF
C_{IN}	Input Capacitance		7	pF

Table 6. Electrical Characteristics for MPC962305-X and MPC962309-X Industrial Temperature Devices[1]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage[2]			0.8	V
V_{IH}	Input HIGH Voltage[2]		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0 V		50.0	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	μA
V_{OL}	Output LOW Voltage[3]	I_{OL} = 8 mA (–1) I_{OH} = 12 mA (–1H)		0.4	V
V_{OH}	Output HIGH Voltage[3]	I_{OH} = –8 mA (–1) I_{OL} = –12 mA (–1H)	2.4		V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		25.0	μA
I_{DD}	Supply Current	Unloaded outputs at 66.67 MHz, SEL inputs at V_{DD}		35.0	mA

1. All parameters are specified with loaded outputs.
2. REF input has a threshold voltage of V_{PP}/2.
3. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 7. Switching Characteristics for MPC962305-1 and MPC962309-1 Industrial Temperature Devices[1]

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30-pF load 10-pF load	10 10		100 133.33	MHz MHz
	Duty Cycle[2] = $t_2 \div t_1$	Measured at 1.4 V, F_{OUT} = 66.67 MHz	40.0	50.0	60.0	%
t_3	Rise Time[2]	Measured between 0.8 V and 2.0 V			2.50	ns
t_4	Fall Time[2]	Measured between 0.8 V and 2.0 V			2.50	ns
t_5	Output to Output Skew[2]	All outputs equally loaded			250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[2]	Measured at $V_{DD}/2$		0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[2]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, MPC962309 device only	1	5	8.7	ns
t_7	Device to Device Skew[2]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices		0	700	ps
t_J	Cycle to Cycle Jitter[2]	Measured at 66.67 MHz, loaded outputs			200	ps
t_{LOCK}	PLL Lock Time[2]	Stable power supply, valid clock presented on REF pin			1.0	ms

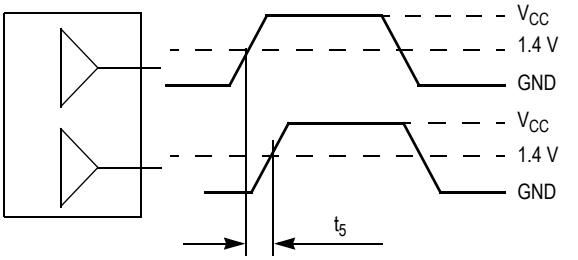
1. All parameters are specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 8. Switching Characteristics for MPC962305-1H and MPC962309-1H Industrial Temperature Devices[1]

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30-pF load 10-pF load	10 10		100 133.33	MHz MHz
	Duty Cycle[2] = t2 ÷ t1	Measured at 1.4 V, F_{OUT} = 66.67 MHz	40.0	50.0	60.0	%
	Duty Cycle[2] = t2 ÷ t1	Measured at 1.4 V, F_{OUT} < 50 MHz	45.0	55.0	55.0	%
t_3	Rise Time[2]	Measured between 0.8 V and 2.0 V			1.50	ns
t_4	Fall Time[2]	Measured between 0.8 V and 2.0 V			1.50	ns
t_5	Output to Output Skew[2]	All outputs equally loaded			250	ps
t_{6A}	Delay, REF Rising Edge to CLKOUT Rising Edge[2]	Measured at $V_{DD}/2$		0	±350	ps
t_{6B}	Delay, REF Rising Edge to CLKOUT Rising Edge[2]	Measured at $V_{DD}/2$. Measured in PLL Bypass Mode, MPC962309 device only	1	5	8.7	ns
t_7	Device to Device Skew[2]	Measured at $V_{DD}/2$ on the CLKOUT pins of devices		0	700	ps
t_8	Output Slew Rate[2]	Measured between 0.8 V and 2.0 V using Test Circuit #2	1			V/ns
t_J	Cycle to Cycle Jitter[2]	Measured at 66.67 MHz, loaded outputs			200	ps
t_{LOCK}	PLL Lock Time[2]	Stable power supply, valid clock presented on REF pin			1.0	ms

1. All parameters are specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

APPLICATIONS INFORMATION



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 1. Output-to-Output Skew $t_{SK(O)}$

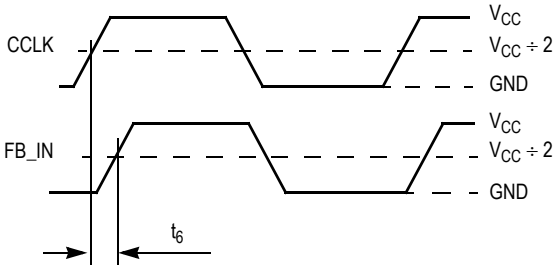
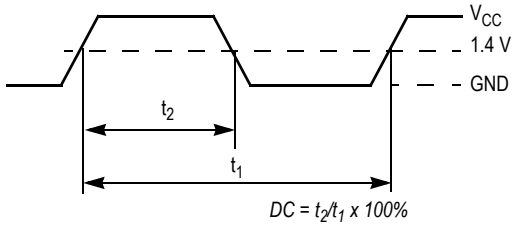


Figure 2. Static Phase Offset Test Reference



The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 3. Output Duty Cycle (DC)

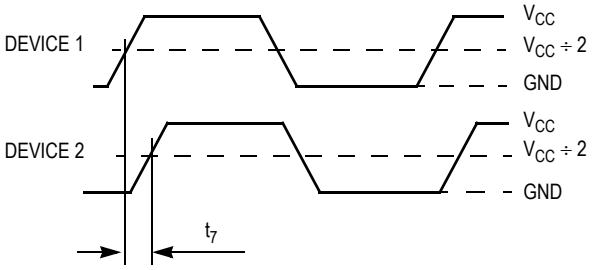
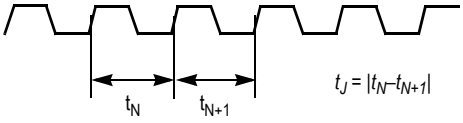


Figure 4. Device-to-Device Skew



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 5. Cycle-to-Cycle Jitter

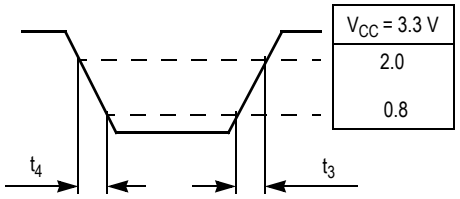
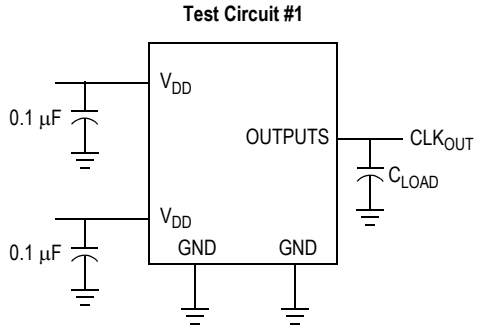
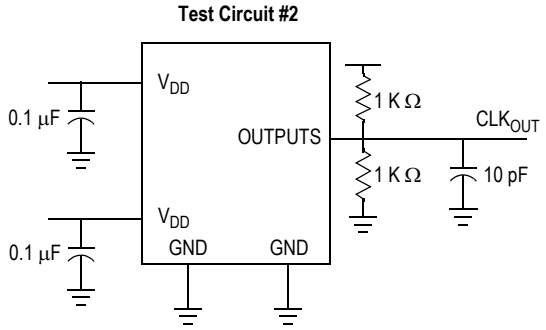


Figure 6. Output Transition Time Test Reference



Test Circuit for all parameters except t_8



Test Circuit for t_8, Output slew rate on –1H, –5 device

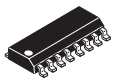
Table 9. Ordering Information

Ordering Code	Package Type
MPC962305D-1	8-pin 150-mil SOIC
MPC962305D-1R2	8-pin 150-mil SOIC-Tape and Reel
MPC962305D-1H	8-pin 150-mil SOIC
MPC962305D-1HR2	8-pin 150-mil SOIC-Tape and Reel
MPC962305DT-1H	8-pin 150-mil TSSOP
MPC962305DT-1HR2	8-pin 150-mil TSSOP-Tape and Reel
MPC962309D-1	16-pin 150-mil SOIC
MPC962309D-1R2	16-pin 150-mil SOIC-Tape and Reel
MPC962309D-1H	16-pin 150-mil SOIC
MPC962309D-1HR2	16-pin 150-mil SOIC-Tape and Reel
MPC962309DT-1H	16-pin 4.4-mm TSSOP
MPC962309DT-1HR2	16-pin 4.4-mm TSSOP-Tape and Reel

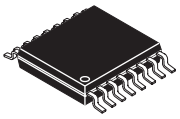
3.3 V Zero Delay Buffer

MPC962308

The MPC962308 is a 3.3 V Zero Delay Buffer designed to distribute high-speed clocks in PC, workstation, datacom, telecom and other high-performance applications. The MPC962308 uses an internal PLL and an external feedback path to lock its low-skew clock output phase to the reference clock phase, providing virtually zero propagation delay. The input-to-output skew is guaranteed to be less than 250 ps and output-to-output skew is guaranteed to be less than 200 ps.



D SUFFIX
16-LEAD SOIC PACKAGE
CASE 751B-05



DT SUFFIX
16-LEAD TSSOP PACKAGE
CASE 948F-01

Features

- 1:8 outputs LVCMOS zero-delay buffer
- Zero input-output propagation delay, adjustable by the capacitive load on FBK input
- Multiple Configurations, see Table 11. Available MPC962308 Configurations
- Multiple low-skew outputs
- 200 ps max output-output skew
- 700 ps max device-device skew
- Two banks of four outputs, output tristate control by two select inputs
- Supports a clock I/O frequency range of 10 MHz to 133 MHz
- Low jitter, 200 ps max cycle-cycle (-1, -1H, -4, -5H)
- ±250 ps static phase offset (SPO)
- 16-pin SOIC package or 16-pin TSSOP package
- Single 3.3 V supply
- Ambient temperature range: –40°C to +85°C
- Compatible with the CY2308 and CY23S08
- Spread spectrum compatible

Functional Description

The MPC962308 has two banks of four outputs each which can be controlled by the select inputs as shown in Table 10. Select Input Decoding. Bank B can be tristated if all of the outputs are not required. The select inputs also allow the input clock to be directly applied to the output for chip and system testing purposes. The MPC962308 PLL enters a power down state when there are no rising edges on the REF input. During this state, all of the outputs are in tristate and there is less than 50 μA of current draw. The PLL shuts down in two additional cases explained in Table 10. Select Input Decoding.

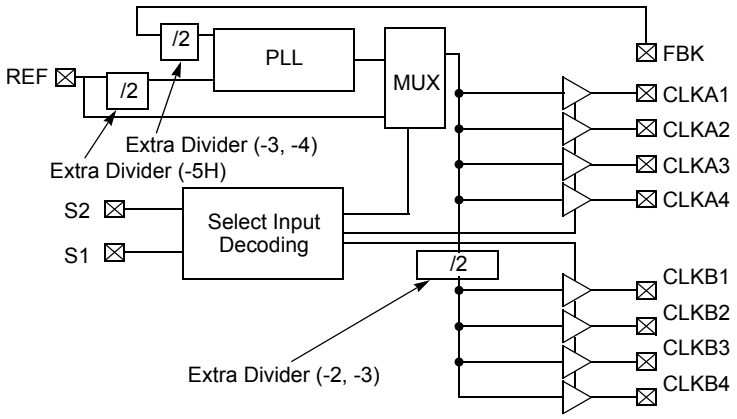
Multiple MPC962308 devices can accept and distribute the same input clock throughout the system. In this situation, the difference between the output skews of two devices will be less than 700 ps.

The MPC962308 is available in five different configurations as shown in Table 11. Available MPC962308 Configurations. In the MPC962308-1, the reference frequency is reproduced by the PLL and provided at the outputs. A high drive version of this configuration, the MPC962308-1H, is available to provide faster rise and fall times of the device.

The MPC962308-2 provides 2X and 1X the reference frequency at the output banks. In addition, the MPC962308-3 provides 4X and 2X the reference frequency at the output banks. The output banks driving the feedback will determine the different configurations of the above devices. The MPC962308-4 provides outputs 2X the reference frequency.The MPC962308-5H is a high drive version with outputs of REF/2.

The MPC962308 is fully 3.3 V compatible and requires no external components for the internal PLL. All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines on the incident edge. Depending on the configuration, the device is offered in a 16-lead SOIC or 16-lead TSSOP package.

Block Diagram



Pin Configuration

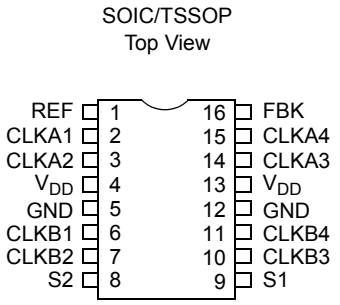


Table 10. Select Input Decoding

S2	S1	CLOCK A1—A4	CLOCK B1—B4	Output Source	PLL Shutdown
0	0	Three-State	Three-State	PLL	Y
0	1	Driven	Three-State	PLL	N
1	0	Driven[1]	Driven[1]	Reference	Y
1	1	Driven	Driven	PLL	N

1. Outputs inverted on MPC962308-2 in bypass mode, S2=1 and S1=0.

Table 11. Available MPC962308 Configurations

Device	Feedback From	Bank A Frequency	Bank B Frequency
MPC962308-1	Bank A or Bank B	Reference	Reference
MPC962308-1H	Bank A or Bank B	Reference	Reference
MPC962308-2	Bank A	Reference	Reference/2
MPC962308-2	Bank B	2 X Reference	Reference
MPC962308-3	Bank A	2 X Reference	Reference or Reference[1]
MPC962308-3	Bank B	4 X Reference	2 X Reference
MPC962308-4	Bank A or Bank B	2 X Reference	2 X Reference
MPC962308-5H	Bank A or Bank B	Reference /2	Reference /2

1. Output phase is indeterminate (0° or 180° from input clock). If phase integrity is required, use the MPC962308-2.

Table 12. Pin Description

Pin	Signal	Description
1	REF[1]	Input reference frequency, 5 V tolerant input
2	CLKA1[2]	Clock output, Bank A
3	CLKA2[2]	Clock output, Bank A
4	V_{DD}	3.3 V supply
5	GND	Ground
6	CLKB1[2]	Clock output, Bank B
7	CLKB2[2]	Clock output, Bank B
8	S2[3]	Select input, bit 2
9	S1[3]	Select input, bit 1
10	CLKB3[2]	Clock output, Bank B
11	CLKB4[2]	Clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3 V supply
14	CLKA3[2]	Clock output, Bank A
15	CLKA4[2]	Clock output, Bank A
16	FBK	PLL feedback input

1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-ups on these inputs.

Table 13. Maximum Ratings

Characteristics	Value	Unit
Supply Voltage to Ground Potential	–0.5 to +3.9	V
DC Input Voltage (Except REF)	–0.5 to V_{DD}+0.5	V
DC Input Voltage REF	–0.5 to 5.5	V
Storage Temperature	–65 to +150	°C
Junction	150	°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2000	V

Table 14. Operating Conditions for MPC962308-X Industrial Temperature Devices

Parameter	Description	Min	Max	Unit
V_{DD}	Supply Voltage	3.0	3.6	V
T_A	Operating Temperature (Ambient Temperature)	–40	85	°C
C_L	Load Capacitance, below 100 MHz		30	pF
	Load Capacitance, from 100 MHz to 133 MHz		15	pF
C_{IN}	Input Capacitance[1]		7	pF

1. Applies to both REF clock and FBK.

Table 15. Electrical Characteristics for MPC962308-X Industrial Temperature Devices[1]

Parameter	Description	Test Conditions	Min	Max	Unit
V_{IL}	Input LOW Voltage			0.8	V
V_{IH}	Input HIGH Voltage		2.0		V
I_{IL}	Input LOW Current	V_{IN} = 0V		50.0	μA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}		100.0	μA
V_{OL}	Output LOW Voltage[2]	I_{OL} = 8 mA (-1, -2, -3, -4) I_{OL} = 12 mA (-1H, -5H)		0.4	V
V_{OH}	Output HIGH Voltage[2]	I_{OH} = -8 mA (-1, -2, -3, -4) I_{OH} = -12 mA (-1H, -5H)	2.4		V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz		25.0	μA
I_{DD}	Supply Current	Unloaded outputs, 100 MHz, Select inputs at V_{DD} or GND		45.0	mA
				70(-1H, -5H)	mA
		Unloaded outputs, 66-MHz REF (-1, -2, -3, -4)		35.0	mA
		Unloaded outputs, 35-MHz REF (-1, -2, -3, -4)		20.0	mA

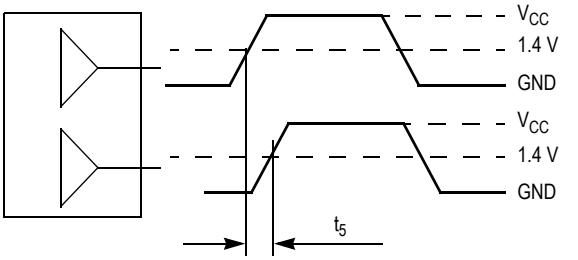
1. All parameters are specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Table 16. Switching Characteristics for MPC962308-X Industrial Temperature Devices[1]

Parameter	Name	Test Conditions	Min	Typ	Max	Unit
t_1	Output Frequency	30-pF load, All devices	10		100	MHz
t_1	Output Frequency[2]	20-pF load, -1H, -5H devices	10		133.3	MHz
t_1	Output Frequency[2]	15-pF load, -1, -2, -3, -4 devices	10		133.3	MHz
	Duty Cycle[2] = $t_2 \div t_1$ (-1, -2, -3, -4, -1H, -5H)	Measured at 1.4 V, FOUT =66.66 MHz 30-pF load	40.0		60.0	%
	Duty Cycle[2] = $t_2 \div t_1$ (-1, -2, -3, -4, -1H, -5H)	Measured at 1.4 V, FOUT <50.0 MHz 15-pF load	45.0		55.0	%
t_3	Rise Time[2] (-1, -2, -3, -4)	Measured between 0.8 V and 2.0 V, 30-pF load			2.50	ns
	Rise Time[2] (-1, -2, -3, -4)	Measured between 0.8 V and 2.0 V, 15-pF load			1.50	ns
	Rise Time[2] (-1H, -5H)	Measured between 0.8 V and 2.0 V, 30-pF load			1.50	ns
t_4	Fall Time[2] (-1, -2, -3, -4)	Measured between 0.8 V and 2.0 V, 30-pF load			2.50	ns
	Fall Time[2] (-1, -2, -3, -4)	Measured between 0.8 V and 2.0 V, 15-pF load			1.50	ns
	Fall Time[2] (-1H, -5H)	Measured between 0.8 V and 2.0 V, 30-pF load			1.25	ns
	Output-to-Output Skew on same Bank (-1, -2, -3, -4)[2]	All outputs equally loaded			200	ps
t_5	Output-to-Output Skew (-1H, -5H)	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (-1, -4, -5H)	All outputs equally loaded			200	ps
	Output Bank A to Output Bank B Skew (-2, -3)	All outputs equally loaded			400	ps
t_6	Delay, REF Rising Edge to FBK Rising Edge[2]	Measured at $V_{DD}/2$		0	±250	ps
t_7	Device-to-Device Skew[2]	Measured at $V_{DD}/2$ on the FBK pins of devices		0	700	ps
t_8	Output Slew Rate[2]	Measured between 0.8 V and 2.0 V on -1H, -5H device using Test Circuit # 2	1			V/ns
t_J	Cycle-to-Cycle Jitter (-1, -1H, -4, -5H)[2]	Measured at 66.67 MHz, loaded outputs, 15-pF load			200	ps
		Measured at 66.67 MHz, loaded outputs, 30-pF load			200	ps
		Measured at 133.3 MHz, loaded outputs, 15 pF load			100	ps
t_J	Cycle-to-Cycle Jitter (-2, -3)[2]	Measured at 66.67 MHz, loaded outputs 30-pF load			400	ps
		Measured at 66.67 MHz, loaded outputs 15-pF load			400	ps
t_{LOCK}	PLL Lock Time[2]	Stable power supply, valid clocks presented on REF and FBK pins			1.0	ms

1. All parameters are specified with loaded outputs.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

APPLICATIONS INFORMATION



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 1. Output-to-Output Skew $t_{SK(O)}$

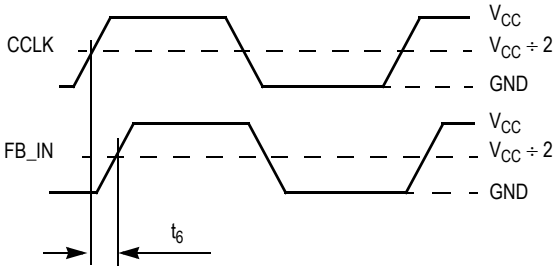
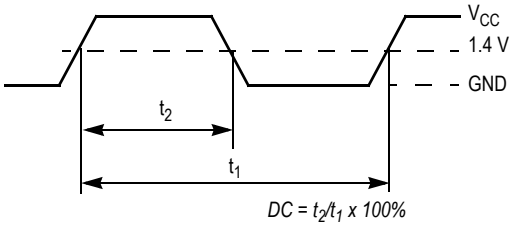


Figure 2. Static Phase Offset Test Reference



The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 3. Output Duty Cycle (DC)

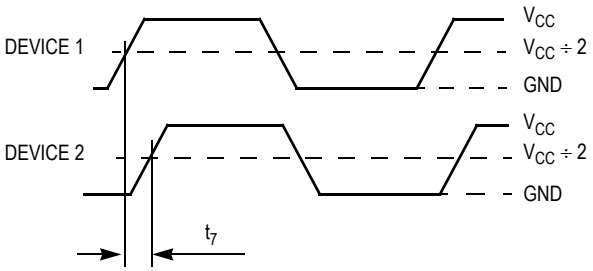
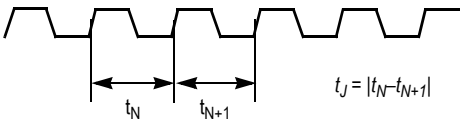


Figure 4. Device-to-Device Skew



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 5. Cycle-to-Cycle Jitter

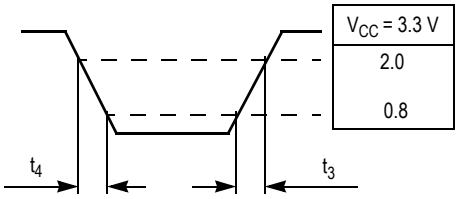
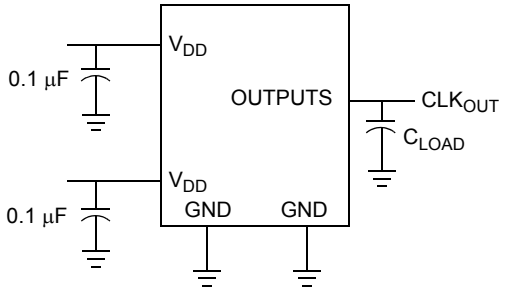


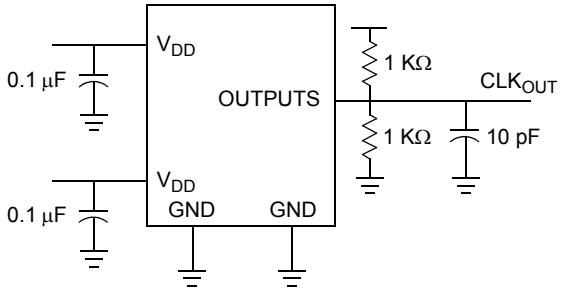
Figure 6. Output Transition Time Test Reference

Test Circuit #1



Test Circuit for all parameters except t_8

Test Circuit #2



Test Circuit for t_8, Output slew rate on -1H, -5 device

Ordering Information (Available)

Ordering Code	Package Name	Package Type
MPC962308D-1	D16	16-pin 150-mil SOIC
MPC962308D-1R2	D16	16-pin 150-mil SOIC — Tape and Reel
MPC962308D-1H	D16	16-pin 150-mil SOIC
MPC962308D-1HR2	D16	16-pin 150-mil SOIC — Tape and Reel
MPC962308DT-1H	DT16	16-pin 150-mil TSSOP
MPC962308DT-1HR2	DT16	16-pin 150-mil TSSOP — Tape and Reel
MPC962308D-2	D16	16-pin 150-mil SOIC
MPC962308D-2R2	D16	16-pin 150-mil SOIC — Tape and Reel

Ordering Information (Planned)

Ordering Code	Package Name	Package Type
MPC962308D-3	D16	16-pin 150-mil SOIC
MPC962308D-3R2	D16	16-pin 150-mil SOIC — Tape and Reel
MPC962308D-4	D16	16-pin 150-mil SOIC
MPC962308D-4R2	D16	16-pin 150-mil SOIC — Tape and Reel
MPC962308D-5H	D16	16-pin 150-mil SOIC
MPC962308D-5HR2	D16	16-pin 150-mil SOIC — Tape and Reel
MPC962308DT-5H	DT16	16-pin 150-mil TSSOP
MPC962308DT-5HR2	DT16	16-pin 150-mil TSSOP — Tape and Reel

Order number: MPC9653
Rev 2, 02/2002

3.3 V 1:8 LVCMOS PLL Clock Generator

MPC9653

LOW VOLTAGE
3.3 V LVCMOS 1:8
PLL CLOCK GENERATOR

FA SUFFIX
32 LEAD LQFP PACKAGE
CASE 873A-03

The MPC9653 is a 3.3 V compatible, 1:8 PLL based clock generator and zero-delay buffer targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking and computing applications. With output frequencies up to 125 MHz and output skews less than 150 ps the device meets the needs of the most demanding clock applications.

Features

- 1:8 PLL based low-voltage clock generator
- Supports zero-delay operation
- 3.3 V power supply
- Generates clock signals up to 125 MHz
- Maximum output skew of 150 ps
- Differential LVPECL reference clock input
- External PLL feedback
- Drives up to 16 clock lines
- 32 lead LQFP packaging
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC953

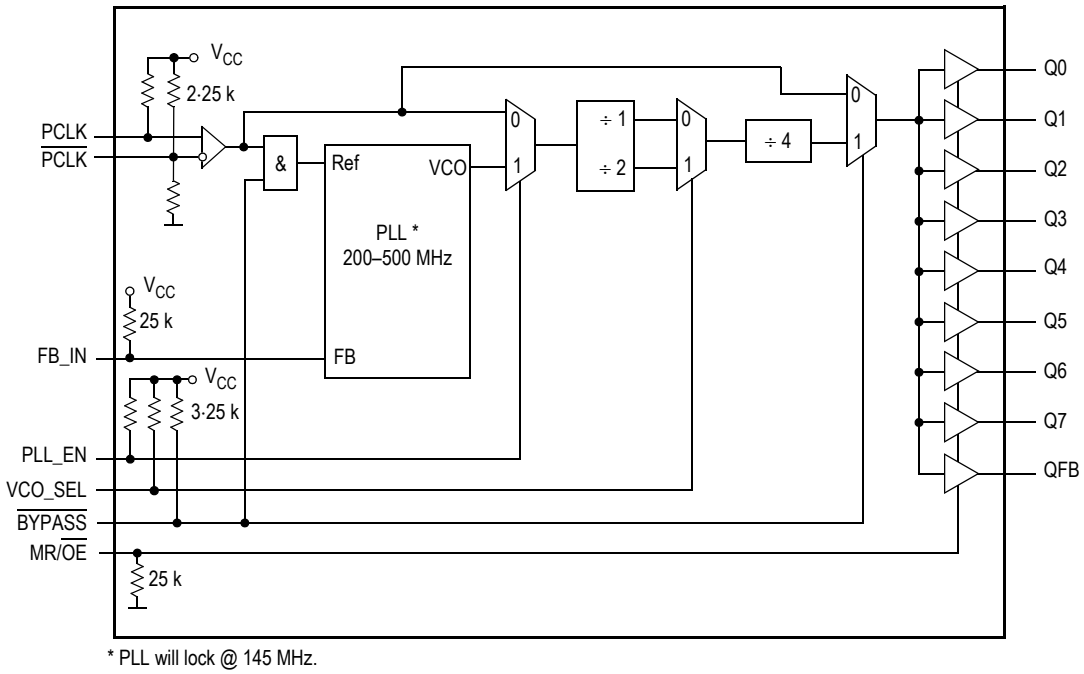
Functional Description

The MPC9653 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9653 requires the connection of the QFB output to the feedback input to close the PLL feedback path (external feedback). With the PLL locked, the output frequency is equal to the reference frequency of the device and VCO_SEL selects the operating frequency range of 25 to 62.5 MHz or 50 to 125 MHz. The two available post-PLL dividers selected by VCO_SEL (divide-by-4 or divide-by-8) and the reference clock frequency determine the VCO frequency. Both must be selected to match the VCO frequency range. The internal VCO of the MPC9653 is running at either 4x or 8x of the reference clock frequency.

The MPC9653 has a differential LVPECL reference input along with an external feedback input. The device is ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance.

The PLL_EN and BYPASS controls select the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is bypassing the PLL and routed either to the output dividers or directly to the outputs. The PLL bypass configurations are fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) and the device reset by asserting the MR/$\overline{OE}$ pin. Asserting MR/OE also causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Deasserting MR/$\overline{OE}$ will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation.

The MPC9653 is fully 3.3 V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS except signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9653 outputs can drive one or two traces giving the devices an effective fanout of 1:16. The device is packaged in a 7x7 mm^2 32-lead LQFP package.



* PLL will lock @ 145 MHz.

Figure 1. MPC9653 Logic Diagram

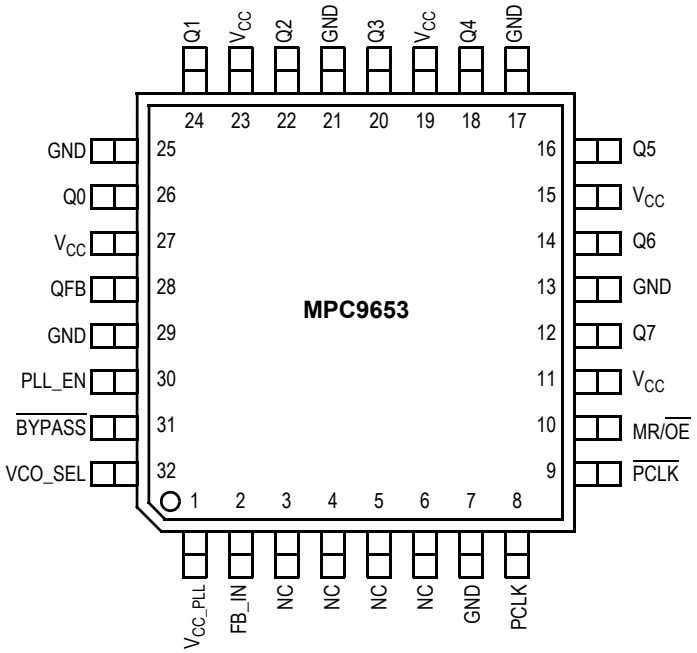


Figure 2. MPC9653 32-Lead Pinout (Top View)

Table 1. Pin Configurations

Number	Name	Type	Description
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	PECL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to QFB
VCO_SEL	Input	LVCMOS	Operating frequency range select
BYPASS	Input	LVCMOS	PLL and output divider bypass select
PLL_EN	Input	LVCMOS	PLL enable/disable
MR/$\overline{\text{OE}}$	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
Q0-7	Output	LVCMOS	Clock outputs
QFB	Output	LVCMOS	Clock output for PLL feedback, connect to FB_IN
GND	Supply	Ground	Negative power supply (GND)
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Please see APPLICATIONS INFORMATION for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table

Control	Default	0	1
PLL_EN	1	Test mode with PLL bypassed. The reference clock (PCLK) is substituted for the internal VCO output. MPC9653 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the VCO output[1]
$\overline{\text{BYPASS}}$	1	Test mode with PLL and output dividers bypassed. The reference clock (PCLK) is directly routed to the outputs. MPC9653 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the output dividers.
VCO_SEL	1	VCO ÷ 1 (High frequency range). $f_{REF} = f_{Q0–7} = 4 \cdot f_{VCO}$	VCO ÷ 2 (Low output range). $f_{REF} = f_{Q0–7} = 8 \cdot f_{VCO}$
MR/$\overline{\text{OE}}$	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset the PLL feedback loop is open. The VCO is tied to its lowest frequency. The length of the reset pulse should be greater than one reference clock cycle (PCLK).

1. PLL operation requires $\overline{\text{BYPASS}}$ = 1 and PLL_EN = 1.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage				0.8	V	LVCMOS
V_{PP}	Peak-to-peak input voltage	(PCLK)	300			mV	LVPECL
V_{CMR}[1]	Common Mode Range	(PCLK)	1.0		V_{CC}–0.6	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA[2]
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output impedance			14 – 17		Ω	
I_{IN}	Input Current[3]				±200	μA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current			5.0	10	mA	V_{CC_PLL} Pin
I_{CCQ}[4]	Maximum Quiescent Supply Current				10	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9653 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines. The MPC9653 meets the V_{OH} and V_{OL} specification of the MPC953 (V_{OH} > V_{CC} –0.6 V at I_{OH}= –20 mA and V_{OL} > 0.6 V at I_{OL}= 20 mA).
3. Inputs have pull-down or pull-up resistors affecting the input current.
4. OE/$\overline{MR}$ = 1 (outputs in high-impedance state).

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Reference Frequency PLL Mode, External Feedback Input reference frequency in PLL bypass mode[4]	÷ 4 feedback[2] ÷ 8 feedback[3]	50 25 0		125 62.5 200	MHz MHz MHz	PLL locked PLL locked
f_{VCO}	VCO Lock Frequency Range[5]		200		500	MHz	
f_{MAX}	Output Frequency	÷ 4 feedback[2] ÷ 8 feedback[3]	50 25		125 62.5	MHz MHz	PLL locked PLL locked
V_{PP}	Peak-to-Peak Input Voltage	PCLK	450		1000	mV	LVPECL
V_{CMR}[6]	Common Mode Range	PCLK	1.2		V_{CC} –0.75	V	LVPECL
$t_{PW,MIN}$	Input Reference Pulse Width[7]		2			ns	
$t_{(\varnothing)}$	Propagation Delay (static phase offset)[8]	PCLK to FB_IN	–75		125	ps	PLL locked
t_{PD}	Propagation Delay PLL and divider bypass ($\overline{BYPASS}$ = 0), PCLK to Q0–7 PLL disable ($\overline{BYPASS}$ = 1 and PLL_EN = 0), PCLK to Q0–7		 1.2 3.0		 3.3 7.0	 ns ns	
$t_{sk(O)}$	Output-to-Output Skew[9]				150	ps	
$t_{sk(PP)}$	Device-to-Device Skew in PLL and Divider Bypass[10]				1.5	ns	$\overline{BYPASS}$ = 0
DC	Output Duty Cycle		45	50	55	%	PLL locked
t_R, t_F	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time				7.0	ns	
$t_{PZL, LZ}$	Output Enable Time				6.0	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter				100	ps	
$t_{JIT(PER)}$	Period Jitter				100	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter[11]	RMS (1σ)			25	ps	
BW	PLL Closed Loop Bandwidth[12] PLL Mode, External Feedback	÷ 4 feedback[2] ÷ 8 feedback[3]			0.8 – 4 0.5 – 1.3	MHz MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. ÷4 PLL feedback (high frequency range) requires VCO_SEL = 0, PLL_EN = 1, $\overline{BYPASS}$ = 1 and MR/$\overline{OE}$ = 0.
3. ÷8 PLL feedback (low frequency range) requires VCO_SEL = 1, PLL_EN = 1, $\overline{BYPASS}$ = 1 and MR/$\overline{OE}$ = 0.
4. In bypass mode, the MPC9653 divides the input reference clock.
5. The input frequency f_{REF} must match the VCO frequency range divided by the feedback divider ratio FB: $f_{REF} = f_{VCO} \div FB$.
6. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
7. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% – DC_{REF,MIN}$.
   For example, at f_{REF} = 100 MHz the input duty cycle range is 20% < DC < 80%.
8. Valid for f_{REF} = 50 MHz and FB = ÷ 8 (VCO_SEL = 1). For other reference frequencies: $t_{(\varnothing)}$ [ps] = 50 ps ± (1 ÷ (120 · f_{REF})).
9. Refer to APPLICATIONS INFORMATION for part-to-part skew calculation in PLL zero-delay mode.
10. For a specified temperature and voltage, includes output skew.
11. I/O phase jitter is reference frequency dependent. Refer to APPLICATIONS INFORMATION for details.
12. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Programming the MPC9653

The MPC9653 supports output clock frequencies from 25 to 125 MHz. Two different feedback divider configurations can be used to achieve the desired frequency operation range. The feedback divider (VCO_SEL) should be used to situate the VCO in the frequency lock range between 200 and 500 MHz for stable and optimal operation. Two operating frequency ranges are supported: 25 to 62.5 MHz and 50 to 125 MHz. Table 7.MPC9653 Configurations (QFB connected to FB_IN) illustrates the configurations supported by the MPC9653. PLL zero-delay is supported if BYPASS = 1, PLL_EN = 1 and the input frequency is within the specified PLL reference frequency range.

Table 7. MPC9653 Configurations (QFB connected to FB_IN)

BYPASS	PLL_EN	VCO_SEL	Operation	Frequency		
				Ratio	Output range ($f_{Q0–7}$)	VCO
0	X	X	Test mode: PLL and divider bypass	$f_{Q0–7} = f_{REF}$	0_200 MHz	n/a
1	0	0	Test mode: PLL bypass	$f_{Q0–7} = f_{REF} \div 4$	0_50 MHz	n/a
1	0	1	Test mode: PLL bypass	$f_{Q0–7} = f_{REF} \div 8$	0_25 MHz	n/a
1	1	0	PLL mode (high frequency range)	$f_{Q0–7} = f_{REF}$	50 to 125 MHz	$f_{VCO} = f_{REF} \cdot 4$
1	1	1	PLL mode (low frequency range)	$f_{Q0–7} = f_{REF}$	25 to 62.5 MHz	$f_{VCO} = f_{REF} \cdot 8$

Power Supply Filtering

The MPC9653 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9653 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9653. Figure 3 illustrates a typical power supply filter scheme. The MPC9653 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CC_PLL} pin) is typically 5 mA (10 mA maximum), assuming that a minimum of 2.985 V must be maintained on the V_{CC_PLL} pin.

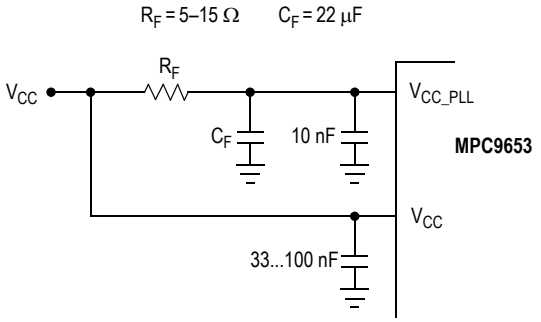


Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 4 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9653 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9653 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9653. Designs using the MPC9653 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9653 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9653 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9653 are connected together, the maximum overall timing uncertainty from the common PCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of four components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

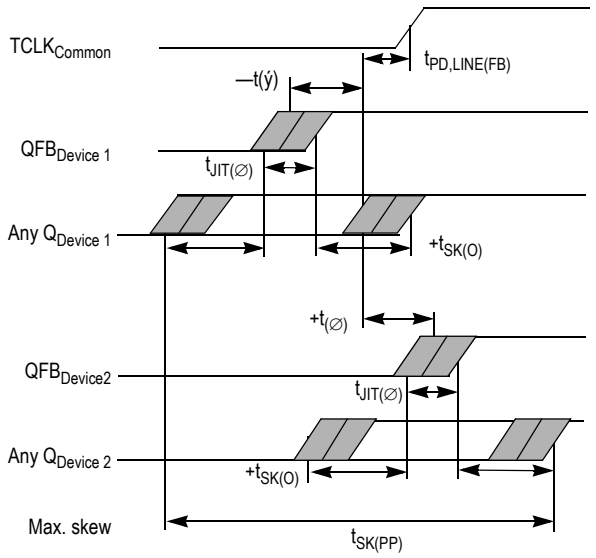


Figure 4. MPC9653 Max. Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.Confidence Factor CF.

Table 8. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of – 197 ps to 297 ps (at 125 MHz reference frequency) relative to PCLK:

$$t_{SK(PP)} = [–17ps...117ps] + [–150ps...150ps] + [(10ps \cdot –3)...(10ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [–197ps...297ps] + t_{PD,\ LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 5 can be used for a more precise timing performance analysis.

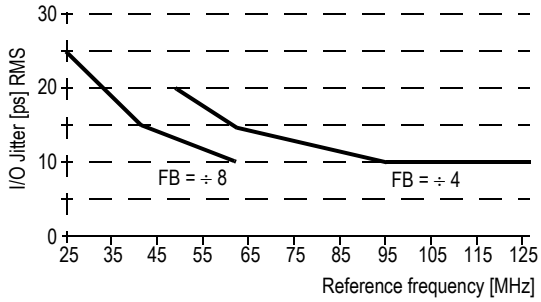


Figure 5. Max. I/O Jitter versus Frequency

Driving Transmission Lines

The MPC9653 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola Application Note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9653 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9653 clock driver is effectively doubled due to its capability to drive multiple lines.

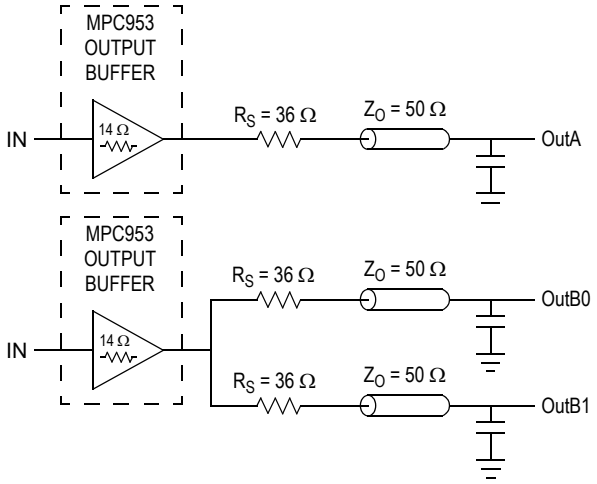


Figure 6. Single versus Dual Transmission Lines

The waveform plots in Figure 7 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9653 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9653. The output waveform in Figure 7 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18 + 14 + 25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0ns).

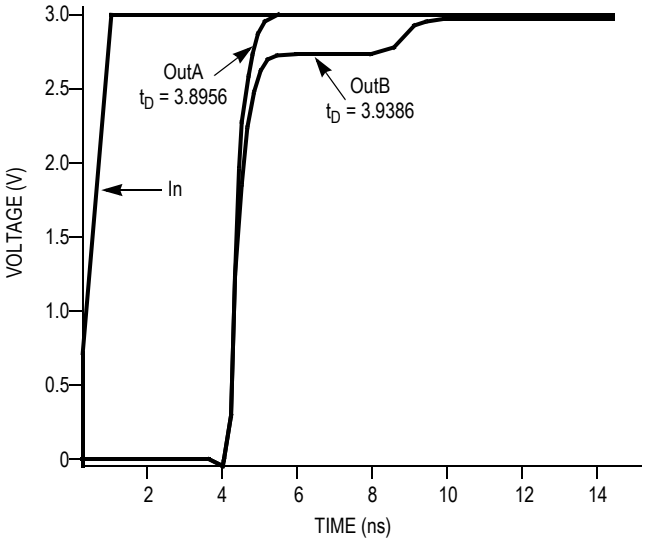
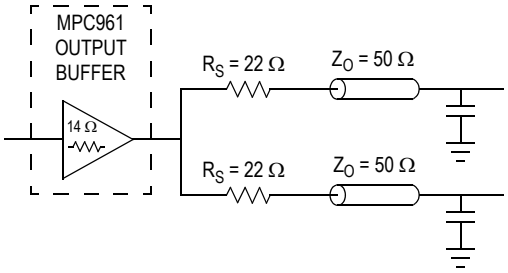


Figure 7. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\ \Omega + 22\ \Omega \parallel 22\ \Omega = 50\ \Omega \parallel 50\ \Omega$
$25\ \Omega = 25\ \Omega$

Figure 8. Optimized Dual Line Termination

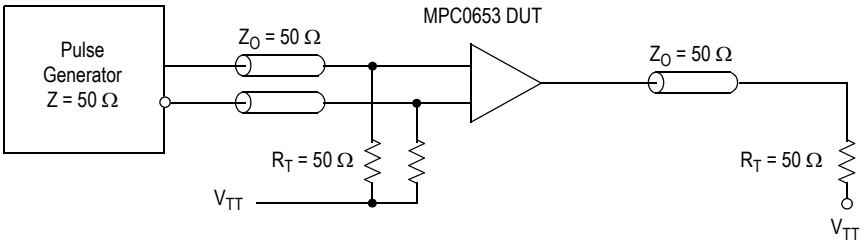
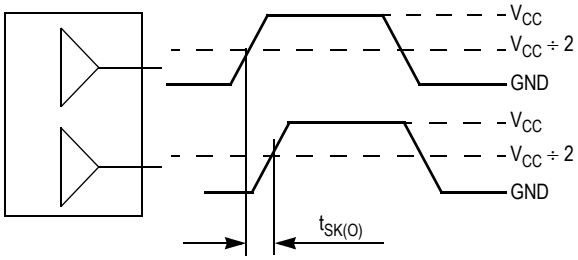


Figure 9. PCLK MPC9653 AC Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output-to-Output Skew $t_{SK(O)}$

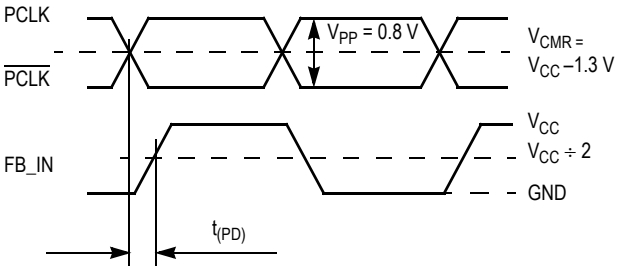
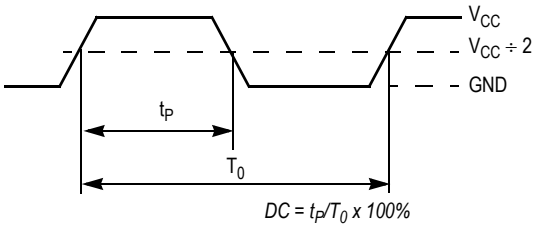
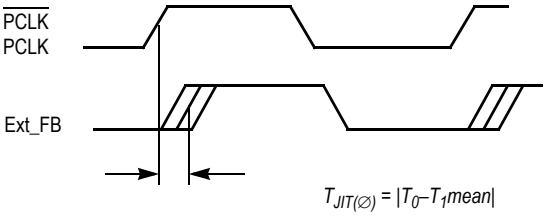


Figure 11. Propagation delay ($t_{(PD)}$, static phase offset) Test Reference



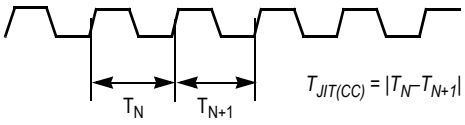
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 12. Output Duty Cycle (DC)



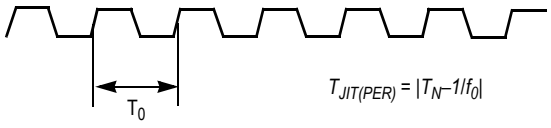
The deviation in t_0 for a controlled edge with respect to a T_0 mean in a random sample of cycles

Figure 13. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 14. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 15. Period Jitter

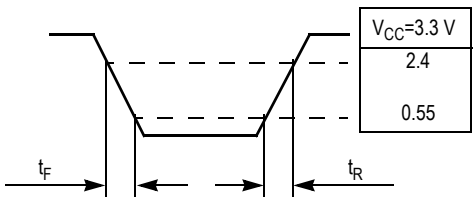


Figure 16. Output Transition Time Test Reference

Order number: MPC9653A
Rev 3, 08/2004

3.3 V 1:8 LVCMOS PLL Clock Generator

MPC9653A

LOW VOLTAGE
3.3 V LVCMOS 1:8
PLL CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

AC SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC9653A is a 3.3 V compatible, 1:8 PLL based clock generator and zero-delay buffer targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking and computing applications. With output frequencies up to 125 MHz and output skews less than 150 ps the device meets the needs of the most demanding clock applications.

Features

- 1:8 PLL based low-voltage clock generator
- Supports zero-delay operation
- 3.3 V power supply
- Generates clock signals up to 125 MHz
- PLL guaranteed to lock down to 145 MHz, output frequency = 36.25 MHz
- Maximum output skew of 150 ps
- Differential LVPECL reference clock input
- External PLL feedback
- Drives up to 16 clock lines
- 32-lead LQFP packaging
- 32-lead Pb-free Package Available
- Ambient temperature range 0°C to +70°C
- Pin and function compatible to the MPC953 and MPC9653

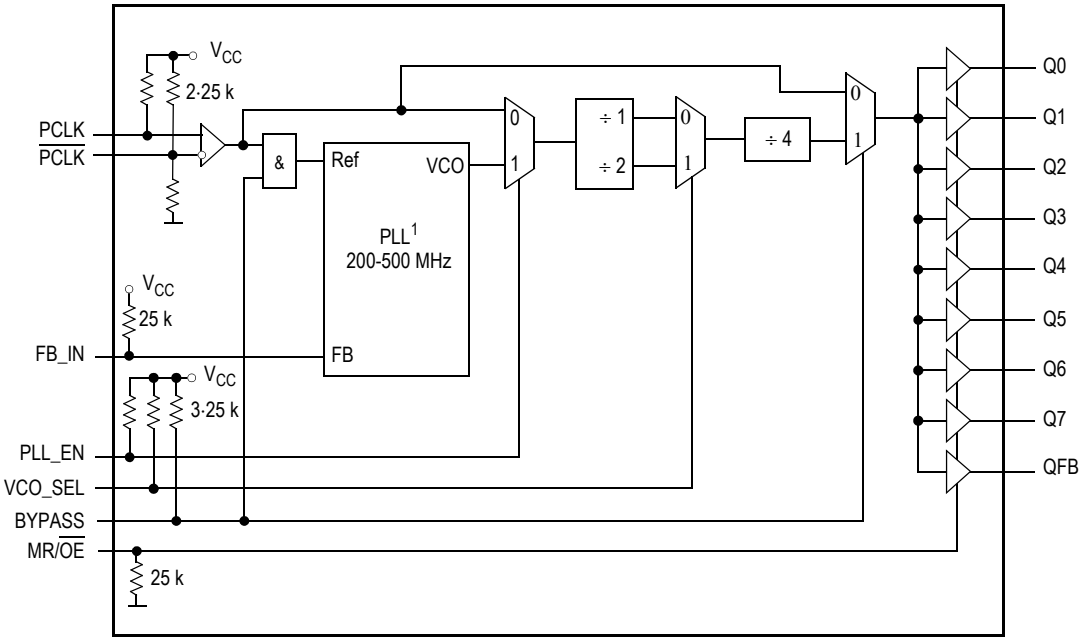
Functional Description

The MPC9653A utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9653A requires the connection of the QFB output to the feedback input to close the PLL feedback path (external feedback). With the PLL locked, the output frequency is equal to the reference frequency of the device and VCO_SEL selects the operating frequency range of 25 to 62.5 MHz or 50 to 125 MHz. The two available post-PLL dividers selected by VCO_SEL (divide-by-4 or divide-by-8) and the reference clock frequency determine the VCO frequency. Both must be selected to match the VCO frequency range. The internal VCO of the MPC9653A is running at either 4x or 8x of the reference clock frequency. The MPC9653A is guaranteed to lock in a low power PLL mode in the high frequency range (VCO_SEL = 0) down to PLL = 145 MHz or F_{ref} = 36.25 MHz.

The MPC9653A has a differential LVPECL reference input along with an external feedback input. The device is ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance.

The PLL_EN and $\overline{\text{BYPASS}}$ controls select the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is bypassing the PLL and routed either to the output dividers or directly to the outputs. The PLL bypass configurations are fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) and the device reset by asserting the MR/OE pin. Asserting MR/OE also causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Deasserting MR/OE will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation.

The MPC9653A is fully 3.3 V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9653A outputs can drive one or two traces giving the devices an effective fanout of 1:16. The device is packaged in a 7x7 mm^2 32-lead LQFP package.



Note 1. PLL will lock @ 145 MHz

Figure 1. MPC9653A Logic Diagram

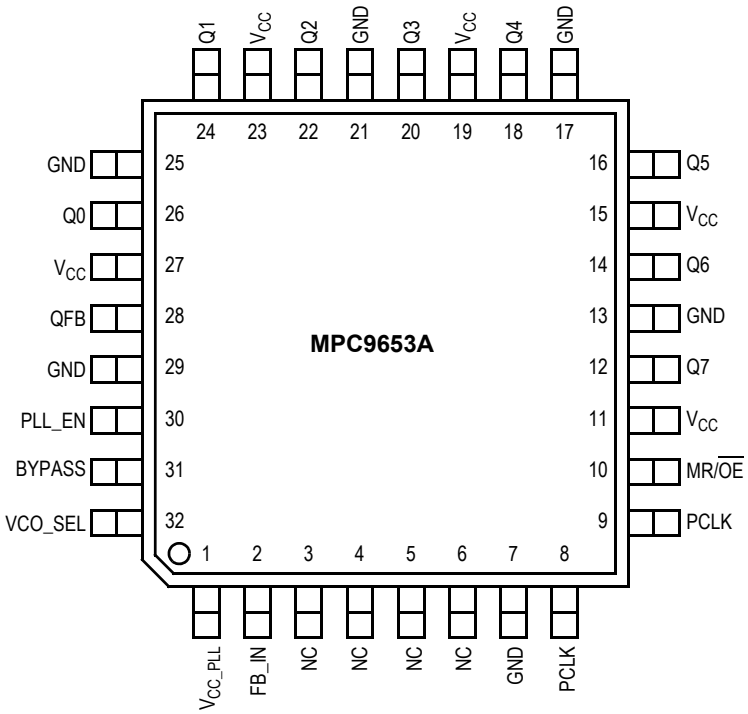


Figure 2. MPC9653A 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	PECL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to QFB
VCO_SEL	Input	LVCMOS	Operating frequency range select
$\overline{\text{BYPASS}}$	Input	LVCMOS	PLL and output divider bypass select
PLL_EN	Input	LVCMOS	PLL enable/disable
MR/$\overline{\text{OE}}$	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
Q0–7	Output	LVCMOS	Clock outputs
QFB	Output	LVCMOS	Clock output for PLL feedback, connect to FB_IN
GND	Supply	Ground	Negative power supply (GND)
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Refer to APPLICATIONS INFORMATION for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 2. Function Table

Control	Default	0	1
PLL_EN	1	Test mode with PLL bypassed. The reference clock (PCLK) is substituted for the internal VCO output. MPC9653A is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the VCO output[1]
$\overline{\text{BYPASS}}$	1	Test mode with PLL and output dividers bypassed. The reference clock (PCLK) is directly routed to the outputs. MPC9653A is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the output dividers.
VCO_SEL	1	VCO ÷ 1 (High frequency range). $f_{REF} = f_{Q0–7} = 4 \cdot f_{VCO}$	VCO ÷ 2 (Low output range). $f_{REF} = f_{Q0–7} = 8 \cdot f_{VCO}$
MR/$\overline{\text{OE}}$	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset the PLL feedback loop is open. The VCO is tied to its lowest frequency. The length of the reset pulse should be greater than one reference clock cycle (PCLK).

1. PLL operation requires $\overline{\text{BYPASS}}$ = 1 and PLL_EN = 1.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage				0.8	V	LVCMOS
V_{PP}	Peak-to-peak input voltage	(PCLK)	300			mV	LVPECL
V_{CMR}[1]	Common Mode Range	(PCLK)	1.0		V_{CC} – 0.6	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA[2]
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output impedance			14 – 17		Ω	
I_{IN}	Input Current[3]				±200	μA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current			5.0	10	mA	V_{CC_PLL} Pin
I_{CCQ}[4]	Maximum Quiescent Supply Current				10	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9653A is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines. The MPC9653A meets the V_{OH} and V_{OL} specification of the MPC953 (V_{OH} > V_{CC} -0.6 V at I_{OH} = -20 mA and V_{OL} > 0.6 V at I_{OL} = 20 mA).
3. Inputs have pull-down or pull-up resistors affecting the input current.
4. OE/$\overline{MR}$ = 1 (outputs in high-impedance state).

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input Reference Frequency	÷ 4 feedback[2]	50		125	MHz	PLL locked
	PLL Mode, External Feedback	÷ 8 feedback[3]	25		62.5	MHz	PLL locked
	Input reference frequency in PLL bypass mode[4]		0		200	MHz	
f_{VCO}	VCO Operating Frequency Range[5, 6]		200		500	MHz	
$f_{VCOlock}$	VCO Lock Frequency Range[7]		145		500	MHz	
f_{MAX}	Output Frequency	÷ 4 feedback[2]	50		125	MHz	PLL locked
		÷ 8 feedback[3]	25		62.5	MHz	PLL locked
V_{PP}	Peak-to-Peak Input Voltage	PCLK	450		1000	mV	LVPECL
V_{CMR}[8]	Common Mode Range	PCLK	1.2		V_{CC} – 0.75	V	LVPECL
$t_{PW, MIN}$	Input Reference Pulse Width[9]		2			ns	
$t_{(\varnothing)}$	Propagation Delay (static phase offset)[10]	PCLK to FB_IN	–75		125	ps	PLL locked
t_{PD}	Propagation Delay						
	PLL and divider bypass ($\overline{BYPASS}$ = 0), PCLK to Q0–7		1.2		3.3	ns	
	PLL disable ($\overline{BYPASS}$ = 1 and PLL_EN = 0), PCLK to Q0–7		3.0		7.0	ns	
$t_{sk(O)}$	Output-to-Output Skew[11]				150	ps	
$t_{sk(PP)}$	Device-to-Device Skew in PLL and Divider Bypass[12]				1.5	ns	$\overline{BYPASS}$ = 0
DC	Output Duty Cycle		45	50	55	%	PLL locked
t_R, t_F	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time				7.0	ns	
$t_{PZL, LZ}$	Output Enable Time				6.0	ns	
$t_{JIT(CC)}$	Cycle-to-Cycle jitter				100	ps	
$t_{JIT(PER)}$	Period Jitter				100	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter[13]	RMS (1σ)			25	ps	
BW	PLL closed loop bandwidth[14]	÷ 4 feedback[2]			0.8 – 4	MHz	
	PLL mode, external feedback	÷ 8 feedback[3]			0.5 – 1.3	MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. ÷ 4 PLL feedback (high frequency range) requires VCO_SEL = 0, PLL_EN = 1, $\overline{BYPASS}$ = 1 and MR/$\overline{OE}$ = 0.
3. ÷ 8 PLL feedback (low frequency range) requires VCO_SEL = 1, PLL_EN = 1, $\overline{BYPASS}$ = 1 and MR/$\overline{OE}$ = 0.
4. In bypass mode, the MPC9653A divides the input reference clock.
5. The input frequency f_{REF} must match the VCO frequency range divided by the feedback divider ratio FB: $f_{REF} = f_{VCO} \div FB$.
6. f_{VCO} is frequency range where AC parameters are guaranteed.
7. $f_{VCOlock}$ is frequency range that the PLL guaranteed to lock, AC parameters only guaranteed over f_{VCO}.
8. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
9. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% - DC_{REF,MIN}$.
   For example, at f_{REF} = 100 MHz the input duty cycle range is 20% < DC < 80%.
10. Valid for f_{REF} = 50 MHz and FB = ÷ 8 (VCO_SEL = 1). For other reference frequencies: $t_{(\varnothing)}$ [ps] = 50 ps ± (1 ÷ (120 · f_{REF})).
11. Refer to the Application Information section for part-to-part skew calculation in PLL zero-delay mode.
12. For a specified temperature and voltage, includes output skew.
13. I/O phase jitter is reference frequency dependent. Refer to APPLICATIONS INFORMATION section for details.
14. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Programming the MPC9653A

The MPC9653A supports output clock frequencies from 25 to 125 MHz. Two different feedback divider configurations can be used to achieve the desired frequency operation range. The feedback divider (VCO_SEL) should be used to situate the VCO in the frequency lock range between 200 and 500 MHz for stable and optimal operation. Two operating frequency ranges are supported: 25 to 62.5 MHz and 50 to 125 MHz. Table 7 illustrates the configurations supported by the MPC9653A. PLL zero-delay is supported if $\overline{\text{BYPASS}}$ = 1, PLL_EN = 1 and the input frequency is within the specified PLL reference frequency range.

Table 7. MPC9653A Configurations (QFB connected to FB_IN)

$\overline{\text{BYPASS}}$	PLL_EN	VCO_SEL	Operation	Frequency		
				Ratio	Output Range (f_{Q0-7})	VCO
0	X	X	Test mode: PLL and divider bypass	$f_{Q0-7} = f_{REF}$	0 – 200 MHz	n/a
1	0	0	Test mode: PLL bypass	$f_{Q0-7} = f_{REF} \div 4$	0 – 50 MHz	n/a
1	0	1	Test mode: PLL bypass	$f_{Q0-7} = f_{REF} \div 8$	0 – 25 MHz	n/a
1	1	0	PLL mode (high frequency range)	$f_{Q0-7} = f_{REF}$	50 to 125 MHz	$f_{VCO} = f_{REF} \cdot 4$
1	1	1	PLL mode (low frequency range)	$f_{Q0-7} = f_{REF}$	25 to 62.5 MHz	$f_{VCO} = f_{REF} \cdot 8$

Power Supply Filtering

The MPC9653A is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9653A provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9653A. Figure 3 illustrates a typical power supply filter scheme. The MPC9653A frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore, the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CCA} current (the current sourced through the V_{CC_PLL} pin) is typically 5 mA (10 mA maximum), assuming that a minimum of 2.985 V must be maintained on the V_{CC_PLL} pin.

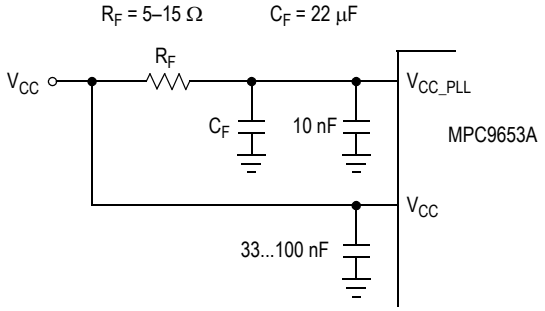


Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 4 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9653A has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9653A in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9653A. Designs using the MPC9653A as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9653A clock driver allows for its use as a zero-delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9653A zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9653As are connected together, the maximum overall timing uncertainty from the common PCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of 4 components: static phase offset, output skew, feedback board trace delay and I/O (phase) jitter:

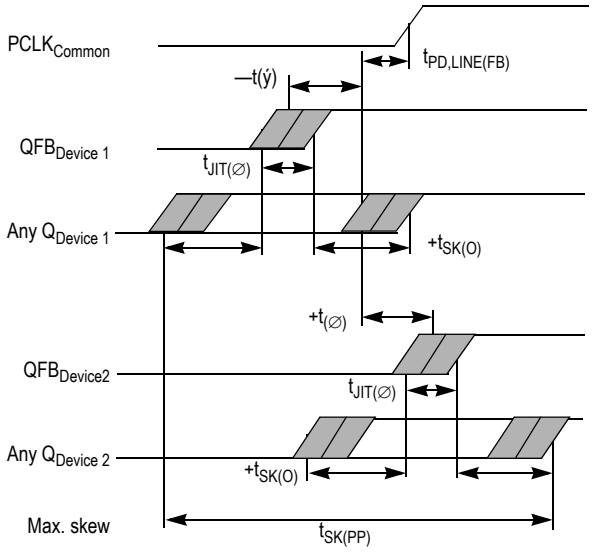


Figure 4. MPC9653A Maximum Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1 σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.

Table 8. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –197 ps to 297 ps (at 125 MHz reference frequency) relative to PCLK:

$$t_{SK(PP)} = [-17ps...117ps] + [-150ps...150ps] + [(10ps\ @\ -3)...(10ps\ @\ 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [-197ps...297ps] + t_{PD,\ LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 5, can be used for a more precise timing performance analysis.

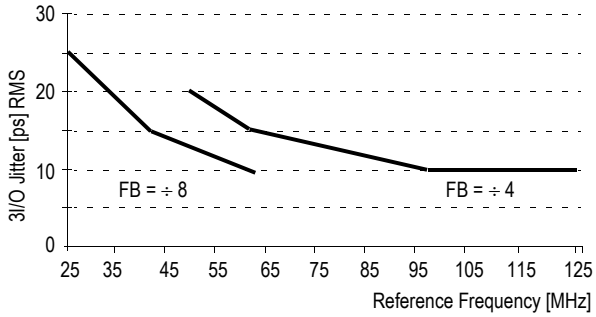


Figure 5. Maximum I/O Jitter versus Frequency

Driving Transmission Lines

The MPC9653A clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9653A clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 5, illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9653A clock driver is effectively doubled due to its capability to drive multiple lines.

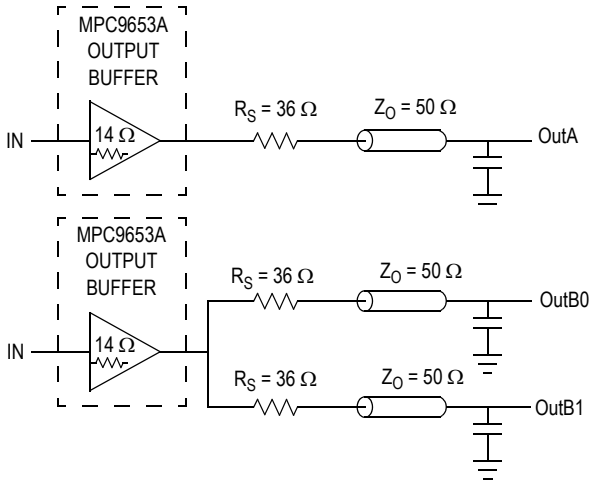


Figure 6. Single versus Dual Transmission Lines

The waveform plots in Figure 7 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9653A output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9653A. The output waveform in Figure 7 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$

$Z_0 = 50\ \Omega \parallel 50\ \Omega$

$R_S = 36\ \Omega \parallel 36\ \Omega$

$R_0 = 14\ \Omega$

$V_L = 3.0 (25 \div (18 + 14 + 25)$

$= 1.31$ V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

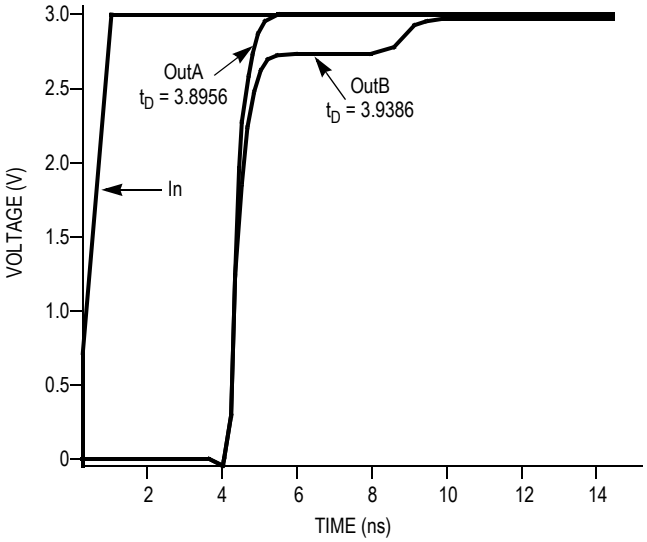
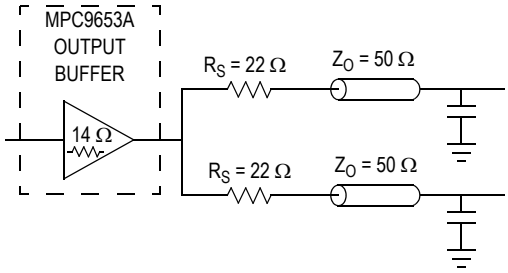


Figure 7. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 8, should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\ \Omega + 22\ \Omega \parallel 22\ \Omega = 50\ \Omega \parallel 50\ \Omega$

$25\ \Omega = 25\ \Omega$

Figure 8. Optimized Dual Line Termination

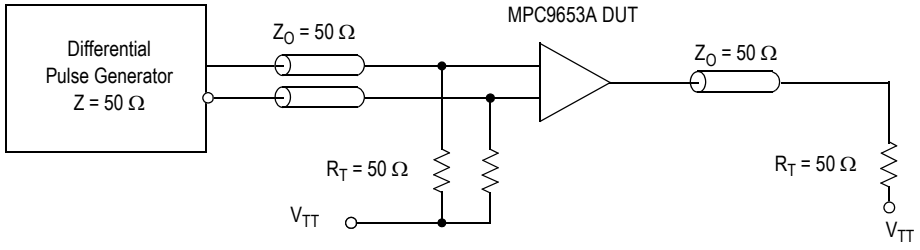
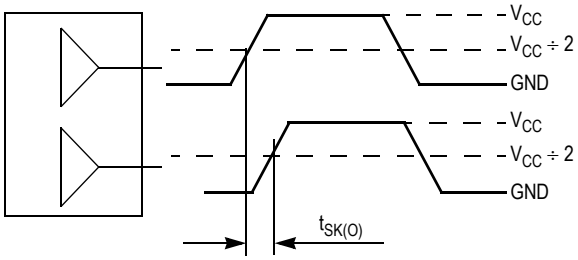


Figure 9. MPC9653A AC Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output-to-Output Skew $t_{SK(O)}$

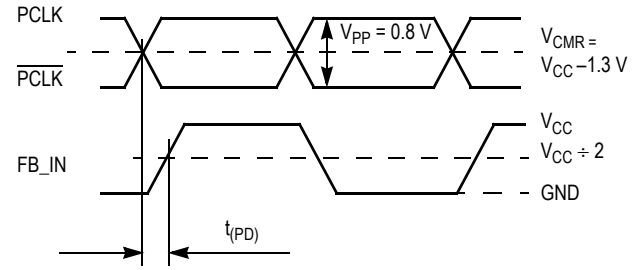
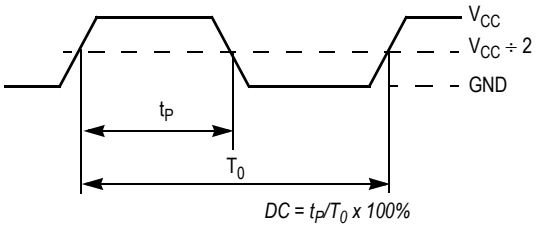
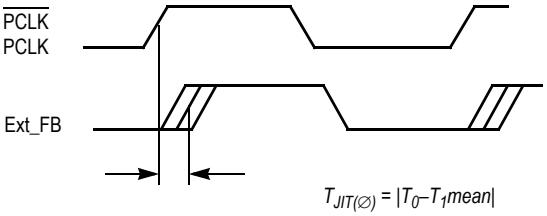


Figure 11. Propagation delay ($t_{(PD)}$, static phase offset) Test Reference



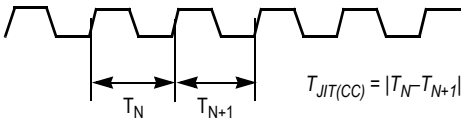
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 12. Output Duty Cycle (DC)



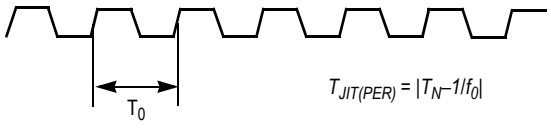
The deviation in t_0 for a controlled edge with respect to a T_0 mean in a random sample of cycles

Figure 13. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 14. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 15. Period Jitter

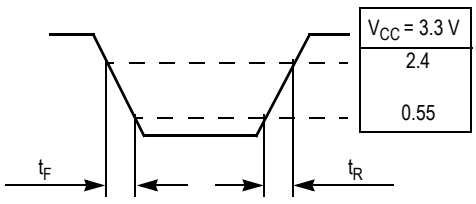


Figure 16. Output Transition Time Test Reference

Order number: MPC9658
Rev 4, 08/2004

3.3 V 1:10 LVCMOS PLL Clock Generator

MPC9658

LOW VOLTAGE
3.3 V LVCMOS 1:10
PLL CLOCK GENERATOR

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC9658 is a 3.3 V compatible, 1:10 PLL based clock generator and zero-delay buffer targeted for high performance low-skew clock distribution in mid-range to high-performance telecom, networking and computing applications. With output frequencies up to 250 MHz and output skews less than 120 ps the device meets the needs of the most demanding clock applications. The MPC9658 is specified for the temperature range of 0°C to +70°C.

Features

- 1:10 PLL based low-voltage clock generator
- Supports zero-delay operation
- 3.3 V power supply
- Generates clock signals up to 250 MHz
- Maximum output skew of 120 ps
- Differential LVPECL reference clock input
- External PLL feedback
- Drives up to 20 clock lines
- 32-lead LQFP packaging
- 32-lead Pb-free Package Available
- Pin and function compatible to the MPC958

Functional Description

The MPC9658 utilizes PLL technology to frequency lock its outputs onto an input reference clock. Normal operation of the MPC9658 requires the connection of the QFB output to the feedback input to close the PLL feedback path (external feedback). With the PLL locked, the output frequency is equal to the reference frequency of the device and VCO_SEL selects the operating frequency range of 50 to 125 MHz or 100 to 250 MHz. The two available post-PLL dividers selected by VCO_SEL (divide-by-2 or divide-by-4) and the reference clock frequency determine the VCO frequency. Both must be selected to match the VCO frequency range. The internal VCO of the MPC9658 is running at either 2x or 4x of the reference clock frequency.

The MPC9658 has a differential LVPECL reference input along with an external feedback input. The MPC9658 is ideal for use as a zero delay, low skew fanout buffer. The device performance has been tuned and optimized for zero delay performance.

The PLL_EN and BYPASS controls select the PLL bypass configuration for test and diagnosis. In this configuration, the selected input reference clock is bypassing the PLL and routed either to the output dividers or directly to the outputs. The PLL bypass configurations are fully static and the minimum clock frequency specification and all other PLL characteristics do not apply. The outputs can be disabled (high-impedance) and the device reset by asserting the MR/$\overline{OE}$ pin. Asserting MR/$\overline{OE}$ also causes the PLL to loose lock due to missing feedback signal presence at FB_IN. Deasserting MR/$\overline{OE}$ will enable the outputs and close the phase locked loop, enabling the PLL to recover to normal operation.

The MPC9658 is fully 3.3 V compatible and requires no external loop filter components. The inputs (except PCLK) accept LVCMOS except signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9658 outputs can drive one or two traces giving the devices an effective fanout of 1:16. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

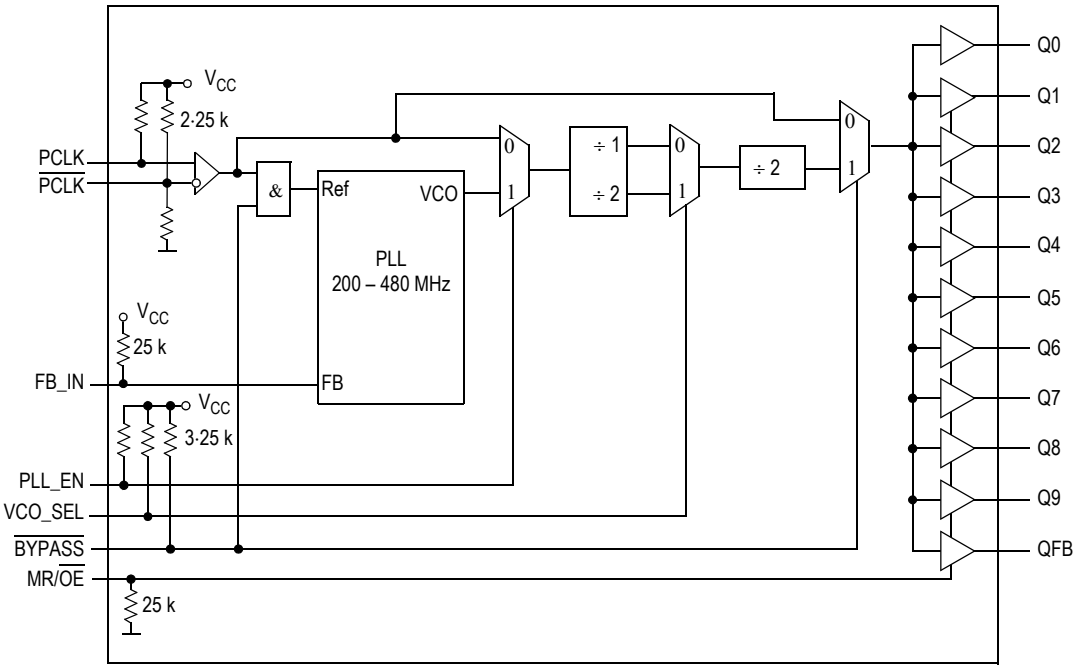


Figure 1. MPC9658 Logic Diagram

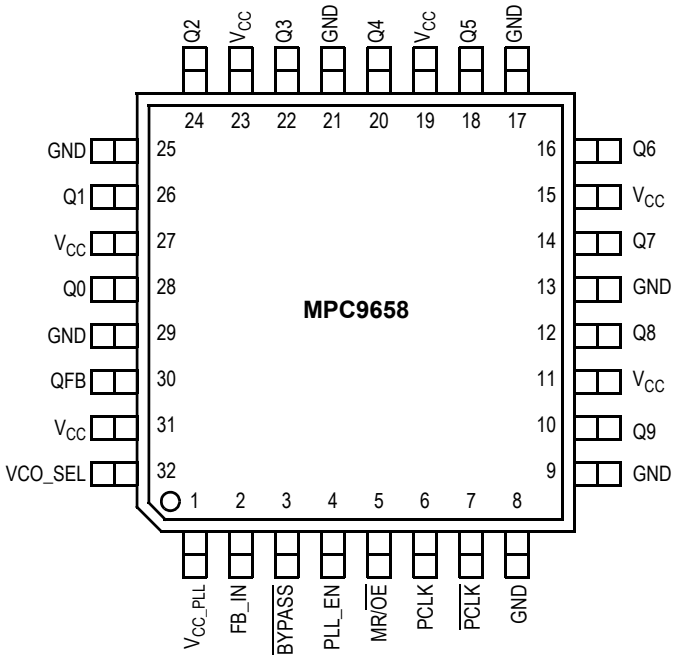


Figure 2. MPC9658 32-Lead Pinout (Top View)

Table 1. Pin Configurations

Number	Name	Type	Description
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	PECL reference clock signal
FB_IN	Input	LVCMOS	PLL feedback signal input, connect to QFB
VCO_SEL	Input	LVCMOS	Operating frequency range select
$\overline{\text{BYPASS}}$	Input	LVCMOS	PLL and output divider bypass select
PLL_EN	Input	LVCMOS	PLL enable/disable
MR/$\overline{\text{OE}}$	Input	LVCMOS	Output enable/disable (high-impedance tristate) and device reset
Q0–9	Output	LVCMOS	Clock outputs
QFB	Output	LVCMOS	Clock output for PLL feedback, connect to FB_IN
GND	Supply	Ground	Negative power supply (GND)
V_{CC_PLL}	Supply	V_{CC}	PLL positive power supply (analog power supply). It is recommended to use an external RC filter for the analog power supply pin V_{CC_PLL}. Refer to APPLICATIONS INFORMATION for details.
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation.

Table 2. Function Table

Control	Default	0	1
PLL_EN	1	Test mode with PLL bypassed. The reference clock (PCLK) is substituted for the internal VCO output. MPC9658 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the VCO output.[1]
$\overline{\text{BYPASS}}$	1	Test mode with PLL and output dividers bypassed. The reference clock (PCLK) is directly routed to the outputs. MPC9658 is fully static and no minimum frequency limit applies. All PLL related AC characteristics are not applicable.	Selects the output dividers.
VCO_SEL	1	VCO ÷ 1 (High frequency range). $f_{REF} = f_{Q0–9} = 2 \cdot f_{VCO}$	VCO ÷ 2 (Low output range). $f_{REF} = f_{Q0–9} = 4 \cdot f_{VCO}$
MR/$\overline{\text{OE}}$	0	Outputs enabled (active)	Outputs disabled (high-impedance state) and reset of the device. During reset the PLL feedback loop is open. The VCO is tied to its lowest frequency. The length of the reset pulse should be greater than one reference clock cycle (PCLK).

1. PLL operation requires $\overline{\text{BYPASS}}$ = 1 and PLL_EN = 1.

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} +0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} +0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	LQFP 32 Thermal resistance junction to ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	LQFP 32 Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage			0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage (PCLK)	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range (PCLK)	1.0		V_{CC} –0.6	V	LVPECL
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA[2]
V_{OL}	Output Low Voltage[3]			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance		14 – 17		Ω	
I_{IN}	Input Current[4]			±200	μA	V_{IN} = V_{CC} or GND
I_{CC_PLL}	Maximum PLL Supply Current		12	20	mA	V_{CC_PLL} Pin
I_{CCQ}	Maximum Quiescent Supply Current		13	20	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9658 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
3. The MPC9658 output levels are compatible to the MPC958 output levels.
4. Inputs have pull-down resistors affecting the input current.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = 0°C to 70°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{REF}	Input reference frequency PLL mode, external feedback Input reference frequency in PLL bypass mode[4]	÷ 2 feedback[2] ÷ 4 feedback[3]	100 50 0		250 125 250	MHz MHz MHz	PLL locked PLL locked
f_{VCO}	VCO lock frequency range[5]		200		500	MHz	
f_{MAX}	Output Frequency	÷ 2 feedback[3] ÷ 4 feedback[4]	100 50		250 125	MHz MHz	PLL locked PLL locked
V_{PP}	Peak-to-peak input voltage (PCLK)		500		1000	mV	LVPECL
V_{CMR}[6]	Common Mode Range (PCLK)		1.2		V_{CC} –0.9	V	LVPECL
$t_{PW,MIN}$	Input Reference Pulse Width[7]		2.0			ns	
$t_{(\varnothing)}$	Propagation Delay (static phase offset)	PCLK to FB_IN f_{REF} = 100 MHz any frequency	 –70 –125		 +80 +125	 ps ps	PLL locked
t_{PD}	Propagation Delay (PLL and divider bypass)	PCLK to Q0-9	1.0		4.0	ns	
$t_{sk(O)}$	Output-to-output Skew[8]				120	ps	
DC	Output Duty Cycle[9]		(T ÷ 2)–400	T ÷ 2	(T ÷ 2)+400	ps	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V
$t_{PLZ, HZ}$	Output Disable Time				7.0	ns	
$t_{PZL, LZ}$	Output Enable Time				6.0	ns	
$t_{JIT(CC)}$	Cycle-to-cycle jitter				80	ps	
$t_{JIT(PER)}$	Period Jitter				80	ps	
$t_{JIT(\varnothing)}$	I/O Phase Jitter f_{VCO} = 500 MHz and ÷ 2 feedback, RMS (1σ)[10] f_{VCO} = 500 MHz and ÷ 4 feedback, RMS (1σ)				5.5 6.5	ps ps	
BW	PLL closed loop bandwidth[11]	÷ 2 feedback[3] ÷ 4 feedback[5]		6 – 20 2 – 8		MHz MHz	
t_{LOCK}	Maximum PLL Lock Time				10	ms	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. ÷ 2 PLL feedback (high frequency range) requires VCO_SEL = 0, PLL_EN = 1, $\overline{\text{BYPASS}}$ = 1 and MR/$\overline{\text{OE}}$ = 0.
3. ÷ 4 PLL feedback (low frequency range) requires VCO_SEL = 1, PLL_EN = 1, $\overline{\text{BYPASS}}$ = 1 and MR/$\overline{\text{OE}}$ = 0.
4. In bypass mode, the MPC9658 divides the input reference clock.
5. The input frequency f_{REF} must match the VCO frequency range divided by the feedback divider ratio FB: $f_{REF} = f_{VCO} \div FB$.
6. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts static phase offset $t_{(\varnothing)}$.
7. Calculation of reference duty cycle limits: $DC_{REF,MIN} = t_{PW,MIN} \cdot f_{REF} \cdot 100\%$ and $DC_{REF,MAX} = 100\% – DC_{REF,MIN}$.
8. Refer to APPLICATIONS INFORMATION for part-to-part skew calculation in PLL zero-delay mode.
9. Output duty cycle is DC = (0.5 ± 400 ps · f_{OUT}) Þ 100%. For example, the DC range at f_{OUT} = 100MHz is 46% < DC < 54%. T = output period.
10. Refer to APPLICATIONS INFORMATION for a jitter calculation for other confidence factors than 1 σ and a characteristic for other VCO frequencies.
11. –3 dB point of PLL transfer characteristics.

APPLICATIONS INFORMATION

Programming the MPC9658

The MPC9658 supports output clock frequencies from 50 to 250 MHz. Two different feedback divider configurations can be used to achieve the desired frequency operation range. The feedback divider (VCO_SEL) should be used to situate the VCO in the frequency lock range between 200 and 500 MHz for stable and optimal operation. Two operating frequency ranges are supported: 50 to 125 MHz and 100 to 250 MHz. Table 7.MPC9658 Configurations (QFB connected to FB_IN) illustrates the configurations supported by the MPC9658. PLL zero-delay is supported if BYPASS = 1, PLL_EN = 1, and the input frequency is within the specified PLL reference frequency range.

Table 7. MPC9658 Configurations (QFB connected to FB_IN)

BYPASS	PLL_EN	VCO_SEL	Operation	Frequency		
				Ratio	Output range (f_{Q0-9})	VCO
0	X	X	Test mode: PLL and divider bypass	$f_{Q0-9} = f_{REF}$	0 – 250 MHz	n/a
1	0	0	Test mode: PLL bypass	$f_{Q0-9} = f_{REF} \div 2$	0 – 125 MHz	n/a
1	0	1	Test mode: PLL bypass	$f_{Q0-9} = f_{REF} \div 4$	0 – 62.5 MHz	n/a
1	1	0	PLL mode (high frequency range)	$f_{Q0-9} = f_{REF}$	100 – 250 MHz	$f_{VCO} = f_{REF} \cdot 2$
1	1	1	PLL mode (low frequency range)	$f_{Q0-9} = f_{REF}$	50 – 125 MHz	$f_{VCO} = f_{REF} \cdot 4$

Power Supply Filtering

The MPC9658 is a mixed analog/digital product. Its analog circuitry is naturally susceptible to random noise, especially if this noise is seen on the power supply pins. Random noise on the V_{CCA_PLL} power supply impacts the device characteristics, for instance I/O jitter. The MPC9658 provides separate power supplies for the output buffers (V_{CC}) and the phase-locked loop (V_{CCA_PLL}) of the device. The purpose of this design technique is to isolate the high switching noise digital outputs from the relatively sensitive internal analog phase-locked loop. In a digital system environment where it is more difficult to minimize noise on the power supplies a second level of isolation may be required. The simple but effective form of isolation is a power supply filter on the V_{CC_PLL} pin for the MPC9658. Figure 3 illustrates a typical power supply filter scheme. The MPC9658 frequency and phase stability is most susceptible to noise with spectral content in the 100 kHz to 20 MHz range. Therefore the filter should be designed to target this range. The key parameter that needs to be met in the final filter design is the DC voltage drop across the series filter resistor R_F. From the data sheet the I_{CC_PLL} current (the current sourced through the V_{CC_PLL} pin) is typically 12 mA (20 mA maximum), assuming that a minimum of 2.835 V must be maintained on the V_{CC_PLL} pin.

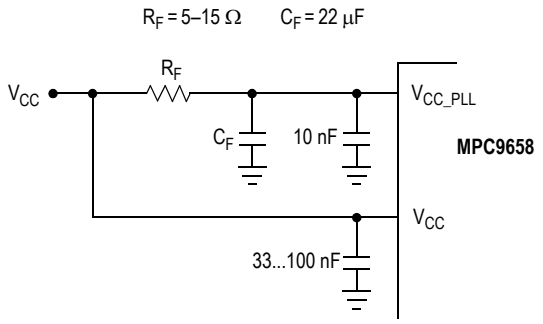


Figure 3. V_{CC_PLL} Power Supply Filter

The minimum values for R_F and the filter capacitor C_F are defined by the required filter characteristics: the RC filter should provide an attenuation greater than 40 dB for noise whose spectral content is above 100 kHz. In the example RC filter shown in Figure 3, the filter cut-off frequency is around 3 – 5 kHz and the noise attenuation at 100 kHz is better than 42 dB.

As the noise frequency crosses the series resonant point of an individual capacitor its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the bandwidth of the PLL. Although the MPC9658 has several design features to minimize the susceptibility to power supply noise (isolated power and grounds and fully differential PLL) there still may be applications in which overall performance is being degraded due to system power supply noise. The power supply filter schemes discussed in this section should be adequate to eliminate power supply noise related problems in most designs.

Using the MPC9658 in Zero-Delay Applications

Nested clock trees are typical applications for the MPC9658. Designs using the MPC9658 as LVCMOS PLL fanout buffer with zero insertion delay will show significantly lower clock skew than clock distributions developed from CMOS fanout buffers. The external feedback option of the MPC9658 clock driver allows for its use as a zero delay buffer. The PLL aligns the feedback clock output edge with the clock input reference edge resulting a near zero delay through the device (the propagation delay through the device is virtually eliminated). The maximum insertion delay of the device in zero-delay applications is measured between the reference clock input and any output. This effective delay consists of the static phase offset, I/O jitter (phase or long-term jitter), feedback path delay and the output-to-output skew error relative to the feedback output.

Calculation of Part-to-Part Skew

The MPC9658 zero delay buffer supports applications where critical clock signal timing can be maintained across several devices. If the reference clock inputs of two or more MPC9658 are connected together, the maximum overall timing uncertainty from the common PCLK input to any output is:

$$t_{SK(PP)} = t_{(\varnothing)} + t_{SK(O)} + t_{PD,\ LINE(FB)} + t_{JIT(\varnothing)} \cdot CF$$

This maximum timing uncertainty consist of four components: static phase offset, output skew, feedback board trace delay, and I/O (phase) jitter:

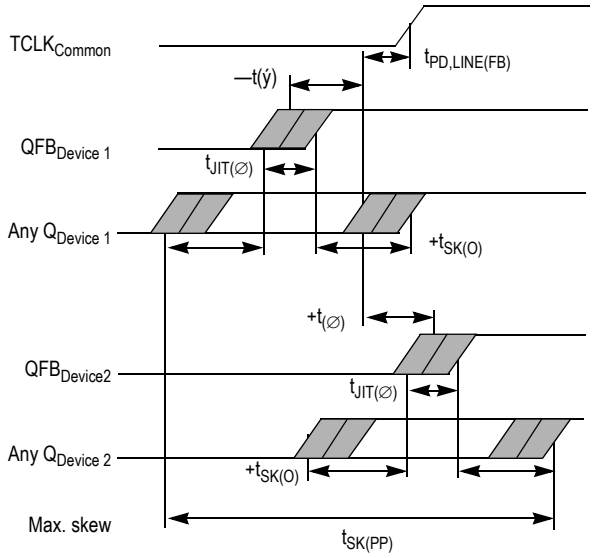


Figure 4. MPC9658 Max. Device-to-Device Skew

Due to the statistical nature of I/O jitter a RMS value (1σ) is specified. I/O jitter numbers for other confidence factors (CF) can be derived from Table 8.Confidence Factor CF.

Table 8. Confidence Factor CF

CF	Probability of clock edge within the distribution
± 1σ	0.68268948
± 2σ	0.95449988
± 3σ	0.99730007
± 4σ	0.99993663
± 5σ	0.99999943
± 6σ	0.99999999

The feedback trace delay is determined by the board layout and can be used to fine-tune the effective delay through each device. In the following example calculation a I/O jitter confidence factor of 99.7% (± 3σ) is assumed, resulting in a worst case timing uncertainty from input to any output of –214 ps to 224 ps relative to PCKL (f_{REF} = 100 MHz, FB = ³4, $t_{jit(\varnothing)}$ = 8 ps RMS at f_{VCO} = 400 MHz):

$$t_{SK(PP)} = [-70ps...80ps] + [-120ps...120ps] + [(8ps \cdot -3)...(8ps \cdot 3)] + t_{PD,\ LINE(FB)}$$

$$t_{SK(PP)} = [-214ps...224ps] + t_{PD,\ LINE(FB)}$$

Due to the frequency dependence of the I/O jitter, Figure 5 can be used for a more precise timing performance analysis.

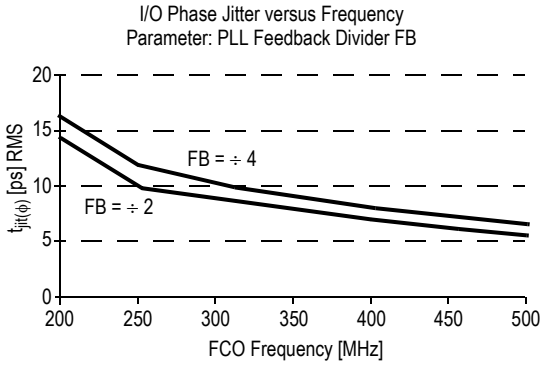


Figure 5. Max. I/O Jitter versus Frequency

Driving Transmission Lines

The MPC9658 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Motorola Application Note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC} \div 2$.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9658 clock driver. However, for the series terminated case there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 6. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9658 clock driver is effectively doubled due to its capability to drive multiple lines.

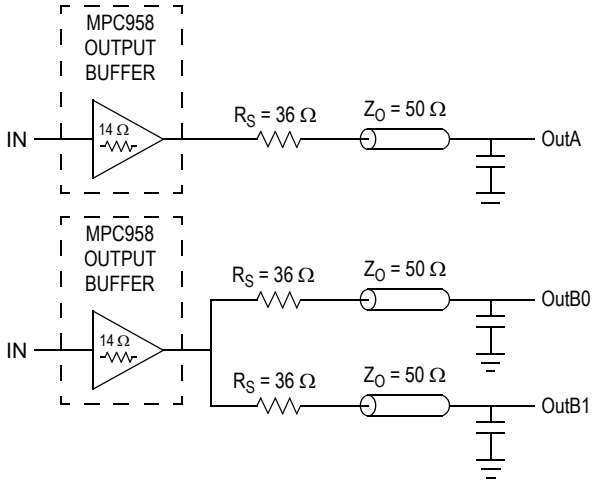


Figure 6. Single versus Dual Transmission Lines

The waveform plots in Figure 7 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9658 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9658. The output waveform in Figure 7 shows a step in the waveform. This step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$

$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$

$$R_S = 36\ \Omega \parallel 36\ \Omega$$

$$R_0 = 14\ \Omega$$

$$V_L = 3.0\ (25 \div (18+14+25)$$

$$= 1.31\ V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0ns).

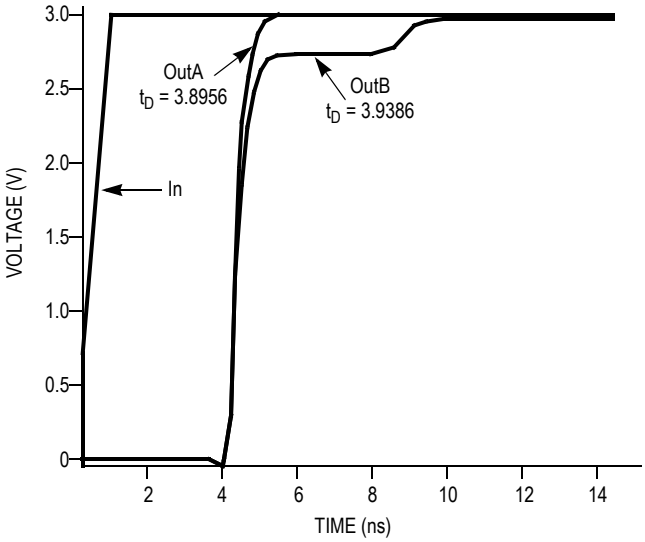
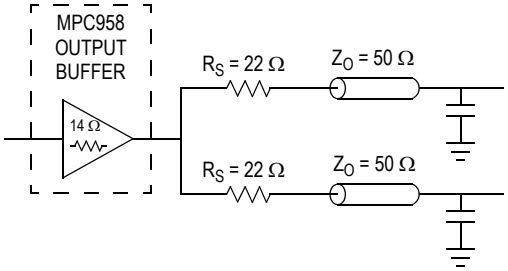


Figure 7. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering. However, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 8 should be used. In this case, the series terminating resistors are reduced such that, when the parallel combination is added to the output buffer impedance, the line impedance is perfectly matched.



$$14\ \Omega + 22\ \Omega \parallel 22\Omega = 50\ \Omega \parallel 50\ \Omega$$

$$25\ \Omega = 25\ \Omega$$

Figure 8. Optimized Dual Line Termination

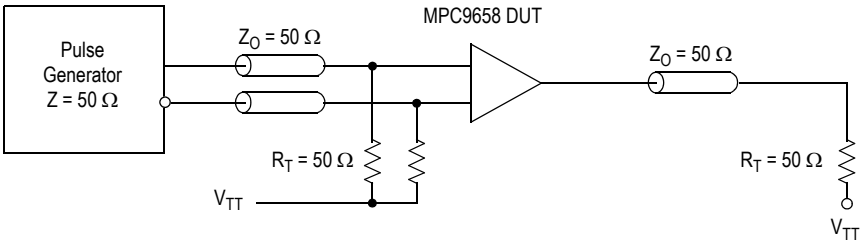
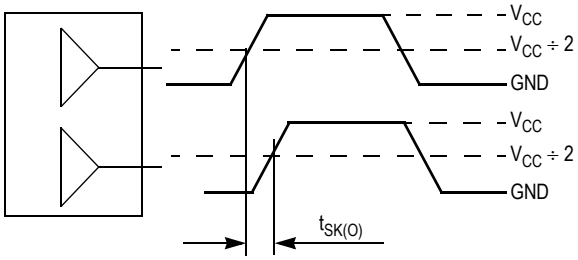


Figure 9. PCLK MPC9658 AC Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output-to-Output Skew $t_{SK(O)}$

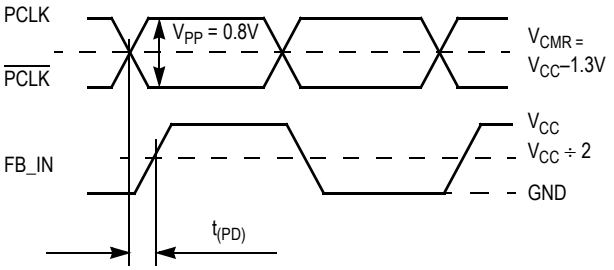
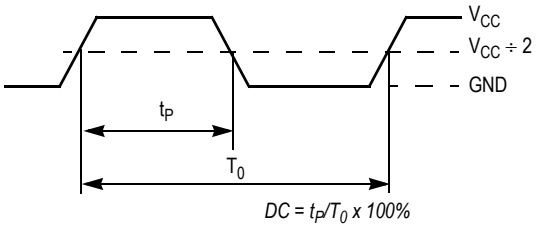
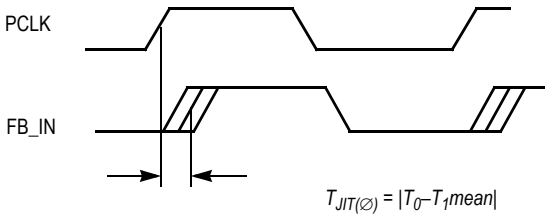


Figure 11. Propagation Delay ($t_{(PD)}$, static phase offset) Test Reference



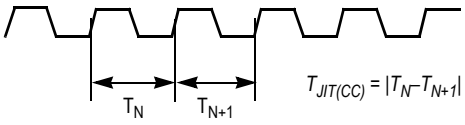
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 12. Output Duty Cycle (DC)



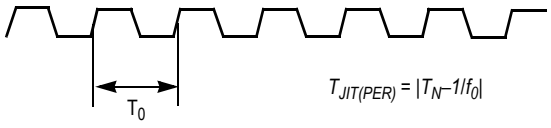
The deviation in t_0 for a controlled edge with respect to a T_0 mean in a random sample of cycles

Figure 13. I/O Jitter



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 14. Cycle-to-Cycle Jitter



The deviation in cycle time of a signal with respect to the ideal period over a random sample of cycles

Figure 15. Period Jitter

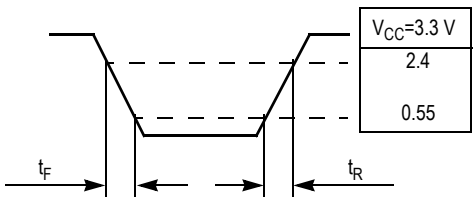


Figure 16. Output Transition Time Test Reference

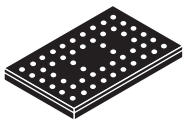
Order number: MPC96877
Rev 1, 08/2004

Product Preview

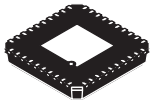
1.8 V PLL 1:10 Differential SDRAM Clock Driver

MPC96877

DDR II MEMORY
CLOCK / ZERO DELAY BUFFER



VK SUFFIX
52-BALL FP-MAPBGA PACKAGE
CASE 1544-01



EP SUFFIX
40-PIN MLF/QFN PACKAGE
CASE 1545-01

Recommended Applications

- DDR II Memory Modules
- Zero Delay Board fan-out

Features

- 1.8 V Phase Lock Loop Clock Driver for (DDR II) Applications
- Spread Spectrum Clock Compatible
- Operating Frequency: 100 MHz to 340 MHz
- 1 to 10 differential clock distribution (SSTL_18)
- 52-Ball VF-BGA (FP-MAPBGA 0.65-mm pitch) and 40-Pin MLF (QFN)
- 52-lead Pb-free Package Available
- External Feedback Pins (FBIN, $\overline{\text{FBIN}}$) are used to synchronize the Outputs to the Input Clocks
- Single-Ended Input and Single-Ended Output Modes
- Meets or Exceeds JESD82-8 PLL Standard for PC2-3200/4300
- Auto Power Down detect logic

Switching Characteristics

- Cycle-to-Cycle Jitter (>165 Mhz): 40 ps max.
- Output-to-Output Skew: 40 ps max.

AVAILABLE ORDERING OPTIONS

T_A	52-Ball BGA	40-Pin QFN
0°C to 70°C	MPC96877VK (Pb-Free)	MPC96877EP (Pb-Free)

Functional Description

The MPC96877 is a high-performance, low-jitter, low-skew, zero-delay buffer that distributes a differential clock input pair (CK, $\overline{\text{CK}}$) to ten differential pairs of clock outputs (Yn, $\overline{\text{Yn}}$) and to one differential pair of feedback clock outputs (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the input clocks (CK, $\overline{\text{CK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), the LVCMOS control pins (OE, OS), and the analog power input (AV_{DD}). When OE is low, the clock outputs, except FBOUT/$\overline{\text{FBOUT}}$, are disabled while the internal PLL continues to maintain its locked-in frequency. OS (output select) is a program pin that must be tied to GND or V_{DD}. When OS is high, OE functions as previously described. When OS and OE are both low, OE has no affect on Y7/$\overline{\text{Y7}}$, they are free running. When AV_{DD} is grounded, the PLL is turned off and bypassed for test purposes. When both clock inputs (CK, $\overline{\text{CK}}$) are logic low, the device enters in a low power mode. An input logic detection circuit on the differential inputs, independent from input buffers, detects the logic low level and performs in a low power state where all outputs, the feedback, and the PLL are off. When the clock inputs transition from being logic low to being differential signals, the PLL turns back on, the inputs and the outputs are enabled, and the PLL obtains phase lock between the feedback clock pair (FBIN, $\overline{\text{FBIN}}$) and the clock input pair (CK, $\overline{\text{CK}}$) within the specified stabilization time.

The MPC96877 is able to track spread spectrum clocking (SSC) for reduced EMI. This device operates from 0°C to 70°C.

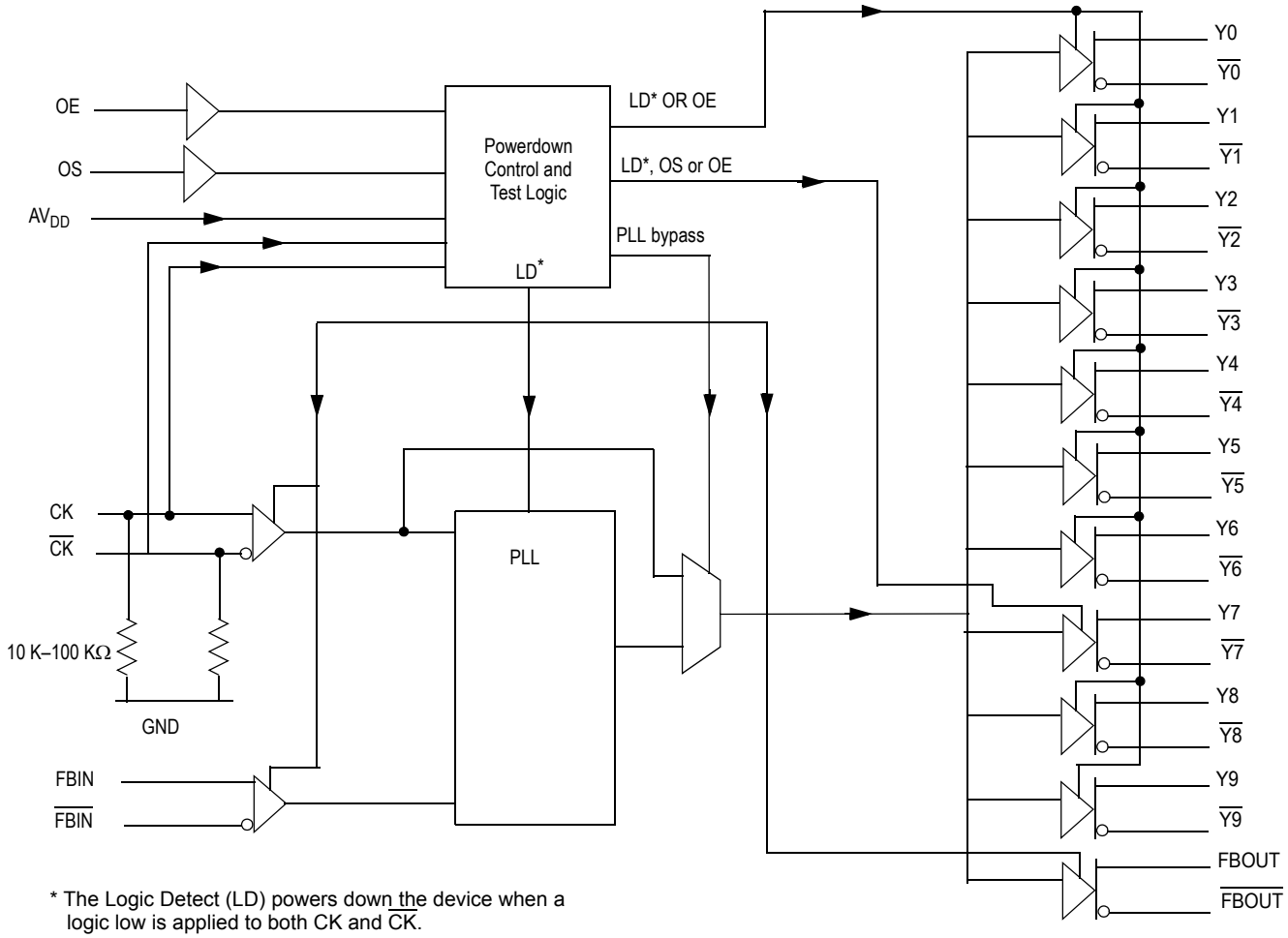
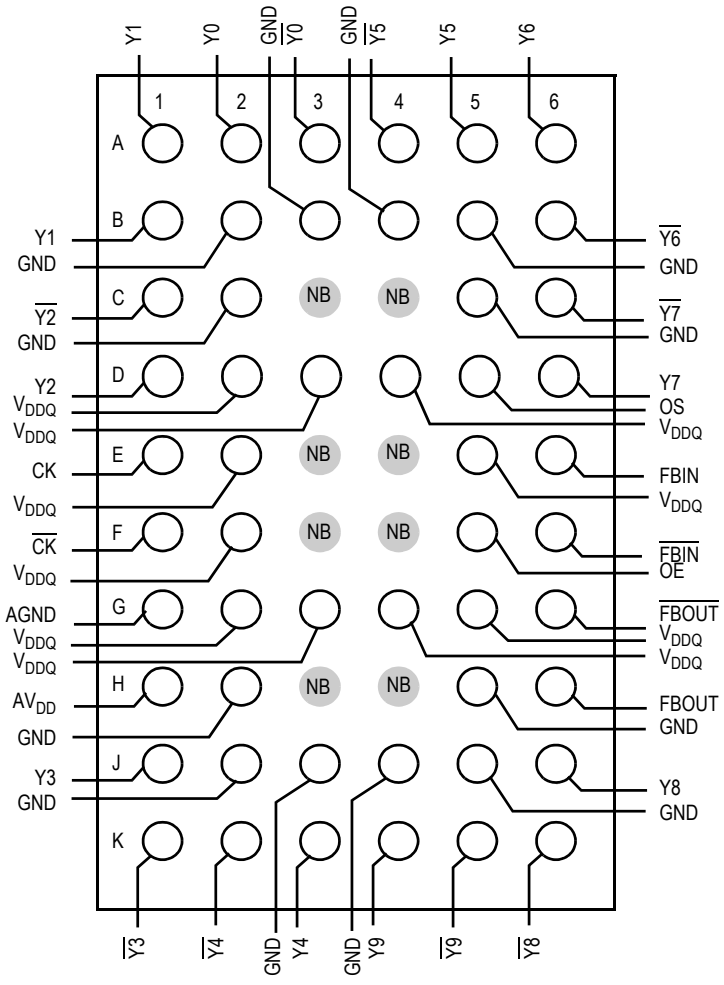
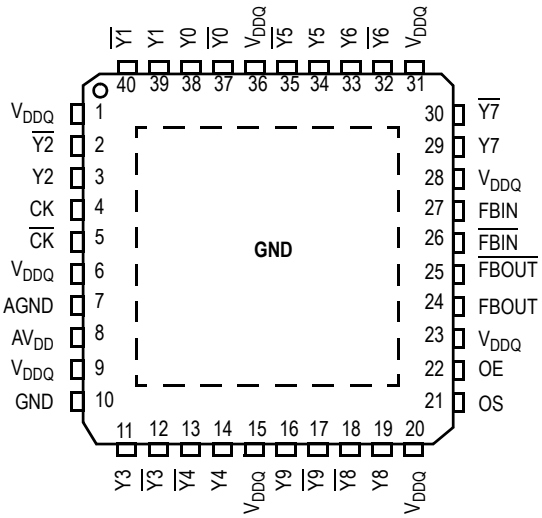


Figure 1. MPC96877 Logic Diagram

VF-MAPBGA (VK) PACKAGE



EP PACKAGE
(TOP VIEW)



40-Pin TE-QFN(6.0 x 6.0 mm Body Size,
0.5 mm Pitch, M0#220, Variation VJJD-2,
E2 = D2 = 2.9 mm ±0.15 mm) Package Pinouts

Table 1. Pin Configuration

Pin	BGA	MLF	I/O	Function
AGND	G1	7		Analog ground
AV_{DD}	H1	8		Analog power
CK	E1	4	Input	Clock input with a (10k to 100k) pulldown resistor
$\overline{CK}$	E6	5	Input	Complimentary clock input with a (10k to 100k) pulldown resistor
FBIN	F6	27	Input	Feedback clock input
$\overline{FBIN}$		26	Input	Complimentary Feedback clock input
FBOUT	H6	24	Output	Feedback clock output
$\overline{FBOUT}$	G6	25	Output	Complimentary feeback clock output
OE	F5	22	Input	Output Enable (asynchronous)
OS	D5	21	Input	Output Select (tied to GND or V_{DD})
GND	B2, B3, B4, B5, C2,C5,H2,H5, J2, J3, J4, J5	10		Ground
V_{DDQ}	D2, D3, D4, E2, E5, F2, G2, G3, G4, G5	1, 6, 9, 15, 20, 23, 28, 31, 36		Logic and output power
Y[0:9]	A2, A1, D1, J1, K3, A5, A6, D6, J6, K4	38, 39, 3, 11, 14, 34, 33, 29,19, 16	Output	Clock outputs
Y[0:9]	A3, B1, C1, K1, K2, A4, B6, C6, K6, K5	37, 40, 2, 12, 13, 35, 32, 30, 18, 17	Output	Complimentary clock outputs

Table 2. Function Table

Inputs					Outputs				PLL
AV_{DD}	OE	OS	CK	$\overline{CK}$	Y	Y	FBOUT	$\overline{FBOUT}$	
GND	H	X	L	H	L	H	L	H	Bypassed / OFF
GND	H	X	H	L	H	L	H	L	Bypassed / OFF
GND	L	H	L	H	L_Z	L_Z	L	H	Bypassed / OFF
GND	L	L	H	L	L_Z[1] Y7 Active	L_Z[1] $\overline{Y7}$ Active	H	L	Bypassed / OFF
1.8 V Nominal	L	H	L	H	L_Z[1]	L_Z[1]	L	H	ON
1.8 V Nominal	L	L	H	L	L_Z[1] Y7 Active	L_Z[1] $\overline{Y7}$ Active	H	L	ON
1.8 V Nominal	H	X	L	H	L	H	L	H	ON
1.8 V Nominal	H	X	H	L	H	L	H	L	ON
1.8 V Nominal	X	X	L	L	L_Z[1]	L_Z[1]	L_Z[1]	L_Z[1]	OFF
X	X	X	H	H	RESERVED				

1. $L_{(Z)}$ means the outputs are disabled to a low state meeting the I_{ODL} limit in Table 5.

Table 3. Absolute Maximum Ratings Over Free-Air Operating Range[1]

Parameter	Value
Supply voltage range, V_{DDQ} or AV_{DD}	–0.5 V to 2.5 V
Input voltage range, V_I[2, 3]	–0.5 V to V_{DDQ} + 0.5 V
Output voltage range, V_O[1, 2]	–0.5 V to V_{DDQ} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{DDQ})	±50 mA
Output clamp voltage, I_{OK} (V_O < 0 or V_O > V_{DDQ})	±50 mA
Continuous output current, IO (V_O = 0 to V_{DDQ})	±50 mA
Continuous current through each V_{DDQ} or GND	±100 mA
Storage temperature range, T_{STG}	–65°C to 150°C

1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 2.5 V maximum.

Table 4. Recommended Operating Conditions

Rating	Parameter	Affected Pins	Min	Nom	Max	Unit
Output supply voltage	V_{DDQ}		1.7	1.8	1.9	V
Supply voltage[1]	AV_{DD}			V_{DDQ}		
Low-level input voltage[2]	V_{IL}	OE, OS, CK, $\overline{CK}$			0.35 x V_{DDQ}	V
High-level input voltage[2]	V_{IH}	OE, OS, CK, $\overline{CK}$	0.65 x V_{DDQ}			
High-level output current	I_{OH}				–9	mA
Low-level output current	I_{OL}				9	mA
Input differential-pair cross voltage	V_{IX}		(V_{DDQ}/2) –0.15		(V_{DDQ}/2) +0.15	V
Input voltage level	V_{IN}		–0.3		V_{DDQ} +0.3	
Input differential-pair voltage[2] (see Figure 9. Half-Period Jitter)	V_{ID}	DC	0.3		V_{DDQ} +0.4	
		AC	0.6		V_{DDQ} +0.4	
Operating free-air temperature			0		70	°C

1. The PLL is turned off and bypassed for test purposes when AV_{DD} is grounded. During this test mode, V_{DDQ} remains within the recommended operating conditions and not timing parameters are guaranteed.
2. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$, see Figure 12. Time Delay between OE and Clock Output for definition. For CK and $\overline{CK}$ the V_{IH} and V_{IL} limits are used to define the DC low and high levels for the logic detect state.

Table 5. Electrical Characteristics Over Recommended Free-Air Operating Temperature Range

Description	Parameter	Affected Pins	Test Conditions	AV_{DD}, V_{DDQ}	Min	Max	Unit
All inputs	V_{IK}		I_I = –18mA	1.7 V		–1.2	V
High output voltage	V_{OH}		I_{OH} = –100 μA	1.7 to 1.9 V	V_{DDQ} –0.2		V
			I_{OH} = –9 mA	1.7 V	1.1		
Low output voltage	V_{OL}		I_{OL} = 100 μA	1.7 to 1.9 V		0.1	V
			I_{OL} = 9 mA	1.7 V		0.6	
Output disable current	I_{ODL}		OE = L, V_{ODL} = 100 mV	1.7 V	100		μA
Output differential voltage	V_{OD}			1.7 V	0.5		V
Input leakage current	I_I	CK, $\overline{CK}$	V_I = V_{DDQ} or GND	1.9 V		± 250	μA
		OE, OS, FBIN, $\overline{FBIN}$	V_I = V_{DDQ} or GND	1.9 V		± 10	
Static supply current I_{DDQ} + I_{ADD}	I_{DDLD}		CK and $\overline{CK}$ = L	1.9 V		500	μA
Dynamic Supply current I_{DDQ} + $I_{ADD,}$ see Note 1 for CPD calculation	I_{DD}		CK and $\overline{CK}$ = 270 MHz all outputs open	1.9 V		300	mA

1. Total I_{DD} = I_{DDQ} + I_{ADD} = F_{CK}* C_{PD} * V_{DDQ}, solving for C_{PD} = (I_{DDQ} + I_{ADD})/(F_{CK} * V_{DDQ}) where F_{CK} is the input Frequency, V_{DDQ} is the power supply and C_{PD} is the Power Dissipation Capacitance.

Table 6. Timing Requirements Over Recommended Free-Air Operating Temperature Range

Timing Requirements	AV_{DD}, V_{DDQ} = 1.8 V ± 0.1 V		Unit
	Min	Max	
Operating clock frequency[1, 2]	125	340	MHz
Application clock frequency[1, 3]	160	340	MHz
Input clock duty cycle	40	60	%
Stabilization time[4]		15	μs

1. The PLL must be able to handle spread spectrum induced skew.
2. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters. (Used for low speed system debug.)
3. Application clock frequency indicates a range over which the PLL must meet all timing parameters.
4. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up. During normal operation, the stabilization time is also the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal when CK and $\overline{CK}$ go to a logic low state, enter the power-down mode and later return to active operation. CK and $\overline{CK}$ may be left floating after they have been driven low for one complete clock cycle.

Table 7. Switching Characteristics over Recommended Free-Air Operating Temperature Range Unless Otherwise Noted (see Notes)

Description	Parameter	Diagram	AV_{DD}, V_{DDQ} = 1.8 V ± 0.1 V			Unit
			Min	Nom	Max	
OE to any Y/$\overline{Y}$	ten	see Figure 11			8	ns
OE to any Y/$\overline{Y}$	tdis	see Figure 11			8	ns
Cycle-to-Cycle period jitter	tjit(cc+)	see Figure 4	0		40	ps
	tjit(cc–)		0		–40	ps
Static phase offset	t(φ)	see Figure 5	–50		50	ps
Dynamic phase offset	t(φ)dyn	see Figure 10	–50		50	ps
Output clock skew	tsk(o)	see Figure 6			40	ps
Period Jitter	tjit(per)	see Figure 7	–40		40	ps
Half -period jitter	tjit(hper)	see Figure 8	–75		75	ps
Output Enable	slr(i)	see Figure 3 and Figure 9	0.5			V/ns
Input clock slew rate, measured single ended			1	2.5	4	
Output clock slew rate, measured single ended	slr(o)	see Figure 3 and Figure 9	1.5	2.5	3	V/ns
Output differential-pair cross voltage	V_{OX}	see Figure 2	(V_{DDQ}/2) – 0.1		(V_{DDQ}/2) + 0.1	V
SSC modulation frequency			30		33	kHz
SSC clock input frequency deviation			0.0		–0.5	
PLL Loop bandwidth (–3dB from unity gain)			2.0			MHz

NOTES:

1. There are two different terminations that are used with the following tests. The loadboard in Figure 2. IBIS Model Output Load is used to measure the input and output differential-pair cross voltage only. The loadboard in Figure 3. Output Load Test Circuit 1 is used to measure all other tests. For consistency, equal length cables must be used.
2. Static Phase offset does not include Jitter.
3. Period Jitter and Half-Period Jitter specifications are separate specifications that must be met independently of each other.
4. The Output Slew Rate is determined form the IBIS model into the load shown in Figure 4. Output Load Test Circuit 2. It is measured single ended.
5. To eliminate the impact of input slew rates on static phase offset, the input slew rates of Reference Clock Input CK, $\overline{CK}$ and Feedback Clock Input FBIN, $\overline{FBIN}$ are recommended to be nearly equal. The 2.5 V/ns slew rates are shown as a recommended target. Compliance with these Nom values is not mandatory if it can be adequately demonstrated that alternative characteristics meet the requirements of the registered DDR2 DIMM application.

TEST CIRCUIT AND SWITCHING WAVEFORMS

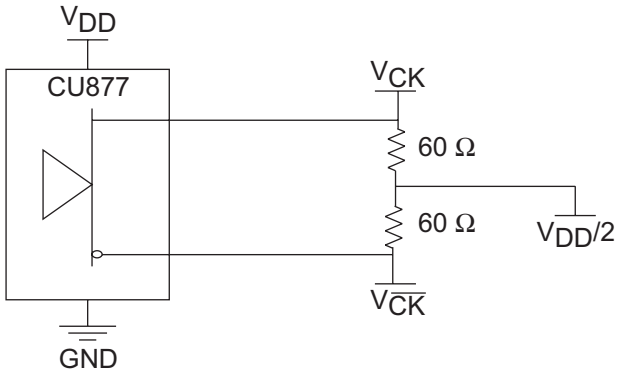


Figure 2. IBIS Model Output Load

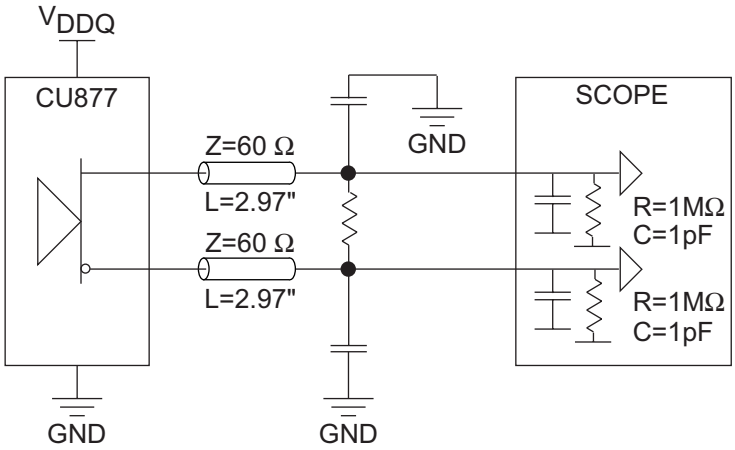


Figure 3. Output Load Test Circuit 1

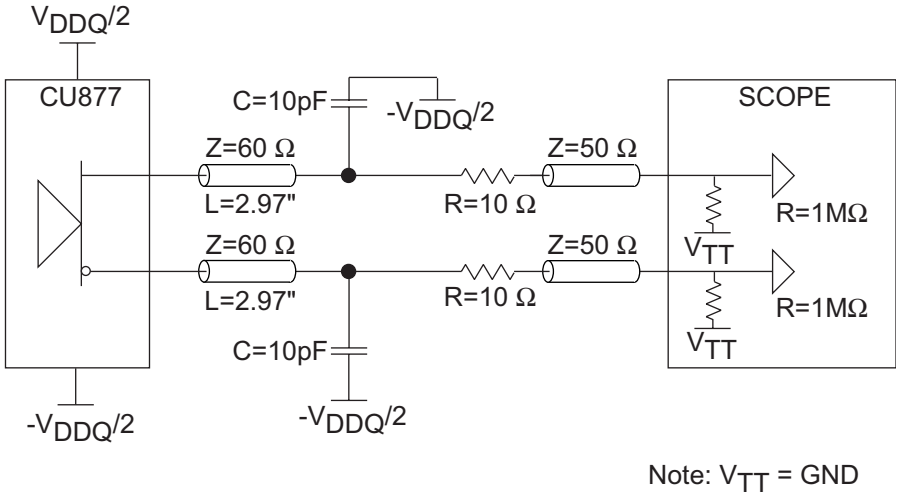
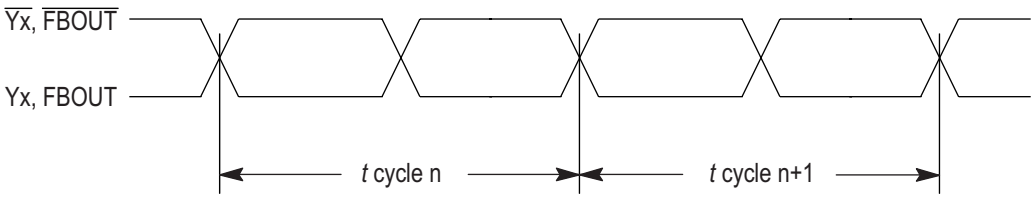


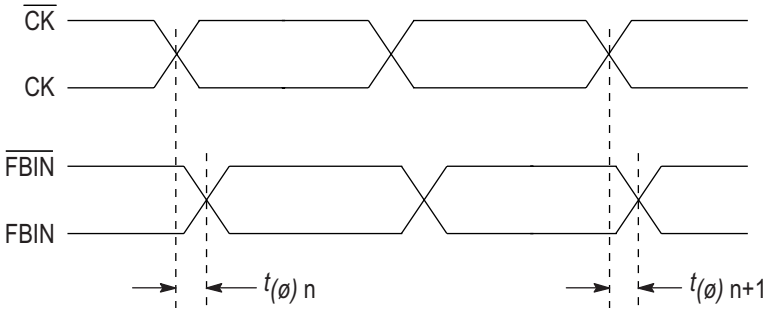
Figure 4. Output Load Test Circuit 2

TEST CIRCUIT AND SWITCHING WAVEFORMS (Continued)



$$t_{jit(cc)} = t \text{ cycle n} - t \text{ cycle n+1}$$

Figure 5. Cycle-to-Cycle Period Jitter



$$t_{(ø)} = \frac{\sum_{1}^{n=N} t_{(ø)\,n}}{N} \quad \text{(N is a large number of samples)}$$

Figure 6. Static Phase Offset

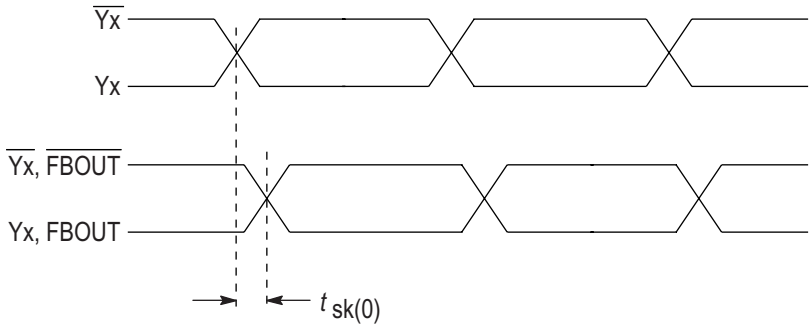


Figure 7. Output Skew

TEST CIRCUIT AND SWITCHING WAVEFORMS (Continued)

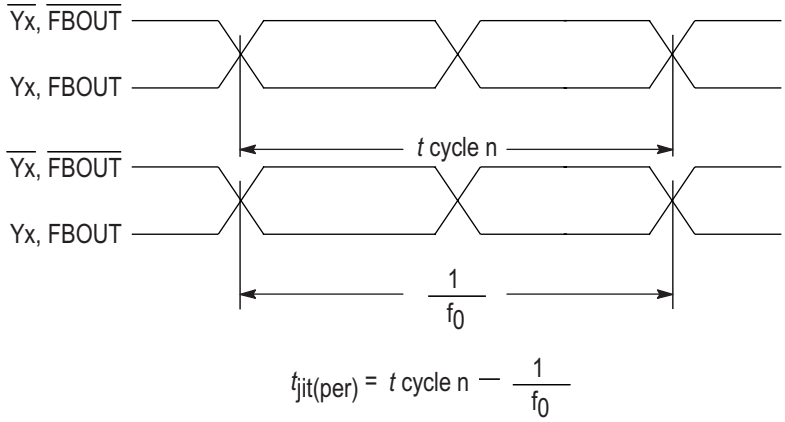


Figure 8. Period Jitter

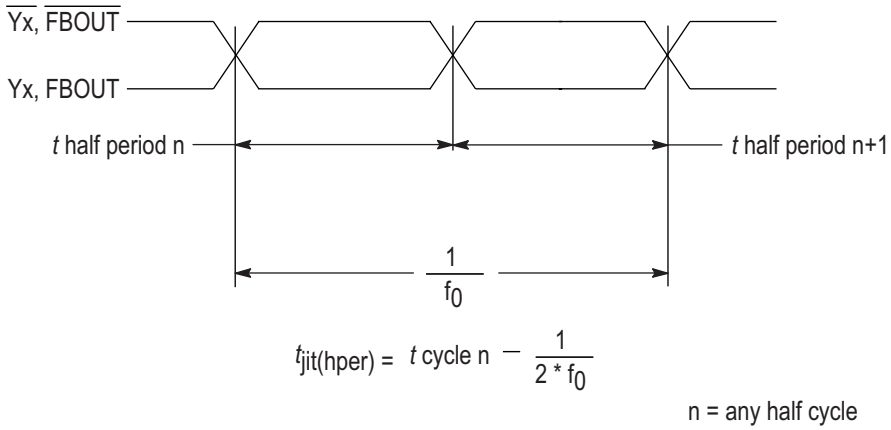


Figure 9. Half-Period Jitter

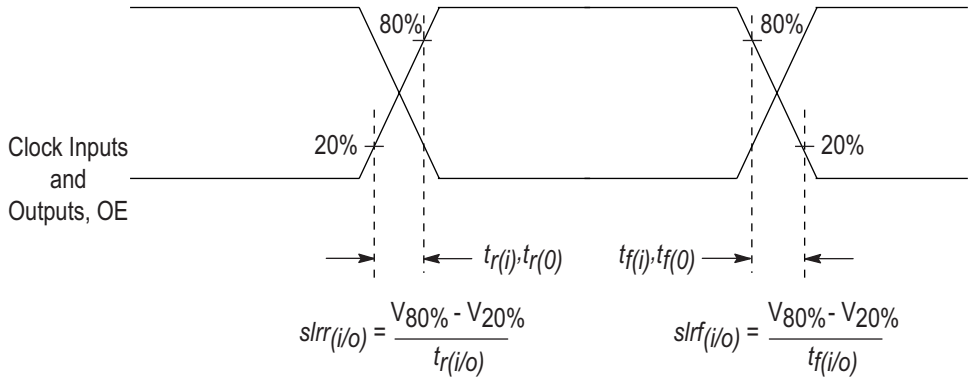


Figure 10. Input and Output Slew Rates

TEST CIRCUIT AND SWITCHING WAVEFORMS (Continued)

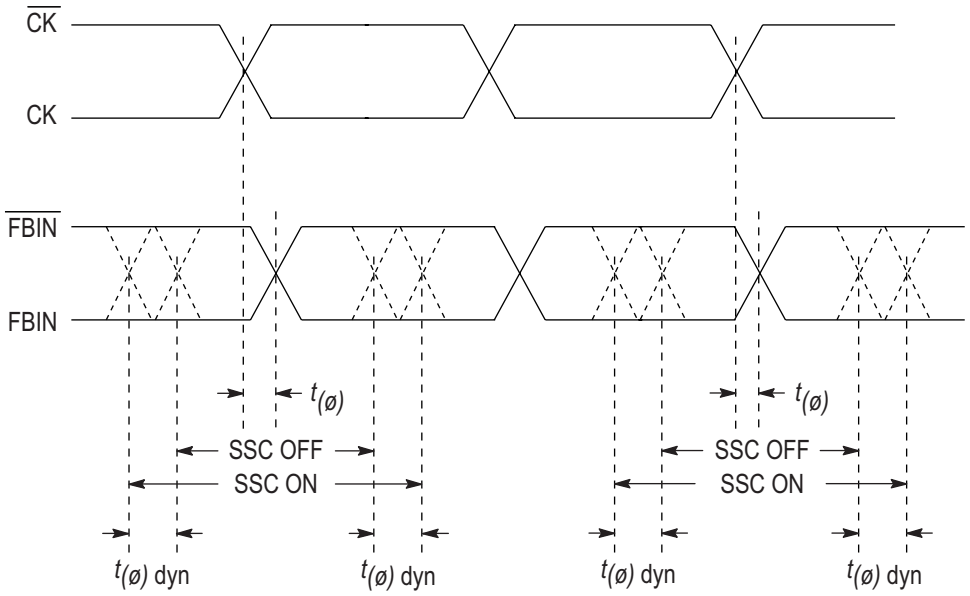


Figure 11. Dynamic Phase Offset

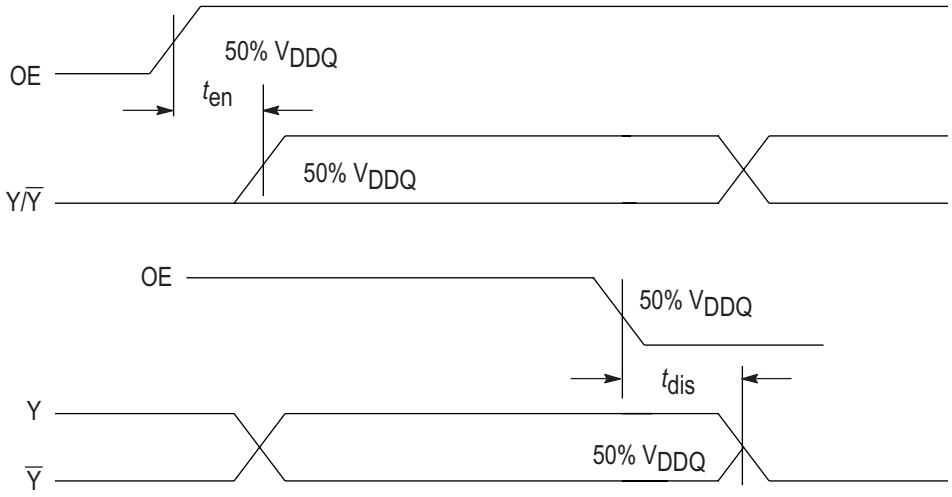
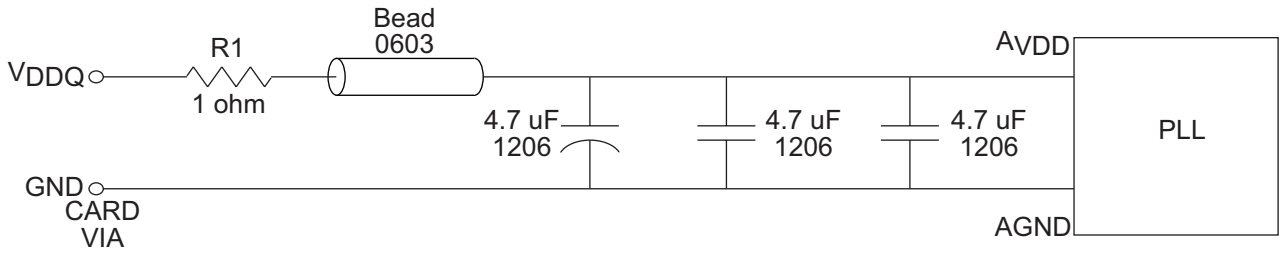


Figure 12. Time Delay between OE and Clock Output

RECOMMENDED FILTERING FOR THE ANALOG POWER SUPPLY (AV_{DD})



NOTES:

1. Place the 2200pF capacitor close to the PLL
2. Use a wide trace for the PLL analog power and ground. Connect PLL and caps to AGND to AGND trace & connect trace to one GND via (farthest from PLL).
3. Recommended bead: Fair Rite P/N 2506036017Y0 or equivalent (0.8 Ohm DC max, 600 Ohms @ 100 MHz)

Figure 13. AV_{DD} Filtering

Chapter Seven
LVCMOS Fanout Buffer Data Sheets

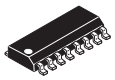
LVCMOS Fanout Buffer Device Index

Order number: MPC905
Rev 2, 05/2003

1:6 PCI Clock Generator/ Fanout Buffer

MPC905

1:6 PCI CLOCK GENERATOR/ FANOUT BUFFER



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B-05

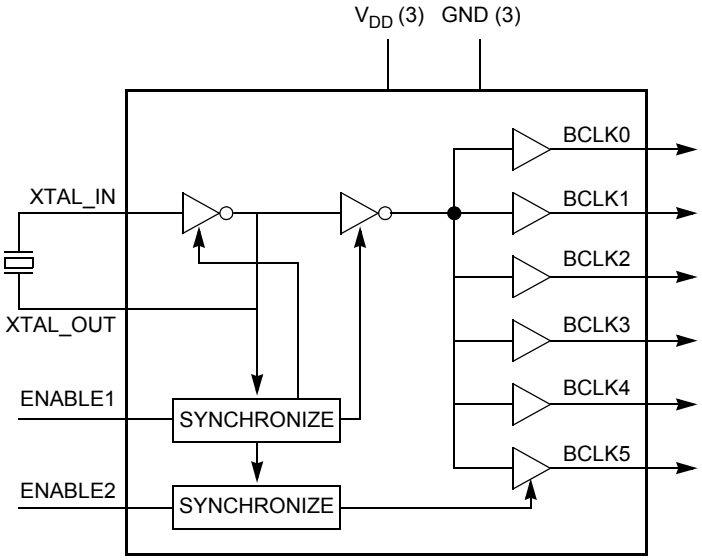
The MPC905 is a six output clock generation device targeted to provide the clocks required in a 3.3V or 5.0V PCI environment. The device operates from a 3.3V supply and can interface to either a TTL input or an external crystal. The inputs to the device can be driven with 5.0V when the V_{CC} is at 3.3V. The outputs of the MPC905 meet all of the specifications of the PCI standard.

- Six Low Skew Outputs
- Synchronous Output Enables for Power Management
- Low Voltage Operation
- XTAL Oscillator Interface
- 16-Lead SOIC Package
- 5.0V Tolerant Enable Inputs

The MPC905 device is targeted for PCI bus or processor bus environments with up to 12 clock loads. Each of the six outputs on the MPC905 can drive two series terminated 50Ω transmission lines. This capability effectively makes the MPC905 a 1:12 fanout buffer.

The MPC905 offers two synchronous enable inputs to allow users flexibility in developing power management features for their designs. Both enable signals are active HIGH inputs. A logic ‘0’ on the ENABLE1 will pull outputs 0 to 4 into the logic ‘0’ state. A logic ‘1’ on the ENABLE1 input will result in outputs 0 to 4 to be toggling. A logic ‘0’ on ENABLE2 will cause output BLK5 to a logic ‘0’ state, whereas a logic ‘1’ on ENABLE2 will cause output BLK5 to toggle. The oscillator remains on.

The ENABLE2 input can be used to disable any high power device for system power savings during periods of inactivity. Both enable inputs are synchronized internal to the chip so that the output disabling will happen only when the outputs are already LOW. This feature guarantees no runt pulses will be generated during enabling and disabling.



Pinout: 16-Lead Plastic Package (Top View)

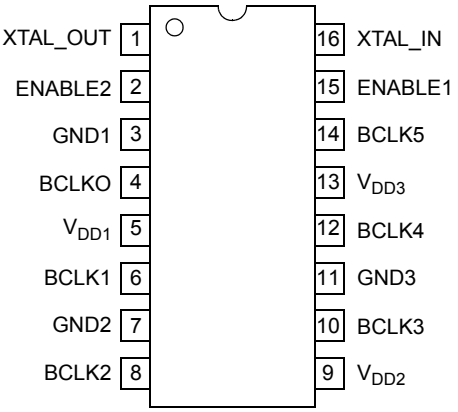


Table 1. Pin Configurations

Pin	I/O	Type	Function
XTAL_IN, XTAL_OUT	Input	Analog	Crystal Oscillator Terminals
ENABLE1, ENABLE2	Input	LVCMOS	Output Enable
BCLK0–BCLK5	Output	LVCMOS	Clock Outputs
V_{DD}		Supply	Positive Power Supply
GND		Supply	Negative Power Supply

Table 2. Function Table

ENABLE1	ENABLE2	Outputs 0 to 4	Output 5	OSC (On/Off)
0	0	Low	Low	ON
0	1	Low	Toggling	ON
1	0	Toggling	Low	ON
1	1	Toggling	Toggling	ON

Table 3. Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage	–0.5	4.6	V
V_{IN}	Input Voltage	–0.5	V_{CC} + 0.5	V
T_{oper}	Operating Temperature Range	0	+70	°C
T_{stg}	Storage Temperature Range	–65	+150	°C
T_{sol}	Soldering Temperature Range (10 Sec)		+260	°C
T_j	Junction Temperature Range		+125	°C
ESD	Static Discharge Voltage	1500		V
I_{Latch}	Latch Up Current	50		mA

1. Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

Table 4. Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Temperature Range	0	70	°C
V_{CC}	Positive Supply Voltage (Functional Range)	3.0	3.6	V
t_{DC}in	T_{high} (at XTAL_IN Input) T_{low} (at XTAL_IN Input)	0.44T[1] 0.44T[1]	0.56T[1] 0.56T[1]	T = Period

1. When using External Source for reference, requirement to meet PCI clock duty cycle requirement on the output.

Table 5. DC Characteristics (T_A = 0–70°C; V_{DD} = 3.3 V ± 0.3 V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	High Level Input Voltage		2.0		5.5[2]	V	
V_{IL}	Low Level Input Voltage				0.8	V	
V_{OH}	High Level Output Voltage		2.4			V	I_{OH} = –36mA[1]
V_{OL}	Low Level Output Voltage				0.4	V	I_{OL} = 36mA[1]
I_{IH}	Input High Current				2.5[2]	µA	
I_{IL}	Input Low Current				2.5	µA	
I_{CC}	Power Supply Current	DC 33MHz 66MHz		20 37 78	 45 95	µA mA mA	
C_{IN}	Input Capacitance	XTAL_IN Others			9.0 4.5	pF	

1. The MPC905 can drive 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to $V_{TT} = V_{CC}/2$. Alternately, the device drives up to two 50Ω series terminated transmission lines per output.
2. XTAL_IN input will sink up to 10mA when driven to 5.5V. There are no reliability concerns associated with the condition. Note that the ENABLE1 input must be a logic HIGH. Do not take the ENABLE1 input to a logic LOW with >V_{CC} volts on the XTAL_IN input.

Table 6. AC CHARACTERISTICS (T_A = 0–70°C; V_{DD} = 3.3V ± 0.3 V)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Operating Frequency	Using External Crystal Using External Clock Source	— DC		50 100	MHz	
t_{pw}	Output Pulse Width	HIGH (Above 2.0V) LOW (Below 0.8V) HIGH (Above 2.0V) LOW (Below 0.8V)	0.40T[1] 0.40T[1] 0.45T[2] 0.45T[2]		0.60T[1] 0.60T[1] 0.55T[2] 0.55T[2]		T = Periods
t_{per}	Output Period		T - 400ps				T = Desired Period
t_{os}	Output-to-Output Skew	Rising Edges Falling Edges			400 500	ps	
t_r, t_f	Rise/Fall Times (Slew Rate)		1		4	V/ns	Series Terminated Transmission Lines
t_{EN}	Enable Time	ENABLE1 ENABLE2			5 4	ms Cycles	
t_{DIS}	Disable Time	ENABLE1 ENABLE2			4 4	Cycles	
A_{osc}	XTAL_IN to XTAL_OUT Oscillator Gain		6			db	
Phase	Loop Phase Shift Modulo 360° +		30			Degrees	

1. Assuming input duty cycle specs from Recommended Operating Conditions table are met.
2. Assuming external crystal or 50% duty cycle external reference is used.

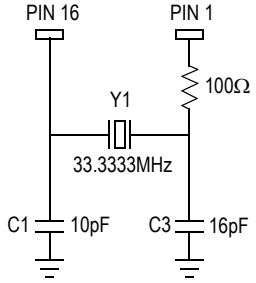


Figure 1. Crystal Oscillator Interface
(Fundamental)

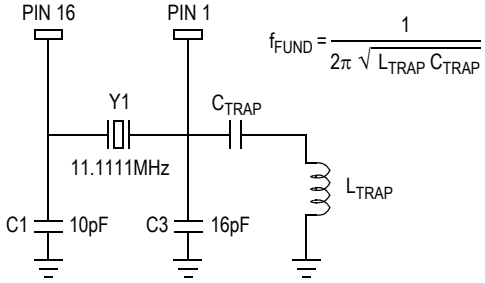


Figure 2. Crystal Oscillator Interface
(3rd Overtone)

Table 7. Crystal Specifications

Parameter	Value
Crystal Cut	Fundamental AT Cut
Resonance	Parallel Resonance
Frequency Tolerance	±75ppm at 25°C
Frequency/Temperature Stability	±150pm 0 to 70°C
Operating Range	0 to 70°C
Shunt Capacitance	5-7pF
Equivalent Series Resistance (ESR)	50 to 80Ω
Correlation Drive Level	100μW
Aging	5ppm/Yr (First 3 Years)

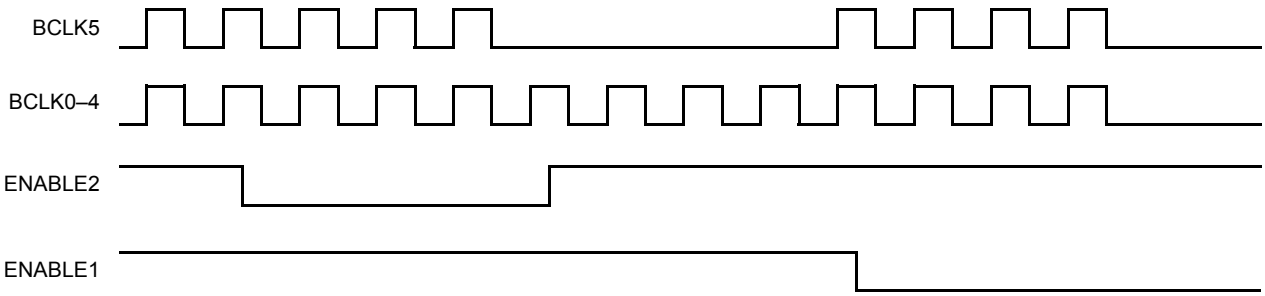


Figure 3. Enable Timing Diagram

APPLICATIONS INFORMATION

DRIVING TRANSMISSION LINES

The MPC905 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of approximately 10Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to $V_{CC}/2$. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC905 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC905 clock driver is effectively doubled due to its capability to drive multiple lines.

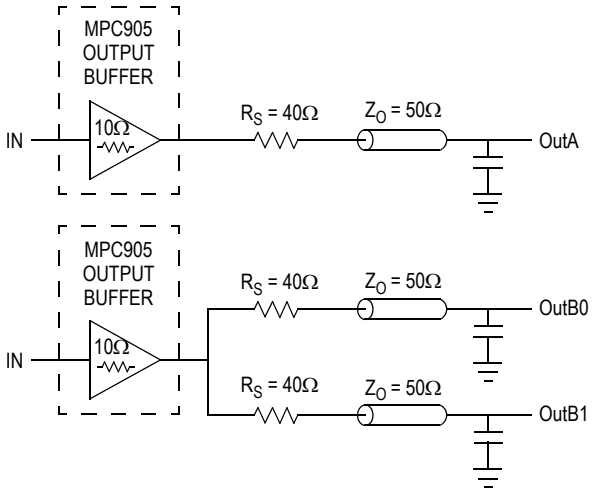


Figure 4. Single versus Dual Transmission Lines

The waveform plots of Figure 5 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC905 output buffers is more than sufficient to drive 50Ω transmission lines on the incident edge.

Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. The output waveform in Figure 5 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 40Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS (Zo / Rs + Ro + Zo) = 3.0 (25/55) = 1.36V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.73V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

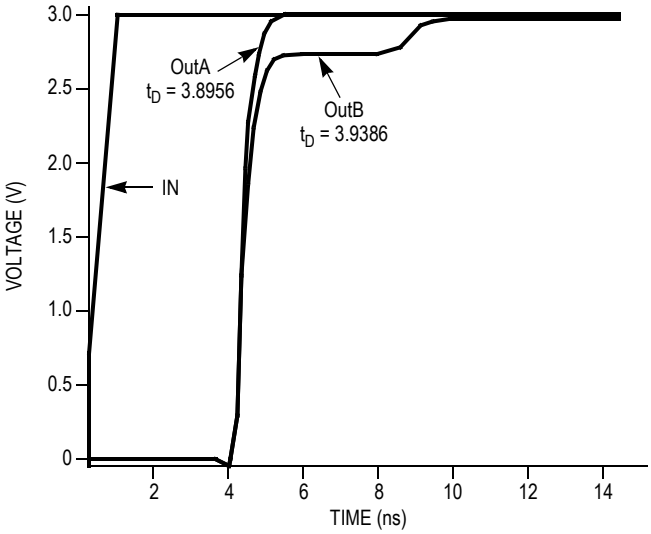
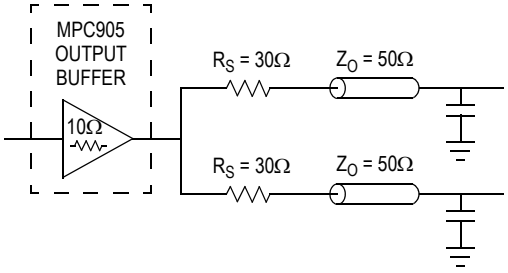


Figure 5. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 6 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



10Ω + 30Ω || 30Ω = 50Ω ||50Ω
25Ω = 25Ω

Figure 6. Optimized Dual Line Termination

Low Voltage 1:18 Clock Distribution Chip

MPC9109

LOW VOLTAGE 1:18 CLOCK DISTRIBUTION CHIP

FA SUFFIX
32-LEAD QFP PACKAGE
CASE 873A-03

The MPC9109 is a 1:18 low voltage clock distribution chip with 2.5 V or 3.3 V LVCMOS output capabilities. The device features the capability to select either a differential LVPECL or an LVCMOS compatible input. The 18 outputs are 2.5 V or 3.3 V LVCMOS compatible and feature the drive strength to drive 50 Ω series or parallel terminated transmission lines. With output-to-output skews of 200 ps, the MPC9109 is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5 V outputs also make the device ideal for supplying clocks for a high performance Pentium II™ microprocessor based design. For a higher performance version of the 9109 refer to the MPC940L data sheet.

Features

- LVPECL or LVCMOS clock input
- 2.5 V LVCMOS outputs for Pentium II microprocessor support
- 200 ps maximum output-to-output skew @ 3.3 V output
- Maximum output frequency of 250 MHz @ 3.3 V core
- 32-lead QFP packaging
- Dual or single supply device:
  - Dual V_{CC} supply voltage, 3.3 V core and 2.5 V output
  - Single 3.3 V V_{CC} supply voltage for 3.3 V outputs
  - Single 2.5 V V_{CC} supply voltage for 2.5 V I/O

Functional Description

With a low output impedance (≈20 Ω), in both the HIGH and LOW logic states, the output buffers of the MPC9109 are ideal for driving series terminated transmission lines. With a 20 Ω output impedance the 9109 has the capability of driving two series terminated lines from each output. This gives the device an effective fanout of 1:36. If a lower output impedance is desired please see the MPC942 data sheet. If better performance is desired please see the MPC940L data sheet.

The differential LVPECL inputs of the MPC9109 allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the LVCMOS level clock input. All inputs of the MPC9109 have internal pullup/pulldown resistor so they can be left open if unused.

The MPC9109 is a single or dual supply device. The device power supply offers a high degree of flexibility. The device can operate with a 3.3 V core and 3.3 V output, a 3.3 V core and 2.5 V outputs as well as a 2.5 V core and 2.5 V outputs. The 32-lead QFP package was chosen to optimize performance, board space and cost of the device. The 32-lead TQFP has a 7x7mm body size with a conservative 0.8 mm pin spacing.

Pentium II is a trademark of Intel Corporation.

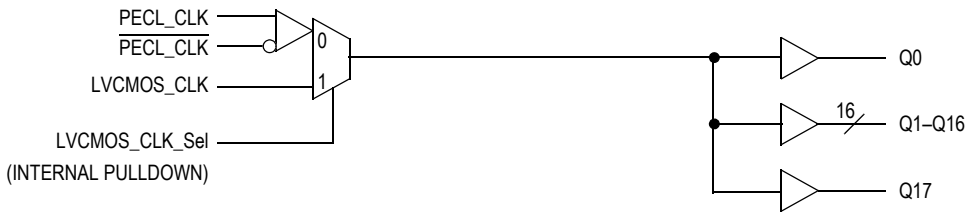


Figure 1. Logic Diagram

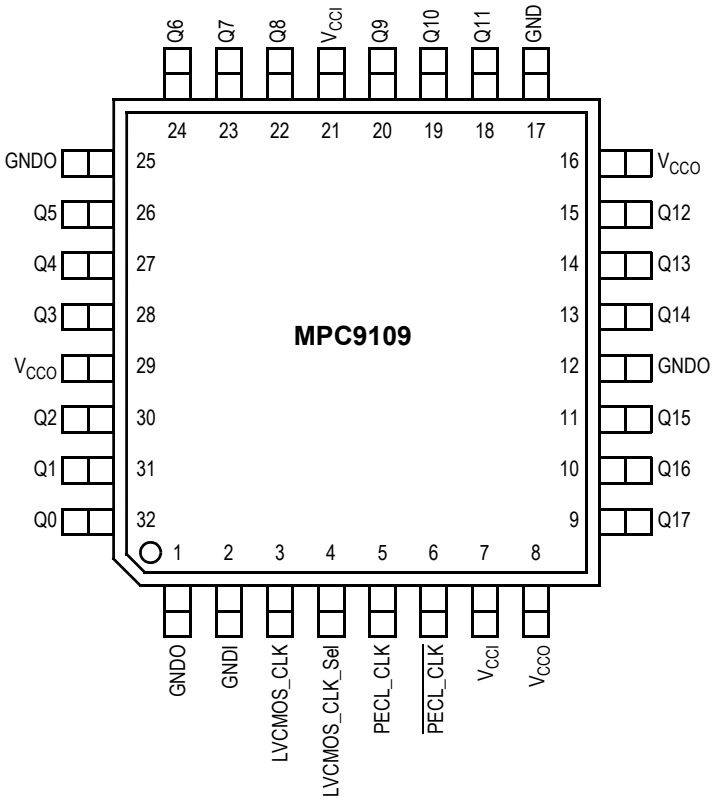


Figure 2. Pinout: 32-Lead TQFP (Top View)

Table 1. Function Table

LVCMOS CLK_Sel	Input
0	PECL_CLK
1	LVCMOS_CLK

Table 2. Power Supply Voltages

Supply Pin	Voltage Level
V_{CCI}	2.5 V or 3.3 V ± 5%
V_{CCO}	2.5 V or 3.3 V ± 5%

Table 3. Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 4. DC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3 V ± 5%; V_{CCO} = 3.3 V ± 5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	CMOS_CLK	2.4		V_{CCI}	V	
V_{IL}	Input LOW Voltage	CMOS_CLK			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK	500		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC}–1.4		V_{CC}–0.6	V	
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH} = –20 mA
V_{OL}	Output LOW Voltage				0.5	V	I_{OH} = 20 mA
I_{IN}	Input Current				±200	μA	
C_{IN}	Input Capacitance			4.0		pF	
C_{pd}	Power Dissipation Capacitance			10		pF	Per output
Z_{OUT}	Output Impedance		18	23	28	Ω	
I_{CC}	Maximum Quiescent Supply Current			0.5		mA	

Table 5. AC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3 V ± 5%; V_{CCO} = 3.3 V ± 5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency				250	MHz	
t_{PLH}	Propagation Delay	PECL_CLK CMOS_CLK	1.8 1.6	2.8 2.5	3.8 3.3	ns	Note[1]
$t_{sk(o)}$	Output-to-Output Skew	PECL_CLK CMOS_CLK			200 200	ps	Note[1]
$t_{sk(pr)}$	Part-to-Part Skew	PECL_CLK CMOS_CLK			2.0 1.7	ns	Note[1]
d_t	Duty Cycle		45		55	%	Note[1]
t_r, t_f	Output Rise/Fall Time		0.1		1.3	ns	Note[1]

1. Guaranteed by statistical analysis, not 100% tested in production.

Table 6. Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 7. DC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3 V ± 5%; V_{CCO} = 2.5 V ± 5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	CMOS_CLK	2.4		V_{CCI}	V	
V_{IL}	Input LOW Voltage	CMOS_CLK			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK	500		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC}–1.4		V_{CC}–0.6	V	
V_{OH}	Output HIGH Voltage		1.8			V	I_{OH} = –20 mA
V_{OL}	Output LOW Voltage				0.5	V	I_{OH} = 20 mA
I_{IN}	Input Current				±200	μA	
C_{IN}	Input Capacitance			4.0		pF	
C_{pd}	Power Dissipation Capacitance			10		pF	Per output
Z_{OUT}	Output Impedance			23		Ω	
I_{CC}	Maximum Quiescent Supply Current			0.5		mA	

Table 8. AC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3 V ± 5%; V_{CCO} = 2.5 V ± 5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency				250	MHz	
t_{PLH}	Propagation Delay	PECL_CLK CMOS_CLK	1.8 1.6	2.8 2.5	3.9 3.4	ns	Note[1]
$t_{sk(o)}$	Output-to-Output Skew	PECL_CLK CMOS_CLK			250 250	ps	Note[1]
$t_{sk(pr)}$	Part-to-Part Skew	PECL_CLK CMOS_CLK			2.1 1.8	ns	Note[1]
d_t	Duty Cycle		45		55	%	Note[1]
t_r, t_f	Output Rise/Fall Time		0.1		1.3	ns	Note[1]

1. Guaranteed by statistical analysis, not 100% tested in production.

Table 9. Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 10. DC Characteristics (T_A = 0° to 70°C, V_{CCI} = 2.5 V ± 5%; V_{CCO} = 2.5 V ± 5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	CMOS_CLK	2.0		V_{CCI}	V	
V_{IL}	Input LOW Voltage	CMOS_CLK			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK	500		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC}–1.0		V_{CC}–0.6	V	
V_{OH}	Output HIGH Voltage		1.8			V	I_{OH} = –12 mA
V_{OL}	Output LOW Voltage				0.5	V	I_{OH} = 12 mA
I_{IN}	Input Current				±200	μA	
C_{IN}	Input Capacitance			4.0		pF	
C_{pd}	Power Dissipation Capacitance			10		pF	Per output
Z_{OUT}	Output Impedance		18	23	28	Ω	
I_{CC}	Maximum Quiescent Supply Current			0.5		mA	

Table 11. AC Characteristics (T_A = 0° to 70°C, V_{CCI} = 2.5 V ± 5%; V_{CCO} = 2.5 V ± 5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency				200	MHz	
t_{PLH}	Propagation Delay	PECL_CLK CMOS_CLK	2.2 2.0	2.8 2.5	4.9 4.2	ns	Note[1]
$t_{sk(o)}$	Output-to-Output Skew	PECL_CLK CMOS_CLK			250 250	ps	Note[1]
$t_{sk(pr)}$	Part-to-Part Skew	PECL_CLK CMOS_CLK			2.7 2.2	ns	Note[1]
d_t	Duty Cycle		45		55	%	Note[1]
t_r, t_f	Output Rise/Fall Time		0.1		1.3	ns	Note[1]

1. Guaranteed by statistical analysis, not 100% tested in production.

Order number: MPC940L
Rev 4, 08/2004

Low Voltage 1:18 Clock Distribution Chip

MPC940L

LOW VOLTAGE 1:18 CLOCK DISTRIBUTION CHIP

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC940L is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVCMOS output capabilities. The device features the capability to select either a differential LVPECL or an LVCMOS compatible input. The 18 outputs are 2.5V or 3.3V LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output-to-output skews of 150ps, the MPC940L is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance microprocessor based design. For a similar device at a lower price/performance point the reader is referred to the MPC9109.

- LVPECL or LVCMOS Clock Input
- 2.5V LVCMOS Outputs for Pentium II Microprocessor Support
- 150ps Maximum Output-to-Output Skew
- Maximum Output Frequency of 250MHz
- 32-Lead LQFP Packaging
- 32-Lead Pb-free Package Available
- Dual or Single Supply Device:
  - Dual V_{CC} Supply Voltage, 3.3V Core and 2.5V Output
  - Single 3.3V V_{CC} Supply Voltage for 3.3V Outputs
  - Single 2.5V V_{CC} Supply Voltage for 2.5V I/O

With a low output impedance (≈20Ω), in both the HIGH and LOW logic states, the output buffers of the MPC940L are ideal for driving series terminated transmission lines. With a 20Ω output impedance the 940L has the capability of driving two series terminated lines from each output. This gives the device an effective fanout of 1:36. If a lower output impedance is desired please see the MPC942 data sheet.

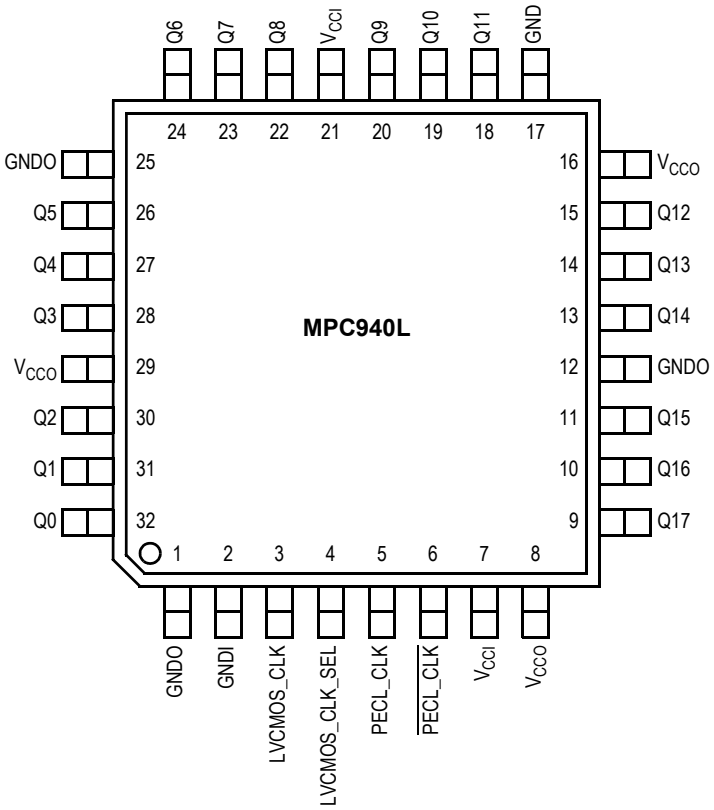
The differential LVPECL inputs of the MPC940L allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used to provide for a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_SEL pin will select the LVCMOS level clock input. All inputs of the MPC940L have internal pullup/pulldown resistor so they can be left open if unused.

The MPC940L is a single or dual supply device. The device power supply offers a high degree of flexibility. The device can operate with a 3.3V core and 3.3V output, a 3.3V core and 2.5V outputs as well as a 2.5V core and 2.5V outputs. The 32-lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

Pentium II is a trademark of Intel Corporation.

LOGIC DIAGRAM

Pinout: 32-Lead TQFP (Top View)



FUNCTION TABLE

LVCMOS_CLK_SEL	Input
0	PECL_CLK
1	LVCMOS_CLK

POWER SUPPLY VOLTAGES

Supply Pin	Voltage Level
V_{CCI}	2.5V or 3.3V ± 5%
V_{CCO}	2.5V or 3.3V ± 5%

Table 1. Pin Configurations

Pin	I/O	Type	Function
PECL_CLK $\overline{\text{PECL\_CLK}}$	Input	LVPECL	Reference Clock Input
LVCMOS_CLK	Input	LVCMOS	Alternative Reference Clock Input
LVCMOS_CLK_SEL	Input	LVCMOS	Selects Clock Source
Q0–Q17	Output	LVCMOS	Clock Outputs
V_{CCO}		Supply	Output Positive Power Supply
V_{CCI}		Supply	Core Positive Power Supply
GNDO		Supply	Output Negative Power Supply
GNDI		Supply	Core Negative Power Supply

Table 2. Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{DD} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3V ±5%; V_{CCO} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	CMOS_CLK	2.4		V_{CCI}	V	
V_{IL}	Input LOW Voltage	CMOS_CLK			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK	500		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC} –1.4		V_{CC} –0.6	V	
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH} = –20mA
V_{OL}	Output LOW Voltage				0.5	V	I_{OH} = 20mA
I_{IN}	Input Current				±200	μA	
C_{IN}	Input Capacitance			4.0		pF	
C_{pd}	Power Dissipation Capacitance			10		pF	per output
Z_{OUT}	Output Impedance		18	23	28	Ω	
I_{CC}	Maximum Quiescent Supply Current			0.5	1.0	mA	

Table 4. AC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3V ±5%; V_{CCO} = 3.3V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency				250	MHz	
t_{PLH}	Propagation Delay	PECL_CLK ≤ 150MHz CMOS_CLK ≤ 150MHz	2.0 1.8	2.7 2.5	3.4 3.0	ns	Note [1]
t_{PLH}	Propagation Delay	PECL_CLK > 150MHz CMOS_CLK > 150MHz	2.0 1.8	2.9 2.4	3.7 3.2	ns	
$t_{sk(o)}$	Output-to-Output Skew	PECL_CLK CMOS_CLK			150 150	ps	Note [1]
$t_{sk(pp)}$	Part-to-Part Skew	PECL_CLK < 150MHz CMOS_CLK < 150MHz			1.4 1.2	ns	Notes [1, 2]
$t_{sk(pp)}$	Part-to-Part Skew	PECL_CLK > 150MHz CMOS_CLK > 150MHz			1.7 1.4	ns	Notes [1, 2]
$t_{sk(pp)}$	Part-to-Part Skew	PECL_CLK CMOS_CLK			850 750	ps	Notes [1, 3]
DC	Output Duty Cycle	f_{CLK} < 134MHz f_{CLK} ≤ 250MHz	45 40	50 50	55 60	% %	Input DC = 50% Input DC = 50%
t_r, t_f	Output Rise/Fall Time		0.3		1.1	ns	0.5 – 2.4 V

1. Tested using standard input levels. Production tested @ 150MHz.
2. Across temperature and voltage ranges. Includes output skew.
3. For specific temperature and voltage. Includes output skew.

Table 5. DC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3V ±5%; V_{CCO} = 2.5V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	CMOS_CLK	2.4		V_{CCI}	V	
V_{IL}	Input LOW Voltage	CMOS_CLK			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK	500		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC} –1.4		V_{CC} –0.6	V	
V_{OH}	Output HIGH Voltage		1.8			V	I_{OH} = –20mA
V_{OL}	Output LOW Voltage				0.5	V	I_{OH} = 20mA
I_{IN}	Input Current				±200	μA	
C_{IN}	Input Capacitance			4.0		pF	
C_{pd}	Power Dissipation Capacitance			10		pF	per output
Z_{OUT}	Output Impedance			23		Ω	
I_{CC}	Maximum Quiescent Supply Current			0.5	1.0	mA	

Table 6. AC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3V ±5%; V_{CCO} = 2.5V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency				250	MHz	
t_{PLH}	Propagation Delay	PECL_CLK ≤ 150MHz CMOS_CLK ≤ 150MHz	2.0 1.7	2.8 2.5	3.5 3.0	ns	Note [1]
t_{PLH}	Propagation Delay	PECL_CLK > 150MHz CMOS_CLK > 150MHz	2.0 1.8	2.9 2.5	3.8 3.3	ns	
$t_{sk(o)}$	Output-to-Output Skew	PECL_CLK CMOS_CLK			150 150	ps	Note [1]
$t_{sk(pp)}$	Part-to-Part Skew	PECL_CLK < 150MHz CMOS_CLK < 150MHz			1.5 1.3	ns	Notes [1, 2]
$t_{sk(pp)}$	Part-to-Part Skew	PECL_CLK > 150MHz CMOS_CLK > 150MHz			1.8 1.5	ns	Notes [1, 2]
$t_{sk(pp)}$	Part-to-Part Skew	PECL_CLK CMOS_CLK			850 750	ps	Notes [1, 3]
DC	Output Duty Cycle	f_{CLK} < 134 MHz f_{CLK} ≤ 250 MHz	45 40	50 50	55 60	% %	Input DC = 50% Input DC = 50%
t_r, t_f	Output Rise/Fall Time		0.3		1.2	ns	0.5 – 1.8 V

1. Tested using standard input levels. Production tested @ 150MHz.
2. Across temperature and voltage ranges. Includes output skew.
3. For specific temperature and voltage. Includes output skew.

Table 7. DC Characteristics (T_A = 0° to 70°C, V_{CCI} = 2.5V ±5%; V_{CCO} = 2.5V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	CMOS_CLK	2.0		V_{CCI}	V	
V_{IL}	Input LOW Voltage	CMOS_CLK			0.8	V	
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK	500		1000	mV	
V_{CMR}	Common Mode Range	PECL_CLK	V_{CC} –1.0		V_{CC} –0.6	V	
V_{OH}	Output HIGH Voltage		1.8			V	I_{OH} = –12mA
V_{OL}	Output LOW Voltage				0.5	V	I_{OH} = 12mA
I_{IN}	Input Current				±200	μA	
C_{IN}	Input Capacitance			4.0		pF	
C_{pd}	Power Dissipation Capacitance			10		pF	per output
Z_{OUT}	Output Impedance		18	23	28	W	
I_{CC}	Maximum Quiescent Supply Current			0.5	1.0	mA	

Table 8. AC Characteristics (T_A = 0° to 70°C, V_{CCI} = 2.5V ±5%; V_{CCO} = 2.5V ±5%)

Symbol	Characteristic		Min	Typ	Max	Unit	Condition
F_{max}	Maximum Input Frequency				200	MHz	
t_{PLH}	Propagation Delay	PECL_CLK ≤ 150MHz CMOS_CLK ≤ 150MHz	2.6 2.3	4.0 3.1	5.2 4.0	ns	Note [1]
t_{PLH}	Propagation Delay	PECL_CLK > 150MHz CMOS_CLK > 150MHz	2.8 2.3	3.8 3.1	5.0 4.0	ns	
$t_{sk(o)}$	Output-to-Output Skew	PECL_CLK CMOS_CLK			200 200	ps	Note [1]
$t_{sk(pp)}$	Part-to-Part Skew	PECL_CLK < 150MHz CMOS_CLK < 150MHz			2.6 1.7	ns	Notes [1, 2]
$t_{sk(pp)}$	Part-to-Part Skew	PECL_CLK > 150MHz CMOS_CLK > 150MHz			2.2 1.7	ns	Notes [1, 2]
$t_{sk(pp)}$	Part-to-Part Skew	PECL_CLK CMOS_CLK			1.2 1.0	ns	Notes [1, 3]
DC	Output Duty Cycle	f_{CLK} < 134MHz f_{CLK} ≤ 250MHz	45 40	50 50	55 60	% %	Input DC = 50% Input DC = 50%
t_r, t_f	Output Rise/Fall Time		0.3		1.2	ns	0.5 - 1.8 V

1. Tested using standard input levels. Production tested @ 150MHz.
2. Across temperature and voltage ranges. Includes output skew.
3. For specific temperature and voltage. Includes output skew.

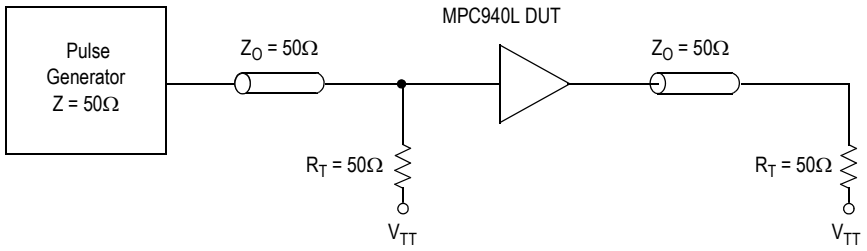


Figure 1. LVCMOS_CLK MPC940L AC Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

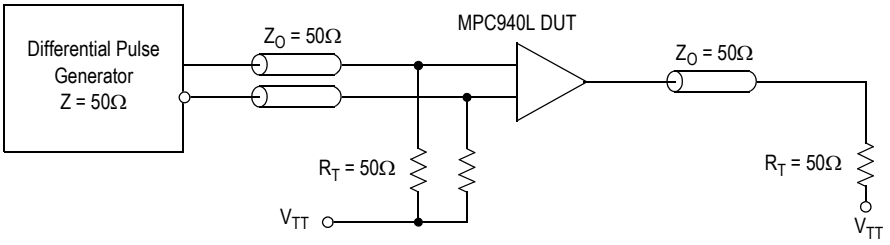


Figure 2. PECL_CLK MPC940L AC Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

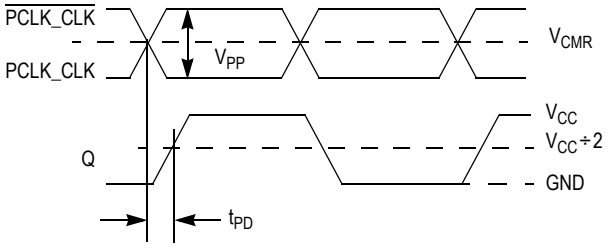


Figure 3. Propagation Delay (t_{PD}) Test Reference

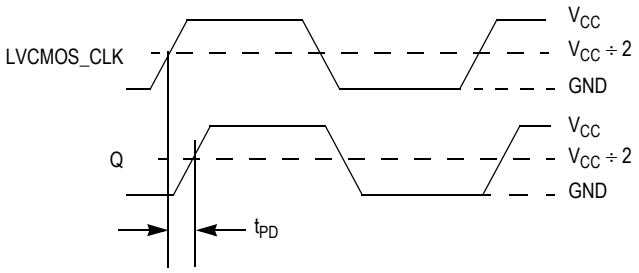
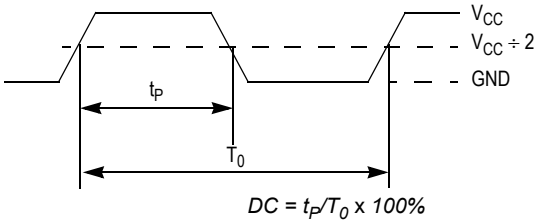
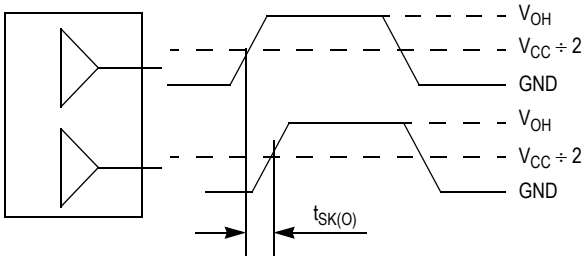


Figure 4. LVCMOS Propagation Delay (t_{PD}) Test Reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 5. Output Duty Cycle (DC)



The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay path within a single device

Figure 6. Output-to-Output Skew $T_{SK(O)}$

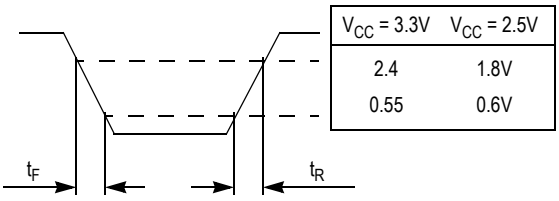


Figure 7. Output Transition Time Test Reference

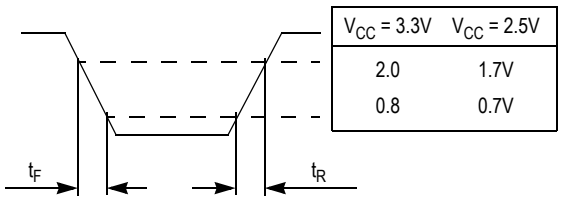


Figure 8. Input Transition Time Test Reference

Low Voltage 1:27 Clock Distribution Chip

MPC941

LOW VOLTAGE 3.3V/2.5V 1:27 CLOCK DISTRIBUTION CHIP

FA SUFFIX
48-LEAD LQFP PACKAGE
CASE 932-03

The MPC941 is a 1:27 low voltage clock distribution chip. The device features the capability to select either a differential LVPECL or an LVCMOS compatible input. The 27 outputs are LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output-to-output skews of 250ps, the MPC941 is ideal as a clock distribution chip for the most demanding of synchronous systems. For a similar product with a smaller number of outputs, please consult the MPC940 data sheet.

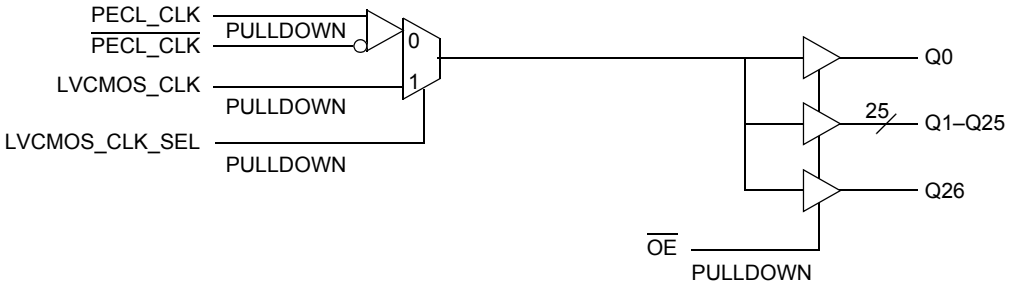
- LVPECL or LVCMOS Clock Input
- 250ps Maximum Output-to-Output Skew
- Drives Up to 54 Independent Clock Lines
- Maximum Output Frequency of 250MHz
- High Impedance Output Enable
- Extended Temperature Range: –40°C to +85°C
- 48-Lead LQFP Packaging
- 32-Lead Pb-free Package Available
- 3.3V or 2.5V V_{CC} Supply Voltage

With a low output impedance, in both the HIGH and LOW logic states, the output buffers of the MPC941 are ideal for driving series terminated transmission lines. More specifically, each of the 27 MPC941 outputs can drive two series terminated 50Ω transmission lines. With this capability, the MPC941 has an effective fanout of 1:54. With this level of fanout, the MPC941 provides enough copies of low skew clocks for most high performance synchronous systems.

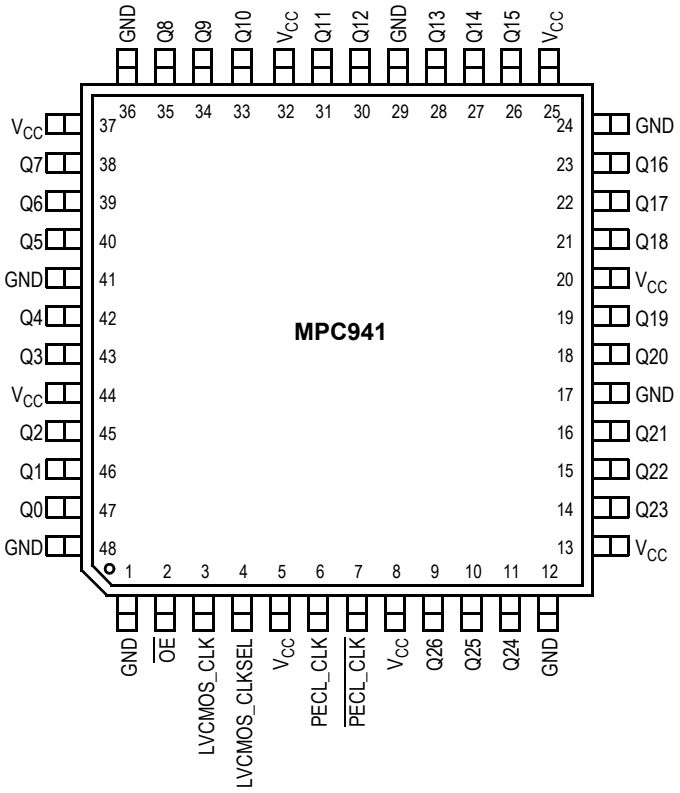
The differential LVPECL inputs of the MPC941 allow the device to interface directly with an LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The LVCMOS input provides a more standard interface for applications requiring only a single clock distribution chip at relatively low frequencies. In addition, the two clock sources can be used as a test clock interface as well as the primary system clock. A logic HIGH on the LVCMOS_CLK_Sel pin will select the LVCMOS level clock input.

The MPC941 is fully 3.3V and 2.5V compatible. The 48-lead LQFP package was chosen to optimize performance, board space and cost of the device. The 48-lead LQFP has a 7x7mm body size.

LOGIC DIAGRAM



Pinout: 48-Lead TQFP (Top View)



FUNCTION TABLE

LVCMOS_CLK_SEL	Input
0	PECL_CLK
1	LVCMOS_CLK

Table 1. Pin Configuration

Pin	I/O	Type	Function
PECL_CLK, PECL_CLK	Input	LVPECL	LVPECL differential reference clock inputs
LVCMOS_CLK	Input	LVCMOS	Alternative reference clock input
LVCMOS_CLK_SEL	Input	LVCMOS	Input reference clock select
OE	Input	LVCMOS	Output tristate control
GND		Supply	Negative voltage supply output bank (GND)
V_{CC}		Supply	Positive voltage supply
Q0–Q26	Output	LVCMOS	Clock outputs

Table 2. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V
I_{IN}	DC Input Current		±20	mA
I_{OUT}	DC Output Current		±50	mA
T_S	Storage Temperature	–40	125	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40 to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	LVCMOS_CLK	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	LVCMOS_CLK	–0.3		0.8	V	LVCMOS
I_{IN}	Input Current				±120[1]	μA	
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK, $\overline{\text{PECL\_CLK}}$	500			mV	LVPECL
V_{CMR}	Common Mode Range	PECL_CLK, $\overline{\text{PECL\_CLK}}$	1.2		V_{CC} –0.8	V	LVPECL
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA[2]
V_{OL}	Output Low Voltage				0.55 0.40	V V	I_{OL} = 24mA[2] I_{OL} = 12mA
I_{OZ}	Output Tristate Leakage Current				100	μA	
Z_{OUT}	Output Impedance			14 – 17		Ω	
C_{PD}	Power Dissipation Capacitance			7-8	10	pF	Per Output
C_{IN}	Input Capacitance			4.0		pF	
I_{CCQ}	Maximum Quiescent Supply Current				5	mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage			$V_{CC} \div 2$		V	

1. Input pull-up / pull-down resistors influence input current.
2. The MPC941 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

Table 4. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = –40 to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{MAX}	Maximum Output Frequency		0		250[2]	MHz	
t_r, t_f	LVCMOS_CLK Input Rise/Fall Time				1.0[3]	ns	0.8 to 2.0V
t_{PLH} t_{PHL}	Propagation Delay	PECL_CLK to any Q LVCMOS_CLK to any Q	1.2 0.9	1.8 1.5	2.6 2.3	ns ns	
$t_{PLZ, HZ}$	Output Disable Time					ns	
$t_{PZL, LZ}$	Output Enable Time					ns	
$t_{sk(O)}$	Output-to-Output Skew	PECL_CLK to any Q LVCMOS_CLK to any Q		125 125	250 250	ps	
$t_{sk(PP)}$	Device-to-Device Skew	PECL_CLK to any Q LVCMOS_CLK to any Q			1000 1000	ps ps	For a given T_A and V_{CC}, any Q
$t_{sk(PP)}$	Device-to-Device Skew	PECL_CLK to any Q LVCMOS_CLK to any Q			1400 1400	ps ps	For any T_A, V_{CC} and Q
DC_Q	Output Duty Cycle	PECL_CLK to any Q LVCMOS_CLK to any Q	45 45	50 50	60 55	% %	DC_{REF} = 50% DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time		0.2		1.0	ns	0.55 to 2.4V

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. AC characteristics are guaranteed up to fmax. Please refer to applications section for information on power consumption versus operating frequency and thermal management.
3. Fast input signal transition times are required to maintain part-to-part skew specification. If part-to-part skew is not critical to the application, signal transition times smaller than 3 ns can be applied to the MPC941.

Table 5. DC Characteristics (V_{CC} = 2.5V ± 5%, T_A = –40 to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	LVCMOS_CLK	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	LVCMOS_CLK	–0.3		0.7	V	LVCMOS
I_{IN}	Input Current				±120[1]	μA	
V_{PP}	Peak-to-Peak Input Voltage	PECL_CLK, $\overline{\text{PECL\_CLK}}$	500			mV	LVPECL
V_{CMR}	Common Mode Range	PECL_CLK, $\overline{\text{PECL\_CLK}}$	1.1		V_{CC} – 0.7	V	LVPECL
V_{OH}	Output High Voltage		1.8			V	I_{OH} = –15 mA[2]
V_{OL}	Output Low Voltage				0.6	V	I_{OL} = 15 mA[2]
I_{OZ}	Output Tristate Leakage Current				100	μA	
Z_{OUT}	Output Impedance			18 – 20		Ω	
C_{PD}	Power Dissipation Capacitance			7 – 8	10	pF	Per Output
C_{IN}	Input Capacitance			4.0		pF	
I_{CCQ}	Maximum Quiescent Supply Current				5	mA	All V_{CC} Pins
V_{TT}	Output Termination Voltage			$V_{CC} \div 2$		V	

1. Input pull-up / pull-down resistors influence input current.
2. The MPC941 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.

Table 6. AC Characteristics (V_{CC} = 2.5V ± 5%, T_A = –40 to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{MAX}	Maximum Output Frequency		0		250[2]	MHz	
t_r, t_f	LVCMOS_CLK Input Rise/Fall Time				1.0[3]	ns	0.7 to 1.7V
t_{PLH} t_{PHL}	Propagation Delay	PECL_CLK to any Q LVCMOS_CLK to any Q	1.3 1.0	2.1 1.8	2.9 2.6	ns ns	
$t_{PLZ, HZ}$	Output Disable Time					ns	
$t_{PZL, LZ}$	Output Enable Time					ns	
$t_{sk(O)}$	Output-to-Output Skew	PECL_CLK to any Q LVCMOS_CLK to any Q		125 125	250 250	ps	
$t_{sk(PP)}$	Device-to-Device Skew	PECL_CLK to any Q LVCMOS_CLK to any Q			1200 1200	ps ps	For a given T_A and V_{CC}, any Q
$t_{sk(PP)}$	Device-to-Device Skew	PECL_CLK to any Q LVCMOS_CLK to any Q			1600 1600	ps ps	For any T_A, V_{CC} and Q
DC_Q	Output Duty Cycle	PECL_CLK to any Q LVCMOS_CLK to any Q	45 45	50 50	60 55	% %	DC_{REF} = 50% DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time		0.2		1.0	ns	0.6 to 1.6V

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. AC characteristics are guaranteed up to f_{MAX}. Please refer to the applications section for information on power consumption versus operating frequency and thermal management.
3. Fast input signal transition times are required to maintain part-to-part skew specification. If part-to-part skew is not critical to the application, signal transition times smaller than 3 ns can be applied to the MPC941.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC941 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091 in the Timing Solutions data book (DL207/D).

In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}/2. This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC941 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 1 illustrates an output driving a single series terminated line vs two series terminated lines in parallel. When taken to its extreme the fanout of the MPC941 clock driver is effectively doubled due to its capability to drive multiple lines.

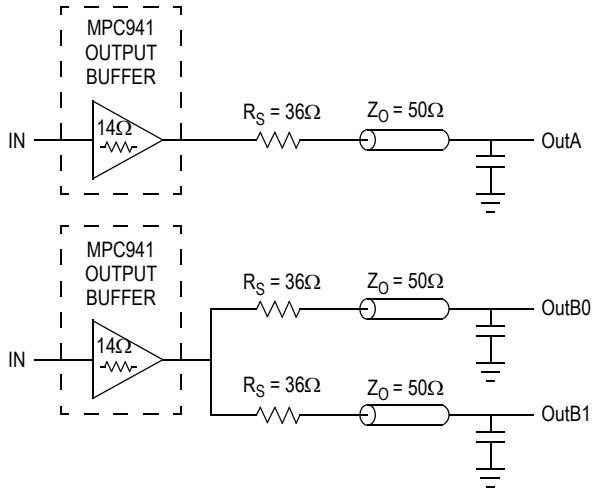


Figure 1. Single versus Dual Transmission Lines

The waveform plots of Figure 2 show the simulation results of an output driving a single line vs two lines. In both cases the drive capability of the MPC941 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC941. The output waveform in Figure 2 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

VL = VS (Zo / (Rs + Ro + Zo))
Zo = 50Ω || 50Ω
Rs = 36Ω || 36Ω
Ro = 14Ω
VL = 3.0 (25 / (18 + 14 + 25) = 3.0 (25 / 57)
= 1.31V

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

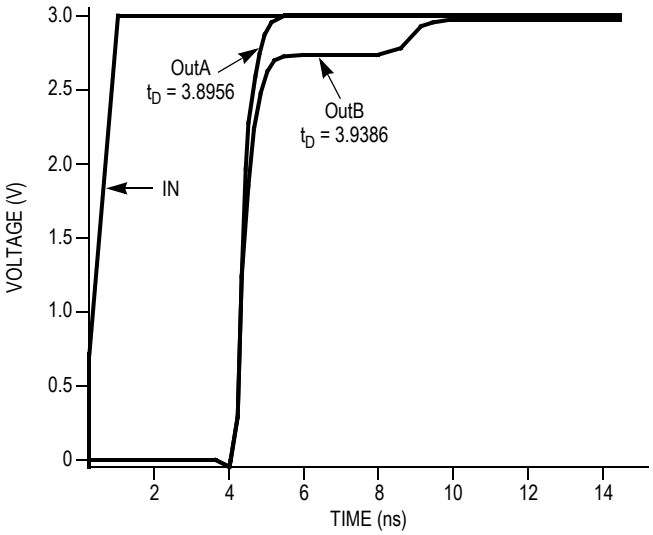
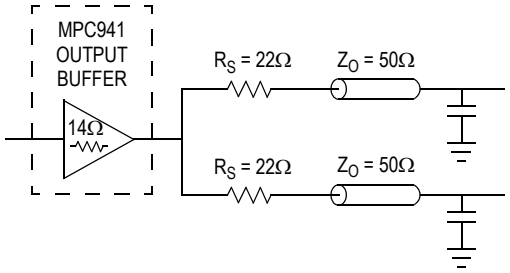


Figure 2. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 3 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



14Ω + 22Ω || 22Ω = 50Ω ||50Ω
25Ω = 25Ω

Figure 3. Optimized Dual Line Termination

Power Consumption of the MPC941 and Thermal Management

The MPC941 AC specification is guaranteed for the entire operating frequency range up to 250 MHz. The MPC941 power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperture, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC941 die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

Table 7. Die Junction Temperature and MTBF

Junction Temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC941 needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC941 is represented in equation 1.

Where I_{CCQ} is the static current consumption of the MPC941, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 27 in case of the MPC941). The MPC941 supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL}, I_{OL}, V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cyle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 7, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC941 in a series terminated transmission line system.

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 7. R_{thja} can be derived from Table 8 The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

Table 8. Thermal Package Impedance of the 48ld LQFP

Convection, LFPM	R_{thja} (1P2S board), K/W
Still air	78
100 lfpm	68
200 lfpm	59
300 lfpm	56
400 lfpm	54
500 lfpm	53

If the calculated maximum frequency is below 250 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the MPC941. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to a estimated MTBF of 9.1 years (4 years), a supply voltage of either 3.3V or 2.5V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \qquad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \qquad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \qquad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{j,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \qquad \text{Equation 4}$$

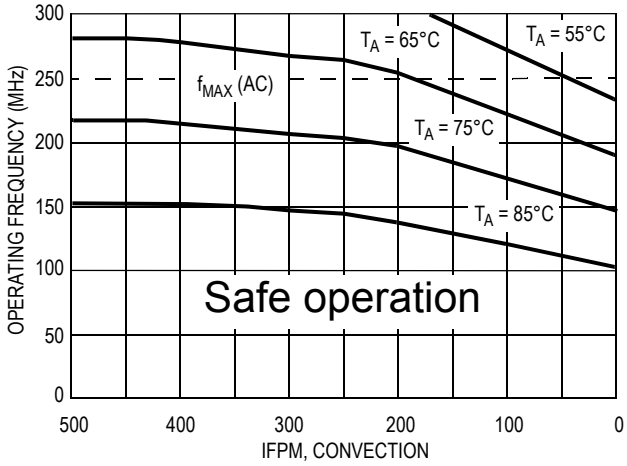


Figure 4. Maximum MPC941 frequency, V_{CC} = 3.3V, MTBF 9.1 years, driving series terminated transmission lines

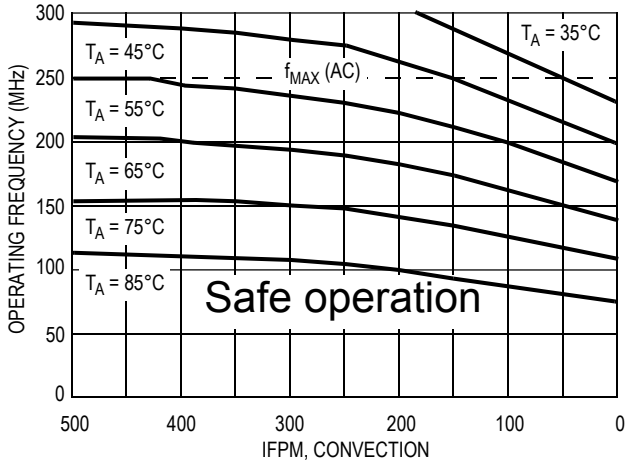


Figure 5. Maximum MPC941 frequency, V_{CC} = 3.3V, MTBF 9.1 years, 4 pF load per line

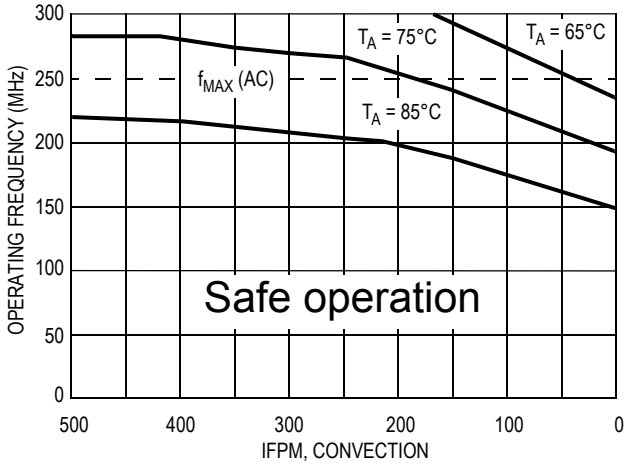


Figure 6. Maximum MPC941 frequency, V_{CC} = 3.3V, MTBF 4 years, driving series terminated transmission lines

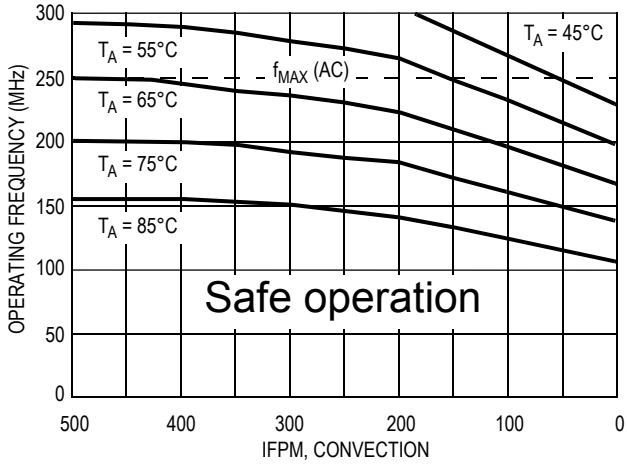


Figure 7. Maximum MPC941 frequency, V_{CC} = 3.3V, MTBF 4 years, 4 pF load per line

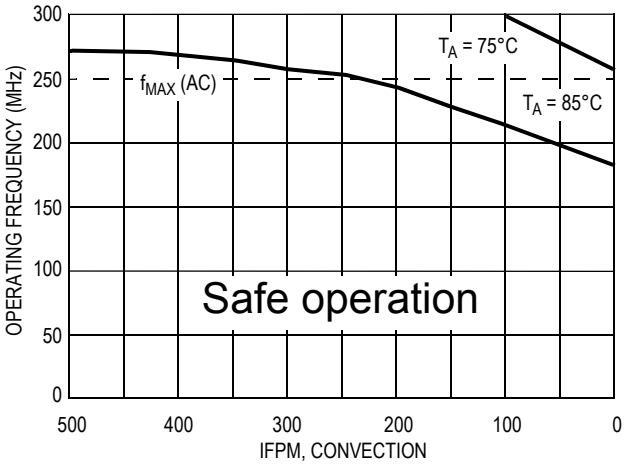


Figure 8. Maximum MPC941 frequency, V_{CC} = 2.5V, MTBF 9.1 years, driving series terminated transmission lines

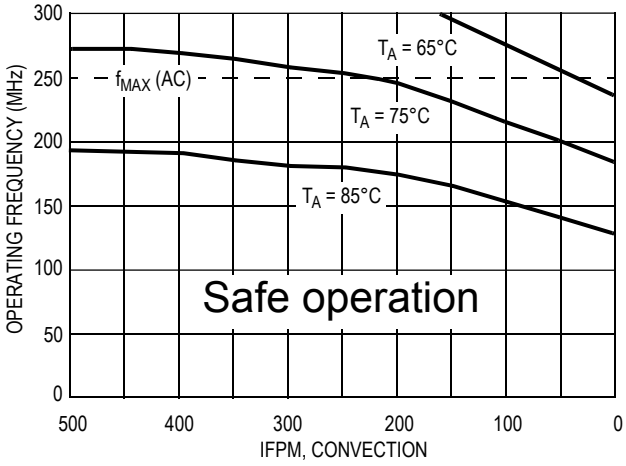


Figure 9. Maximum MPC941 frequency, V_{CC} = 2.5V, MTBF 9.1 years, 4 pF load per line

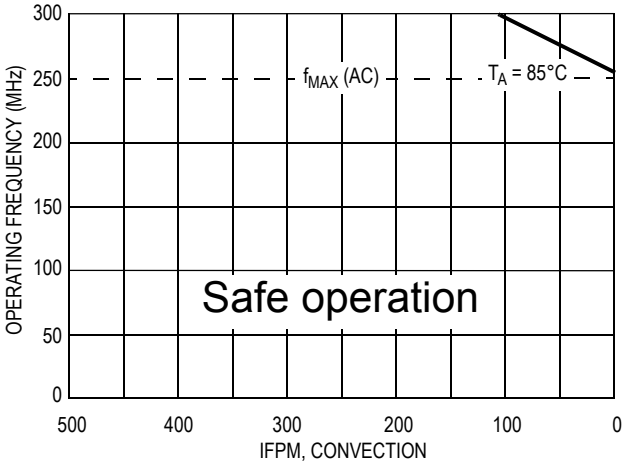


Figure 10. Maximum MPC941 frequency, V_{CC} = 2.5V, MTBF 4 years, driving series terminated transmission lines

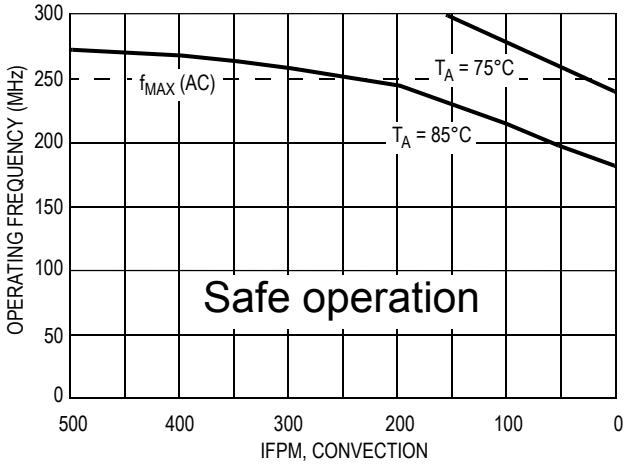


Figure 11. Maximum MPC941 frequency, V_{CC} = 2.5V, MTBF 4 years, 4 pF load per line

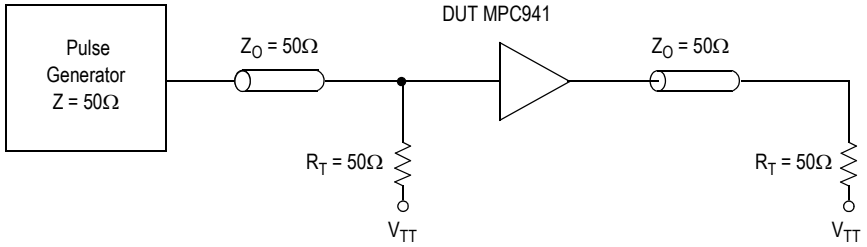


Figure 12. LVCMOS_CLK MPC941 AC Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

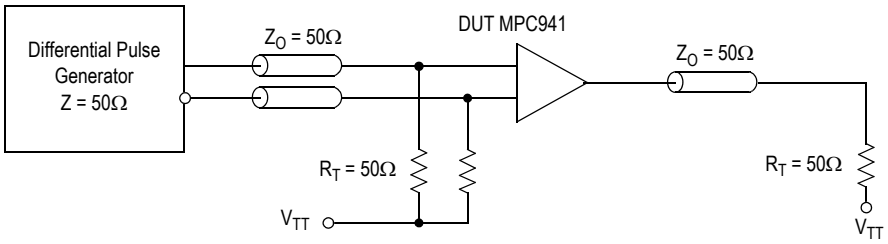


Figure 13. PECL_CLK MPC941 AC Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

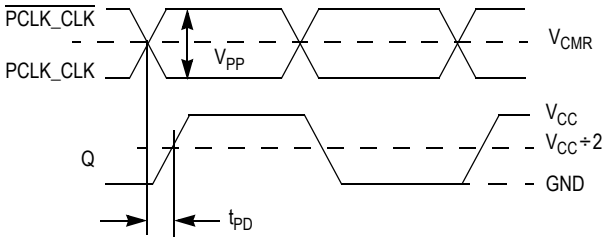


Figure 14. LVPECL Propagation Delay (t_{PD}) Test Reference

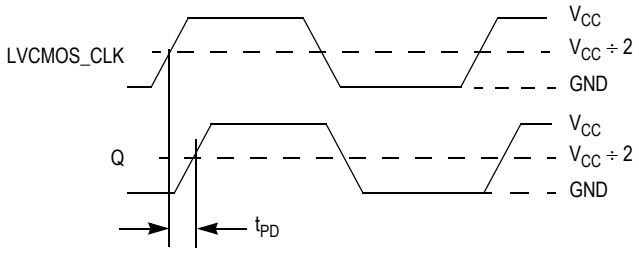
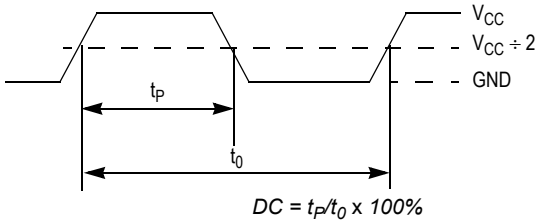
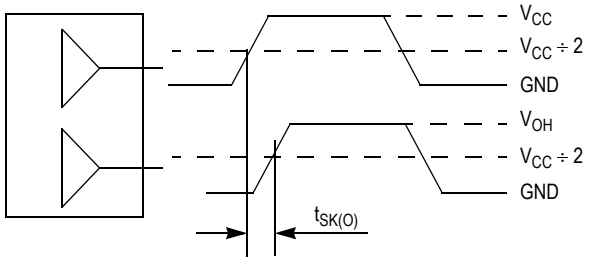


Figure 15. LVCMOS Propagation Delay (t_{PD}) Test Reference



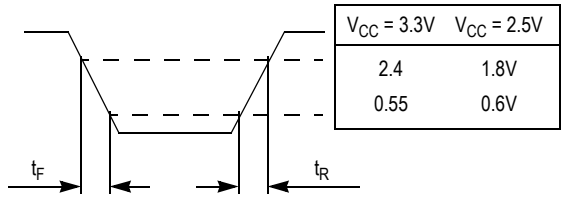
The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)



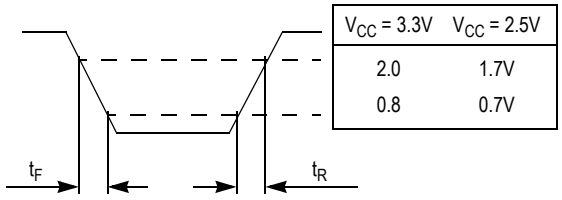
The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay path within a single device

Figure 17. Output-to-Output Skew $t_{SK(O)}$



V_{CC} = 3.3V	V_{CC} = 2.5V
2.4	1.8V
0.55	0.6V

Figure 18. Output Transition Time Test Reference



V_{CC} = 3.3V	V_{CC} = 2.5V
2.0	1.7V
0.8	0.7V

Figure 19. Input Transition Time Test Reference

Order number: MPC942C
Rev 0, 02/2001

Low Voltage 1:18 Clock Distribution Chip

MPC942C

LOW VOLTAGE 1:18 CLOCK DISTRIBUTION CHIP

FA SUFFIX
32-LEAD TQFP PACKAGE
CASE 873A-03

The MPC942 is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVCMOS output capabilities. The device is offered in two versions; the MPC942C has an LVCMOS input clock while the MPC942P has a LVPECL input clock. The 18 outputs are 2.5V or 3.3V LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output-to-output skews of 200ps, the MPC942 is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance Pentium II™ microprocessor based design.

- LVCMOS/LVTTL Clock Input
- 2.5V LVCMOS Outputs for Pentium II Microprocessor Support
- 150ps Maximum Targeted Output-to-Output Skew
- Maximum Output Frequency of 250MHz @ 3.3 V_{CC}
- 32-Lead TQFP Packaging
- Single 3.3V or 2.5V Supply

With a low output impedance (≈12Ω), in both the HIGH and LOW logic states, the output buffers of the MPC942 are ideal for driving series terminated transmission lines. With an output impedance of 12Ω the MPC942 can drive two series terminated transmission lines from each output. This capability gives the MPC942 an effective fanout of 1:36. The MPC942 provides enough copies of low skew clocks for most high performance synchronous systems.

The LVCMOS/LVTTL input of the MPC942C provides a more standard LVCMOS interface. The OE pins will place the outputs into a high impedance state. The OE pin has an internal pullup resistor.

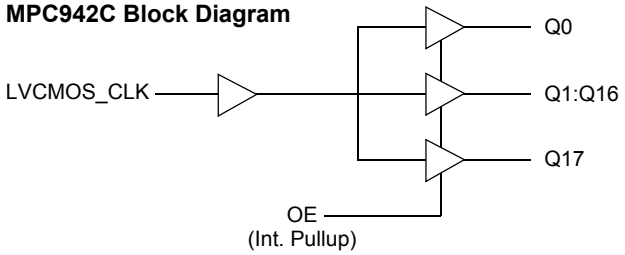
The MPC942 is a single supply device. The V_{CC} power pins require either 2.5V or 3.3V. The 32-lead TQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead TQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

Pentium II is a trademark of Intel Corporation.

Pentium II is a trademark of Intel Corporation.

LOGIC DIAGRAM

MPC942C Block Diagram



FUNCTION TABLE

OE	Output
0	HIGH IMPEDANCE
1	OUTPUTS ENABLED

Pinout: 32-Lead (Top View)

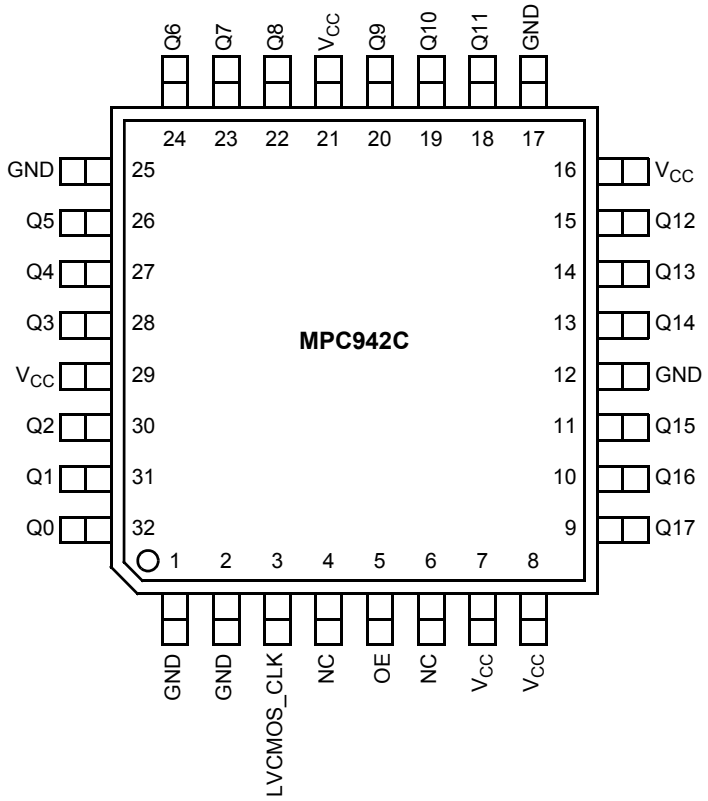


Table 1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

Table 2. DC Characteristics (T_A = 0° to 70°C, V_{CCI} = 2.5V ±5%, V_{CCO} = 2.5V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CCI}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.0			V	I_{OH} = –16 mA
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 16 mA
I_{IN}	Input Current			±200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5		mA	

Table 3. AC Characteristics (T_A = 0° to 70°C, V_{CCI} = 2.5V ±5%, V_{CCO} = 2.5V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			200	MHz	
t_{PLH}	Propagation Delay	1.5		2.8	ns	
$t_{sk(o)}$	Output-to-Output Skew			200	ps	
$t_{sk(pr)}$	Part-to-Part Skew			1.3	ns	Notes 1, 2
$t_{sk(pr)}$	Part-to-Part Skew			600	ps	Notes 1, 3
d_t	Duty Cycle	45		55	%	
t_r, t_f	Output Rise/Fall Time	0.2		1.0	ns	

Table 4. DC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3V ±5%, V_{CCO} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.4		V_{CCI}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20 mA
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 20 mA
I_{IN}	Input Current			±200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5		mA	

Table 5. AC Characteristics (T_A = 0° to 70°C, V_{CCI} = 3.3V ±5%, V_{CCO} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			250	MHz	
t_{PLH}	Propagation Delay	1.3		2.3	ns	Note 1
$t_{sk(o)}$	Output-to-Output Skew			200	ps	
$t_{sk(pr)}$	Part-to-Part Skew			1.0	ns	Notes 1, 2
$t_{sk(pr)}$	Part-to-Part Skew			500	ps	Notes 1, 3
d_t	Duty Cycle	45		55	%	
t_r, t_f	Output Rise/Fall Time	0.2		1.0	ns	

1. Tested using standard input levels, production tested @ 133 MHz.
2. Across temperature and voltage ranges, includes output skew.
3. For a specific temperature and voltage, includes output skew.

Order number: MPC942P
Rev 1, 02/2001

Low Voltage 1:18 Clock Distribution Chip

MPC942P

LOW VOLTAGE 1:18 CLOCK DISTRIBUTION CHIP

FA SUFFIX
32-LEAD TQFP PACKAGE
CASE 873A-03

The MPC942 is a 1:18 low voltage clock distribution chip with 2.5V or 3.3V LVCMOS output capabilities. The device is offered in two versions; the MPC942C has an LVCMOS input clock while the MPC942P has a LVPECL input clock. The 18 outputs are 2.5V or 3.3V LVCMOS compatible and feature the drive strength to drive 50Ω series or parallel terminated transmission lines. With output-to-output skews of 200ps, the MPC942 is ideal as a clock distribution chip for the most demanding of synchronous systems. The 2.5V outputs also make the device ideal for supplying clocks for a high performance Pentium II™ microprocessor based design.

- LVPECL Clock Input
- 2.5V LVCMOS Outputs for Pentium II Microprocessor Support
- 200ps Maximum Targeted Output-to-Output Skew
- Maximum Output Frequency of 250MHz @ 3.3 V_{CC}
- 32-Lead LQFP Packaging
- Single 3.3V or 2.5V Supply

With a low output impedance (≈12Ω), in both the HIGH and LOW logic states, the output buffers of the MPC942 are ideal for driving series terminated transmission lines. With an output impedance of 12Ω the MPC942 can drive two series terminated transmission lines from each output. This capability gives the MPC942 an effective fanout of 1:36. The MPC942 provides enough copies of low skew clocks for most high performance synchronous systems.

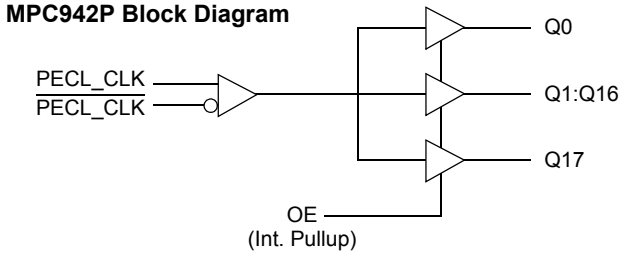
The differential LVPECL inputs of the MPC942P allow the device to interface directly with a LVPECL fanout buffer like the MC100EP111 to build very wide clock fanout trees or to couple to a high frequency clock source. The OE pins will place the outputs into a high impedance state. The OE pin has an internal pullup resistor.

The MPC942 is a single supply device. The V_{CC} power pins require either 2.5V or 3.3V. The 32-lead LQFP package was chosen to optimize performance, board space and cost of the device. The 32-lead LQFP has a 7x7mm body size with a conservative 0.8mm pin spacing.

Pentium II is a trademark of Intel Corporation.

LOGIC DIAGRAM

MPC942P Block Diagram



FUNCTION TABLE

OE	Output
0 1	HIGH IMPEDANCE OUTPUTS ENABLED

Pinout: 32-Lead (Top View)

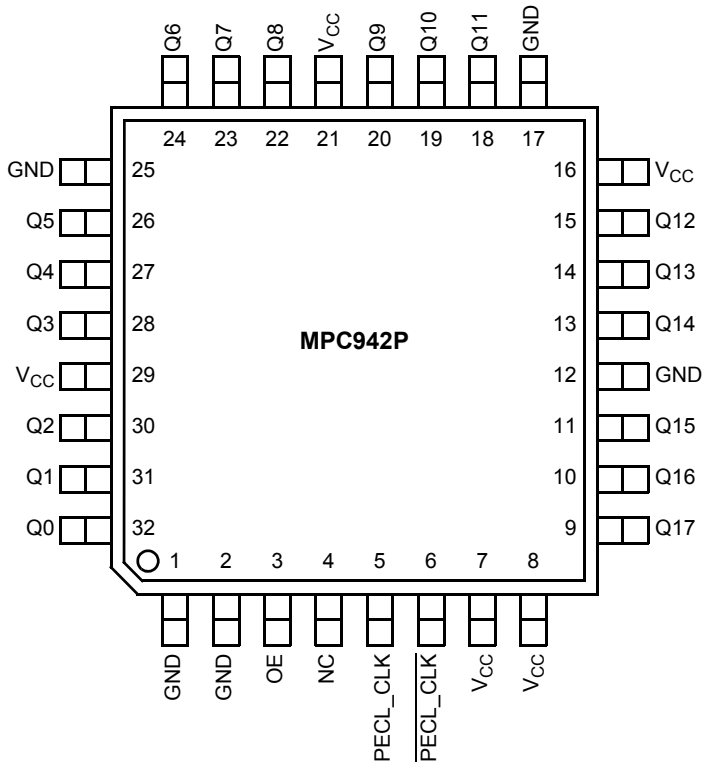


Table 1. Absolute Maximum Ratings[1]

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.6	V
V_I	Input Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	Input Current		±20	mA
T_{Stor}	Storage Temperature Range	–40	125	°C

1. Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 2. DC Characteristics (T_A = 0° to 70°C, V_{CC} = 2.5V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{PP}	Input Swing PECL_CLK	0.6		1.0	V	
V_X	Input Crosspoint PECL_CLK	V_{CC}–1.0		V_{CC}–0.6	V	
V_{OH}	Output HIGH Voltage	2.0			V	I_{OH} = –16 mA
V_{OL}	Output LOW Voltage			0.5	V	I_{OL} = 16 mA
I_{IN}	Input Current			±200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5	5.0	mA	

Table 3. AC Characteristics (T_A = 0° to 70°C, V_{CC} = 2.5V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			200	MHz	
t_{PLH}	Propagation Delay	1.8		4.0	ns	
t_{PHL}	Propagation Delay	2.0		4.3	ns	
$t_{sk(o)}$	Output-to-Output Skew			200	ps	
$t_{sk(pr)}$	Part-to-Part Skew			2.2	ns	Note 2
$t_{sk(pr)}$	Part-to-Part Skew			1.3	ps	Note 1
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	

1. For a specific temperature and voltage, includes output skew.
2. Across temperature and voltage ranges, includes output skew.

Table 4. DC Characteristics (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage	2.4		V_{CC}	V	
V_{IL}	Input LOW Voltage			0.8	V	
V_{PP}	Input Swing PECL.CLK	0.6		1.0	V	
V_X	Input Crosspoint PECL_CLK	V_{CC}–1.0		V_{CC}–0.6	V	
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = –20 mA
V_{OL}	Output LOW Voltage			0.6	V	I_{OL} = 20 mA
I_{IN}	Input Current			±200	μA	
C_{IN}	Input Capacitance		4.0		pF	
C_{PD}	Power Dissipation Capacitance		14		pF	Per Output
Z_{OUT}	Output Impedance		12		Ω	
I_{CC}	Maximum Quiescent Supply Current		0.5	5.0	mA	

Table 5. AC Characteristics (T_A = 0° to 70°C, V_{CC} = 3.3V ±5%)

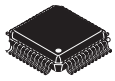
Symbol	Characteristic	Min	Typ	Max	Unit	Condition
F_{max}	Maximum Frequency			250	MHz	
t_{PLH}	Propagation Delay	1.5		3.2	ns	
t_{PHL}	Propagation Delay	1.5		3.6	ns	
$t_{sk(o)}$	Output-to-Output Skew			200	ps	
$t_{sk(pr)}$	Part-to-Part Skew			1.7	ns	Note 2
$t_{sk(pr)}$	Part-to-Part Skew			1.0	ps	Note 1
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	

1. For a specific temperature and voltage, includes output skew.
2. Across temperature and voltage ranges, includes output skew.

2.5 V and 3.3 V LVCMOS Clock Fanout Buffer

MPC9443

LOW VOLTAGE SUPPLY
2.5 V AND 3.3 V LVCMOS
CLOCK FANOUT BUFFER



FA SUFFIX
48-LEAD LQFP PACKAGE
CASE 932-03

The MPC9443 is a 2.5 V and 3.3 V compatible 1:16 clock distribution buffer designed for low-voltage high-performance telecom, networking and computing applications. The device supports 3.3 V, 2.5 V and dual supply voltage (mixed-voltage) applications. The MPC9443 offers 16 low-skew outputs which are divided into 4 individually configurable banks. Each output bank can be individually supplied by 2.5 V or 3.3 V, individually set to run at 1X or 1/2X of the input clock frequency or be disabled (logic low output state). Two selectable LVPECL compatible inputs support differential clock distribution systems. In addition, one selectable LVCMOS input is provided for LVCMOS clock distribution systems. The MPC9443 is specified for the extended temperature range of –40 to +85°C.

Features

- Configurable 16 outputs LVCMOS clock distribution buffer
- Compatible to single, dual and mixed 3.3 V / 2.5 V voltage supply
- Output clock frequency up to 350 MHz
- Designed for high-performance telecom, networking and computer applications
- Supports applications requiring clock redundancy
- Maximum output skew of 250 ps (125 ps within one bank)
- Selectable output configurations per output bank
- Individually per-bank high-impedance tristate
- Output disable (stop in logic low state) control
- 48-lead LQFP package
- 48-lead Pb-free Package Available
- Ambient operating temperature range of –40 to 85°C

Functional Description

The MPC9443 is a full static design supporting clock frequencies up to 350 MHz. The signals are generated and retimed on-chip to ensure minimal skew between the four output banks.

Two independent LVPECL compatible clock inputs are available. This feature supports redundant differential clock sources. In addition, the MPC9443 supports single-ended LVCMOS clock distribution systems. Each of the four output banks can be individually supplied by 2.5 V or 3.3 V, supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each output bank. The MPC9443 output banks are in high-impedance state by deasserting the $\overline{OE}_N$ pins. Asserting $\overline{OE}_N$ will the enable output banks. Please see Table 4. Output High-Impedance Control (OE_N) for details. The outputs can be synchronously stopped (logic low state). The outputs provide

LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. For series terminated transmission lines, each of the MPC9443 outputs can drive one or two traces giving the devices an effective fanout of 1:32 at V_{CC} = 3.3 V. The device is packaged in a 7x7 mm^2 48-lead LQFP package.

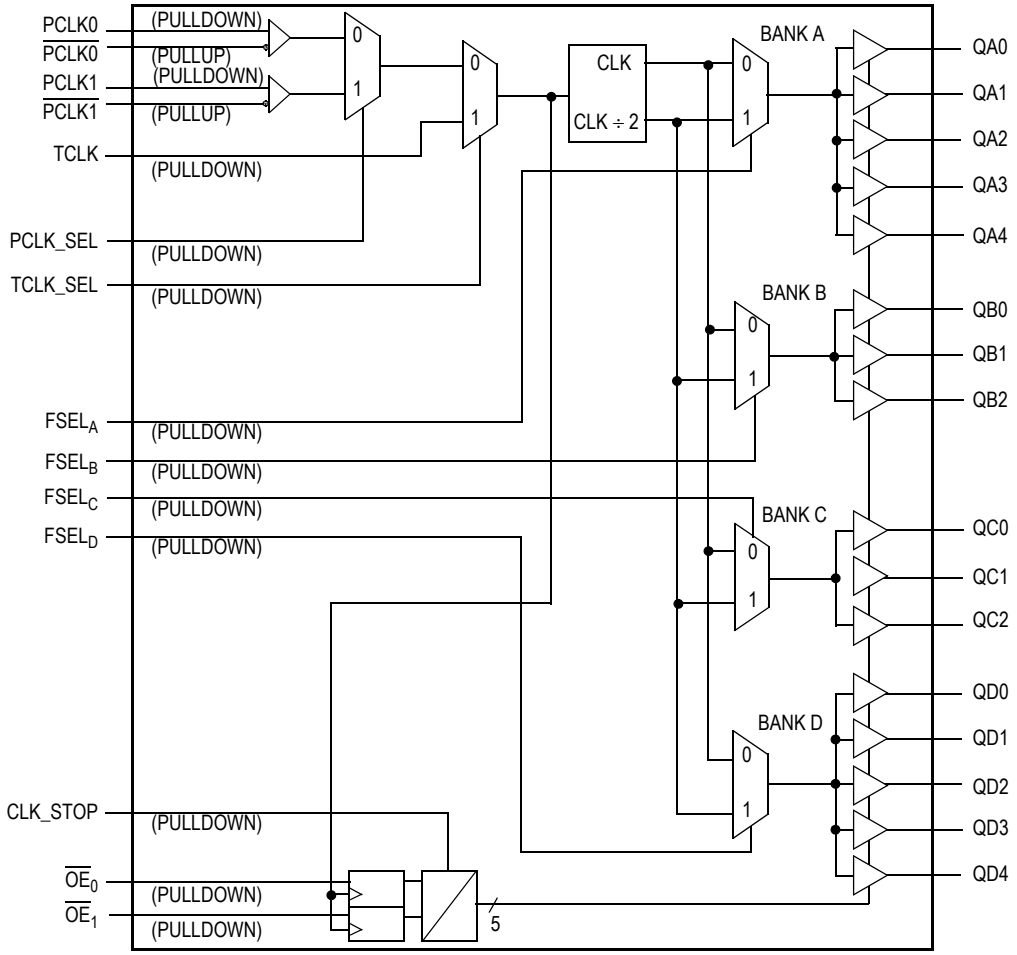


Figure 1. MPC9443 Logic Diagram

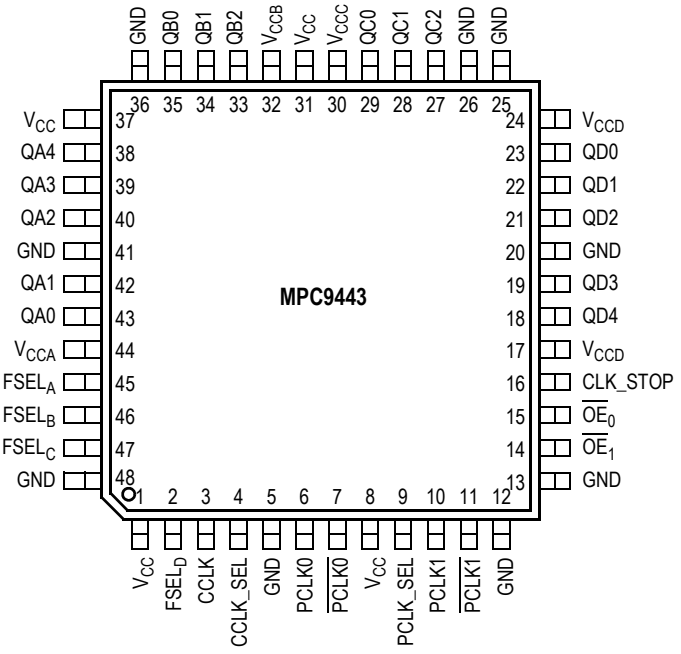


Figure 2. 48-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK	Input	LVCMOS	LVCMOS clock inputs
PCLK0, $\overline{\text{PCLK0}}$	Input	LVCMOS	LVPECL differential clock input
PCLK1, $\overline{\text{PCLK1}}$	Input	LVCMOS	LVPECL differential clock input
$FSEL_A$, $FSEL_B$, $FSEL_C$, $FSEL_D$	Input	LVCMOS	Output bank divide select input
CCLK_SEL	Input	LVCMOS	LVCMOS/LVPECL clock input select
PCLK_SEL	Input	LVCMOS	PCLK0/PCLK1 clock input select
OE_0, OE_1	Input	LVCMOS	Output tristate control
CLK_STOP	Input	LVCMOS	Synchronous output enable/disable (clock stop) control
GND		Supply	Negative voltage supply
V_{CCA}, V_{CCB}, V_{CCC}, V_{CCD}		Supply	Positive voltage supply output bank (V_{CC})
V_{CC}		Supply	Positive voltage supply core (V_{CC})
QA0 to QA4	Output	LVCMOS	Bank A outputs
QB0 to QB2	Output	LVCMOS	Bank B outputs
QC0 to QC2	Output	LVCMOS	Bank C outputs
QD0 to QD4	Output	LVCMOS	Bank D outputs

Table 2. Supported Single and Dual Supply Configurations

Supply Voltage Configuration	V_{CC}[1]	V_{CCA}[2]	V_{CCB}[3]	V_{CCC}[4]	V_{CCD}[5]	GND
3.3 V Supply	3.3 V	3.3 V	3.3 V	3.3 V	3.3 V	0 V
Mixed Mode Supply	3.3 V	3.3 V or 2.5 V	3.3 V or 2.5 V	3.3 V or 2.5 V	3.3 V or 2.5 V	0 V
2.5 V Supply	2.5 V	2.5 V	2.5 V	2.5 V	2.5 V	0 V

1. V_{CC} is the positive power supply of the device core and input circuitry. V_{CC} voltage defines the input threshold and levels.
2. V_{CCA} is the positive power supply of the bank A outputs. V_{CCA} voltage defines bank A output levels.
3. V_{CCB} is the positive power supply of the bank B outputs. V_{CCB} voltage defines bank B output levels.
4. V_{CCC} is the positive power supply of the bank C outputs. V_{CCC} voltage defines bank C output levels.
5. V_{CCD} is the positive power supply of the bank D outputs. V_{CCD} voltage defines bank D output levels.

Table 3. Function Table (Controls)

Control	Default	0	1
CCLK_SEL	0	PCLK or PCLK1 active (LVPECL clock mode)	CCLK active (LVCMOS clock mode)
PCLK_SEL	0	PCLK0 active, PCLK1 inactive	PCLK1 active, PCLK0 inactive
$FSEL_A$	0	$f_{QA0:4} = f_{REF}$	$f_{QA0:4} = f_{REF} \div 2$
$FSEL_B$	0	$f_{QB0:2} = f_{REF}$	$f_{QB0:2} = f_{REF} \div 2$
$FSEL_C$	0	$f_{QC0:2} = f_{REF}$	$f_{QC0:2} = f_{REF} \div 2$
$FSEL_D$	0	$f_{QD0:4} = f_{REF}$	$f_{QD0:4} = f_{REF} \div 2$
CLK_STOP	0	Normal operation	Outputs are synchronously disabled (stopped) in logic low state
OE_0, OE_1	00	Asynchronous output enable control. See Table 4. Output High-Impedance Control (OE_N)	

Table 4. Output High-Impedance Control ($\overline{OE_N}$)[1]

OE_0	OE_1	QA0 to QA4	QB0 to QB2	QC0 to QC2	QD0 to QD4	Total Number of Enabled Outputs
0	0	Enabled	Enabled	Enabled	Enabled	16
0	1	Enabled	Disabled (tristate)	Disabled (tristate)	Enabled	10
1	0	Enabled	Enabled	Disabled (tristate)	Disabled (tristate)	8
1	1	Disabled (tristate)	Disabled (tristate)	Disabled (tristate)	Disabled (tristate)	0

1. $\overline{OE_N}$ will tristate (high impedance) output banks independent on the logic state of the output and the status of CLK_STOP.

Table 5. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 6. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	

Table 7. DC Characteristics (V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD} = 3.3 V ± 5%, T_A = –40 to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage		–0.3		0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage	PCLK0, 1	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK0, 1	1.1		V_{CC} – 0.6	V	LVPECL
I_{IN}	Input Current[2]				200	μA	V_{IN} = GND or V_{IN} = V_{CC}
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA[3]
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24 mA[3] I_{OL} = 12 mA
Z_{OUT}	Output Impedance			19		Ω	
I_{CCQ}[4]	Maximum Quiescent Supply Current				3.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. Input pull-up / pull-down resistors influence input current.
3. The MPC9443 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines (for V_{CC} =3.3 V) or one 50 Ω series terminated transmission line (for V_{CC} = 2.5 V).
4. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 8. AC Characteristics (V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD} = 3.3 V ± 5%, T_A = –40 to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		350	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output ÷2 output	0 0		350 175	MHz MHz	FSELx = 0 FSELx = 1
V_{PP}	Peak-to-Peak Input Voltage	PCLK0,1	500		1000	mV	LVPECL
V_{CMR}[2]	Common Mode Range	PCLK0,1	1.3		V_{CC} – 0.8	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time				1.0[3]	ns	0.8 to 2.0 V
t_{PLH} t_{PHL} t_{PLH} t_{PHL}	Propagation Delay	PCLK0,1 to any Q PCLK0,1 to any Q CCLK to any Q CCLK to any Q	2.5 2.4 2.1 1.9		5.0 5.2 4.2 4.6	ns ns ns ns	
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
t_S, t_H	Setup, Hold Time (reference clock to CLK_STOP)		500			ps	
$t_{sk(LH, HL)}$	Output-to-Output Skew[4]	Within one bank Any output, same output divider Any output, any output divider			125 225 250	ps ps ps	
$t_{sk(PP)}$	Device-to-Device Skew (LH)[5] Device-to-Device Skew (LH, HL)[6]	Using PCLK0,1 Using CCLK Using PCLK0,1 Using CCLK			2.5 2.1 2.8 2.7	ns ns ns ns	
$t_{SK(P)}$	Output Pulse Skew[7]	Using PCLK0,1 Using CCLK			300 400	ps ps	DC_{REF} = 50%
DC_Q	Output Duty Cycle	f_Q<140 MHz and using CCLK f_Q<250 MHz and using PCLK0,1	45 45	50 50	55 55	% %	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification.
3. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
4. $t_{sk(LH, HL)}$ includes both device skew referenced to the rising output edge and device skew referenced to the falling output edge.
5. Device-to-device skew referenced to the rising output edge.
6. Device-to-device skew referenced to the rising output edge or referenced to the falling output edge.
7. Output pulse skew is the absolute difference of the propagation delay times: | t_{PLH} – t_{PHL} |

Table 9. DC Characteristics (V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD} = 2.5 V ± 5%, T_A = –40 to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage		–0.3		0.7	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage	PCLK0, 1	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK0, 1	1.1		V_{CC} – 0.7	V	LVPECL
I_{IN}	Input Current[2]				200	μA	V_{IN} = GND or V_{IN} = V_{CC}
V_{OH}	Output High Voltage		1.8			V	I_{OH} = –15 mA[3]
V_{OL}	Output Low Voltage				0.6	V	I_{OL} = 15 mA[3]
Z_{OUT}	Output Impedance			22		Ω	
I_{CCQ}[4]	Maximum Quiescent Supply Current				3.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. Input pull-up / pull-down resistors influence input current.
3. The MPC9443 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to one 50 Ω series terminated transmission line at V_{CC} =2.5 V.
4. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 10. AC Characteristics (V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = V_{CCD} = 2.5 V ± 5%, T_A = –40 to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		350	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output	0		350	MHz	FSELx = 0
		÷2 output	0		175	MHz	FSELx = 1
V_{PP}	Peak-to-Peak Input Voltage	PCLK0,1	500		1000	mV	LVPECL
V_{CMR}[2]	Common Mode Range	PCLK0,1	1.3		V_{CC} – 0.7	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time				1.0[3]	ns	0.8 to 2.0 V
t_{PLH}	Propagation Delay	PCLK0,1 to any Q	2.5		6.0	ns	
t_{PHL}		PCLK0,1 to any Q	2.4		6.2	ns	
t_{PLH}		CCLK to any Q	2.1		5.3	ns	
t_{PHL}		CCLK to any Q	1.9		5.5	ns	
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
t_S, t_H	Setup, Hold Time (reference clock to CLK_STOP)		500			ps	
$t_{sk(LH, HL)}$	Output-to-Output Skew[4]	Within one bank			125	ps	
		Any output, same output divider			225	ps	
		Any output, any output divider			250	ps	
$t_{sk(PP)}$	Device-to-Device Skew (LH)[5]	Using PCLK0,1			3.2	ns	
		Using CCLK			3.1	ns	
	Device-to-Device Skew (LH, HL)[6]	Using PCLK0,1			3.5	ns	
		Using CCLK			3.4	ns	
$t_{SK(P)}$	Output Pulse Skew[7]	Using PCLK0,1			300	ps	DC_{REF} = 50%
		Using CCLK			400	ps	
DC_Q	Output Duty Cycle	f_Q<140 MHz and using CCLK	45	50	55	%	
		f_Q<140 MHz and using PCLK0,1	45	50	55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification.
3. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
4. $t_{sk(LH, HL)}$ includes both device skew referenced to the rising output edge and device skew referenced to the falling output edge.
5. Device-to-device skew referenced to the rising output edge.
6. Device-to-device skew referenced to the rising output edge or referenced to the falling output edge.
7. Output pulse skew is the absolute difference of the propagation delay times: | t_{PLH} – t_{PHL} |

Table 11. DC Characteristics (V_{CC} = 3.3 V ± 5%, any $V_{CCA,B,C,D}$ = 2.5 V ± 5% or 3.3 V ± 5% (mixed), T_A = –40 to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage		–0.3		0.8	V	LVCMOS
I_{IN}	Input Current[1]				200	μA	
V_{OH}	Output High Voltage	2.5 V output 3.3 V output	1.7 2.0			V	I_{OH} = –15 mA[2] I_{OH} = 24 mA[2]
V_{OL}	Output Low Voltage	2.5 V output 3.3 V output			0.6 0.55	V	I_{OL} = 15 mA[2] I_{OL} = 24 mA[2]
V_{PP}	Peak-to-Peak Input Voltage	PCLK0,1	250			mV	LVPECL
V_{CMR}[3]	Common Mode Range	PCLK0, 1	1.1		V_{CC} – 0.6	V	LVPECL
Z_{OUT}	Output Impedance	2.5 V output 3.3 V output		22 19		Ω Ω	
C_{PD}	Power Dissipation Capacitance			10		pF	Per Output
I_{CCQ}[4]	Maximum Quiescent Supply Current				3.0	mA	All V_{CC} Pins

1. Input pull-up / pull-down resistors influence input current.
2. The MPC9443 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines (for V_{CC} = 3.3 V) or one 50 Ω series terminated transmission line (for V_{CC} =2.5 V).
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
4. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 12. AC Characteristics (V_{CC} = 3.3 V ± 5%, any $V_{CCA,B,C,D}$ = 2.5 V ± 5% or 3.3 V ± 5% (mixed), T_A = –40 to +85°C)[1 2]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
$t_{sk(LH, HL)}$	Output-to-Output Skew[3] Any output, same output divider Any output, any output divider				 275 350	 ps ps	
$t_{sk(PP)}$	Device-to-Device Skew		See Table 8 (3.3 V AC Characteristics)				
$t_{PLH, HL}$	Propagation Delay		See Table 8 (3.3 V AC Characteristics)				
$t_{SK(P)}$	Output Pulse Skew[4]	Using PCLK0,1 Using CCLK			400 500	ps ps	DC_{REF} = 50%
DC_Q	Output Duty Cycle	f_Q<140 MHz and using CCLK f_Q<250 MHz and using PCLK0,1	45 45	50 50	55 55	% %	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. This table only specifies AC parameter in mixed voltage supply conditions that vary from the corresponding AC tables. For all other parameters, see Table 8 (for 3.3 V outputs) or Table 10 (for 2.5 V outputs)
3. $t_{sk(LH, HL)}$ includes both device skew referenced to the rising output edge and device skew referenced to the falling output edge.
4. Output pulse skew is the absolute difference of the propagation delay times: | t_{PLH} – t_{PHL} |

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC9443 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines at V_{CC} = 3.3 V. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9443 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9443 clock driver is effectively doubled due to its capability to drive multiple lines (at V_{CC} = 3.3 V).

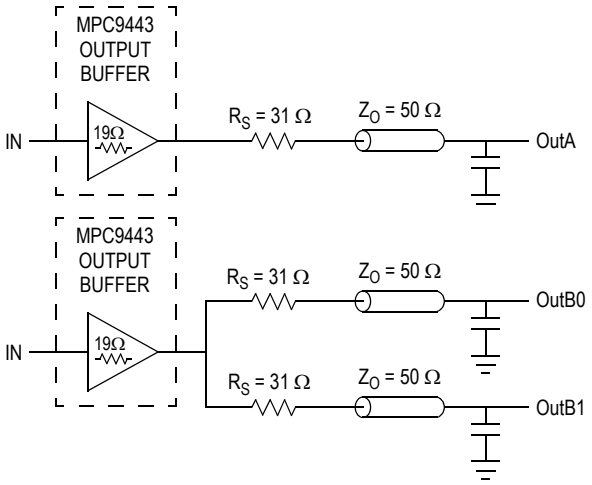


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4. Single versus Dual Waveforms show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9443 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9443. The output waveform in Figure 4. Single versus Dual Waveforms shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 31 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 31\ \Omega \parallel 31\ \Omega$$
$$R_0 = 19\ \Omega$$
$$V_L = 3.0\ (25 \div (15.5 + 19 + 25)$$
$$= 1.26V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.52 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

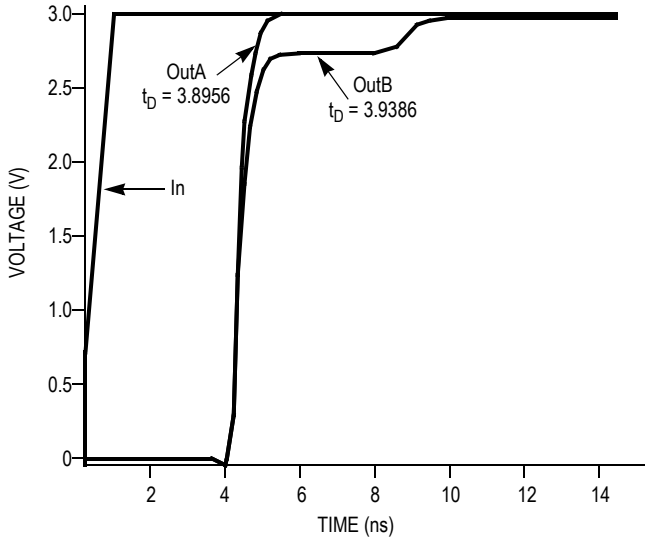
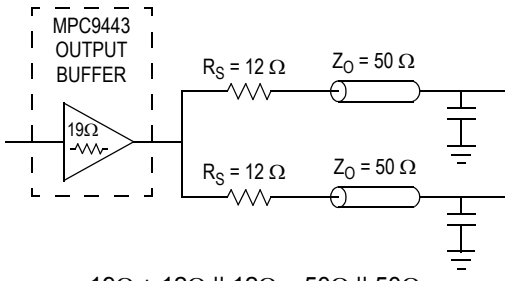


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5. Optimized Dual Line Termination should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



19Ω + 12Ω || 12Ω = 50Ω || 50Ω
25Ω = 25Ω

Figure 5. Optimized Dual Line Termination

Power Consumption of the MPC9443 and Thermal Management

The MPC9443 AC specification is guaranteed for the entire operating frequency range up to 350 MHz. The MPC9443 power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC9443 die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature.

Table 13. Die Junction Temperature and MTFBF

Junction Temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC9443 needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC9443 is represented in Equation 1.

Where I_{CCQ} is the static current consumption of the MPC9443, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 16 in case of the MPC9443). The MPC9443 supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from Equation 1. Using parallel termination output termination results in Equation 2 for power dissipation.

In Equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL}, I_{OL}, V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in Equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature ($T_{J)}$ as a function of the power consumption.

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 13, the junction temperature can be used to estimate the long-term device reliability. Further, combining Equation 1 and Equation 2 results in a maximum operating frequency for the MPC9443 in a series terminated transmission line system.

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 13. R_{thja} can be derived from Table 14. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

Table 14. Thermal Package Impedance of the 48 ld LQFP

Convection, LFPM	R_{thja} (1P2S board), K/W	R_{thja} (2P2S board), K/W
Still air	69	53
100 lfpm		
200 lfpm	64	50
300 lfpm		
400 lfpm		
500 lfpm		

If the calculated maximum frequency is below 250 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the MPC9443. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to an estimated MTBF of 9.1 years (4 years), a supply voltage of 3.3 V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \quad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \quad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \quad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V^2_{CC}} \cdot \left[\frac{T_{j,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \quad \text{Equation 4}$$

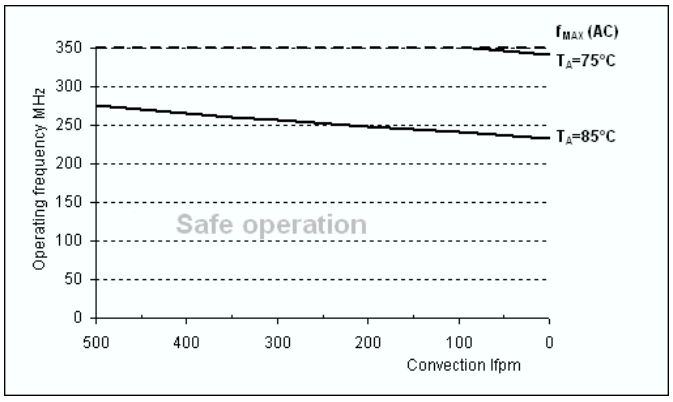


Figure 6. Maximum MPC9443 frequency, V_{CC} = 3.3 V, MTBF 9.1 Years, Driving Series Terminated Transmission Lines

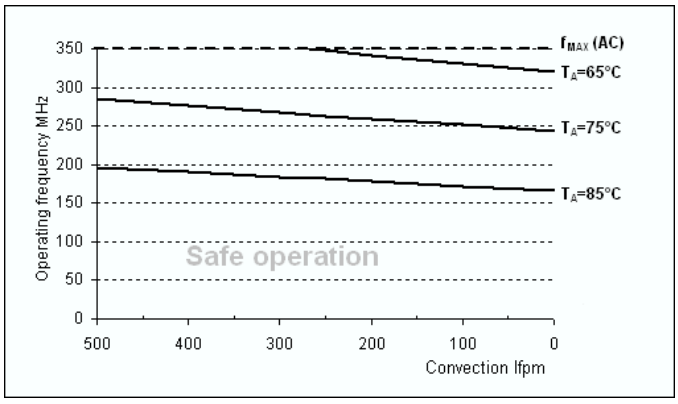


Figure 7. Maximum MPC9443 Frequency, V_{CC} = 3.3 V, MTBF 9.1 Years, 4 pF Load per Line

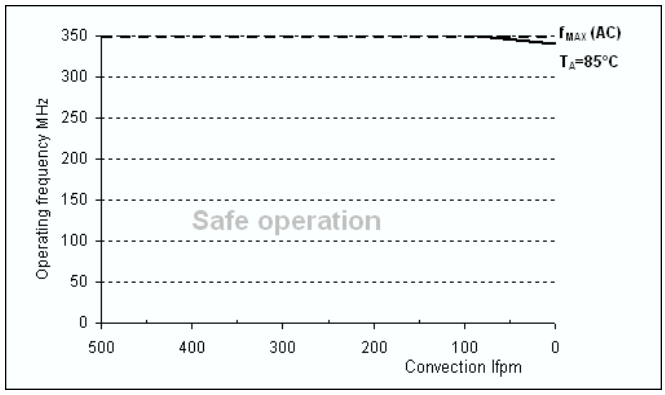


Figure 8. Maximum MPC9443 Frequency, V_{CC} = 3.3 V, MTBF 4 Years, Driving Series Terminated Transmission Lines

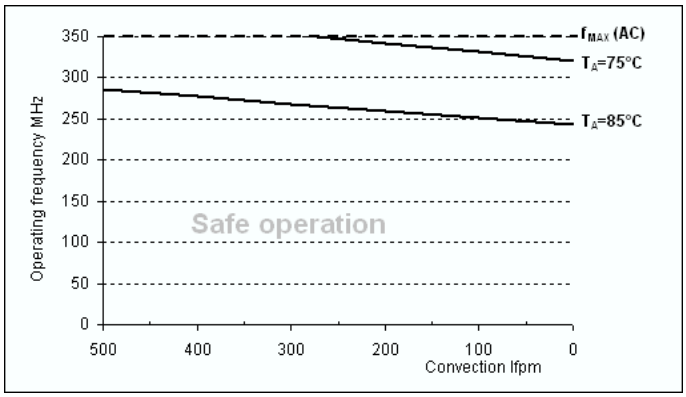


Figure 9. Maximum MPC9443 Frequency, V_{CC} = 3.3 V, MTBF 4 Years, 4 pF Load per Line

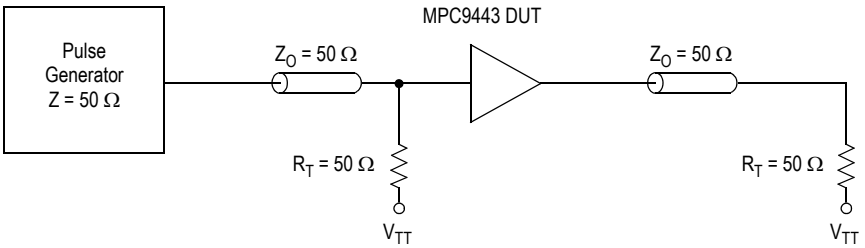


Figure 10. CCLK MPC9443 AC Test Reference for V_{cc} = 3.3 V and V_{cc} = 2.5 V

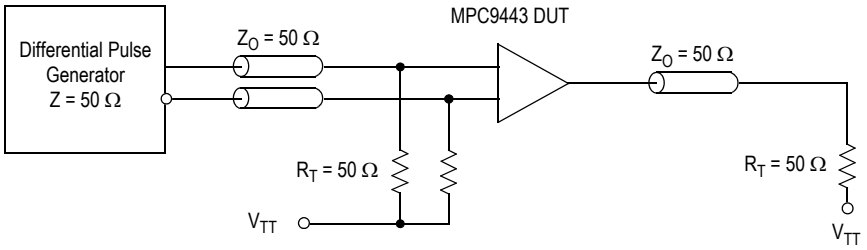


Figure 11. PCLK MPC9443 AC Test Reference

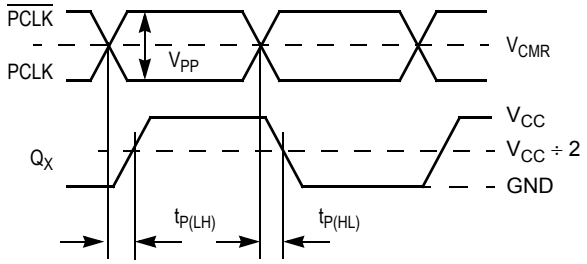


Figure 12. Propagation Delay (t_{PD}) Test Reference

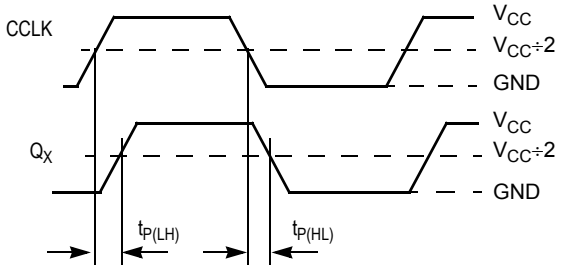
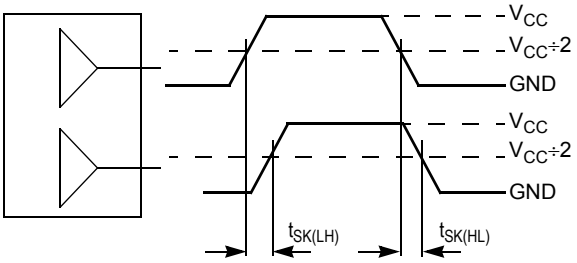
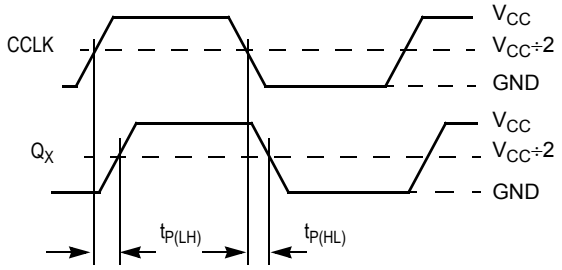


Figure 13. Propagation Delay (t_{PD}) Test Reference



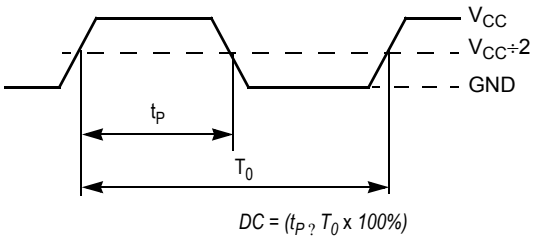
The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 14. Output-to-Output Skew $t_{SK(LH, HL)}$



$t_{SK(P)} = | t_{PLH} - t_{PHL} |$

Figure 15. Output Pulse Skew ($t_{SK(P)}$) Test Reference



The time from the PLL controlled edge to the non-controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 16. Output Duty Cycle (DC)

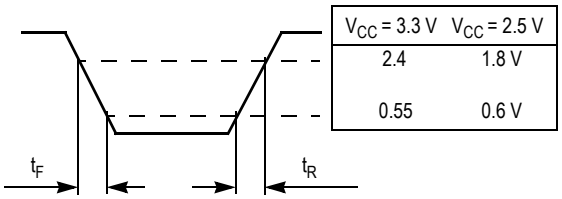
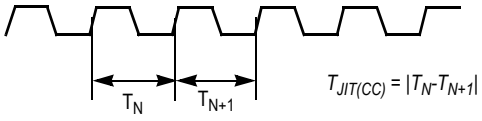


Figure 17. Output Transition Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 18. Cycle-to-Cycle Jitter

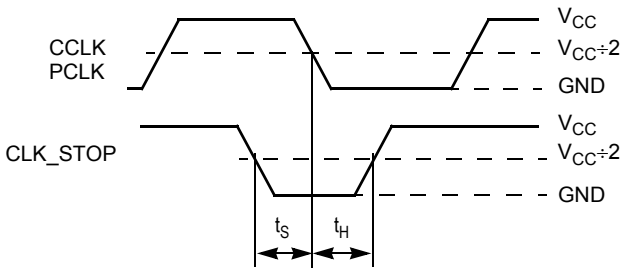


Figure 19. Setup and Hold Time (t_S, t_H) Test Reference

Order number: MPC9446
Rev 2, 08/2004

2.5V and 3.3V LVCMOS Clock Fanout Buffer

MPC9446

LOW VOLTAGE SINGLE OR DUAL SUPPLY 2.5V AND 3.3V LVCMOS CLOCK DISTRIBUTION BUFFER

FA SUFFIX
LQFP PACKAGE
CASE 873A-03

The MPC9446 is a 2.5V and 3.3V compatible 1:10 clock distribution buffer designed for low-voltage mid-range to high-performance telecom, networking and computing applications. Both 3.3V, 2.5V and dual supply voltages are supported for mixed-voltage applications. The MPC9446 offers 10 low-skew outputs and 2 selectable inputs for clock redundancy. The outputs are configurable and support 1:1 and 1:2 output to input frequency ratios. The MPC9446 is specified for the extended temperature range of –40°C to 85°C.

Features

- Configurable 10 outputs LVCMOS clock distribution buffer
- Compatible to single, dual and mixed 3.3V/2.5V voltage supply
- Wide range output clock frequency up to 250 MHz
- Designed for mid-range to high-performance telecom, networking and computer applications
- Supports applications requiring clock redundancy
- Maximum output skew of 200 ps (150 ps within one bank)
- Selectable output configurations per output bank
- Tristable outputs
- 32-lead LQFP package
- 32-lead Pb-free Package Available
- Ambient operating temperature range of –40 to 85°C

Functional Description

The MPC9446 is a full static fanout buffer design supporting clock frequencies up to 250 MHz. The signals are generated and retimed on-chip to ensure minimal skew between the three output banks. Two independent LVCMOS compatible clock inputs are available. This feature supports redundant clock sources or the addition of a test clock into the system design. Each of the three output banks can be individually supplied by 2.5V or 3.3V supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the three output banks. The MPC9446 can be reset and the outputs are disabled by deasserting the MR/$\overline{OE}$ pin (logic high state). Asserting MR/$\overline{OE}$ will enable the outputs.

All inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. Please consult the MPC9456 specification for a 1:10 mixed voltage buffer with LVPECL compatible inputs. For series terminated transmission lines, each of the MPC9446 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

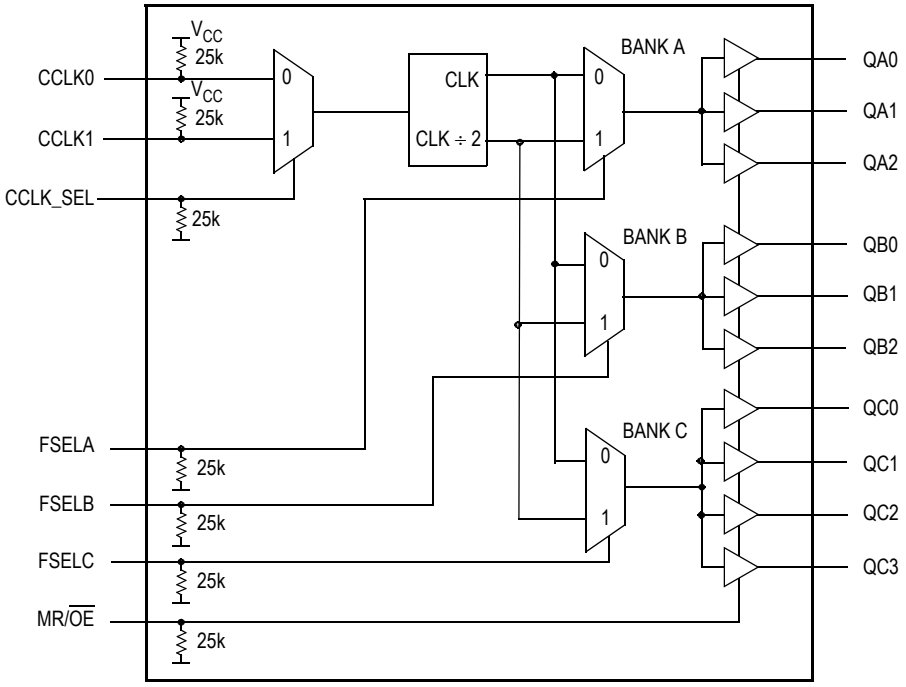


Figure 1. MPC9446 Logic Diagram

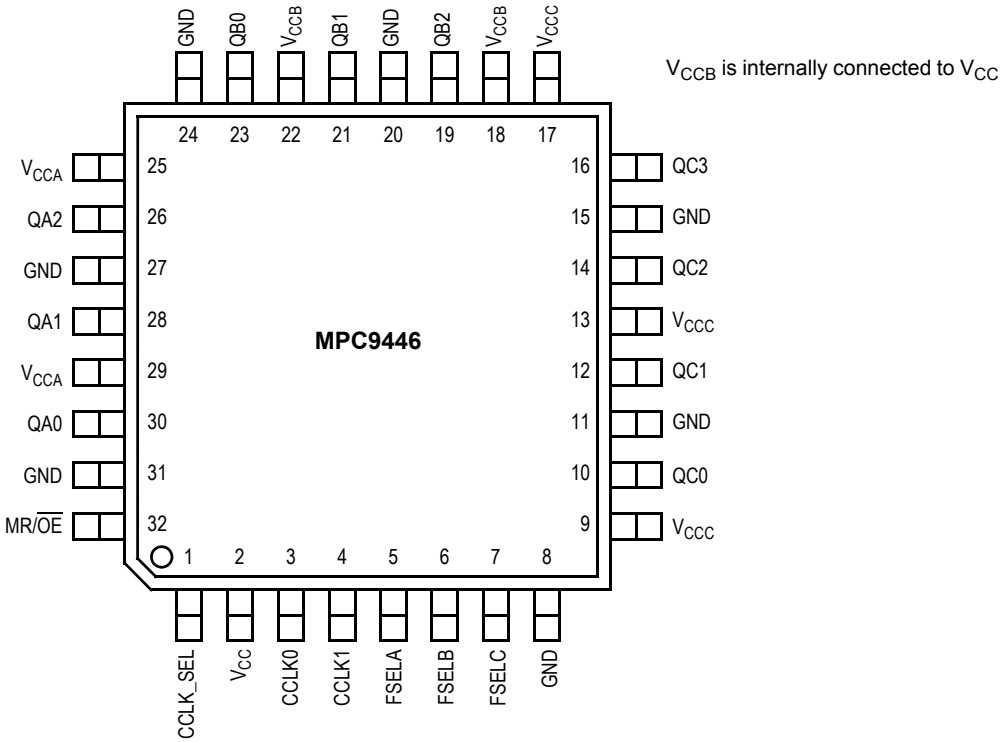


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CCLK0,1	Input	LVCMOS	LVCMOS clock inputs
FSELA, FSELB, FSELC	Input	LVCMOS	Output bank divide select input
MR/$\overline{OE}$	Input	LVCMOS	Internal reset and output (high impedance) control
GND		Supply	Negative voltage supply (GND)
V_{CCA}, V_{CCB}[1], V_{CCC}		Supply	Positive voltage supply for output banks
V_{CC}		Supply	Positive voltage supply for core (VCC)
QA0 – QA2	Output	LVCMOS	Bank A outputs
QB0 – QB2	Output	LVCMOS	Bank B outputs
QC0 – QC3	Output	LVCMOS	Bank C outputs

1. V_{CCB} is internally connected to V_{CC}.

Table 2. Supported Single and Dual Supply Configurations

Supply Voltage Configuration	V_{CC}[1]	V_{CCA}[2]	V_{CCB}[3]	V_{CCC}[4]	GND
3.3V	3.3V	3.3V	3.3V	3.3V	0V
Mixed Voltage Supply	3.3V	3.3V or 2.5V	3.3V	3.3V or 2.5V	0 V
2.5V	2.5V	2.5V	2.5V	2.5V	0 V

1. V_{CC} is the positive power supply of the device core and input circuitry. V_{CC} voltage defines the input threshold and levels.
2. V_{CCA} is the positive power supply of the bank A outputs. V_{CCA} voltage defines bank A output levels.
3. V_{CCB} is the positive power supply of the bank B outputs. V_{CCB} voltage defines bank B output levels. V_{CCB} is internally connected to V_{CC}.
4. V_{CCC} is the positive power supply of the bank C outputs. V_{CCC} voltage defines bank C output levels.

Table 3. Function Table (Controls)

Control	Default	0	1
CCLK_SEL	0	CCLK0	CCLK1
FSELA	0	$f_{QA0:2} = f_{REF}$	$f_{QA0:2} = f_{REF} \div 2$
FSELB	0	$f_{QB0:2} = f_{REF}$	$f_{QB0:2} = f_{REF} \div 2$
FSELC	0	$f_{QC0:3} = f_{REF}$	$f_{QC0:3} = f_{REF} \div 2$
MR/$\overline{OE}$	0	Outputs enabled	Internal reset outputs disabled (tristate)

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	

Table 6. DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 3.3V \pm 5\%$, $T_A = –40°C$ to $+85°C$)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	–0.3		0.8	V	LVCMOS
I_{IN}	Input Current[1]			200	μA	V_{IN} = GND or V_{IN} = VCC
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA[2]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24mA[2] I_{OL} = 12mA
Z_{OUT}	Output Impedance		14 – 17		Ω	
I_{CCQ}[3]	Maximum Quiescent Supply Current			2.0	mA	All V_{CC} Pins

1. Input pull-up / pull-down resistors influence input current.
2. The MPC9446 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
3. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 7. AC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 3.3V \pm 5\%$, $T_A = –40°C$ to $+85°C$)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		250[2]	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output ÷2 output	0 0		250[2] 125	MHz MHz	FSELx = 0 FSELx = 1
$t_{P, REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time				1.0[3]	ns	0.8 to 2.0V
t_{PLH} t_{PHL}	Propagation Delay	CCLK0,1 to any Q CCLK0,1 to any Q	2.2 2.2	2.8 2.8	4.45 4.2	ns ns	
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{sk(O)}$	Output-to-Output Skew	Within one bank Any output bank, same output divider Any output, Any output divider			150 200 350	ps ps ps	
$t_{sk(PP)}$	Device-to-Device Skew				2.25	ns	
$t_{SK(P)}$	Output Pulse Skew[4]				200	ps	
DC_Q	Output Duty Cycle	÷1 output ÷2 output	47 45	50 50	53 55	% %	DC_{REF} = 50% DC_{REF} = 25%–75%
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. The MPC9446 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.
3. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
4. Output pulse skew is the absolute difference of the propagation delay times: $| t_{pLH} – t_{pHL} |$.

Table 8. DC Characteristics (V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 2.5V ± 5%, T_A = –40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	–0.3		0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.8			V	I_{OH} = –15 mA[1]
V_{OL}	Output Low Voltage			0.6	V	I_{OL} = 15 mA
Z_{OUT}	Output Impedance		17 – 20[2]		Ω	
I_{IN}	Input Current[2]			±200	μA	V_{IN} = GND or V_{IN} = V_{CC}
I_{CCQ}[3]	Maximum Quiescent Supply Current			2.0	mA	All V_{CC} Pins

1. The MPC9446 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.
2. Input pull-up / pull-down resistors influence input current.
3. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 9. AC Characteristics (V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 2.5V ± 5%, T_A = –40°C to +85°C)[1] [2]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		250[3]	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output	0		250[3]	MHz	FSELx = 0
		÷2 output	0		125	MHz	FSELx = 1
$t_{P, REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time				1.0[4]	ns	0.7 to 1.7V
t_{PLH}	Propagation Delay	CCLK0,1 to any Q	2.6		5.6	ns	
t_{PHL}		CCLK0,1 to any Q	2.6		5.5	ns	
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{sk(O)}$	Output-to-Output Skew	Within one bank			150	ps	
		Any output bank, same output divider			200	ps	
		Any output, Any output divider			350	ps	
$t_{sk(PP)}$	Device-to-Device Skew				3.0	ns	
$t_{SK(P)}$	Output Pulse Skew[5]				200	ps	
			45	50			DC_{REF} = 50%
DC_Q	Output Duty Cycle	÷1 or ÷2 output			55	%	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8V

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. AC specifications are design targets, final specification is pending device characterization.
3. The MPC9446 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.
4. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
5. Output pulse skew is the absolute difference of the propagation delay times: | t_{pLH} – t_{pHL} |.

Table 10. AC Characteristics (V_{CC} = 3.3V + 5%, V_{CCA}, V_{CCB}, V_{CCC} = 2.5 V + 5% or 3.3 V + 5%, T_A = –40°C to +85°C)[1] [2]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
$t_{sk(O)}$	Output-to-Output Skew	Within one bank			150	ps	
		Any output bank, same output divider			250	ps	
		Any output, Any output divider			350	ps	
$t_{sk(PP)}$	Device-to-Device Skew				2.5	ns	
$t_{PLH,HL}$	Propagation Delay	CCLK0,1 to any Q	See 3.3V Table				
$t_{SK(P)}$	Output Pulse Skew[3]				250	ps	
			45	50			DC_{REF} = 50%
DC_Q	Output Duty Cycle	÷1 or ÷2 output			55	%	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. For all other AC specifications, refer to 2.5V or 3.3V tables according to the supply voltage of the output bank.
3. Output pulse skew is the absolute difference of the propagation delay times: | t_{PLH} – t_{PHL} |.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC9446 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9446 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9446 clock driver is effectively doubled due to its capability to drive multiple lines.

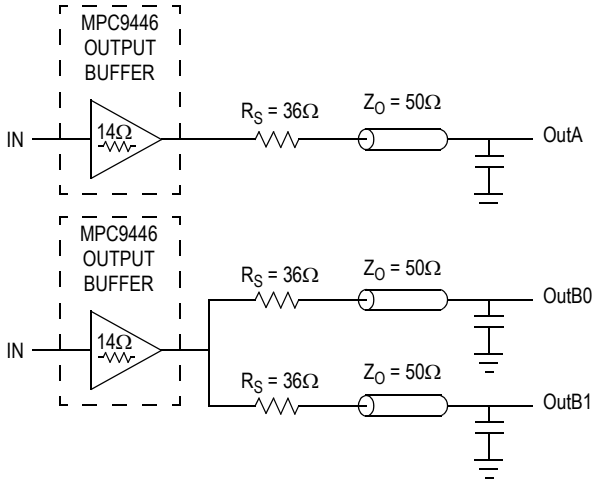


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9446 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9446. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 36\Omega \parallel 36\Omega$$
$$R_0 = 14\Omega$$
$$V_L = 3.0 (25 \div (18 + 14 + 25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

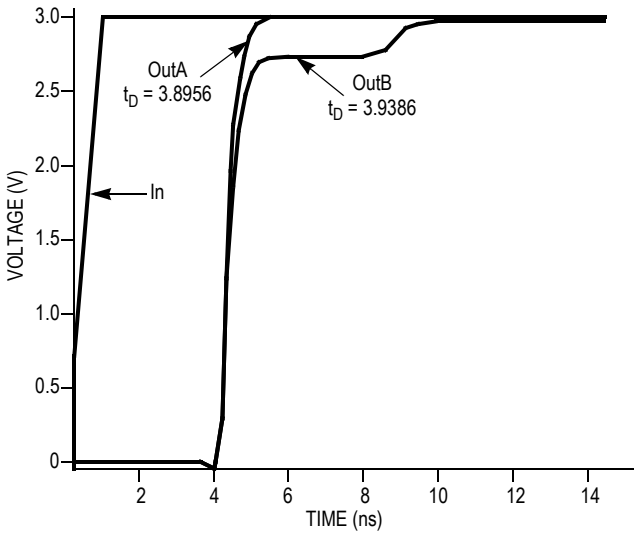


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

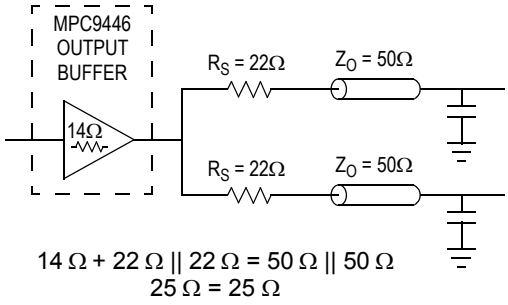


Figure 5. Optimized Dual Line Termination

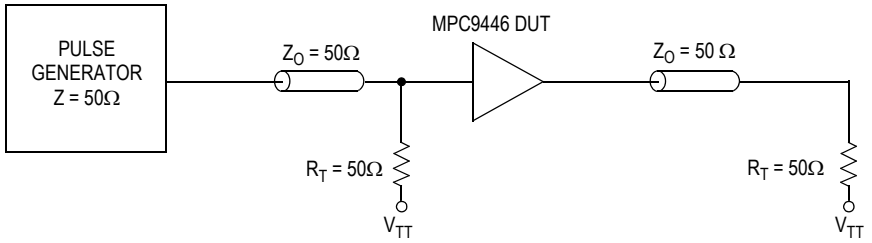


Figure 6. CCLK0, 1 MPC9446 AC Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

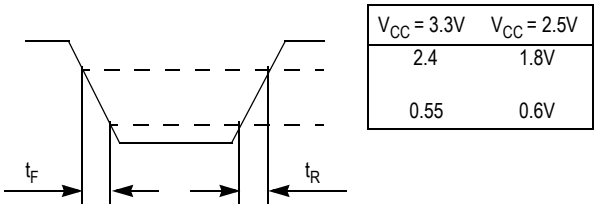


Figure 7. Output Transition Time Test Reference

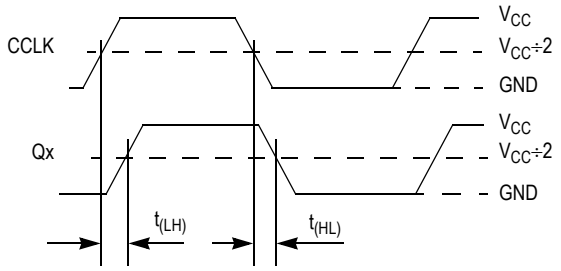
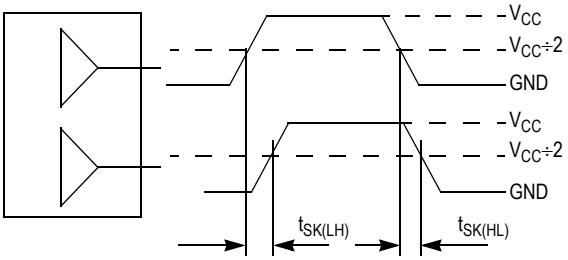
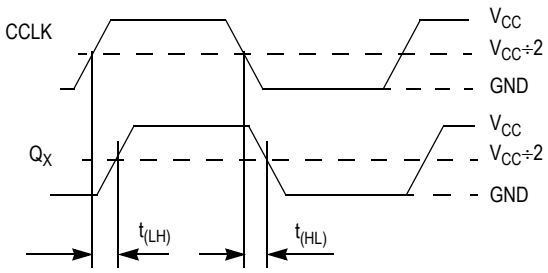


Figure 8. Propagation Delay (t_{PD}) Test Reference



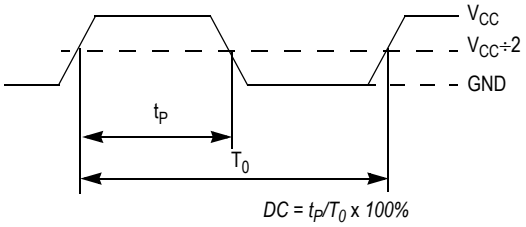
The pin-to-pin skew is defined as the worst case difference in propagation delay between any two similar delay paths within a single device

Figure 9. Output-to-Output Skew $t_{SK(LH, HL)}$



$t_{SK(P)} = | t_{PLH} - t_{PHL} |$

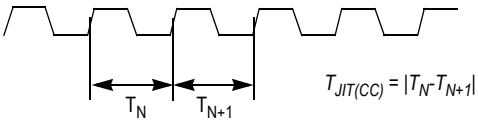
Figure 10. Output Pulse Skew ($t_{SK(P)}$) Test Reference



DC = t_P/T_0 x 100%

The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 11. Output Duty Cycle (DC)



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 12. Cycle-to-Cycle Jitter

Order number: MPC9447
Rev 3, 08/2004

3.3 V/2.5 V 1:9 LVCMOS Clock Fanout Buffer

MPC9447

LOW VOLTAGE
3.3 V/2.5 V LVCMOS 1:9
CLOCK FANOUT BUFFER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MPC9447 is a 3.3V or 2.5V compatible, 1:9 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 350 MHz and output skews less than 150 ps, the device meets the needs of most demanding clock applications.

Features

- 9 LVCMOS Compatible Clock Outputs
- 2 Selectable, LVCMOS Compatible Inputs
- Maximum Clock Frequency of 350 MHz
- Maximum Clock Skew of 150 ps
- Synchronous Output Stop in Logic Low State Eliminates Output Runt Pulses
- High-Impedance Output Control
- 3.3V or 2.5V Power Supply
- Drives up to 18 Series Terminated Clock Lines
- Ambient Temperature Range -40°C to +85°C
- 32-Lead LQFP Packaging
- 32-lead Pb-free Package Available
- Supports Clock Distribution in Networking, Telecommunications, and Computer Applications
- Pin and Function Compatible to MPC947

Functional Description

MPC9447 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 350 MHz. Each output provides a precise copy of the input signal with a near zero skew. The outputs buffers support driving of 50Ω terminated transmission lines on the incident edge: each is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable independent LVCMOS compatible clock inputs are available, providing support of redundant clock source systems. The MPC9447 CLK_STOP control is synchronous to the falling edge of the input clock. It allows the start and stop of the output clock signal only in a logic low state, thus eliminating potential output runt pulses. Applying the OE control will force the outputs into high-impedance mode.

All inputs have an internal pull-up or pull-down resistor preventing unused and open inputs from floating. The device supports a 2.5V or 3.3V power supply and an ambient temperature range of -40°C to +85°C. The MPC9447 is pin and function compatible but performance-enhanced to the MPC947.

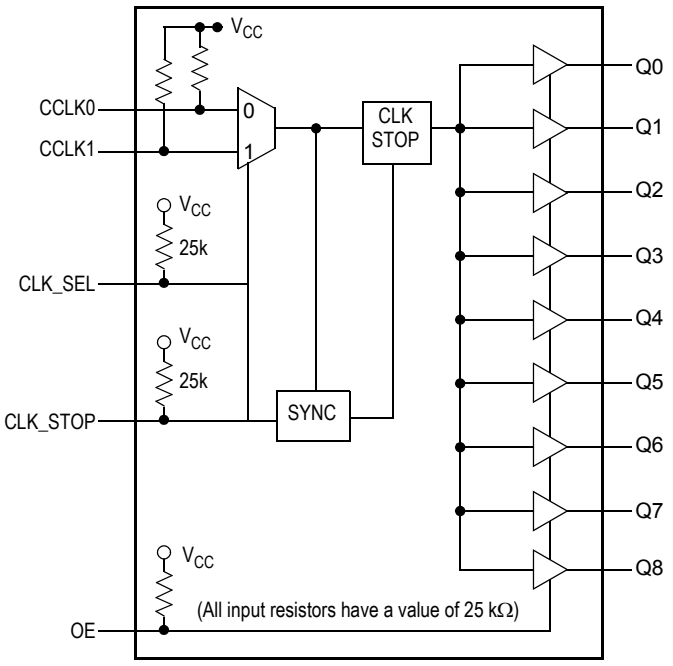


Figure 1. Logic Diagram

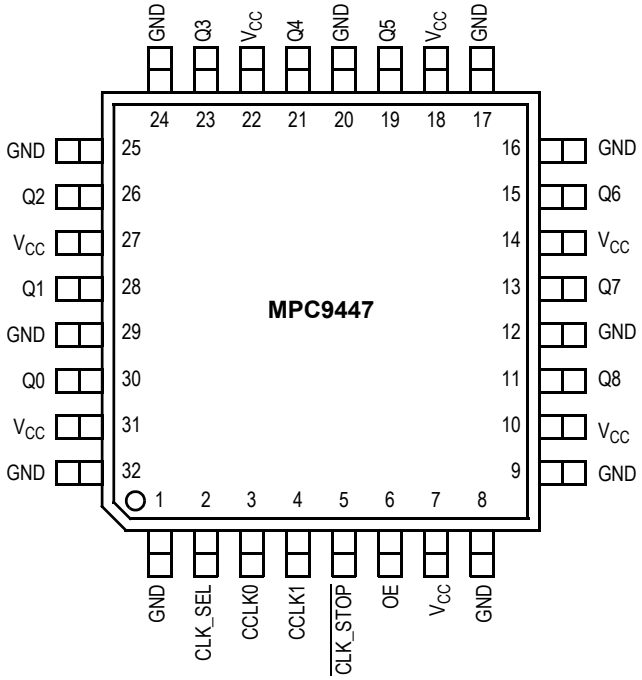


Figure 2. 32-Lead Pinout (Top View)

Table 1. Function Table

Control	Default	0	1
CLK_SEL	1	CLK0 input selected	CLK1 input selected
OE	1	Outputs disabled (high-impedance state)[1]	Outputs enabled
$\overline{\text{CLK\_STOP}}$	1	Outputs synchronously stopped in logic low state	Outputs active

1. OE = 0 will high-impedance tristate all outputs independent on $\overline{\text{CLK\_STOP}}$

Table 2. Pin Configurations

Pin	I/O	Type	Function
CCLK0	Input	LVCMOS	Clock Signal Input
CCLK1	Input	LVCMOS	Alternative Clock Signal Input
CLK_SEL	Input	LVCMOS	Clock Input Select
$\overline{\text{CLK\_STOP}}$	Input	LVCMOS	Clock Output Enable/Disable
OE	Input	LVCMOS	Output Enable/Disable (high-impedance tristate)
Q0–8	Output	LVCMOS	Clock Outputs
GND	Supply	Ground	Negative Power Supply (GND)
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
LU	Latch-up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	–0.3		0.8	V	LVCMOS
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –24 mA[1]
V_{OL}	Output Low Voltage			0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance		17		Ω	
I_{IN}	Input Current[2]			±300	µA	V_{IN} = V_{CC} or GND
I_{CCQ}	Maximum Quiescent Supply Current[3]			2.0	mA	All V_{CC} Pins

1. The MPC9447 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines (for V_{CC} = 3.3V).
2. Inputs have pull-down or pull-up resistors affecting the input current.
3. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 6. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40°C to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		350	MHz	
f_{max}	Output Frequency		0		350	MHz	
$f_{P,REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	CCLK0, CCLK1 Input Rise/Fall Time				1.0[2]	ns	0.8 to 2.0 V
$t_{PLH/HL}$	Propagation Delay	CCLK0 or CCLK1 to any Q	1.3		3.3	ns	
$t_{PLZ, HZ}$	Output Disable Time				11	ns	
$t_{PZL, ZH}$	Output Enable Time				11	ns	
t_S	Setup Time	CCLK0 or CCLK1 to CLK_STOP[3]	0.0			ns	
t_H	Hold Time	CCLK0 or CCLK1 to CLK_STOP[3]	1.0			ns	
$t_{sk(O)}$	Output-to-Output Skew				150	ps	
$t_{sk(PP)}$	Device-to-Device Skew				2.0	ns	
$t_{SK(P)}$ DC_Q	Output Pulse Skew[4] Output Duty Cycle	 f_Q<170 MHz	 45	 50	300 55	ps %	 DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4 V
$t_{JIT(CC)}$	Cycle-to-cycle jitter	RMS (1 σ)		TBD		ps	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
3. Setup and hold times are referenced to the falling edge of the selected clock signal input.
4. Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

Table 7. DC Characteristics (V_{CC} = 2.5V ± 5%, T_A = -40°C to +85°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage	1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage	–0.3		0.7	V	LVCMOS
V_{OH}	Output High Voltage	1.8			V	I_{OH} = –15 mA[1]
V_{OL}	Output Low Voltage			0.6	V	I_{OL} = 15 mA
Z_{OUT}	Output Impedance		19		Ω	
I_{IN}	Input Current[2]			±300	μA	V_{IN} = V_{CC} or GND
I_{CCQ}	Maximum Quiescent Supply Current[3]			2.0	mA	All V_{CC} Pins

1. The MPC9447 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives one 50Ω series terminated transmission lines per output (V_{CC} = 2.5V).
2. Inputs have pull-down or pull-up resistors affecting the input current.
3. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 8. AC Characteristics (V_{CC} = 2.5V ± 5%, T_A = -40°C to +85°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency	0		350	MHz	
f_{max}	Output Frequency	0		350	MHz	
$f_{P,REF}$	Reference Input Pulse Width	1.4			ns	
t_r, t_f	CCLK0, CCLK1 Input Rise/Fall Time			1.0[2]	ns	0.7 to 1.7V
$t_{PLH/HL}$	Propagation Delay CCLK0 or CCLK1 to any Q	1.7		4.4	ns	
$t_{PLZ, HZ}$	Output Disable Time			11	ns	
$t_{PZL, ZH}$	Output Enable Time			11	ns	
t_S	Setup Time CCLK0 or CCLK1 to CLK_STOP[3]	0.0			ns	
t_H	Hold Time CCLK0 or CCLK1 to CLK_STOP[3]	1.0			ns	
$t_{sk(O)}$	Output-to-Output Skew			150	ps	
$t_{sk(PP)}$	Device-to-Device Skew			2.7	ns	
$t_{SK(P)}$ DC_Q	Ouput Pulse Skew[4] Output Duty Cycle f_Q<350 MHz	 45	50	200 55	ps %	 DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time	0.1		1.0	ns	0.6 to 1.8V
$t_{JIT(CC)}$	Cycle-to-Cycle jitter RMS (1 σ)		TBD		ps	

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
3. Setup and hold times are referenced to the falling edge of the selected clock signal input.
4. Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$

APPLICATION INFORMATION

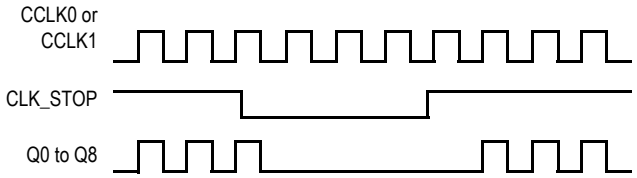


Figure 3. Output Clock Stop (CLK_STOP) Timing Diagram

Driving Transmission Lines

The MPC9447 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of 17Ω (V_{CC}=3.3V), the outputs can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Motorola application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

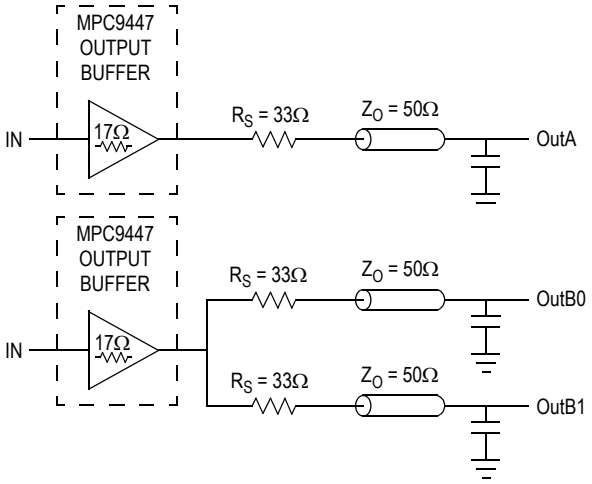


Figure 4. Single versus Dual Transmission Lines

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9447 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 4. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9447 clock driver is effectively doubled due to its capability to drive multiple lines at V_{CC} = 3.3V.

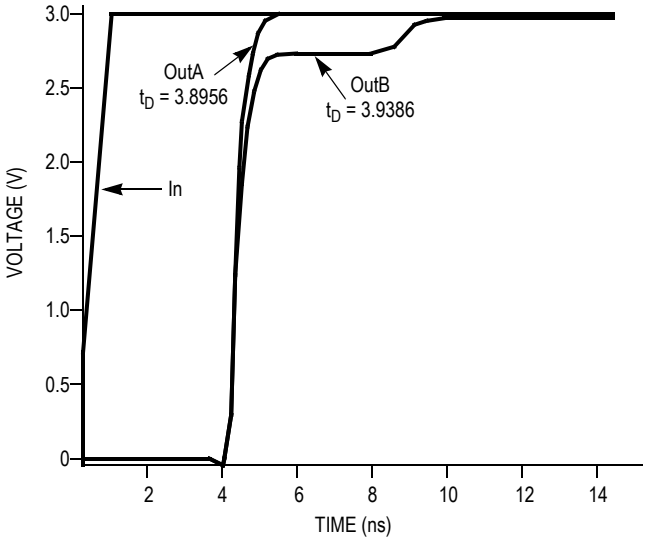


Figure 5. Single versus Dual Line Termination Waveforms

The waveform plots in Figure 5. Single versus Dual Line Termination Waveforms show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9447 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9447. The output waveform in Figure 5. Single versus Dual Line Termination Waveforms shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 33Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 33\Omega \parallel 33\Omega$$
$$R_0 = 17\Omega$$
$$V_L = 3.0 (25 \div (16.5+17+25)$$
$$= 1.28V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 6. Optimized Dual Line Termination should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

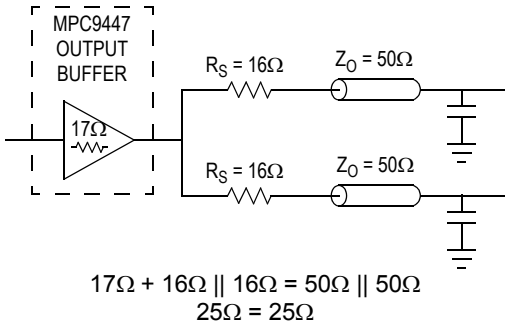


Figure 6. Optimized Dual Line Termination

The Following Figures Illustrate the Measurement Reference for the MPC9447 Clock Driver Circuit

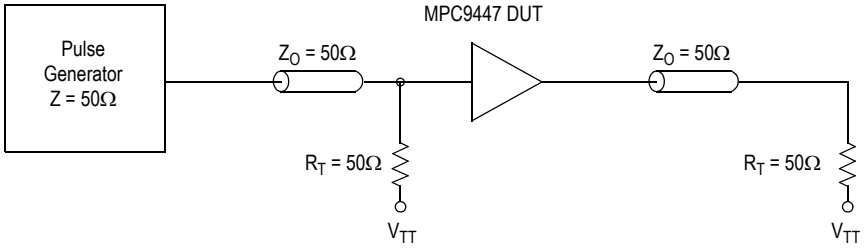


Figure 7. CCLK MPC9447 AC Test Reference for V_{CC} = 3.3V and V_{CC} = 2.5V

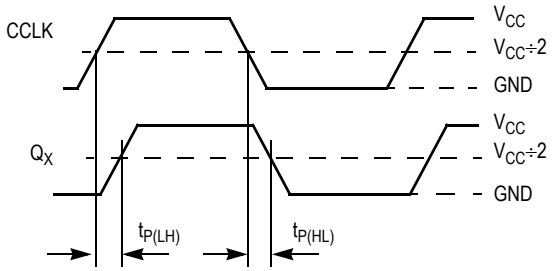
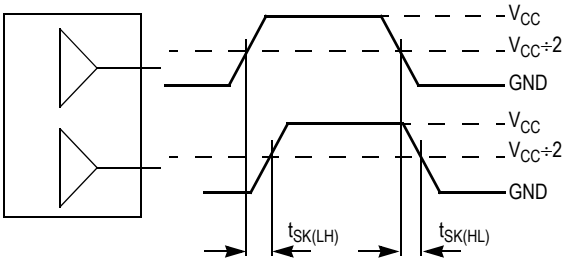


Figure 8. Propagation Delay (t_{PD}) Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 9. Output-to-Output Skew $t_{SK(LH, HL)}$

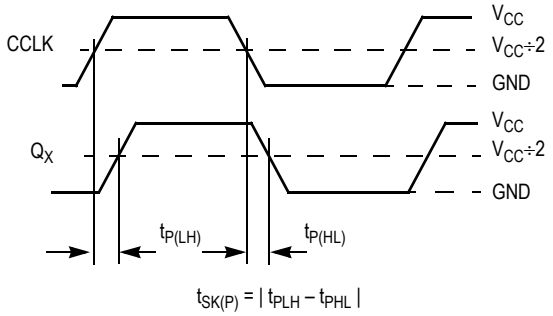
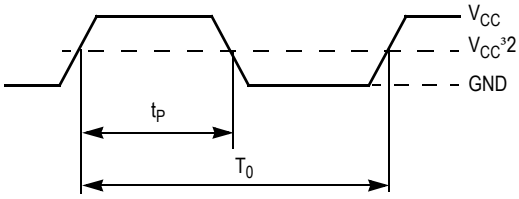


Figure 10. Output Pulse Skew ($t_{SK(P)}$) Test Reference



The time from the output controlled edge to the non-controlled edge, divided by the time between output controlled edges, expressed as a percentage

Figure 11. Output Duty Cycle (DC)

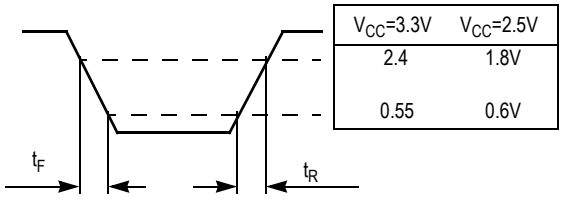
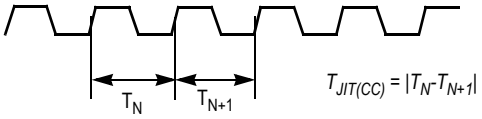


Figure 12. Output Transition Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 13. Cycle-to-Cycle Jitter

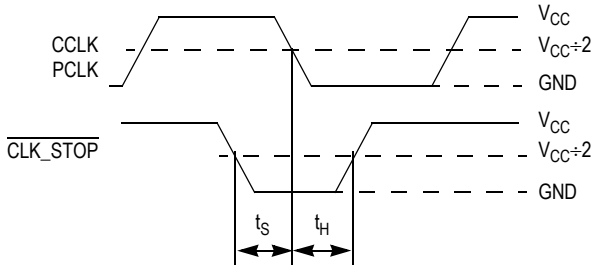


Figure 14. Setup and Hold Time (t_S, t_H) Test Reference

3.3 V/2.5 V LVCMOS 1:12 Clock Fanout Buffer

MPC9448

LOW VOLTAGE
3.3 V/2.5 V LVCMOS 1:12
CLOCK FANOUT BUFFER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

he MPC9448 is a 3.3V or 2.5V compatible, 1:12 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 350 MHz and output skews less than 150 ps, the device meets the needs of most demanding clock applications.

Features

- 12 LVCMOS compatible clock outputs
- Selectable LVCMOS and differential LVPECL compatible clock inputs
- Maximum clock frequency of 350 MHz
- Maximum clock skew of 150 ps
- Synchronous output stop in logic low state eliminates output runt pulses
- High-impedance output control
- 3.3V or 2.5V power supply
- Drives up to 24 series terminated clock lines
- Ambient temperature range -40°C to +85°C
- 32-Lead LQFP packaging
- 32-lead Pb-free package available
- Supports clock distribution in networking, telecommunication and computing applications
- Pin and function compatible to MPC948

Functional Description

The MPC9448 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 350 MHz. Each output provides a precise copy of the input signal with a near zero skew. The outputs buffers support driving of 50Ω terminated transmission lines on the incident edge: each output is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable, independent clock inputs are available, providing support of LVCMOS and differential LVPECL clock distribution systems. The MPC9448 $\overline{\text{CLK\_STOP}}$ control is synchronous to the falling edge of the input clock. It allows the start and stop of the output clock signal only in a logic low state, thus eliminating potential output runt pulses. Applying the OE control will force the outputs into high-impedance mode.

All inputs have an internal pull-up or pull-down resistor preventing unused and open inputs from floating. The device supports a 2.5V or 3.3V power supply and an ambient temperature range of -40°C to +85°C. The MPC9448 is pin and function compatible but performance-enhanced to the MPC948.

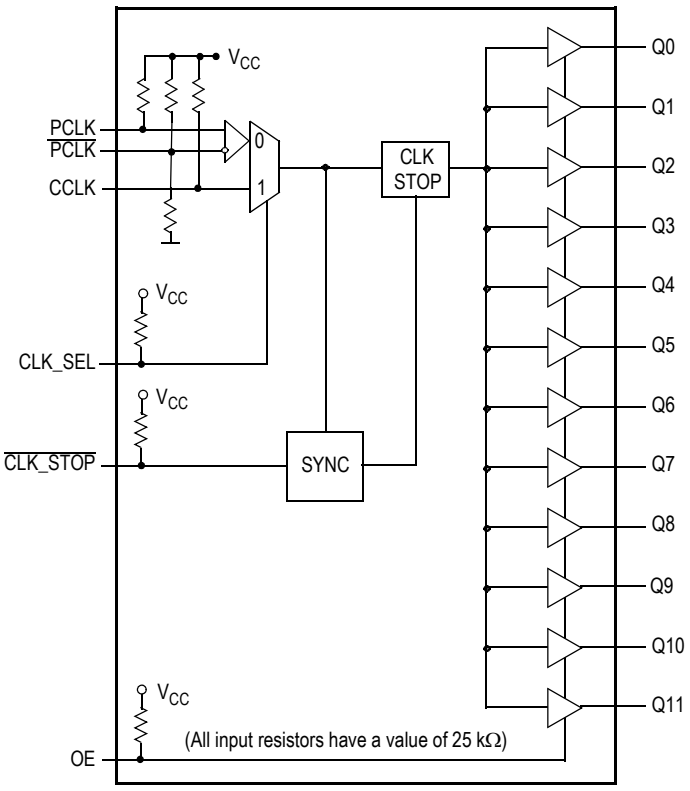


Figure 1. Logic Diagram

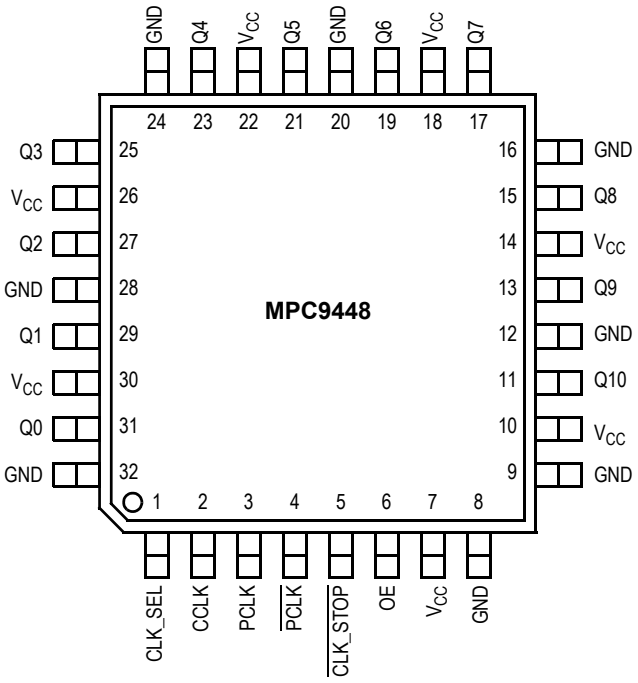


Figure 2. 32-Lead Pinout (Top View)

Table 1. Function Table

Control	Default	0	1
CLK_SEL	1	PECL differential input selected	CCLK input selected
OE	1	Outputs disabled (high-impedance state)[1]	Outputs enabled
$\overline{\text{CLK\_STOP}}$	1	Outputs synchronously stopped in logic low state	Outputs active

1. OE = 0 will high-impedance tristate all outputs independent on $\overline{\text{CLK\_STOP}}$

Table 2. Pin Configurations

Pin	I/O	Type	Function
PCLK, $\overline{\text{PCLK}}$	Input	LVPECL	Clock signal input
CCLK	Input	LVCMOS	Alternative clock signal input
CLK_SEL	Input	LVCMOS	Clock input select
$\overline{\text{CLK\_STOP}}$	Input	LVCMOS	Clock output enable/disable
OE	Input	LVCMOS	Output enable/disable (high-impedance tristate)
Q0–11	Output	LVCMOS	Clock outputs
GND	Supply	Ground	Negative power supply (GND)
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit
V_{CC}	Supply Voltage	–0.3	3.9	V
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V
I_{IN}	DC Input Current		±20	mA
I_{OUT}	DC Output Current		±50	mA
T_{Stor}	Storage temperature	–65	125	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
LU	Latch-up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 5. DC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40°C to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input HIGH Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input LOW Voltage		–0.3		0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage	PCLK	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK	1.1		V_{CC} – 0.6	V	LVPECL
I_{IN}	Input Current[2]				300	µA	V_{IN} = V_{CC} or GND
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH} = –24mA[3]
V_{OL}	Output LOW Voltage				0.55 0.30	V V	I_{OL} = 24mA[3] I_{OL} = 12mA
Z_{OUT}	Output Impedance			17		Ω	
I_{CCQ}[4]	Maximum Quiescent Supply Current				2.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. Input pull-up / pull-down resistors influence input current.
3. The MPC9448 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines (for V_{CC} = 3.3V) or one 50Ω series terminated transmission line (for V_{CC}=2.5V).
4. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 6. AC Characteristics (V_{CC} = 3.3V ± 5%, T_A = -40°C to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		350	MHz	
f_{MAX}	Maximum Output Frequency		0		350	MHz	
V_{PP}	Peak-to-Peak Input Voltage	PCLK	400		1000	mV	LVPECL
V_{CMR}[2]	Common Mode Range	PCLK	1.3		V_{CC} – 0.8	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time				1.0[3]	ns	0.8 to 2.0V
$t_{PLH/HL}$ $t_{PLH/HL}$	Propagation Delay	PCLK to any Q CCLK to any Q	1.6 1.3		3.6 3.3	ns ns	
$t_{PLZ, HZ}$	Output Disable Time				11	ns	
$t_{PZL, LZ}$	Output Enable Time				11	ns	
t_S	Setup Time	CCLK to $\overline{CLK\_STOP}$ PCLK to $\overline{CLK\_STOP}$	0.0 0.0			ns ns	
t_H	Hold Time	CCLK to $\overline{CLK\_STOP}$ PCLK to $\overline{CLK\_STOP}$	1.0 1.5			ns ns	
$t_{sk(O)}$	Output-to-Output Skew				150	ps	
$t_{sk(PP)}$	Device-to-Device Skew	PCLK or CCLK to any Q			2.0	ns	
$t_{SK(P)}$	Output Pulse skew[4]	Using CCLK Using PCLK			300 400	ps ps	
DC_Q	Output Duty Cycle	f_Q<170 MHz	45	50	55	%	DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts $t_{PLH/HL}$ and $t_{SK(PP)}$.
3. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
4. Output pulse skew is the absolute difference of the propagation delay times: $| t_{pLH} - t_{pHL} |$.

Table 7. DC Characteristics (V_{CC} = 2.5V ± 5%, T_A = -40°C to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage		1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input low voltage		–0.3		0.7	V	LVCMOS
V_{PP}	Peak-to-peak input voltage	PCLK	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK	1.0		V_{CC} – 0.7	V	LVPECL
I_{IN}	Input current[2]				300	μA	V_{IN} = GND or V_{IN} = V_{CC}
V_{OH}	Output High Voltage		1.8			V	I_{OH} = –15 mA[3]
V_{OL}	Output Low Voltage				0.6	V	I_{OL}= 15 mA[3]
Z_{OUT}	Output impedance			19		Ω	
I_{CCQ}[4]	Maximum Quiescent Supply Current				2.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. Input pull-up / pull-down resistors influence input current.
3. The MPC9448 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives one 50Ω series terminated transmission lines at V_{CC} = 2.5V.
4. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 8. AC Characteristics (V_{CC} = 2.5V ± 5%, T_A = -40°C to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		350	MHz	
f_{MAX}	Maximum Output Frequency		0		350	MHz	
V_{PP}	Peak-to-peak input voltage	PCLK	400		1000	mV	LVPECL
V_{CMR}[2]	Common Mode Range	PCLK	1.2		V_{CC} – 0.8	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	CCLK Input Rise/Fall Time				1.0[3]	ns	0.8 to 2.0V
$t_{PLH/HL}$ $t_{PLH/HL}$	Propagation delay	PCLK to any Q CCLK to any Q	1.5 1.7		4.2 4.4	ns ns	
$t_{PLZ, HZ}$	Output Disable Time				11	ns	
$t_{PZL, LZ}$	Output Enable Time				11	ns	
t_S	Setup time	CCLK to $\overline{CLK\_STOP}$ PCLK to $\overline{CLK\_STOP}$	0.0 0.0			ns ns	
t_H	Hold time	CCLK to $\overline{CLK\_STOP}$ PCLK to $\overline{CLK\_STOP}$	1.0 1.5			ns ns	
$t_{sk(O)}$	Output-to-output Skew				150	ps	
$t_{sk(PP)}$	Device-to-device Skew	PCLK or CCLK to any Q			2.7	ns	
$t_{SK(p)}$	Output pulse skew[4]	Using CCLK Using PCLK			200 300	ps ps	DC_{REF} = 50%
DC_Q	Output Duty Cycle	f_Q< 350 MHz and using CCLK f_Q<200 MHz and using PCLK	45 45	50 50	55 55	% %	
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8V

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts $t_{PLH/HL}$ and $t_{SK(PP)}$.
3. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
4. Output pulse skew is the absolute difference of the propagation delay times: $| t_{pLH} - t_{pHL} |$.

APPLICATION INFORMATION

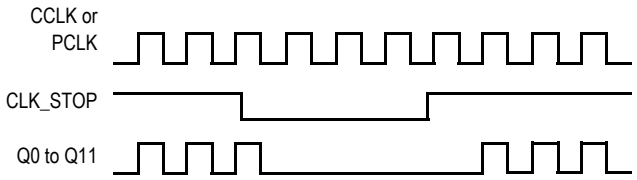


Figure 3. 32-Lead Pinout (Top View)

Driving Transmission Lines

The MPC9448 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of 17Ω (V_{CC}=3.3V), the outputs can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Motorola application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

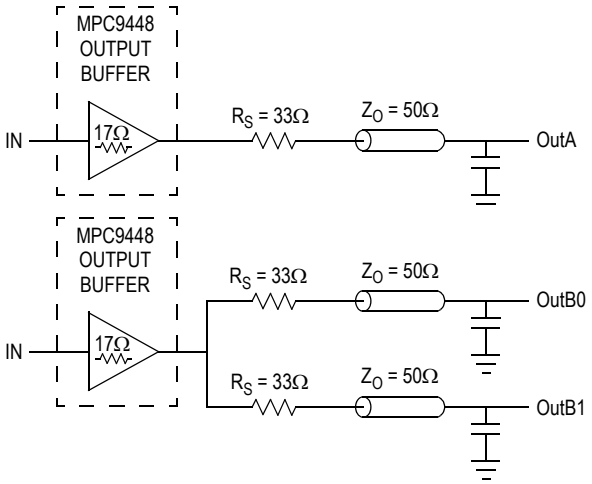


Figure 4. Single versus Dual Transmission Lines

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9448 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 4. Single versus Dual Transmission Lines illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9448 clock driver is effectively doubled due to its capability to drive multiple lines at V_{CC} = 3.3V.

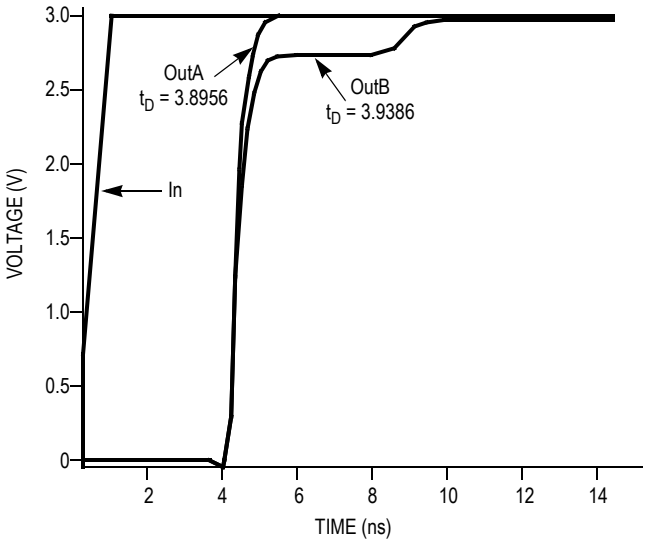


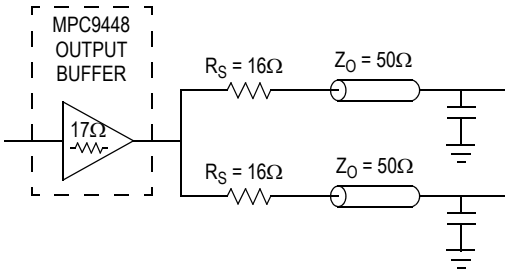
Figure 5. Single versus Dual Line Termination Waveforms

The waveform plots in Figure 5. Single versus Dual Line Termination Waveforms show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9448 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9448. The output waveform in Figure 5. Single versus Dual Line Termination Waveforms shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 33Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S+R_0 +Z_0))$$
$$Z_0 = 50\Omega \parallel 50\Omega$$
$$R_S = 33\Omega \parallel 33\Omega$$
$$R_0 = 17\Omega$$
$$V_L = 3.0 (25 \div (16.5+17+25)$$
$$= 1.28V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

Since this step is well above the threshold region it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 6. Optimized Dual Line Termination should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



17Ω + 16Ω || 16Ω = 50Ω || 50Ω
25Ω = 25Ω

Figure 6. Optimized Dual Line Termination

Power Consumption of the MPC9448 and Thermal Management

The MPC9448 AC specification is guaranteed for the entire operating frequency range up to 350 MHz. The MPC9448 power consumption and the associated long-term reliability may decrease the maximum frequency limit, depending on operating conditions such as clock frequency, supply voltage, output loading, ambient temperature, vertical convection and thermal conductivity of package and board. This section describes the impact of these parameters on the junction temperature and gives a guideline to estimate the MPC9448 die junction temperature and the associated device reliability. For a complete analysis of power consumption as a function of operating conditions and associated long term device reliability please refer to the application note AN1545. According the AN1545, the long-term device reliability is a function of the die junction temperature:

Table 9. Die Junction Temperature and MTFB

Junction Temperature (°C)	MTBF (Years)
100	20.4
110	9.1
120	4.2
130	2.0

Increased power consumption will increase the die junction temperature and impact the device reliability (MTBF). According to the system-defined tolerable MTBF, the die junction temperature of the MPC9448 needs to be controlled and the thermal impedance of the board/package should be optimized. The power dissipated in the MPC9448 is represented in equation 1.

Where I_{CCQ} is the static current consumption of the MPC9448, C_{PD} is the power dissipation capacitance per output, $(M)\Sigma C_L$ represents the external capacitive output load, N is the number of active outputs (N is always 12 in case of the MPC9448). The MPC9448 supports driving transmission lines to maintain high signal integrity and tight timing parameters. Any transmission line will hide the lumped capacitive load at the end of the board trace, therefore, ΣC_L is zero for controlled transmission line systems and can be eliminated from equation 1. Using parallel termination output termination results in equation 2 for power dissipation.

In equation 2, P stands for the number of outputs with a parallel or thevenin termination, V_{OL}, I_{OL}, V_{OH} and I_{OH} are a function of the output termination technique and DC_Q is the clock signal duty cycle. If transmission lines are used ΣC_L is zero in equation 2 and can be eliminated. In general, the use of controlled transmission line techniques eliminates the impact of the lumped capacitive loads at the end lines and greatly reduces the power dissipation of the device. Equation 3 describes the die junction temperature T_J as a function of the power consumption.

Where R_{thja} is the thermal impedance of the package (junction to ambient) and T_A is the ambient temperature. According to Table 9. Die Junction Temperature and MTFB, the junction temperature can be used to estimate the long-term device reliability. Further, combining equation 1 and equation 2 results in a maximum operating frequency for the MPC9448 in a series terminated transmission line system, equation 4.

$$P_{TOT} = \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] \cdot V_{CC} \qquad \text{Equation 1}$$

$$P_{TOT} = V_{CC} \cdot \left[I_{CCQ} + V_{CC} \cdot f_{CLOCK} \cdot \left(N \cdot C_{PD} + \sum_{M} C_L \right) \right] + \sum_{P} \left[DC_Q \cdot I_{OH} \cdot (V_{CC} - V_{OH}) + (1 - DC_Q) \cdot I_{OL} \cdot V_{OL} \right] \qquad \text{Equation 2}$$

$$T_J = T_A + P_{TOT} \cdot R_{thja} \qquad \text{Equation 3}$$

$$f_{CLOCK,MAX} = \frac{1}{C_{PD} \cdot N \cdot V_{CC}^2} \cdot \left[\frac{T_{j,MAX} - T_A}{R_{thja}} - (I_{CCQ} \cdot V_{CC}) \right] \qquad \text{Equation 4}$$

$T_{J,MAX}$ should be selected according to the MTBF system requirements and Table 9. Die Junction Temperature and MTFB. R_{thja} can be derived from Table 10. Thermal Package Impedance of the 32ld LQFP. The R_{thja} represent data based on 1S2P boards, using 2S2P boards will result in a lower thermal impedance than indicated below.

Table 10. Thermal Package Impedance of the 32ld LQFP

Convection, LFPM	R_{thja} (1P2S board), °C/W	R_{thja} (2P2S board), °C/W
Still air	86	61
100 lfpm	76	56
200 lfpm	71	54
300 lfpm	68	53
400 lfpm	66	52
500 lfpm	60	49

If the calculated maximum frequency is below 350 MHz, it becomes the upper clock speed limit for the given application conditions. The following eight derating charts describe the safe frequency operation range for the MPC9448. The charts were calculated for a maximum tolerable die junction temperature of 110°C (120°C), corresponding to an estimated MTBF of 9.1 years (4 years), a supply voltage of 3.3V and series terminated transmission line or capacitive loading. Depending on a given set of these operating conditions and the available device convection a decision on the maximum operating frequency can be made.

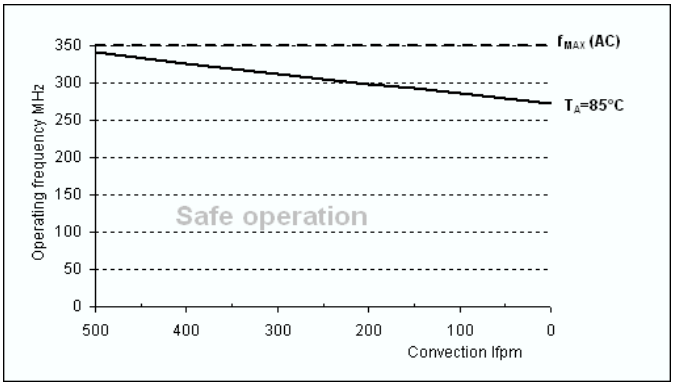


Figure 7. Maximum MPC9448 Frequency, V_{CC} = 3.3V, MTBF 9.1 Years, Driving Series Terminated transmission lines, 2s2p board

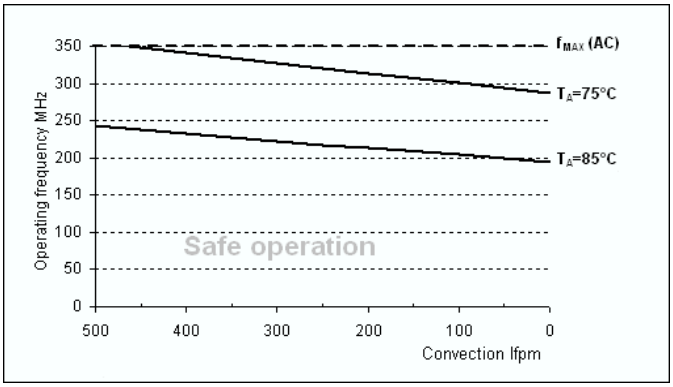


Figure 8. Maximum MPC9448 frequency, V_{CC} = 3.3V, MTBF 9.1 Years, 4 pF Load per Line, 2s2p Board

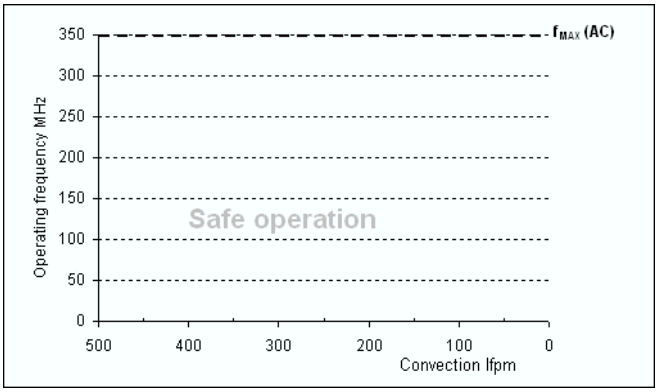


Figure 9. No maximum Frequency Limitation for V_{CC} = 3.3V, MTBF 4 Years, Driving Series Terminated Transmission Lines, 2s2p Board

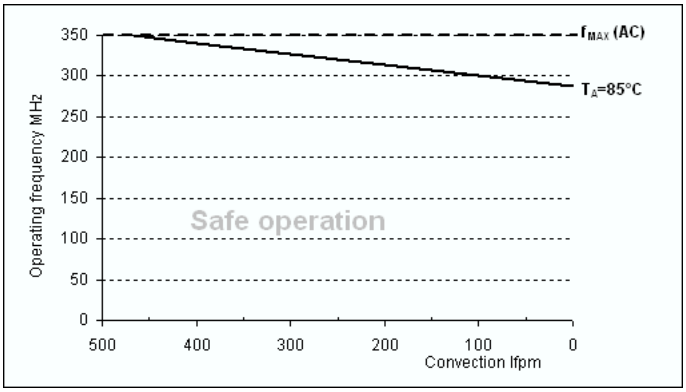


Figure 10. Maximum MPC9448 Frequency, V_{CC} = 3.3V, MTBF 4 Years, 4 pF Load per Line, 2s2p Board

The Following Figures Illustrate the Measurement Reference for the MPC9448 Clock Driver Circuit

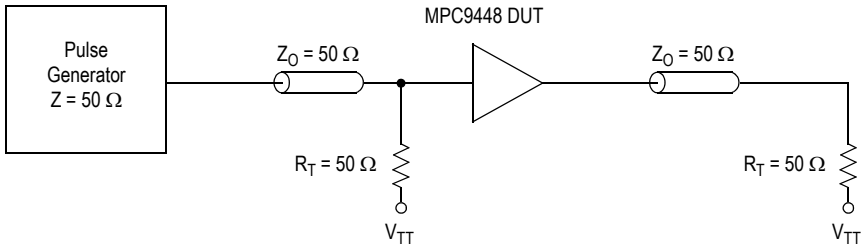


Figure 11. CCLK MPC9448 AC Test Reference for V_{cc} = 3.3V and V_{cc} = 2.5V

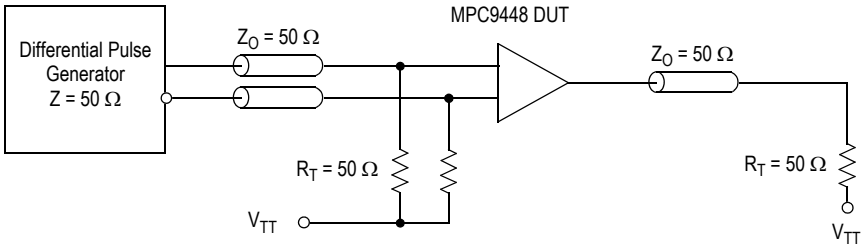


Figure 12. PCLK MPC9448 AC Test Reference

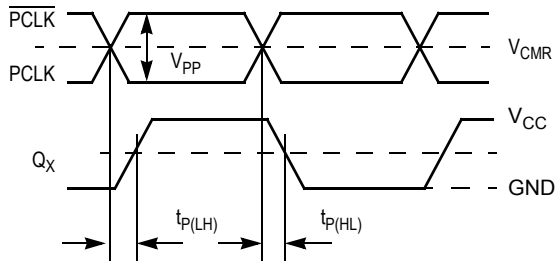


Figure 13. Propagation Delay (t_{PD}) Test Reference

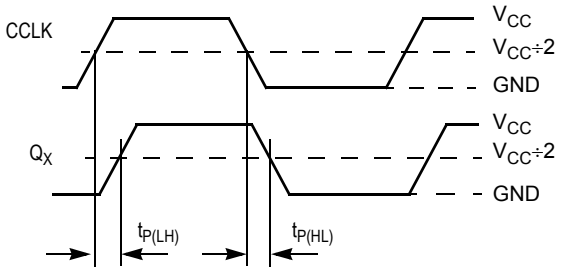
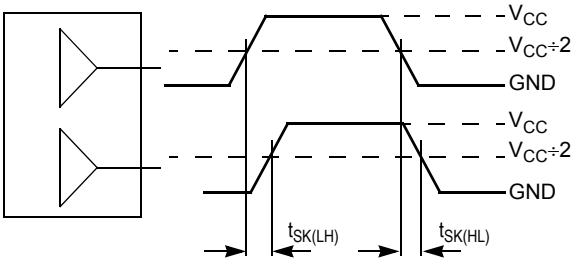


Figure 14. Propagation Delay (t_{PD}) Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 15. Output-to-Output Skew $t_{SK(LH, HL)}$

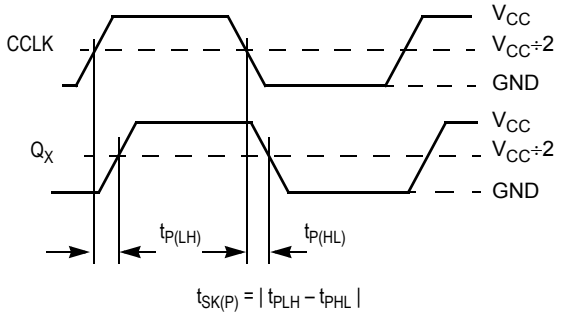
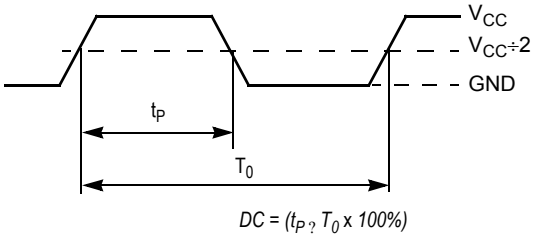


Figure 16. Output Pulse Skew ($t_{SK(P)}$) Test Reference



The time from the output controlled edge to the non-controlled edge, divided by the time between output controlled edges, expressed as a percentage

Figure 17. Output Duty Cycle (DC)

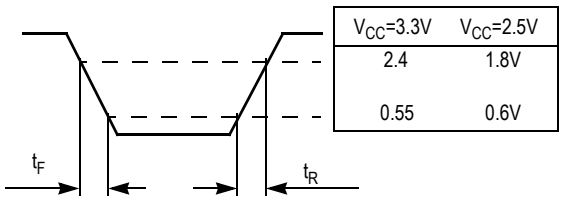
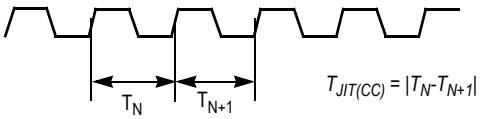


Figure 18. Output Transition Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 19. Cycle-to-Cycle Jitter

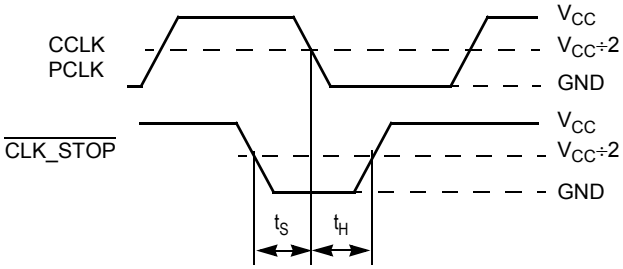


Figure 20. Setup and Hold Time (t_S, t_H) Test Reference

Order number: MPC9449
Rev 2, 08/2004

3.3 V/2.5 V 1:15 PECL/LVCMOS Clock Fanout Buffer

MPC9449

3.5 V/2.5 V 1:15
PECL/LVCMOS
CLOCK FANOUT BUFFER

FA SUFFIX
52-LEAD LQFP PACKAGE
CASE 848D-03

The MPC9449 is a 3.3 V or 2.5 V compatible, 1:15 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 200 MHz and output skews less than 200 ps the device meets the needs of the most demanding clock applications.

Features

- 15 LVCMOS compatible clock outputs
- Two selectable LVCMOS and one differential LVPECL compatible clock inputs
- Selectable output frequency divider (divide-by-one and divide-by-two)
- Maximum clock frequency of 200 MHz
- Maximum clock skew of 200 ps
- High-impedance output control
- 3.3 V or 2.5 V power supply
- Drives up to 30 series terminated clock lines
- Ambient temperature range –40°C to +85°C
- 52-lead LQFP packaging
- 52-lead Pb-free package available
- Supports clock distribution in networking, telecommunication and computing applications
- Pin and function compatible to MPC949

Functional Description

The MPC9449 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 200 MHz. The device has 15 identical outputs, organized in four output banks. Each output bank provides a retimed or frequency divided copy of the input signal with a near zero skew. The output buffer supports driving of 50 Ω terminated transmission lines on the incident edge: each output is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable LVCMOS compatible clock inputs are available. This feature supports redundant differential clock sources. In addition, the MPC9449 accepts one differential PECL clock signal. The DSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the four output banks. Applying the OE control will force the outputs into high-impedance mode.

All inputs have an internal pull-up or pull-down resistor preventing unused and open inputs from floating. The device supports a 2.5 V or 3.3 V power supply and an ambient temperature range of –40°C to +85°C. The MPC9449 is pin and function compatible but performance-enhanced to the MPC949. The device is packaged in a 52-lead LQFP package.

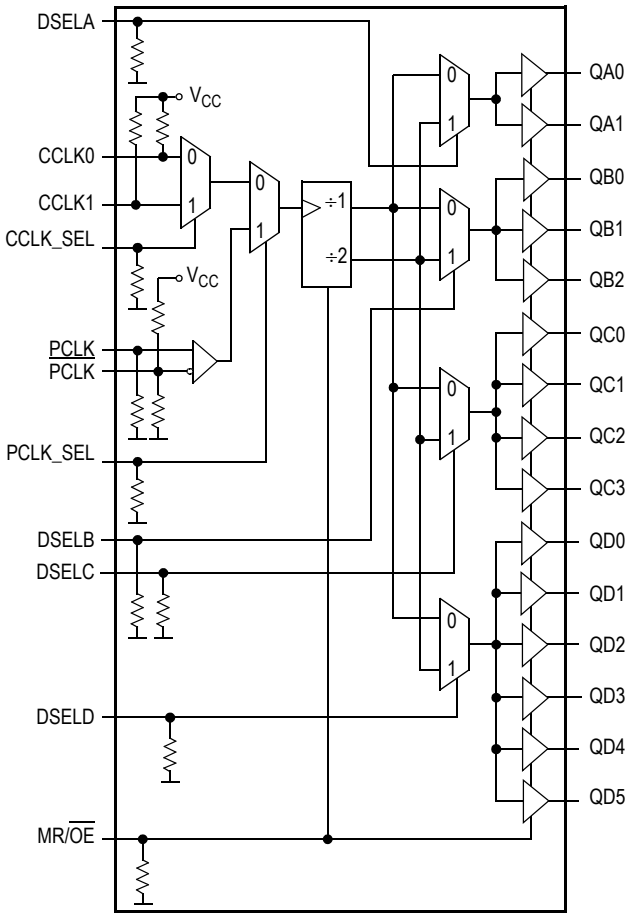


Figure 1. MPC9449 Logic Diagram

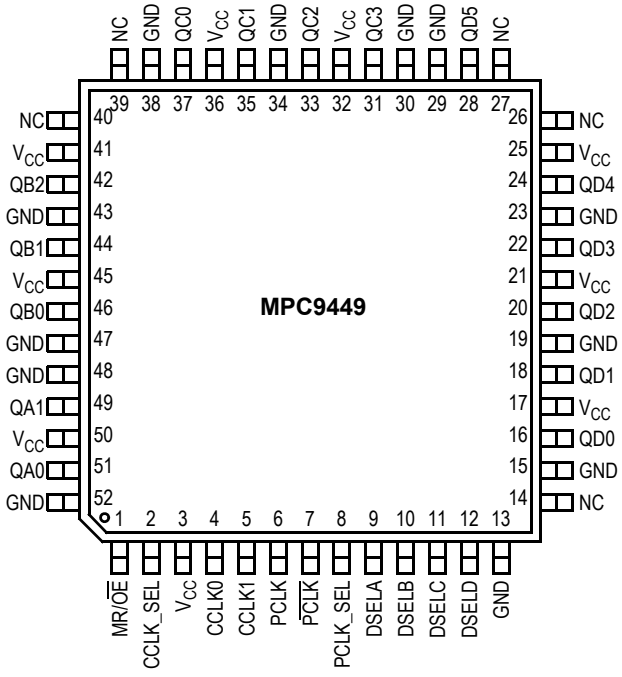


Figure 2. PC9449 52-Lead Package Pinout (Top View)

Table 1. Function Table

Control	Default	0	1
PCLK_SEL	0	LVCMOS clock input selected (CCLK0 or CCLK1)	PCLK differential input selected
CCLK_SEL	0	CCLK0 selected	CCLK1 selected
DSELA, DSELB, DSELC, DSELD	0 0 0 0	÷1	÷2
MR/$\overline{OE}$	1	Outputs enabled	Outputs disabled (high impedance)

Table 2. Pin Configuration

Pin	I/O	Type	Function
PCLK, $\overline{PCLK}$	Input	LVPECL	Differential LVPECL clock input
CCLK0, CCLK1	Input	LVCMOS	LVCMOS clock inputs
PCLK_SEL	Input	LVCMOS	LVPECL clock input select
CCLK_SEL	Input	LVCMOS	LVCMOS clock input select
DSELA, DSELB, DSELC, DSELD	Input	LVCMOS	Clock divider selection
MR/$\overline{OE}$	Input	LVCMOS	Output enable/disable (high-impedance tristate)
QA0-1, QB0-2, QC0-3, QD0-5	Output	LVCMOS	Clock outputs
GND	Supply	Ground	Negative power supply (GND)
V_{CC}	Supply	V_{CC}	Positive power supply for I/O and core. All V_{CC} pins must be connected to the positive power supply for correct operation

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		12		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	Inputs

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.8	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40°C to 85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		2.0		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage				0.8	V	LVCMOS
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA[1]
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[2]	Common Mode Range	PCLK, $\overline{PCLK}$	1.0		V_{CC}–0.6	V	LVPECL
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL} = 24 mA I_{OL} = 12 mA
Z_{OUT}	Output Impedance			14 – 17		Ω	
I_{IN}	Input Current				±200	μA	V_{IN} = V_{CC} or GND
I_{CCQ}	Maximum Quiescent Supply Current				10	mA	All V_{CC} Pins

1. The MPC9449 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50 Ω series terminated transmission lines.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_A = –40°C to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	400		1000	mV	LVPECL
V_{CMR}[2]	Common Mode Range	PCLK, $\overline{PCLK}$	1.0		V_{CC}–0.6	V	LVPECL
f_{max}	Output Frequency		0		200	MHz	
f_{ref}	Input Frequency		0		200	MHz	
$t_{P, REF}$	Reference Input Pulse Width		1.5			ns	
t_r, t_f	CCLK0, CCLK1 Input Rise/Fall Time				1.0	ns	0.8 to 2.0 V
$t_{sk(O)}$	Output-to-Output Skew	Qa outputs Qb outputs Qc outputs Qd outputs All outputs All outputs			50 50 50 100 200 300	ps ps ps ps ps ps	 Same Frequency Different Frequencies
$t_{sk(PP)}$	Device-to-Device Skew			2.5		ns	
$t_{sk(P)}$	Output Pulse Skew				250	ps	DC_{REF} = 50%
$t_{PLH, HL}$	Propagation Delay	CCLK0 or CCLK1 to any Q PCLK to any Q	1.0 1.0	3.0 3.0	5.0 5.0	ns ns	
$t_{PLZ, HZ}$	Output Disable Time	OE to any Q			11	ns	
$t_{PZL, LZ}$	Output Enable Time	OE to any Q			11	ns	
t_r, t_f	Output Rise/Fall Time[3]		0.1		1.0	ns	0.55 to 2.4 V
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	RMS (1 σ)		TBD		ps	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts propagation delay.
3. An input rise/fall time greater than that specified may be used, but AC characteristics are not guaranteed under such a condition.

Table 7. DC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = –40°C to 85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		1.7		V_{CC} + 0.3	V	LVCMOS
V_{IL}	Input Low Voltage		–0.3		0.7	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK, $\overline{PCLK}$	1.0		V_{CC}–0.6	V	LVPECL
V_{OH}	Output High Voltage		1.8			V	I_{OH} = –15 mA[2]
V_{OL}	Output Low Voltage				0.6	V	I_{OL} = 15 mA
Z_{OUT}	Output Impedance			17–20		Ω	
I_{IN}	Input Current[3]				±200	μA	V_{IN} = V_{CC} or GND
I_{CC}	Maximum Quiescent Supply Current				10	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9449 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of V_{TT}.
3. Inputs have pull-down or pull-up resistors affecting the input current.

Table 8. AC Characteristics (V_{CC} = 2.5 V ± 5%, T_A = -40°C to 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{PP}	Peak-to-Peak Input Voltage	PCLK, $\overline{PCLK}$	400		1000	mV	LVPECL
V_{CMR}[2]	Common Mode Range	PCLK, $\overline{PCLK}$	1.2		V_{CC}–0.6	V	LVPECL
f_{max}	Output Frequency		0		200	MHz	
f_{ref}	Input Frequency		0		200	MHz	
$t_{P, REF}$	Reference Input Pulse Width		1.5			ns	
tr, tf	CCLK Input Rise/Fall Time				1.0	ns	0.7 to 1.7 V
$t_{sk(O)}$	Output-to-Output Skew	Qa outputs			50	ps	
		Qb outputs			50	ps	
		Qc outputs			50	ps	
		Qd outputs			100	ps	
	Same Frequency	All outputs			200	ps	
	Different Frequencies	All outputs			300	ps	
$t_{sk(PP)}$	Device-to-Device Skew			5.0		ns	
$t_{SK(P)}$	Output Pulse Skew				350	ps	DC_{REF} = 50%
$t_{PLH, HL}$	Propagation Delay	CCLK0 or CCLK1 to any Q	1.0	3.5	7.0	ns	
		PCLK to any Q	1.0	3.5	7.0	ns	
$t_{PLZ, HZ}$	Output Disable Time	OE to any Q			11	ns	
$t_{PZL, LZ}$	Output Enable Time	OE to any Q			11	ns	
t_r, t_f	Output Rise/Fall Time[3]		0.1		1.0	ns	0.6 to 1.8 V
$t_{JIT(CC)}$	Cycle-to-Cycle Jitter	RMS (1 σ)		TBD		ps	

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} or V_{PP} impacts propagation delay.
3. An input rise/fall time greater than that specified may be used, but AC characteristics are not guaranteed under such a condition.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC9449 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20 Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to Motorola application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9449 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9449 clock driver is effectively doubled due to its capability to drive multiple lines.

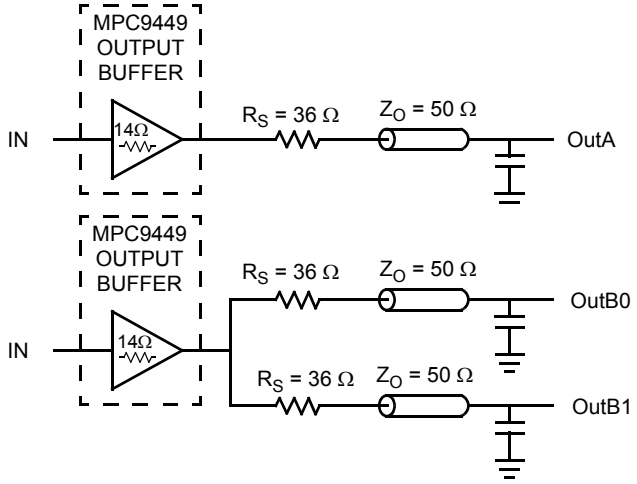


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9449 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9449. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36 Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \parallel 50\ \Omega$$
$$R_S = 36\ \Omega \parallel 36\ \Omega$$
$$R_0 = 14\ \Omega$$
$$V_L = 3.0\ (25 \div (18 + 17 + 25)$$
$$= 1.31V$$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.6 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

1. Final skew data pending specification.

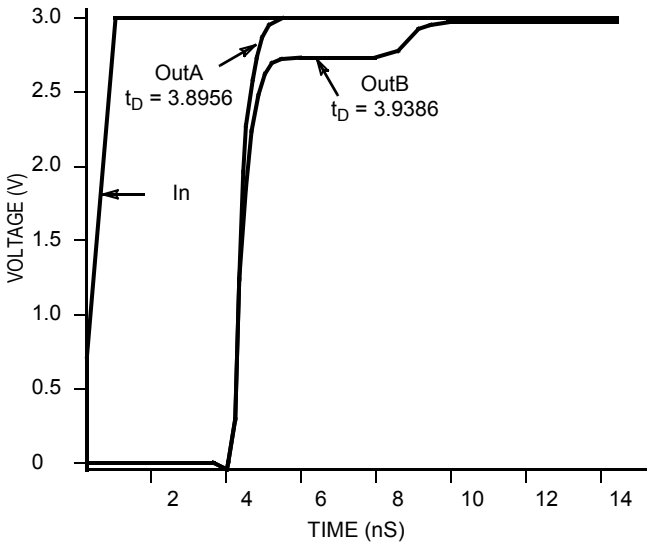
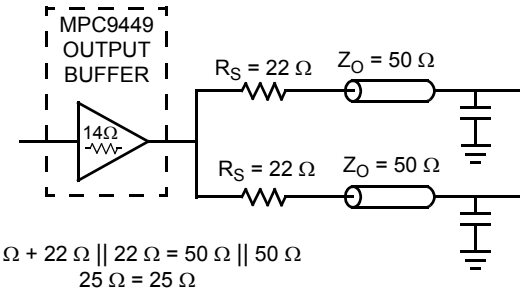


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.



$14\ \Omega + 22\ \Omega \parallel 22\ \Omega = 50\ \Omega \parallel 50\ \Omega$
$25\ \Omega = 25\ \Omega$

Figure 5. Optimized Dual Line Termination

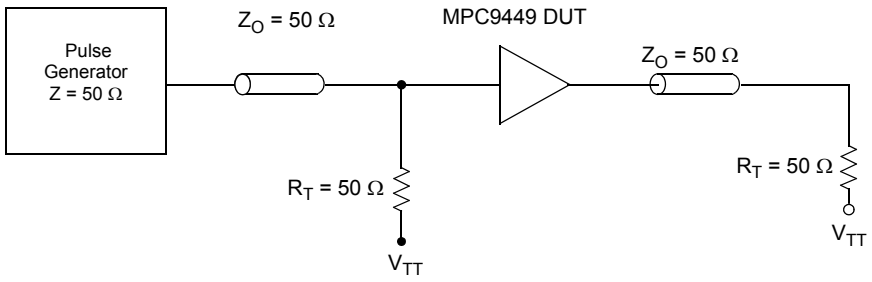


Figure 6. CCLK MPC9449 AC Test Reference for V_{cc} = 3.3V and V_{cc} = 2.5V

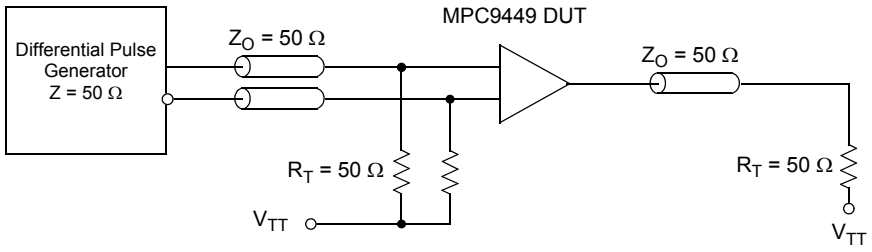
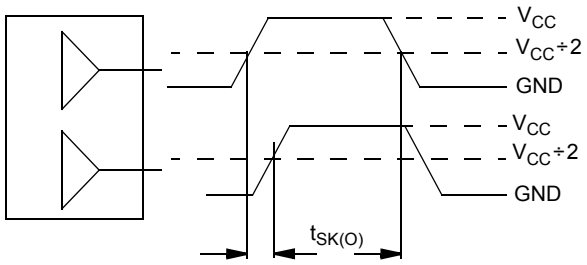


Figure 7. PCLK MPC9449 AC Test Reference



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 8. Output-to-Output Skew $t_{SK(O)}$

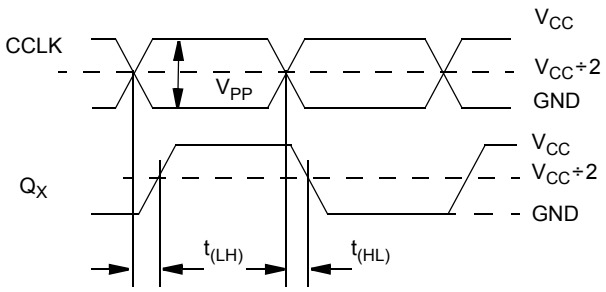


Figure 9. Propagation Delay (t_{PD}) Test Reference

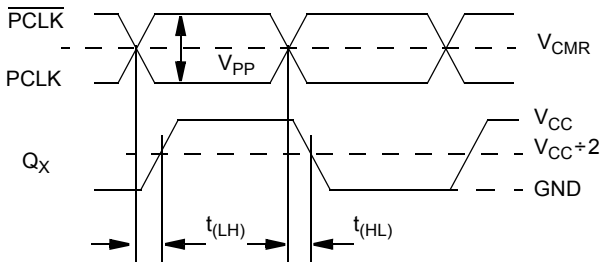


Figure 10. Propagation Delay (t_{PD}) Test Reference

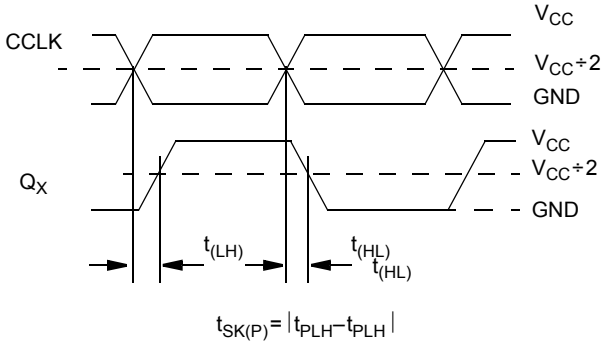


Figure 11. Propagation Delay $t_{SK(P)}$ Test Reference

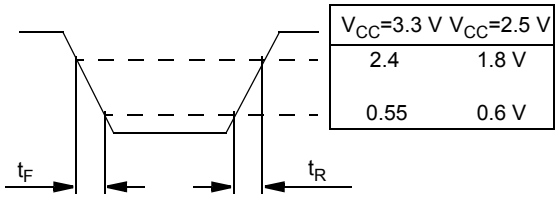
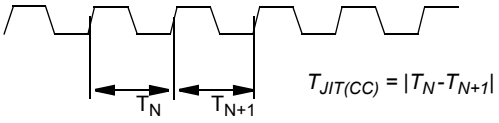


Figure 12. Output Transition Time Test Reference



The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs

Figure 13. Cycle-to-Cycle Jitter

Order number: MPC94551
Rev 2, 06/2004

Product Preview

Low Voltage 1:4 CMOS Clock Buffer

The MPC94551 is a CMOS 1:4 fanout buffer. The MPC94551 is ideal for applications requiring lower voltage.

Features

- 1:4 CMOS fanout buffer
- 250 ps output to output skew
- I/O frequency up to 160 MHz operation
- Non-inverting output clock
- 3.3 V supply voltage
- Output Enable mode tri-states outputs
- -40°C to 85°C industrial temperature range
- Standard 8-lead SOIC package

MPC94551

1:4 LVCMOS CLOCK BUFFER

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-06

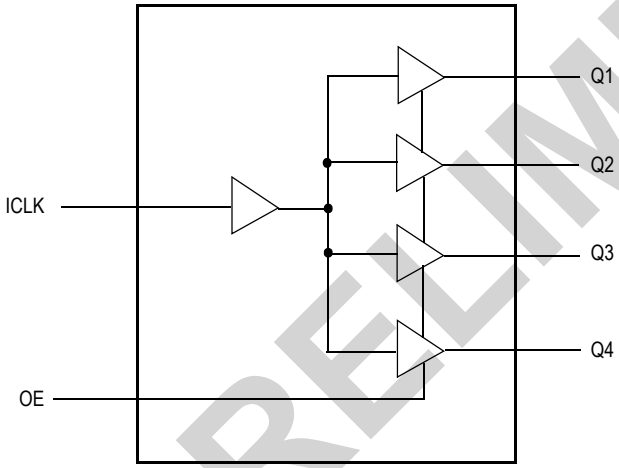


Figure 1. Logic Diagram

ORDERING INFORMATION

Device	Package
MPC94551D	SO-8
MPC94551DR2	SO-8

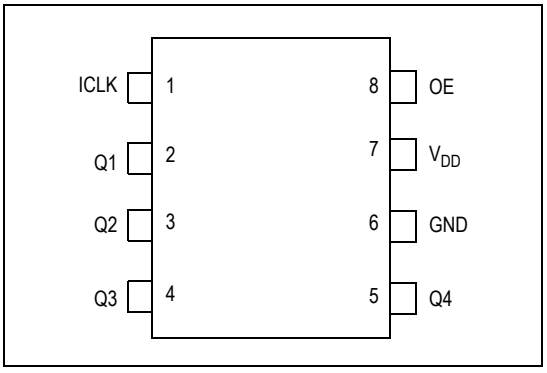


Figure 2. Pin Assignment

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table 1. Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	ICLK	Input	Clock input, internal pull-up resistor
2	Q1	Output	Clock output [1]
3	Q2	Output	Clock output [1]
4	Q3	Output	Clock output [1]
5	Q4	Output	Clock output [1]
6	GND	Power	Connect to ground [2]
7	V_{DD}	Power	Connect to 3.3 V [2]
8	OE	Input	Output enable, tri-states outputs when low, internal pull-up resistor

1. A 33 Ω series terminating resistor may be used on each clock output if the trace is longer than 1 inch.
2. A decoupling capacitor of 0.01 μ F should be connected between V_{DD} on pin 7 and GND on pin 6, as close to the device as possible.

Table 2. Absolute Maximum Ratings[1]

Parameter	Rating	Unit
Power Supply Voltage, V_{DD}	3.9	V
All Inputs and Outputs	–0.5 to V_{DD} +0.5	V
Ambient Operating Temperature	–40 to +85	°C
Storage Temperature	–65 to +150	°C
Junction Temperature	175	°C
Soldering Temperature	260	°C

1. Stresses above the ratings listed below can cause permanent damage to the device. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Table 3. Recommended Operation Conditions

Parameter	Min	Typ	Max	Unit
Ambient Operating Temperature	–40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.135		+3.465	V

Table 4. DC Characteristics (V_{DD} = 3.3 V ± 5%; Ambient Temperature = –40°C to 85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		3.15		3.45	V
Input High Voltage[1], ICLK	V_{IH}		$V_{DD}/2 + 0.7$		3.8	V
Input Low Voltage[1], ICLK	V_{IL}				$V_{DD}/2 – 0.7$	V
Input High Voltage, OE	V_{IH}		2		V_{DD}	V
Input Low Voltage, OE	V_{IL}				0.8	V
Output High Voltage	V_{OH}	I_{OH} = –25 mA	2.4			V
Ouput Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V
Output High Voltage (CMOS Level)	V_{OH}	I_{OH} = –12 mA	$V_{DD} – 0.4$			V
Operating Supply Current	I_{DD}	No load, 135 MHz		18		mA
Nominal Output Impedance	Z_O			20		W
Internal Pull-up Resistor	R_{PU}	ICLK		30		kΩ
Input Capacitance	C_{IN}	OE pin		5		pF
	C_{IN}	ICLK		TBD		pF
Short Circuit Current	I_{OS}			±50		mA

1. Nominal switching threshold is $V_{DD}/2$.

Table 5. AC Characteristics (V_{DD} = 3.3 V ± 5%; Ambient Temperature = –40°C to 85°C)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Frequency			0		160	MHz
Output Frequency[1]		15 pF load			160	MHz
Output Clock Rise Time	t_{OR}	0.8 V to 2.0 V			1.5	ns
Output Clock Fall Time	t_{OF}	2.0 V to 0.8 V			1.5	ns
Propagation Delay[2]		135 MHz	2	4	8	ns
Output to Output Skew[3]		Rising edges at $V_{DD}/2$			250	ps

1. Measured with an external series resistor of 33Ω positioned close to each output pin
2. Measured with rail to rail input clock
3. Measured between any 2 outputs with equal loading

Order number: MPC9456
Rev 2, 08/2004

2.5 V and 3.3 V LVCMOS Clock Fanout Buffer

MPC9456

LOW VOLTAGE SINGLE OR DUAL SUPPLY 2.5 V AND 3.3 V LVCMOS CLOCK DISTRIBUTION BUFFER

FA SUFFIX
LQFP PACKAGE
CASE 873A-03

The MPC9456 is a 2.5 V and 3.3 V compatible 1:10 clock distribution buffer designed for low-voltage mid-range to high-performance telecom, networking and computing applications. Both 3.3 V, 2.5 V and dual supply voltages are supported for mixed-voltage applications. The MPC9456 offers 10 low-skew outputs and a differential LVPECL clock input. The outputs are configurable and support 1:1 and 1:2 output to input frequency ratios. The MPC9456 is specified for the extended temperature range of –40 to 85°C.

Features

- Configurable 10 outputs LVCMOS clock distribution buffer
- Compatible to single, dual and mixed 3.3 V/2.5 V voltage supply
- Wide range output clock frequency up to 250 MHz
- Designed for mid-range to high-performance telecom, networking and computer applications
- Supports high-performance differential clocking applications
- Maximum output skew of 200 ps (150 ps within one bank)
- Selectable output configurations per output bank
- Tristable outputs
- 32-lead LQFP package
- Ambient operating temperature range of –40 to 85°C
- 32-lead Pb-free package available

Functional Description

The MPC9456 is a full static design supporting clock frequencies up to 250 MHz. The signals are generated and retimed on-chip to ensure minimal skew between the three output banks.

Each of the three output banks can be individually supplied by 2.5 V or 3.3 V supporting mixed voltage applications. The FSELx pins choose between division of the input reference frequency by one or two. The frequency divider can be set individually for each of the three output banks. The MPC9456 can be reset and the outputs are disabled by deasserting the MR/$\overline{OE}$ pin (logic high state). Asserting MR/$\overline{OE}$ will enable the outputs.

All control inputs accept LVCMOS signals while the outputs provide LVCMOS compatible levels with the capability to drive terminated 50 Ω transmission lines. The clock input is low voltage PECL compatible for differential clock distribution support. Please consult the MPC9446 specification for a full CMOS compatible device. For series terminated transmission lines, each of the MPC9456 outputs can drive one or two traces giving the devices an effective fanout of 1:20. The device is packaged in a 7×7 mm^2 32-lead LQFP package.

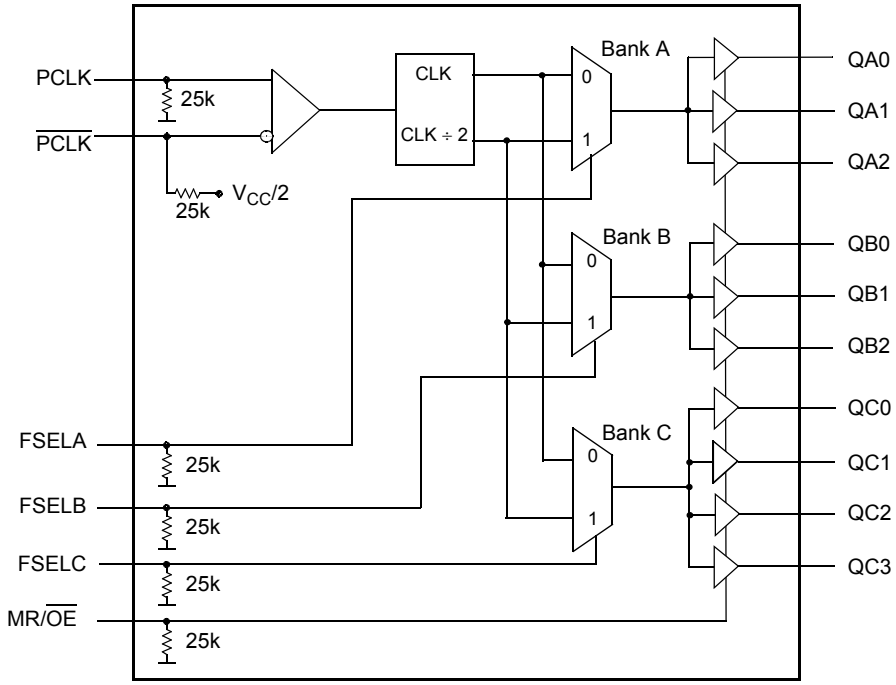


Figure 1. MPC9456 Logic Diagram

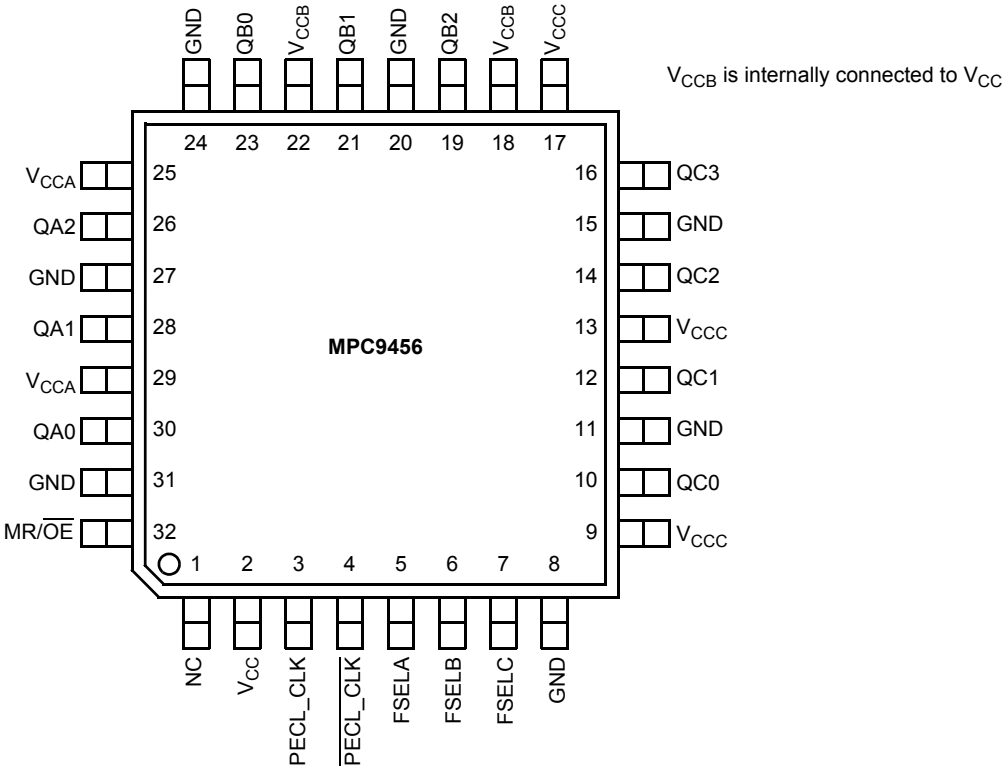


Figure 2. Pinout: 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
PECL_CLK, $\overline{\text{PECL\_CLK}}$	Input	LVPECL	Differential clock reference Low voltage positive ECL input
$FSEL_A$, $FSEL_B$, $FSEL_C$	Input	LVCMOS	Output bank divide select input
MR/$\overline{OE}$	Input	LVCMOS	Internal reset and output tristate control
GND		Supply	Negative voltage supply output bank (GND)
V_{CCA}, V_{CCB}[1], V_{CCC}		Supply	Positive voltage supply for output banks
V_{CC}		Supply	Positive voltage supply core (VCC)
QA0 – QA2	Output	LVCMOS	Bank A outputs
QB0 – QB2	Output	LVCMOS	Bank B outputs
QC0 – QC3	Output	LVCMOS	Bank C outputs

1. V_{CCB} is internally connected to V_{CC}.

Table 2. Supported Single and Dual Supply Configurations

Supply Voltage Configuration	V_{CC}[1]	V_{CCA}[2]	V_{CCB}[3]	V_{CCC}[4]	GND
3.3V	3.3V	3.3V	3.3V	3.3V	0V
Mixed Voltage Supply	3.3V	3.3V or 2.5V	3.3V	3.3V or 2.5V	0 V
2.5V	2.5V	2.5V	2.5V	2.5V	0 V

1. V_{CC} is the positive power supply of the device core and input circuitry. V_{CC} voltage defines the input threshold and levels.
2. V_{CCA} is the positive power supply of the bank A outputs. V_{CCA} voltage defines bank A output levels.
3. V_{CCB} is the positive power supply of the bank B outputs. V_{CCB} voltage defines bank B output levels. V_{CCB} is internally connected to V_{CC}.
4. V_{CCC} is the positive power supply of the bank C outputs. V_{CCC} voltage defines bank C output levels.

Table 3. Function Table (Controls)

Control	Default	0	1
FSELA	0	$f_{QA0:2} = f_{REF}$	$f_{QA0:2} = f_{REF} \div 2$
FSELB	0	$f_{QB0:2} = f_{REF}$	$f_{QB0:2} = f_{REF} \div 2$
FSELC	0	$f_{QC0:3} = f_{REF}$	$f_{QC0:3} = f_{REF} \div 2$
MR/$\overline{OE}$	0	Outputs enabled	Internal reset Outputs disabled (tristate)

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	4.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–40	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} \div 2$		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	2000			V	
LU	Latch-Up Immunity	200			mA	
C_{PD}	Power Dissipation Capacitance		10		pF	Per output
C_{IN}	Input Capacitance		4.0		pF	

Table 6. DC Characteristics ($V_{CC} = V_{CCA} = V_{CCB} = V_{CCC}$ = 3.3V ± 5%, T_A = –40 to + 85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input High Voltage		2.0		V_{CC}+0.3	V	LVCMOS
V_{IL}	Input Low Voltage		–0.3		0.8	V	LVCMOS
V_{PP}	Peak-to-Peak Input Voltage	PCLK	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK	1.1		V_{CC}–0.6	V	LVPECL
I_{IN}	Input Current[2]				200	µA	V_{IN} = GND or V_{IN} = V_{CC}
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –24 mA[3]
V_{OL}	Output Low Voltage				0.55 0.30	V V	I_{OL}= 24mA[2] I_{OL}= 12mA
Z_{OUT}	Output Impedance			14–17		Ω	
I_{CCQ}[4]	Maximum Quiescent Supply Current				2.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. Input pull-up / pull-down resistors influence input current.
3. The MPC9456 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines.
4. I_{CCQ} is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 7. AC Characteristics (V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 3.3V ± 5%, T_A = –40 to + 85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		250[2]	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output ÷2 output	0 0		250[2] 125	MHz MHz	FSELx = 0 FSELx = 1
V_{PP}	Peak-to-Peak Input Voltage	PCLK	500		1000	mV	LVPECL
V_{CMR}[3]	Common Mode Range	PCLK	1.3		V_{CC}–0.8	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	PCLK Input Rise/Fall Time				1.0[4]	ns	0.8 to 2.0V
t_{PLH} t_{PHL}	Propagation Delay	CCLK to any Q CCLK to any Q	2.2 2.2	2.8 2.8	4.45 4.2	ns ns	
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{sk(O)}$	Output-to-Output Skew	Within one bank Any output bank, same output divider Any output, Any output divider			150 200 350	ps ps ps	
$t_{sk(PP)}$	Device-to-Device Skew				2.25	ns	
$t_{SK(P)}$	Output Pulse Skew[5]				200	ps	
DC_Q	Output Duty Cycle	÷1 output ÷2 output	47 45	50 50	53 55	% %	DC_{REF} = 50% DC_{REF} = 25%–75%
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.55 to 2.4V

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. he MPC9456 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification.
4. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
5. Output pulse skew is the absolute difference of the propagation delay times: | t_{pLH}–t_{pHL} |.

Table 8. DC Characteristics (V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 2.5V ± 5%, T_A = –40 to +85°C)

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
V_{IH}	Input high voltage		1.7		V_{CC}+0.3	V	LVCMOS
V_{IL}	Input low voltage		–0.3		0.7	V	LVCMOS
V_{PP}	Peak-to-peak input voltage	PCLK	250			mV	LVPECL
V_{CMR}[1]	Common Mode Range	PCLK	1.1		V_{CC}–0.7	V	LVPECL
V_{OH}	Output High Voltage		1.8			V	I_{OH} = –15 mA[2]
V_{OL}	Output Low Voltage				0.6	V	I_{OL} = 15 mA
Z_{OUT}	Output impedance			17–20[2]		Ω	
I_{IN}	Input current[3]				±200	µA	V_{IN} = GND or V_{IN} = V_{CC}
I_{CCQ}[4]	Maximum Quiescent Supply Current				2.0	mA	All V_{CC} Pins

1. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (DC) specification.
2. The MPC9456 is capable of driving 50Ω transmission lines on the incident edge. Each output drives one 50Ω parallel terminated transmission line to a termination voltage of V_{TT}. Alternatively, the device drives up to two 50Ω series terminated transmission lines per output.
3. Input pull-up / pull-down resistors influence input current.
4. CCQ is the DC current consumption of the device with all outputs open and the input in its default state or open.

Table 9. AC Characteristics (V_{CC} = V_{CCA} = V_{CCB} = V_{CCC} = 2.5V ± 5%, T_A = –40 to +85°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
f_{ref}	Input Frequency		0		250[2]	MHz	
f_{MAX}	Maximum Output Frequency	÷1 output ÷2 output	0 0		250[2] 125	MHz MHz	FSELx = 0 FSELx = 1
V_{PP}	Peak-to-Peak Input Voltage	PCLK	500		1000	mV	LVPECL
V_{CMR}[3]	Common Mode Range	PCLK	1.1		V_{CC}–0.7	V	LVPECL
$t_{P, REF}$	Reference Input Pulse Width		1.4			ns	
t_r, t_f	PCLK Input Rise/Fall Time				1.0[4]	ns	0.7 to 1.7V
t_{PLH} t_{PHL}	Propagation Delay	PCLK to any Q PCLK to any Q	2.6 2.6		5.6 5.5	ns ns	
$t_{PLZ, HZ}$	Output Disable Time				10	ns	
$t_{PZL, LZ}$	Output Enable Time				10	ns	
$t_{sk(O)}$	Output-to-Output Skew	Within one bank Any output bank, same output divider Any output, Any output divider			150 200 350	ps ps ps	
$t_{sk(PP)}$	Device-to-Device Skew				3.0	ns	
$t_{SK(P)}$	Output Pulse Skew[5]				200	ps	
DC_Q	Output Duty Cycle	÷1 or ÷2 output	45	50	55	%	DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time		0.1		1.0	ns	0.6 to 1.8V

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. The MPC9456 is functional up to an input and output clock frequency of 350 MHz and is characterized up to 250 MHz.
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} range and the input swing lies within the V_{PP} (AC) specification.
4. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
5. Output pulse skew is the absolute difference of the propagation delay times: | t_{pLH}–t_{pHL} |.

Table 10. AC Characteristics (V_{CC} = 3.3V ± 5%, V_{CCA} = V_{CCB} = V_{CCC} = 2.5V ± 5% or 3.3V ± 5%, T_A = –40 to +85°C)[1, 2]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
$t_{sk(O)}$	Output-to-Output Skew	Within one bank Any output bank, same output divider Any output, Any output divider			150 250 350	ps ps ps	
$t_{sk(PP)}$	Device-to-Device Skew				2.5	ns	
$t_{PLH,HL}$	Propagation Delay	PCLK to any Q	See 3.3V Table				
$t_{SK(P)}$	Output Pulse Skew[3]				250	ps	
DC_Q	Output Duty Cycle	÷1 or ÷2 output	45	50	55	%	DC_{REF} = 50%

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. For all other AC specifications, refer to 2.5V or 3.3V tables according to the supply voltage of the output bank.
3. Output pulse skew is the absolute difference of the propagation delay times: | t_{pLH}–t_{pHL} |.

APPLICATIONS INFORMATION

Driving Transmission Lines

The MPC9456 clock driver was designed to drive high speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of less than 20Ω the drivers can drive either parallel or series terminated transmission lines. For more information on transmission lines the reader is referred to application note AN1091. In most high performance clock networks point-to-point distribution of signals is the method of choice. In a point-to-point scheme either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50Ω resistance to V_{CC}÷2.

This technique draws a fairly high level of DC current and thus only a single terminated line can be driven by each output of the MPC9456 clock driver. For the series terminated case however there is no DC current draw, thus the outputs can drive multiple series terminated lines. Figure 3 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme the fanout of the MPC9456 clock driver is effectively doubled due to its capability to drive multiple lines.

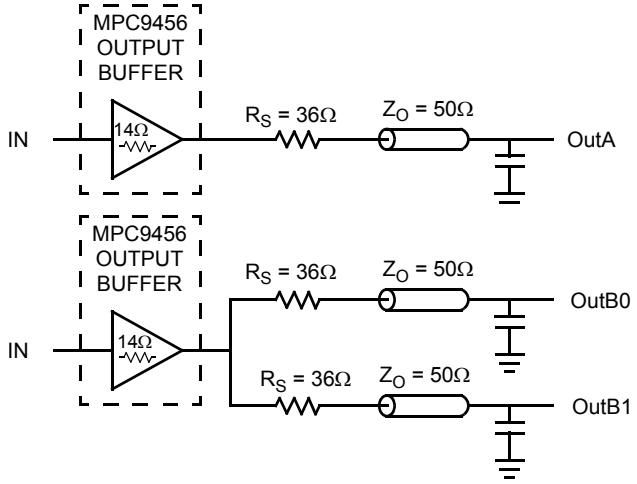


Figure 3. Single versus Dual Transmission Lines

The waveform plots in Figure 4 show the simulation results of an output driving a single line versus two lines. In both cases the drive capability of the MPC9456 output buffer is more than sufficient to drive 50Ω transmission lines on the incident edge. Note from the delay measurements in the simulations a delta of only 43ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9456. The output waveform in Figure 4 shows a step in the waveform, this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 36Ω series resistor plus the output impedance does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$
$Z_0 = 50\Omega \parallel 50\Omega$
$R_S = 36\Omega \parallel 36\Omega$
$R_0 = 14\Omega$
$V_L = 3.0 (25 \div (18 + 14 + 25)$
$= 1.31V$

At the load end the voltage will double, due to the near unity reflection coefficient, to 2.5V. It will then increment towards the quiescent 3.0V in steps separated by one round trip delay (in this case 4.0ns).

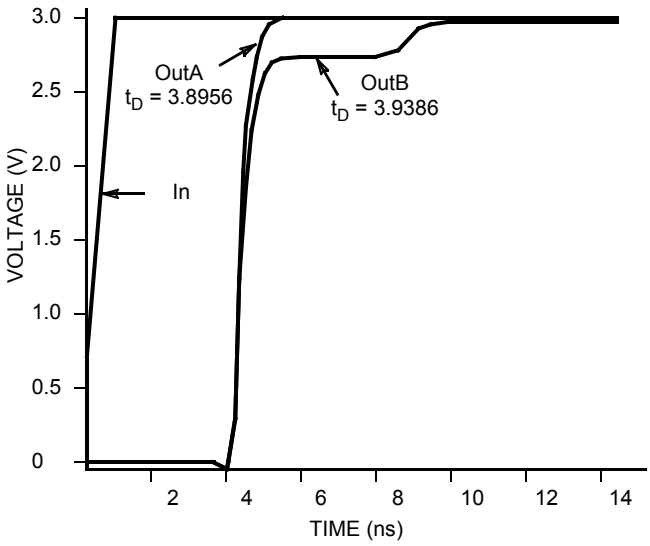


Figure 4. Single versus Dual Waveforms

Since this step is well above the threshold region it will not cause any false clock triggering, however designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines the situation in Figure 5 should be used. In this case the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance the line impedance is perfectly matched.

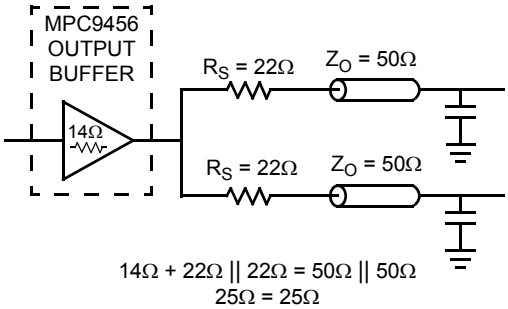


Figure 5. Optimized Dual Line Termination

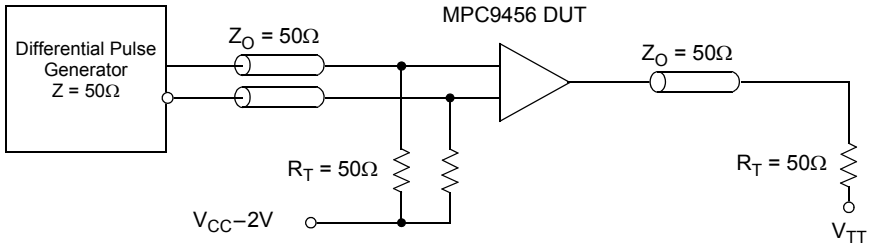


Figure 6. PCLK MPC9456 AC Test Reference for V_{cc} = 3.3V and V_{cc} = 2.5V

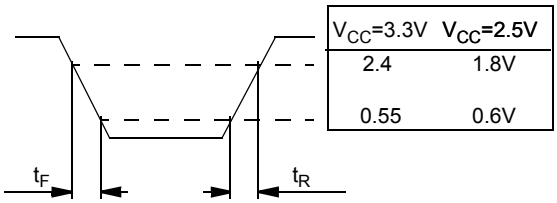


Figure 7. Output Transition Time Test Reference

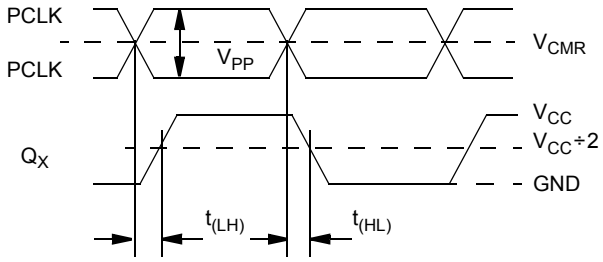
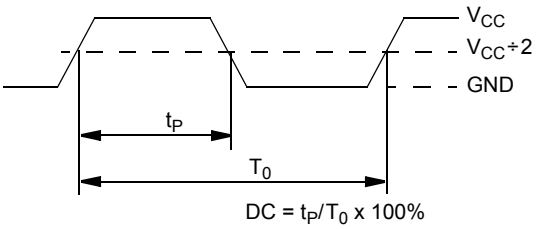
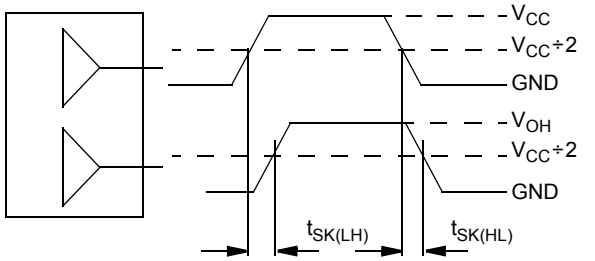


Figure 8. Propagation Delay (t_{PD}) Test Reference



The time from the PLL controlled edge to the non controlled edge, divided by the time between PLL controlled edges, expressed as a percentage

Figure 9. Output Duty Cycle (DC)



The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device

Figure 10. Output-to-Output Skew $t_{SK(O)}$

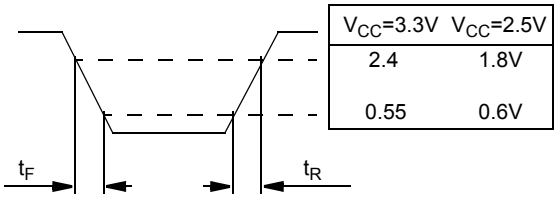


Figure 11. Output Transition Time Test Reference

Chapter Eight
Differential Fanout Buffer Data Sheets

Differential Fanout Buffer Device Index

2.5V / 3.3V ECL 1:2 Differential Fanout Buffer

MC100ES6011

The MC100ES6011 is a differential 1:2 fanout buffer. The ES6011 is ideal for applications requiring lower voltage.

The 100ES Series contains temperature compensation.

Features

- 270 ps Typical Propagation Delay
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: V_{CC} = 2.375 V to 3.8 V with V_{EE} = 0 V
- ECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -2.375 V to -3.8 V
- Open Input Default State
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- LVDS Input Compatible
- 32-lead Pb-free Package Available

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-06

ORDERING INFORMATION

Device	Package
MC100ES6011D	SO-8
MC100ES6011DR2	SO-8

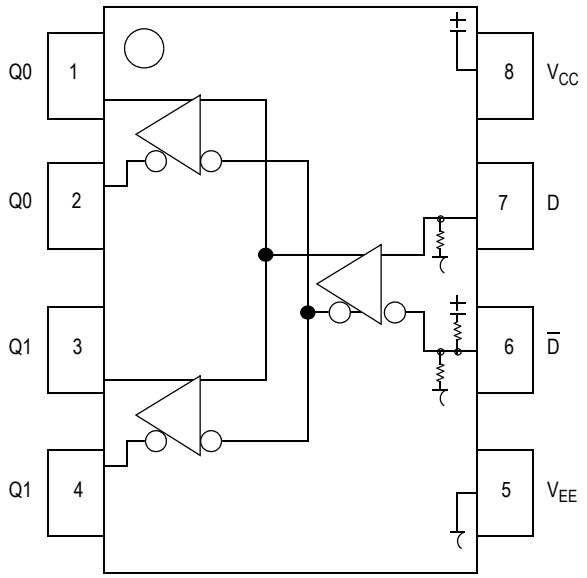


Figure 1. 8-Lead Pinout (Top View) **and Logic Diagram**

PIN DESCRIPTION

Pin	Function
D[1], $\overline{D}$[2]	ECL Data Inputs
Q0, $\overline{Q0}$ Q1, $\overline{Q1}$	ECL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

1. Pins will default LOW when left open.
2. Pins will default to 0.572 V_{CC}/2 when left open.

Table 1. Attributes

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		56 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 4000 V > 200 V > 1500 V
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	190°C/W 130°C/W

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 2. Maximum Ratings[1]

Symbol	Parameter	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	V_{CC}–V_{EE} < 3.6 V	V_{CC} +0.3 V_{EE} –0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
TA	Operating Temperature Range		–40 to +85	°C
T_{stg}	Storage Temperature Range		–65 to +150	°C

1. Absolute maxim continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics (V_{CC} = 0 V; V_{EE} = –2.5 V ± 5% or V_{CC} = 2.5 V ± 5%; V_{EE} = 0 V)[1]

Symbol	Characteristic	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		12	25		12	25	mA
V_{OH}	Output HIGH Voltage[2]	V_{CC}–1160	V_{CC}–1005	V_{CC}–880	V_{CC}–1100	V_{CC}–955	V_{CC}–740	mV
V_{OL}	Output LOW Voltage[2]	V_{CC}–1830	V_{CC}–1605	V_{CC}–1305	V_{CC}–1810	V_{CC}–1705	V_{CC}–1405	mV
V_{OUTPP}	Output Peak-to-Peak Voltage	200			200			mV
V_{IH}	Input HIGH Voltage (Single Ended)	V_{CC}–1165		V_{CC}–880	V_{CC}–1165		V_{CC}–880	mV
V_{IL}	Input LOW Voltage (Single Ended)	V_{CC}–1810		V_{CC}–1475	V_{CC}–1810		V_{CC}–1475	mV
V_{PP}	Differential Input Voltage[3]	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage[4]	V_{EE} +1.0		V_{CC} –0.8	V_{EE} +1.0		V_{CC}–0.8	V
I_{IN}	Input Current			±150			±150	μA

1. ES6011 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow > 500 LFPM is maintained.
2. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
3. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
4. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. DC Characteristics (V_{CC} = 0 V; V_{EE} = –3.8 to –3.135 or V_{CC} = 3.8 to 3.135 V; V_{EE} = 0 V)[1]

Symbol	Characteristic	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		12	25		12	25	mA
V_{OH}	Output HIGH Voltage[2]	V_{CC} –1160	V_{CC} –1005	V_{CC} –880	V_{CC} –1100	V_{CC}–955	V_{CC} –740	mV
V_{OL}	Output LOW Voltage[2]	V_{CC} –1830	V_{CC} –1705	V_{CC} –1405	V_{CC} –1830	V_{CC} –1705	V_{CC} –1405	mV
V_{OUTPP}	Output Peak-to-Peak Voltage	200			200			mV
V_{IH}	Input HIGH Voltage (Single Ended)	V_{CC} –1165		V_{CC} –880	V_{CC} –1165		V_{CC} –880	mV
V_{IL}	Input LOW Voltage (Single Ended)	V_{CC} –1810		V_{CC} –1475	V_{CC} –1810		V_{CC} –1475	mV
V_{PP}	Differential Input Voltage[3]	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage[4]	V_{EE} +1.0		V_{CC} –0.8	V_{EE} +1.0		V_{CC} –0.8	V
I_{IN}	Input Current			±150			±150	μA

1. ES6011 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow > 500 LFPM is maintained.
2. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
3. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
4. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 5. AC Characteristics (V_{CC} = 0 V; V_{EE} = –3.8 to –2.375 or V_{CC} = 2.375 to 3.8 V; V_{EE} = 0 V)[1]

Symbol	Characteristic	–40°C			25°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Maximum Frequency		> 3			> 3			> 3		GHz
t_{PLH}, t_{PHL}	Propagation Delay (Differential) CLK to Q, $\overline{Q}$	170	260	300	180	270	310	210	285	360	ps
t_{SKEW}	Within Device Skew Q, $\overline{Q}$ Device-to-Device Skew[2]		9	20 130		9	20 130		9	20 150	ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1σ)			1			1			1	ps
V_{PP}	Input Voltage Swing (Differential)	150		1200	150		1200	150		1200	mV
V_{CMR}	Differential Cross Point Voltage	V_{EE} +1.2		V_{CC}–1.1	V_{EE} +1.2		V_{CC} –1.1	V_{EE} +1.2		V_{CC} –1.1	V
t_r t_f	Output Rise/Fall Times (20% – 80%)	70		220	70		220	70		220	ps

1. Measured using a 750 mV source 50% Duty Cycle clock source. All loading with 50 Ω to V_{CC}–2.0 V.
2. Skew is measured between outputs under identical transitions.

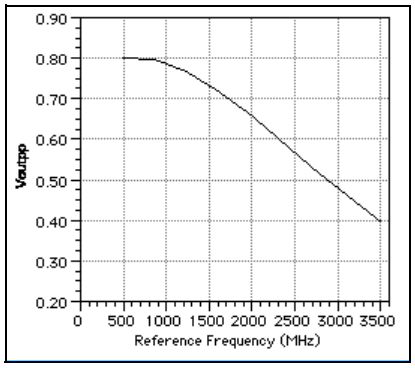


Figure 2. V_{OUTPP} versus Frequency

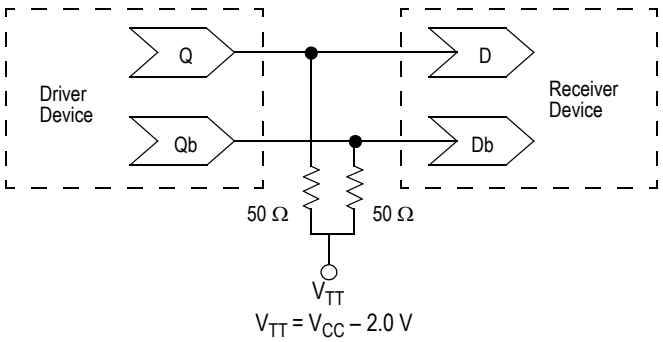


Figure 3. Typical Termination for Output Driver and Device Evaluation

Marking Notes:

Device Nomenclature	8-Lead SOIC Marking
MC100ES6011D	M6011

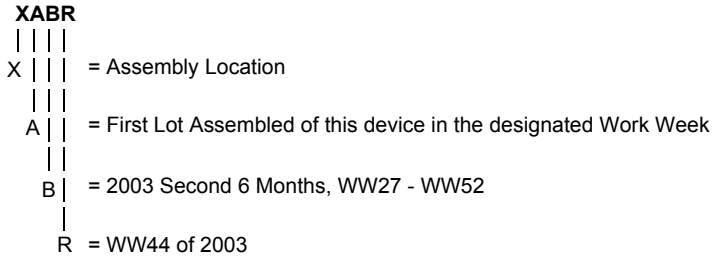
Trace Code Identification:

"A" — The First character indicates the Assembly location.
"L" — The Second character indicates the Source Wafer Lot Tracking Code.
"Y" — The Third character indicates the "ALPHA CODE" of the year device was assembled.
"W" — The Fourth character indicates the "ALPHA CODE" of the Work Week device was assembled.

The "Y" Year ALPHA CODES		
Year	**Month**	**Work Week Code**
A = 2003	FIRST 6 MONTHS	WW01 – WW26
B = 2003	SECOND 6 MONTHS	WW27 – WW52
C = 2004	FIRST 6 MONTHS	WW01 – WW26
D = 2004	SECOND 6 MONTHS	WW27 – WW52
E = 2005	FIRST 6 MONTHS	WW01 – WW26
F = 2005	SECOND 6 MONTHS	WW27 – WW52
G = 2006	FIRST 6 MONTHS	WW01 – WW26
H = 2006	SECOND 6 MONTHS	WW27 – WW52
I = 2007	FIRST 6 MONTHS	WW01 – WW26
J = 2007	SECOND 6 MONTHS	WW27 – WW52
K = 2008	FIRST 6 MONTHS	WW01 – WW26
L = 2008	SECOND 6 MONTHS	WW27 – WW52
M = 2009	FIRST 6 MONTHS	WW01 – WW26
N = 2009	SECOND 6 MONTHS	WW27 – WW52
O = 2010	FIRST 6 MONTHS	WW01 – WW26
P = 2010	SECOND 6 MONTHS	WW27 – WW52
Q = 2011	FIRST 6 MONTHS	WW01 – WW26
R = 2011	SECOND 6 MONTHS	WW27 – WW52
S = 2012	FIRST 6 MONTHS	WW01 – WW26
T = 2012	SECOND 6 MONTHS	WW27 – WW52
U = 2013	FIRST 6 MONTHS	WW01 – WW26
V = 2013	SECOND 6 MONTHS	WW27 – WW52
W = 2014	FIRST 6 MONTHS	WW01 – WW26
X = 2014	SECOND 6 MONTHS	WW27 – WW52
Y = 2015	FIRST 6 MONTHS	WW01 – WW26
Z = 2015	SECOND 6 MONTHS	WW27 – WW52

The "W" Work Week ALPHA CODES	
1st 6 Months (WW01 – WW26)	**2nd 6 Months (WW27 – WW52)**
A = WW01	A = WW27
B = WW02	B = WW28
C = WW03	C = WW29
D = WW04	D = WW30
E = WW05	E = WW31
F = WW06	F = WW32
G = WW07	G = WW33
H = WW08	H = WW34
I = WW09	I = WW35
J = WW10	J = WW36
K = WW11	K = WW37
L = WW12	L = WW38
M = WW13	M = WW39
N = WW14	N = WW40
O = WW15	O = WW41
P = WW16	P = WW42
Q = WW17	Q = WW43
R = WW18	R = WW44
S = WW19	S = WW45
T = WW20	T = WW46
U = WW21	U = WW47
V = WW22	V = WW48
W = WW23	W = WW49
X = WW24	X = WW50
Y = WW25	Y = WW51
Z = WW26	Z = WW52

Marking Example:



Order number: MC100ES6014
Rev 2, 5/2004

2.5V / 3.3V 1:5 Differential ECL/PECL/HSTL/LVDS Clock Driver

MC100ES6014

DT SUFFIX
20 LEAD TSSOP PACKAGE
CASE 948E-02

The MC100ES6014 is a low skew 1-to-5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The ECL/PECL input signals can be either differential or single-ended (if the V_{BB} output is used). HSTL and LVDS inputs can be used when the ES6014 is operating under PECL conditions.

The ES6014 specifically guarantees low output-to-output skew. Optimal design, layout, and processing minimize skew within a device and from device to device.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated identically into 50 Ω even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

The common enable ($\overline{EN}$) is synchronous, outputs are enabled/disabled in the LOW state. This avoids a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock; therefore, all associated specification limits are referenced to the negative edge of the clock input.

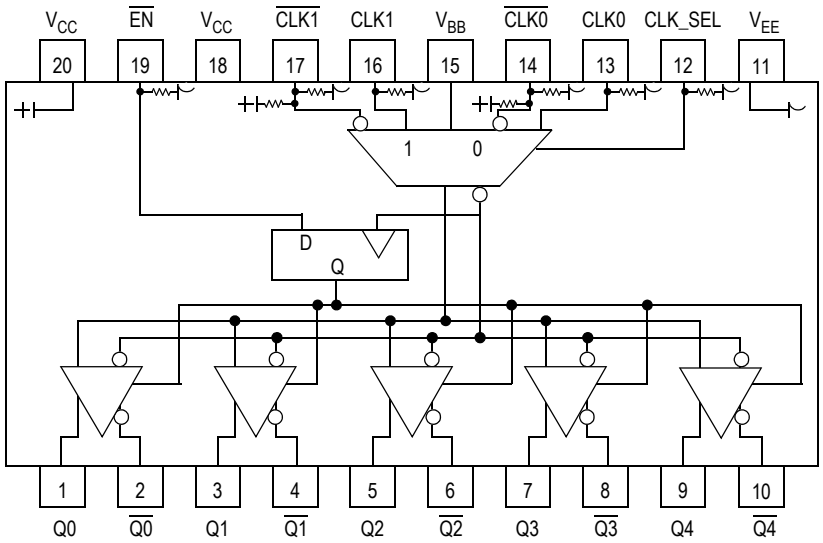
The MC100ES6014, as with most other ECL devices, can be operated from a positive V_{CC} supply in PECL mode. This allows the ES6014 to be used for high performance clock distribution in +3.3 V or +2.5 V systems. Single ended CLK input pin operation is limited to a $V_{CC} \geq 3.0$ V in PECL mode, or $V_{EE} \leq -3.0$ V in ECL mode. Designers can take advantage of the ES6014's performance to distribute low skew clocks across the backplane or the board.

ORDERING INFORMATION

Device	Package
MC100ES6014DT	TSSOP-20
MC100ES6014DTR2	TSSOP-20

Features

- 25 ps Within Device Skew
- 400 ps Typical Propagation Delay
- Maximum Frequency > 2 GHz Typical
- The 100 Series Contains Temperature Compensation
- PECL and HSTL Mode: V_{CC} = 2.375 V to 3.8 V with V_{EE} = 0 V
- ECL Mode: V_{CC} = 0 V with V_{EE} = –2.375 V to –3.8 V
- LVDS and HSTL Input Compatible
- Open Input Default State



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View) **and Logic Diagram**

Table 1. Pin Description

Pin	Function
CLK0*, $\overline{\text{CLK0}}$**	ECL/PECL/HSTL CLK Input
CLK1*, $\overline{\text{CLK1}}$**	ECL/PECL/HSTL CLK Input
Q0:4, $\overline{\text{Q0:4}}$	ECL/PECL Outputs
CLK_SEL*	ECL/PECL Active Clock Select Input
$\overline{\text{EN}}$*	ECL Sync Enable
V_{BB}	Reference Voltage Output
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default LOW when left open.
** Pins will default to $V_{CC}/2$ when left open.

Table 2. Function Table

CLK0	CLK1	CLK_SEL	$\overline{\text{EN}}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK0 or CLK1

Table 3. General specifications

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2000 V > 200 V > 1500 V
Thermal Resistance (Junction-to-Ambient)	0 LFPM, 20 TSSOP 500 LFPM, 20 TSSOP	140°C/W 100°C/W

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristic	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	V_{CC} + 0.3 V_{EE} – 0.3	V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
I_{BB}	V_{BB} Sink/Source Current		±0.5	°C
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 0 V, V_{EE} = –2.5 V±5% or V_{CC} = 2.5 V±5%, V_{EE} = 0 V)

Symbol	Characteristics	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	60		30	60	mA
V_{OH}	Output HIGH Voltage[1]	V_{CC}–1250	V_{CC}–990	V_{CC}–800	V_{CC}–1200	V_{CC}–960	V_{CC}–750	mV
V_{OL}	Output LOW Voltage[1]	V_{CC}–2000	V_{CC}–1550	V_{CC}–1150	V_{CC}–1925	V_{CC}–1630	V_{CC}–1200	mV
V_{outPP}	Output Peak-to-Peak Voltage	200			200			mV
V_{IH}	Input HIGH Voltage	V_{CC}–1165		V_{CC}–880	V_{CC}–1165		V_{CC}–880	mV
V_{IL}	Input LOW Voltage	V_{CC}–1810		V_{CC}–1475	V_{CC}–1810		V_{CC}–1475	mV
V_{BB}	Output Reference Voltage I_{BB} = 200 μA	V_{CC}–1400		V_{CC}–1200	V_{CC}–1400		V_{CC}–1200	mV
V_{PP}	Differential Input Voltage[2]	0.12		1.3	0.12		1.3	mV
V_{CMR}	Differential Cross Point Voltage[3]	V_{EE}+0.2		V_{CC}–1.0	V_{EE}+0.2		V_{CC}–1.0	mV
I_{IN}	Input Current			±150			±150	μA

1. Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. DC Characteristics (V_{CC} = 0 V, V_{EE} = –3.8 V to –3.135 V or V_{CC} = 3.135 V to 3.8 V, V_{EE} = 0 V)

Symbol	Characteristics	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	60		30	60	mA
V_{OH}	Output HIGH Voltage[1]	V_{CC}–1150	V_{CC}–1020	V_{CC}–800	V_{CC}–1200	V_{CC}–970	V_{CC}–750	mV
V_{OL}	Output LOW Voltage[1]	V_{CC}–1950	V_{CC}–1620	V_{CC}–1250	V_{CC}–2000	V_{CC}–1680	V_{CC}–1300	mV
V_{outPP}	Output Peak-to-Peak Voltage	200			200			mV
V_{IH}	Input HIGH Voltage	V_{CC}–1165		V_{CC}–880	V_{CC}–1165		V_{CC}–880	mV
V_{IL}	Input LOW Voltage	V_{CC}–1810		V_{CC}–1475	V_{CC}–1810		V_{CC}–1475	mV
V_{BB}	Output Reference Voltage I_{BB} = 200 μA	V_{CC}–1400		V_{CC}–1200	V_{CC}–1400		V_{CC}–1200	mV
V_{PP}	Differential Input Voltage[2]	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage[3]	V_{EE}+0.2		V_{CC}–1.1	V_{EE}+0.2		V_{CC}–1.1	V
I_{IN}	Input Current			±150			±150	μA

1. Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 7. AC Characteristics (V_{CC} = 0 V, V_{EE} = –3.8 V to –3.135 V or V_{CC} = 3.135 V to 3.8 V, V_{EE} = 0 V)[1]

Symbol	Characteristics	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Output Frequency	2			2			2			GHz
t_{PLH} t_{PHL}	Propagation Delay (Differential) CLK to Q, $\overline{Q}$	300	355	425	300	375	475	300	400	525	ps
t_{SKEW}	Within Device Skew[2] Q, $\overline{Q}$ Device-to-Device Skew[2]		23	45 125		23	45 175		23	45 225	ps ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1σ)			1			1			1	ps
V_{PP}	Input Peak-to-Peak Voltage Swing (Differential)	200		1200	200		1200	200		1200	mV
V_{CMR}	Differential Cross Point Voltage	V_{EE}+0.2		V_{CC}–1.2	V_{EE}+0.2		V_{CC}–1.2	V_{EE}+0.2		V_{CC}–1.2	V
t_r/t_f	Output Rise/Fall Time (20%–80%)	70		225	70		250	70		275	ps

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to V_{CC}–2.0 V.
2. Skew is measured between outputs under identical transitions.

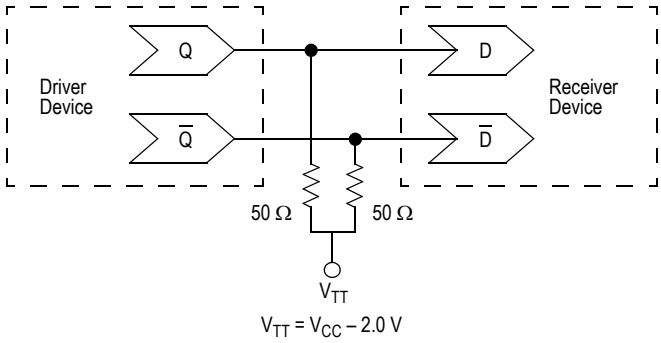


Figure 2. Typical Termination for Output Driver and Device Evaluation

Marking Notes:

Device Nomenclature	20-Lead TSSOP Marking
MC100ES6014DT	6014

Trace Code Identification for 20 TSSOP: ALYW

"A" – The First character indicates the Assembly location.
"L" – The Second character indicates the Source Wafer Lot Tracking Code.
"Y" – The Third character indicates the "ALPHA CODE" of the year device was assembled.
"W" – The Fourth character indicates the "ALPHA CODE" of the Work Week device was assembled.

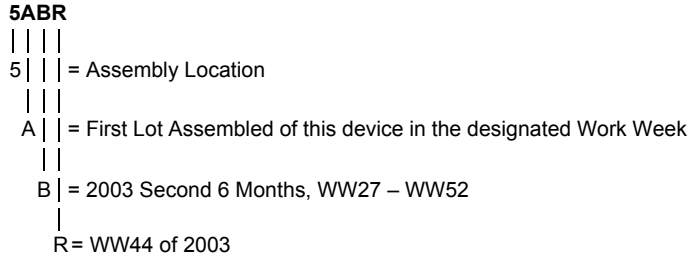
The "Y" Year ALPHA CODES

Year	Month	Work Week Code
A = 2003	FIRST 6 MONTHS	WW01 – WW26
B = 2003	SECOND 6 MONTHS	WW27 – WW52
C = 2004	FIRST 6 MONTHS	WW01 – WW26
D = 2004	SECOND 6 MONTHS	WW27 – WW52
E = 2005	FIRST 6 MONTHS	WW01 – WW26
F = 2005	SECOND 6 MONTHS	WW27 – WW52
G = 2006	FIRST 6 MONTHS	WW01 – WW26
H = 2006	SECOND 6 MONTHS	WW27 – WW52
I = 2007	FIRST 6 MONTHS	WW01 – WW26
J = 2007	SECOND 6 MONTHS	WW27 – WW52
K = 2008	FIRST 6 MONTHS	WW01 – WW26
L = 2008	SECOND 6 MONTHS	WW27 – WW52
M = 2009	FIRST 6 MONTHS	WW01 – WW26
N = 2009	SECOND 6 MONTHS	WW27 – WW52
O = 2010	FIRST 6 MONTHS	WW01 – WW26
P = 2010	SECOND 6 MONTHS	WW27 – WW52
Q = 2011	FIRST 6 MONTHS	WW01 – WW26
R = 2011	SECOND 6 MONTHS	WW27 – WW52
S = 2012	FIRST 6 MONTHS	WW01 – WW26
T = 2012	SECOND 6 MONTHS	WW27 – WW52
U = 2013	FIRST 6 MONTHS	WW01 – WW26
V = 2013	SECOND 6 MONTHS	WW27 – WW52
W = 2014	FIRST 6 MONTHS	WW01 – WW26
X = 2014	SECOND 6 MONTHS	WW27 – WW52
Y = 2015	FIRST 6 MONTHS	WW01 – WW26
Z = 2015	SECOND 6 MONTHS	WW27 – WW52

The "W" Work Week ALPHA CODES

1st 6 Months (WW01 – WW26)	2nd 6 Months (WW27 – WW52)
A = WW01	A = WW27
B = WW02	B = WW28
C = WW03	C = WW29
D = WW04	D = WW30
E = WW05	E = WW31
F = WW06	F = WW32
G = WW07	G = WW33
H = WW08	H = WW34
I = WW09	I = WW35
J = WW10	J = WW36
K = WW11	K = WW37
L = WW12	L = WW38
M = WW13	M = WW39
N = WW14	N = WW40
O = WW15	O = WW41
P = WW16	P = WW42
Q = WW17	Q = WW43
R = WW18	R = WW44
S = WW19	S = WW45
T = WW20	T = WW46
U = WW21	U = WW47
V = WW22	V = WW48
W = WW23	W = WW49
X = WW24	X = WW50
Y = WW25	Y = WW51
Z = WW26	Z = WW52

20 TSSOP Tracecode Marking Example:



3.3 V Dual LVTTL/LVCMOS to Differential LVPECL Translator

MC100ES60T22

The MC100ES60T22 is a low skew dual LVTTL/LVCMOS to differential LVPECL translator. The low voltage PECL levels, small package, and dual gate design are ideal for clock translation applications.

Features

- 280 ps typical propagation delay
- 100 ps max output-to-output skew
- LVPECL operating range: V_{CC} = 3.135 V to 3.8 V
- 8-lead SOIC package

Ambient temperature range –40°C to +85°C

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-06

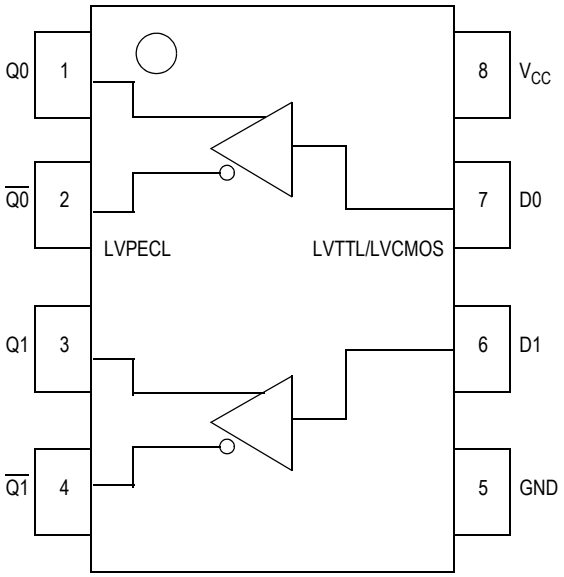


Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

ORDERING INFORMATION

Device	Package
MC100ES60T22D	SO-8
MC100ES60T22DR2	SO-8

PIN DESCRIPTION

Pin	Function
D0, D1	LVTTL/LVCMOS Inputs
Qn, $\overline{Qn}$	LVPECL Differential Outputs
V_{CC}	Positive Supply
GND	Negative Supply

Table 1. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model	> 2000 V > 200 V
θ_{JA} Thermal Resistance (Junction-to-Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	190°C/W 130°C/W

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 2. Absolute Maximum Ratings[1]

Symbol	Rating	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{out}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics (V_{CC} = 3.135 V to 3.8 V; V_{EE} = 0 V)

Symbol	Characteristic	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{GND}	Power Supply Current			17			22	mA
V_{OH}[1]	Output HIGH Voltage	V_{CC} – 1150	V_{CC} – 1020	V_{CC} – 800	V_{CC} – 1200	V_{CC} – 970	V_{CC} – 750	mV
V_{OL}[1]	Output LOW Voltage	V_{CC} – 1950	V_{CC} – 1620	V_{CC} – 1250	V_{CC} – 2000	V_{CC} – 1680	V_{CC} – 1300	mV

1. Outputs are terminated through a 50 Ω resistor to V_{CC} – 2 volts

Table 4. LVTTL / LVCMOS Input DC Characteristics (V_{CC} = 3.135 V to 3.8 V)

Symbol	Characteristic	Condition	–40°C			0°C to 85°C			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{IN}	Input Current	$V_{IN} = V_{CC}$			±150			±150	μA
V_{IK}	Input Clamp Voltage	I_{IN} = –18 mA			–1.2			–1.2	V
V_{IH}	Input HIGH Voltage		2.0		V_{CC}+0.3	2.0		V_{CC}+0.3	V
V_{IL}	Input LOW Voltage				0.8			0.8	V

Table 5. AC Characteristics (V_{CC} = 3.134 V to 3.8 V; V_{EE} = 0 V)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency			1			1			1	GHz
t_{PLH}, t_{PHL}	Propagation Delay	100	260	400	100	280	400	100	280	450	ps
t_{SKEW}	Skew part-to-part			300			300			350	ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1σ)			1			1			1	ps
V_{outPP}	Output Peak-to-Peak Voltage	350	750		350	750		350	750		mV
t_r / t_f	Output Rise/Fall Times (20% – 80%)	50		400	50		400	50		400	ps

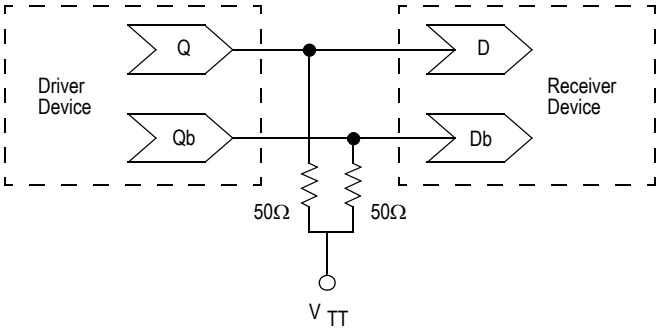


Figure 2. Typical Termination for Output Driver and Device Evaluation

Product Preview

3.3 V Dual Differential LVPECL-to-LVTTL Translator

The MC100ES60T23 is a dual differential LVPECL-to-LVTTL translator. The low voltage PECL levels, small package, and dual gate design is ideal for clock translation applications.

Features

- Maximum Frequency > 180 MHz
- Differential LVPECL Inputs
- LVPECL Operating Range: V_{CC} = 3.0 V to 3.6 V
- 24 mA LVTTL Compatible Outputs
- 8-Lead SOIC and 8-Lead TSSOP Packages
- Ambient Temperature Range: –40°C to +85°C

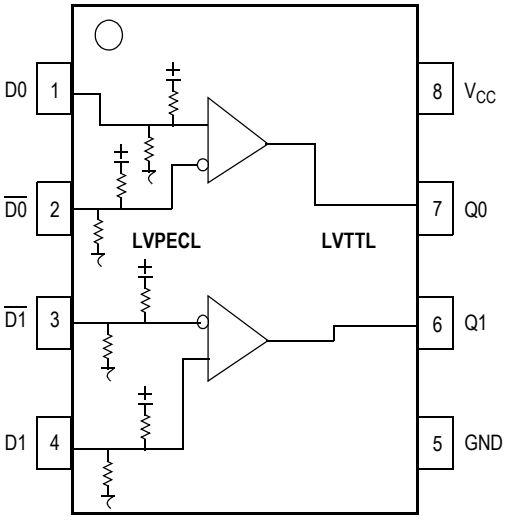


Figure 1. 8-Lead Pinout (Top View**) and Logic Diagram**

MC100ES60T23

DUAL LVPECL TO LVTTL TRANSLATOR

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-06

DT SUFFIX
8-LEAD TSSOP PACKAGE
CASE TBD

ORDERING INFORMATION

Device	Package
MC100ES60T23D	SO-8
MC100ES60T23DR2	SO-8
MC100ES60T23DT	TSSOP-8
MC100ES60T23DTR2	TSSOP-8

PIN DESCRIPTION

Pin	Function
Qn	LVTTL Outputs
Dn, $\overline{Dn}$	LVPECL Differential Inputs
V_{CC}	Positive Supply
GND	Negative Supply

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table 1. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor	D $\overline{D}$	75 kΩ 112.5 kΩ
Internal Input Pullup Resistors		75 kΩ
ESD Protection	Human Body Model Machine Model	> 2000 V > 200 V
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	190 °C/W 130 °C/W
	0 LFPM, 8 TSSOP 500 LFPM, 8 TSSOP	TBD TBD

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 2. Absolute Maximum Ratings[1]

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} and V_{EE}	3.9	V
V_{IN}	Input Voltage	V_{CC}–V_{EE} ≤ 3.6 V	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. LVPECL Input DC Characteristics (V_{CC} = 3.0 to 3.6 V; V_{EE} = 0 V)

Symbol	Characteristic	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{CCH}	Power Supply Current (Outputs set to HIGH)		18	25		18	25	mA
I_{CCL}	Power Supply Current (Outputs set to LOW)		26	33		26	33	mA
V_{IH}	Input HIGH Voltage	V_{CC}–1165		V_{CC}–880	V_{CC}–1165		V_{CC}–880	mV
V_{IL}	Input LOW Voltage	V_{CC}–1810		V_{CC}–1475	V_{CC}–1810		V_{CC}–1475	mV
V_{PP}	Differential Input Voltage[1]	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage[2]	V_{EE} +1.5		V_{CC}–0.65	V_{EE} +1.5		V_{CC}–0.65	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current D $\overline{D}$	 –150		0.5	 –150		0.5	μA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. LVTTL / LVCMOS Output DC Characteristics (V_{CC} = 3.0 to 3.6 V)

Symbol	Characteristic	Condition	–40°C			0°C to 85°C			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = –24 mA	2.4			2.4			V
V_{0L}	Output LOW Voltage	I_{OL} = 24 mA			0.5			0.5	V
I_{0S}	Output Short Circuit Current			–150			–150		mA

Table 5. AC Characteristics (V_{CC} = 3.0 to 3.6 V; V_{EE} = 0 V)[1]

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency[2]	180			180			180			MHz
t_{PLH} t_{PHL}	Propagation Delay	1.0	1.5	2.5	1.0	1.7	2.5	1.0	1.7	2.5	ns
t_{SK++} t_{SK--} t_{SKPP} t_{SKPW}	Data Path Skew++[3] Data Path Skew--[3] Part-to-Part Skew[3] Pulse Width Skew[3]			60 25 500 250			60 25 500 250			60 25 500 250	ps ps ps ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1 σ)			1			1			1	ps
V_{PP}	Input Voltage Swing (Differential)[4]	200	800	1000	200	800	1000	200	800	1000	mV
t_r / t_f	Output Rise/Fall Times (0.8 V – 2.0 V)	120			120			120			ps

1. LVTTL output R_L = 500 Ω to GND and C_L = 20 pF to GND. Refer to **Figure 2**.
2. f_{max} guaranteed for functionality only. V_{OL} and V_{OH} levels are guaranteed at DC only.
3. Skews are measured between outputs under identical conditions.
4. 200 mV input guarantees full logic swing at the output.

Figure 2. TTL Output Loading Used for Device Evaluation

Order number: MC100ES6030
Rev 0, 06/2004

Preliminary Information

2.5/3.3 V ECL Triple D Flip-Flop with Set and Reset

MC100ES6030

The MC100ES6030 is a triple master-slave D flip-flop with differential outputs. When the clock input is low, data enters the master latch and transfers to the slave during a positive transition on the clock input.

Each flip-flop has individual Reset inputs while the Set input is shared. The Set and Reset inputs are asynchronous and override the clock inputs.

Features

- 1.2 GHz minimum toggle frequency
- 450 ps typical propagation delay
- LVPECL operating range: V_{CC} = 2.375 V to 3.8 V, V_{EE} = 0 V
- LVECL operating range: V_{CC} = 0 V, V_{EE} = –2.375 V to –3.8 V
- 20-lead SOIC package
- Ambient temperature range –40°C to +85°C

DW SUFFIX
20-LEAD SOIC PACKAGE
CASE 751D-06

OREDERING INFORMATION

Device	Package
MC100ES6030DW	SO-20
MC100ES6030DWR2	SO-20

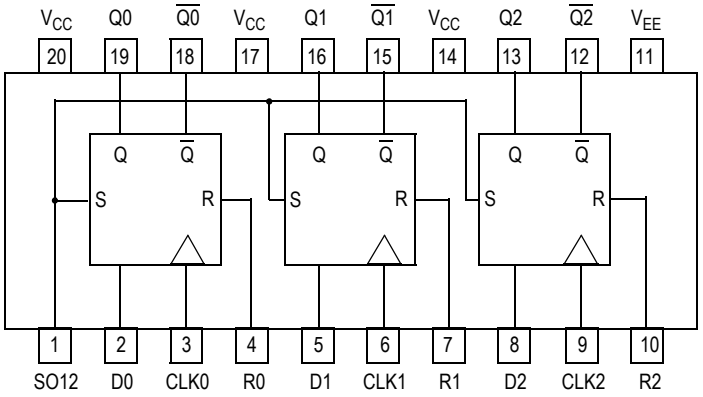


Figure 1. 20-Lead Pinout (Top View) **and Logic Diagram**

PIN DESCRIPTION

Pin	Function
D0–D2	ECL Data Inputs
R0–R2	ECL Reset Inputs
CLK0–CLK2	ECL Clock Inputs
SO12	ECL Common Set Input
Q0–Q2, $\overline{Q0}$–$\overline{Q2}$	ECL Differential Data Outputs
VCC	Positive Supply
VEE	Negative Supply

TRUTH TABLE

R	S	D	CLK	Q	$\overline{Q}$
L	L	L	Z	L	H
L	L	H	Z	H	L
H	L	X	X	L	H
L	H	X	X	H	L
H	H	X	X	Undef	Undef

Z = LOW to HIGH Transition
X = Don't Care

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table 1. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		TBD
Internal Input Pullup Resistor		TBD
ESD Protection	Human Body Model Machine Model Charged Device Model	TBD TBD TBD
θ_{JA} Thermal Resistance (Junction-to-Ambient)	0 LFPM, 20 SOIC 500 LFPM, 20 SOIC	TBD TBD

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 2. Absolute Maximum Ratings[1]

Symbol	Rating	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{out}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{store}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics (V_{CC} = 0 V, V_{EE} = –2.5 V ± 5% or –3.8 V to –3.135 V; V_{CC} = 2.5 V ± 5% or 3.135 V to 3.8 V, V_{EE} = 0 V)

Symbol	Characteristic	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		TBD			TBD		mA
V_{OH}	Output HIGH Voltage[1]	V_{CC}–1085	V_{CC}–1005	V_{CC}–880	V_{CC}–1025	V_{CC}–955	V_{CC}–880	mV
V_{OL}	Output LOW Voltage[1]	V_{CC}–1830	V_{CC}–1695	V_{CC}–1555	V_{CC}–1810	V_{CC}–1705	V_{CC}–1620	mV
V_{IH}	Input HIGH Voltage	V_{CC}–1165		V_{CC}–880	V_{CC}–1165		V_{CC}–880	mV
V_{IL}	Input LOW Voltage	V_{CC}–1810		V_{CC}–1475	V_{CC}–1810		V_{CC}–1475	mV
I_{IN}	Input Current			±150			±150	μV

1. Outputs are terminated through a 50Ω resistor to V_{CC}–2 volts. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported, but the power consumption of the device will increase.

Table 4. AC Characteristics (V_{CC} = 0 V, V_{EE} = –2.5 V ± 5% or –3.8 V to –3.135 V; V_{CC} = 2.5 V ± 5% or 3.135 V to 3.8 V, V_{EE} = 0 V)

Symbol	Characteristic		–40°C			25°C			85°C			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency		1.2			1.2			1.2			GHz
t_{PLH} t_{PHL}	Propagation Delay to Output	CLK S, R					600					ps
t_s t_h	Setup Time Hold Time		150 200	0 100		150 200	0 100		150 200	0 100		ps ps
t_{RR}	Set/Reset Recovery		200	100		200	100		200	100		ps
t_{PW}	Minimum Pulse Width	CLK S, R	400 650			400 650			400 650			ps ps
t_{JITTER}	Cycle-to-Cycle Jitter			< 2			< 2			< 2		ps
t_r/t_f	Output Rise/Fall Time (20%–80%)		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ps

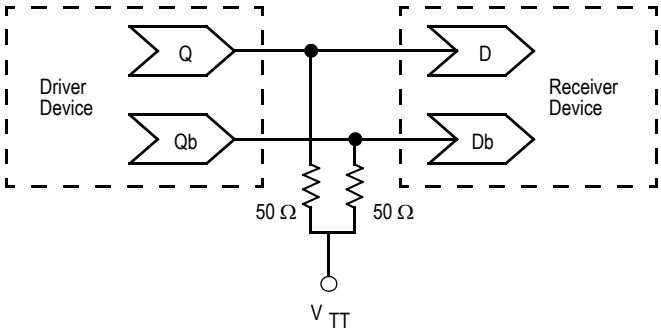


Figure 3. Typical Termination for Output Driver and Device Evaluation

Order number: MC100ES6039
Rev 1, 06/2004

3.3 V ECL/PECL/HSTL/LVDS ÷2/4, ÷4/6 Clock Generation Chip

MC100ES6039

DW SUFFIX
20 LEAD SOIC PACKAGE
CASE 751D-06

The MC100ES6039 is a low skew ÷2/4, ÷4/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, LVPECL input signals. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple ES6039s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one ES6039, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2/4 and the ÷4/6 outputs of a single device. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation.

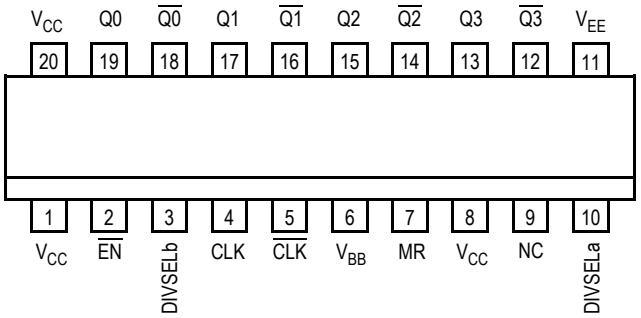
The 100ES Series contains temperature compensation.

Features

- Maximum Frequency >1.0 GHz Typical
- 50 ps Output-to-Output Skew
- PECL Mode Operating Range: V_{CC} = 3.135 V to 3.8 V with V_{EE} = 0 V
- ECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –3.135 V to –3.8 V
- Open Input Default State
- Synchronous Enable/Disable
- Master Reset for Synchronization of Multiple Chips
- V_{BB} Output
- LVDS and HSTL Input Compatible

ORDERING INFORMATION

Device	Package
MC100ES6039DW	SO-20
MC100ES6039DWR2	SO-20



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View)

Table 1. Pin Description

Pin	Function
CLK[1], $\overline{CLK}$[1]	ECL Diff Clock Inputs
$\overline{EN}$[1]	ECL Sync Enable
MR[1]	ECL Master Reset
V_{BB}	ECL Reference Output
Q0, Q1, $\overline{Q0}$, $\overline{Q1}$	ECL Diff ÷2/4 Outputs
Q2, Q3, $\overline{Q2}$, $\overline{Q3}$	ECL Diff ÷4/6 Outputs
DIVSELa[1]	ECL Freq. Select Input ÷2/4
DIVSELb[1]	ECL Freq. Select Input ÷4/6
V_{CC}	ECL Positive Supply
V_{EE}	ECL Negative Supply
NC	No Connect

1. Pins will default low when left open.

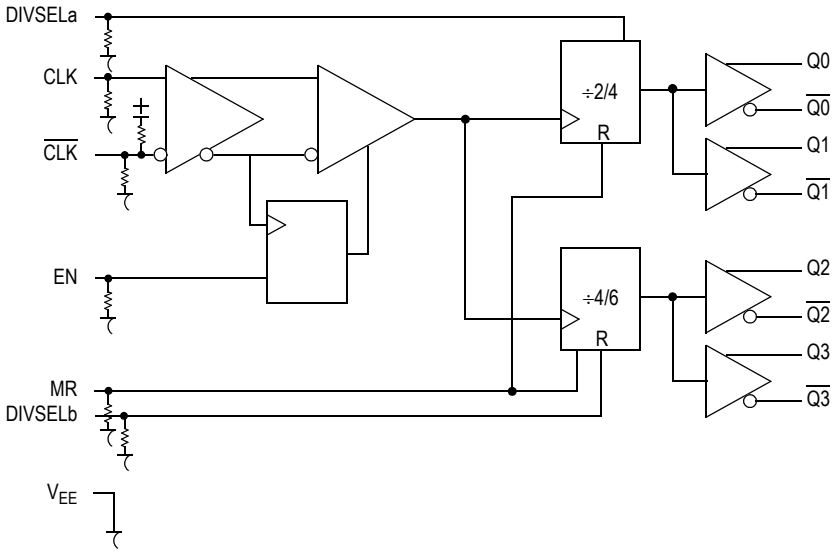


Figure 2. Logic Diagram

Table 2. Function Tables

CLK	$\overline{EN}$	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q0:3
X	X	H	Reset Q0:3

X = Don't Care
Z = Low-to-High Transition
ZZ = High-to-Low Transition

DIVSELa	Q0:1 Outputs
L	Divide by 2
H	Divide by 4
DIVSELb	Q2:3 Outputs
L	Divide by 4
H	Divide by 6

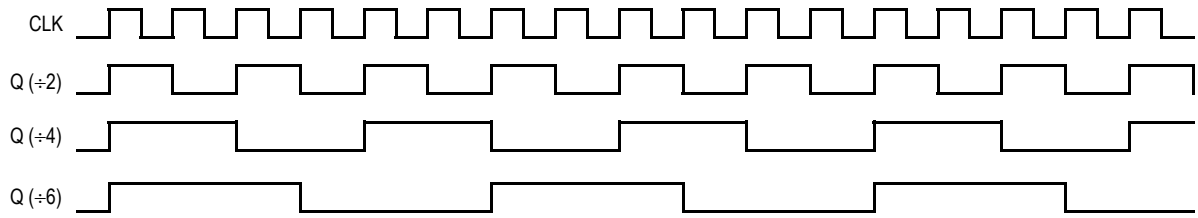


Figure 3. Timing Diagram

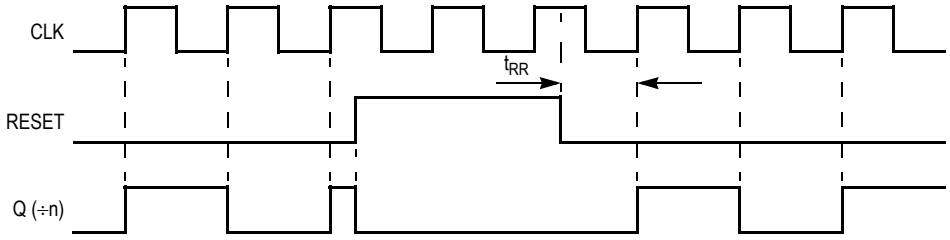


Figure 4. Timing Diagram

Table 3. Attributes

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Maximum Ratings[1]

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		3.9	V
V_{EE}	ECL Mode Power Supply	V_{CC} = 0 V		–3.9	V
V_I	PECL Mode Input Voltage ECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.9 –3.9	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	20 SOIC 20 SOIC	TBD TBD	°C/W °C/W

1. Maximum Ratings are those values beyond which device damage may occur.

Table 5. DC Characteristics (V_{CC} = 0 V, V_{EE} = –3.8 V to –3.135 V or V_{CC} = 3.135 V to 3.8 V, V_{EE} = 0 V)[1]

Symbol	Characteristic	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		35	60		35	60	mA
V_{OH}	Output HIGH Voltage[2]	V_{CC} –1150	V_{CC} –1020	V_{CC} –800	V_{CC} –1200	V_{CC} –970	V_{CC} –750	mV
V_{OL}	Output LOW Voltage[2]	V_{CC} –1950	V_{CC} –1620	V_{CC} –1250	V_{CC} –2000	V_{CC} –1680	V_{CC} –1300	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	V_{CC} –1165		V_{CC} –880	V_{CC} –1165		V_{CC} –880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	V_{CC} –1810		V_{CC} –1475	V_{CC} –1810		V_{CC} –1475	mV
V_{BB}	Output Reference Voltage	V_{CC} –1400		V_{CC} –1200	V_{CC} –1400		V_{CC} –1200	mV
V_{PP}	Differential Input Voltage[3]	0.12		1.4	0.12		1.4	V
V_{CMR}	Differential Cross Point Voltage[4]	V_{EE}+0.2		V_{CC}–0.7	V_{EE}+0.2		V_{CC}–0.7	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			μA

1. MC100ES6039 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
2. All loading with 50 Ω to V_{CC}–2.0 volts.
3. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
4. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics (V_{CC} = 0 V; V_{EE} = –3.8 V to –3.135 V or V_{CC} = 3.135 V to 3.8 V; V_{EE} = 0 V)[1]

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency		> 1			> 1			> 1		GHz
t_{PLH}, t_{PHL}	Propagation Delay CLK, Q (Diff) MR, Q	575 500		875 850	575 500		875 850	575 500		875 850	ps ps
t_{RR}	Reset Recovery	200	100		200	100		200	100		ps
t_s	Setup Time $\overline{EN}$, $\overline{CLK}$ DIVSEL, CLK	200 400	120 180		200 400	120 180		200 400	120 180		ps ps
t_h	Hold Time $\overline{CLK}$, $\overline{EN}$ CLK, DIVSEL	100 200	50 140		100 200	50 140		100 200	50 140		ps ps
t_{PW}	Minimum Pulse Width MR	550	450		550	450		550	450		ps
t_{SKEW}	Within Device Skew Q, $\overline{Q}$ Q, $\overline{Q}$ @ Same Frequency Device-to-Device Skew[2]			80 50 300			80 50 300			80 50 300	ps ps ps
t_{JITTER}	Cycle-to-Cycle Jitter (RMS 1σ)			1			1			1	ps
V_{PP}	Input Voltage Swing (Differential)	150		1400	150		1400	150		1400	mV
V_{CMR}	Differential Cross Point Voltage	V_{EE}+0.2		V_{CC}–1.1	V_{EE}+0.2		V_{CC}–1.1	V_{EE}+0.2		V_{CC}–1.1	V
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% – 80%)	50		300	50		300	50		300	ps

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC}–2.0 V.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

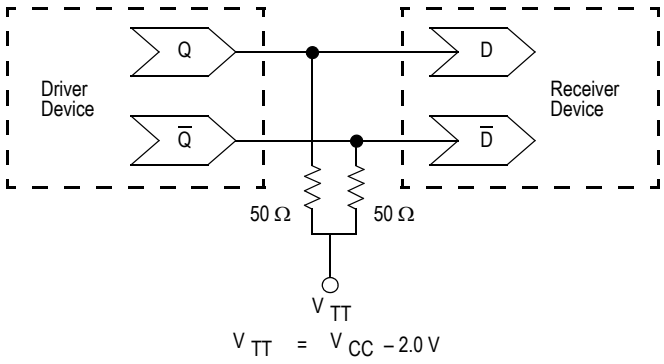


Figure 5. Typical Termination for Output Driver and Device Evaluation

Marking Notes:

Device Nomenclature	20-Lead SOIC W/B Marking
MC100ES6039DW	MC100ES6039

Trace Code Identification for 20 SOIC: AWLYYWW

"A" - The First character indicates the Assembly location.
"WL" - The Second & Third characters indicate the Source Wafer Lot Tracking Code.
"YY" - The Fourth & Fifth characters indicate the Year device was assembled.
"WW" - The Sixth & Seventh characters indicate the Work Week device was assembled.

The "Y" Year ALPHA CODES

Year	Month	Work Week Code
A = 2003	FIRST 6 MONTHS	WW01 – WW26
B = 2003	SECOND 6 MONTHS	WW27 – WW52
C = 2004	FIRST 6 MONTHS	WW01 – WW26
D = 2004	SECOND 6 MONTHS	WW27 – WW52
E = 2005	FIRST 6 MONTHS	WW01 – WW26
F = 2005	SECOND 6 MONTHS	WW27 – WW52
G = 2006	FIRST 6 MONTHS	WW01 – WW26
H = 2006	SECOND 6 MONTHS	WW27 – WW52
I = 2007	FIRST 6 MONTHS	WW01 – WW26
J = 2007	SECOND 6 MONTHS	WW27 – WW52
K = 2008	FIRST 6 MONTHS	WW01 – WW26
L = 2008	SECOND 6 MONTHS	WW27 – WW52
M = 2009	FIRST 6 MONTHS	WW01 – WW26
N = 2009	SECOND 6 MONTHS	WW27 – WW52
O = 2010	FIRST 6 MONTHS	WW01 – WW26
P = 2010	SECOND 6 MONTHS	WW27 – WW52
Q = 2011	FIRST 6 MONTHS	WW01 – WW26
R = 2011	SECOND 6 MONTHS	WW27 – WW52
S = 2012	FIRST 6 MONTHS	WW01 – WW26
T = 2012	SECOND 6 MONTHS	WW27 – WW52
U = 2013	FIRST 6 MONTHS	WW01 – WW26
V = 2013	SECOND 6 MONTHS	WW27 – WW52
W = 2014	FIRST 6 MONTHS	WW01 – WW26
X = 2014	SECOND 6 MONTHS	WW27 – WW52
Y = 2015	FIRST 6 MONTHS	WW01 – WW26
Z = 2015	SECOND 6 MONTHS	WW27 – WW52

The "W" Work Week ALPHA CODES

1st 6 Months (WW01 – WW26)	2nd 6 Months (WW27 – WW52)
A = WW01	A = WW27
B = WW02	B = WW28
C = WW03	C = WW29
D = WW04	D = WW30
E = WW05	E = WW31
F = WW06	F = WW32
G = WW07	G = WW33
H = WW08	H = WW34
I = WW09	I = WW35
J = WW10	J = WW36
K = WW11	K = WW37
L = WW12	L = WW38
M = WW13	M = WW39
N = WW14	N = WW40
O = WW15	O = WW41
P = WW16	P = WW42
Q = WW17	Q = WW43
R = WW18	R = WW44
S = WW19	S = WW45
T = WW20	T = WW46
U = WW21	U = WW47
V = WW22	V = WW48
W = WW23	W = WW49
X = WW24	X = WW50
Y = WW25	Y = WW51
Z = WW26	Z = WW52

2.5V / 3.3V ECL/PECL/LVDS Dual Differential 2:1 Multiplexer

MC100ES6056

The MC100ES6056 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple V_{BB} pins are provided.

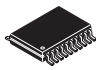
The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to V_{BB} as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor and limit current sourcing or sinking to 0.5 mA. When not used, V_{BB} should be left open.

The device features both individual and common select inputs to address both data path and random logic applications.

The 100ES Series contains temperature compensation.

Features

- 360 ps Typical Propagation Delays
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range: V_{CC} = 2.375 V to 3.8 V with V_{EE} = 0 V
- ECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –2.375 V to –3.8 V
- Open Input Default State
- Separate and Common Select
- Q Output Will Default LOW with Inputs Open or at V_{EE}
- V_{BB} Outputs
- LVDS Input Compatible

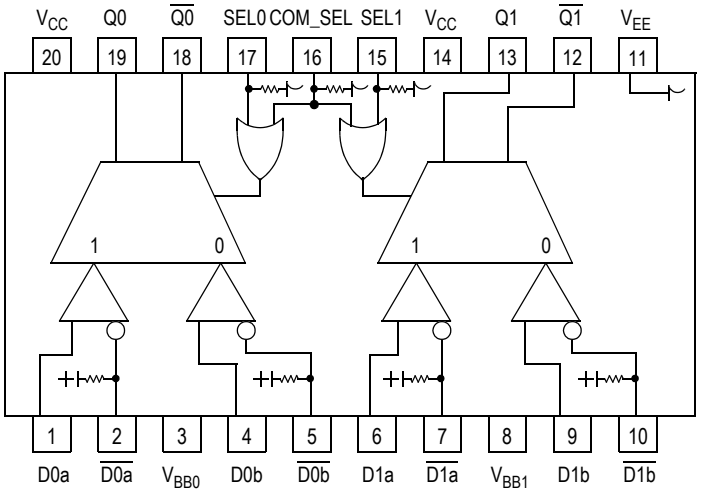


DT SUFFIX
20 LEAD TSSOP PACKAGE
CASE 948E-02

DW SUFFIX
20 LEAD SOIC PACKAGE
CASE 751D-06

ORDERING INFORMATION

Device	Package
MC100ES6056DT	TSSOP-20
MC100ES6056DTR2	TSSOP-20
MC100ES6056DW	SO-20
MC100ES6056DWR2	SO-20



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View) **and Logic Diagram**

* Input function will default LOW when left open.

Table 1. Pin Description

Pin	Function
D0a* – D1a*	ECL Input Data a
$\overline{D0a}$* – $\overline{D1a}$*	ECL Input Data a Invert
D0b* – D1b*	ECL Input Data b
$\overline{D0b}$* – $\overline{D1b}$*	ECL Input Data b Invert
SEL0* – SEL1*	ECL Indiv. Select Input
COM_SEL*	ECL Common Select Input
V_{BB0}, V_{BB1}	Output Reference Voltage
Q0 – Q1	ECL True Outputs
$\overline{Q0}$ – $\overline{Q1}$	ECL Inverted Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

Table 2. Function Table

SEL0	SEL1	COM_SEL	Q0, $\overline{Q0}$	Q1, $\overline{Q1}$
X	X	H	a	a
L	L	L	b	b
L	H	L	b	a
H	H	L	a	a
H	L	L	a	b

Table 3. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 4 kV > 400 V > 2 kV
Thermal Resistance (Junction-to-Ambient)	0 LFPM, 20 TSSOP 500 LFPM, 20 TSSOP	140°C/W 100°C/W
	0 LFPM, 20 SOIC 500 LFPM, 20 SOIC	TBD TBD

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristic	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	V_{CC} + 0.3 V_{EE} – 0.3	V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
I_{BB}	V_{BB} Sink/Source Current		±0.5	°C
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 0 V, V_{EE} = –2.5 V±5% or 3.8 V to –3.135 V; V_{CC} = 2.5 V±5% or 3.135 V to 3.8 V, V_{EE} = 0 V)

Symbol	Characteristics	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		30	60		30	60	mA
V_{OH}	Output HIGH Voltage[1]	V_{CC}–1085	V_{CC}–960	V_{CC}–880	V_{CC}–1025	V_{CC}–930	V_{CC}–860	mV
V_{OL}	Output LOW Voltage[1]	V_{CC}–1950	V_{CC}–1695	V_{CC}–1500	V_{CC}–1950	V_{CC}–1705	V_{CC}–1500	mV
V_{IH}	Input HIGH Voltage	V_{CC}–1165		V_{CC}–880	V_{CC}–1165		V_{CC}–880	mV
V_{IL}	Input LOW Voltage	V_{CC}–1810		V_{CC}–1475	V_{CC}–1810		V_{CC}–1475	mV
V_{BB}	Output Reference Voltage	V_{CC}–1380	V_{CC}–1290	V_{CC}–1220	V_{CC}–1380	V_{CC}–1290	V_{CC}–1200	mV
V_{PP}	Differential Input Voltage[2]	0.15		1.3	0.15		1.3	V
V_{CMR}	Differential Cross Point Voltage[3]	V_{CC} –2.3		V_{CC}–0.8	V_{CC} –2.3		V_{CC}–0.8	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			μA

1. Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics (V_{CC} = 0 V; V_{EE} = –2.5 V ±5% or –3.8 V to –3.135 V; V_{CC} = 2.5 V ±5% or 3.135 V to 3.8 V; V_{EE} = 0 V)[1]

Symbol	Characteristics	–40°C to 85°C			Unit
		Min	Typ	Max	
f_{max}	Maximum Frequency		> 3		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential D to Q, $\overline{Q}$ SEL to Q, $\overline{Q}$ COM_SEL to Q, $\overline{Q}$	 300 300 300	 400 430 490	 500 600 650	 ps ps ps
t_{SKEW}	Skew Output-to-Output[2] Part-to-Part		10	 50 200	 ps ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1σ)			1	ps
V_{PP}	Minimum Input Swing	200	800	1200	mV
V_{CMR}	Differential Cross Point Voltage	V_{CC}–2.1		V_{CC}–1.1	V
t_r / t_f	Output Rise/Fall Time (20%–80%)	70	120	230	ps

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50Ω to V_{CC}–2.0 V.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

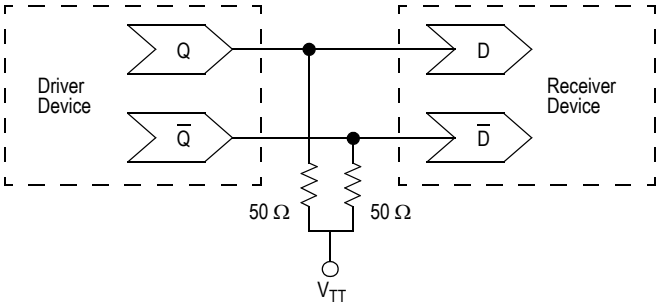


Figure 2. Typical Termination for Output Driver and Device Evaluation

Marking Notes:

Device Nomenclature	20-Lead TSSOP Marking	20-Lead SOIC W/B Marking
MC100ES6056DT	6056	
MC100ES6056DW		MC100ES6056

Trace Code Identification for 20 SOIC: AWLYYWW

"A" – The First character indicates the Assembly location.
"WL" – The Second & Third characters indicate the Source Wafer Lot Tracking Code.
"YY" – The Fourth & Fifth characters indicate the Year device was assembled.
"WW" – The Sixth & Seventh characters indicate the Work Week device was assembled.

Trace Code Identification for 20 TSSOP: ALYW

"A" – The First character indicates the Assembly location.
"L" – The Second character indicates the Source Wafer Lot Tracking Code.
"Y" – The Third character indicates the "ALPHA CODE" of the year device was assembled.
"W" – The Fourth character indicates the "ALPHA CODE" of the Work Week device was assembled.

The "Y" Year ALPHA CODES

Year	Month	Work Week Code
A = 2003	FIRST 6 MONTHS	WW01 – WW26
B = 2003	SECOND 6 MONTHS	WW27 – WW52
C = 2004	FIRST 6 MONTHS	WW01 – WW26
D = 2004	SECOND 6 MONTHS	WW27 – WW52
E = 2005	FIRST 6 MONTHS	WW01 – WW26
F = 2005	SECOND 6 MONTHS	WW27 – WW52
G = 2006	FIRST 6 MONTHS	WW01 – WW26
H = 2006	SECOND 6 MONTHS	WW27 – WW52
I = 2007	FIRST 6 MONTHS	WW01 – WW26
J = 2007	SECOND 6 MONTHS	WW27 – WW52
K = 2008	FIRST 6 MONTHS	WW01 – WW26
L = 2008	SECOND 6 MONTHS	WW27 – WW52
M = 2009	FIRST 6 MONTHS	WW01 – WW26
N = 2009	SECOND 6 MONTHS	WW27 – WW52
O = 2010	FIRST 6 MONTHS	WW01 – WW26
P = 2010	SECOND 6 MONTHS	WW27 – WW52
Q = 2011	FIRST 6 MONTHS	WW01 – WW26
R = 2011	SECOND 6 MONTHS	WW27 – WW52
S = 2012	FIRST 6 MONTHS	WW01 – WW26
T = 2012	SECOND 6 MONTHS	WW27 – WW52
U = 2013	FIRST 6 MONTHS	WW01 – WW26
V = 2013	SECOND 6 MONTHS	WW27 – WW52
W = 2014	FIRST 6 MONTHS	WW01 – WW26
X = 2014	SECOND 6 MONTHS	WW27 – WW52
Y = 2015	FIRST 6 MONTHS	WW01 – WW26
Z = 2015	SECOND 6 MONTHS	WW27 – WW52

The "W" Work Week ALPHA CODES

1st 6 Months (WW01 – WW26)	2nd 6 Months (WW27 – WW52)
A = WW01	A = WW27
B = WW02	B = WW28
C = WW03	C = WW29
D = WW04	D = WW30
E = WW05	E = WW31
F = WW06	F = WW32
G = WW07	G = WW33
H = WW08	H = WW34
I = WW09	I = WW35
J = WW10	J = WW36
K = WW11	K = WW37
L = WW12	L = WW38
M = WW13	M = WW39
N = WW14	N = WW40
O = WW15	O = WW41
P = WW16	P = WW42
Q = WW17	Q = WW43
R = WW18	R = WW44
S = WW19	S = WW45
T = WW20	T = WW46
U = WW21	U = WW47
V = WW22	V = WW48
W = WW23	W = WW49
X = WW24	X = WW50
Y = WW25	Y = WW51
Z = WW26	Z = WW52

20 TSSOP Tracecode Marking Example:

5ABR
5 = Assembly Location
A = First Lot Assembled of this device in the designated Work Week
B = 2003 Second 6 Months, WW27 – WW52
R = WW44 of 2003

Order number: MC100ES6111
Rev 2, 08/2004

Low Voltage 2.5/3.3 V Differential ECL/PECL/HSTL Fanout Buffer

MC100ES6111

LOW-VOLTAGE 1:10 DIFFERENTIAL ECL/PECL/HSTL CLOCK FANOUT DRIVER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MC100ES6111 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6111 supports various applications that require distribution of precisely aligned differential clock signals. Using SiGe:C technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:10 differential clock distribution
- 35 ps maximum device skew
- Fully differential architecture from input to all outputs
- SiGe:C technology supports near-zero output skew
- Supports DC to 2.7 GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL/HSTL compatible differential clock inputs
- Single 3.3 V, –3.3 V, 2.5 V or –2.5 V supply
- Standard 32-lead LQFP package
- 32-lead Pb-free package available
- Industrial temperature range
- Pin and function compatible to the MC100EP111

Functional Description

The MC100ES6111 is designed for low skew clock distribution systems and supports clock frequencies up to 2.7 GHz. The device accepts two clock sources. The CLKA input can be driven by ECL or PECL compatible signals, the CLKB input accepts HSTL compatible signals. The selected input signal is distributed to 10 identical, differential ECL/PECL outputs. If V_{BB} is connected to the CLKA input and bypassed to GND by a 10 nF capacitor, the MC100ES6111 can be driven by single-ended ECL/PECL signals utilizing the V_{BB} bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6111 can be operated from a single 3.3 V or 2.5 V supply. As most other ECL compatible devices, the MC100ES6111 supports positive (PECL) and negative (ECL) supplies. The MC100ES6111 is pin and function compatible to the MC100EP111.

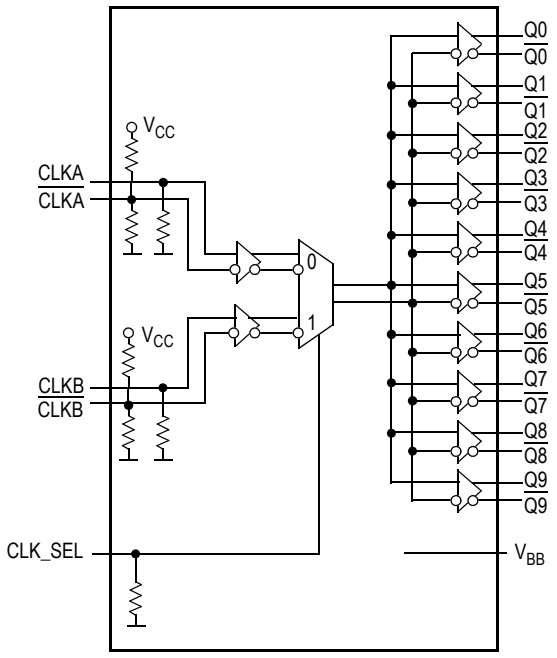


Figure 1. MC100ES6111 Logic Diagram

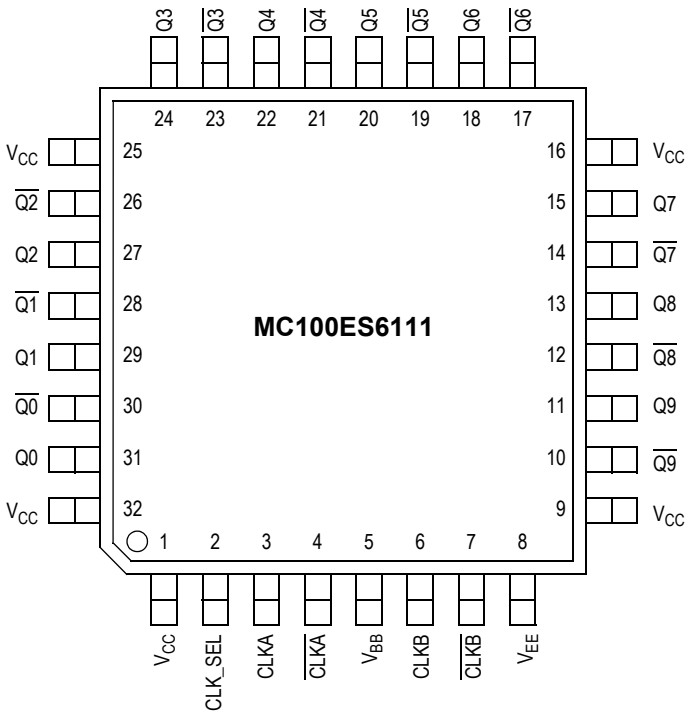


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLKA, $\overline{\text{CLKA}}$	Input	ECL/PECL	Differential reference clock signal input
CLKB, $\overline{\text{CLKB}}$	Input	HSTL	Alternative differential reference clock signal input
CLK_SEL	Input	ECL/PECL	Active clock input select
Q[0–9], $\overline{\text{Q[0–9]}}$	Output	ECL/PECL	Differential clock outputs
V_{EE}[1]	Supply		Negative power supply
V_{CC}	Supply		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
V_{BB}	Output	DC	Reference voltage output for single ended ECL or PECL operation

1. In ECL mode (negative power supply mode), V_{EE} is either –3.3 V or –2.5 V and V_{CC} is connected to GND (0V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0V) and V_{CC} is either +3.3 V or +2.5 V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}).

Table 2. Function Table

Control	Default	0	1
CLK_SEL	0	CLKA, $\overline{\text{CLKA}}$ input pair is active. CLKA can be driven by ECL or PECL compatible signals.	CLKB, $\overline{\text{CLKB}}$ input pair is active. CLKB can be driven by HSTL compatible signals.

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	
T_{Func}	Functional Temperature Range	T_A = –40	T_J = +110	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2[1]		V	
MM	ESD Protection (Machine Model)	200			V	
HBM	ESD Protection (Human Body Model)	4000			V	
CDM	ESD Protection (Charged Device Model)	2000			V	
LU	Latch-up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient					
	JESD 51–3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51–6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T_J	Operating Junction Temperature[2] (Continuous Operation) MTBF = 9.1 years			110	°C	

1. Output termination voltage V_{TT} = 0V for V_{CC} = 2.5V operation is supported but the power consumption of the device will increase
2. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this data sheet for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6111 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6111 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. PECL/HSTL DC Characteristics (V_{CC} = 2.5 V ± 5% or V_{CC} = 3.3 V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Control Input CLK_SEL						
V_{IL}	Input Voltage Low	V_{CC} – 1.810		V_{CC} – 1.475	V	
V_{IH}	Input Voltage High	V_{CC} – 1.165		V_{CC} – 0.880	V	
I_{IN}	Input Current[1]			100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock Input Pair CLKA, $\overline{\text{CLKA}}$ (PECL differential signals)						
V_{PP}	Differential Input Voltage[2]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[3]	1.0		V_{CC} – 0.3	V	Differential operation
I_{IN}	Input Current[1]			100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock Input Pair CLKB, $\overline{\text{CLKB}}$ (HSTL differential signals)						
V_{DIF}	Differential Input Voltage[4] V_{CC} = 3.3V V_{CC} = 2.5V	 0.4 0.4			 V V	
V_X	Differential Cross Point Voltage[5]	0.68		0.9	V	
I_{IN}	Input Current			200	μA	$V_{IN} = V_X \pm 0.2V$
PECL Clock Outputs (Q0-9, $\overline{\text{Q0-9}}$)						
V_{OH}	Output High Voltage	V_{CC} – 1.2	V_{CC} – 1.005	V_{CC} – 0.7	V	I_{OH} = –30 mA[6]
V_{OL}	Output Low Voltage V_{CC} = 3.3V±5% V_{CC} = 2.5V±5%	V_{CC} – 1.9 V_{CC} – 1.9	V_{CC} – 1.705 V_{CC} – 1.705	V_{CC} – 1.5 V_{CC} – 1.3	V	I_{OL} = –5 mA[6]
Supply Current and V_{BB}						
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current[7]			100	mA	V_{EE} pin
V_{BB}	Output Reference Voltage	V_{CC} – 1.4		V_{CC} – 1.2	V	I_{BB} = 200 μA

1. Input have internal pullup/pulldown resistors which affect the input current
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
5. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
6. Equivalent to a termination of 50Ω to V_{TT}.
7. I_{CC} calculation: I_{CC} = (number of differential output pairs used) x (I_{OH} + I_{OL}) + I_{EE}
   I_{CC} = (number of differential output pairs used) x (V_{OH} – V_{TT})/R_{load} + (V_{OL} – V_{TT})/R_{load} + I_{EE}.

Table 6. ECL DC Characteristics (V_{EE} = –2.5 V ± 5% or V_{EE} = –3.3 V ± 5%, V_{CC} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Control Input CLK_SEL						
V_{IL}	Input Voltage Low	–1.810		–1.475	V	
V_{IH}	Input Voltage High	–1.165		–0.880	V	
I_{IN}	Input Current[1]			100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock Input Pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (ECL differential signals)						
V_{PP}	Differential Input Voltage[2]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[3]	V_{EE} + 1.0		–0.3	V	Differential operation
I_{IN}	Input Current[1]			100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL Clock Outputs (Q0-9, $\overline{\text{Q0-9}}$)						
V_{OH}	Output High Voltage	–1.2	–1.005	–0.7	V	I_{OH} = –30 mA[4]
V_{OL}	Output Low Voltage V_{EE} = –3.3V ± 5% V_{EE} = –2.5V ± 5%	–1.9 –1.9	–1.705 –1.705	–1.5 –1.3	V	I_{OL} = –5 mA[6]
Supply Current and V_{BB}						
I_{EE}	Maximum Quiescent Supply Current without Output Termination Current[5]			100	mA	V_{EE} pin
V_{BB}	Output Reference Voltage	V_{CC} – 1.4		V_{CC} – 1.2	V	I_{BB} = 200 μA

1. Input have internal pullup/pulldown resistors which affect the input current
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. Equivalent to a termination of 50Ω to V_{TT}.
5. I_{CC} calculation: I_{CC} = (number of differential output pairs used) x (I_{OH} + I_{OL}) + I_{EE}
   I_{CC} = (number of differential output pairs used) x (V_{OH} – V_{TT})/R_{load} + (V_{OL} – V_{TT})/R_{load} + I_{EE}.

Table 7. AC Characteristics(ECL: V_{EE} = –3.3 V ± 5% or V_{EE} = –2.5 V ± 5%, V_{CC} = GND) or (HSTL/PECL: V_{CC} = 3.3 V ± 5% or V_{CC} = 2.5 V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock Input Pair CLKA, $\overline{\text{CLKA}}$ (PECL or ECL differential signals)						
V_{PP}	Differential Input Voltage[2] (peak-to-peak)	0.15		1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[3] PECL	V_{EE} + 1.0		V_{CC} – 0.3	V	
f_{CLK}	Input Frequency[4]			2.7	GHz	Differential
t_{PD}	Propagation Delay CLKA or CLKB to Q0–9	280	400	530	ps	Differential
Clock Input Pair CLKB, $\overline{\text{CLKB}}$ (HSTL differential signals)						
V_{DIF}	Differential Input Voltage (peak-to-peak)[5]	0.4		1.0	V	
V_X	Differential Input Crosspoint Voltage[6]	V_{EE} + 0.68		V_{EE} + 0.9	V	
f_{CLK}	Input Frequency			2.7	GHz	Differential
t_{PD}	Propagation Delay CLKB to Q0-9	280	400	530	ps	Differential
ECL Clock Outputs (Q0-9, $\overline{\text{Q0-9}}$)						
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak) f_O < 300 MHz f_O < 1.5 GHz f_O < 2.7 GHz	 0.45 0.3 TBD	 0.72 0.55 0.37	 0.95 0.95 0.95	 V V V	
$t_{sk(O)}$	Output-to-Output Skew			35	ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part)			250	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			1		
$t_{sk(P)}$	Output Pulse Skew[7]			75	ps	
t_r, t_f	Output Rise/Fall Time	0.05		0.3	ns	20% to 80%

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
3. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew
4. The MC100ES6111 is fully operational up to 3.0 GHz and is characterized up to 2.7 GHz.
5. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
6. V_X (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF} (AC) impacts the device propagation delay, device and part-to-part skew.
7. Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.

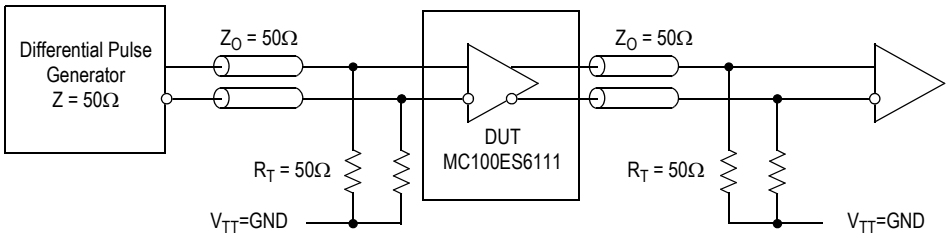


Figure 1. MC100ES6111 AC Test Reference

APPLICATIONS INFORMATION

Understanding the Junction Temperature Range of the MC100ES6111

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6111, the MC100ES6111 is specified, characterized and tested for the junction temperature range of T_J = 0°C to +110°C. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this data sheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 54.4 °C/W (2s2p board, 200 ft/min airflow, see Table 4) and a typical power consumption of 610 mW (all outputs terminated 50 ohms to V_{TT}, V_{CC} = 3.3V, frequency independent), the junction temperature of the MC100ES6111 is approximately T_A + 33 °C, and the minimum ambient temperature in this example case calculates to –33 °C (the maximum ambient temperature is 77 °C, see Table 8). Exceeding the minimum junction temperature specification of the MC100ES6111 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6111 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the application note AN1545 for a power consumption calculation guideline.

Table 8. Ambient Temperature Range (P_{tot} = 610 mW)

R_{thja} (2s2p board)		T_A, Min[1]	T_A, Max
Natural convection	59.0°C/W	–36°C	74°C
100 ft/min	54.4°C/W	–33°C	77°C
200 ft/min	52.5°C/W	–32°C	78°C
400 ft/min	50.4°C/W	–30°C	79°C
800 ft/min	47.8°C/W	–29°C	81°C

1. The MC100ES6111 device function is guaranteed from T_A = –40°C to T_J = 110°C

Maintaining Lowest Device Skew

The MC100ES6111 guarantees low output-to-output bank skew of 35 ps and a part-to-part skew of max. 250 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6111 is a mixed analog/digital product. The differential architecture of the MC100ES6111 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

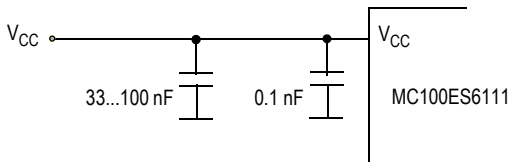


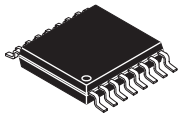
Figure 2. V_{CC} Power Supply Bypass

Order number: MC100ES6130
Rev 1, 05/2004

2.5/3.3 V 1:4 PECL Clock Driver with 2:1 Input MUX

MC100ES6130

The MC100ES6130 is a 2.5 GHz differential PECL 1:4 fanout buffer. The ES6130 offers a wide operating range of 2.5 V and 3.3 V and also features a 2:1 input MUX which is ideal for redundant clock switchover applications. This device also includes a synchronous enable pin that forces the outputs into a fixed logic state. Enable or disable state is initiated only after the outputs are in a LOW state to eliminate the possibility of a runt clock pulse.



DT SUFFIX
16-LEAD TSSOP PACKAGE
CASE 948F-01

Features

- 2 GHz maximum output frequency
- 25 ps maximum output-to-output skew
- 150 ps part-to-part skew
- 350 ps typical propagation delay
- 2:1 differential MUX input
- 2.5 / 3.3 V operating range
- LVPECL and HSTL input compatible
- 16-lead TSSOP package
- Temperature range –40°C to +85°C

ORDERING INFORMATION

Device	Package
MC100ES6130DT	TSSOP-16
MC100ES6130DTR2	TSSOP-16

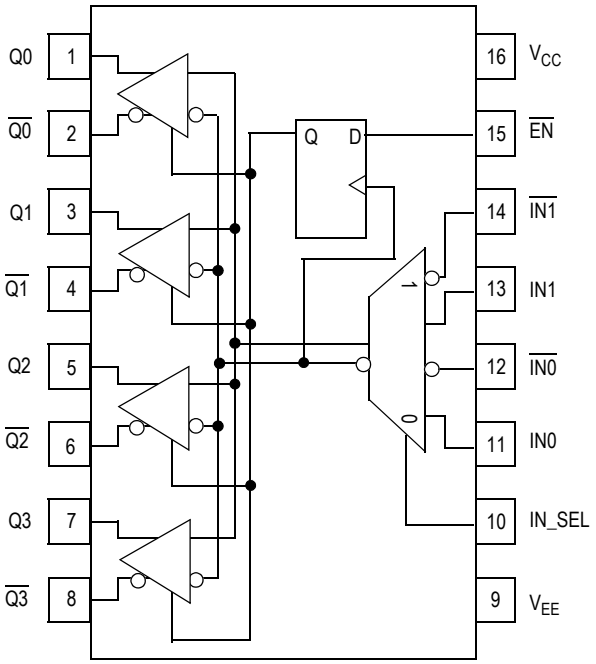


Figure 1. 16-Lead Pinout (Top View) and Logic Diagram

Table 1. Pin Description

Number	Name	Description
1, 2, 3, 4, 5, 6, 7, 8	Q0 to Q3 $\overline{Q0}$ to $\overline{Q3}$	LVPECL differential outputs: Terminate with 50Ω to V_{CC}–2V. For single-ended applications, terminate the unused output with 50Ω to V_{CC}–2V.
9	V_{EE}	Negative power supply: For LVPECL applications, connect to GND.
10	IN_SEL	LVPECL compatible 2:1 mux input signal select: When IN_SEL is LOW, the IN0 input pair is selected. When IN_SEL is HIGH, the IN1 input pair is selected. Includes a 75kΩ pulldown. Default state is LOW and IN0 is selected.
11, 12, 13, 14	IN0, $\overline{IN0}$ IN1, $\overline{IN1}$	LVPECL, HSTL clock or data inputs. Internal 75kΩ pulldown resistors on IN0 and IN1. Internal 75kΩ pullup and 75kΩ pulldown resistors on $\overline{IN0}$, $\overline{IN1}$. $\overline{IN0}$, $\overline{IN1}$ default condition is V_{CC}/2 when left floating. IN0, IN1 default condition is LOW when left floating.
15	$\overline{EN}$	LVPECL compatible synchronous enable: When $\overline{EN}$ goes HIGH, Q_{OUT} will go LOW and $\overline{Q}_{OUT}$ will go HIGH on the next LOW input clock transition. Includes a 75kΩ pulldown. Default state is LOW when left floating. The internal latch is clocked on the falling edge of the input (IN0, IN1).
16	V_{CC}	Positive power supply: Bypass with 0.1μF//0.01μF low ESR capacitors.

Table 2. Truth Table[1]

IN0	IN1	IN_SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	L
Z	X	L	H	L
X	Z	H	H	L

1. Z = HIGH to LOW Transition
   X = Don't Care

Table 3. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2000 V > 200 V > 1500 V
θ_{JA} Thermal Resistance (Junction-to-Ambient)	0 LFPM, 16 TSSOP 500 LFPM, 16 TSSOP	138°C/W 108°C/W

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Absolute Maximum Ratings[1]

Symbol	Rating	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{out}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 0 V, V_{EE} = –2.5 V ±5% or V_{CC} = 2.5 V ±5%, V_{EE} = 0 V)

Symbol	Characteristic	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		45	70		45	70	mA
V_{OH}	Output HIGH Voltage[1]	V_{CC} – 1250	V_{CC} – 990	V_{CC} – 800	V_{CC} – 1200	V_{CC} – 960	V_{CC} – 750	mV
V_{OL}	Output LOW Voltage[1]	V_{CC} – 2000	V_{CC} – 1550	V_{CC} – 1150	V_{CC} – 1925	V_{CC} – 1630	V_{CC} – 1200	mV
V_{outPP}	Output Peak-to-Peak Voltage	200			200			mV
V_{IH}	Input HIGH Voltage	V_{CC} – 1165		V_{CC} – 880	V_{CC} – 1165		V_{CC} – 880	mV
V_{IL}	Input LOW Voltage	V_{CC} – 1810		V_{CC} – 1475	V_{CC} – 1810		V_{CC} – 1475	mV
V_{PP}	Differential Input Voltage[2]	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage[3]	V_{EE} + 0.2		V_{CC} – 1.0	V_{EE} + 0.2		V_{CC} – 1.0	V
I_{IN}	Input Current			±150			±150	μA

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the cross point of the differential input signal. Functional operation is obtained when the cross point is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. DC Characteristics (V_{CC} = 0 V, V_{EE} = –3.8 to 3.135 V or V_{CC} = 3.135 to 3.8 V, V_{EE} = 0 V)

Symbol	Characteristic	–40°C			0°C to 85°C			
		Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current		48	70		48	70	mA
V_{OH}	Output HIGH Voltage[1]	V_{CC} – 1150	V_{CC} – 1020	V_{CC} – 800	V_{CC} – 1200	V_{CC} – 970	V_{CC} – 750	mV
V_{OL}	Output LOW Voltage[1]	V_{CC}– 1950	V_{CC} – 1620	V_{CC} – 1250	V_{CC} – 2000	V_{CC} – 1680	V_{CC} – 1300	mV
V_{outPP}	Output Peak-to-Peak Voltage	200			200			mV
V_{IH}	Input HIGH Voltage	V_{CC} – 1165		V_{CC} – 880	V_{CC} – 1165		V_{CC} – 880	mV
V_{IL}	Input LOW Voltage	V_{CC} – 1810		V_{CC} – 1475	V_{CC} – 1810		V_{CC} – 1475	mV
V_{PP}	Differential Input Voltage[2]	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage[3]	V_{EE} + 0.2		V_{CC} - 1.1	V_{EE} + 0.2		V_{CC} – 1.1	V
I_{IN}	Input Current			±150			±150	μA

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 7. AC Characteristics (V_{CC} = 0 V, V_{EE} = –3.8 V to –2.375 V; V_{CC} = 2.375 to 3.8 V, V_{EE} = 0 V)[1]

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency	2			2			2			GHz
t_{PLH} / t_{PHL}	Propagation Delay to Output Differential CLK to Q, $\overline{Q}$	300	340	450	300	350	450	300	350	475	ps
t_{SKEW}	Skew[2] output-to-output part-to-part		15	25 125		15	25 150		15	25 150	ps ps
t_{JITTER}	Cycle-to-Cycle Jitter RMS (1σ)			1			1			1	ps
V_{PP}	Minimum Input Swing	200		1200	200		1200	200		1200	mV
V_{CMR}	Differential Cross Point Voltage	V_{EE} + 0.2		V_{CC} – 1.2	V_{EE} + 0.2		V_{CC} – 1.2	V_{EE} + 0.2		V_{CC} – 1.2	V
t_r / t_f	Output Rise/Fall Times (20% – 80% @ 50 MHz)	70		225	70		250	70		275	ps

1. Measured using a 750 mV source, 50% Duty Cycle clock source. All loading with 50 ohms to V_{CC} –2.0V.
2. Skew is measured between outputs under identical transitions.

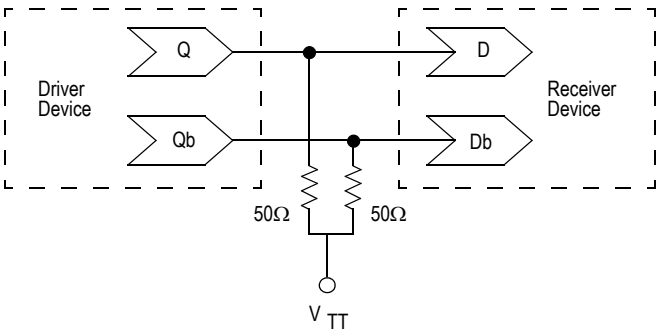


Figure 2. Typical Termination for Output Driver and Device Evaluation

Order number: MC100ES6139
Rev 1, 06/2004

3.3 V ECL/PECL/HSTL/LVDS ÷2/4, ÷4/5/6 Clock Generation Chip

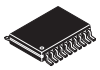
MC100ES6139

The MC100ES6139 is a low skew ÷2/4, ÷4/5/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, LVPECL input signals. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device. If a single-ended input is to be used, the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to ground via a 0.01 μF capacitor.

The common enable ($\overline{EN}$) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple ES6139s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one ES6139, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2/4 and the ÷4/5/6 outputs of a single device. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation.

The 100ES Series contains temperature compensation.



DT SUFFIX
20-LEAD TSSOP PACKAGE
CASE 948E-02

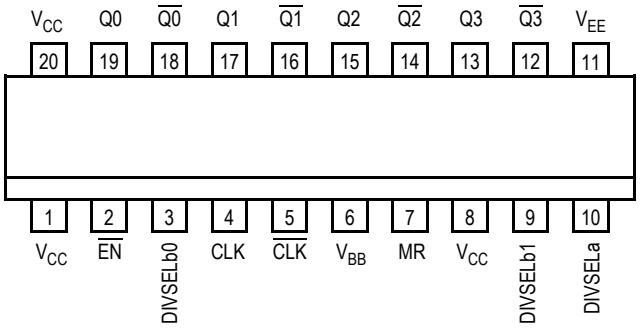
DW SUFFIX
20-LEAD SOIC PACKAGE
CASE 751D-06

ORDERING INFORMATION

Device	Package
MC100ES6139DT	TSSOP-20
MC100ES6139DTR2	TSSOP-20
MC100ES6139DW	SO-20
MC100ES6139DWR2	SO-20

Features

- Maximum Frequency >1.0 GHz Typical
- 50 ps Output-to-Output Skew
- PECL Mode Operating Range: V_{CC} = 3.135 V to 3.8 V with V_{EE} = 0 V
- ECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = –3.135 V to –3.8 V
- Open Input Default State
- Synchronous Enable/Disable
- Master Reset for Synchronization of Multiple Chips
- V_{BB} Output
- LVDS and HSTL Input Compatible



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View)

Table 1. Pin Description

Pin	Function
CLK[1], $\overline{\text{CLK}}$[1]	ECL Diff Clock Inputs
$\overline{\text{EN}}$[1]	ECL Sync Enable
MR[1]	ECL Master Reset
V_{BB}	ECL Reference Output
Q0, Q1, $\overline{\text{Q0}}$, $\overline{\text{Q1}}$	ECL Diff ÷2/4 Outputs
Q2, Q3, $\overline{\text{Q2}}$, $\overline{\text{Q3}}$	ECL Diff ÷4/5/6 Outputs
DIVSELa[1]	ECL Freq. Select Input ÷2/4
DIVSELb0[1]	ECL Freq. Select Input ÷4/5/6
DIVSELb1[1]	ECL Freq. Select Input ÷4/5/6
V_{CC}	ECL Positive Supply
V_{EE}	ECL Negative Supply

1. Pins will default low when left open.

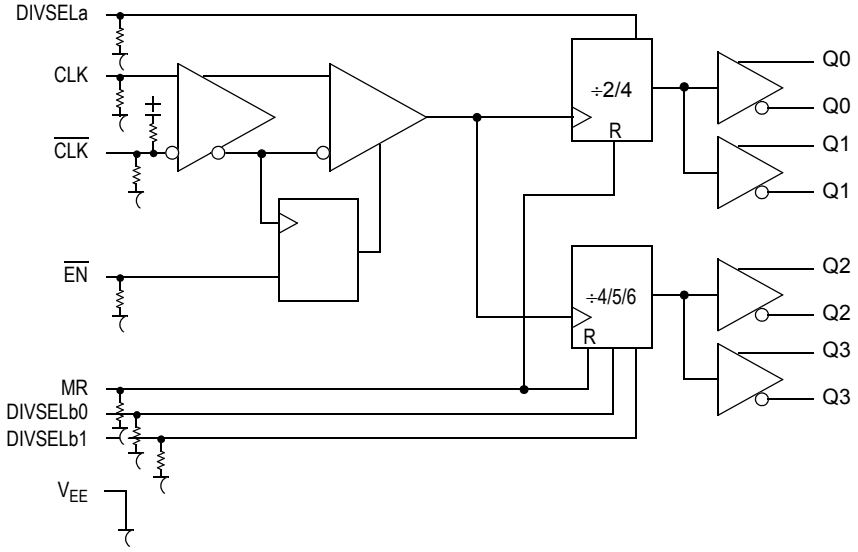


Figure 2. Logic Diagram

Table 2. Function Tables

CLK	$\overline{\text{EN}}$	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q0:3
X	X	H	Reset Q0:3

X = Don't Care
Z = Low-to-High Transition
ZZ = High-to-Low Transition

DIVSELa		Q0:1 Outputs
L		Divide by 2
H		Divide by 4
DIVSELb0	DIVSELb1	Q2:3 Outputs
L	L	Divide by 4
H	L	Divide by 6
L	H	Divide by 5
H	H	Divide by 5

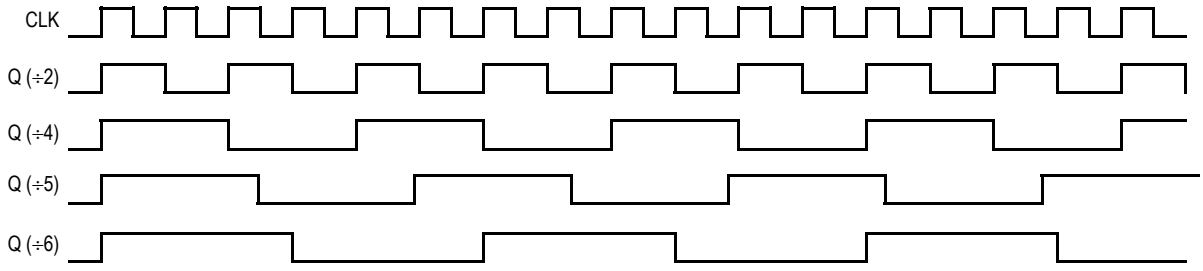


Figure 3. Timing Diagram

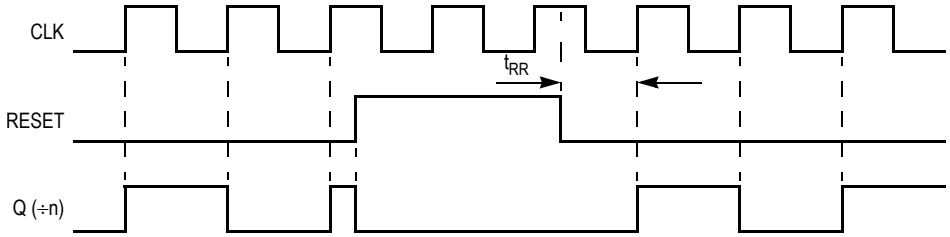


Figure 4. Timing Diagram

Table 3. Attributes

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model	> 4 kV > 200 V > 2 kV

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Maximum Ratings[1]

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		3.9	V
V_{EE}	ECL Mode Power Supply	V_{CC} = 0 V		–3.9	V
V_I	PECL Mode Input Voltage ECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.9 –3.9	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			–40 to +85	°C
T_{stg}	Storage Temperature Range			–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	20 TSSOP 20 TSSOP	74 64	°C/W °C/W
		0 LFPM 500 LFPM	20 SOIC 20 SOIC	TBD TBD	°C/W °C/W

1. Maximum Ratings are those values beyond which device damage may occur.

Table 5. DC Characteristics (V_{CC} = 0 V, V_{EE} = –3.8 V to –3.135 V or V_{CC} = 3.135 V to 3.8 V, V_{EE} = 0 V)[1]

Symbol	Characteristic	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current		35	60		35	60	mA
V_{OH}	Output HIGH Voltage[2]	V_{CC} –1150	V_{CC} –1020	V_{CC} –800	V_{CC} –1200	V_{CC} –970	V_{CC} –750	mV
V_{OL}	Output LOW Voltage[2]	V_{CC} –1950	V_{CC} –1620	V_{CC} –1250	V_{CC} –2000	V_{CC} –1680	V_{CC} –1300	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	V_{CC} –1165		V_{CC} –880	V_{CC} –1165		V_{CC} –880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	V_{CC} –1810		V_{CC} –1475	V_{CC} –1810		V_{CC} –1475	mV
V_{BB}	Output Reference Voltage	V_{CC} –1400		V_{CC} –1200	V_{CC} –1400		V_{CC} –1200	mV
V_{PP}	Differential Input Voltage[3]	0.12		1.3	0.12		1.3	V
V_{CMR}	Differential Cross Point Voltage[4]	V_{EE} +0.2		V_{CC} –1.1	V_{EE} +0.2		V_{CC} –1.1	V
I_{IH}	Input HIGH Current			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			μA

1. MC100ES6139 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
2. All loading with 50 Ω to V_{CC}–2.0 volts.
3. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
4. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics (V_{CC} = 0 V, V_{EE} = –3.8 V to –3.135 V or V_{CC} = 3.135 V to 3.8 V, V_{EE} = 0 V)[1]

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Frequency		> 1			> 1			> 1		GHz
t_{PLH}, t_{PHL}	Propagation Delay CLK, Q (Diff) MR, Q	550 400		850 850	550 400		850 850	550 400		850 850	ps
t_{RR}	Reset Recovery	200	100		200	100		200	100		ps
t_s	Setup Time $\overline{EN}$, $\overline{CLK}$ DIVSEL, CLK	200 400	120 180		200 400	120 180		200 400	120 180		ps
t_h	Hold Time $\overline{CLK}$, $\overline{EN}$ CLK, DIVSEL	100 200	50 140		100 200	50 140		100 200	50 140		ps
t_{PW}	Minimum Pulse Width MR	550	450		550	450		550	450		ps
t_{SKEW}	Within Device Skew Q, $\overline{Q}$ Q, $\overline{Q}$ @ Same Frequency Device-to-Device Skew[2]			100 50 300			100 50 300			100 50 300	ps
t_{JITTER}	Cycle-to-Cycle Jitter (RSM 1σ)			1			1			1	ps
V_{PP}	Input Voltage Swing (Differential)	200		1200	200		1200	200		1200	mV
V_{CMR}	Differential Cross Point Voltage	V_{EE}+0.2		V_{CC}–1.2	V_{EE}+0.2		V_{CC}–1.2	V_{EE}+0.2		V_{CC}–1.2	V
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% – 80%)	50		300	50		300	50		300	ps

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} –2.0 V.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

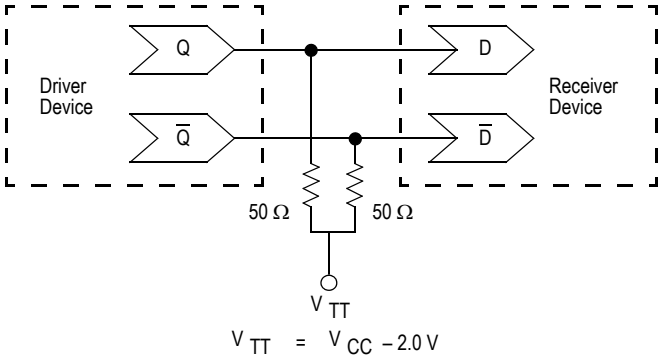


Figure 5. Typical Termination for Output Driver and Device Evaluation

Marking Notes:

Device Nomenclature	20-Lead TSSOP Marking	20-Lead SOIC W/B Marking
MC100ES6139DT	6139	
MC100ES6139DW		MC100ES6139

Trace Code Identification for 20 SOIC: AWLYYWW

"A" - The First character indicates the Assembly location.
"WL" - The Second & Third characters indicate the Source Wafer Lot Tracking Code.
"YY" - The Fourth & Fifth characters indicate the Year device was assembled.
"WW" - The Sixth & Seventh characters indicate the Work Week device was assembled.

Trace Code Identification for 20 TSSOP: ALYW

"A" - The First character indicates the Assembly location.
"L" - The Second character indicates the Source Wafer Lot Tracking Code.
"Y" - The Third character indicates the "ALPHA CODE" of the year device was assembled.
"W" - The Fourth character indicates the "ALPHA CODE" of the Work Week device was assembled.

The "Y" Year ALPHA CODES

Year	Month	Work Week Code
A = 2003	FIRST 6 MONTHS	WW01 – WW26
B = 2003	SECOND 6 MONTHS	WW27 – WW52
C = 2004	FIRST 6 MONTHS	WW01 – WW26
D = 2004	SECOND 6 MONTHS	WW27 – WW52
E = 2005	FIRST 6 MONTHS	WW01 – WW26
F = 2005	SECOND 6 MONTHS	WW27 – WW52
G = 2006	FIRST 6 MONTHS	WW01 – WW26
H = 2006	SECOND 6 MONTHS	WW27 – WW52
I = 2007	FIRST 6 MONTHS	WW01 – WW26
J = 2007	SECOND 6 MONTHS	WW27 – WW52
K = 2008	FIRST 6 MONTHS	WW01 – WW26
L = 2008	SECOND 6 MONTHS	WW27 – WW52
M = 2009	FIRST 6 MONTHS	WW01 – WW26
N = 2009	SECOND 6 MONTHS	WW27 – WW52
O = 2010	FIRST 6 MONTHS	WW01 – WW26
P = 2010	SECOND 6 MONTHS	WW27 – WW52
Q = 2011	FIRST 6 MONTHS	WW01 – WW26
R = 2011	SECOND 6 MONTHS	WW27 – WW52
S = 2012	FIRST 6 MONTHS	WW01 – WW26
T = 2012	SECOND 6 MONTHS	WW27 – WW52
U = 2013	FIRST 6 MONTHS	WW01 – WW26
V = 2013	SECOND 6 MONTHS	WW27 – WW52
W = 2014	FIRST 6 MONTHS	WW01 – WW26
X = 2014	SECOND 6 MONTHS	WW27 – WW52
Y = 2015	FIRST 6 MONTHS	WW01 – WW26
Z = 2015	SECOND 6 MONTHS	WW27 – WW52

The "W" Work Week ALPHA CODES

1st 6 Months (WW01 – WW26)	2nd 6 Months (WW27 – WW52)
A = WW01	A = WW27
B = WW02	B = WW28
C = WW03	C = WW29
D = WW04	D = WW30
E = WW05	E = WW31
F = WW06	F = WW32
G = WW07	G = WW33
H = WW08	H = WW34
I = WW09	I = WW35
J = WW10	J = WW36
K = WW11	K = WW37
L = WW12	L = WW38
M = WW13	M = WW39
N = WW14	N = WW40
O = WW15	O = WW41
P = WW16	P = WW42
Q = WW17	Q = WW43
R = WW18	R = WW44
S = WW19	S = WW45
T = WW20	T = WW46
U = WW21	U = WW47
V = WW22	V = WW48
W = WW23	W = WW49
X = WW24	X = WW50
Y = WW25	Y = WW51
Z = WW26	Z = WW52

20 TSSOP Tracecode Marking Example:

5ABR

5 = Assembly Location

A = First Lot Assembled of this device in the designated Work Week

B = 2003 Second 6 Months, WW27 - WW52

R= WW44 of 2003

Order number: MC100ES6210
Rev 2, 08/2004

Low Voltage 2.5/3.3 V Differential ECL/PECL/HSTL Fanout Buffer

MC100ES6210

LOW VOLTAGE DUAL 1:5 DIFFERENTIAL PECL/ECL/HSTL CLOCK FANOUT BUFFER

FA SUFFIX
32–LEAD LQFP PACKAGE
CASE 873A-03

The MC100ES6210 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6210 supports various applications that require to distribute precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low clock skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

Features

- Dual 1:5 differential clock distribution
- 30 ps maximum device skew
- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Supports DC to 3GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL compatible differential clock inputs
- Single 3.3 V, –3.3 V, 2.5 V or –2.5 V supply
- Standard 32 lead LQFP package
- Industrial temperature range
- Pin and function compatible to the MC100EP210
- 32-lead Pb-free Package Available

Functional Description

The MC100ES6210 is designed for low skew clock distribution systems and supports clock frequencies up to 3 GHz. The device consists of two independent 1:5 clock fanout buffers. The input signal of each fanout buffer is distributed to five identical, differential ECL/PECL outputs. Both CLKA and CLKB inputs can be driven by ECL/PECL compatible signals.

If V_{BB} is connected to the CLKA or CLKB input and bypassed to GND by a 10 nF capacitor, the MC100ES6210 can be driven by single-ended ECL/PECL signals utilizing the V_{BB} bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6210 can be operated from a single 3.3 V or 2.5 V supply. As most other ECL compatible devices, the MC100ES6210 supports positive (PECL) and negative (ECL) supplies. The is function and pin compatible to the MC100EP210.

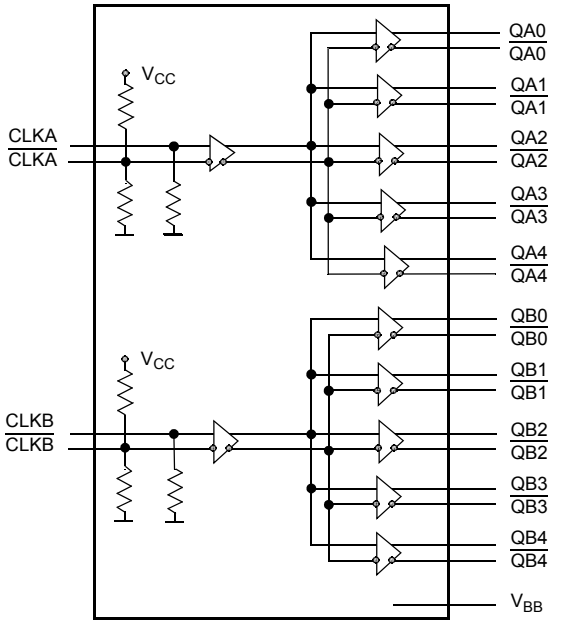


Figure 1. MC100ES6210 Logic Diagram

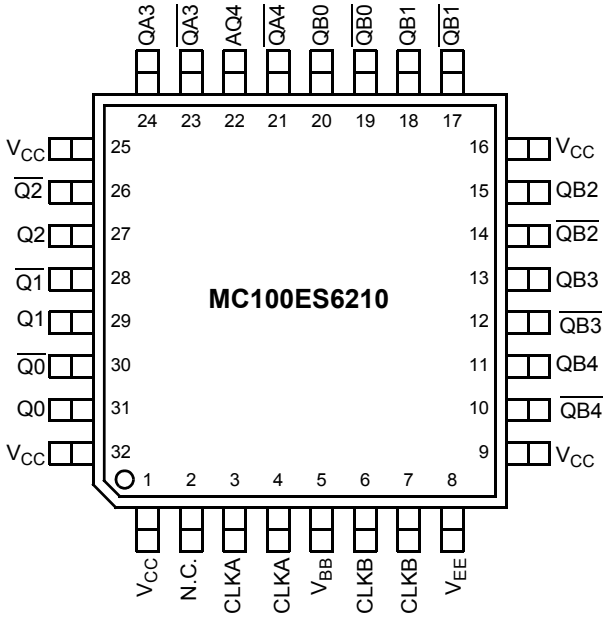


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLKA, CLKA	Input	ECL/PECL	Differential reference clock signal input (fanout buffer A)
CLKB, CLKB	Input	ECL/PECL	Differential reference clock signal input (fanout buffer B)
QA[0-4], QA[0-4]	Output	ECL/PECL	Differential clock outputs (fanout buffer A)
QB[0-4], QB[0-4]	Output	ECL/PECL	Differential clock outputs (fanout buffer B)
VEE[1]	Supply		Negative power supply
V_{CC}	Supply		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
VBB	Output	DC	Reference voltage output for single ended ECL or PECL operation

1. In ECL mode (negative power supply mode), V_{EE} is either –3.3 V or –2.5 V and V_{CC} is connected to GND (0 V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0 V) and V_{CC} is either +3.3 V or +2.5 V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC})

Table 2. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2[1]		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model				V	
LU	Latch-up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T_J	Operating Junction Temperature[2] (continuous operation) MTBF = 9.1 years			110	°C	

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6210 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6210 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 4. PECL DC Characteristics (V_{CC} = 2.5 V ± 5% or V_{CC} = 3.3 V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, CLKB (PECL differential signals)						
V_{PP}	Differential Input Voltage[1]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[2]	1.0		V_{CC} – 0.3	V	Differential operation
I_{IN}	Input Current[1]			±100	μA	V_{IN} = V_{IL} or V_{IN} = V_{IH}
PECL clock outputs (QA0-4, $\overline{\text{QA0-4}}$, QB0-4, QB0-4)						
V_{OH}	Output High Voltage	V_{CC} –1.2	V_{CC} –1.005	V_{CC} –0.7	V	I_{OH} = –30 mA[3]
V_{OL}	Output Low Voltage V_{CC} = 3.3V±5%	V_{CC} –1.9	V_{CC} –1.705	V_{CC} –1.5	V	I_{OL} = –5 mA[3]
	V_{CC} = 2.5V±5%	V_{CC} –1.9	V_{CC} –1.705	V_{CC} –1.3		
Supply current and V_{BB}						
I_{EE}	Maximum Quiescent Supply Current without output termination current		60	100	mA	V_{EE} pin
V_{BB}	Output Reference Voltage	V_{CC} –1.38	V_{CC} –1.26	V_{CC} –1.14	V	I_{BB} = 0.2 mA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
3. Equivalent to a termination of 50Ω to V_{TT}.

Table 5. ECL DC Characteristics (V_{EE} = –2.5 V ± 5% or V_{EE} = –3.3 V ± 5%, V_{CC} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, CLKB (ECL differential signals)						
V_{PP}	Differential input voltage[1]	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage[2]	V_{EE} + 1.0		–0.3	V	Differential operation
I_{IN}	Input Current[1]			±100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL clock outputs (QA0–4, $\overline{\text{QA0–4}}$, QB0–4, QB0–4)						
V_{OH}	Output High Voltage	–1.2	–1.005	–0.7	V	I_{OH} = –30 mA[3]
V_{OL}	Output Low Voltage V_{CC} = 3.3 V ±5% V_{CC} = 2.5 V ±5%	–1.9 –1.9	–1.705 –1.705	–1.5 –1.3	V	I_{OL} = –5 mA[3]
Supply current and V_{BB}						
I_{EE}	Maximum Quiescent Supply Current without output termination current		60	100	mA	V_{EE} pin
V_{BB}	Output reference voltage	–1.38	–1.26	–1.14	V	I_{BB} = 0.2 mA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
3. Equivalent to a termination of 50Ω to V_{TT}.

Table 6. AC Characteristics (ECL: V_{EE} = –3.3 V ± 5% or V_{EE} = –2.5 V ± 5%, V_{CC} = GND) or (PECL: V_{CC} = 3.3 V ± 5% or V_{CC} = 2.5 V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)[1,2]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (PECL or ECL differential signals)						
V_{PP}	Differential Input Voltage[3] (peak-to-peak)	0.3	0.3	1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[4] PECL ECL	 1.2 V_{EE} + 1.2		 V_{CC} – 0.3 –0.3V	 V V	
ECL clock outputs (Q0–9, $\overline{\text{Q0–9}}$)						
f_{CLK}	Input Frequency	0		3000	MHz	Differential
t_{PD}	Propagation Delay CLKA to QAx or CLKB to QBx	 175	 260	 350	 ps	 Differential
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak) f_O < 1.1 GHz f_O < 2.5 GHz f_O < 3.0 GHz	 0.45 0.35 0.20	 0.70 0.55 0.35		 V V V	
$t_{sk(O)}$	Output-to-Output Skew (per bank)		13	30	ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part)			175	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			1		
$t_{SK(P)}$	Output Pulse Skew[5]			50	ps	
DC_Q	Output Duty Cycle f_{REF} < 0.1 GHz f_{REF} < 1.0 GHz	49.5 45.0	50 50	50.5 55.0	% %	DC_{REF} = 50% DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time	30		250	ps	20% to 80%

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
4. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
5. Output pulse skew is the absolute difference of the propagation delay times: $|t_{PLH} - t_{PHL}|$.

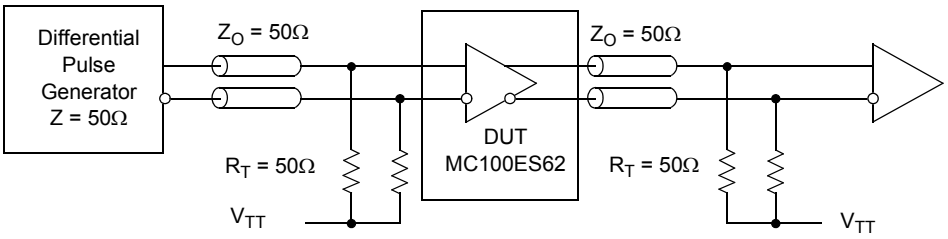


Figure 3. MC100ES6210 AC Test Reference

Order number: MC100ES6220
Rev 2, 08/2004

Low Voltage Dual 1:10 Differential ECL/PECL Clock Fanout Buffer

MC100ES6220

LOW VOLTAGE DUAL 1:10 DIFFERENTIAL ECL/PECL CLOCK FANOUT BUFFER

TB SUFFIX
52-LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336A-01

The MC100ES6220 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6220 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are high performance clock distribution in computing, networking and telecommunication systems.

Features

- Two independent 1:10 differential clock fanout buffers
- 130 ps maximum device skew
- SiGe technology
- Supports DC to 1GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL compatible differential clock inputs
- Single 3.3 V, –3.3 V, 2.5 V or –2.5 V supply
- Standard 52-lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP220

Functional Description

The MC100ES6220 is designed for low skew clock distribution systems and supports clock frequencies up to 1 GHz. The device consists of two independent clock fanout buffers. The CLKA and CLKB inputs can be driven by ECL or PECL compatible signals. The input signal of each clock buffer is distributed to 10 identical, differential ECL/PECL outputs. If V_{BB} is connected to the $\overline{CLKA}$ or $\overline{CLKB}$ input and bypassed to GND by a 10 nF capacitor, the MC100ES6220 can be driven by single-ended ECL/PECL signals utilizing the V_{BB} bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6220 can be operated from a single 3.3 V or 2.5 V supply. As most other ECL compatible devices, the MC100ES6220 supports positive (PECL) and negative (ECL) supplies. The MC100ES6220 is pin and function compatible to the MC100EP220.

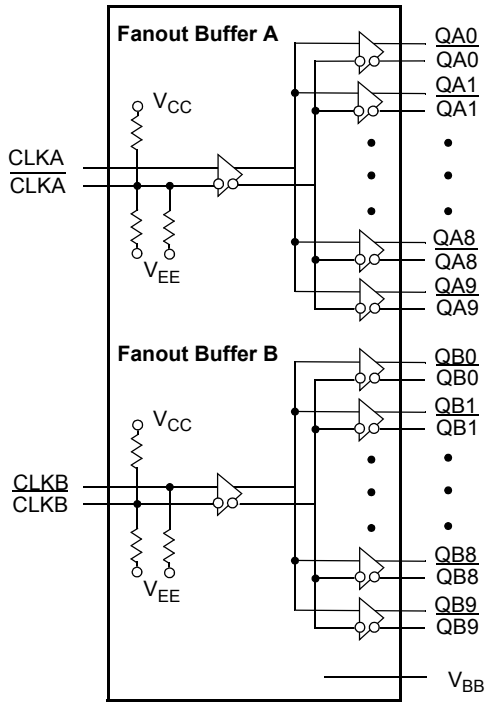


Figure 1. MC100ES6220 Logic Diagram

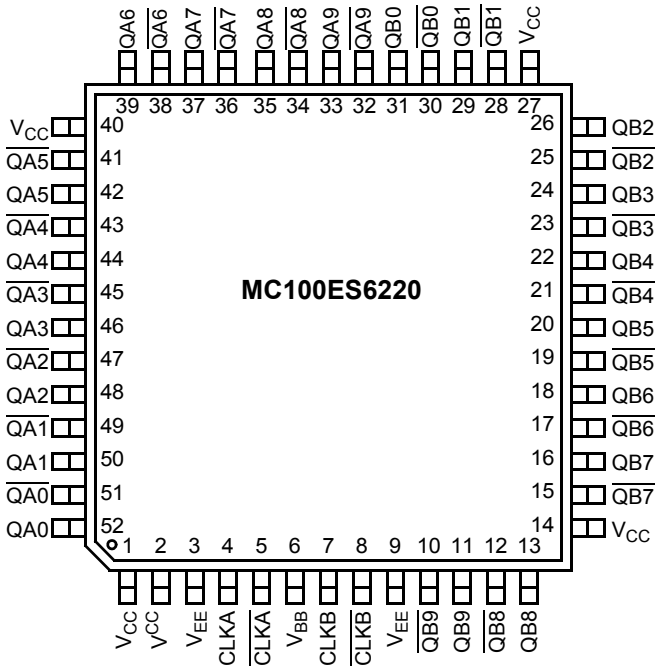


Figure 2. 52-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLKA, CLKA	Input	ECL/PECL	Differential reference clock signal input for fanout buffer A
CLKB, CLKB	Input	ECL/PECL	Differential reference clock signal input for fanout buffer B
QA[0-9], QA[0-9]	Output	ECL/PECL	Differential clock outputs of fanout buffer A
QB[0-9], QB[0-9]	Output	ECL/PECL	Differential clock outputs of fanout buffer B
V_{EE}[1]	Supply		Negative power supply
V_{CC}	Supply		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
VBB	Output	DC	Reference voltage output for single ended ECL and PECL operation

1. In ECL mode (negative power supply mode), V_{EE} is either –3.3 V or –2.5 V and V_{CC} is connected to GND (0 V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0 V) and V_{CC} is either +3.3 V or +2.5 V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}).

Table 2. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	
T_{FUNC}	Functional Temperature Range	T_A = –40	T_J = +110	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		V_{CC} – 2[1]		V	
MM	ESD Protection (Machine model)	175			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model	TBD			V	
LU	Latch-up immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA},θ_{JC},θ_{JB}	Thermal resistance (junction-to-ambient, junction-to-board, junction-to-case)	See Table 8. Thermal Resistance			°C/W	
T_J	Operating junction temperature[2] (continuous operation) MTBF = 9.1 years	0		110	°C	

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6220 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6220 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 4. PECL DC Characteristics (V_{CC} = 2.5 V ± 5% or V_{CC} = 3.3 V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (PECL differential signals)						
V_{PP}	Differential Input Voltage[1]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[2]	1.0		V_{CC} – 0.3	V	Differential operation
I_{IN}	Input Current[1]			±150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock inputs (PECL single ended signals)						
V_{IH}	Input Voltage High	V_{CC} – 1.165		V_{CC} – 0.880	V	
V_{IL}	Input Voltage Low	V_{CC} – 1.810		V_{CC} – 1.475	V	
I_{IN}	Input Current[3]			±150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
PECL clock outputs (QA0-A9, $\overline{\text{QA0-A9}}$, QB0-B9, $\overline{\text{QB0-B9}}$)						
V_{OH}	Output High Voltage	V_{CC} – 1.1	V_{CC} – 1.005	V_{CC} – 0.7	V	I_{OH} = –30 mA[4]
V_{OL}	Output Low Voltage	V_{CC} – 1.9	V_{CC} – 1.705	V_{CC} – 1.4	V	I_{OL} = –5 mA[4]
Supply current and V_{BB}						
I_{EE}[5]	Maximum Quiescent Supply Current without output termination current		80	130	mA	V_{EE} pins
V_{BB}	Output Reference Voltage	V_{CC} – 1.42		V_{CC} – 1.20	V	I_{BB} = 0.3 mA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
3. Input have internal pullup/pulldown resistors which affect the input current.
4. Termination 50Ω to V_{TT}.
5. I_{CC} calculation: I_{CC} = (number of differential output used) x (I_{OH} + I_{OL}) + I_{EE}
   I_{CC} = (number of differential output used) x (V_{OH} – V_{TT}) ÷ R_{load} + (V_{OL} – V_{TT}) ÷R_{load} + I_{EE}.

Table 5. ECL DC Characteristics (V_{EE} = –2.5 V ± 5% or V_{EE} = –3.3 V ± 5%, V_{CC} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLKA, $\overline{\text{CLKA}}$, CLKB, $\overline{\text{CLKB}}$ (ECL differential signals)						
V_{PP}	Differential Input Voltage[1]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[2]	V_{EE} + 1.0		–0.3	V	Differential operation
I_{IN}	Input Current[1]			±150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock inputs (ECL single ended signals)						
V_{IH}	Input Voltage High	–1.165		–0.880	V	
V_{IL}	Input Voltage Low	–1.810		–1.475	V	
I_{IN}	Input Current[3]			±150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL clock outputs (QA0–A9, $\overline{\text{QA0–A9}}$, QB0–B9, $\overline{\text{QB0–B9}}$)						
V_{OH}	Output High Voltage	–1.1	–1.005	–0.7	V	I_{OH} = –30 mA[4]
V_{OL}	Output Low Voltage	–1.9	–1.705	–1.4	V	I_{OL} = –5 mA[4]
Supply current and V_{BB}						
I_{EE}[5]	Maximum Quiescent Supply Current without output termination current		80	130	mA	V_{EE} pins
V_{BB}	Output Reference Voltage	–1.42		–1.20	V	I_{BB} = 0.3 mA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
3. Input have internal pullup/pulldown resistors which affect the input current.
4. Termination 50Ω to V_{TT}.
5. I_{CC} calculation: I_{CC} = (number of differential output used) x (I_{OH} + I_{OL}) + I_{EE}
   I_{CC} = (number of differential output used) x (V_{OH} – V_{TT}) ÷ R_{load} + (V_{OL} – V_{TT}) ÷ R_{load} + I_{EE}.

Table 6. AC Characteristics (ECL: V_{EE} = –3.3 V ± 5% or V_{EE} = –2.5 V ± 5%, V_{CC} = GND) or (PECL: V_{CC} = 3.3 V ± 5% or V_{CC} = 2.5 V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
Clock input pair CLKA, CLKA, CLKB, CLKB (PECL or ECL differential signals)							
V_{PP}	Differential Input Voltage[2] (peak-to-peak)		0.3		1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[3]	PECL ECL	1.1 V_{EE} + 1.1		V_{CC} – 0.3 –0.3	V V	
f_{CLK}	Input Frequency		0		1000	MHz	Differential
PECL/ECL clock outputs (QA0-A9, $\overline{QA0\text{-}A9}$, QB0-B9, $\overline{QB0\text{-}B9}$)							
t_{PD}	Propagation Delay CLKx to Qx0-9		285		550	ps	Differential
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak)		400	600		mV	
$t_{sk(O)}$	Output-to-Output Skew			60	130	ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part)				200	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter				1	ps	
$t_{SK(P)}$	Output Pulse Skew[4]				35	ps	
DC_O	Output Duty Cycle	f_{REF} < 0.1 GHz f_{REF} < 1.0 GHz	49.65 46.5	50 50	50.35 53.5	% %	DC_{REF} = 50% DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time		50		350	ps	20% to 80%

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
3. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
4. Output pulse skew is the absolute difference of the propagation delay times: $| t_{pLH} - t_{pHL} |$.

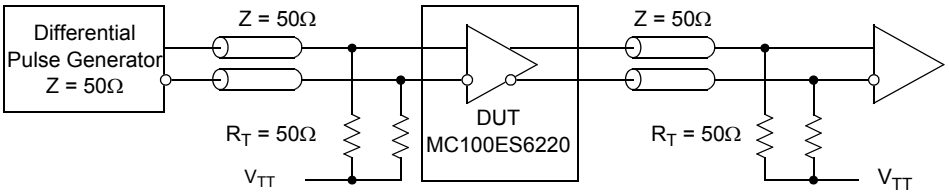


Figure 3. MC100ES6220 AC Test Reference

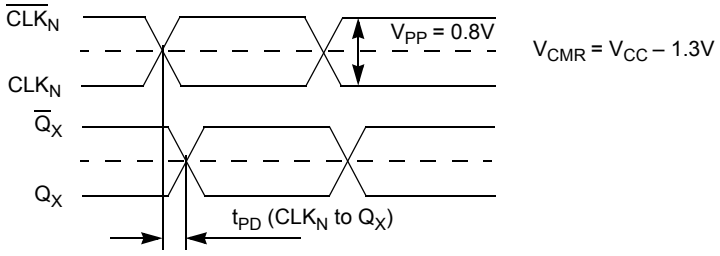


Figure 4. MC100ES6220 AC Reference Measurement Waveform

APPLICATIONS INFORMATION

Understanding the Junction Temperature Range of the MC100ES6220

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6220, the MC100ES6220 is specified, characterized and tested for the junction temperature range of T_J=0°C to +110°C. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this data sheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 17 °C/W (2s2p board, 200 ft/min airflow, see Table 8) and a typical power consumption of 1049 mW (all outputs terminated 50 ohms to V_{TT}, V_{CC} = 3.3V, frequency independent), the junction temperature of the MC100ES6220 is approximately T_A + 18 °C, and the minimum ambient temperature in this example case calculates to –18 °C (the maximum ambient temperature is 92 °C. See Table 7). Exceeding the minimum junction temperature specification of the MC100ES6220 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6220 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the application note AN1545 for a power consumption calculation guideline.

Table 7. Ambient Temperature Ranges (P_{tot} = 1049 mW)

R_{thja} (2s2p board)		$T_{A, min}$[1]	$T_{A, max}$
Natural convection	20 °C/W	–21°C	89°C
100 ft/min	18 °C/W	–19°C	91°C
200 ft/min	17 °C/W	–18°C	92°C
400 ft/min	16 °C/W	–17°C	93°C
800 ft/min	15 °C/W	–16°C	94°C

1. The MC100ES6220 device function is guaranteed from T_A = –40 °C to T_J=110 °C

Maintaining Lowest Device Skew

The MC100ES6220 guarantees low output-to-output bank skew of 100 ps and a part-to-part skew of max. 200 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6220 is a mixed analog/digital product. The differential architecture of the MC100ES6220 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

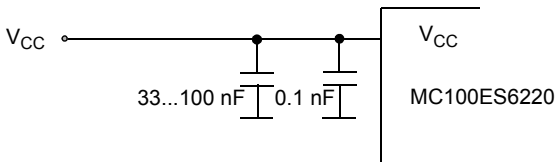


Figure 5. V_{CC} Power Supply Bypass

APPLICATIONS INFORMATION

Using the Thermally Enhanced Package of the MC100ES6220

The MC100ES6220 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the lead frame is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100ES6220 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES6220. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is a requirement for MC100ES6220 applications on multi-layer boards. The recommended thermal land design comprises a 3 x 3 thermal via array as shown in Figure 6, providing an efficient heat removal path.

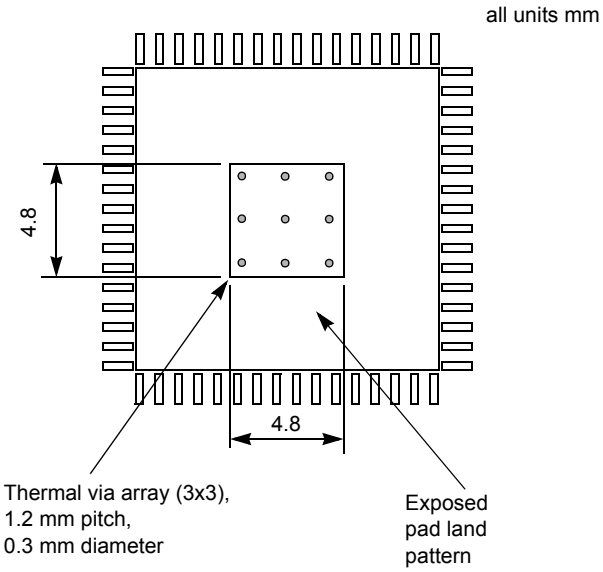


Figure 6. Recommended thermal land pattern

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. ‘ shows a recommend solder mask opening with respect to the recommended 3 x 3 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 7. For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

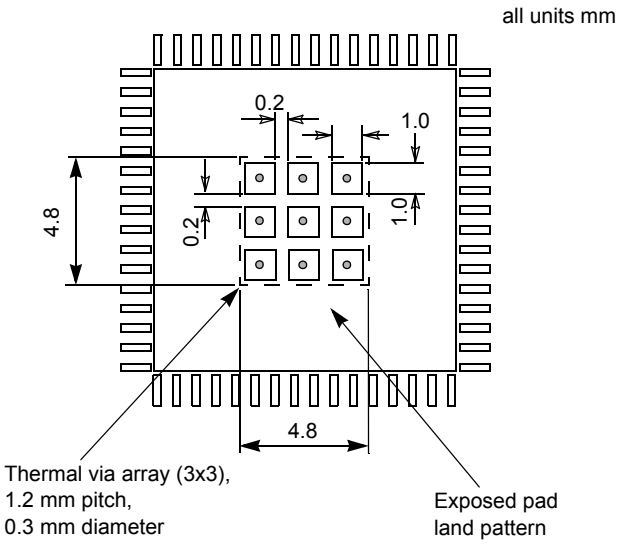


Figure 7. Recommended Solder Mask Openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 8. Thermal Resistance[1]

Convection LFPM	R_{THJA}[2] °C/W	R_{THJA}[3] °C/W	R_{THJC} °C/W	R_{THJB}[4] °C/W
Natural	20	48	4[5] 29[6]	16
100	18	47		
200	17	46		
400	16	43		
800	15	41		

1. Applicable for a 3 x 3 thermal via array
2. Junction to ambient, four conductor layer test board (2S2P), per JES51-7 and JESD 51-5
3. Junction to ambient, single layer test board, per JESD51-3
4. Junction to board, four conductor layer test board (2S2P) per JESD 51-8
5. Junction to exposed pad
6. Junction to top of package

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES6220 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

Order number: MC100ES6221
Rev 3, 08/2004

Low Voltage 1:20 Differential ECL/PECL/HSTL Clock Fanout Buffer

MC100ES6221

LOW VOLTAGE DUAL 1:20 DIFFERENTIAL ECL/PECL/HSTL CLOCK FANOUT BUFFER

TB SUFFIX
52-LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336A-01

The MC100ES6221 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6221 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:20 differential clock fanout buffer
- 100 ps maximum device skew
- SiGe technology
- Supports DC to 2 GHz operation of clock or data signals
- ECL/PECL compatible differential clock outputs
- ECL/PECL/HSTL compatible differential clock inputs
- Single 3.3V, –3.3V, 2.5V or –2.5V supply
- Standard 52 lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP221

Functional Description

The MC100ES6221 is designed for low skew clock distribution systems and supports clock frequencies up to 2 GHz. The device accepts two clock sources. The CLK0 input can be driven by ECL or PECL compatible signals, the CLK1 input accepts HSTL compatible signals. The selected input signal is distributed to 20 identical, differential ECL/PECL outputs. If V_{BB} is connected to the $\overline{CLK0}$ or $\overline{CLK1}$ input and bypassed to GND by a 10 nF capacitor, the MC100ES6221 can be driven by single-ended ECL/PECL signals utilizing the V_{BB} bias voltage output.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6221 can be operated from a single 3.3 V or 2.5 V supply. As most other ECL compatible devices, the MC100ES6221 supports positive (PECL) and negative (ECL) supplies. The MC100ES6221 is pin and function compatible to the MC100EP221.

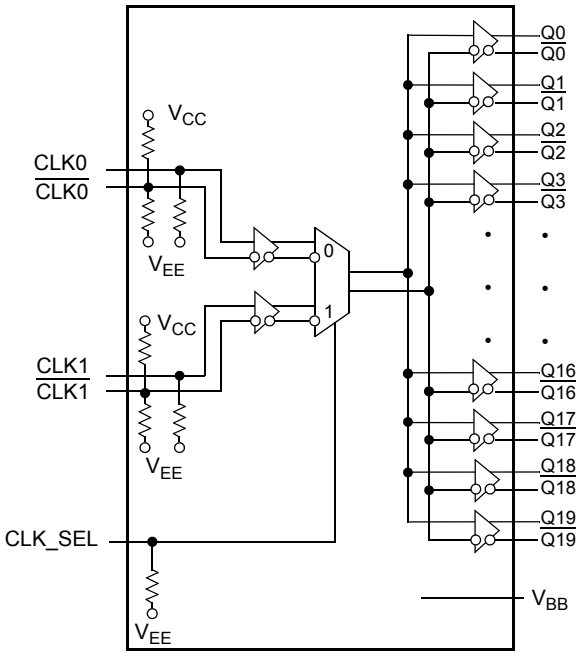


Figure 1. MC100ES6221 Logic Diagram

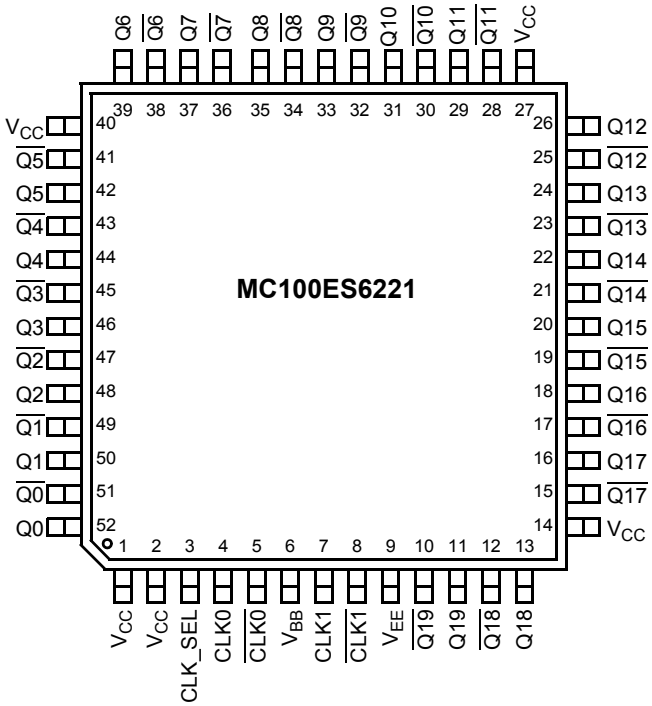


Figure 2. 52-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLK0, $\overline{\text{CLK0}}$	Input	ECL/PECL	Differential reference clock signal input
CLK1, $\overline{\text{CLK1}}$	Input	HSTL	Alternative differential reference clock signal input
CLK_SEL	Input	ECL/PECL	Reference clock input select
QA[0–19], QA[0–19]	Output	ECL/PECL	Differential clock outputs
V_{EE}[1]	Supply		Negative power supply
V_{CC}	Supply		Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.
V_{BB}	Output	DC	Reference voltage output for single ended ECL and PECL operation

1. In ECL mode (negative power supply mode), V_{EE} is either –3.3 V or –2.5 V and V_{CC} is connected to GND (0 V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0 V) and V_{CC} is either +3.3 V or +2.5 V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}).

Table 2. Function Table

Pin	0	1
CLK_SEL	CLK0, $\overline{\text{CLK0}}$ input pair is the reference clock. CLK0 can be driven by ECL or PECL compatible signals.	CLK1, $\overline{\text{CLK1}}$ input pair is the reference clock. CLK1 can be driven by HSTL compatible signals.

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	
T_{FUNC}	Functional Temperature Range	T_A = –40	T_J = +110	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		V_{CC} – 2[1]		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	TBD			V	
LU	Latch-up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}, θ_{JB}, θ_{JC}	Thermal Resistance (junction-to-ambient, junction-to-board, junction-to-case)	See Table 9. Thermal Resistance			°C/W	
T_J	Operating Junction Temperature[2] (continuous operation) MTBF = 9.1 years	0		110	°C	

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6221 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6221 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. PECL DC Characteristics (V_{CC} = 2.5V ± 5% or V_{CC} = 3.3V±5%, V_{EE} = GND, TJ = 0°C to + 110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$[1] (PECL differential signals)						
V_{PP}	Differential Input Voltage[2]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[3]	1.0		V_{CC} – 0.3	V	Differential operation
I_{IN}	Input Current[1]			±100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock input pair CLK1, $\overline{CLK1}$[4] (HSTL differential signals)						
V_{DIF}	Differential Input Voltage[5]	0.2		1.4	V	
V_X	Differential Cross Point Voltage[6]	0	0.68 - 0.9	V_{CC} – 0.7	V	
V_{IH}	Input High Voltage	V_X + 0.1		V_X + 0.7	V	
V_{IL}	Input Low Voltage	V_X – 0.7		V_X – 0.1	V	
I_{IN}	Input Current			±100	μA	$V_{IN} = V_X$ ± 0.2V
Clock inputs (PECL single ended signals)						
V_{IH}	Input Voltage High	V_{CC} – 1.165		V_{CC} – 0.880	V	
V_{IL}	Input Voltage Low	V_{CC} – 1.810		V_{CC} – 1.475	V	
I_{IN}	Input Current[7]			±100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
PECL clock outputs (Q0–19, $\overline{Q0–19}$)						
V_{OH}	Output High Voltage	V_{CC} – 1.1	V_{CC} – 1.005	V_{CC} – 0.7	V	I_{OH} = –30 mA[8]
V_{OL}	Output Low Voltage	V_{CC} – 1.9	V_{CC} – 1.705	V_{CC} – 1.4	V	I_{OL} = –5 mA[8]
Supply current and V_{BB}						
I_{EE}[9]	Maximum Quiescent Supply Current without output termination current		84	160	mA	V_{EE} pins
V_{BB}	Output Reference Voltage (f_{ref} < 1.0 GHz)[10]	V_{CC} – 1.42		V_{CC} – 1.20	V	I_{BB} = 0.4 mA

1. The input pairs CLK0, CLK1 are compatible to differential signaling standards. CLK0 is compatible to LVPECL signals and CLK1 meets both HSTL differential signal specifications. The difference between CLK0 and CLK1 is the differential input threshold voltage (V_{CMR}).
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. Clock inputs driven by differential HSTL compatible signals. Only applicable to CLK1, $\overline{CLK1}$.
5. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
6. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
7. Inputs have internal pullup/pulldown resistors which affect the input current.
8. Equivalent to a termination of 50Ω to V_{TT}.
9. I_{CC} calculation: I_{CC} = (number of differential output used) x (I_{OH} + I_{OL}) + I_{EE}
   I_{CC} = (number of differential output used) x (V_{OH} – V_{TT}) ÷ R_{load} + (V_{OL} – V_{TT}) ÷ R_{load} + I_{EE}.
10. Using V_{BB} to bias unused single-ended inputs is recommended only up to a clock reference frequency of 1 GHz. Above 1 GHz, only differential input signals should be used with the MC100ES6221.

Table 6. ECL DC Characteristics (V_{EE} = –2.5 V ± 5% or V_{EE} = –3.3 V ± 5%, V_{CC} = GND, T_J = 0°C to + 110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$ (ECL differential signals)						
V_{PP}	Differential Input Voltage[1]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Junction to top of package voltage[2]	V_{EE} + 1.0		–0.3	V	Differential operation
I_{IN}	Input Current[1]			±100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock inputs (ECL single ended signals)						
V_{IH}	Input Voltage High	–1.165		–0.880	V	
V_{IL}	Input Voltage Low	–1.810		–1.475	V	
I_{IN}	Input Current[3]			±100	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL clock outputs (Q0–A19, $\overline{Q0–Q19}$)						
V_{OH}	Output High Voltage	–1.1	–1.005	–0.7	V	I_{OH} = –30 mA[4]
V_{OL}	Output Low Voltage	–1.9	–1.705	–1.4	V	I_{OL} = –5 mA[4]
Supply current and V_{BB}						
I_{EE}[5]	Maximum Quiescent Supply Current without output termination current		84	160	mA	V_{EE} pins
V_{BB}	Output Reference Voltage (f_{ref} < 1.0 GHz)[6]	–1.42		–1.20	V	I_{BB} = 0.4 mA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
3. Inputs have internal pullup/pulldown resistors which affect the input current.
4. Equivalent to a termination of 50Ω to V_{TT}.
5. I_{CC} calculation: I_{CC} = (number of differential output used) x (I_{OH} + I_{OL}) + I_{EE}
   I_{CC} = (number of differential output used) x (V_{OH} – V_{TT}) ÷ R_{load} + (V_{OL} – V_{TT}) ÷ R_{load} + I_{EE}.
6. V_{BB} can be used to bias unused single-ended inputs up to a clock reference frequency of 1 GHz. Above 1 GHz, only differential signals should be used with the MC100ES6221.

Table 7. AC Characteristics (ECL: V_{EE} = –3.3 V ± 5% or V_{EE} = –2.5 V± 5%, V_{CC} = GND) or (PECL: V_{CC} = 3.3 V ± 5% or V_{CC} = 2.5 V± 5%, V_{EE} = GND, T_J = 0°C to + 110°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$ (PECL or ECL differential signals)						
V_{PP}	Differential Input Voltage[2] (peak-to-peak)	0.2		1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[3] PECL ECL	1.0 V_{EE} + 1.0		V_{CC} – 0.3 –0.3V	V V	
f_{CLK}	Input Frequency	0		2000	MHz	Differential
t_{PD}	Propagation Delay CLK0 to Q0-19	400	540	670	ps	Differential
Clock input pair CLK1, $\overline{CLK1}$ (HSTL differential signals)						
V_{DIF}	Differential Input Voltage[4] (peak-to-peak)	0.2		1.3	V	
V_X	Differential Input Crosspoint Voltage[5]	0.1	0.68–0.9	V_{CC} – 1.0	V	
f_{CLK}	Input Frequency	0		1000	MHz	Differential
t_{PD}	Propagation Delay CLK1 to Q0–19	650	780	950	ps	Differential
PECL/ECL clock outputs (Q0–19, $\overline{Q0–19}$)						
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak) f_O < 1.0 GHz f_O < 2.0 GHz	 0.375 TDB	 0.630 0.250		 V V	
$t_{sk(O)}$	Output-to-Output Skew		50	100	ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part) using CLK0 using CLK1 parts at one given T_J, V_{CC}, f_{ref}			 270 300 250	 ps ps ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			1	ps	
$t_{SK(P)}$	Output Pulse Skew[6]		30	50	ps	
DC_Q	Output Duty Cycle f_{REF} < 0.1 GHz f_{REF} < 1.0 GHz	49.5 45.0	50 50	50.5 55.0	% %	DC_{REF} = 50% DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time	50		350	ps	20% to 80%

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
3. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
4. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew. Only applicable to CLKB.
5. V_X (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF} (AC) impacts the device propagation delay, device and part-to-part skew.
6. Output pulse skew is the absolute difference of the propagation delay times: $| t_{pLH} - t_{pHL} |$.

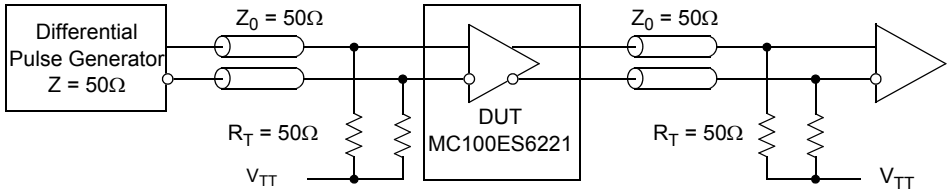


Figure 3. MC100ES6221 Test Reference

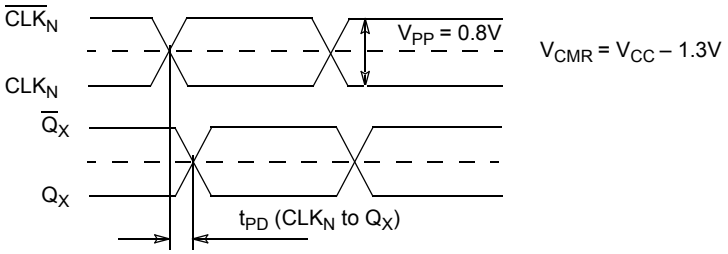


Figure 4. MC100ES6221 AC Test Reference Measurement Waveform

APPLICATIONS INFORMATION

Understanding the Junction Temperature Range of the MC100ES6221

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6221, the MC100ES6221 is specified, characterized and tested for the junction temperature range of T_J=0°C to +110°C. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this data sheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 17 °C/W (2s2p board, 200 ft/min airflow, see Table 8) and a typical power consumption of 1148 mW (all outputs terminated 50 ohms to V_{TT}, V_{CC} = 3.3 V, frequency independent), the junction temperature of the MC100ES6221 is approximately T_A + 21 °C, and the minimum ambient temperature in this example case calculates to –21 °C (the maximum ambient temperature is 89 °C. See Table 8). Exceeding the minimum junction temperature specification of the MC100ES6221 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6221 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the application note AN1545 for a power consumption calculation guideline.

Table 8. Ambient Temperature Ranges (P_{tot} =1148 mW)

R_{thja} (2s2p board)		$T_{A, min}$[1]	$T_{A, max}$
Natural convection	20 °C/W	–23 °C	87 °C
100 ft/min	18 °C/W	–21 °C	89 °C
200 ft/min	17 °C/W	–20 °C	90 °C
400 ft/min	16 °C/W	–18 °C	92 °C
800 ft/min	15 °C/W	–17 °C	93 °C

1. The MC100ES6221 device function is guaranteed from T_A = –40 °C to T_J = 110 °C

Maintaining Lowest Device Skew

The MC100ES6221 guarantees low output-to-output bank skew of 50 ps and a part-to-part skew of max. 270 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6221 is a mixed analog/digital product. The differential architecture of the MC100ES6221 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

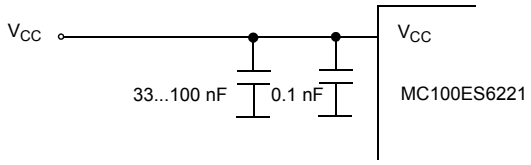


Figure 5. V_{CC} Power Supply Bypass

APPLICATIONS INFORMATION

Using the Thermally Enhanced Package of the MC100ES6221

The MC100ES6221 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so that the lead frame is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance that supports the power consumption of the MC100ES6221 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES6221. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is a requirement for MC100ES6221 applications on multi-layer boards. The recommended thermal land design comprises a 3 x 3 thermal via array as shown in Figure 6, providing an efficient heat removal path.

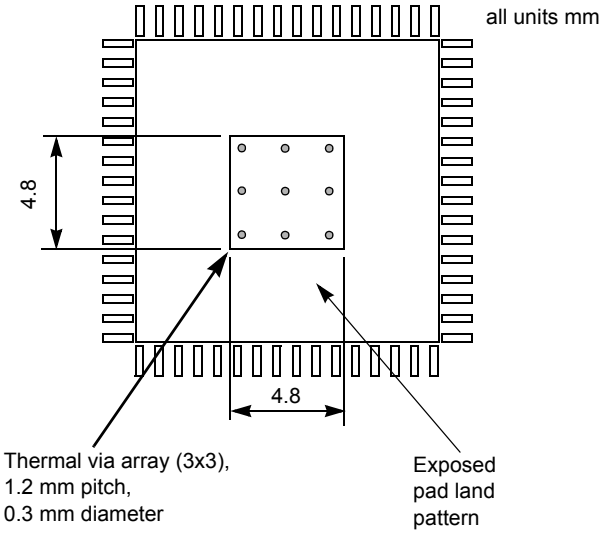


Figure 6. Recommended Thermal Land Pattern

The via diameter is should be approx. 0.3 mm with 1 oz. copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 7 shows a recommend solder mask opening with respect to the recommended 3 x 3 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as shown in Figure 7. For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

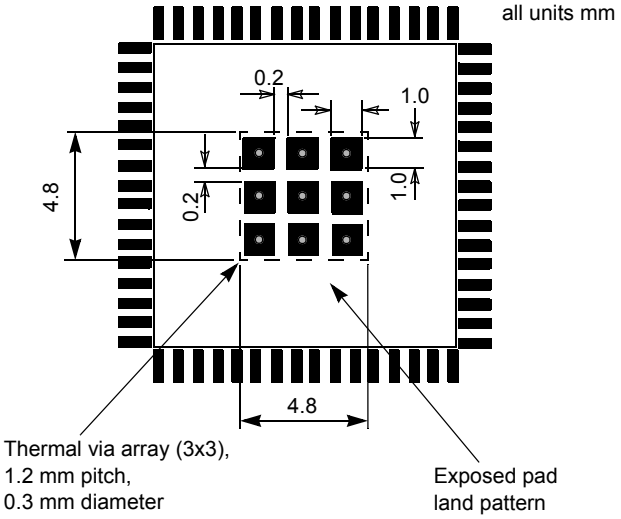


Figure 7. Recommended Solder Mask Openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 9. Thermal Resistance[1]

Convection LFPM	R_{THJA}[2] °C/W	R_{THJA}[3] °C/W	R_{THJC} °C/W	R_{THJB}[4] °C/W
Natural	20	48	4[5] 29[6]	16
100	18	47		
200	17	46		
400	16	43		
800	15	41		

1. Applicable for a 3 x 3 thermal via array
2. Junction to ambient, four conductor layer test board (2S2P), per JES51–7 and JESD 51–5
3. Junction to ambient, single layer test board, per JESD51–3
4. Junction to board, four conductor layer test board (2S2P) per JESD 51–8
5. Junction to exposed pad
6. Junction to top of package

It is recommended that users employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES6221 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

Order number: MC100ES6222
Rev 2, 08/2004

Low Voltage 1:15 Differential ECL/PECL Clock Divider and Fanout Buffer

MC100ES6222

LOW-VOLTAGE 1:15 DIFFERENTIAL ECL/PECL CLOCK DIVIDER AND FANOUT DRIVER

TB SUFFIX
52-LEAD LQFP PACKAGE
EXPOSED PAD
CASE 1336A-01

The MC100ES6222 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6222 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver is high performance clock distribution in computing, networking and telecommunication systems.

Features

- 15 differential ECL/PECL outputs (4 output banks)
- 2 selectable differential ECL/PECL inputs
- Selectable ÷1 or ÷2 frequency divider
- 130 ps maximum device skew
- Supports DC to 3 GHz input frequency
- Single 3.3 V, –3.3 V, 2.5 V or –2.5 V supply
- Standard 52-lead LQFP package with exposed pad for enhanced thermal characteristics
- Supports industrial temperature range
- Pin and function compatible to the MC100EP222

Functional Description

The MC100ES6222 is designed for low skew clock distribution systems and supports clock frequencies up to 3 GHz. The CLK0 and CLK1 inputs can be driven by ECL or PECL compatible signals. Each of the four output banks of two, three, four and six differential clock output pairs can be independently configured to distribute the input frequency or ÷2 of the input frequency. The FSELA, FSELB, FSELC, FSELD, and CLK_SEL are asychronous control inputs. Any changes of the control inputs require a MR pulse for resynchronization of the ÷2 outputs. For the functionality of the MR control input, see Figure 5. Functional Diagram.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all ten outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The MC100ES6222 can be operated from a single 3.3V or 2.5V supply. As most other ECL compatible devices, the MC100ES6222 supports positive (PECL) and negative (ECL) supplies. The MC100ES6222 is pin and function compatible to the MC100EP222.

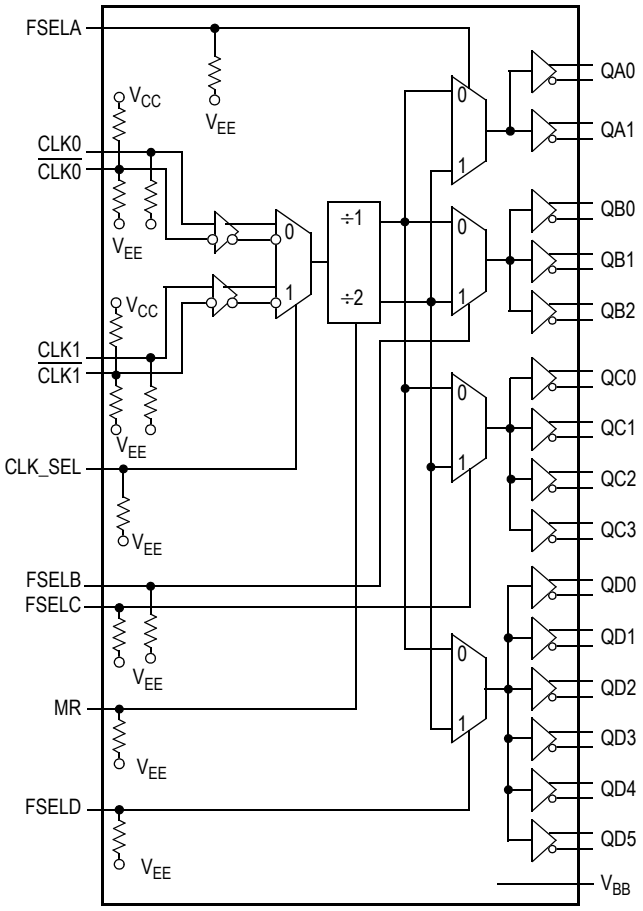


Figure 1. MC100ES6222 Logic Diagram

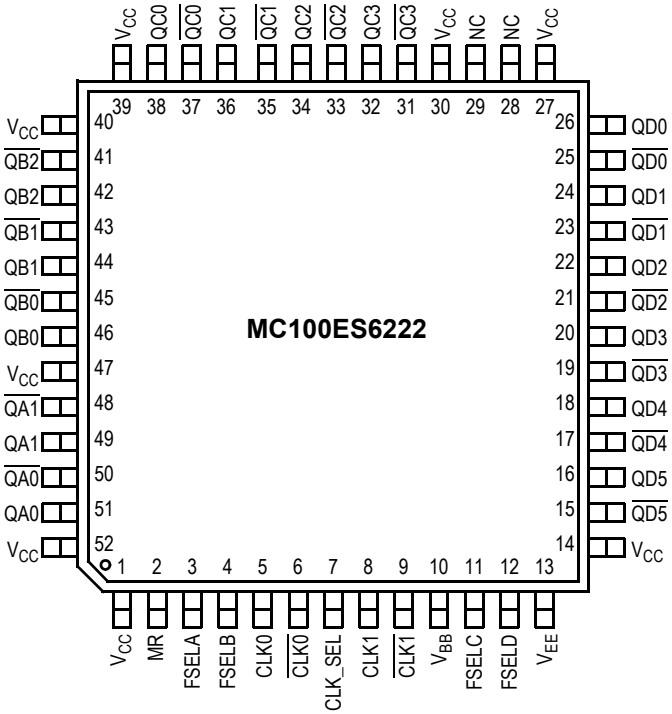


Figure 2. 52-Lead Package Pinout (Top View)

Table 1. Function Table

Control Pin	0	1
FSELA (asynchronous)	÷1	÷2
FSELB (asynchronous)	÷1	÷2
FSELC (asynchronous)	÷1	÷2
FSELD (asynchronous)	÷1	÷2
CLK_SEL (asynchronous)	CLK0	CLK1
MR (asynchronous)	Active	Reset. Q_X = L and $\overline{Q_X}$ = H.

Table 2. Pin Configurations

Pin	I/O	Type	Description
CLK0, $\overline{CLK0}$	Input	ECL/PECL	Differential reference clock signal input
CLK1, $\overline{CLK1}$	Input	ECL/PECL	Alternative differential reference clock signal input
FSELA, FSELB, FSELC, FSELD	Input	ECL/PECL	Selection output frequency divider for bank A, B, C and D
MR	Input	ECL/PECL	Reset
CLK_SEL	Input	ECL/PECL	Clock reference select input
QA[0:1], $\overline{QA[0:1]}$	Output	ECL/PECL	Bank A differential outputs
QB[0:2], $\overline{QB[0:2]}$	Output	ECL/PECL	Bank B differential outputs
QC[0:3], $\overline{QC[0:3]}$	Output	ECL/PECL	Bank C differential outputs
QD[0:5], $\overline{QD[0:5]}$	Output	ECL/PECL	Bank D differential outputs
V_{BB}	Output	DC	Reference voltage output for single ended ECL or PECL operation
V_{EE}[1]		Power supply	Negative power supply
V_{CC}		Power supply	Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation.

1. In ECL mode (negative power supply mode), V_{EE} is either –3.3 V or –2.5 V and V_{CC} is connected to GND (0 V). In PECL mode (positive power supply mode), V_{EE} is connected to GND (0 V) and V_{CC} is either +3.3 V or +2.5 V. In both modes, the input and output levels are referenced to the most positive supply (V_{CC}).

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	
T_{FUNC}	Functional Temperature Range	T_A = –40	T_J = +110	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2[1]		V	
MM	ESD Protection (Machine model)	175			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model	TBD			V	
LU	Latch-up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}, θ_{JC} θ_{JB}	Thermal Resistance (junction-to-ambient, junction-to-board, junction-to-case)	See Table 9. Thermal Resistance			°C/W	
T_J	Operating Junction Temperature[2] (continuous operation) MTBF = 9.1 years	0		110	°C	

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6222 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6222 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. PECL DC Characteristics (V_{CC} = 2.5 V ± 5% or V_{CC} = 3.3 V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock Input Pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (PECL differential signals)						
V_{PP}	Differential Input Voltage[1]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[2]	1.0		V_{CC} – 0.3	V	Differential operation
I_{IN}	Input Current[1]			±150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock Inputs MR, CLK_SEL, FSELA, FSELB, FSELC, FSELD (PECL single ended signals)						
V_{IH}	Input Voltage High	V_{CC} – 1.165		V_{CC} – 0.880	V	
V_{IL}	Input Voltage Low	V_{CC} – 1.810		V_{CC} – 1.475	V	
I_{IN}	Input Current[3]			±150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
PECL clock outputs (QA[0:1], $\overline{QA[0:1]}$, QB[0:2], $\overline{QB[0:2]}$, QC[0:3], $\overline{QC[0:3]}$, QD[0:5], $\overline{QD[0:5]}$						
V_{OH}	Output High Voltage	V_{CC} – 1.1	V_{CC} – 1.005	V_{CC} – 0.7	V	I_{OH} = –30 mA[4]
V_{OL}	Output Low Voltage	V_{CC} – 1.9	V_{CC} – 1.705	V_{CC} – 1.4	V	I_{OL} = –5 mA[4]
Supply current and V_{BB}						
I_{EE}[5]	Maximum Quiescent Supply Current without Output Termination Current		96	170	mA	V_{EE} pins
V_{BB}	Output Reference Voltage	V_{CC} – 1.38		V_{CC} – 1.22	V	I_{BB} = 0.4 mA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
3. Input have internal pullup/pulldown resistors which affect the input current.
4. Equivalent to a termination of 50Ω to V_{TT}.
5. I_{CC} calculation: I_{CC} = (number of differential output used) x (I_{OH} + I_{OL}) + I_{EE}
   I_{CC} = (number of differential output used) x (V_{OH} – V_{TT}) ÷ R_{load} + (V_{OL} – V_{TT}) ÷ R_{load} + I_{EE}.

Table 6. ECL DC Characteristics (V_{EE} = –2.5 V ± 5% or V_{EE} = –3.3 V ± 5%, V_{CC} = GND, T_J = 0°C to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock Input Pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (ECL differential signals)						
V_{PP}	Differential Input Voltage[1]	0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[2]	V_{EE} + 1.0		-0.3	V	Differential operation
I_{IN}	Input Current[1]			±150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
Clock Inputs MR, CLK_SEL, FSELA, FSELB, FSELC, FSELD (PECL single ended signals)						
V_{IH}	Input Voltage High	–1.165		–0.880	V	
V_{IL}	Input Voltage Low	–1.810		–1.475	V	
I_{IN}	Input Current[3]			±150	μA	$V_{IN} = V_{IL}$ or $V_{IN} = V_{IH}$
ECL Clock Outputs (QA[0:1], $\overline{QA[0:1]}$, QB[0:2], $\overline{QB[0:2]}$, QC[0:3], $\overline{QC[0:3]}$, QD[0:5], $\overline{QD[0:5]}$						
V_{OH}	Output High Voltage	–1.1	–1.005	–0.7	V	I_{OH} = -30 mA[4]
V_{OL}	Output Low Voltage	–1.9	–1.705	1.4	V	I_{OL} = -5 mA[4]
Supply Current and V_{BB}						
I_{EE}[5]	Maximum Quiescent Supply Current without Output Termination Current		96	170	mA	V_{EE} pins
V_{BB}	Output Reference Voltage	–1.38		–1.22	V	I_{BB} = 0.4 mA

1. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
2. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
3. Input have internal pullup/pulldown resistors which affect the input current.
4. Equivalent to a termination of 50Ω to V_{TT}.
5. I_{CC} calculation: I_{CC} = (number of differential output used) x (I_{OH} + I_{OL}) + I_{EE}
   I_{CC} = (number of differential output used) x (V_{OH} – V_{TT}) ÷ R_{load} + (V_{OL} – V_{TT}) ÷ R_{load} + I_{EE}.

Table 7. AC Characteristics (ECL: V_{EE} = –3.3 V ± 5% or V_{EE} = –2.5 V ± 5%, V_{CC} = GND) or (PECL: V_{CC} = 3.3 V ± 5% or V_{CC} = 2.5 V ± 5%, V_{EE} = GND, T_J = 0°C to +110°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
Clock Input Pair CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$ (PECL or ECL differential signals)							
V_{PP}	Differential Input Voltage[2] (peak-to-peak)		0.2		1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[3]	PECL ECL	1.0 V_{EE}+1.0		V_{CC} – 0.3 -0.3V	V V	
f_{CLK}	Input Frequency		0		2000	MHz	Differential
ECL/PECL Clock Outputs (QA[0:1], $\overline{QA[0:1]}$, QB[0:2], $\overline{QB[0:2]}$, QC[0:3], $\overline{QC[0:3]}$, QD[0:5], $\overline{QD[0:5]}$							
t_{PD}	Propagation Delay	CLK0 or CLK1 to Qx MR to Qx	670	820	970	ps ps	Differential
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak)	f_O < 1.0 GHz f_O < 2.0 GHz	TBD TBD			mV mV	
$t_{sk(O)}$	Output-to-Output Skew	within QA[0:1] within QB[0:2] within QC[0:3] within QD[0:5] any output			35 35 50 60 130	ps ps ps ps ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part)				300	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter				1	ps	
$t_{SK(P)}$	Output Pulse Skew[4]			5	15	ps	
DC_O	Output Duty Cycle	f_{REF} < 0.1 GHz f_{REF} < 1.0 GHz f_{REF} < 2.0 GHz	49.85 48.50 47.00	50 50 50	50.15 51.50 53.00	% % %	DC_{REF} = 50% DC_{REF} = 50% DC_{REF} = 50%
t_r, t_f	Output Rise/Fall Time		50		300	ps	20% to 80%

1. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
2. V_{PP} (AC) is the minimum differential ECL/PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
3. V_{CMR} (AC) is the crosspoint of the differential ECL/PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
4. Output pulse skew is the absolute difference of the propagation delay times: $| t_{pLH} - t_{pHL} |$.

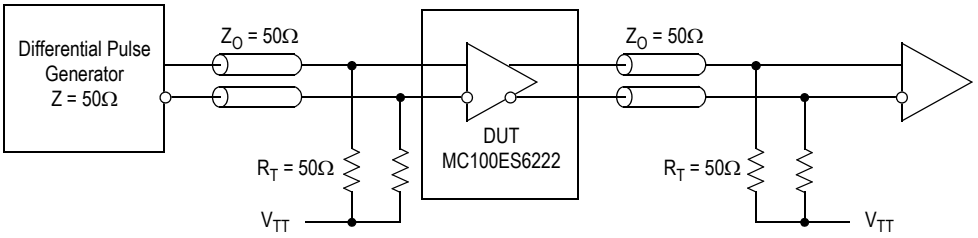


Figure 3. MC100ES6222 AC Test Reference

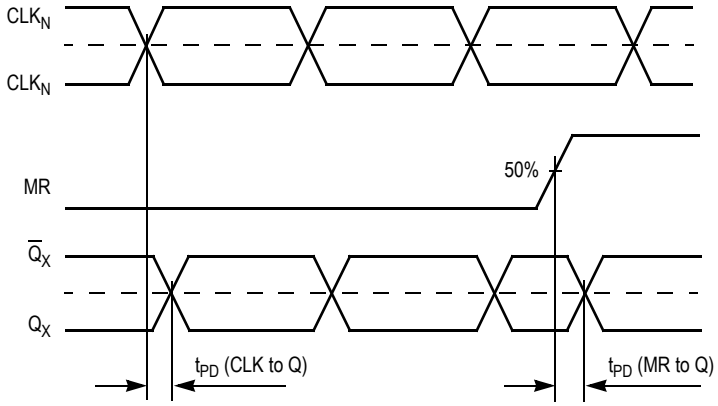


Figure 4. MC100ES6222 t_{PD} Measurement Waveform

APPLICATIONS INFORMATION

Asynchronous Reset Functional Diagram

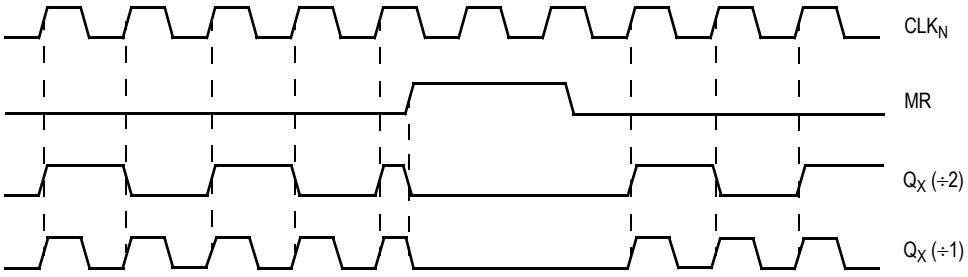


Figure 5. Functional Diagram

APPLICATIONS INFORMATION

Understanding the Junction Temperature Range of the MC100ES6222

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6222, the MC100ES6222 is specified, characterized and tested for the junction temperature range of T_J=0°C to +110°C. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this data sheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 17°C/W (2s2p board, 200 ft/min airflow, see Table 9. Thermal Resistance) and a typical power consumption of 1026 mW (all outputs terminated 50 ohms to V_{TT}, V_{CC}=3.3V, frequency independent), the junction temperature of the MC100ES6222 is approximately T_A + 17°C, and the minimum ambient temperature in this example case calculates to –17°C (the maximum ambient temperature is 93°C, see Table 8). Exceeding the minimum junction temperature specification of the MC100ES6222 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6222 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Please see the application note AN1545 for a power consumption calculation guideline.

Table 8. Ambient Temperature Ranges (P_{tot} = 1026 mW)

R_{thja} (2s2p board)		T_A, Min[1]	T_A, Max
Natural convection	20°C/W	-21°C	89°C
100 ft/min	18°C/W	-18°C	92°C
200 ft/min	17°C/W	-17°C	93°C
400 ft/min	16°C/W	-16°C	94°C
800 ft/min	15°C/W	-15°C	95°C

1. The MC100ES6222 device function is guaranteed from T_A = -40°C to T_J = 110°C.

Maintaining Lowest Device Skew

The MC100ES6222 guarantees low output-to-output bank skew of 130 ps and a part-to-part skew of max. 300 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6222 is a mixed analog/digital product. The differential architecture of the MC100ES6222 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

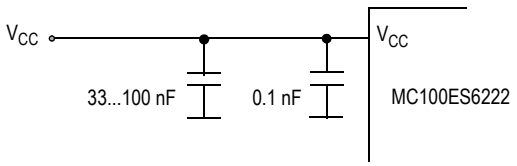


Figure 6. V_{CC} Power Supply Bypass

APPLICATIONS INFORMATION

Using the Thermally Enhanced Package of the MC100ES6222

The MC100ES6222 uses a thermally enhanced exposed pad (EP) 52 lead LQFP package. The package is molded so the lead frame is exposed at the surface of the package bottom side. The exposed metal pad will provide the low thermal impedance supporting the power consumption of the MC100ES6222 high-speed bipolar integrated circuit and eases the power management task for the system design. A thermal land pattern on the printed circuit board and thermal vias are recommended in order to take advantage of the enhanced thermal capabilities of the MC100ES6222. Direct soldering of the exposed pad to the thermal land will provide an efficient thermal path. In multilayer board designs, thermal vias thermally connect the exposed pad to internal copper planes. Number of vias, spacing, via diameters and land pattern design depend on the application and the amount of heat to be removed from the package. A nine thermal via array, arranged in a 3 x 3 array and using a 1.2 mm pitch in the center of the thermal land is a requirement for MC100ES6222 applications on multi-layer boards. The recommended thermal land design comprises a 3 x 3 thermal via array as illustrated in Figure 7. Recommended Thermal Land Pattern, providing an efficient heat removal path.

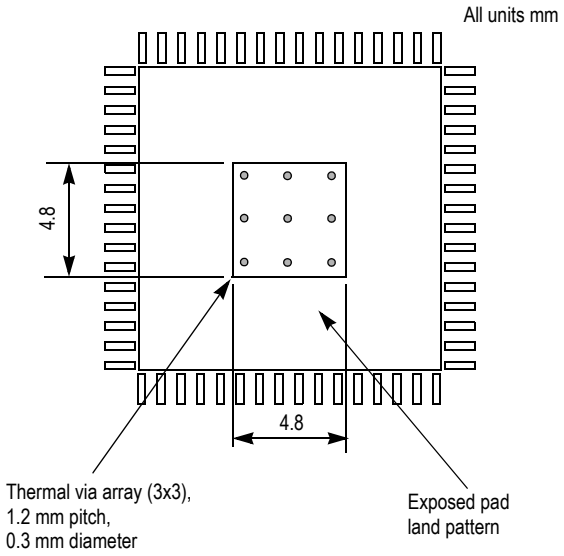


Figure 7. Recommended Thermal Land Pattern

The via diameter is should be approximately 0.3 mm with 1 ounce copper via barrel plating. Solder wicking inside the via resulting in voids during the solder process must be avoided. If the copper plating does not plug the vias, stencil print solder paste onto the printed circuit pad. This will supply enough solder paste to fill those vias and not starve the solder joints. The attachment process for exposed pad package is equivalent to standard surface mount packages. Figure 8. Recommended Solder Mask Openings illustrates a recommend solder mask opening with respect to the recommended 3 x 3 thermal via array. Because a large solder mask opening may result in a poor release, the opening should be subdivided as illustrated in Figure 8. Recommended Solder Mask Openings. For the nominal package standoff 0.1 mm, a stencil thickness of 5 to 8 mils should be considered.

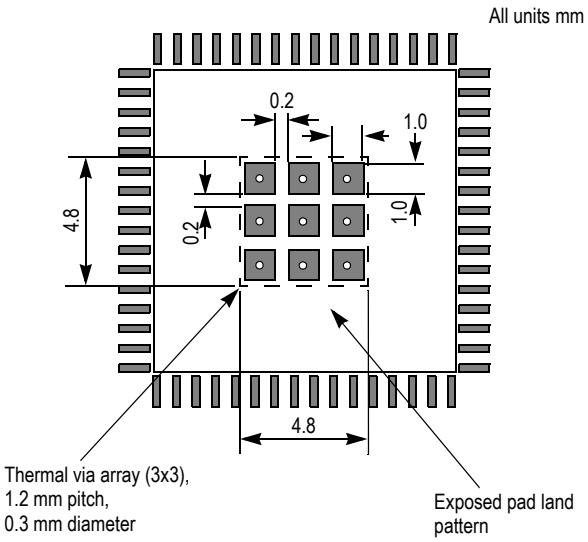


Figure 8. Recommended Solder Mask Openings

For thermal system analysis and junction temperature calculation the thermal resistance parameters of the package is provided:

Table 9. Thermal Resistance[1]

Convection LFPM	R_{THJA}[2] °C/W	R_{THJA}[3] °C/W	R_{THJC} °C/W	R_{THJB}[4] °C/W
Natural	20	48	4[5] 29[6]	16
100	18	47		
200	17	46		
400	16	43		
800	15	41		

1. Applicable for a 3 x 3 thermal via array
2. Junction to ambient, four conductor layer test board (2S2P), per JES51-7 and JESD 51-5
3. Junction to ambient, single layer test board, per JESD51-3
4. Junction to board, four conductor layer test board (2S2P) per JESD 51-8
5. Junction to exposed pad
6. Junction to top of package

It is recommended to employ thermal modeling analysis to assist in applying the general recommendations to their particular application. The exposed pad of the MC100ES6222 package does not have an electrical low impedance path to the substrate of the integrated circuit and its terminals. The thermal land should be connected to GND through connection of internal board layers.

Order number: MC100ES6226
Rev 2, 08/2004

2.5/3.3 V Differential LVPECL 1:9 Clock Distribution Buffer and Clock Divider

MC100ES6226

2.5V/3.3V DIFFERENTIAL LVPECL 1:9 CLOCK DISTRIBUTION BUFFER AND CLOCK DIVIDER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MC100ES6226 is a bipolar monolithic differential clock distribution buffer and clock divider. Designed for most demanding clock distribution systems, the MC100ES6226 supports various applications requiring a large number of outputs to drive precisely aligned clock signals. Using SiGe technology and a fully differential architecture, the device offers superior digital signal characteristics and very low clock skew error. Target applications for this clock driver are high performance clock distribution systems for computing, networking and telecommunication systems.

Features

- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Selectable 1:1 or 1:2 frequency outputs
- LVPECL compatible differential clock inputs and outputs
- LVCMOS compatible control inputs
- Single 3.3V or 2.5V supply
- Max. 35 ps maximum output skew (within output bank)
- Max. 50 ps maximum device skew
- Supports DC operation and up to 3 GHz (typ.) clock signals
- Synchronous output enable eliminating output runt pulse generation and metastability
- Standard 32-lead LQFP package
- Industrial temperature range
- 32-lead Pb-free Package Available

Functional Description

MC100ES6226 is designed for very skew critical differential clock distribution systems and supports clock frequencies from DC up to 3.0 GHz. Typical applications for the MC100ES6226 are primary clock distribution systems on backplanes of high-performance computer, networking and telecommunication systems, as well as on-board clocking of OC-3, OC-12 and OC-48 speed communication systems.

The MC100ES6226 can be operated from a 3.3 V or 2.5 V positive supply without the requirement of a negative supply line. Each of the output banks of three differential clock output pairs may be independently configured to distribute the input frequency or half of the input frequency. The FSEL0 and FSEL1 clock frequency selects are asychronous control inputs. Any changes of the control inputs require a MR pulse for resynchronization of the ÷2 outputs.

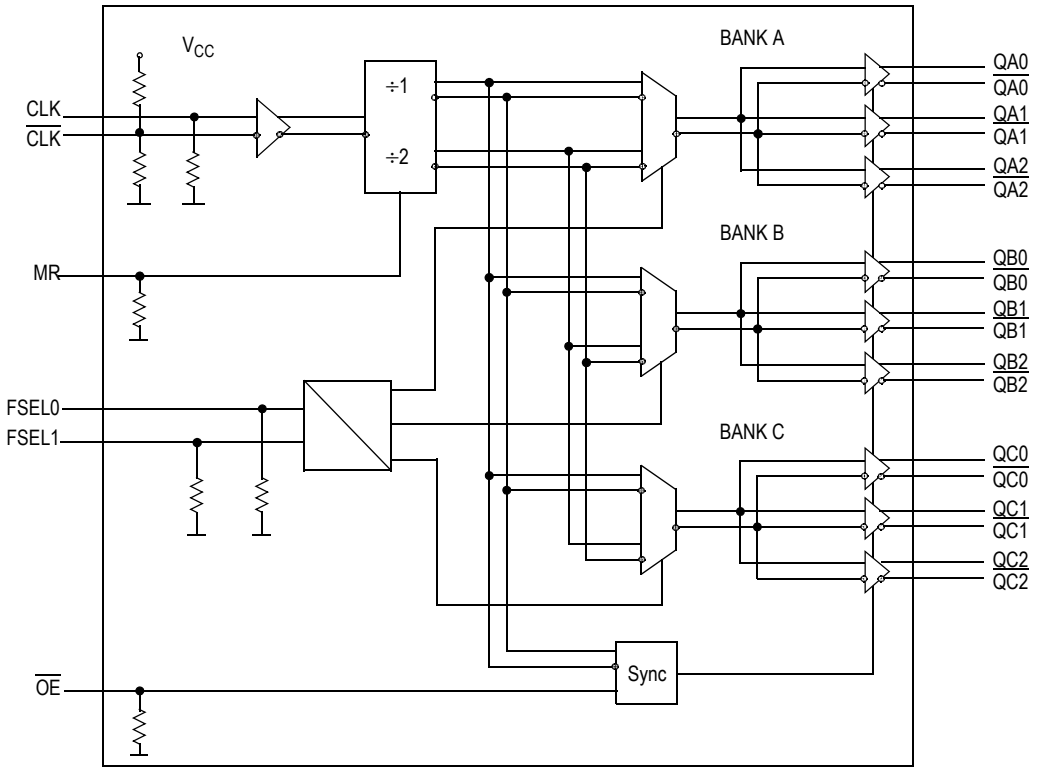


Figure 1. MC100ES6226 Logic Diagram

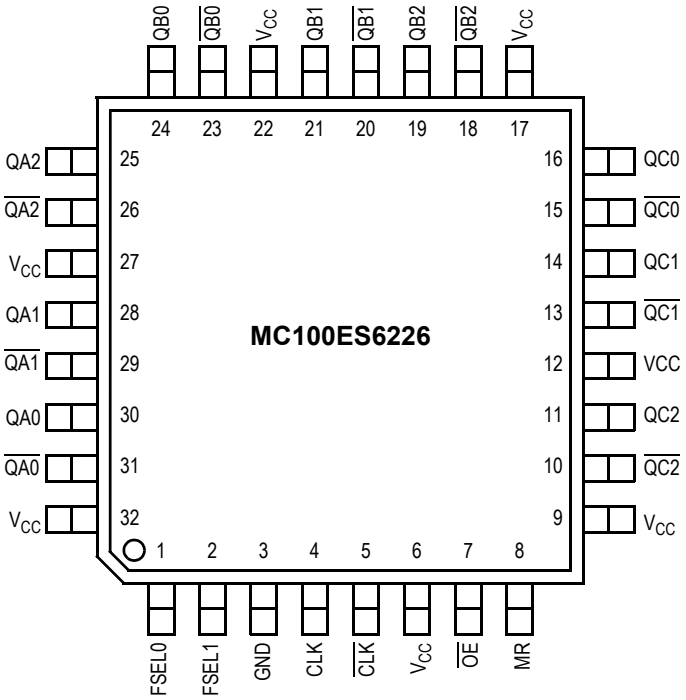


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLK, $\overline{\text{CLK}}$	Input	LVPECL	Differential reference clock signal input
$\overline{\text{OE}}$	Input	LVCMOS	Output enable
MR	Input	LVCMOS	Device reset
FSEL0, FSEL1	Input	LVCMOS	Output frequency divider select
QA[0-2], $\overline{\text{QA[0–2]}}$ QB[0-2], $\overline{\text{QB[0–2]}}$ QC[0-2], $\overline{\text{QC[0–2]}}$	Output	LVPECL	Differential clock outputs (banks A, B and C)
GND	Supply	GND	Negative power supply
V_{CC}	Supply	V_{CC}	Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation

Table 2. Function Table

Control	Default	0	1
$\overline{\text{OE}}$	0	Qx[0–2], $\overline{\text{Qx[0–2]}}$ are active. Deassertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses	Qx[0–2] = L, $\overline{\text{Qx[0–2]}}$ =H (outputs disabled). Assertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses
MR	0	Normal operation	Device reset (asynchronous)
FSEL0, FSEL1	00	See Table 3	

Table 3. Output Frequency Select Control

FSEL0	FSEL1	QA0 to QA2	QB0 to QB2	QC0 to QC2
0	0	$f_{QA0:2} = f_{CLK}$	$f_{QB0:2} = f_{CLK}$	$f_{QC0:2} = f_{CLK}$
0	1	$f_{QA0:2} = f_{CLK}$	$f_{QB0:2} = f_{CLK}$	$f_{QC0:2} = f_{CLK} \div 2$
1	0	$f_{QA0:2} = f_{CLK}$	$f_{QB0:2} = f_{CLK} \div 2$	$f_{QC0:2} = f_{CLK} \div 2$
1	1	$f_{QA0:2} = f_{CLK} \div 2$	$f_{QB0:2} = f_{CLK} \div 2$	$f_{QC0:2} = f_{CLK} \div 2$

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		V_{CC} – 2[1]		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	1000			V	
LU	Latch-up Immunity	200			mA	
C_{IN}			4.0		pF	Inputs
θ_{JA}	Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
	Operating Junction Temperature[2] (continuous operation) MTBF = 9.1 years	0		110	°C	

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6226 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6226 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 6. DC Characteristics (V_{CC} = 3.3 V ± 5% and 2.5 V ± 5%, T_J = 0°C to +110°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs ($\overline{OE}$, FSEL0, FSEL1, MR)							
V_{IL}	Input voltage low	V_{CC} = 3.3 V V_{CC} = 2.5 V			0.8 0.7	V	
V_{IH}	Input voltage high	V_{CC} = 3.3 V V_{CC} = 2.5 V	2.2 1.7			V	
I_{IN}	Input Current[2]				±150	μA	V_{IN} = V_{CC} or V_{IN} = GND
LVPECL Clock Inputs (CLK, $\overline{CLK}$)[3]							
V_{PP}	DC Differential Input Voltage[4]		0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[5]		1.0		V_{CC} – 0.3	V	Differential operation
V_{IH}	Input High Voltage		TBD		TBD		
V_{IL}	Input Low Voltage		TBD		TBD		
I_{IN}	Input Current				±150	μA	V_{IN} = TBD or V_{IN} = TBD
LVPECL Clock Outputs (QA[2:0], QB[2:0], QC[2:0])							
V_{OH}	Output High Voltage		V_{CC} – 1.1		V_{CC} – 0.8	V	Termination 50Ω to V_{TT}
V_{OL}	Output Low Voltage		V_{CC} – 1.8		V_{CC} – 1.4	V	Termination 50Ω to V_{TT}
Supply Current							
I_{GND}	Maximum Quiescent Supply Current without Output Termination Current			65	110	mA	GND pin
I_{CC}	Maximum Quiescent Supply Current with Output Termination Current			325	400	mA	All V_{CC} pins

1. AC characteristics are design targets and pending characterization.
2. Input have internal pullup/pulldown resistors which affect the input current.
3. Clock inputs driven by LVPECL compatible signals.
4. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristic.
5. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5% and 2.5 V ± 5%, T_J = 0°C to +110°C)[1, 2]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{PP}	Differential Input Voltage[3] (peak-to-peak)	0.2	0.3	1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[4]	1.0		V_{CC} – 0.3	V	
$V_{X,OUT}$	Differential Output Crosspoint Voltage	V_{CC} – 1.45		V_{CC} – 1.1	V	
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak) f_O < 300 MHz f_O < 1.5 GHz f_O < 2.7 GHz	 0.45 0.3 TBD	 0.72 0.55 0.37	 0.95 0.95 0.95	 V V V	
f_{CLK}	Input Frequency	0		3000[5]	MHz	
t_{PD}	Propagation Delay CLK to Qx[]	475	500	800	ps	Differential
$t_{sk(O)}$	Output-to-Output Skew (within QA[2:0]) (within QB[2:0]) (within QC[2:0]) (within device)		 11 12 4	 25 25 20 60	 ps ps ps ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part)			325	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter single frequency configuration ÷1/÷2 frequency configuration			 1 1		 FSEL0 = FSEL1 FSEL0 ≠ FSEL1
DC_O	Output Duty Cycle Qx = ÷1, f_O < 300 MHz Qx = ÷1, f_O > 300 MHz Qx = ÷2, f_O < 300 MHz Qx = ÷2, f_O > 300 MHz	48 45 49 47.5	50 50 50 50	52 55 51 52.5	% % % %	DC_{fref}= 50%[7]
t_r, t_f	Output Rise/Fall Time	0.05		200	ns	20% to 80%
t_{PDL}[6]	Output Disable Time	2.5·T + t_{PD}		4.5·T + t_{PD}	ns	T=CLK period
t_{PLD}[7]	Output Enable Time	3·T + t_{PD}		5·T + t_{PD}	ns	T=CLK period

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
4. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
5. The MC100ES6226 is fully operational up to 3.0 GHz and is characterized up to 2.7 GHz.
6. Propagation delay $\overline{OE}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
7. Propagation delay $\overline{OE}$ assertion to output enabled (active).

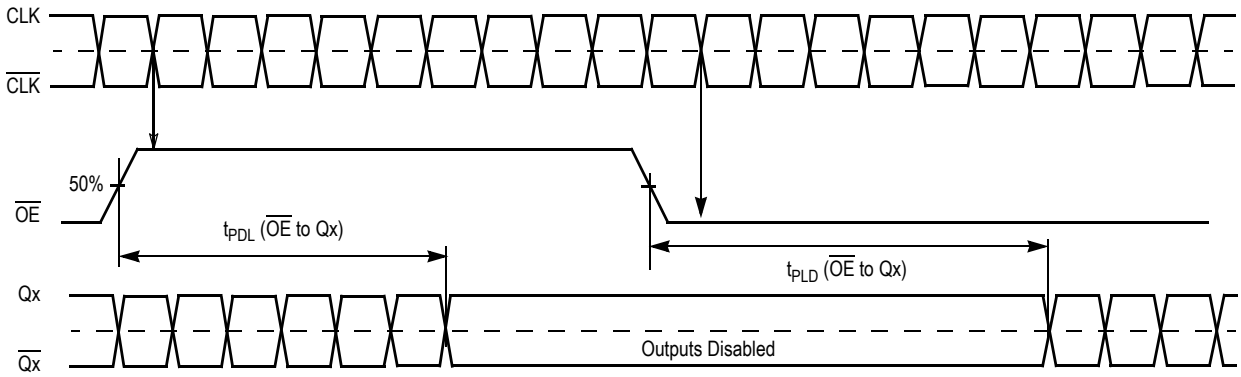


Figure 3. MC100ES6226 Output Disable/Enable Timing

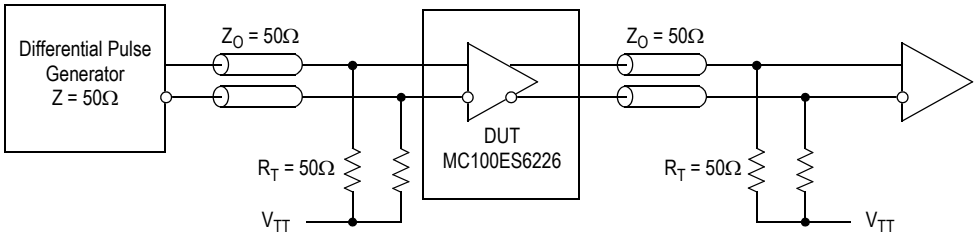


Figure 4. MC100ES6226 AC Test Reference

APPLICATIONS INFORMATION

Maintaining Lowest Device Skew

The MC100ES6226 guarantees low output-to-output bank skew of 35 ps and a part-to-part skew of max. TBD ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6226 is a mixed analog/digital product. The differential architecture of the MC100ES6226 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

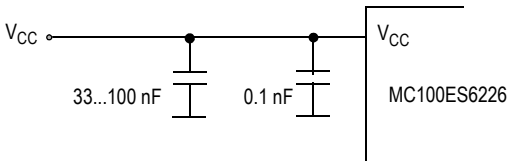


Figure 5. V_{CC} Power Supply Bypass

Order number: MC100ES6254
Rev 4, 08/2004

2.5/3.3 V Differential LVPECL 2x2 Clock Switch and Fanout Buffer

MC100ES6254

2.5/3.3 V DIFFERENTIAL LVPECL 2x2 CLOCK SWITCH AND FANOUT BUFFER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MC100ES6254 is a bipolar monolithic differential 2x2 clock switch and fanout buffer. Designed for most demanding clock distribution systems, the MC100ES6254 supports various applications that require to drive precisely aligned clock signals. The device is capable of driving and switching differential LVPECL signals. Using SiGe technology and a fully differential architecture, the device offers superior digital signal characteristics and very low clock skew error. Target applications for this clock driver are high performance clock/data switching, clock distribution or data loopback in computing, networking and telecommunication systems.

Features

- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Supports DC to 3GHz operation(1) of clock or data signals
- LVPECL compatible differential clock inputs and outputs
- LVCMOS compatible control inputs
- Single 3.3 V or 2.5 V supply
- 50 ps maximum device skew[1]
- Synchronous output enable eliminating output runt pulse generation and metastability
- Standard 32 lead LQFP package
- Industrial temperature range
- 32-lead Pb-free Package Available

Functional Description

MC100ES6254 is designed for very skew critical differential clock distribution systems and supports clock frequencies from DC up to 3.0 GHz. Typical applications for the MC100ES6254 are primary clock distribution, switching and loopback systems of high-performance computer, networking and telecommunication systems, as well as on-board clocking of OC-3, OC-12 and OC-48 speed communication systems. Primary purpose of the MC100ES6254 is high-speed clock switching applications. In addition, the MC100ES6254 can be configured as single 1:6 or dual 1:3 LVPECL fanout buffer for clock signals, or as loopback device in high-speed data applications.

The MC100ES6254 can be operated from a 3.3 V or 2.5 V positive supply without the requirement of a negative supply line.

1. The device is functional up to 3 GHz and characterized up to 2.7 GHz.

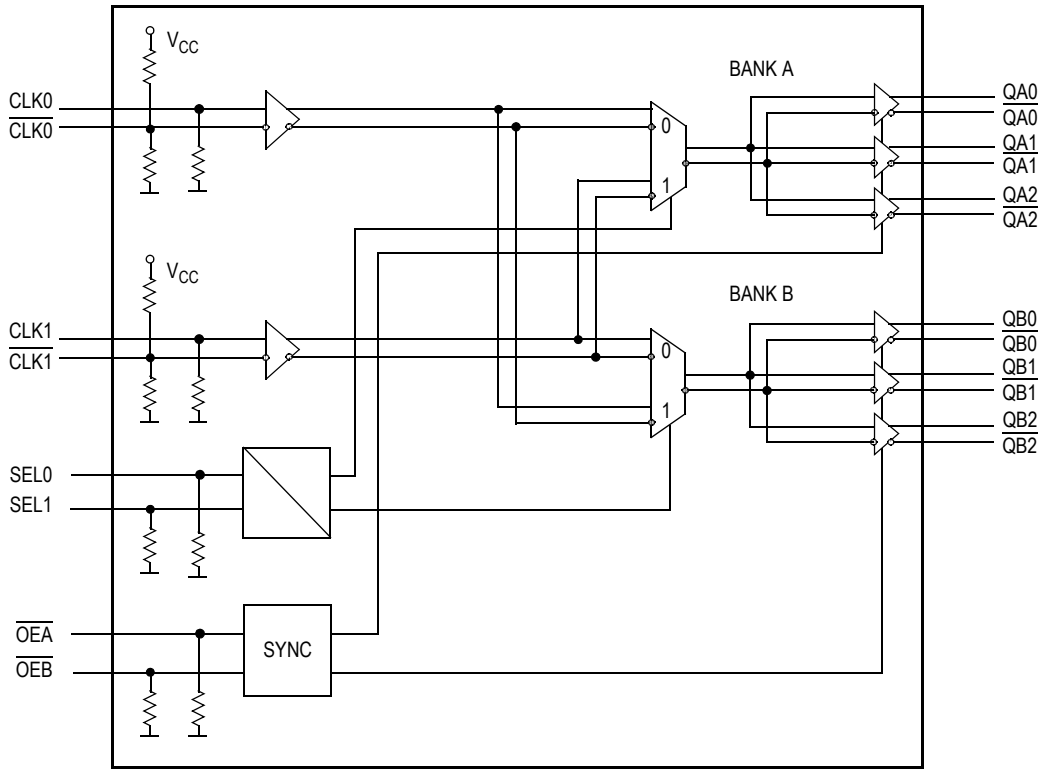


Figure 1. MC100ES6254 Logic Diagram

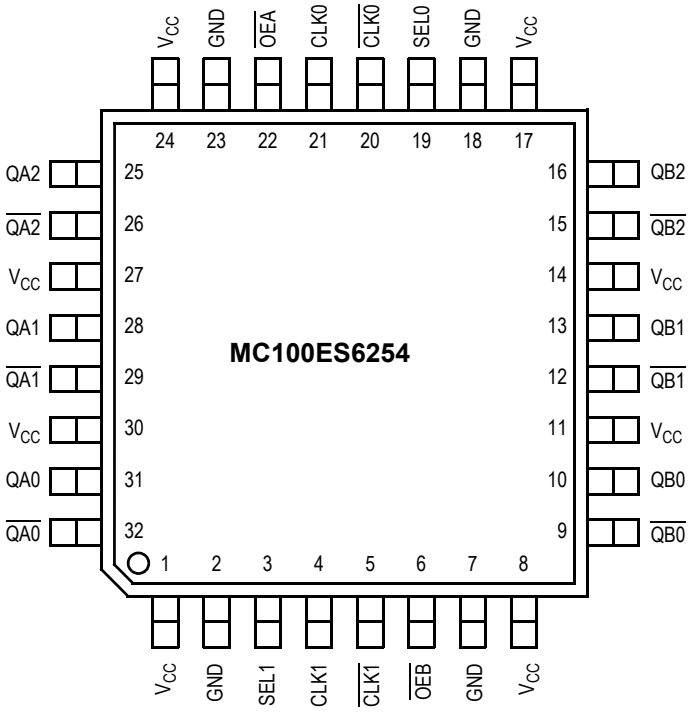


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLK0, $\overline{\text{CLK0}}$	Input	LVPECL	Differential reference clock signal input 0
CLK1, $\overline{\text{CLK1}}$	Input	LVPECL	Differential reference clock signal input 1
$\overline{\text{OEA}}$, $\overline{\text{OEB}}$	Input	LVCMOS	Output enable
SEL0, SEL1	Input	LVCMOS	Clock switch select
QA[0-2], $\overline{\text{QA[0-2]}}$ QB[0-2], $\overline{\text{QB[0-2]}}$	Output	LVPECL	Differential clock outputs (banks A and B)
GND	Supply	GND	Negative power supply
V_{CC}	Supply	VCC	Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation

Table 2. Function Table

Control	Default	0	1
$\overline{\text{OEA}}$	0	QA[0-2], $\overline{\text{Qx[0-2]}}$ are active. Deassertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses	QA[0-2] = L, $\overline{\text{QA[0-2]}}$ = H (outputs disabled). Assertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses
$\overline{\text{OEB}}$	0	QA[0-2], $\overline{\text{Qx[0-2]}}$ are active. Deassertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses	QA[0-2] = L, $\overline{\text{QA[0-2]}}$ = H (outputs disabled). Assertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses
SEL0, SEL1	00	Refer to Table 4	

Table 3. Clock Select Control

SEL0	SEL1	CLK0 Routed to	CLK1 Routed to	Application Mode
0	0	QA[0:2] and QB[0:2]	—	1:6 fanout of CLK0
0	1	—	QA[0:2] and QB[0:2]	1:6 fanout of CLK1
1	0	QA[0:2]	QB[0:2]	Dual 1:3 buffer
1	1	QB[0:2]	QA[0:2]	Dual 1:3 buffer (crossed)

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		V_{CC}–2[1]		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	1500			V	
LU	Latch-up immunity	200			mA	
C_{IN}			4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal resistance junction to case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
	Operating junction temperature[2] (continuous operation) MTBF = 9.1 years			110	°C	
T_{Func}	Functional temperature range	T_A = –40		T_J = +110	°C	

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this data sheet for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6254 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6254 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 6. DC Characteristics (V_{CC} = 3.3 V ± 5% or 2.5 V ± 5%, T_J = 0° to +110°C)

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs ($\overline{OEA}$, $\overline{OEB}$, SEL0, SEL1)						
V_{IL}	Input Voltage Low			0.8	V	
V_{IH}	Input Voltage High	2.0			V	
I_{IN}	Input Current[1]			±100	μA	V_{IN} = V_{CC} or V_{IN} = GND
-+ Clock Inputs (CLK0, $\overline{CLK0}$, CLK1, $\overline{CLK1}$)						
V_{PP}	AC differential input voltage[2]	0.1		1.3	V	Differential operation
V_{CMR}	Differential cross point voltage[3]	1.0		V_{CC}–0.3	V	Differential operation
LVPECL Clock Outputs (QA0–2, $\overline{QA0–2}$, QB0–2, $\overline{QB0–2}$)						
V_{OH}	Output High Voltage	V_{CC}–1.2	V_{CC}–1.005	V_{CC}–0.7	V	I_{OH} = –30 mA[4]
V_{OL}	Output Low Voltage V_{CC} = 3.3 V ±5% V_{CC} = 2.5 V ±5%	V_{CC}–1.9 V_{CC}–1.9	V_{CC}–1.705 V_{CC}–1.705	V_{CC}–1.5 V_{CC}–1.3	V	I_{OL} = –5 mA[5]
Supply Current						
I_{GND}	Maximum Quiescent Supply Current without output termination current		52	85	mA	GND pin

1. Inputs have internal pullup/pulldown resistors that affect the input current.
2. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristic.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. Equivalent to a termination 50 Ω to V_{TT}.
5. I_{CC} calculation: I_{CC} = (number of differential output pairs used) * (I_{OH} + I_{OL}) + I_{GND}
   I_{CC} = (number of differential output pairs used) * (V_{OH}-V_{TT})÷R_{load} +(V_{OL}-V_{TT})÷R_{load}) + I_{GND}

Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5% or 2.5 V ± 5%, T_J = 0° to +110°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{PP}	Differential Input Voltage[2] (peak-to-peak)	0.3		1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[3]	1.2		V_{CC}-0.3	V	
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak) f_O < 1.1 GHz f_O < 2.5 GHz f_O < 3.0 GHz	 0.45 0.35 0.20	 0.7 0.55 0.35		 V V V	
f_{CLK}	Input Frequency	0		3000[4]	MHz	
t_{PD}	Propagation Delay CLK, 1 to QA[] or QB[]	360	485	610	ps	Differential
$t_{sk(O)}$	Output-to-Output Skew			50	ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part)			250	ps	Differential
$t_{SK(P)}$	Output Pulse Skew[5]			60	ps	
DC_O	Output Duty Cycle t_{REF} < 100 MHz Output Duty Cycle t_{REF} < 800 MHz	49.4 45.2		50.6 54.8	% %	DC_{fref} = 50% DC_{fref} = 50%
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter (SEL0 ≠ SEL1)			TBD		
t_r, t_f	Output Rise/Fall Time	0.05		300	ps	20% to 80%
t_{PDL}[6]	Output Disable Time	2.5·T + t_{PD}		3.5·T + t_{PD}	ns	T = CLK period
t_{PLD}[7]	Output Enable Time	3·T + t_{PD}		4·T + t_{PD}	ns	T = CLK period

1. AC characteristics apply for parallel output termination of 50 Ω to V_{TT}.
2. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
3. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
4. The MC100ES6254 is fully operational up to 3.0 GHz and is characterized up to 2.7 GHz.
5. Output pulse skew is the absolute difference of the propagation delay times: $| t_{PLH} - t_{PHL} |$.
6. Propagation delay $\overline{OE}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
7. Propagation delay $\overline{OE}$ assertion to output enabled (active).

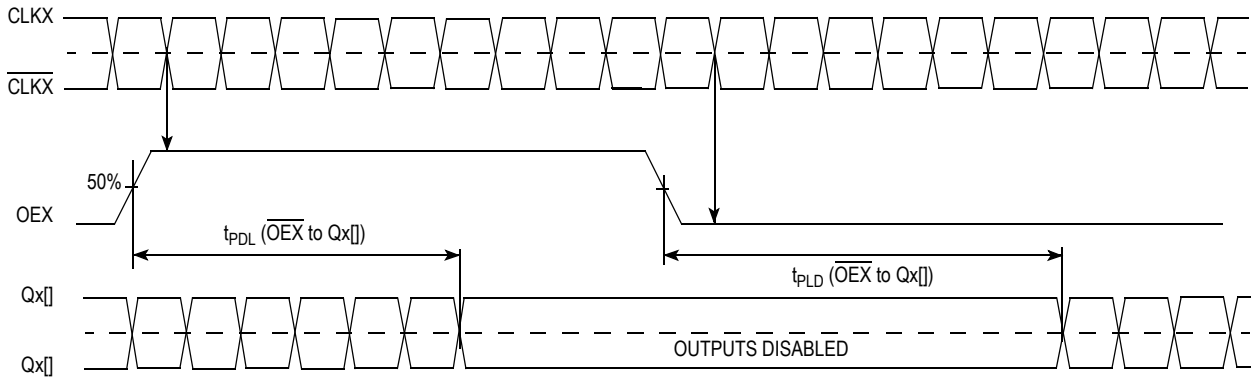


Figure 3. MC100ES6254 Output Disable/Enable Timing

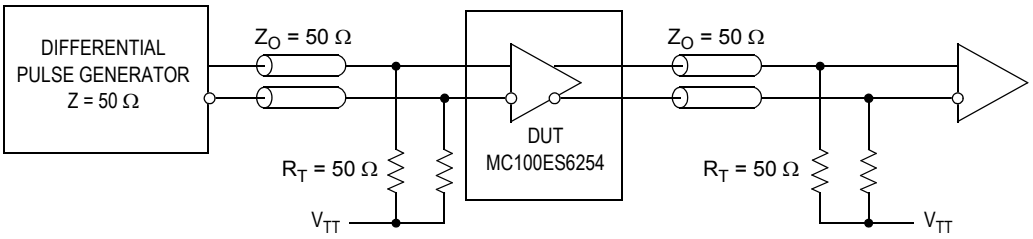
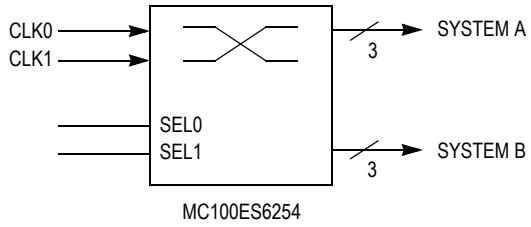


Figure 4. MC100ES6254 AC Test Reference

APPLICATIONS INFORMATION

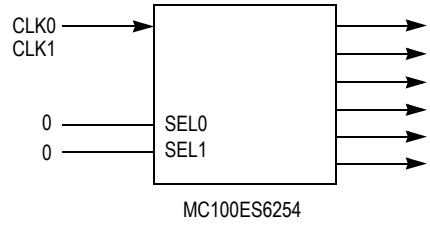
Example Configurations

2 x 2 CLOCK SWITCH

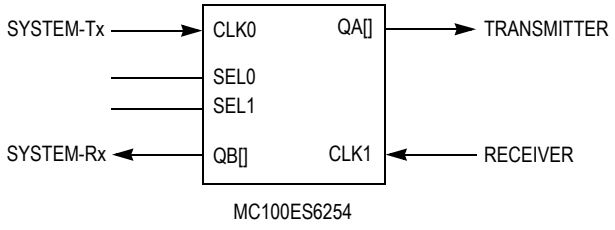


SEL0	SEL1	Switch Configuration
0	0	CLK0 clocks systems A and system B
0	1	CLK1 clocks system A and system B
1	0	CLK0 clocks system A and CLK1 clocks system B
1	1	CLK1 clocks system B and CLK1 clocks system A

1:6 CLOCK FANOUT BUFFER



LOOPBACK DEVICE



SEL0	SEL1	Switch Configuration
0	0	System loopback
0	1	Line loopback
1	0	Transmit/Receive operation
1	1	System and line loopback

Understanding the Junction Temperature Range of the MC100ES6254

To make the optimum use of high clock frequency and low skew capabilities of the MC100ES6254, the MC100ES6254 is specified, characterized and tested for the junction temperature range of T_J = 0°C to +110°C. Because the exact thermal performance depends on the PCB type, design, thermal management and natural or forced air convection, the junction temperature provides an exact way to correlate the application specific conditions to the published performance data of this data sheet. The correlation of the junction temperature range to the application ambient temperature range and vice versa can be done by calculation:

$$T_J = T_A + R_{thja} \cdot P_{tot}$$

Assuming a thermal resistance (junction to ambient) of 54.4°C/W (2s2p board, 200 ft/min airflow, refer to Table 8) and a typical power consumption of 467 mW (all outputs terminated 50 Ω to V_{TT}, V_{CC} = 3.3 V, frequency independent), the junction temperature of the MC100ES6254 is approximately T_A + 24.5°C, and the minimum ambient temperature in this example case calculates to –24.5°C (the maximum ambient temperature is 85.5°C, refer to Table 8). Exceeding the minimum junction temperature specification of the MC100ES6254 does not have a significant impact on the device functionality. However, the continuous use the MC100ES6254 at high ambient temperatures requires thermal management to not exceed the specified maximum junction temperature. Refer to the Application Note AN1545 for a power consumption calculation guideline.

Table 8. Ambient Temperature Range (P_{tot} = 467 mW)

R_{thja} (2s2p board)		$T_{A, min}$[1]	$T_{A, max}$
Natural Convection	59.0°C/W	–28°C	82°C
100 ft/min	54.4°C/W	–25°C	85°C
200 ft/min	52.5°C/W	–24.5°C	85.5°C
400 ft/min	50.4°C/W	–23.5°C	86.5°C
800 ft/min	47.8°C/W	–22°C	88°C

1. The MC100ES6254 device function is guaranteed from T_A = –40°C to T_J = 110°C

Maintaining Lowest Device Skew

The MC100ES6254 guarantees low output-to-output bank skew of 50 ps and a part-to-part skew of maximum 250 ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6254 is a mixed analog/digital product. The differential architecture of the MC100ES6254 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

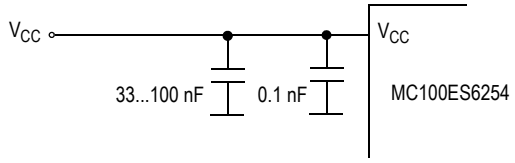


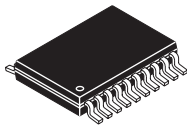
Figure 5. V_{CC} Power Supply Bypass

Order number: MC100ES6535
Rev 2, 05/2004

3.3 V LVCMOS-to-LVPECL 1:4 Fanout Buffer

MC100ES6535

The MC100ES6535 is a low skew, high performance 3.3 V 1-to-4 LVCMOS to LVPECL fanout buffer. The ES6535 has two selectable inputs that allow LVCMOS or LVTTL input levels which translate to LVPECL outputs. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin. The ES6535 is ideal for high performance clock distribution applications.



DT SUFFIX
20-LEAD TSSOP PACKAGE
CASE 948E-02

Features

- 4 differential LVPECL outputs
- 2 selectable LVCMOS/LVTTL inputs
- 1 GHz maximum output frequency
- Translates LVCMOS/LVTTL levels to LVPECL levels
- 30 ps maximum output skew
- 190 ps part-to-part skew
- 3.3 V operating range
- 20-lead TSSOP package
- Ambient temperature range –40°C to +85°C

ORDERING INFORMATION

Device	Package
MC100ES6535DT	TSSOP-20
MC100ES6535DTR2	TSSOP-20

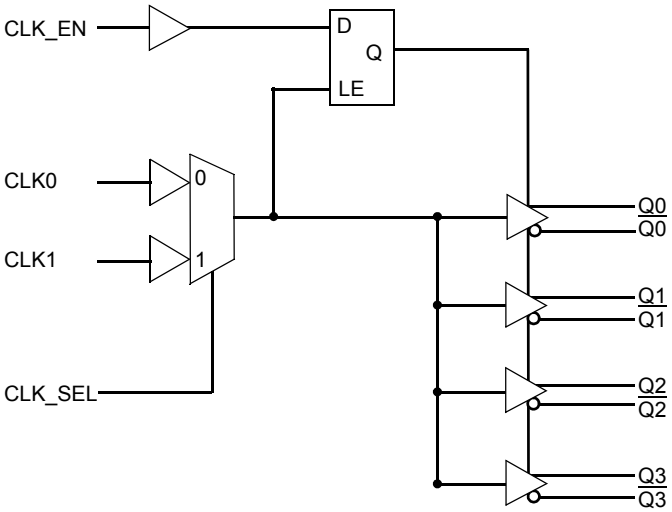


Figure 1. Logic Diagram

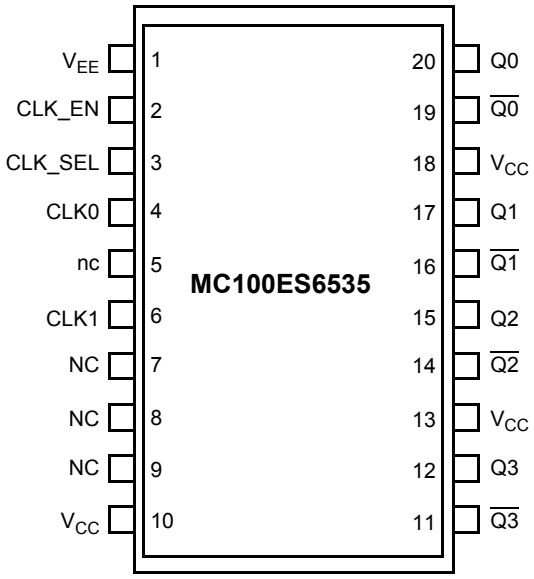


Figure 2. 20-Lead Pinout (Top View)

Table 1. Pin Description

Number	Name	Type		Description
1	V_{EE}	Power		Negative supply pin
2	CLK_EN	Input	Pullup[1]	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Q outputs are forced low, $\overline{Q}$ outputs are forced high. LVCMOS/LVTTL interface levels
3	CLK_SEL	Input	Pulldown[1]	Clock select input. When HIGH, selects CLK1 input. When LOW, selects CLK0 input. LVCMOS/LVTTL interface levels
4	CLK0	Input	Pulldown[1]	LVCMOS/LVTTL clock input
6	CLK1	Input	Pulldown[1]	LVCMOS/LVTTL clock input
5, 7, 8, 9	NC	Unused		No connect
10, 13, 18	V_{CC}	Power		Positive supply pin
11, 12	Q3, $\overline{Q3}$	Output		LVPECL differential output pair
14, 15	Q2, $\overline{Q2}$	Output		LVPECL differential output pair
16, 17	Q1, $\overline{Q1}$	Output		LVPECL differential output pair
19, 20	Q0, $\overline{Q0}$	Output		LVPECL differential output pair

1. Pullup and Pulldown refer to internal input resistors.

Table 2. Control Input Function Table[1]

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q0:Q3**	**$\overline{Q0}$:$\overline{Q3}$**
0	0	CLK0	Disabled; LOW	Disabled; HIGH
0	1	CLK1	Disabled; LOW	Disabled; HIGH
1	0	CLK0	Enabled	Enabled
1	1	CLK1	Enabled	Enabled

1. After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge. In the active mode, the state of the outputs are a function of the CLK0 and CLK1 inputs as described in Table 3.

Table 3. Clock Input Function Table

Inputs	Outputs	
CLK0 or CLK1	**Q0:Q3**	**$\overline{Q0}$:$\overline{Q3}$**
0	LOW	HIGH
1	HIGH	LOW

Table 4. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pullup Resistor		75 kΩ
ESD Protection	Human Body Model Machine Model	4000 V 200 V
θ_{JA} Thermal Resistance (Junction-to-Ambient)	0 LFPM, 20 TSSOP 500 LFPM, 20 TSSOP	140°C/W 100°C/W

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 5. Absolute Maximum Ratings[1]

Symbol	Rating	Conditions	Rating	Units
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6$ V	V_{CC} +0.3 V_{EE} –0.3	V V
I_{out}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{store}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 6. DC Characteristics (V_{CC} = 3.135 V to 3.8 V; V_{EE} = 0 V)

Symbol	Characteristic	–40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current			35			45	mA
V_{OH}[1]	Output HIGH Voltage	V_{CC}–1150	V_{CC}–1020	V_{CC}–800	V_{CC}–1200	V_{CC}–970	V_{CC}–750	mV
V_{OL}	Output LOW Voltage	V_{CC}–1950	V_{CC}–1620	V_{CC}–1250	V_{CC}–2000	V_{CC}–1680	V_{CC}–1300	mV

1. Outputs are terminated through a 50Ω resistor to V_{CC} –2 volts.

Table 7. LVTTL / LVCMOS Input DC Characteristics (V_{CC} = 3.135 V to 3.8 V)

Symbol	Characteristic	Condition	-40°C			0°C to 85°C			Unit
			Min	Typ	Max	Min	Typ	Max	
I_{IN}	Input Current	$V_{IN} = V_{CC}$			±150			±150	μA
V_{IK}	Input Clamp Voltage	I_{IN} = –18 mA			–1.2			–1.2	V
V_{IH}	Input HIGH Voltage		2.0		V_{CC} +0.3	2.0		V_{CC} +0.3	V
V_{IL}	Input LOW Voltage				0.8			0.8	V

Table 8. AC Characteristics (V_{CC} = 3.135 V to 3.8 V, V_{EE} = 0 V)

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Toggle Frequency			1			1			1	GHz
t_{PD}	Propagation Delay to Output Differential	150	350	500	175	360	550	200	380	600	ps
t_{SKEW}	Skew Output-to-Output		20	30		20	30		20	30	ps
	Part-to-Part			190			190			190	ps
t_{JITTER}	Cycle-to-Cycle JitterRMS (1σ)			1			1			1	ps
V_{outPP}	Output Peak-to-Peak Voltage	350	750		350	750		350	750		mV
t_r/t_f	Output Rise/Fall Time (20%−80% @ 50 MHz)	50		400	50		400	50		400	ps

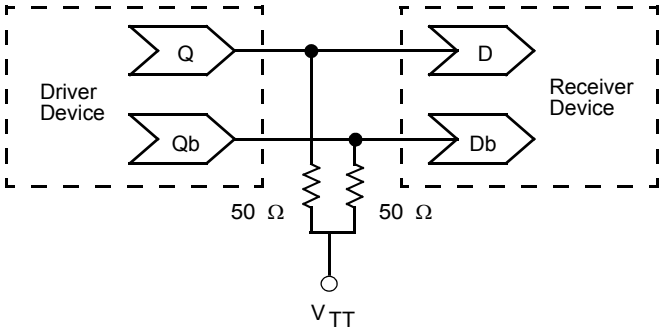


Figure 3. Typical Termination for Output Driver and Device Evaluation

Order number: MC100ES7011H
Rev 0, 05/2004

Product Preview

Low Voltage 1:2 Differential HSTL/LVDS-to-LVDS Clock Fanout Buffer

The MC100ES7011H is a low voltage 1:2 Differential HSTL/LVDS to LVDS clock fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES7011H supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are in high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:2 differential clock fanout buffer
- 50 ps maximum device skew
- SiGe Technology
- Supports DC to 1000 MHz operation
- LVDS compatible differential clock outputs
- HSTL/LVDS compatible differential clock inputs
- 3.3V power supply
- Supports industrial temperature range
- Standard 8 lead SOIC package

MC100ES7011H

1:2 DIFFERENTIAL HSTL/LVDS TO LVDS CLOCK FANOUT DRIVER

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-06

ORDERING INFORMATION

Device	Package
MC100ES7011HD	SO-8
MC100ES7011HDR2	SO-8

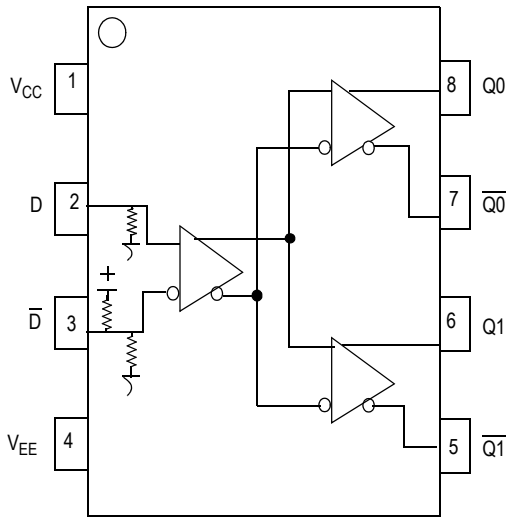


Figure 1. 8-Lead Pinout (Top View) **and Logic Diagram**

PIN DESCRIPTION

Pin	Function
D, $\overline{D}$	HSTL/LVDS Data Inputs
Qn, $\overline{Qn}$	LVDS Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table 1. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		TBD
Internal Input Pullup Resistor		TBD
ESD Protection	Human Body Model Machine Model	TBD
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	TBD

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 2. Absolute Maximum Ratings[1]

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6V$	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics (V_{CC} = 3.3V±5%; T_J = 0°C to 110°C)[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL/LVDS differential input signals (D, $\overline{D}$)						
V_{DIF}	Differential input voltage[2]	0.2			V	
$V_{X, IN}$	Differential cross point voltage[3]	0.25	0.68 – 0.9	V_{CC} – 1.3	V	
V_{IH}	Input high voltage	V_X + 0.1			V	
V_{IL}	Input low voltage			V_X – 0.1	V	
I_{IN}	Input current			±150	mA	$V_{IN} = V_X \pm 0.1V$
LVDS clock outputs (Q[0:4], $\overline{Q[0:4]}$)						
V_{PP}	Output differential voltage (peak-to-peak)	250			mV	LVDS
V_{OS}	Output offset voltage	1125		1275	mV	LVDS
Supply Current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{CC} pin (core)

1. DC characteristics are design targets and pending characterization.
2. V_{DIF} (DC) is the minimum differential HSTL/LVDS input voltage swing required for device functionality.
3. V_X (DC) is the crosspoint of the differential HSTL/LVDS input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. AC Characteristics (V_{CC} = 3.3V±5%; T_J = 0°C to 110°C)[1] [2]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL/LVDS differential input signals (D, $\overline{D}$)						
V_{DIF}	Differential input voltage (peak-to-peak)[3]	0.4			V	
$V_{X, IN}$	Differential cross point voltage[4]	0.68		1.275	V	
f_{CLK}	Input Frequency		1000	TBD	MHz	Differential
t_{PD}	Propagation Delay D to Q[0:1}			TBD	ps	Differential
LVDS clock outputs (Q[0:1], $\overline{Q[0:1]}$)						
$t_{SK(O)}$	Output-to-output skew			50	ps	Differential
$t_{SK(PP)}$	Output-to-output skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output cycle-to-cycle jitter			TBD		
DC_O	Output duty cycle	TBD	50	TBD	%	DC_{fref} = 50%
t_r / t_f	Output Rise/Fall Times	0.05		TBD	ns	20% to 80%

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to $V_{TT.}$
3. V_{DIF} (AC) is the minimum differential HSTL/LVDS input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
4. V_X (AC) is the crosspoint of the differential HSTL/LVDS input signal. Functional operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF} (AC) impacts the device propagation delay, device and part-to-part skew.

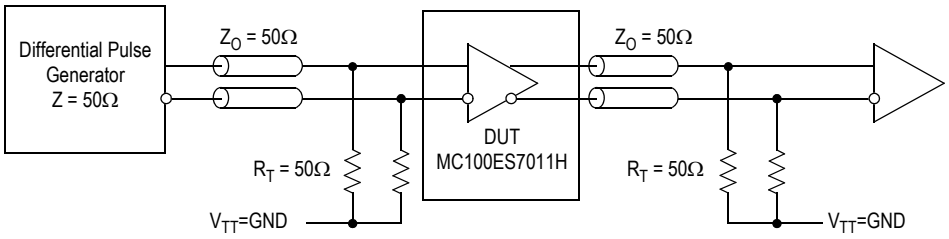


Figure 2. MC100ES7011H AC Test Reference

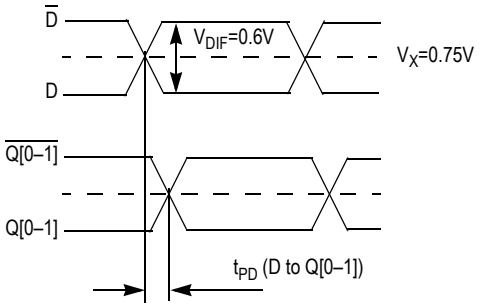


Figure 3. MC100ES7011H AC Reference Measurement Waveform (HSTL Input)

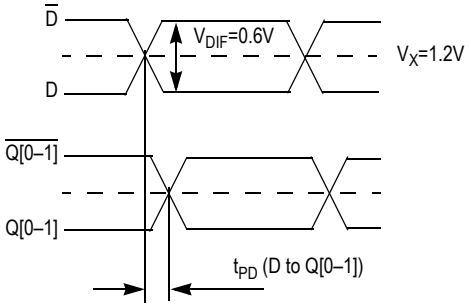


Figure 4. MC100ES7011H AC Reference Measurement Waveform (LVDS Input)

Order number: MC100ES7011P
Rev 0, 05/2004

Product Preview

Low Voltage 1:2 Differential PECL Clock Fanout Buffer

The MC100ES7011P is a low voltage 1:2 Differential PECL to LVDS clock fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES7011P supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are in high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:2 differential clock fanout buffer
- 50 ps maximum device skew
- SiGe Technology
- Supports DC to 1000 MHz operation
- LVDS compatible differential clock outputs
- PECL compatible differential clock inputs
- 3.3V power supply
- Supports industrial temperature range
- Standard 8 lead SOIC package

MC100ES7011P

1:2 DIFFERENTIAL PECL TO LVDS CLOCK FANOUT DRIVER

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-06

ORDERING INFORMATION

Device	Package
MC100ES7011PD	SO-8
MC100ES7011PDR2	SO-8

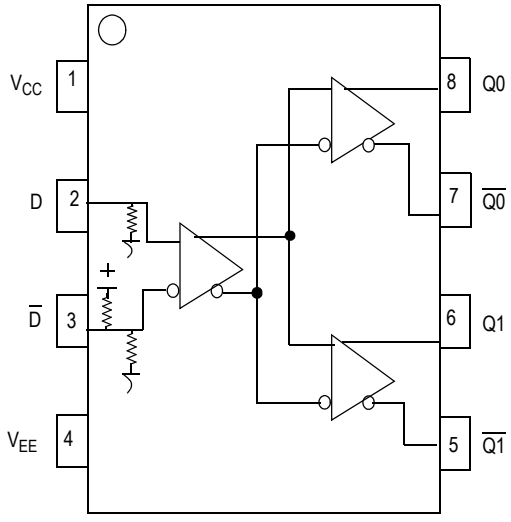


Figure 1. 8-Lead Pinout (Top View) **and Logic Diagram**

PIN DESCRIPTION

Pin	Function
D, $\overline{D}$	ECL Data Inputs
Qn, $\overline{Qn}$	LVDS Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table 1. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		TBD
Internal Input Pullup Resistor		TBD
ESD Protection	Human Body Model Machine Model	TBD
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	TBD

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 2. Absolute Maximum Ratings[1]

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6V$	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics (V_{CC} = 3.3V±5%; T_J = 0°C to 110°C)[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
PECL differential input signals (D, $\overline{D}$)						
V_{PP}	Differential Input Voltage[2]	0.15		1.0	V	Differential Operation
V_{CMR}	Differential Cross Point Voltage[3]	1.0		V_{CC} – 0.6	V	Differential Operation
V_{IH}	Input High Voltage	V_{CC} – 1.165		V_{CC} – 0.880	V	
V_{IL}	Input Low Voltage	V_{CC} – 1.810		V_{CC} – 1.475	V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_{IH}$ or V_{IN}
LVDS clock outputs (Q[0:1], $\overline{Q[0:1]}$)						
V_{PP}	Output Differential Voltage (peak-to-peak)	250			mV	LVDS
V_{OS}	Output Offset Voltage	1125		1275	mV	LVDS
Supply Current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{CC} pin (core)

1. DC characteristics are design targets and pending characterization.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. AC Characteristics (V_{CC} = 3.3V±5%; T_J = 0°C to 110°C)[1] [2]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
PECL differential input signals (D, $\overline{D}$)						
V_{PP}	Differential Input Voltage (peak-to-peak)[3]	0.2		1.0	V	
V_{CMR}	Differential Cross Point Voltage[4]	1		V_{CC} - 0.6	V	
f_{CLK}	Input Frequency		1000		MHz	Differential
t_{PD}	Propagation Delay D to Q[0:1]			TBD	ps	Differential
LVDS clock outputs (Q[0:1], $\overline{Q[0:1]}$)						
$t_{SK(O)}$	Output-to-Output Skew			50	ps	Differential
$t_{SK(PP)}$	Output-to-Output Skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			TBD		
DC_O	Output Duty Cycle	TBD	50	TBD	%	DC_{fref} = 50%
t_r / t_f	Output Rise/Fall Times	0.05		TBD	ns	20% to 80%

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to $V_{TT.}$
3. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
4. V_{CMR} (AC) is the crosspoint of the differential PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP}(AC) impacts the device propagation delay, device and part-to-part skew.

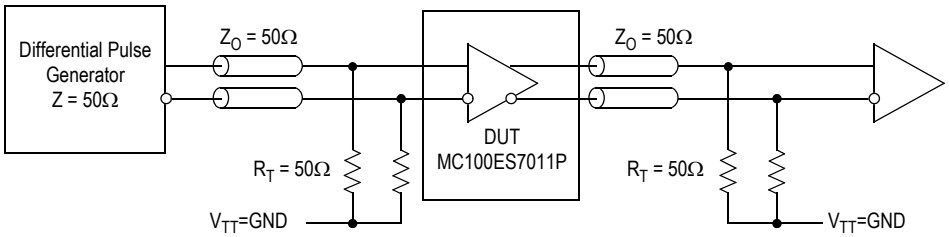


Figure 2. MC100ES7011P AC Test Reference

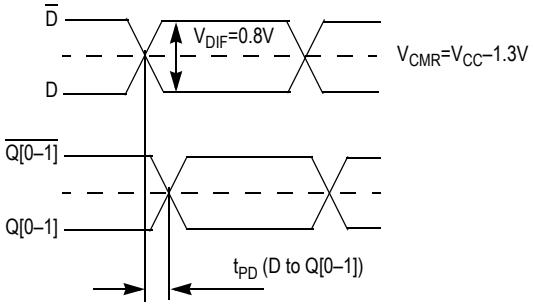


Figure 3. MC100ES7011P AC Reference Measurement Waveform (PECL Input)

Order number: MC100ES7014
Rev 1, 05/2004

Product Preview

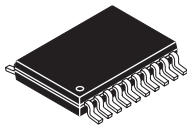
Low Voltage 1:5 Differential LVDS Clock Fanout Buffer

MC100ES7014

1:5 DIFFERENTIAL LVDS CLOCK FANOUT DRIVER

The MC100ES7014 is a LVDS differential clock fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES7014 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are in high performance clock distribution in computing, networking and telecommunication systems.

The MC100ES7014 is designed for low skew clock distribution systems and supports clock frequencies up to 1000MHz. The device accepts two clock sources. The CLK0 input accepts LVDS or HSTL compatible signals and CLK1 accepts PECL compatible signals. The selected input signal is distributed to 5 identical, differential LVDS compatible outputs.



DT SUFFIX
20-LEAD TSSOP PACKAGE
CASE 948E-02

Features

- 1:5 differential clock fanout buffer
- 50 ps maximum device skew
- SiGe Technology
- Supports DC to 1000 MHz operation
- LVDS compatible differential clock outputs
- PECL and HSTL/LVDS compatible differential clock inputs
- 3.3V power supply
- Supports industrial temperature range
- Standard 20 lead TSSOP package

ORDERING INFORMATION

Device	Package
MC100ES7014DT	TSSOP-20
MC100ES7014DTR2	TSSOP-20

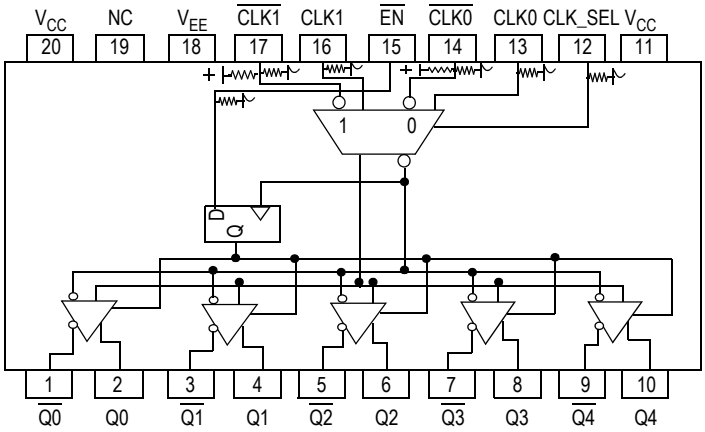


Figure 1. 20-Lead Pinout (Top View) **and Logic Diagram**

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table 1. Pin Description

Pin	Function
CLK0, $\overline{\text{CLK0}}$	HSTL/LVDS Data Inputs
CLK1, $\overline{\text{CLK1}}$	PECL Data Inputs
Q[0:4], $\overline{\text{Q[0:4]}}$	LVDS Data Outputs
CLK_SEL	LVCMOS Active Clock Select Input
$\overline{\text{EN}}$	LVCMOS Sync Enable
V_{CC}	Positive Supply
V_{EE}	Negative Supply
nc	no connect

Table 2. Function Table

Control	Default	0	1
CLK_SEL	0	CLK0, $\overline{\text{CLK0}}$ (HSTL/LVDS) is the active differential clock input	CLK1, $\overline{\text{CLK1}}$ (PECL) is the active differential clock input
$\overline{\text{EN}}$	0	Q[0:4], $\overline{\text{Q[0:4]}}$ are active. Deassertion of $\overline{\text{EN}}$ can be asynchronous to the reference clock without generation of output runt pulses.	Q[0:4] = L, $\overline{\text{Q[0:4]}}$ = H (outputs disabled). Assertion of $\overline{\text{EN}}$ can be asynchronous to the reference clock without generation of output runt pulses.

Table 3. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		TBD
Internal Input Pullup Resistor		TBD
ESD Protection	Human Body Model Machine Model	TBD
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	TBD

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Absolute Maximum Ratings[1]

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6V$	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3V±5%; T_J = 0°C to 110°C)[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL/LVDS differential input signals (CLK0, $\overline{CLK0}$)						
V_{DIF}	Differential Input Voltage[2]	0.2			V	
$V_{X, IN}$	Differential Cross Point Voltage[3]	0.25	0.68 – 0.9	V_{CC} – 1.3	V	
V_{IH}	Input High Voltage	V_X + 0.1			V	
V_{IL}	Input Low Voltage			V_X – 0.1	V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_X$ ± 0.1V
PECL differential input signals (CLK1, $\overline{CLK1}$)						
V_{PP}	Differential input Voltage[4]	0.15		1.0	V	Differential Operation
V_{CMR}	Differential Cross Point Voltage[5]	1.0		V_{CC} – 0.6	V	Differential Operation
V_{IH}	Input High Voltage	V_{CC} – 1.165		V_{CC} – 0.880	V	
V_{IL}	Input Low Voltage	V_{CC} – 1.810		V_{CC} – 1.475	V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_{IH}$ or V_{IN}
LVCMOS control inputs $\overline{EN}$, CLK_SEL						
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_{IH}$ or V_{IN}
LVDS clock outputs (Q[0:4], $\overline{Q[0:4]}$)						
V_{PP}	Output Differential Voltage (peak-to-peak)	250			mV	LVDS
V_{OS}	Output Offset Voltage	1125		1275	mV	LVDS
Supply Current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{CC} pin (core)

1. DC characteristics are design targets and pending characterization.
2. V_{DIF} (DC) is the minimum differential HSTL/LVDS input voltage swing required for device functionality.
3. V_X (DC) is the crosspoint of the differential HSTL/LVDS input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
5. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics (V_{CC} = 3.3V±5%; T_J = 0°C to 110°C)[1] [2]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL/LVDS differential input signals (CLK0, $\overline{CLK0}$)						
V_{DIF}	Differential Input Voltage (peak-to-peak)[3]	0.4			V	
$V_{X, IN}$	Differential Cross Point Voltage[4]	0.68		1.275	V	
f_{CLK}	Input Frequency		1000	TBD	MHz	Differential
t_{PD}	Propagation Delay			TBD	ps	Differential
PECL differential input signals (CLK1, $\overline{CLK1}$)						
V_{PP}	Differential Input Voltage (peak-to-peak)[5]	0.2		1.0	V	
V_{CMR}	Differential Cross Point Voltage[6]	1		V_{CC} – 0.6	V	
f_{CLK}	Input Frequency		1000		MHz	Differential
t_{PD}	Propagation Delay			TBD	ps	Differential
LVDS clock outputs (Q[0:4], $\overline{Q[0:4]}$)						
$t_{SK(O)}$	Output-to-Output Skew			50	ps	Differential
$t_{SK(PP)}$	Output-to-Output Skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			TBD		
DC_O	Output Duty Cycle	TBD	50	TBD	%	DC_{fref} = 50%
t_r / t_f	Output Rise/Fall Times	0.05		TBD	ns	20% to 80%
t_{PDL}	Output Disable Time[7]	2.5*T +t_{PD}		3.5*T +t_{PD}	ns	T = CLK period
t_{PLD}	Output Enable Time[8]	3*T +t_{PD}		4*T +t_{PD}	ns	T = CLK period

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. V_{DIF} (AC) is the minimum differential HSTL/LVDS input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
4. V_X (AC) is the crosspoint of the differential HSTL/LVDS input signal. Functional operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF}(AC) impacts the device propagation delay, device and part-to-part skew.
5. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
6. V_{CMR} (AC) is the crosspoint of the differential PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP}(AC) impacts the device propagation delay, device and part-to-part skew.
7. Propagation delay $\overline{EN}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
8. Propagation delay $\overline{EN}$ assertion to output enabled (active).

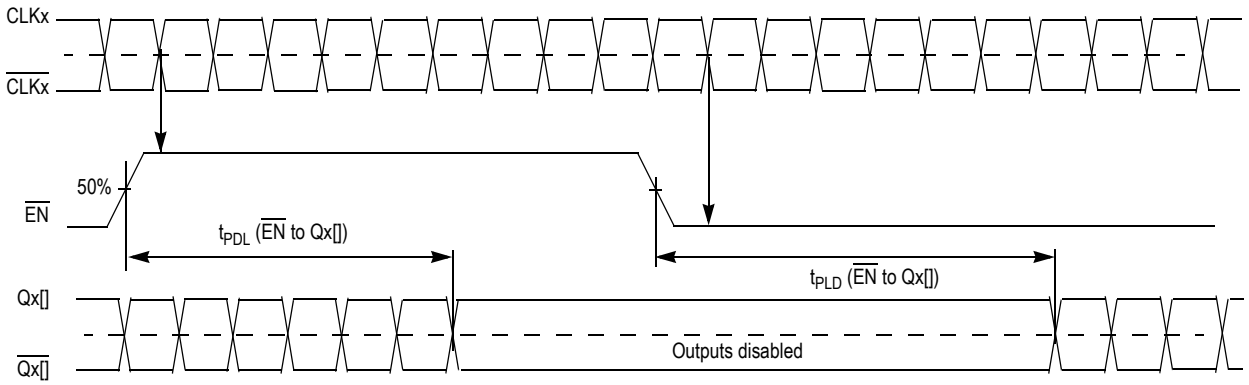


Figure 2. MC100ES7014 AC Test Reference

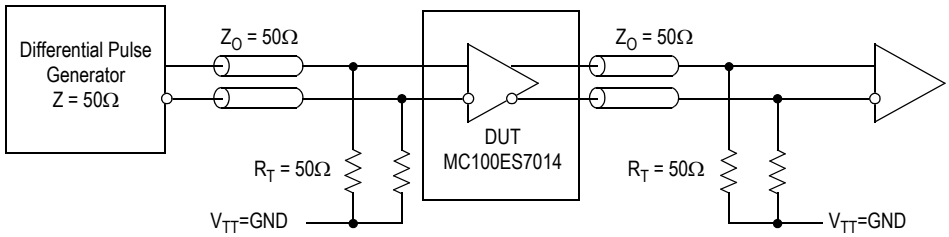


Figure 3. MC100ES7014 AC Test Reference

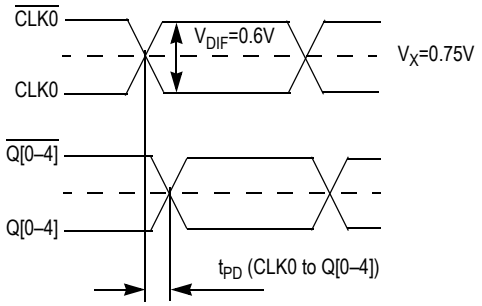


Figure 4. MC100ES7014 AC Reference Measurement Waveform (HSTL Input)

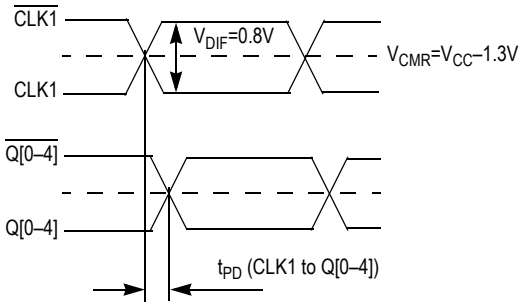


Figure 5. MC100ES7014 AC Reference Measurement Waveform (PECL Input)

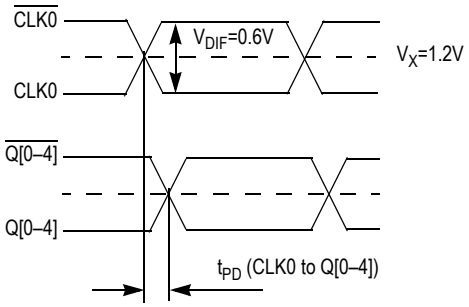


Figure 6. MC100ES7014 AC Reference Measurement Waveform (LVDS Input)

Order number: MC100ES7111
Rev 0, 12/2002

Preliminary Information

Low Voltage 1:10 Differential LVDS Clock Fanout Buffer

MC100ES7111

LOW VOLTAGE
1:10 DIFFERENTIAL
LVDS CLOCK
FANOUT DRIVER

FA SUFFIX
32-LEAD TQFP PACKAGE
CASE 873A-03

The MC100ES7111 is a LVDS differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES7111 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:10 differential clock fanout buffer
- 50 ps maximum device skew[1]
- SiGe technology
- Supports DC to 1000 MHz operation[(1)] of clock or data signals
- LVDS compatible differential clock outputs
- PECL and HSTL/LVDS compatible differential clock inputs
- 3.3V power supply
- Supports industrial temperature range
- Standard 32-lead LQFP package

Functional Description

The MC100ES7111 is designed for low skew clock distribution systems and supports clock frequencies up to 1000 MHz[1]. The device accepts two clock sources. The CLK0 input accepts LVDS or HSTL compatible signals and CLK1 accepts PECL compatible signals. The selected input signal is distributed to 10 identical, differential LVDS compatible outputs.

The output enable control is synchronized internally preventing output runt pulse generation. Outputs are only disabled or enabled when the outputs are already in logic low state (true outputs logic low, inverted outputs logic high). The internal synchronizer eliminates the setup and hold time requirements for the external clock enable signal. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

1. AC specifications are design targets and subject to change

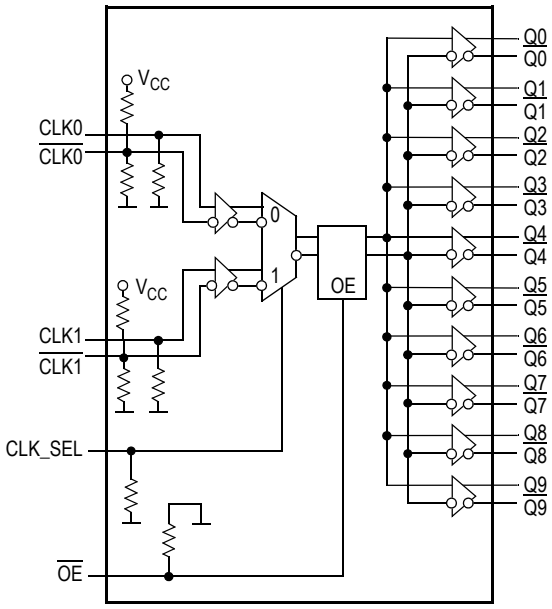


Figure 1. MC100ES7111 Logic Diagram

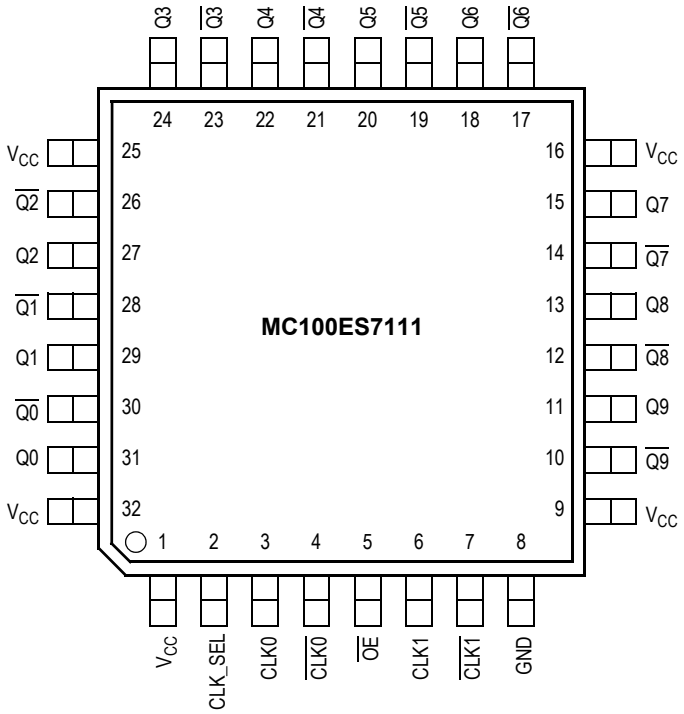


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLK0, $\overline{\text{CLK0}}$	Input	HSTL/LVDS	Differential HSTL or LVDS reference clock signal input
CLK1, $\overline{\text{CLK1}}$	Input	PECL	Differential PECL reference clock signal input
CLK_SEL	Input	LVCMOS	Reference clock input select
OE	Input	LVCMOS	Output enable/disable. OE is synchronous to the input reference clock which eliminates possible output runt pulses when the OE state is changed.
Q[0–9], $\overline{\text{Q[0–9]}}$	Output	LVDS	Differential clock outputs
GND	Supply		Negative power supply
V_{CC}	Supply		Positive power supply of the device (3.3V)

Table 2. Function Table

Control	Default	0	1
CLK_SEL	0	CLK0, $\overline{\text{CLK0}}$ (HSTL/LVDS) is the active differential clock input	CLK1, $\overline{\text{CLK1}}$ (PECL) is the active differential clock input
$\overline{\text{OE}}$	0	Q[0-9], $\overline{\text{Q[0-9]}}$ are active. Deassertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses.	Q[0-9] = L, $\overline{\text{Q[0-9]}}$ =H (outputs disabled). Assertion of OE can be asynchronous to the reference clock without generation of output runt pulses.

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.9	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	
T_{Func}	Functional Temperature Range	T_A = –40	T_J = +110	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	TBD			V	
LU	Latch-up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T_J	Operating Junction Temperature[1] (continuous operation) MTBF = 9.1 years			110	°C	

1. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this data sheet for more information). The device AC and DC parameters are specified up to 110×C junction temperature allowing the MC100ES7111 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES7111 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. DC Characteristics (V_{CC} = 3.3V ± 5%, T_J = 0°C to +110°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock Input Pair CLK0, $\overline{CLK0}$ (HSTL/LVDS differential signals)						
V_{DIF}	Differential Input Voltage[2]	0.2			V	
$V_{X, IN}$	Differential Cross Point Voltage[3]	0.25	0.68 - 0.9	V_{CC}–1.3	V	
V_{IH}	Input High Voltage	V_X+0.1			V	
V_{IL}	Input Low Voltage			V_X-0.1	V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_X \pm 0.1V$
Clock input pair CLK1, $\overline{CLK1}$ (PECL differential signals)						
V_{PP}	Differential Input Voltage[4]	0.15		1.0	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[5]	1.0		V_{CC}–0.6	V	Differential operation
V_{IH}	Input Voltage High	V_{CC}–1.165		V_{CC}–0.880	V	
V_{IL}	Input Voltage Low	V_{CC}–1.810		V_{CC}–1.475	V	
I_{IN}	Input Current[1]			±150	mA	$V_{IN} = V_{IH}$ or V_{IN}
LVCMOS Control Inputs $\overline{OE}$, CLK_SEL						
V_{IL}	Input Voltage Low			0.8	V	
V_{IH}	Input Voltage High	2.0			V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_{IH}$ or V_{IN}
LVDS clock outputs (Q[0-9], $\overline{Q[0-9]}$)						
V_{PP}	Output Differential Voltage (peak-to-peak)	250			mV	LVDS
V_{OS}	Output Offset Voltage	1125		1275	mV	LVDS
Supply current						
I_{CC}	Maximum Quiescent Supply Current without Output Termination Current		TBD	TBD	mA	V_{CC} pin (core)

1. DC characteristics are design targets and pending characterization.
2. V_{DIF} (DC) is the minimum differential HSTL/LVDS input voltage swing required for device functionality.
3. V_X (DC) is the crosspoint of the differential HSTL/LVDS input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
5. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%, T_J = 0°C to 110°C)[1] [2]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$ (HSTL/LVDS differential signals)						
V_{DIF}	Differential Input Voltage[3] (peak-to-peak)	0.4			V	
$V_{X, IN}$	Differential Cross Point Voltage[4]	0.68		1.275	V	
f_{CLK}	Input Frequency		1000	TBD	MHz	
t_{PD}	Propagation Delay CLK0 to Q[0-9]			TBD	ps	
Clock input pair CLK1, $\overline{CLK1}$ (PECL differential signals)						
V_{PP}	Differential Input Voltage[5] (peak-to-peak)	0.2		1.0	V	
V_{CMR}	Differential Input Cross Point Voltage[6]	1		V_{CC}-0.6	V	
f_{CLK}	Input Frequency		1000		MHz	Differential
t_{PD}	Propagation Delay CLK1 to Q[0-9]			TBD	ps	Differential
LVDS clock outputs (Q[0-9], $\overline{Q[0-9]}$)						
$t_{sk(O)}$	Output-to-Output Skew			50	ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			TBD		
DC_O	Output Duty Cycle	TBD	50	TBD	%	DC_{fref} = 50%
t_r, t_f	Output Rise/Fall Time	0.05		TBD	ns	20% to 80%
t_{PDL}[7]	Output Disable Time	2.5·T + t_{PD}		3.5·T + t_{PD}	ns	T = CLK period
t_{PLD}[8]	Output Enable Time	3·T + t_{PD}		4·T + t_{PD}	ns	T = CLK period

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. V_{DIF} (DC) is the minimum differential HSTL/LVDS input voltage swing required for device functionality.
4. V_X (DC) is the crosspoint of the differential HSTL/LVDS input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{DIF} (DC) specification.
5. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
6. V_{CMR} (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
7. Propagation delay $\overline{OE}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
8. Propagation delay $\overline{OE}$ assertion to output enabled (active).

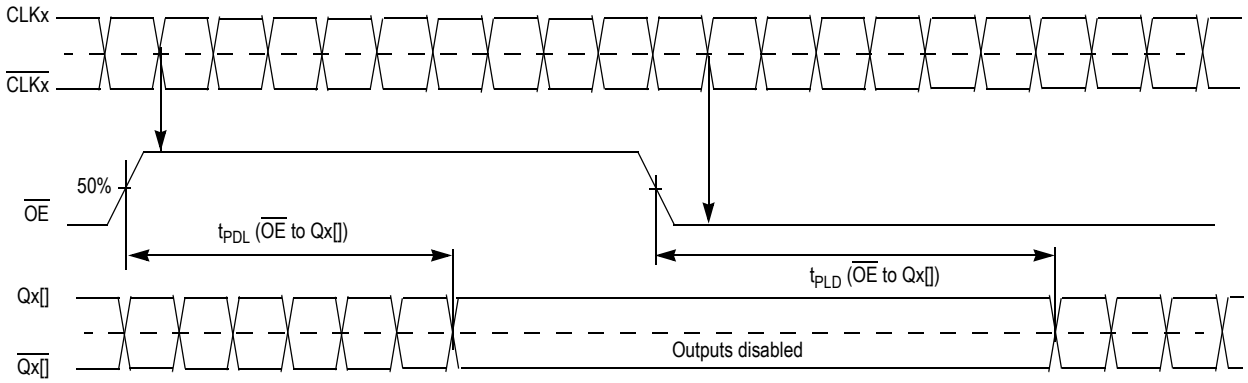


Figure 3. MC100ES7111 AC Test Reference

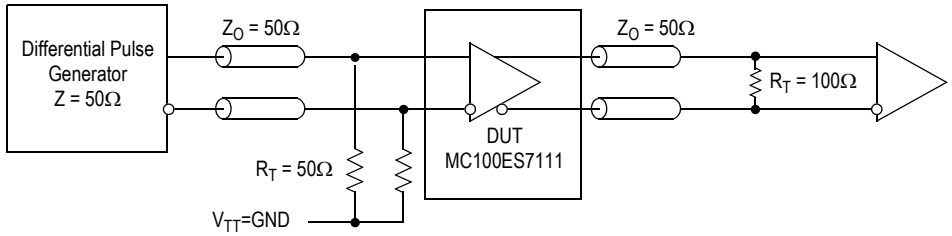


Figure 4. MC100ES7111 AC Test Reference

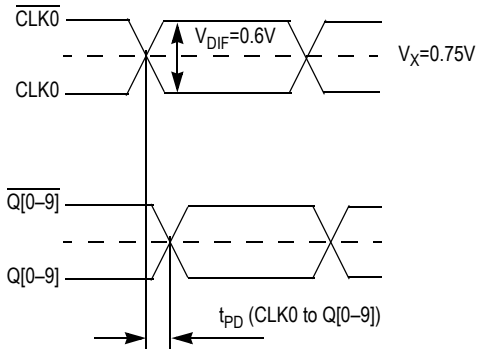


Figure 5. MC100ES7111 AC Reference Measurement Waveform (HSTL Input)

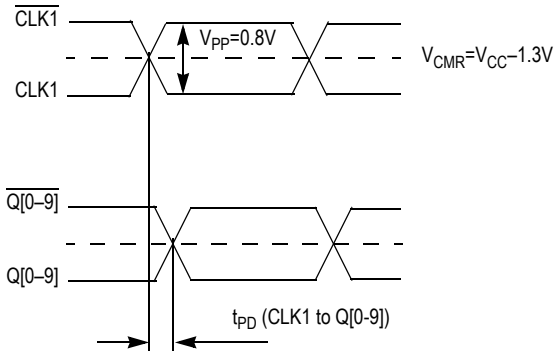


Figure 6. MC100ES7111 AC Reference Measurement Waveform (PECL Input)

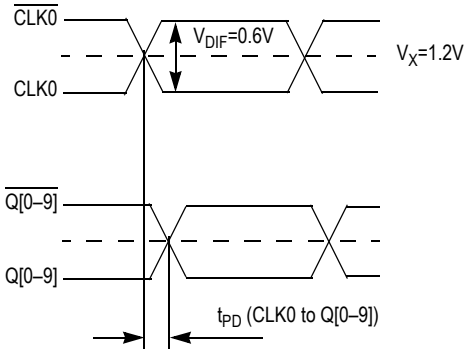


Figure 7. MC100ES7111 AC Reference Measurement Waveform (LVDS Input)

Order number: MC100ES8011H
Rev 0, 05/2004

Product Preview

Low Voltage 1:2 Differential HSTL Clock Fanout Buffer

The MC100ES8011H is a low voltage 1:2 Differential HSTL fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES8011H supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are in high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:2 differential clock fanout buffer
- 50 ps maximum device skew
- SiGe Technology
- Supports DC to 400 MHz operation
- HSTL compatible differential clock outputs
- HSTL compatible differential clock inputs
- 3.3V power supply
- Supports industrial temperature range
- Standard 8 lead SOIC package

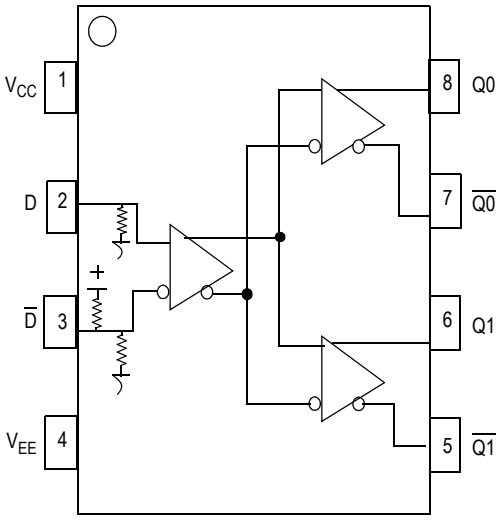


Figure 1. 8-Lead Pinout (Top View) **and Logic Diagram**

MC100ES8011H

1:2 DIFFERENTIAL HSTL CLOCK FANOUT DRIVER

D SUFFIX
8 LEAD SOIC PACKAGE
CASE 751-06

ORDERING INFORMATION

Device	Package
MC100ES8011HD	SO-8
MC100ES8011HDR2	SO-8

PIN DESCRIPTION

Pin	Function
D, $\overline{D}$	HSTL Data Inputs
Qn, $\overline{Qn}$	HSTL Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table 1. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		TBD
Internal Input Pullup Resistor		TBD
ESD Protection	Human Body Model Machine Model	TBD
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	TBD

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 2. Absolute Maximum Ratings[1]

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6V$	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics (V_{CC} = 3.3 V ± 5%; T_J = 0°C to 110°C)[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL differential input signals (D, $\overline{D}$)						
V_{DIF}	Differential Input Voltage[2]	0.2			V	
$V_{X, IN}$	Differential Cross Point Voltage[3]	0.25	0.68 – 0.9	V_{CC} – 1.3	V	
V_{IH}	Input High Voltage	V_X + 0.1			V	
V_{IL}	Input Low Voltage			V_X – 0.1	V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_X$ ± 0.1V
HSTL clock outputs (Q[0:1], $\overline{Q[0:1]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Ouput Low Voltage			0.4	V	
Supply Current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{CC} pin (core)

1. DC characteristics are design targets and pending characterization.
2. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
3. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. AC Characteristics (V_{CC} = 3.3 V ± 5%; T_J = 0°C to 110°C)[1] [2]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL differential input signals (D, $\overline{D}$)						
V_{DIF}	Differential Input Voltage (peak-to-peak)[3]	0.4			V	
$V_{X, IN}$	Differential Cross Point Voltage[4]	0.68		0.9	V	
f_{CLK}	Input Frequency		0 – 400	TBD	MHz	Differential
t_{PD}	Propagation Delay D to Q[0:1}			TBD	ps	Differential
HSTL clock outputs (Q[0:1], $\overline{Q[0:1]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Ouput Low Voltage			0.5	V	
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak)	0.5			V	
$t_{SK(O)}$	Output-to-Output Skew			50	ps	Differential
$t_{SK(PP)}$	Output-to-Output Skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			TBD		
DC_O	Output Duty Cycle	TBD	50	TBD	%	DC_{fref} = 50%
t_r / t_f	Output Rise/Fall Times	0.05		TBD	ns	20% to 80%

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including t_{PD} and device-to-device skew.
4. V_X (AC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF} (AC) impacts the device propagation delay, device and part-to-part skew.

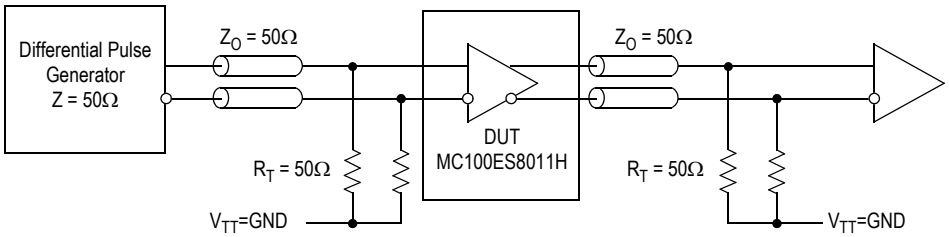


Figure 2. MC100ES8011H AC Test Reference

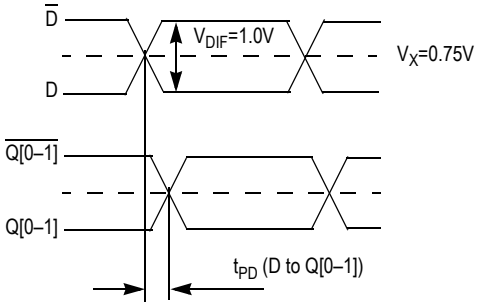


Figure 3. MC100ES8011H AC Reference Measurement Waveform (HSTL Input)

Order number: MC100ES8011P
Rev 0, 05/2004

Product Preview

Low Voltage 1:2 Differential PECL-to-HSTL Clock Fanout Buffer

The MC100ES8011P is a low voltage 1:2 Differential PECL-to-HSTL clock fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES8011P supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are in high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:2 differential clock fanout buffer
- 50 ps maximum device skew
- SiGe Technology
- Supports DC to 400 MHz operation
- HSTL compatible differential clock outputs
- PECL compatible differential clock inputs
- 3.3V power supply
- Supports industrial temperature range
- Standard 8 lead SOIC package

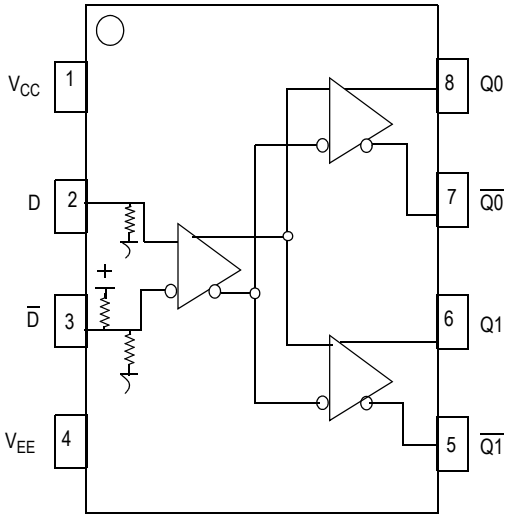


Figure 1. 8-Lead Pinout (Top View) **and Logic Diagram**

MC100ES8011P

1:2 DIFFERENTIAL PECL TO HSTL CLOCK FANOUT DRIVER

D SUFFIX
8-LEAD SOIC PACKAGE
CASE 751-06

ORDERING INFORMATION

Device	Package
MC100ES8011PD	SO-8
MC100ES8011PDR2	SO-8

PIN DESCRIPTION

Pin	Function
D, $\overline{D}$	ECL Data Inputs
Qn, $\overline{Qn}$	LVDS Data Outputs
V_{CC}	Positive Supply
V_{EE}	Negative Supply

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table 1. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		TBD
Internal Input Pullup Resistor		TBD
ESD Protection	Human Body Model Machine Model	TBD
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	TBD

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 2. Absolute Maximum Ratings[1]

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6V$	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 3. DC Characteristics (V_{CC} = 3.3 V ± 5%; T_J = 0°C to 110°C)[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
PECL differential input signals (D, $\overline{D}$)						
V_{PP}	Differential Input Voltage[2]	0.15		1.0	V	Differential Operation
V_{CMR}	Differential Cross Point Voltage[3]	1.0		V_{CC} – 0.6	V	Differential Operation
V_{IH}	Input High Voltage	V_{CC} – 1.165		V_{CC} – 0.880	V	
V_{IL}	Input Low Voltage	V_{CC} – 1.810		V_{CC} – 1.475	V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_{IH}$ or V_{IN}
HSTL clock outputs (Q[0:1], $\overline{Q[0:1]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Ouput Low Voltage			0.4	V	
Supply Current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{CC} pin (core)

1. DC characteristics are design targets and pending characterization.
2. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
3. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 4. AC Characteristics (V_{CC} = 3.3 V ± 5%; T_J = 0°C to 110°C)[1] [2]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
PECL differential input signals (D, $\overline{D}$)						
V_{PP}	Differential Input Voltage (peak-to-peak)[3]	0.2		1.0	V	
V_{CMR}	Differential Cross Point Voltage[4]	1		V_{CC} – 0.6	V	
f_{CLK}	Input Frequency		0 – 400		MHz	Differential
t_{PD}	Propagation Delay D to Q[0:1]			TBD	ps	Differential
HSTL clock outputs (Q[0:1], $\overline{Q[0:1]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Ouput Low Voltage			0.5	V	
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak)	0.5			V	
$t_{SK(O)}$	Output-to-Output Skew			50	ps	Differential
$t_{SK(PP)}$	Output-to-Output Skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			TBD		
DC_O	Output Duty Cycle	TBD	50	TBD	%	DC_{fref} = 50%
t_r / t_f	Output Rise/Fall Times	0.05		TBD	ns	20% to 80%
t_{PDL}	Output Disable Time[5]	2.5*T +t_{PD}		3.5*T +t_{PD}	ns	T = CLK period
t_{PLD}	Output Enable Time[6]	3*T +t_{PD}		4*T +t_{PD}	ns	T = CLK period

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
4. V_{CMR} (AC) is the crosspoint of the differential PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP}(AC) impacts the device propagation delay, device and part-to-part skew.
5. Propagation delay $\overline{EN}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
6. Propagation delay $\overline{EN}$ assertion to output enabled (active).

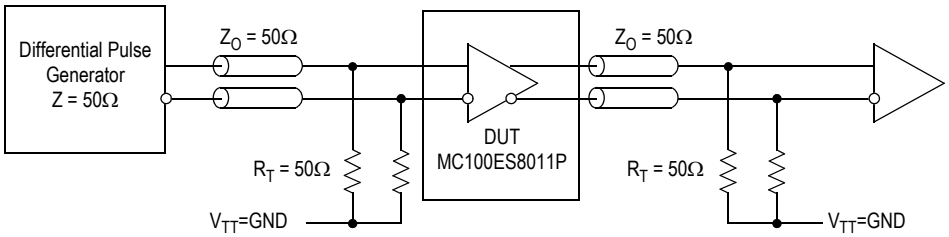


Figure 2. MC100ES8011P AC Test Reference

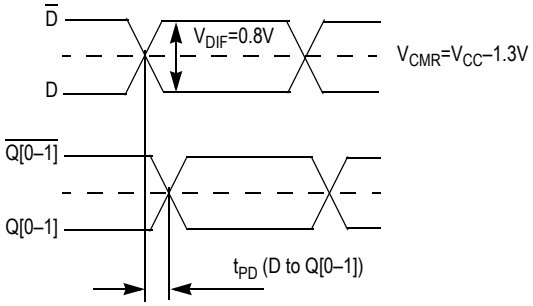


Figure 3. MC100ES8011P AC Reference Measurement Waveform (PECL Input)

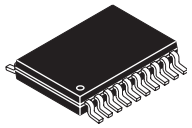
Order number: MC100ES8014
Rev 0, 05/2004

Product Preview

Low Voltage 1:5 Differential LVDS Clock Fanout Buffer

MC100ES8014

1:5 DIFFERENTIAL HSTL CLOCK FANOUT DRIVER



DT SUFFIX
20-LEAD TSSOP PACKAGE
CASE 948E-02

The MC100ES8014 is a HSTL differential clock fanout buffer. Designed for the most demanding clock distribution systems, the MC100ES8014 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are in high performance clock distribution in computing, networking and telecommunication systems.

The MC100ES8014 is designed for low skew clock distribution systems and supports clock frequencies up to 400MHz. The device accepts two clock sources. The CLK0 input accepts HSTL compatible signals and CLK1 accepts PECL compatible signals. The selected input signal is distributed to 5 identical, differential HSTL compatible outputs.

Features

- 1:5 differential clock fanout buffer
- 50 ps maximum device skew
- SiGe Technology
- Supports DC to 400 MHz operation
- 1.5V HSTL compatible differential clock outputs
- PECL and HSTL compatible differential clock inputs
- 3.3V power supply for device core, 1.5V or 1.8V HSTL output supply
- Supports industrial temperature range
- Standard 20 lead TSSOP package

ORDERING INFORMATION

Device	Package
MC100ES8014DT	TSSOP-20
MC100ES8014DTR2	TSSOP-20

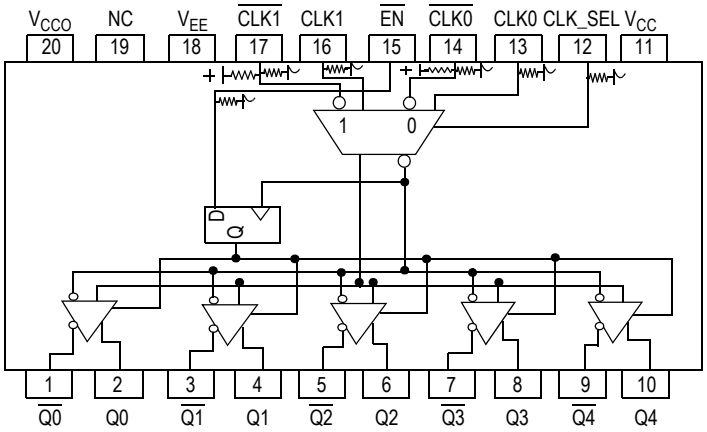


Figure 1. 20-Lead Pinout (Top View) **and Logic Diagram**

This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

Table 1. Pin Description

Pin	Function
CLK0, $\overline{\text{CLK0}}$	HSTL Data Inputs
CLK1, $\overline{\text{CLK1}}$	PECL Data Inputs
Q[0:4], $\overline{\text{Q[0:4]}}$	HSTL Data Outputs
CLK_SEL	LVCMOS Active Clock Select Input
$\overline{\text{EN}}$	LVCMOS Sync Enable
V_{CC}	Positive Supply of device core (3.3V)
V_{CCO}	Positive power supply of the HSTL outputs. All VCCO pins must be connected to the positive power supply (1.5V or 1.8V) for correct DC and AC operation.
V_{EE}	Negative Supply
nc	no connect

Table 2. Function Table

Control	Default	0	1
CLK_SEL	0	CLK0, $\overline{\text{CLK0}}$ (HSTL) is the active differential clock input	CLK1, $\overline{\text{CLK1}}$ (PECL) is the active differential clock input
$\overline{\text{EN}}$	0	Q[0:4], $\overline{\text{Q[0:4]}}$ are active. Deassertion of $\overline{\text{EN}}$ can be asynchronous to the reference clock without generation of output runt pulses.	Q[0:4] = L, $\overline{\text{Q[0:4]}}$ = H (outputs disabled). Assertion of $\overline{\text{EN}}$ can be asynchronous to the reference clock without generation of output runt pulses.

Table 3. General Specifications

Characteristics		Value
Internal Input Pulldown Resistor		TBD
Internal Input Pullup Resistor		TBD
ESD Protection	Human Body Model Machine Model	TBD
θ_{JA} Thermal Resistance (Junction to Ambient)	0 LFPM, 8 SOIC 500 LFPM, 8 SOIC	TBD

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Absolute Maximum Ratings[1]

Symbol	Parameter	Conditions	Rating	Unit
V_{SUPPLY}	Power Supply Voltage	Difference between V_{CC} & V_{EE}	3.9	V
V_{IN}	Input Voltage	$V_{CC} - V_{EE} \leq 3.6V$	V_{CC} + 0.3 V_{EE} – 0.3	V V
I_{OUT}	Output Current	Continuous Surge	50 100	mA mA
T_A	Operating Temperature Range		–40 to +85	°C
T_{STG}	Storage Temperature Range		–65 to +150	°C

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. DC Characteristics (V_{CC} = 3.3 V ± 5%; T_J = 0°C to 110°C)[1]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL differential input signals (CLK0, $\overline{CLK0}$)						
V_{DIF}	Differential Input Voltage[2]	0.2			V	
$V_{X, IN}$	Differential Cross Point Voltage[3]	0.25	0.68 – 0.9	V_{CC} – 1.3	V	
V_{IH}	Input High Voltage	V_X + 0.1			V	
V_{IL}	Input Low Voltage			V_X – 0.1	V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_X$ ± 0.1V
PECL differential input signals (CLK1, $\overline{CLK1}$)						
V_{PP}	Differential Input Voltage[4]	0.15		1.0	V	Differential Operation
V_{CMR}	Differential Cross Point Voltage[5]	1.0		V_{CC} – 0.6	V	Differential Operation
V_{IH}	Input High Voltage	V_{CC} – 1.165		V_{CC} – 0.880	V	
V_{IL}	Input Low Voltage	V_{CC} – 1.810		V_{CC} – 1.475	V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_{IH}$ or V_{IN}
LVCMOS control inputs $\overline{EN}$, CLK_SEL						
V_{IL}	Input Low Voltage			0.8	V	
V_{IH}	Input High Voltage	2.0			V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_{IH}$ or V_{IN}
HSTL clock outputs (Q[0:4], $\overline{Q[0:4]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Ouput Low Voltage			0.4	V	
Supply Current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		TBD	TBD	mA	V_{CC} pin (core)
I_{CCO}	Maximum Quiescent Supply Current, outputs terminated 50Ω to V_{TT}		TBD	TBD	mA	V_{CCO} pin (outputs)

1. DC characteristics are design targets and pending characterization.
2. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
3. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
5. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics (V_{CC} = 3.3 V ± 5%; T_J = 0°C to 110°C)[1] [2]

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
HSTL/LVDS differential input signals (CLK0, $\overline{CLK0}$)						
V_{DIF}	Differential Input Voltage (peak-to-peak)[3]	0.4			V	
$V_{X, IN}$	Differential Cross Point Voltage[4]	0.68		0.9	V	
f_{CLK}	Input Frequency		0 – 400	TBD	MHz	Differential
t_{PD}	Propagation Delay			TBD	ps	Differential
PECL differential input signals (CLK1, $\overline{CLK1}$)						
V_{PP}	Differential Input Voltage (peak-to-peak)[5]	0.2		1.0	V	
V_{CMR}	Differential Cross Point Voltage[6]	1		V_{CC} – 0.6	V	
f_{CLK}	Input Frequency		0 – 400		MHz	Differential
t_{PD}	Propagation Delay			TBD	ps	Differential
HSTL clock outputs (Q[0:4], $\overline{Q[0:4]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Ouput Low Voltage			0.5	V	
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak)	0.5			V	
$t_{SK(O)}$	Output-to-Output Skew			50	ps	Differential
$t_{SK(PP)}$	Output-to-Output Skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			TBD		
DC_O	Output Duty Cycle	TBD	50	TBD	%	DC_{fref} = 50%
t_r / t_f	Output Rise/Fall Times	0.05		TBD	ns	20% to 80%
t_{PDL}	Output Disable Time[7]	2.5*T +t_{PD}		3.5*T +t_{PD}	ns	T = CLK period
t_{PLD}	Output Enable Time[8]	3*T +t_{PD}		4*T +t_{PD}	ns	T = CLK period

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. V_{DIF} (AC) is the minimum differential HSTL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
4. V_X (AC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (AC) range and the input swing lies within the V_{DIF} (AC) specification. Violation of V_X (AC) or V_{DIF}(AC) impacts the device propagation delay, device and part-to-part skew.
5. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
6. V_{CMR} (AC) is the crosspoint of the differential PECL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP}(AC) impacts the device propagation delay, device and part-to-part skew.
7. Propagation delay $\overline{EN}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
8. Propagation delay $\overline{EN}$ assertion to output enabled (active).

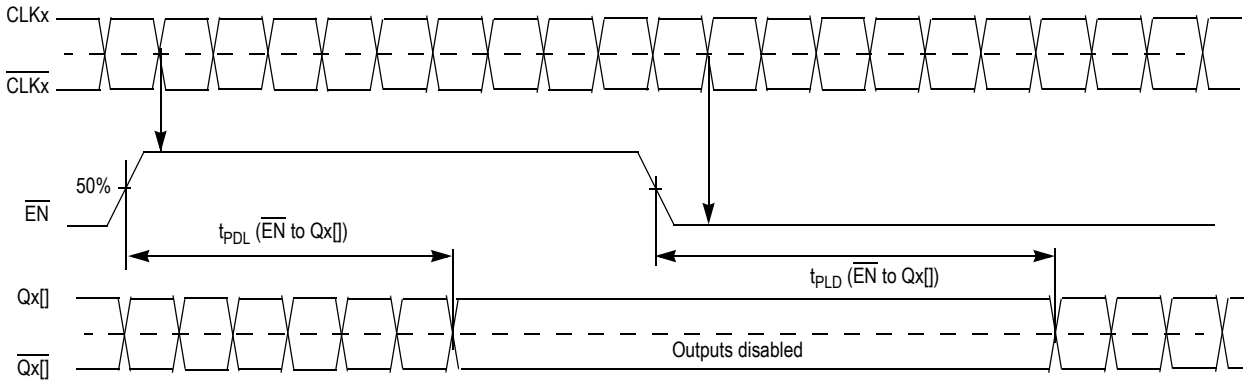


Figure 2. MC100ES8014 AC Test Reference

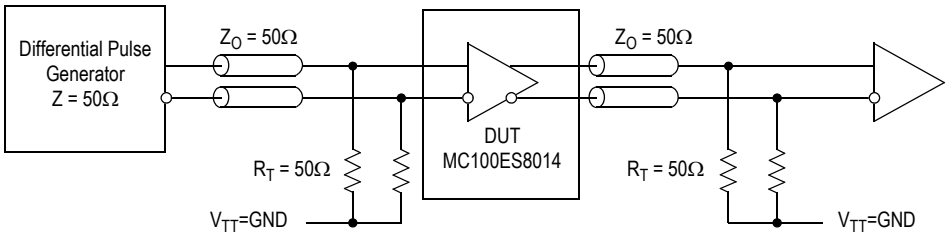


Figure 3. MC100ES8014 AC Test Reference

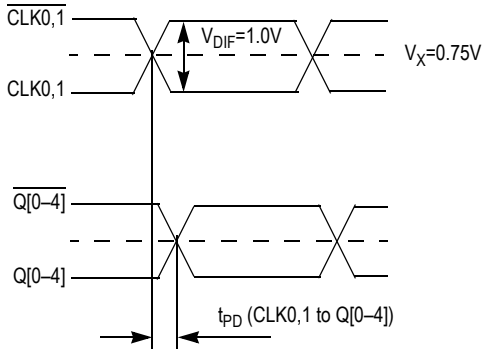


Figure 4. MC100ES8014 AC Reference Measurement Waveform (HSTL Input)

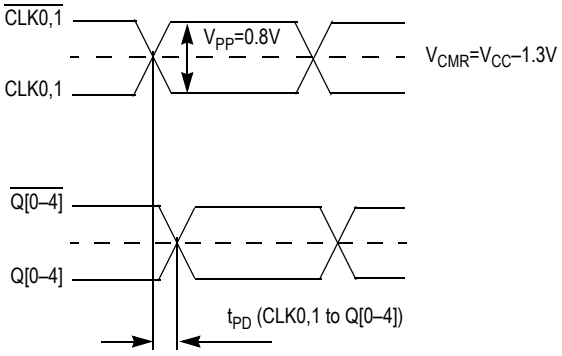


Figure 5. MC100ES8014 AC Reference Measurement Waveform (PECL Input)

Order number: MC100ES8111
Rev 1, 08/2004

Preliminary Information

Low Voltage 1:10 Differential HSTL Clock Fanout Buffer

MC100ES8111

LOW-VOLTAGE 1:10 DIFFERENTIAL HSTL CLOCK FANOUT DRIVER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MC100ES8111 is a bipolar monolithic differential clock fanout buffer. Designed for most demanding clock distribution systems, the MC100ES8111 supports various applications that require the distribution of precisely aligned differential clock signals. Using SiGe technology and a fully differential architecture, the device offers very low skew outputs and superior digital signal characteristics. Target applications for this clock driver are high performance clock distribution in computing, networking and telecommunication systems.

Features

- 1:10 differential clock fanout buffer
- 50 ps maximum device skew[1]
- SiGe technology
- Supports DC to 400 MHz operation[1] of clock or data signals
- 1.5V HSTL compatible differential clock outputs
- PECL and HSTL compatible differential clock inputs
- 3.3V power supply for device core, 1.5V or 1.8V HSTL output supply
- Supports industrial temperature range
- Standard 32 lead LQFP package

Functional Description

The MC100ES8111 is designed for low skew clock distribution systems and supports clock frequencies up to 400 MHz[1]. The device accepts two clock sources. The CLK0 input accepts HSTL compatible signals and CLK1 accepts PECL compatible signals. The selected input signal is distributed to 10 identical, differential HSTL compatible outputs.

In order to meet the tight skew specification of the device, both outputs of a differential output pair should be terminated, even if only one output is used. In the case where not all 10 outputs are used, the output pairs on the same package side as the parts being used on that side should be terminated.

The HSTL compatible output levels are generated with an open emitter architecture. This minimizes part-to-part and output-to-output skew. The open-emitter outputs require a 50Ω DC termination to GND (0 V). The output supply voltage can be either 1.5 V or 1.8 V, the core voltage supply is 3.3 V. The output enable control is synchronized internally preventing output runt pulse generation. Outputs are only disabled or enabled when the outputs are already in logic low state (true outputs logic low, inverted outputs logic high). The internal synchronizer eliminates the setup and hold time requirements for the external clock enable signal. The device is packaged in a 7x7 mm^2 32-lead LQFP package.

1. AC specifications are design targets and subject to change

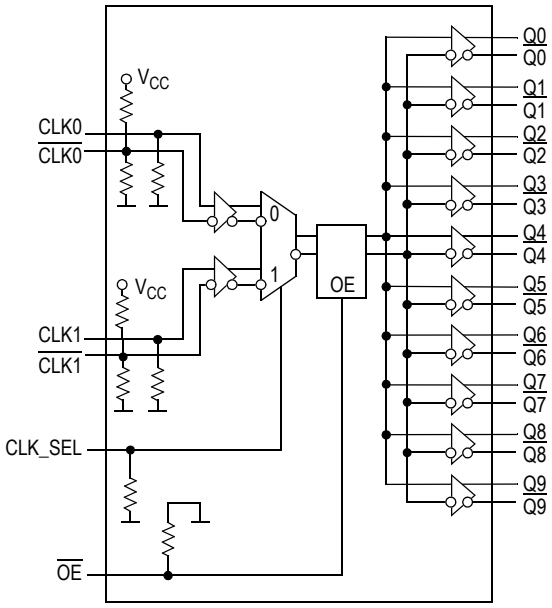


Figure 1. MC100ES8111 Logic Diagram

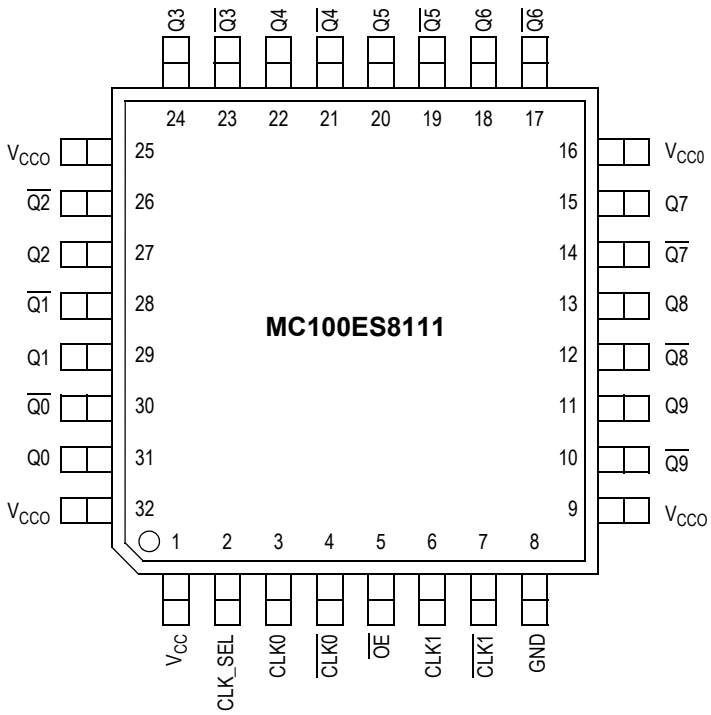


Figure 2. 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLK0, $\overline{\text{CLK0}}$	Input	HSTL	Differential HSTL reference clock signal input
CLK1, $\overline{\text{CLK1}}$	Input	PECL	Differential PECL reference clock signal input
CLK_SEL	Input	LVCMOS	Reference clock input select
OE	Input	LVCMOS	Output enable/disable. OE is synchronous to the input reference clock which eliminates possible output runt pulses when the OE state is changed.
Q[0-9], $\overline{\text{Q[0-9]}}$	Output	HSTL	Differential clock outputs
GND	Supply		Negative power supply
V_{CC}	Supply		Positive power supply of the device core (3.3V)
V_{CCO}	Supply		Positive power supply of the HSTL outputs. All V_{CCO} pins must be connected to the positive power supply (1.5 V or 1.8 V) for correct DC and AC operation.

Table 2. Function Table

Control	Default	0	1
CLK_SEL	0	CLK0, $\overline{\text{CLK0}}$ (HSTL) is the active differential clock input	CLK1, $\overline{\text{CLK1}}$ (PECL) is the active differential clock input
$\overline{\text{OE}}$	0	Q[0-9], $\overline{\text{Q[0-9]}}$ are active. Deassertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses.	Q[0-9] = L, $\overline{\text{Q[0-9]}}$ =H (outputs disabled). Assertion of $\overline{\text{OE}}$ can be asynchronous to the reference clock without generation of output runt pulses.

Table 3. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	–0.3	3.6	V	
V_{CCO}	Supply Voltage	–0.3	3.1	V	
V_{IN}	DC Input Voltage	–0.3	V_{CC} + 0.3	V	
V_{OUT}	DC Output Voltage	–0.3	V_{CC} + 0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	–65	125	°C	
T_{Func}	Functional Temperature Range	T_A = –40	T_J = +110	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 4. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output termination voltage		0		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	TBD			V	
LU	Latch-up Immunity	200			mA	
C_{IN}	Input Capacitance		4.0		pF	Inputs
θ_{JA}	Thermal resistance junction to ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
T_J	Operating Junction Temperature[1] (continuous operation) MTBF = 9.1 years			110	°C	

1. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 and the application section in this datasheet for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES8111 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES8111 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 5. DC Characteristics (V_{CC} = 3.3 V±5%, V_{CCO} = 1.5 V±0.1 V or V_{CCO} = 1.8 V±0.1 V, T_J = 0°C to +110°C)[1]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$ (HSTL differential signals)						
V_{DIF}	Differential Input Voltage[2]	0.2			V	
$V_{X, IN}$	Differential Cross Point Voltage[3]	0.25	0.68 – 0.9	V_{CC}–1.3	V	
V_{IH}	Input High Voltage	V_X+0.1			V	
V_{IL}	Input Low Voltage			V_X–0.1	V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_X \pm 0.1V$
Clock input pair CLK1, $\overline{CLK1}$ (PECL differential signals)						
V_{PP}	Differential Input Voltage[4]	0.15		1.0	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[5]	1.0		V_{CC}–0.6	V	Differential operation
V_{IH}	Input Voltage High	V_{CC}–1.165		V_{CC}–0.880	V	
V_{IL}	Input Voltage Low	V_{CC}–1.810		V_{CC}–1.475	V	
I_{IN}	Input Current[1]			±150	mA	$V_{IN} = V_{IH}$ or V_{IN}
LVCMOS control inputs $\overline{OE}$, CLK_SEL						
V_{IL}	Input Voltage Low			0.8	V	
V_{IH}	Input Voltage High	2.0			V	
I_{IN}	Input Current			±150	mA	$V_{IN} = V_{IH}$ or V_{IN}
HSTL clock outputs (Q[0-9], $\overline{Q[0-9]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Output Low Voltage			0.4	V	
Supply current						
I_{CC}	Maximum Quiescent Supply Current without output termination current		100	TBD	mA	V_{CC} pin (core)
I_{CCO}[6]	Maximum Quiescent Supply Current, outputs terminated 50Ω to V_{TT}		TBD	TBD	mA	V_{CCO} pins (outputs)

1. DC characteristics are design targets and pending characterization.
2. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
3. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{PP} (DC) specification.
4. V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
5. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.
6. I_{CC} includes current through the output resistors (all outputs terminated to V_{TT}).

Table 6. AC Characteristics (V_{CC} = 3.3 V±5%, V_{CCO} = 1.5 V ± 1 V or V_{CCO} = 1.8 V ± 0.1 V, T_J = 0°C to +110°C)[1, 2]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
Clock input pair CLK0, $\overline{CLK0}$ (HSTL differential signals)						
V_{DIF}	Differential Input Voltage (peak-to-peak)[3]	0.4			V	
$V_{X, IN}$	Differential Cross Point Voltage[4]	0.68		0.9	V	
f_{CLK}	Input Frequency		0–400	TBD	MHz	
t_{PD}	Propagation Delay CLK0 to Q[0-9]			TBD	ps	
Clock input pair CLK1, $\overline{CLK1}$ (PECL differential signals)						
V_{PP}	Differential Input Coltage (peak-to-peak)[5]	0.2		1.0	V	
V_{CMR}	Differential Input Crosspoint Voltage[6]	1		V_{CC}–0.6	V	
f_{CLK}	Input Frequency		0-400		MHz	Differential
t_{PD}	Propagation Delay CLK1 to Q[0-9]			TBD	ps	Differential
HSTL clock outputs (Q[0-9], $\overline{Q[0-9]}$)						
$V_{X, OUT}$	Output Differential Crosspoint	0.68	0.75	0.9	V	
V_{OH}	Output High Voltage	1			V	
V_{OL}	Output Low Voltage			0.5	V	
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak)	0.5			V	
$t_{sk(O)}$	Output-to-Output Skew			50	ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part)			TBD	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter			TBD		
DC_O	Output Duty Cycle	TBD	50	TBD	%	DC_{fref}= 50%
t_r, t_f	Output Rise/Fall Time	0.05		TBD	ns	20% to 80%
t_{PDL}[7]	Output Disable Time	2.5·T + t_{PD}		3.5·T + t_{PD}	ns	T=CLK period
t_{PLD}[8]	Output Enable Time	3·T + t_{PD}		4·T + t_{PD}	ns	T=CLK period

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. V_{DIF} (DC) is the minimum differential HSTL input voltage swing required for device functionality.
4. V_X (DC) is the crosspoint of the differential HSTL input signal. Functional operation is obtained when the crosspoint is within the V_X (DC) range and the input swing lies within the V_{DIF} (DC) specification.
5. V_{PP} (AC) is the minimum differential PECL input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
6. V_{CMR} (AC) is the crosspoint of the differential HSTL input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
7. Propagation delay $\overline{OE}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
8. Propagation delay $\overline{OE}$ assertion to output enabled (active).

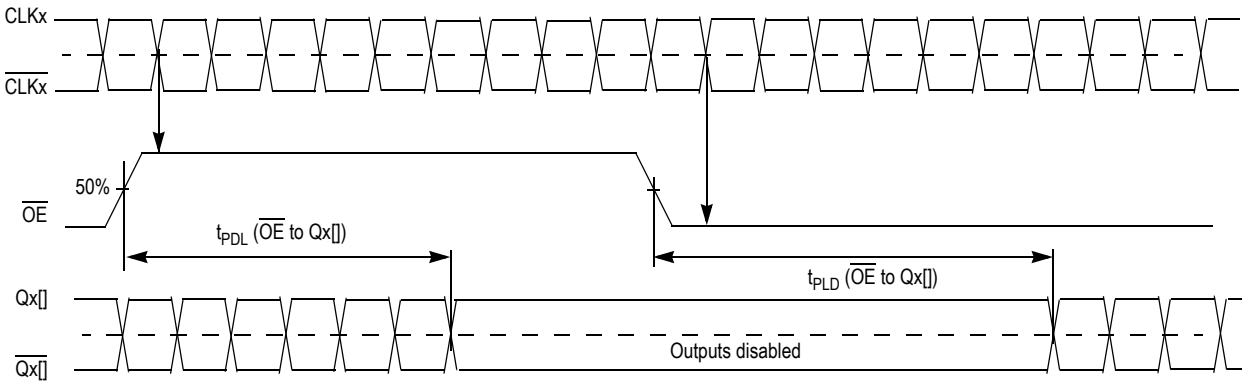


Figure 3. MC100ES8111 AC Test Reference

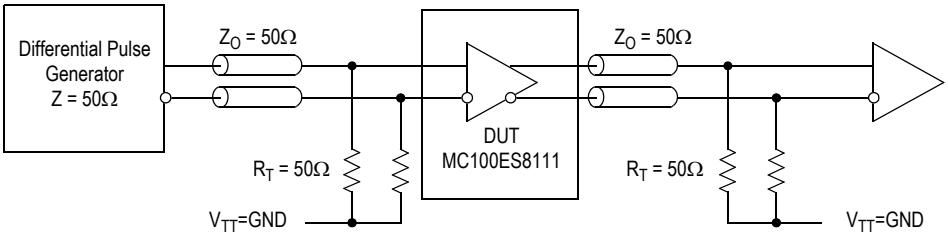


Figure 4. MC100ES8111 AC Test Reference

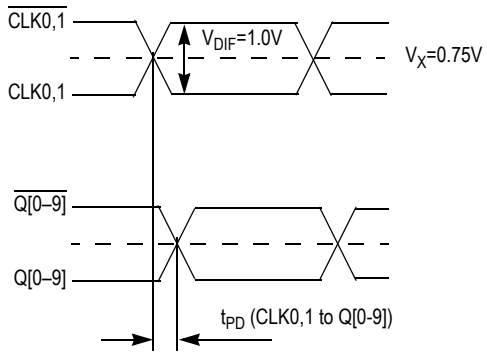


Figure 5. MC100ES8111 AC Reference Measurement Waveform (HSTL Input)

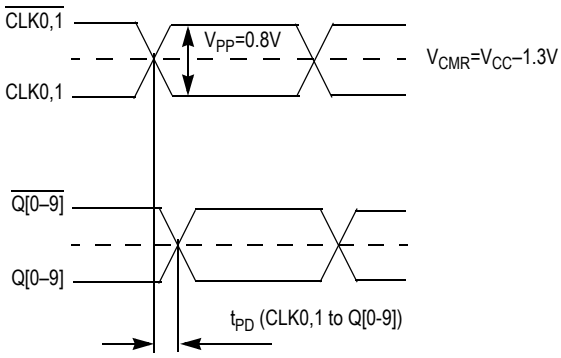


Figure 6. MC100ES8111 AC Reference Measurement Waveform (PECL Input)

Chapter Nine
Packaging Information

The packaging information for each device type can be determined in one of two ways: by the specific case number indicated on the individual data sheet (for example, the case number for MPC9600 is 932), or by using the *Case Dimensions Cross-Reference Tables* provided at the beginning of this chapter. Case dimension information is presented in numerical order; by case number.

Case Dimension Cross-Reference Tables

Table 1. Clock Generators

Device	Package	Case Number	Page
MC88915T	28 PLCC	776-02	787
MC88LV915T	28 PLCC	776-02	787
MC88LV926	20 SOIC	751D-06	786
MPC9315	32 LQFP	873A-03	789
MPC9330	32 LQFP	873A-03	789
MPC9331	32 LQFP	873A-03	789
MPC9350	32 LQFP	873A-03	789
MPC9351	32 LQFP	873A-03	789
MPC93H51	32 LQFP	873A-03	789
MPC93R51	32 LQFP	873A-03	789
MPC9352	32 LQFP	873A-03	789
MPC93H52	32 LQFP	873A-03	789
MPC93R52	32 LQFP	873A-03	789
MPC9600	32 LQFP	932-03	790
MPC9772	52 LQFP	848D-03	788
MPC9773	52 LQFP	848D-03	788
MPC97H73	52 LQFP	848D-03	788
MPC9774	52 LQFP	848D-03	788
MPC97H74	52 LQFP	848D-03	788
MPC992	32 LQFP	873A-03	789
MPC9992	32 LQFP	873A-03	789

Table 2. QUICCClock Generators

Device	Package	Case Number	Page
MPC9817	20 SSOP	1461-01	795
MPC9850	20 LQFP	1462-01	796
MPC9855	20 LQFP	1462-01	796

Table 3. Failover or Redundant Clock

Device	Package	Case Number	Page
MPC9892	32 LQFP	873A-03	789
MPC9893	48 LQFP	932-03	790
MPC9894	100 MAPBGA	1462-01	796
MPC9895	100 MAPBGA	1462-01	796
MPC9993	32 LQFP	873A-03	789
MPC99J93	32 LQFP	873A-03	789

Table 4. Clock Synthesizers

Device	Package	Case Number	Page
MC12429	28 PLCC	776-02	787
	32 LQFP	873A-03	789
MC12430	32 LQFP	873A-03	789
MC12439	28 PLCC	776-02	787
MPC9229	28 PLCC	776-02	787
	32 LQFP	873A-03	789
MPC9230	28 PLCC	776-02	787
	32 LQFP	873A-03	789
MPC9239	28 PLCC	776-02	787
MPC92429	28 PLCC	776-02	787
	32 LQFP	873A-03	789
MPC92430	28 PLCC	776-02	787
	32 LQFP	873A-03	789
MPC92432	32 LQFP	932-03	790
MPC92439	28 PLCC	776-02	787
	32 LQFP	873A-03	789
MPC92459	32 LQFP	873A-03	789
MPC926508	20 LQFP	1461-01	795
MPC9994	32 LQFP	873A-03	789

Table 5. Zero–Delay Buffers

Device	Package	Case Number	Page
MPC9608	32 LQFP	873A-03	789
MPC961C	32 LQFP	873A-03	789
MPC961P	32 LQFP	873A-03	789
MPC962304	8 SOIC	751-06	784
MPC962305	8 SOIC	751-06	784
	8 TSSOP	948J-01	793
	16 SOIC	751B-05	785
	16 TSSOP	948F-01	792
MPC962308	16 SOIC	751B-05	785
	16 TSSOP	948F-01	792
MPC9653	32 LQFP	873A-03	789
MPC9653A	32 LQFP	873A-03	789
MPC9658	32 LQFP	873A-03	789
MPC96877	52 MAPBGA	1544-01	797
	40 MLF/QFN	1545-01	798

Case Dimension Cross-Reference Tables (continued)

Table 6. LVCMOS Fanout Buffers

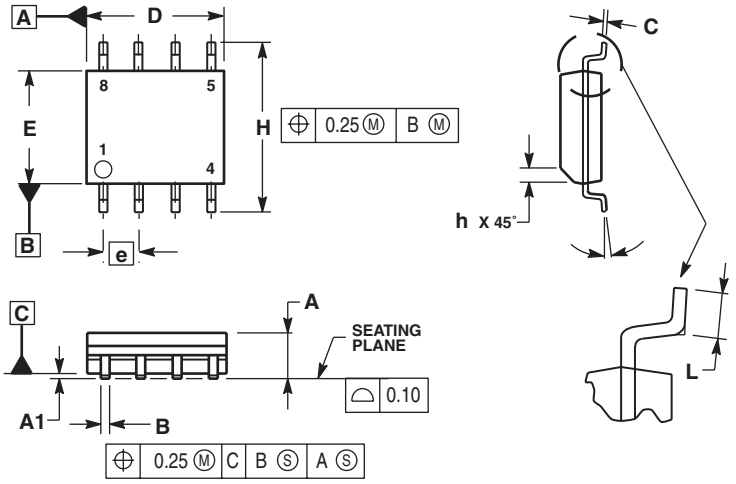
Device	Package	Case Number	Page
MPC905	16 SOIC	751B-05	785
MPC9109	32 QFP	873A-03	789
MPC940L	32 LQFP	873A-03	789
MPC941	32 LQFP	932-03	790
MPC942C	32 LQFP	873A-03	789
MPC942P	32 LQFP	873A-03	789
MPC9443	32 LQFP	932-03	790
MPC9446	32 LQFP	873A-03	789
MPC9447	32 LQFP	873A-03	789
MPC9448	32 LQFP	873A-03	789
MPC9449	52 LQFP	848D-03	788
MPC94551	8 SOIC	751-06	784
MPC9456	32 LQFP	873A-03	789

Table 7. Differential Fanout Buffers

Device	Package	Case Number	Page
MC100ES6011	8 SOIC	751-06	784
MC100ES6014	20 SOIC	751D-06	786
	20 TSSOP	948E-02	791
MC100ES60T22	8 SOIC	751-06	784
MC100ES60T23	8 SOIC	751-06	784
MC100ES6030	20 SOIC	751D-06	786
MC100ES6039	20 SOIC	751D-06	786
MC100ES6056	20 SOIC	751D-06	786
	20 TSSOP	948E-02	791
MC100ES6111	32 LQFP	873A-03	789
MC100ES6130	16 TSSOP	948F-01	792
MC100ES6139	20 TSSOP	948E-02	791
	20 SOIC	751D-06	786
MC100ES6210	32 LQFP	873A-03	789
MC100ES6220	52 LQFP	1336A-01	794
MC100ES6221	52 LQFP	1336A-01	794
MC100ES6222	52 LQFP	1336A-01	794
MC100ES6226	32 LQFP	873A-03	789
MC100ES6254	32 LQFP	873A-03	789
MC100ES6535	20 TSSOP	948E-02	791
MC100ES7011H	8 SOIC	751-06	784
MC100ES7011P	8 SOIC	751-06	784
MC100ES7014	20 TSSOP	948E-02	791
MC100ES7111	32 LQFP	873A-03	789
MC100ES8011H	8 SOIC	751-06	784
MC100ES8011P	8 SOIC	751-06	784
MC100ES8014	20 TSSOP	948E-02	791
MC100ES8111	32 LQFP	873A-03	789

Case Dimensions

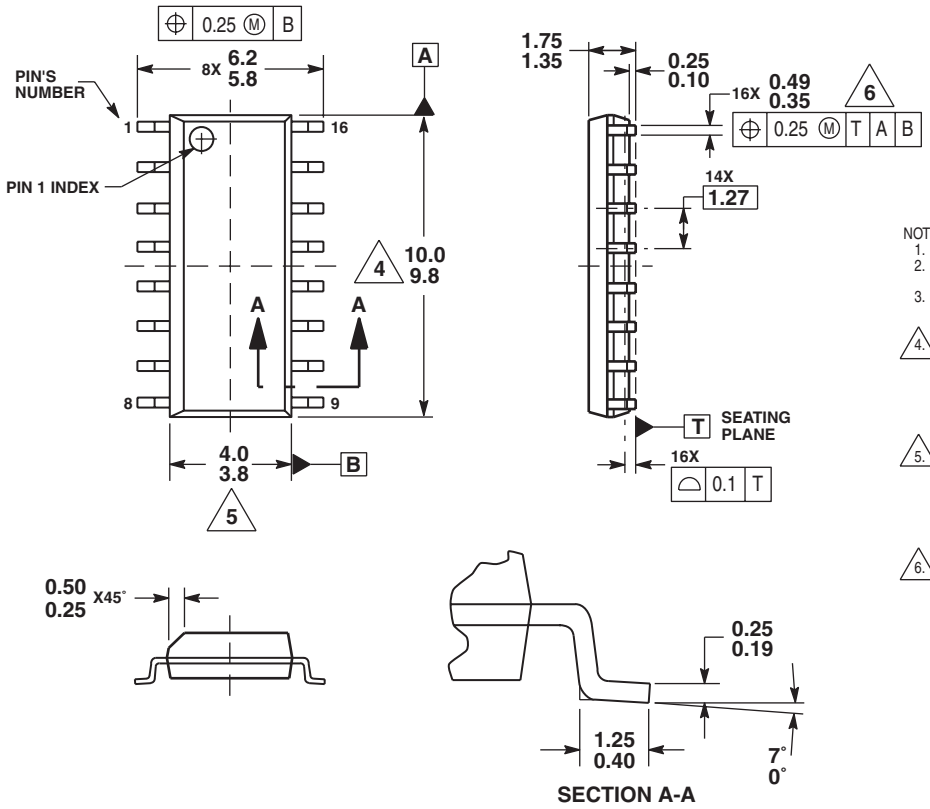
D SUFFIX
PLASTIC 8 SOIC PACKAGE
CASE 751-06
ISSUE T



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
q	0°	7°

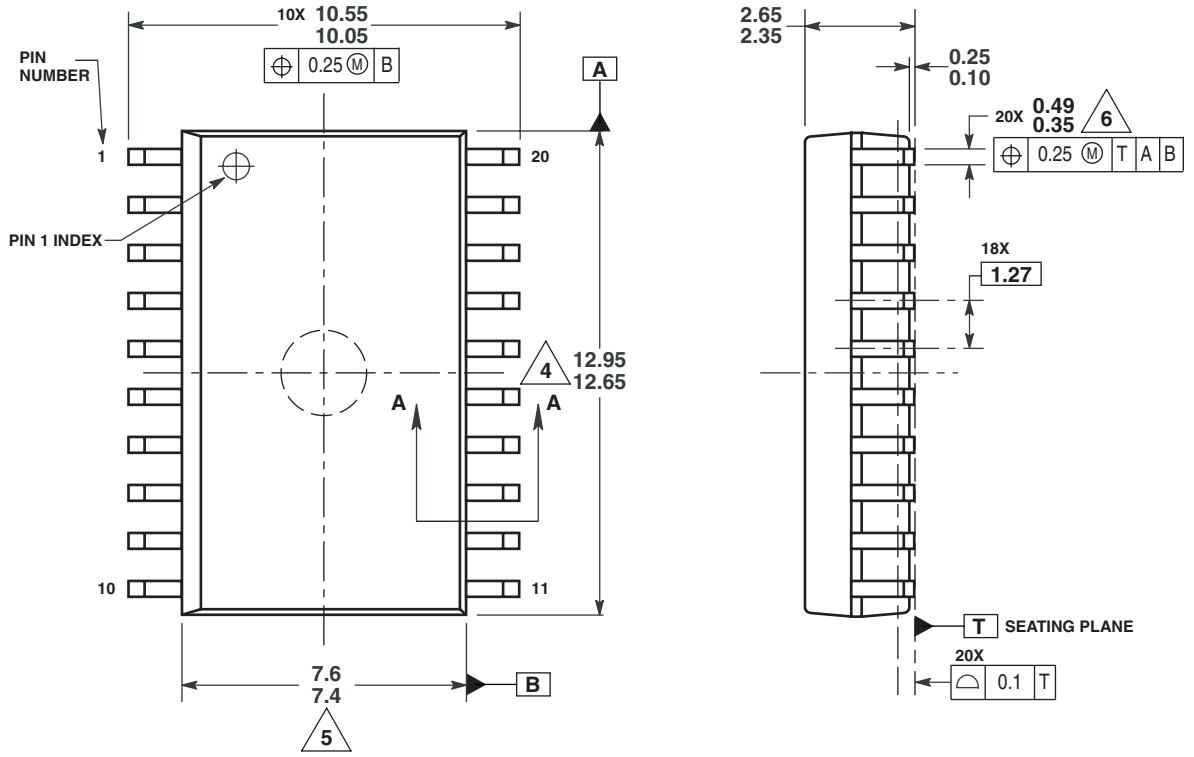
D SUFFIX
PLASTIC 16 SOIC PACKAGE
CASE 751B-05
ISSUE K

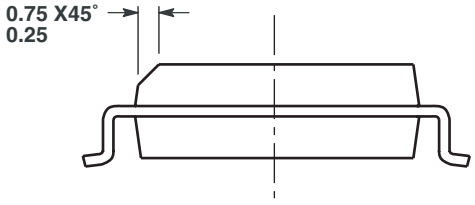


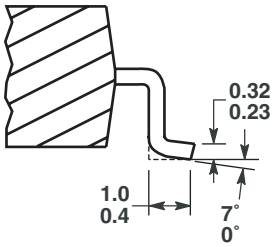
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.62MM.

Case Dimensions

D SUFFIX
PLASTIC 20 SOIC PACKAGE
CASE 751D-06
ISSUE H



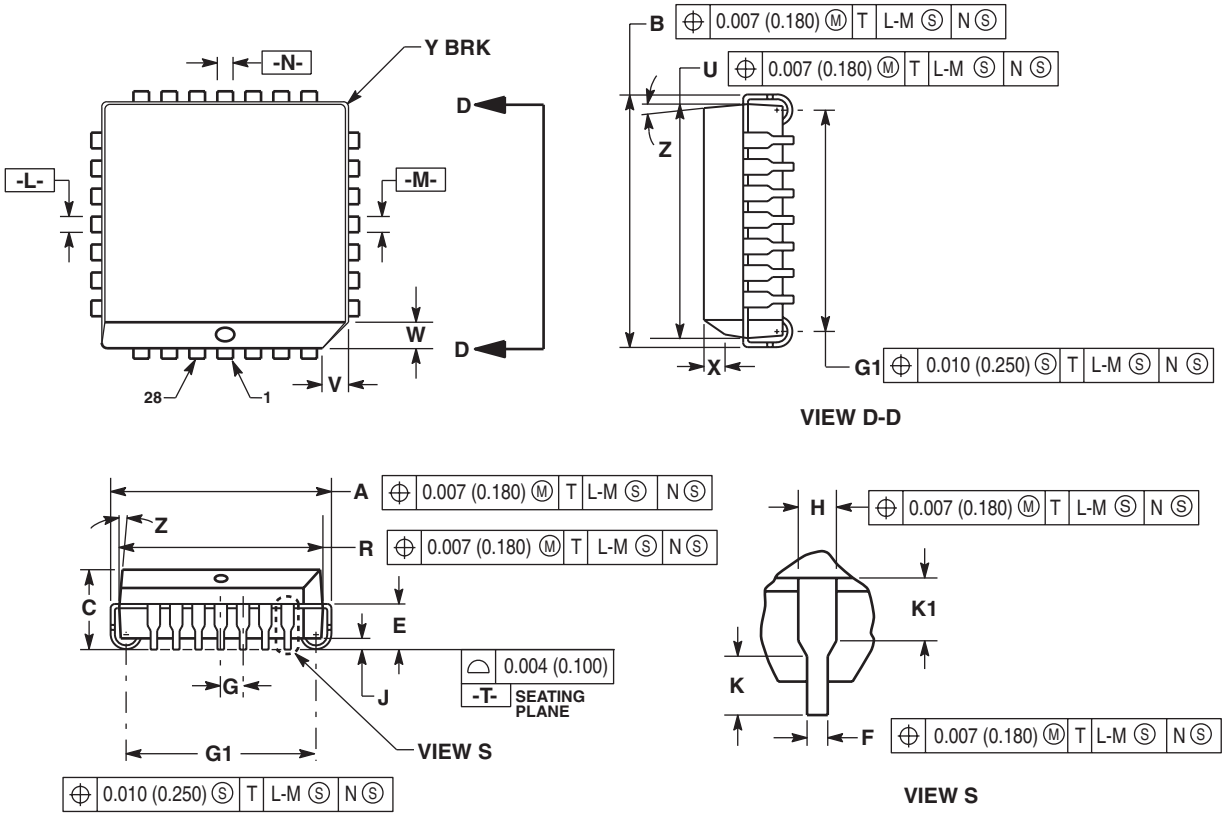




SECTION A-A

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUMS A AND B TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE WIDTH TO EXCEED 0.62 MM.

FN SUFFIX
PLASTIC 28 PLCC PACKAGE
CASE 776-02
ISSUE D

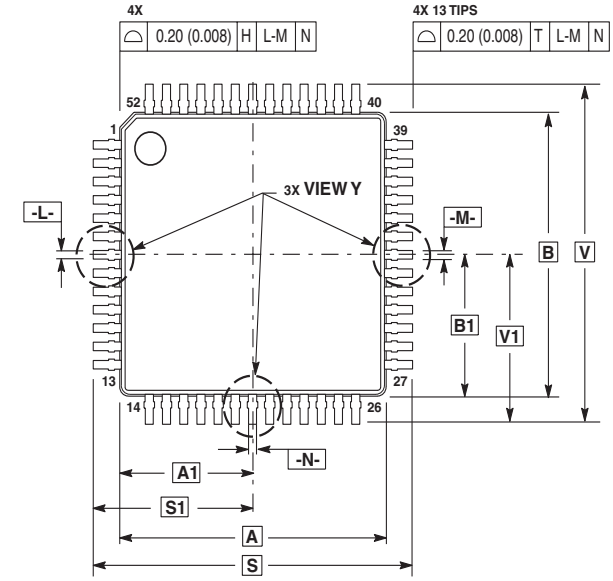


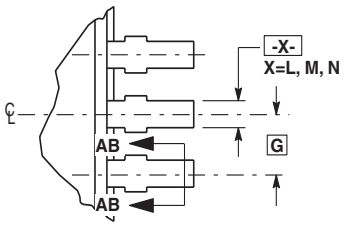
NOTES:
1. DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXISTS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DEMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASITC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

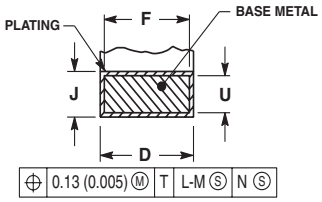
Case Dimensions

FA SUFFIX
PLASTIC 52 LQFP PACKAGE
CASE 848D-03
ISSUE D

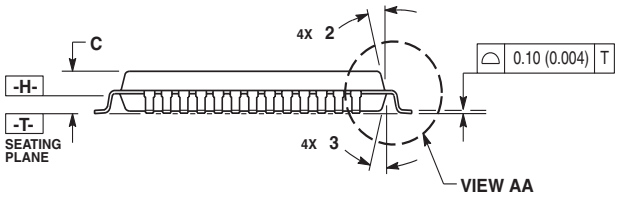




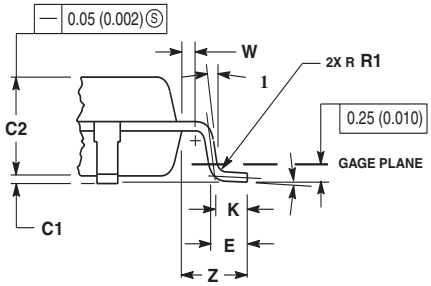
VIEW Y



SECTION AB-AB
ROTATED 90° CLOCKWISE



VIEW AA

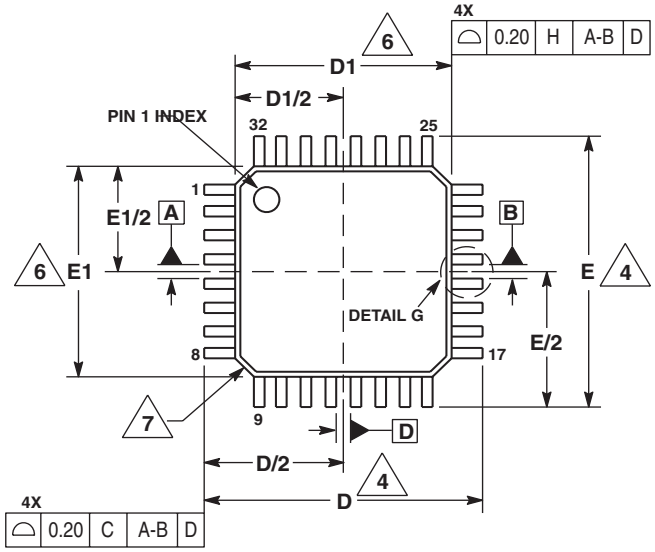


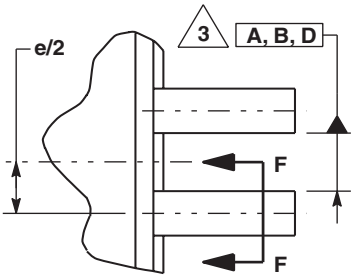
VIEW AA

NOTES:
1. CONTROLLING DIMENSIONS: MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -L-, -M- AND -N- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -T-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 (0.018). MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSTION 0.07 (0.003).

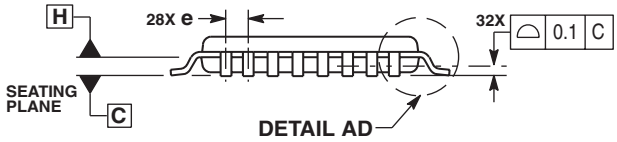
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.00 BSC		0.394 BSC	
A1	5.00 BSC		0.197 BSC	
B	10.00 BSC		0.394 BSC	
B1	5.00 BSC		0.197 BSC	
C	---	1.70	---	0.067
C1	0.05	0.20	0.002	0.008
C2	1.30	1.50	0.051	0.059
D	0.20	0.40	0.008	0.016
E	0.45	0.75	0.018	0.030
F	0.22	0.35	0.009	0.014
G	0.65 BSC		0.026 BSC	
J	0.07	0.20	0.003	0.008
K	0.50 REF		0.020 REF	
R1	0.08	0.20	0.003	0.008
S	12.00 BSC		0.472 BSC	
S1	6.00 BSC		0.236 BSC	
U	0.09	0.16	0.004	0.006
V	12.00 BSC		0.472 BSC	
V1	6.00 BSC		0.236 BSC	
W	0.20 REF		0.008 REF	
Z	1.00 REF		0.039 REF	
	0°	7°	0°	7°
1	0°	---	0°	---
2	12° REF		12° REF	
3	12° REF		12° REF	

FA SUFFIX
PLASTIC 32 LQFP PACKAGE
CASE 873A-03
ISSUE B

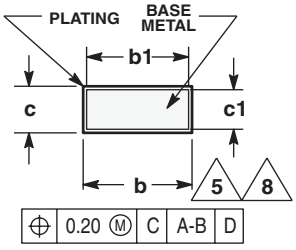




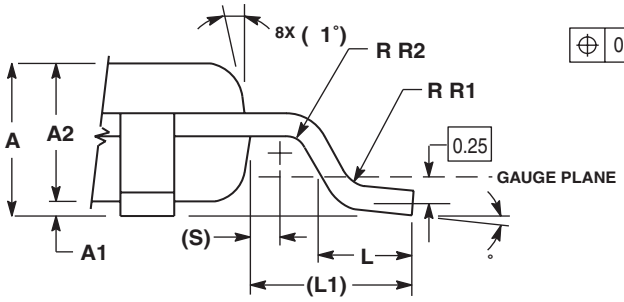
DETAIL G



DETAIL AD



SECTION F-F



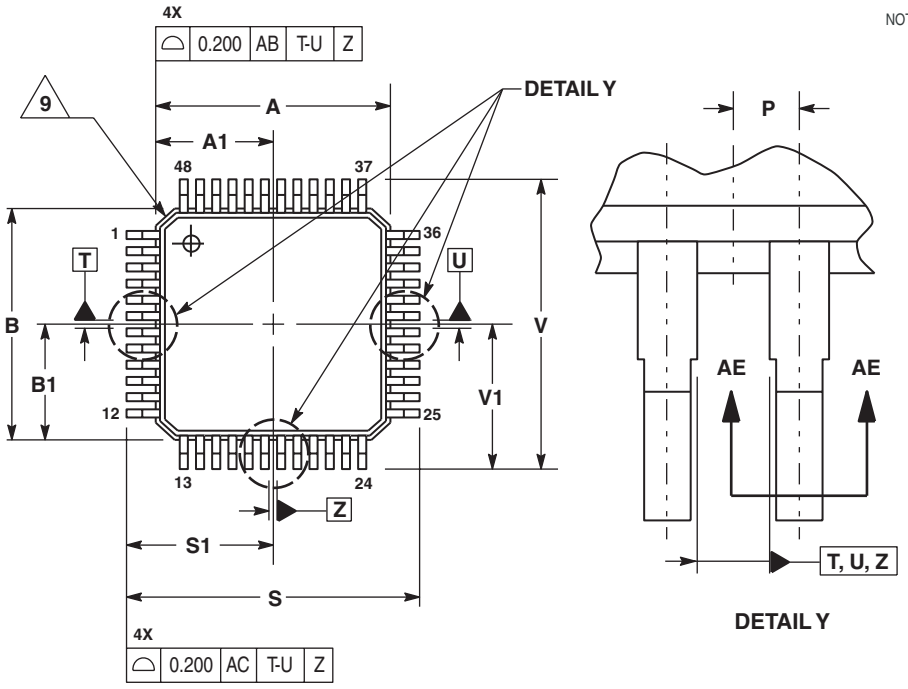
DETAIL AD

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40	1.60
A1	0.05	0.15
A2	1.35	1.45
b	0.30	0.45
b1	0.30	0.40
c	0.09	0.20
c1	0.09	0.16
D	9.00 BSC	
D1	7.00 BSC	
e	0.80 BSC	
E	9.00 BSC	
E1	7.00 BSC	
L	0.50	0.70
L1	1.00 REF	
q	0°	7°
q1	12 REF	
R1	0.08	0.20
R2	0.08	---
S	0.20 REF	

Case Dimensions

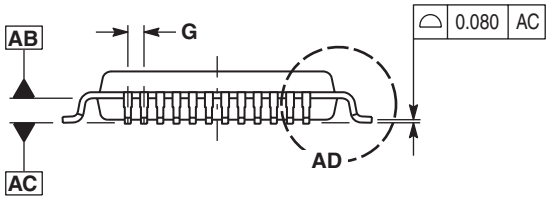
FA SUFFIX
PLASTIC 32 LQFP PACKAGE
CASE 932-03
ISSUE F

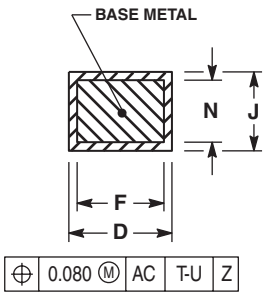


DETAIL Y

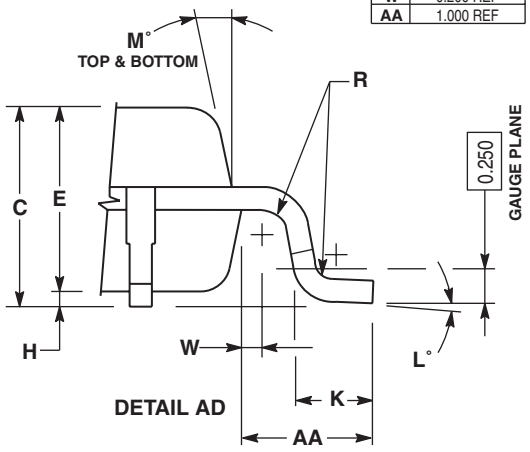
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5m, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLAN AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATAUM PLANE AB.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

	MILLIMETERS	
DIM	MIN	MAX
A	7.000 BSC	
A1	3.500 BSC	
B	7.000 BSC	
B1	3.500 BSC	
C	1.400	1.600
D	0.170	0.270
E	1.350	1.450
F	0.170	0.230
G	0.500 BSC	
H	0.050	0.150
J	0.090	0.200
K	0.500	0.700
L	0°	7°
M	12° REF	
N	0.090	0.160
P	0.250 BSC	
R	0.150	0.250
S	9.000 BSC	
S1	4.500 BSC	
V	9.000 BSC	
V1	4.500 BSC	
W	0.200 REF	
AA	1.000 REF	



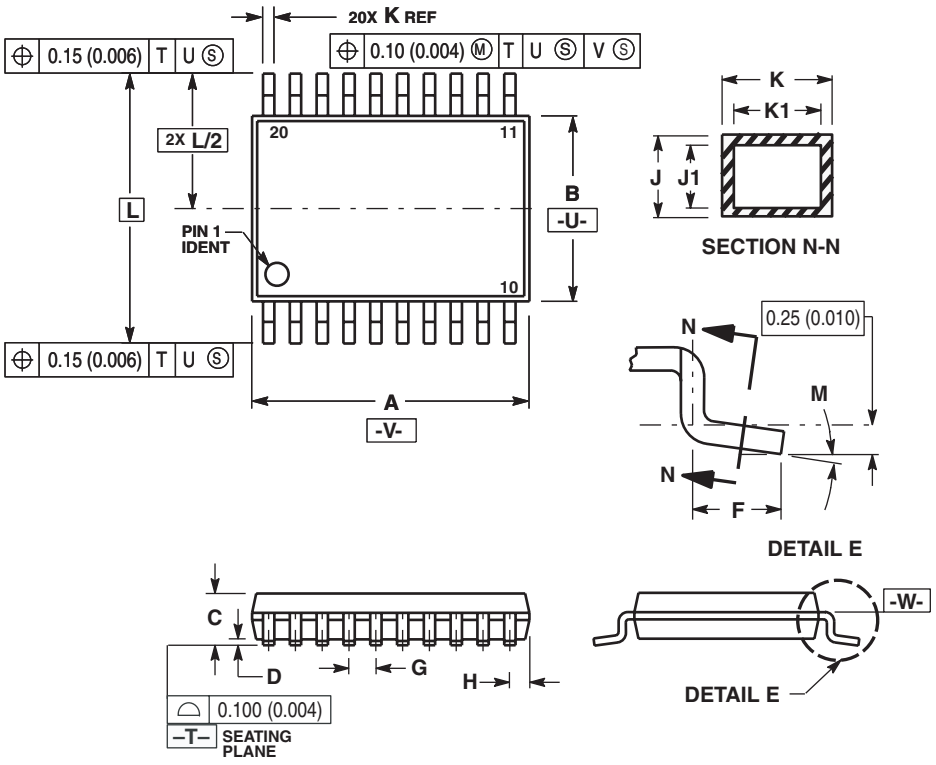


SECTION AE-AE



DETAIL AD

DT SUFFIX
PLASTIC 20 TSSOP PACKAGE
CASE 948E-02
ISSUE A

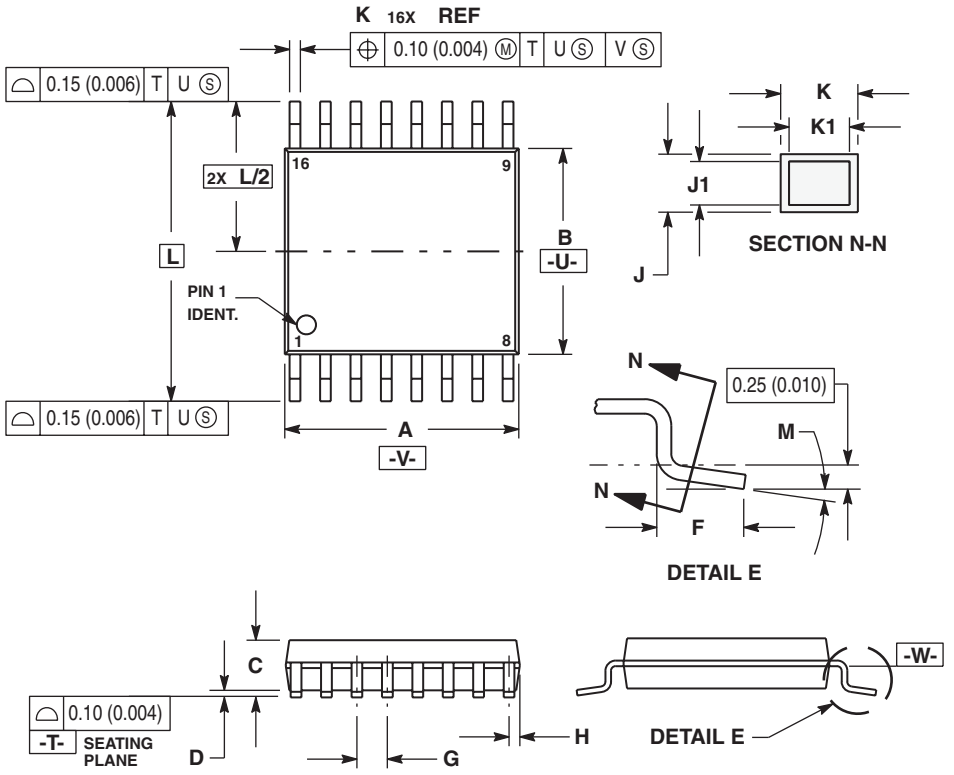


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND BE ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

Case Dimensions

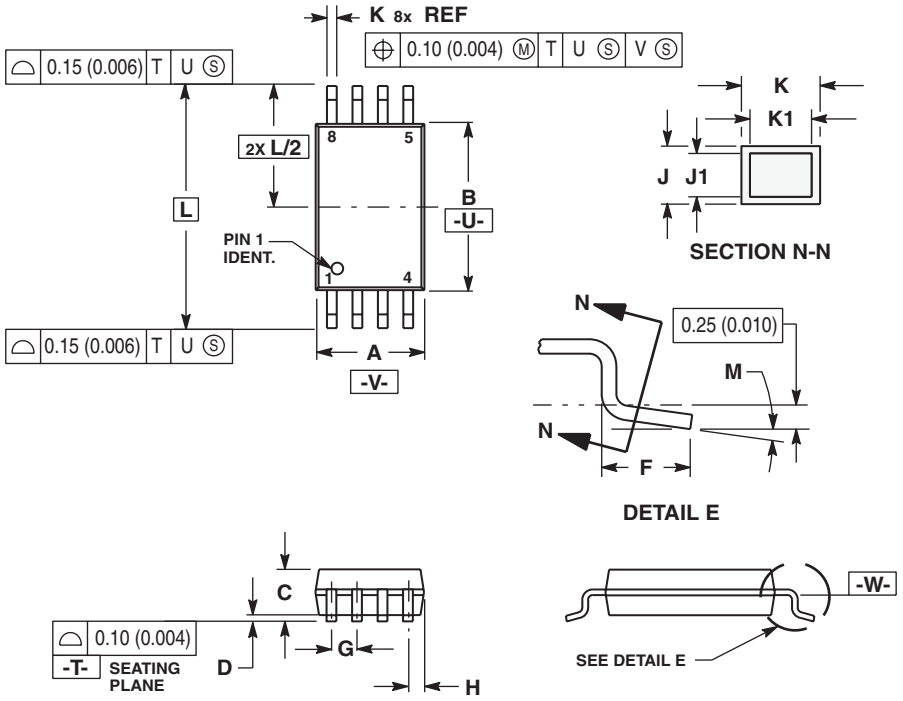
DT SUFFIX
PLASTIC 16 TSSOP PACKAGE
CASE 948F-01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

DT SUFFIX
PLASTIC 8 TSSOP PACKAGE
CASE 948J-01
ISSUE O

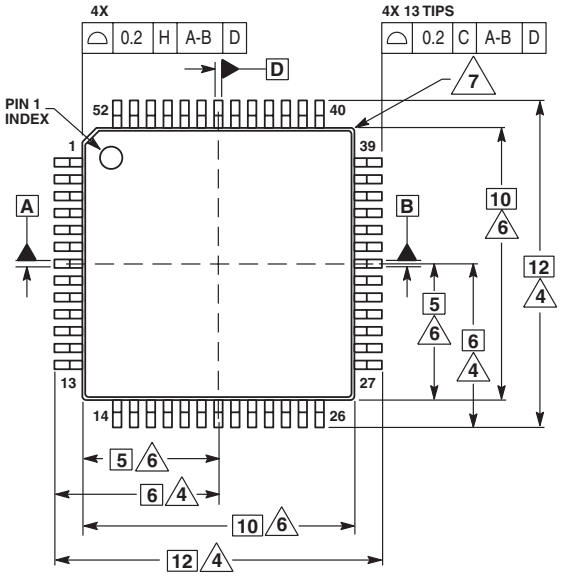


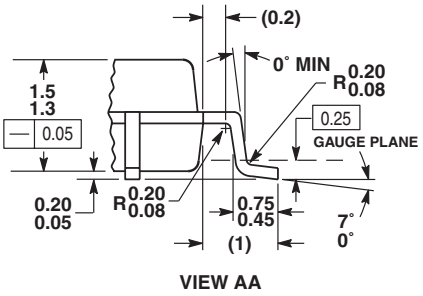
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

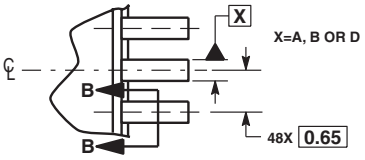
Case Dimensions

FA SUFFIX
PLASTIC 52 LQFP EXPOSED PAD PACKAGE
CASE 1336A-01
ISSUE O

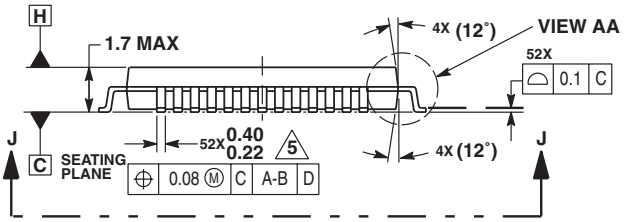


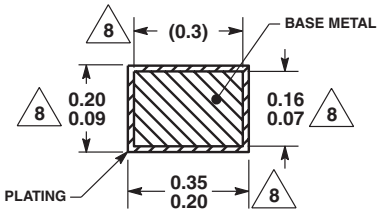


VIEW AA

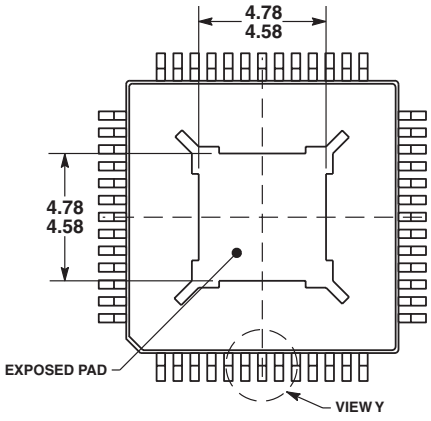


VIEW Y





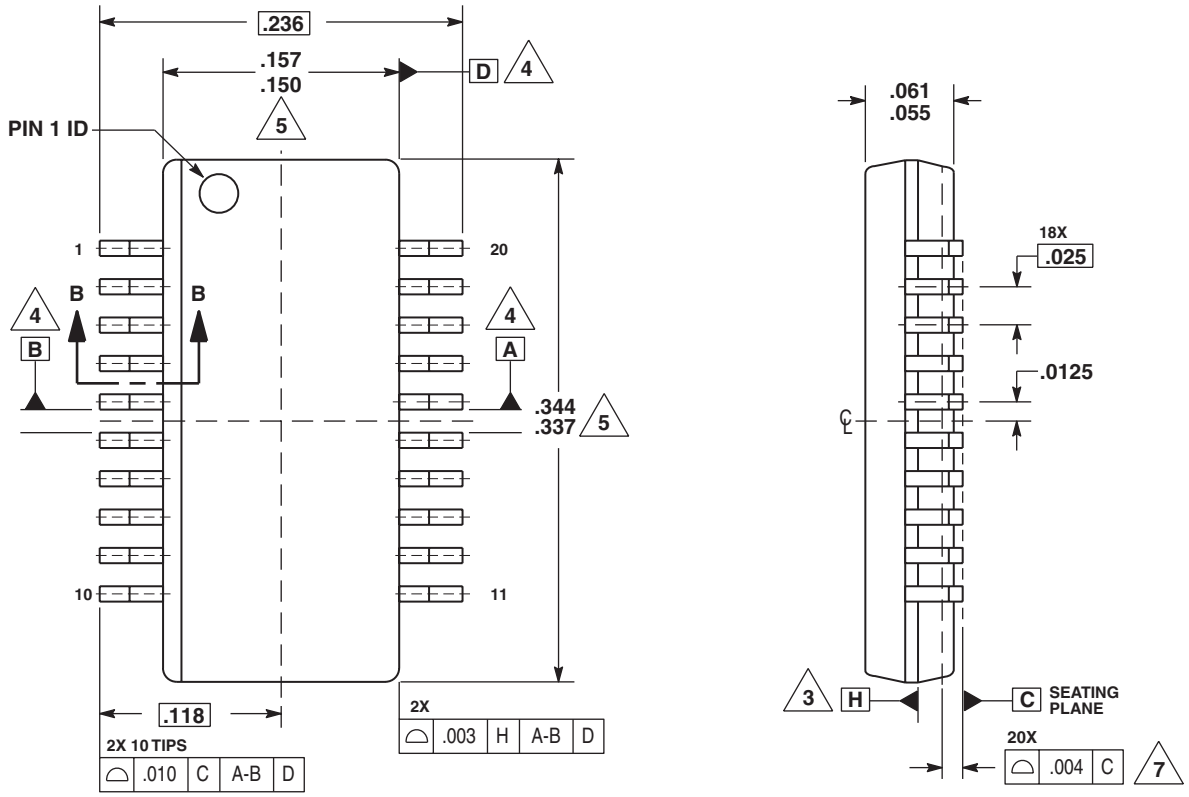
SECTION B-B

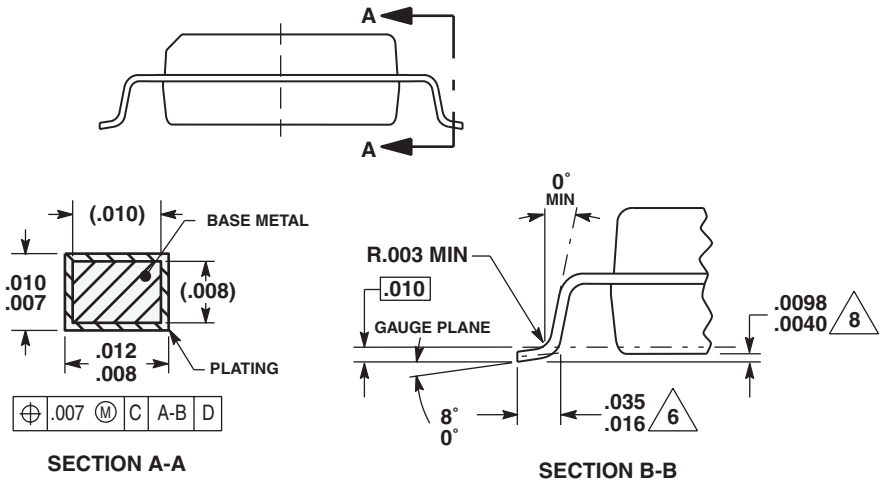


VIEW J-J

NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSION TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. THIS DIMENSION IS MAXIMUM PLSTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.

SD SUFFIX
PLASTIC 20 LQFP SSOP PACKAGE
CASE 1461-01
ISSUE O

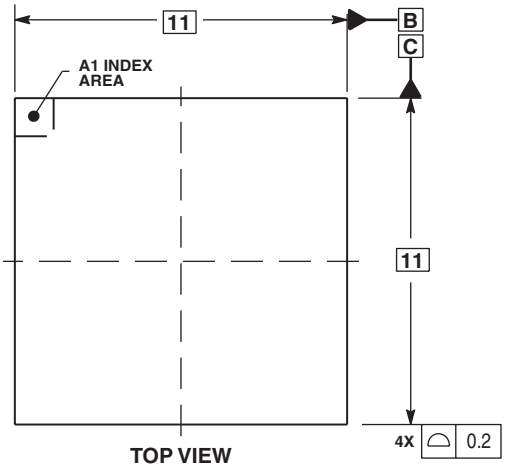




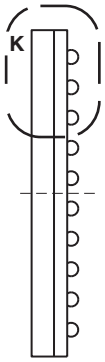
NOTES:
1. DIMENSIONS ARE IN INCHES.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
4. DATUM A, B AND D TO BE DETRMINED WHERE CENTERLINE BETWEEN LEADS EXITS PLASTIC BODY AT DATUM PLANE H.
5. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DO INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006 INCHES FOR ENDS AND .008 INCHES FOR SIDES.
6. THIS DIMENSION IS LENGTH OF TERMINAL FOR SOLDERING A SUBSTRATE.
7. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .004 INCHES AT SEATING PLANE.
8. THIS DIMENSION IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

Case Dimensions

VF SUFFIX
100 MAP PBGA PACKAGE
CASE 1462-01
ISSUE O

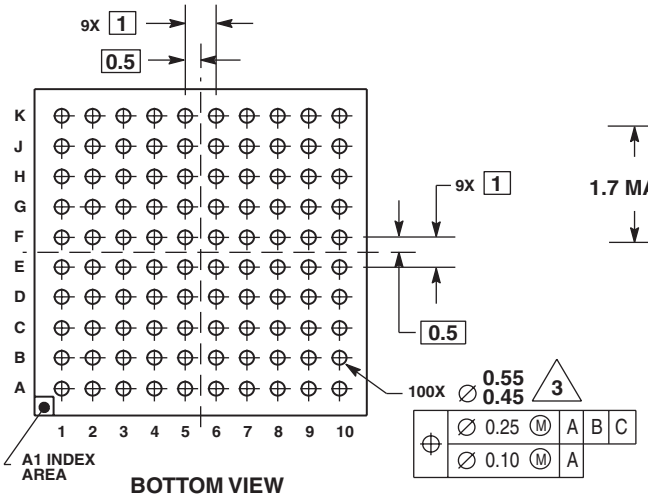


TOP VIEW

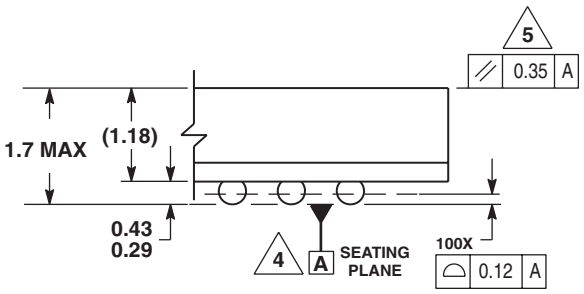


SIDE VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGING.

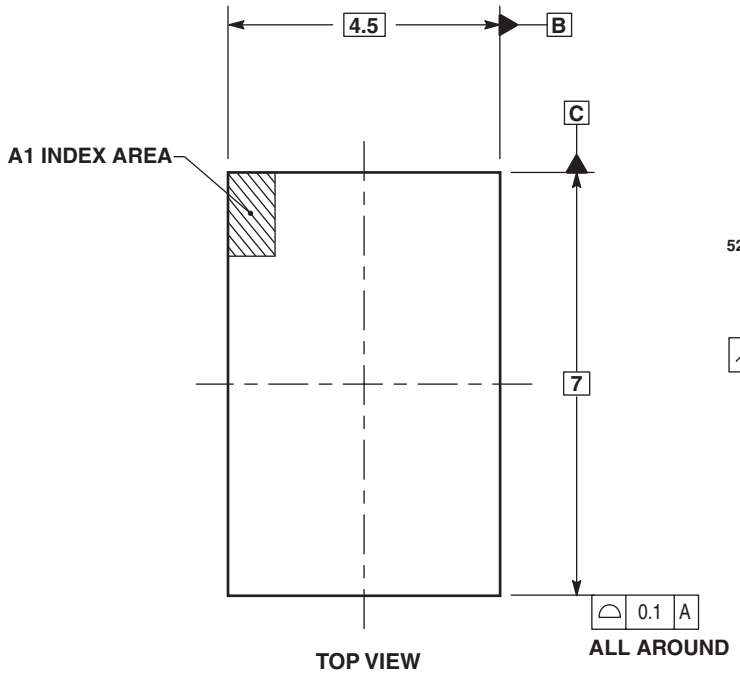


BOTTOM VIEW

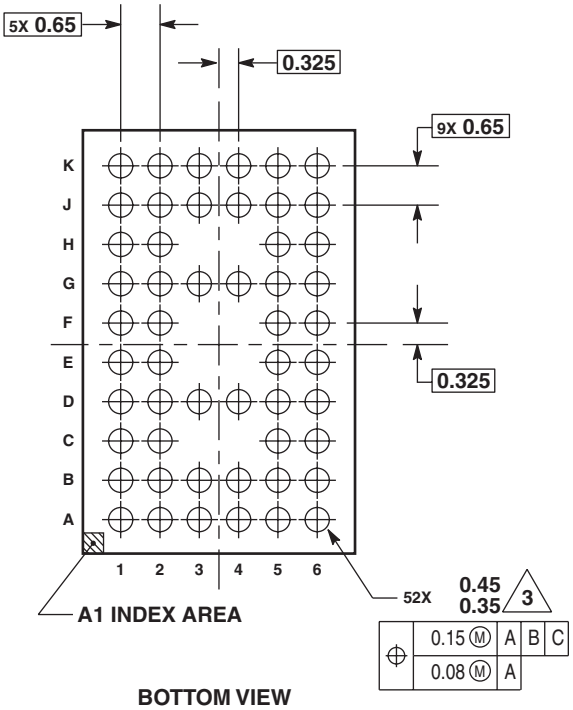


DETAIL K
ROTATED 90° CLOCKWISE

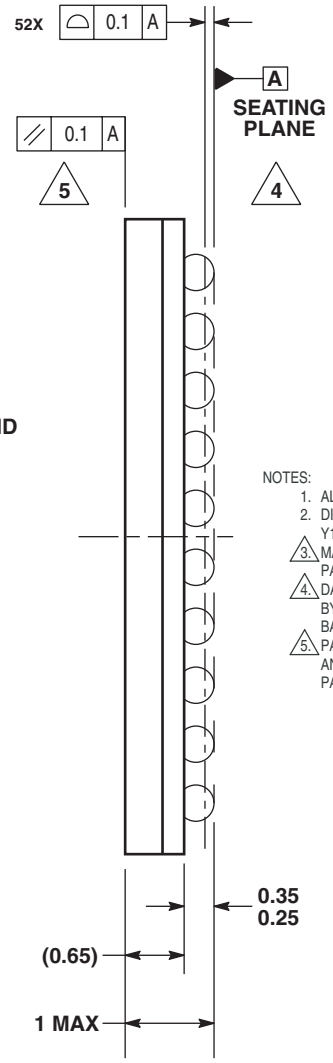
VK SUFFIX
52-BALL FP-MAPBGA
NON-LEADED PACKAGE
CASE 1544-01
ISSUE O



TOP VIEW



BOTTOM VIEW

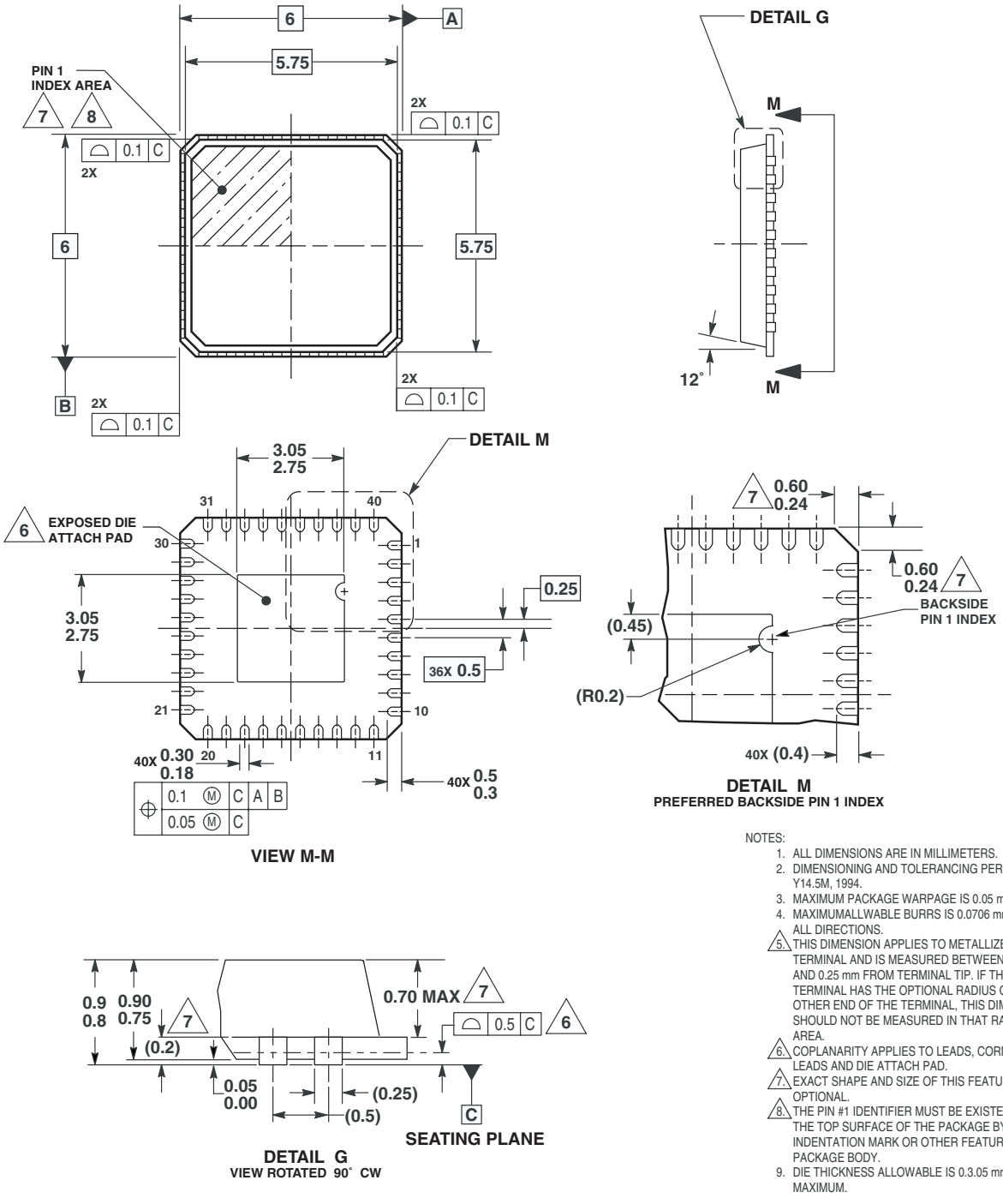


SIDE VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A. THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Case Dimensions

EP SUFFIX
40-PIN MLF/QFN PACKAGE
CASE 1545-01
ISSUE O



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
3. MAXIMUM PACKAGE WARPAGE IS 0.05 mm.
4. MAXIMUMALLWABLE BURRS IS 0.0706 mm IN ALL DIRECTIONS.
5. THIS DIMENSION APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THIS DIMENSION SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
6. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
7. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
8. THE PIN #1 IDENTIFIER MUST BE EXISTED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
9. DIE THICKNESS ALLOWABLE IS 0.3.05 mm MAXIMUM.

Chapter Ten
Application Notes

Application Notes

Order number: AN1091
Rev 4, 09/2001

AN1091

Low Skew Clock Drivers and Their System Design Considerations

ABSTRACT

This application note addresses various system design issues to help ensure that Motorola's low skew clock drivers are used effectively in a system environment.

Several varieties of clock drivers with 1 ns or less skew from output-to-output are available from Motorola. Microprocessor-based systems are now running at 33 MHz and beyond, and system clock distribution at these frequencies mandate the use of low skew clock drivers. Unfortunately, just plugging a high performance clock driver into a system does not guarantee trouble free operation. Only careful board layout and consideration of system noise issues can guarantee reliable clock distribution. This application note addresses these system design issues to help ensure that Motorola's low skew clock drivers are used effectively in a system environment.

INTRODUCTION

With frequencies regularly reaching 33 MHz and approaching 40-50 MHz in today's CISC and RISC microprocessor systems, well controlled and precise clock signals are required to maintain a synchronous system. Many microprocessors also require input clock duty cycles very close to 50%. These stringent timing requirements mandate the use of specially designed, low skew clock distribution circuits or 'clock drivers.' However, just plugging one of these parts into your board does not ensure a trouble free system. Careful system and board design techniques must be used in conjunction with a low skew clock driver to meet system timing requirements and provide clean clock signals.

Why are Low Skew Clock Drivers Necessary

An MPU system designer wants to utilize as much of a clock cycle as possible without adding unnecessary timing guardbands. Propagation delays of peripheral logic do not scale with frequency. Therefore, as the clock period decreases, the system designer has less time but the same logic delays to accomplish the function. How can he get more time? A viable option is to use a special clock source that minimizes clock 'uncertainty.'

A simple example illustrates this concept. At 33 MHz, t_{cycle} = 30 ns. An FCT240A, for example, has a High-Low uncertainty of the min/max spread of t_{PLH} to t_{PHL} of approximately 3.3 ns. If 1.7 ns of pin-to-pin skew due to the actual part and PCB trace delays is also considered, then only 25 ns of the clock period is still available. The worst case t_P of clock-to-data valid on the 88200 M-Bus is 12 ns, which leaves only 13 ns to accomplish additional functions. In this case 17% of a cycle is required for clock distribution or clock 'uncertainty,' which is an unacceptable penalty from a system designer's point of view. At 50 MHz this penalty becomes 25%. A maximum of 10% of the period allotted for clock distribution is an acceptable standard.

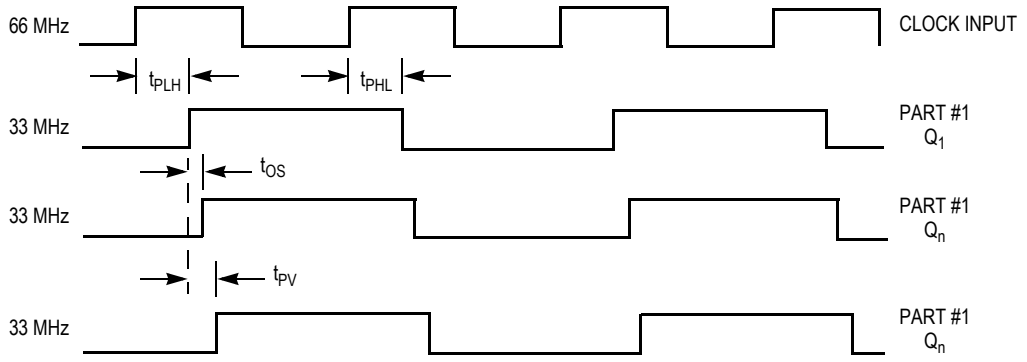
If multiple levels of clock distribution (one clock driver's output feeding the inputs of several other clock drivers) are necessary due to large clock fan-outs, the additional part-to-part skew variations add even more to the clock uncertainty. Standard logic has always been specified with a large (and conservative) delta between the minimum and maximum propagation delays. This delta creates the excessive amount of clock 'uncertainty' which the system designer has been forced to design into his system, even though it is not realistic. When system frequencies were below 16 MHz this large clock penalty could be tolerated, but as the above example points out, not anymore. A clock driver's specs guarantee this min/max delta to be a specific, small value. To reduce the clock overhead to manageable levels, a clock driver with minimal variation (<5%) from a 50% duty cycle and guaranteed low output-to-output and part-to-part skew must be used.

DEFINITIONS

A typical clock driver has a single input which is usually driven by a crystal oscillator. The clock driver can have any number of outputs which have a certain frequency relationship to the clock input. Clock driver skew is typically defined by three different specs. These specs are graphically illustrated in **Figure 1**.

The first spec, t_{OS}, measures the difference between the fastest and slowest propagation delays (any transition) between the outputs of a single part. This number must be 1ns or less for high-end systems.

The second, t_{PS}, measures the difference between the high-to-low and low-to-high transition for a single output (pin). This spec defines how close to a 50% duty cycle the outputs of the clock driver will be. For example, if this spec is 1 ns (±0.5 ns), at 33 MHz the output duty cycle is 50% ±3.5%. A clock driver which only buffers the crystal input, creating a 1:1 input to output frequency relationship, can be a problem if a very tight tolerance to a 50% duty cycle is required. In this situation the output duty cycle is directly dependent on the input duty cycle, which is not well controlled in most crystal oscillators. The clock driver's outputs switching at half the input frequency (÷2) is a common relationship, which means that the outputs switch on only one edge of the oscillator, eliminating the output's dependence on the duty cycle of the input (crystal oscillator frequency is very stable).



Notes: 1) t_{PS} measures $|t_{PLH}-t_{PHL}|$ for any single output on a part.
2) t_{OS} measures the maximum difference between any t_{PHL} or t_{PLH} between any output on a single part.
3) t_{PV} measures the maximum difference between any t_{PHL} or t_{PLH} between any output on any part.

Figure 1. Timing Diagram Depicting Clock Skew Specs Within One Part and Between Any Two Parts

The third spec, t_{PV}, measures the maximum propagation delay delta between any given pin on any part. This spec defines the part to part variation between any clock driver (of the same device type) which is ever shipped. This number reflects the process variation inherent in any technology. For CMOS, this spec is usually 3 ns or less. High performance ECL technologies can bring this number down into the 1–2 ns range. Another way to minimize the part-to-part variation is to use a phase-locked loop clock driver, which are just now becoming available.

An important consideration when designing a clock driver into a system is that the skew specs described above are usually specified at a fixed, lumped capacitive load. In a real system environment the clock lines usually have various loads distributed over several inches of PCB trace which can contribute additional delay and sometimes act like transmission lines, so the system designer must use careful board layout techniques to minimize the total system skew. In other words, just plugging a low skew clock driver into a board will not solve all your timing problems.

DESIGN CONSIDERATIONS

Figure 2 is a scale replication of a section of an actual 88000 RISC system board layout. The section shown in **Figure 2** includes the MC88100 MPU and the MC88200 CMMU devices and the MC88914 CMOS clock driver. The only PCB traces shown are the clock output traces from the MC88914 to the various loads. For this clock driver the output-to-output skew (t_{OS}) is guaranteed to be less than 1 ns at any given temperature, supply voltage, and fixed load up to 50 pF.

In calculating the total system skew, the difference in clock PCB trace length and loading must be taken into account. For an unloaded PCB trace, the signal delay per unit length, t_{PD}, is dependent only on the dielectric constant, e_r. of the board material. The characteristic impedance, Z_O, of the line is dependent upon e_r and the geometry of the trace. These relationships are depicted in **Figure 3** for a microstrip line.[1] The formulas for t_{PD} and Z_O are slightly different for other types of strip lines, but for simplicity's sake all calculations in this article will assume a microstrip line.

The equations in **Figure 3** are valid only for an unloaded trace; loading down a line will increase its delay and lower its impedance. The signal propagation delay (t_{PD}') and characteristic impedance (Z_O') due to a loaded trace are calculated by the following formulas:

$$t_{PD}' = t_{PD}\sqrt{1 + \frac{C_d}{C_O}}$$

$$Z_O' = \frac{Z_O}{\sqrt{1 + \frac{C_d}{C_O}}}$$

C_d is the distributed load capacitance per unit length, which is the total input capacitance of the receiving devices divided by the length of the trace. C_O is the intrinsic capacitance of the trace, which is defined as:

$$C_O = \frac{t_{PD}}{Z_O}$$

Assuming typical microstrip dimensions and characteristics as w = 0.01 in, t = 0.002 in, h = 0.012 in, and e_r = 4.7, the equations of **Figure 3** yield Z_O = 69.4 Ω and t_{PD} = 0.144 ns/in C_O is then calculated as 2.075 pF/in. If it is assumed that an MC88100 or 88200 clock input load is 15 pF, and that two of these loads, in addition to a 7 pF FAST TTL load, are distributed along a 9.6 in clock trace,

$$C_d = (2 \times 15 + 7)\text{pF}/9.6 \text{ in} = \text{pF/in}.$$

The loaded trace propagation delay and characteristic impedance are then calculated as

$$t_{PD}' = 0.243 \text{ ns/in and } Z_O' = 41\ \Omega.$$

Looking at trace C in **Figure 2**, the two MC88200's are approximately 3 inches apart. Using the calculated value of t_{PD}', the clock signal skew due to the trace is about 0.7 ns. Since these two devices are on the same trace, this is the total clock

skew between these devices. Upon careful inspection of all the clock traces, it can be seen that clock signal skew was accounted for and minimized on this board layout. The longest distance between any 88 K devices on a single clock trace is about 4.5 inches, which translates to approximately 1.1 ns of skew. The two 88 K devices farthest away from the clock driver (traces a and c), are located at almost exactly the same distance along their respective traces, making the clock skew between them the 1 ns guaranteed from output to output of the clock driver. This means that the worst case clock skew between any two devices on this board is approximately 2.1 ns, which at 33 MHz is 7% of the period. Without careful attention to matching the clock traces on the board, this number could easily exceed 3 ns and the 10% cut-off point, even if a low skew clock driver is used.

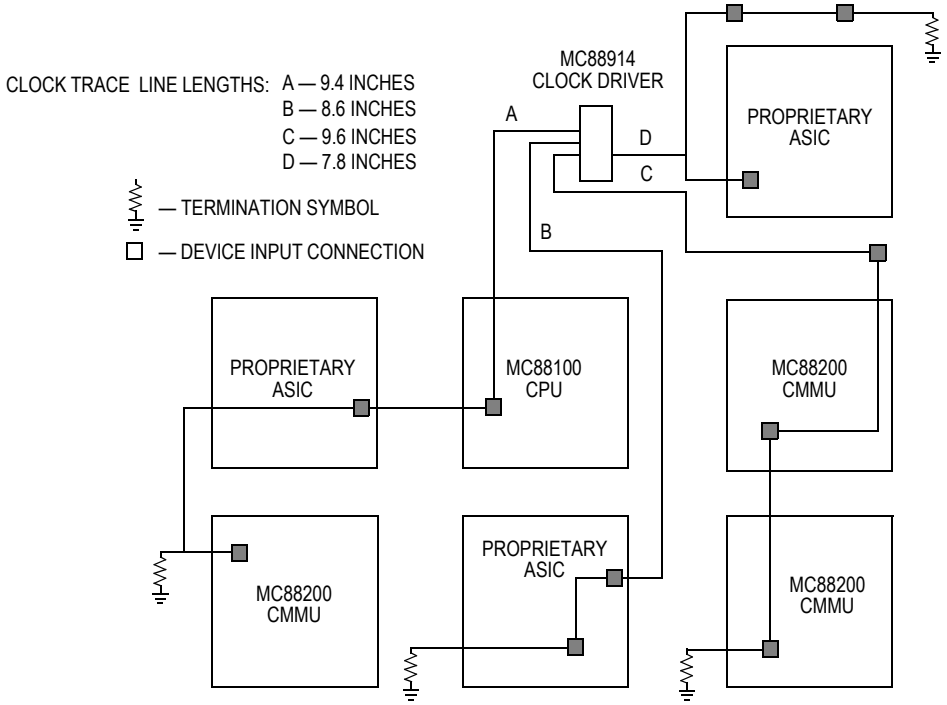
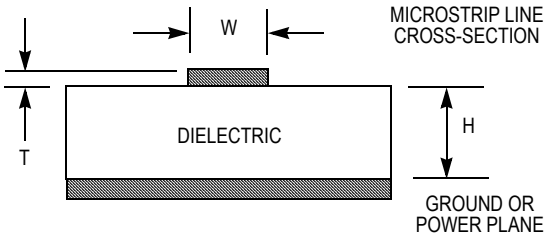


Figure 2. Scale Representation of an Actual 88000 System PCB Layout
(Only sections of the board related to the clock driver outputs are shown.)



$$Z_O = \frac{87}{\sqrt{e_r + 1.41}} \ln\left(\frac{5.98h}{0.8w + t}\right)$$

$$t_{PD} = 1.017 \sqrt{0.475\, e_r + 0.67}\ \text{ns/ft}$$

WHERE:
e_r = Relative Dielectric Constant of the Board Material
w, h, t = Dimensions Indicated in a Microstrip Diagram

Figure 3. Formulas for the Characteristic Impedance and Propagation Delay of a Microstrip Line (Ref. 1)

CLOCK SIGNAL TERMINATIONS

Transmission line effects occur when a large mismatch is present between the characteristic impedance of the line and the input or output impedances of the receiving or driving device. The basic guidelines used to determine if a PCB trace needs to be examined for transmission line effects is that if the smaller of the driving device's rise or fall time is less than three times the propagation delay of a switching wave through a trace, the transmission line effects will be present.[2] This relationship can be stated in equation form as:[3]

$$3 \text{ X } t_{PD}' \text{ X trace length} \leq t_{RISE} \text{ or } t_{FALL}$$

For the MC88914 CMOS clock driver described in this article, rise and fall times are typically 1.5 ns or less (from 20% to 80% of V_{CC}). Analyzing the clock trace characteristics presented earlier for transmission line effects, 3 x 0.243 ns/in x trace length ≤1 ns (1 ns is used as 'fastest' rise or fall time). Therefore the trace length must be less than 1.5 inches for the transmission line effects to be masked by the rise and fall times.

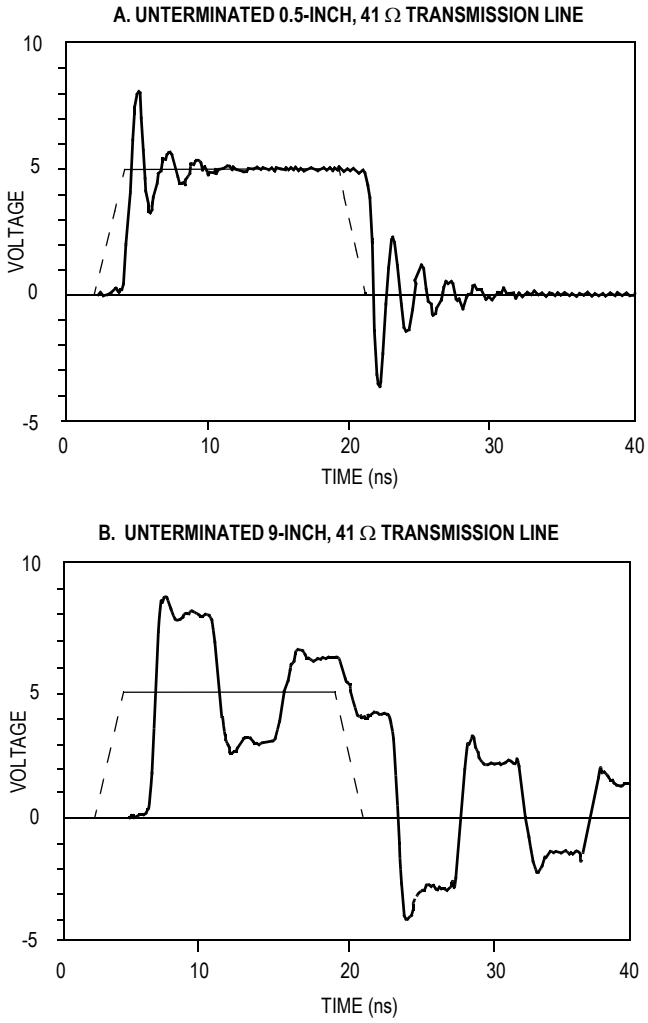


Figure 4. SPICE Simulation Results of 'Short' and 'Long' Transmission Lines. Simulations Were Run with Typical Parameters @ 25°C and V_{CC} = 5.0 V

Figure 4 shows the clock signal waveform seen at the receiver end of an unterminated 0.5 inch trace and an unterminated 9 inch trace. These results were obtained using SPICE simulations, which may not be exact, but are adequate to predict trends and for comparison purposes. The 9 inch trace, which is well beyond the 1.5 inch limit where transmission line effects come into play, exhibits unacceptable switching characteristics caused by reflections going back and forth on the trace. Even the 0.5 inch line exhibits substantial overshoot and undershoot. Any unterminated line will exhibit some overshoot and undershoot at these edge rates.

Clock lines shorter than 1–1.5 inches are unrealistic on a practical board layout, therefore it is recommended that CMOS clock lines be terminated if the driver has 1–2 ns edge rates. Termination, which is used to more closely match the line to the load or source impedances, has been a fact of life in the ECL world for many years (reference 1 is an excellent source for transmission line theory and practice in ECL systems), but CMOS and TTL devices have only recently reached the speeds and edge rates which require termination. CMOS outputs further complicate the issue by driving from rail to rail (5 V), with slew rates exceeding those of high performance ECL devices.

Since clock lines are only driven from a single location, they lend themselves to termination more easily than bus lines which are commonly driven from multiple locations. Termination of bus lines with multiple drivers is a complicated manner which will not be addressed in this article. The most common types of termination in digital systems are shown in Figure 5. Since no single termination scheme is optimal in all cases, the tradeoffs involving the use of each will be discussed, and recommendations specific to clock drivers will be made. Reference 2 is a comprehensive and practical treatment of transmission line theory and analysis of CMOS signals, and is recommended reading for those who want to gain a better understanding of transmission lines. Figure 6 shows SPICE simulated waveforms of the different termination schemes to be discussed. The driving device in the simulations was the MC88914 output buffer; in all simulations it drove a 9 inch 41 Ω transmission line. The simulations were run using typical model parameters at 25°C and V_{CC} = 5 V.

Series termination, depicted in Figure 5b, is recommended if the load is lumped at the end of the trace and the output impedance of the driving device is less than the loaded characteristic impedance of the trace, or when a minimum number of components is required. The main problem with series termination occurs when the driving device has different output impedance values in the low and high states, which is a problem in TTL and some CMOS devices. A well designed CMOS clock driver should have nearly equal output impedances in the high and low states, avoiding this problem. An additional advantage is that series termination does not create a DC current path, thus the V_{OL} and V_{OH} levels are not degraded. The SPICE generated waveforms of series termination in Figure 6a show that series termination effectively masks the transmission line effects exhibited in Figure 4. If each clock output is driving only one device, series termination would be recommended, but this is not a realistic case in most systems, so series termination is not generally recommended for termination of clock lines.

Parallel termination utilizes a single resistor tied to ground or V_{CC} whose value is equal to the characteristic impedance of the line. Its major disadvantage is the DC current path it creates when the driver is in the high state (if the resistor is tied to ground). This causes excessive power dissipation and V_{OH} level degradation. Since a clock driver output is always switching, the DC current draw argument loses some credibility at higher frequencies because the AC switching current becomes a major component of the overall current. Therefore the main consideration in parallel termination is how much V_{OH} degradation can be tolerated by the receiving devices. **Figure 6**b demonstrates that this termination technique is effective in minimizing the switching noise, but Thevenin termination has some advantages over parallel termination.

Thevenin termination utilizes one resistor tied to ground and a second tied to V_{CC}. An important consideration when using this type of termination is choosing the resistor values to avoid settling of the voltage between the high and low logic levels of the receiving device.[2] TTL designers commonly use a 220/330 resistor value ratio, but CMOS is a little tricky because the switch point is at $V_{CC}/2$. With a 1:1 resistor ratio a failure at the driver output would cause the line to settle at 2.5 V, causing system debug problems and also potential damage to the receiving devices.

In Thevenin termination, the parallel equivalent value of the two resistors should be equal to the characteristic impedance of the line. A DC path does exist in both the high and low states, but it is not as bad as parallel termination because the resistance in the Thevenin DC path is at least 2 times greater.

Figure 6c shows the termination waveforms, which exhibit characteristics similar to parallel termination, but with less V_{OH} degradation. The only real advantage of parallel over Thevenin is less resistors (1/2 as many) and less space taken up on the board by the resistors. If this is not a factor, Thevenin termination is recommended over parallel.

AC termination, shown in **Figure 5**e, normally utilizes a resistor and capacitor in series to ground. The capacitor blocks DC current flow, but allows the AC signal to flow to ground during switching. The RC time constant of the resistor and capacitor must be greater than twice the loaded line delay. AC termination is recommended because of its low power dissipation and also because of the availability of the resistor and capacitor in single- in-line packages (SIP). A pullup resistor to V_{CC} is sometimes added to set the DC level at a certain point because of the failure condition described in regards to Thevenin termination. As discussed earlier, the argument of lower DC current is less convincing at high frequencies. The AC terminated waveform walks out slightly toward the end of a high-to-low or low-to-high transition as seen in **Figure 6**d, making it slightly less desirable than Thevenin termination.

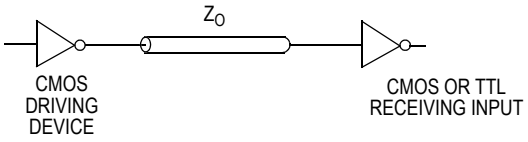
Thevenin and AC termination are the two recommended termination schemes for clock lines, but it depends on what frequency the clock is running at when making a decision between these types of termination. Although hard data is not provided to back this statement up, it is a safe assumption that at frequencies of 25 MHz and below AC is the best choice. If the system frequency could reach 40 MHz and beyond, Thevenin becomes the better choice.

ADDITIONAL CONSIDERATIONS WHEN TERMINATING CLOCK LINES

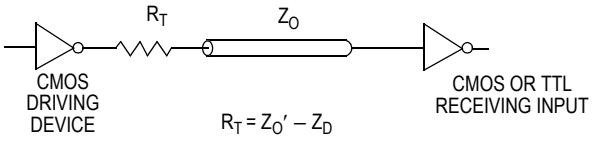
The results presented might imply that terminating the clock lines will completely solve noise problems, but termination can cause secondary problems with some logic devices. Termination acts to reduce the noise seen at the receiver, but that noise actually is seen as additional current and noise at the output of the driving device. If the internal and input logic on the source device is not sufficiently decoupled on chip from the high current outputs, internal threshold problems can occur. This phenomenon is commonly known as ‘dynamic threshold.’ It is usually evidenced by glitches appearing on the outputs of a fast, high current drive logic device as it switches high or low. This is most severe on ‘ACT’ devices which have high current and high slew rate CMOS outputs along with TTL inputs which have low noise immunity. This problem can be minimized by decoupling the internal ground and V_{CC} supplies on-chip and in the package. This decoupling is accomplished by having separate ‘quiet' ground and V_{CC} pads on chip which supply the input circuitry's ground and V_{CC} references. These pads are then tied to extra ‘quiet’ ground and ‘quiet’ V_{CC} pins on the package, or to special ‘split leads’ which resemble a tuning fork and utilize the leadframe inductance to accomplish the decoupling. When choosing a clock source, make sure that the part has one of these decoupling schemes.

References

1. Blood, William R., *MECL System Design Handbook*, Motorola Inc., 1983.
2. Application Note AN1051, *Transmission Line Effects in PCB Applications*, Motorola Inc., 1990.
3. *Motorola FACT Data Book* DL138, Motorola Inc., 1990.

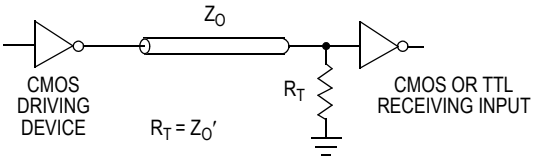


A. TRANSMISSION LINE WITH NO TERMINATION

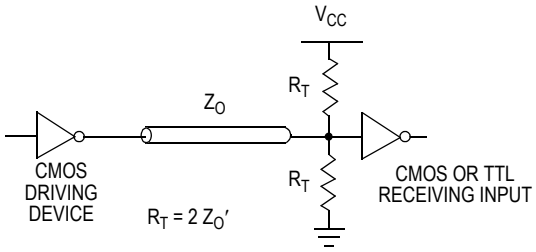


WHERE, Z_D = DRIVING DEVICE OUTPUT IMPEDANCE

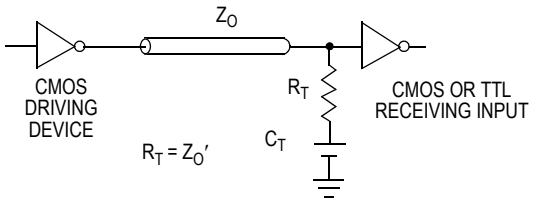
B. TRANSMISSION LINE WITH SERIES TERMINATION



C. TRANSMISSION LINE WITH PARALLEL TERMINATION



D. TRANSMISSION LINE WITH THEVENIN TERMINATION



E. TRANSMISSION LINE WITH AC TERMINATION

Figure 5. Schematic Representation of Common Termination Techniques

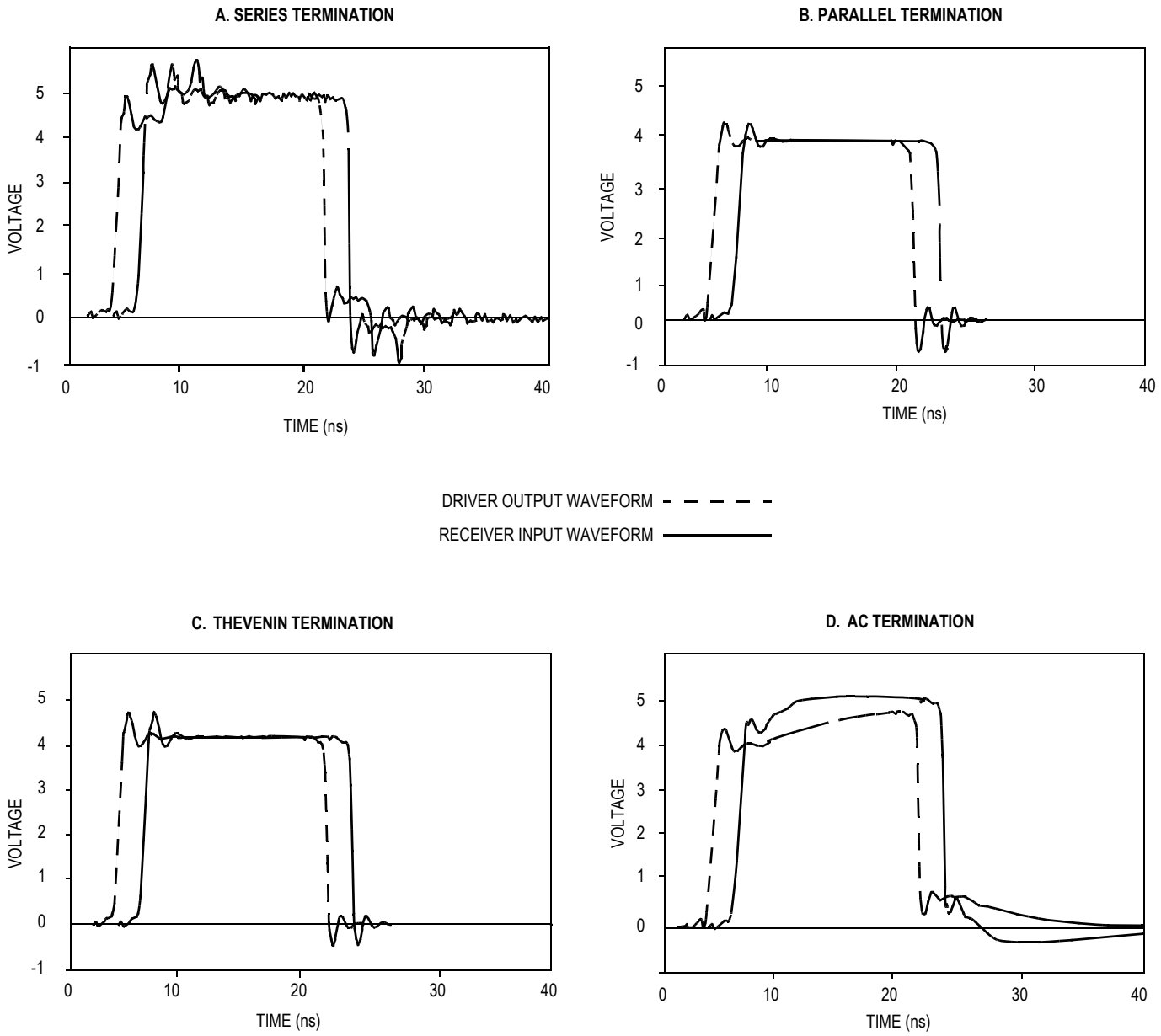


Figure 6. SPICE Simulation Results for Various Terminations of a 9-Inch 41 Ω transmission Line.
(Simulations Were Run with Typical Model Parameters @ 25°C and V_{CC} = 5.0 V)

Order number: AN1405
Rev 1, 09/2001

AN1405

ECL Clock Distribution Techniques

By: Todd Pearson
ECL Applications Engineering

ABSTRACT

This application note provides information on system design using ECL logic technologies for reducing system clock skew over the alternative CMOS and TTL technologies.

INTRODUCTION

The ever increasing performance requirements of today's systems has placed an even greater emphasis on the design of low skew clock generation and distribution networks. Clock skew, the difference in time between “simultaneous” clock transitions within a system, is a major component of the constraints which form the upper bound for the system clock frequency. Reductions in system clock skew allow designers to increase the performance of their designs without having to resort to more complicated architectures or more costly, faster logic. ECL logic technologies offer a number of advantages for reducing system clock skew over the alternative CMOS and TTL technologies.

SKEW DEFINITIONS

The skew introduced by logic devices can be divided into three parts: duty cycle skew, output-to-output skew and part-to-part skew. Depending on the specific application, each of the three components can be of equal or overriding importance.

Duty Cycle Skew

The duty cycle skew is a measure of the difference between the T_{PLH} and T_{PHL} propagation delays (**Figure 1**). Because differences in T_{PLH} and T_{PHL} will result in pulse width distortion the duty cycle skew is sometimes referred to as pulse skew. Duty cycle skew is important in applications where timing operations occur on both edges or when the duty cycle of the clock signal is critical. The later is a common requirement when driving the clock inputs of advanced microprocessors.

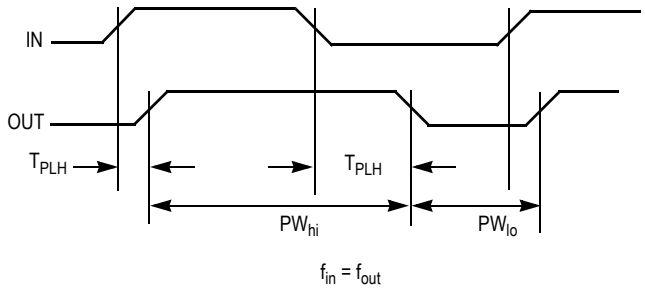


Figure 1. Duty Cycle Skew

Output-to-Output Skew

Output-to-output skew is defined as the difference between the propagation delays of all the outputs of a device. A key constraint on this measurement is the requirement that the output transitions are identical, therefore if the skew between all edges produced by a device is important the output-to-output skew would need to be added to the duty cycle skew to get the total system skew. Typically the output-to-output skew will be smaller than the duty cycle skew for TTL and CMOS devices. Because of the near zero duty cycle skew of a differential ECL device the output-to-output skew will generally be larger. The output-to-output skew is important in systems where either a single device can provide all of the necessary clocks or for the first level device of a nested clock distribution tree. In these two situations the only parameter of importance will be the relative position of each output with respect to the other outputs on that die. Since these outputs will all see the same environmental and process conditions the skew will be significantly less than the propagation delay windows specified in the standard device data sheet.

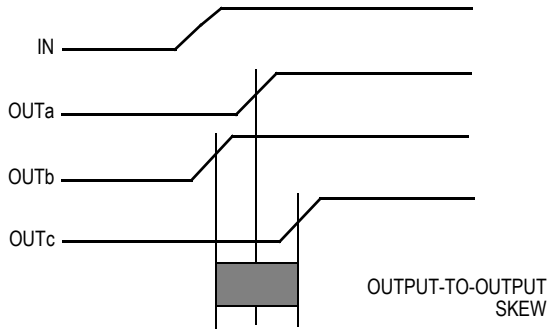


Figure 2. Output-to-Output Skew

Part-to-Part Skew

The part-to-part skew specification is by far the most difficult performance aspect of a device to minimize. Because the part-to-part skew is dependent on both process variations and variations in the environment the resultant specification is significantly larger than for the other two components of skew. Many times a vendor will provide subsets of part-to-part skew specifications based on non-varying environmental conditions. Care should be taken in reading data sheets to fully understand the conditions under which the specified limits are guaranteed. If the part-to-part skew is specified and is different than the specified propagation delay window for the device one can be assured there are constraints on the part-to-part skew specification.

Power supply and temperature variations are major contributors to variations in propagation delays of silicon devices. Constraints on these two parameters are commonly seen in part-to-part skew specifications. Although there are situations where the power supply variations could be ignored, it is difficult for this author to perceive of a realistic system whose devices are all under identical thermal conditions. Hot spots on boards or

cabinets, interruption in air flow and variations in IC density of a board all lead to thermal gradients within a system. These thermal gradients will guarantee that devices in various parts of the system are under different junction temperature conditions. Although it is unlikely that a designer will need the entire commercial temperature range, a portion of this range will need to be considered. Therefore, a part-to-part skew specified for a single temperature is of little use, especially if the temperature coefficient of the propagation delay is relatively large.

For designs whose clock distribution networks lie on a single board which utilizes power and ground planes an assumption of non-varying power supplies would be a valid assumption and a specification limit for a single power supply would be valuable. If, however, various pieces of the total distribution tree will be on different boards within a system there is a very real possibility that each device will see different power supply levels. In this case a specification limit for a fixed V_{CC} will be inadequate for the design of the system. Ideally the data sheets for clock distribution devices should include information which will allow designers to tailor the skew specifications of the device to their application environment.

SYSTEM ADVANTAGES OF ECL

Skew Reductions

ECL devices provide superior performance in all three areas of skew over their TTL or CMOS competitors. A skew reducing mechanism common to all skew parameters is the faster propagation delays of ECL devices. Since, to some extent, all skew represent a percentage of the typical delays faster delays will usually mean smaller skews. ECL devices, especially clock distribution devices, can be operated in either single-ended or differential modes. To minimize the skew of these devices the differential mode of operation should be used, however even in the single-ended mode the skew performance will be significantly better than for CMOS or TTL drivers.

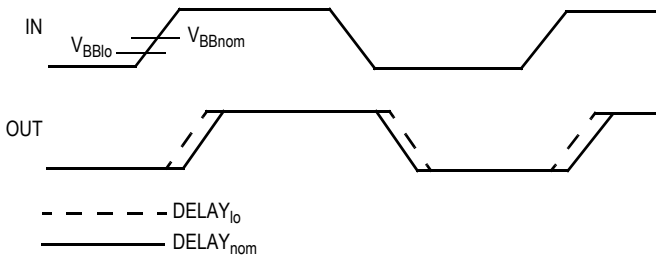


Figure 3. V_{BB} Induced Duty Cycle Skew

ECL output buffers inherently show very little difference between T_{PLH} and T_{PHL} delays. What differences one does see are due mainly to switching reference levels which are not ideally centered in the input swing (see **Figure 3**). For worst case switching reference levels the pulse skew of an ECL device will still be less than 300 ps. If the ECL device is used differentially the variation in the switching reference will not impact the duty cycle skew as it is not used. In this case the pulse skew will be less than 50 ps and can generally be ignored in all but the highest performance designs. The problem of generating clocks which are capable of meeting the duty cycle requirements of the most advanced microprocessors, would be a trivial task if differential ECL compatible clock inputs were used. TTL and CMOS clock drivers on the other hand have inherent differences between the T_{PLH} and T_{PHL} delays in addition to the problems with non-centered switching thresholds. In devices specifically designed to minimize this parameter it generally cannot be guaranteed to anything less than 1 ns.

The major contributors to output-to-output skew is IC layout and package choice. Differences in internal paths and paths through the package generally can be minimized regardless of the silicon technology utilized at the die level, therefore ECL devices offer less of an advantage in this area than for other skew parameters. CMOS and TTL output performance is tied closely to the power supply levels and the stability of the power busses within the chip. Clock distribution trees by definition always switch simultaneously, thus creating significant disturbances on the internal power busses. To alleviate this problem multiple power and ground pins are utilized on TTL and CMOS clock distribution devices. However even with this strategy TTL and CMOS clock distribution devices are limited to 500 ps – 700 ps output-to-output skew guarantees. With differential ECL outputs very little if any noise is generated and coupled onto the internal power supplies. This coupled with the faster propagation delays of the output buffers produces output-to-output skews on ECL clock chips as low as 50 ps.

Two aspects of ECL clock devices will lead to significantly smaller part-to-part skews than their CMOS and TTL competitors: faster propagation delays and delay insensitivity to environmental variations. Variations in propagation delays with process are typically going to be based on a percentage of the typical delay of the device. Assuming this percentage is going to be approximately equivalent between ECL, TTL and CMOS processes, the faster the device the smaller the delay variations. Because state-of-the-art ECL devices are at least 5 times faster than TTL and CMOS devices, the expected delay variation would be one fifth those of CMOS and TTL devices without even considering environmental dependencies.

The propagation delays of an ECL device are insensitive to variations in power supply while CMOS and TTL device propagation delays vary significantly with changes in this parameter. Across temperature the percentage variation for all technologies is comparable, however, again the faster propagation delays of ECL will reduce the magnitude of the variation. **Figure 4** on the following page represents normalized propagation delay versus temperature and power supply for the three technologies.

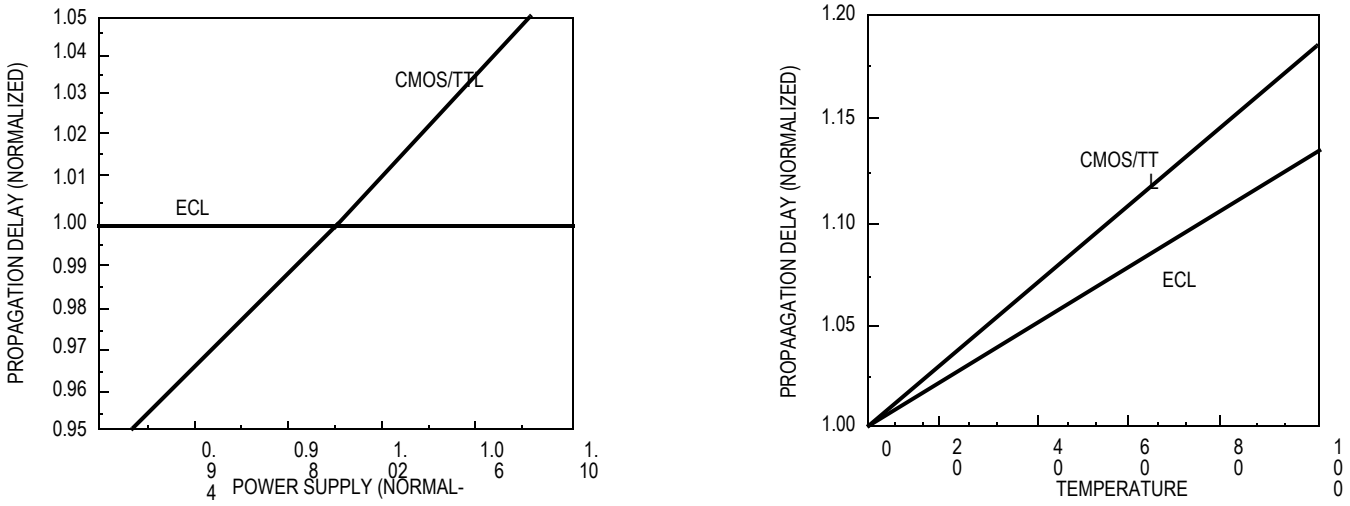


Figure 4. T_{PD} vs Environmental Condition Comparison

Low Impedance Line Driving

The clock requirements of today's systems necessitate an almost exclusive use of controlled impedance interconnect. In the past this requirement was unique to the performance levels associated with ECL technologies, and in fact precluded its use in all but the highest performance systems. However the high performance CMOS and TTL clock distribution chips now require care in the design and layout of PC boards to optimize their performance, with this criteria established the migration from these technologies to ECL is simplified. In fact, the difficulties involved in designing with these “slower” technologies in a controlled impedance environment may even enhance the potential of using ECL devices as they are ideally suited to the task.

The low impedance outputs and high impedance inputs of an ECL device are ideal for driving 50 Ω to 130 Ω controlled impedance transmission lines. The specified driving impedance of ECL is 50 Ω, however this value is used only for convenience sake due to the 50 Ω impedance of most commonly used measurement equipment. Utilizing higher impedance lines will reduce the power dissipated by the termination resistors and thus should be considered in power sensitive designs. The major drawback of higher impedance lines (delays more dependent on capacitive loading) may not be an issue in the point to point interconnect scheme generally used in low skew clock distribution designs.

Differential Interconnect

The device skew minimization aspects of differential ECL have already been discussed however there are other system level advantages that should be mentioned. Whenever clock lines are distributed over long distances the losses in the line and the variations in power supply upset the ideal relationship between input voltages and switching thresholds. Because differential interconnect “carries” the switching threshold information from the source to the load the relationship between the two is less likely to be changed. In addition for long lines the smaller swings of an ECL device produce much lower levels of cross-talk between adjacent lines and minimizes EMI radiation from the PC board.

There is a cost associated with fully differential ECL, more pins for equivalent functions and more interconnect to be laid on a typically already crowded PC board. The first issue is really a non-issue for clock distribution devices. The output-to-output and duty cycle skew are very much dependent on quiet internal power supplies. Therefore the pins sacrificed for the complimentary outputs would otherwise have to be used as power supply pins, thus functionality is actually gained for an equivalent pin count as the inversion function is also available on a differential device. The presence of the inverted signal could be invaluable for a design which clocks both off the positive and negative edges. **Figure 5** shows a method of obtaining very low skew (<50 ps) 180° shifted two phase clocks.

It is true that differential interconnect requires more signals to be routed on the PC board. Fortunately with the wide data and address buses of today's designs the clock lines represent a small fraction of the total interconnect. The final choice as to whether or not to use differential interconnect lies in the level of skew performance necessary for the design. It should be noted that although single-ended ECL provides less attractive skew performance than differential ECL, it does provide significantly better performance than equivalent CMOS and TTL functions.

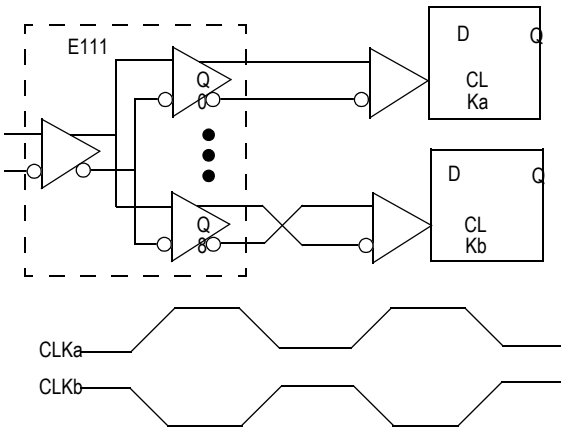


Figure 5. 180° Shifted Two Phase Clocks

USING ECL WITH POSITIVE SUPPLIES

It is hard to argue with the clock distribution advantages of ECL presented thus far, but it may be argued that except for all ECL designs it is too costly to include ECL devices in the distribution tree. This claim is based on the assumption that at least two extra power supplies are required; the negative V_{EE} supply and the negative V_{TT} termination voltage. Fortunately both these assumptions are false. PECL (Positive ECL) is an acronym which describes using ECL devices with a positive rather than negative power supply. It is important to understand that all ECL devices are also PECL devices. By using ECL devices as PECL devices on a +5 volt supply and incorporating termination techniques which do not require a separate termination voltage (series termination, thevenin equivalent) ECL can be incorporated in a CMOS or TTL design with no added cost.

The reason for the choice of negative power supplies as standard for ECL is due to the fact that all of the output levels and internal switching bias levels are referenced to the V_{CC} rail. It is generally easier to keep the grounds quieter and equal potential throughout a system than it is with a power supply. Because the DC parameters are referenced to the V_{CC} rail any disturbances or voltage drops seen on V_{CC} will translate 1:1 to the output and internal reference levels. For this reason when communicating with PECL between two boards it is recommended that only differential interconnect be used. By using differential interconnect V_{CC} variations within the specified range will not in any way affect the performance of the device.

Finally mentioning ECL to a CMOS designer invariably conjures up visions of space heaters as their perception of ECL is high power. Although it is true that the static power of ECL is higher than for CMOS the dynamic power differences between the technologies narrows as the frequency increases. As can be seen in **Figure 6** at frequencies as low as 20 MHz the per gate power of ECL is actually less than for CMOS. Since clock distribution devices are never static it does not make sense to compare the power dissipation of the two technologies in a static environment.

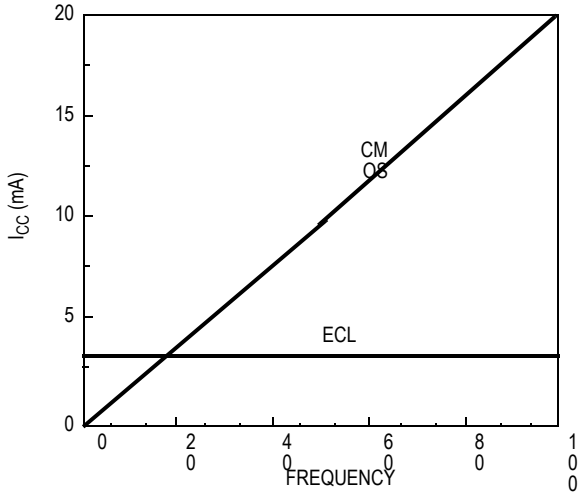


Figure 6. I_{CC}/Gate vs Frequency Comparison

MIXED SIGNAL CLOCK DISTRIBUTION

ECL Clock Distribution Networks

Clock distribution in a ECL system is a relatively trivial matter. **Figure 7** illustrates a two level clock distribution tree which produces nine differential ECL clocks on six different cards. The ECLinPS E211 device gives the flexibility of disabling each of the cards individually. In addition the synchronous registered enables will disable the device only when the clock is already in the LOW state, thus avoiding the problem of generating runt pulses when an asynchronous disable is used. The device also provides a muxed clock input for incorporating a high speed system clock and a lower speed test or scan clock within the same distribution tree. The ECLinPS E111 device is used to receive the signals from the backplane and distribute it on the card. The worst case skew between all 54 clocks in this situation would be 275 ps assuming that all the loads and signal traces are equalized.

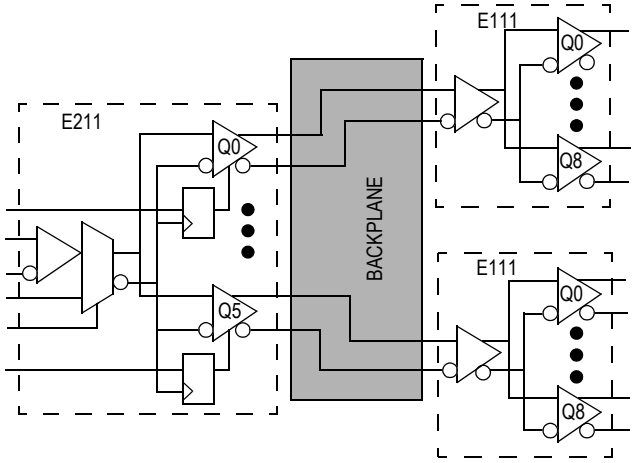


Figure 7. ECL Clock Distribution Tree

Mixed Technology Distribution Networks

Building clock networks in TTL and CMOS systems can be a little more complicated as there are more alternatives available. For simple one level distribution trees fanout devices like the MECL 10H645 1:9 TTL to TTL fanout tree can be used. However as the number of levels of fanout increases the addition of ECL devices in an other wise TTL or CMOS system becomes attractive. In **Figure 8** on the next page an E111 device is combined with a MECL H641 device to produce 81 TTL level clocks. Analyzing the skew between the 81 clocks yields a worst case skew, allowing for the full temperature and V_{CC} range variation, of 1.25 ns. Under ideal situations, no variation in temperature or V_{CC} supply, the skew would be only 750 ps. When compared with distribution trees utilizing only TTL or CMOS technologies these numbers represent ≈50% improvement, more if the environmental conditions vary to any degree. For a 50 MHz clock the total skew between the 81 TTL clocks is less than 6.5% of the clock period, thus providing the designer extra margin for layout induced skew to meet the overall skew budget of the design.

Many designers have already realized the benefits of ECL clock distribution trees and thus are implementing them in their designs. Furthermore where they have the capability, i.e. ASICs, they are building their VLSI circuits with ECL compatible clock inputs. Unfortunately other standard VLSI circuits such as microprocessors, microprocessor support chips and memory still cling to TTL or CMOS clock inputs. As a result many systems need both ECL and TTL clocks within the same system. Unlike the situation outlined in **Figure 8** the ECL levels are not merely intermediate signals but rather are driving the clock inputs of the logic. As a result the ECL edges need to be matched with the TTL edges as pictured in **Figure 9**.

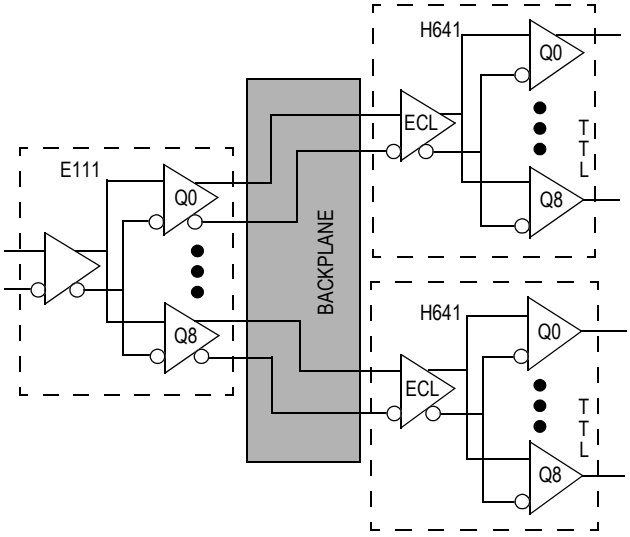


Figure 8. ECL to TTL Clock Distribution

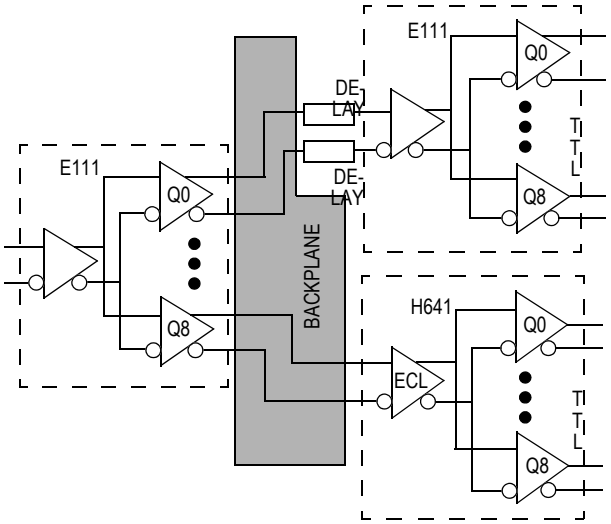


Figure 9. Mixed ECL and TTL Distribution

An ECL clock driver will be significantly faster than a TTL or CMOS equivalent function. Therefore to de-skew the ECL and TTL signals of **Figure 9** a delay needs to be added to the input of the ECL device. Because a dynamic delay adjust would not lend itself to most production machines a static delay would be used. The value of the delay element would be a best guess estimate of the differences in the two propagation delays. It is highly unlikely that the temperature coefficients of the propagation delays of the ECL devices, TTL devices and delay devices would be equal. Although these problems will add skew to the system, the resultant total skew of the distribution network will be less than if no ECL chips were used.

PLL Based Clock Drivers

A potential solution for the problem outlined in **Figure 9** is in the use of phase locked loop based clock distribution chips. Because these devices feedback an output and lock it to a reference clock input the delay differences between the various technology output buffers will be eliminated. One might believe that with all of the euphoria surrounding the performance of PLL based clock distribution devices that the need for any ECL in the distribution tree will be eliminated. However when analyzed further the opposite appears to be the case.

For a single board design with a one level distribution system there obviously is no need for ECL. When, however, a multiple board system is required where nested levels of devices are needed ECL once again becomes useful. One major aspect of part-to-part skew for PLL based clock chips often overlooked is the dependence on the skew of the various reference clocks being locked to. As can be seen in **Figure 10** the specified part-to-part skew of the device would necessarily need to be added to the reference clock skew to get the overall skew of the clock tree. From the arguments presented earlier this skew will be minimized if the reference clock is distributed in ECL. It has not been shown as of yet where a PLL based ECL clock distribution chip can provide the skew performance of the simple fanout buffer. From a system standpoint the buffer type circuits are much easier to design with and thus given equivalent performance would represent the best alternative. The extra features provided by PLL based chips could all be realized if they were used in only the final stage of the distribution tree.

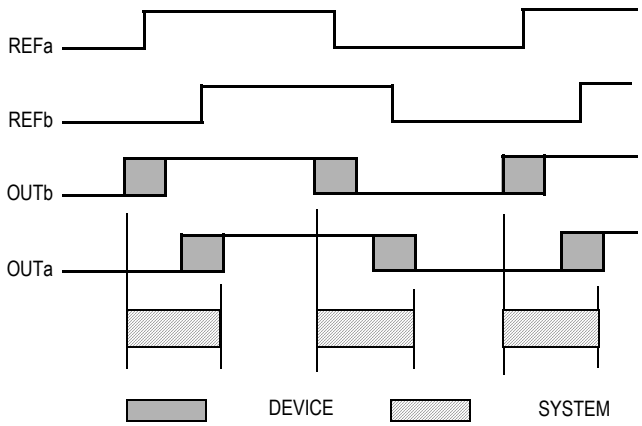


Figure 10. System Skew for PLL Clock Distribution

The MPC973 is a PLL based clock driver which features differential PECL reference clock inputs. When combined with the very low skew MC10E111 fanout buffer, very low skew clock trees can be realized for multiprocessor MPP designs. There will be a family of devices featuring various technology compat-

ible inputs and outputs to allow for the building of precisely aligned clock trees based on either ECL, TTL, CMOS or differential GTL (or a mixture of all four) compatible levels.

CONCLUSION

The best way to maximize the performance of any synchronous system is to spend the entire clock period performing value added operations. Obviously any portion of the clock period spent idle due to clock skew limits the potential performance of the system. Using ECL technology devices in clock distribution networks will minimize all aspects of skew and thus maximize the performance of a system. Unfortunately the VLSI world is not yet ECL clock based so that the benefits of a totally ECL based distribution tree cannot be realized for many systems. However there are methods of incorporating ECL into the intermediate levels of the tree to significantly reduce the overall skew. In addition the system designers can utilize their new found knowledge to incorporate ECL compatible clocks on those VLSI chips of which they have control while at the same time pressuring other VLSI vendors in doing the same so that future designs can enjoy fully the advantages of distributing clocks with ECL.

AN1406

Designing With PECL (ECL at +5.0 V)
The High Speed Solution for the CMOS/TTL Designer

By: Cleon Petty, Todd Pearson
ECL Applications Engineering

ABSTRACT

This application note provides detailed information on designing with Positive Emitter Coupled Logic (PECL) devices.

INTRODUCTION

PECL, or Positive Emitter Coupled Logic, is nothing more than standard ECL devices run off of a positive power supply. Because ECL, and therefore PECL, has long been the “black magic” of the logic world many misconceptions and falsehoods have arisen concerning its use. However, many system problems which are difficult to address with TTL or CMOS technologies are ideally suited to the strengths of ECL. By breaking through the wall of misinformation concerning the use of ECL, the TTL and CMOS designers can arm themselves with a powerful weapon to attack the most difficult of high speed problems.

It has long been accepted that ECL devices provide the ultimate in logic speed; it is equally well known that the price for this speed is a greater need for attention to detail in the design and layout of the system PC boards. Because this requirement stems only from the speed performance aspect of ECL devices, as the speed performance of any logic technology increases these same requirements will hold. As can be seen in **Table 1** the current state-of-the-art TTL and CMOS logic families have attained performance levels which require controlled impedance interconnect for even relatively short distances between source and load. As a result system designers who are using state-of-the-art TTL or CMOS logic are already forced to deal with the special requirements of high speed logic; thus it is a relatively small step to extend their thinking from a TTL and CMOS bias to include ECL devices where their special characteristics will simplify the design task.

Table 1. Relative Logic Speeds

Logic Family	Typical Output Rise/Fall	Maximum Open Line Length (L_{max}) [1]
10KH	1.0 ns	3"
ECLinPS	400 ps	1"
FAST	2.0 ns	6"
FACT	1.5 ns	4"

[1] Approximate for stripline interconnect ($L_{max} = T_r/2T_{pd}$)

SYSTEM ADVANTAGES OF ECL

The most obvious area to incorporate ECL into an otherwise CMOS/TTL design would be for a subsystem which requires very fast data or signal processing. Although this is the most obvious it may also be the least common. Because of the need for translation between ECL and CMOS/TTL technologies the performance gain must be greater than the overhead required to translate back and forth between technologies. With typical delays of six to seven nanoseconds for translating between technologies, a significant portion of the logic would need to be realized using ECL for the overall system performance to improve. However, for very high speed subsystem requirements ECL may very well provide the best system solution.

Transmission Line Driving

Many of the inherent features of an ECL device make it ideal for driving long, controlled impedance lines. The low impedance of the open emitter outputs and high input impedance of any standard ECL device make it ideally suited for driving controlled impedance lines. Although designed to drive 50 Ω lines an ECL device is equally adept at driving lines of impedances of up to 130 Ω without significant changes in the AC characteristics of the device. Although some of the newer CMOS/TTL families have the ability to drive 50 Ω lines many require special driver circuits to supply the necessary currents to drive low impedance transmission interconnect. In addition the large output swings and relatively fast output slew rates of today's high performance CMOS/TTL devices exacerbate the problems of crosstalk and EMI radiation. The problems of crosstalk and EMI radiation, along with common mode noise and signal amplitude losses, can be alleviated to a great degree with the use of differential interconnect. Because of their architectures, neither CMOS nor TTL devices are capable of differential communication. The differential amplifier input structure and complimentary outputs of ECL devices make them perfectly suited for differential applications. As a result, for systems requiring signal transmission between several boards, across relatively large distances, ECL devices provide the CMOS/TTL designer a means of ensuring reliable transmission while minimizing EMI radiation and crosstalk.

Figure 1 shows a typical application in which the long line driving, high bandwidth capabilities of ECL can be utilized. The majority of the data processing is done on wide bit width words with a clock cycle commensurate with the bandwidth capabilities of CMOS and TTL logic. The parallel data is then serialized into a high bandwidth data stream, a bandwidth which requires ECL technologies, for transmission across a long line to another box or machine. The signal is received differentially and converted back to relatively low speed parallel data where it can be processed further in CMOS/TTL logic. By taking advantage of the bandwidth and line driving capabilities of ECL the system minimizes the number of lines required for interconnecting the subsystems without sacrificing the overall performance. Furthermore by taking advantage of PECL this application can be realized with a single five volt power supply. The configuration of **Figure 1** illustrates a situation where the mixing of logic technologies can produce a design which maximizes the overall performance while managing power dissipation and minimizing cost.

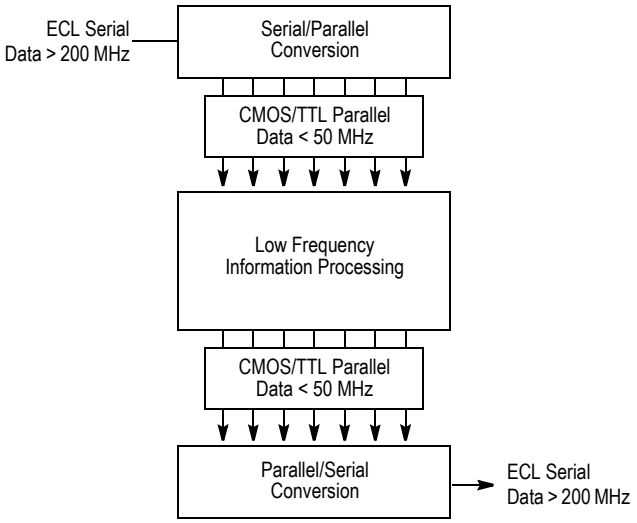


Figure 1. Typical Use of ECL's High Bandwidth, Line Driving Capabilities

Clock Distribution

Perhaps the most attractive area for ECL in CMOS/ TTL designs is in clock distribution. The ever increasing performance capabilities of today's designs has placed an even greater emphasis on the design of low skew clock generation and distribution networks. Clock skew, the difference in time between "simultaneous" clock transitions throughout an entire system, is a major component of the constraints which form the upper bound for the system clock frequency. Reductions in system clock skew allow designers to increase the performance of their designs without having to resort to more complicated architectures or costly, faster logic. ECL logic has the capability of significantly reducing the clock skew of a system over an equivalent design utilizing CMOS or TTL technologies.

The skew introduced by a logic device can be broken up into three areas; the part-to-part skew, the within-part skew and the rise-to-fall skew. The part-to-part skew is defined as the differences in propagation delays between any two devices while the within-device skew is the difference between the propagation delays of similar paths for a single device. The final portion of the device skew is the rise-to-fall skew or simply the differences in propagation delay between a rising input and a failing input on the same gate. The within-device skew and the rise-to-fall skew combine with delay variations due to environmental conditions and processing to comprise the part-to-part skew. The part-to-part skew is defined by the propagation delay window described in the device data sheets.

Careful attention to die layout and package choice will minimize within-device skew. Although this minimization is independent of technology, there are other characteristics of ECL which will further reduce the skew of a device. Unlike their CMOS/TTL counterparts, ECL devices are relatively insensitive to variations in supply voltage and temperature. Propagation delay variations with environmental conditions must be accounted for in the specification windows of a device. As a result because of ECLs AC stability the delay windows for a device will inherently be smaller than similar CMOS or TTL functions.

The virtues of differential interconnect in line driving have already been addressed, however the benefits of differential interconnect are even more pronounced in clock distribution. The propagation delay of a signal through a device is intimately tied to the switching threshold of that device. Any deviations of the threshold from the center of the input voltage swing will increase or decrease the delay of the signal through the device. This difference will manifest itself as rise-to-fall skew in the device. The threshold levels for both CMOS and TTL devices are a function of processing, layout, temperature and other factors which are beyond the control of the system level designer. Because of the variability of these switching references, specification limits must be relaxed to guarantee acceptable manufacturing yields. The level of relaxation of these specifications increases with increasing logic depth. As the depth of the logic within a device increases the input signal will switch against an increasing number of reference levels; each encounter will add skew when the reference level is not perfectly centered. These relaxed timing windows add directly to the overall system skew. Differential ECL, both internal and external to the die, alleviates this threshold sensitivity as a DC switching reference is no longer required. Without the need for a switching reference the delay windows, and thus system skew, can be significantly reduced while maintaining acceptable manufacturing yields.

What does this mean to the CMOS/TTL designer? It means that CMOS/TTL designers can build their clock generation card and backplane clock distribution using ECL. Designers will not only realize the benefits of driving long lines with ECL but will also be able to realize clock distribution networks with skew specs unheard of in the CMOS/TTL world. Many specialized functions for clock distribution are available from Motorola (MC10/100E111, MC10/100E211, MC10/100EL11). Care must be taken that all of the skew gained using ECL for clock distribution is not lost in the process of translating into CMOS/TTL levels. To alleviate this problem the MC10/100H646 can be used to translate and fanout a differential ECL input signal into TTL levels. In this way all of the fanout on the backplane can be done in ECL while the fanout on each card can be done in the CMOS/TTL levels necessary to drive the logic.

Figure 2 illustrates the use of specialized fanout buffers to design a CMOS/TTL clock distribution network with minimal skew. With 50ps output-to-output skew of the MC10/100E111 and 1ns part-to-part skew available on the MC10/100H646 or MC10/100H641, a total of 72 or 81 TTL clocks, respectively, can be generated with a worst case skew between all outputs of only 1.05 ns. A similar distribution tree using octal CMOS or TTL buffers would result in worst case skews of more than 6 ns. This 5 ns improvement in skew equates to about 50% of the up/down time of a 50 MHz clock cycle. It is not difficult to imagine situations where an extra 50% of time to perform necessary operations would be either beneficial or even a life saver. For more information about using ECL for clock distribution, refer to application note AN1405/D — ECL Clock Distribution Techniques.

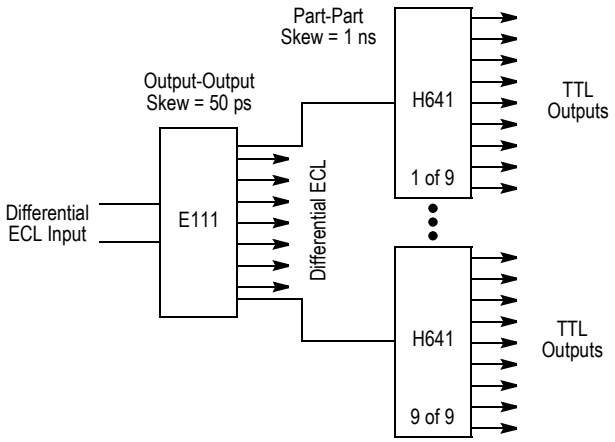


Figure 2. Low Skew Clock Fanout Tree

PECL VERSUS ECL

Nobody will argue that the benefits presented thus far are not attractive, however the argument will be made that the benefits are not enough to justify the requirements of including ECL devices in a predominantly CMOS/TTL design. After all the inclusion of ECL requires two additional negative voltage supplies; V_{EE} and the terminating voltage V_{TT}. Fortunately this is where the advantages of PECL come into play. By using ECL devices on a positive five volt CMOS/TTL power supply and using specialized termination techniques ECL logic can be incorporated into CMOS/TTL designs without the need for additional power supplies. What about power dissipation you ask, although it is true that in a DC state ECL will typically dissipate more power than a CMOS/TTL counterpart, in applications which operate continually at frequency, i.e. clock distribution, the disparity between ECL and CMOS/TTL power dissipation is reduced. The power dissipation of an ECL device remains constant with frequency while the power of a CMOS/TTL device will increase with frequency. As frequencies approach 50 MHz the difference between the power dissipation of a CMOS or TTL gate and an ECL gate will be minimal. 50 MHz clock speeds are becoming fairly common in CMOS/TTL based designs as today's high performance MPUs are fast approaching these speeds. In addition, because ECL output swings are significantly less than those of CMOS and TTL the power dissipated in the load will be significantly less under continuous AC conditions.

It is clear that PECL can be a powerful design tool for CMOS/TTL designers, but where can one get these PECL devices. Perhaps the most confusing aspect of PECL is the misconception that a PECL device is a special adaptation of an ECL device. In reality *every* ECL device is also a PECL device; there is nothing magical about the negative voltage supply used for ECL devices. The only real requirement of the power supplies is that the potential difference described in the device data sheets appears across the upper and lower power supply rails (V_{CC} and V_{EE} respectively). A potential stumbling block arises in the specified V_{EE} levels for the various ECL families. The 10 H and 100 K families specify parametric values for potential differences between V_{CC} and V_{EE} of 4.94 V to 5.46 V and 4.2 V to 4.8 V respectively; this poses a problem for the CMOS/TTL designer who works with a typical V_{CC} of 5.0 V ±5%. However, because both of these ECL standards are voltage compensated both families will operate perfectly fine and meet all of the performance specifications when operated on standard CMOS/TTL power supplies. In fact, Motorola is extending the V_{EE} specification ranges of many of their ECL families to be compatible with standard CMOS/TTL power supplies. Unfortunately earlier ECL families such as MECL 10 K™ are not voltage compensated and therefore any reduction in the potential difference between the two supplies will result in an increase in the V_{OL} level, and thus a decreased noise margin. For the typical CMOS/TTL power supplies a 10 K device will experience an ≈50 mV increase in the V_{OL} level. Designers should analyze whether this loss of noise margin could jeopardize their designs before implementing PECL formatted 10 K using 5.0 V ± 5% power supplies.

The traditional choice of a negative power supply for ECL is the result of the upper supply rail being used as the reference for the I/0 and internal switching bias levels of the technology. Since these critical parameters are referenced to the upper rail any noise on this rail will couple 1:1 onto them; the result will be reduced noise margins in the design. Because, in general, it is a simpler task to keep a ground rail relatively noise free, it is beneficial to use the ground rail as this reference. However when careful attention is paid to the power supply design, PECL can be used to optimize system performance. Once again the use of differential PECL will simplify the designer's task as the noise margins of the system will be doubled and any noise riding on the upper V_{CC} rail will appear as common mode noise; common mode noise will be rejected by the differential receiver.

MECL TO PECL DC LEVEL CONVERSION

Although using ECL on positive power supplies is feasible, as with any high speed design there are areas in which special attention should be placed. When using ECL devices with positive supplies the input output voltage levels need to be translated. This translation is a relatively simple task. Since these levels are referenced off of the most positive rail, V_{CC}, the following equation can be used to calculate the various specified DC levels for a PECL device:

$$\text{PECL Level} = V_{CCNEW} - |\text{Specification Level}|$$

As an example, the V_{OHMAX} level for a 10H device operating with a V_{CC} of 5.0 V at 25°C would be as follows:

$$\text{PECL Level} = 5.0\text{ V} - |-0.81\text{ V}|$$

$$\text{PECL Level} = (5.0 - 0.81)\text{V} = 4.19\text{ V}$$

The same procedure can be followed to calculate all of the DC levels, including V_{BB} for any ECL device. **Table 2** outlines the various PECL levels for a V_{CC} of 5.0 V for both the 10H and 100K ECL standards. As mentioned earlier any changes in V_{CC} will show up 1:1 on the output DC levels. Therefore any tolerance values for V_{CC} can be transferred to the device I/0 levels by simply adding or subtracting the V_{CC} tolerance values from those values provided in **Table 2**.

Table 2. ECL/PECL DC Level Conversion for V_{CC} = 5.0 V

Symbol	10E Characteristics						100E Characteristics		Unit
	0°C		25°C		85°C		0 to 85°C		
	Min	Max	Min	Max	Min	Max	Min	Max	
V_{OH}	–1.02/3.98	–0.84/4.16	–0.98/4.02	–0.81/4.19	–0.92/4.08	–0.735/4.265	–1.025/3.975	–0.880/4.120	V
V_{OL}	–1.95/3.05	–1.63/3.37	–1.95/3.05	–1.63/3.37	–1.95/3.05	–1.600/3.400	–1.810/3.190	–1.620/3.380	V
V_{OHA}	—	—	—	—	—	—	—	–1.610/3.390	V
V_{OLA}	—	—	—	—	—	—	–1.035/3.965	—	V
V_{IH}	–1.17/3.83	–0.84/4.16	–1.13/3.87	–0.81/4.19	–1.07/3.93	–0.735/4.265	–1.165/3.835	–0.880/4.120	V
V_{IL}	–1.95/3.05	–1.48/3.52	–1.95/3.05	–1.48/3.52	–1.95/3.05	–1.450/3.550	–1.810/3.190	–1.475/3.525	V
V_{BB}	–1.38/3.62	–1.27/3.73	–1.35/3.65	–1.25/3.75	–1.31/3.69	–1.190/3.810	–1.380/3.620	–1.260/3.740	V

PECL TERMINATION SCHEMES

PECL outputs can be terminated in all of the same ways standard ECL, this would be expected since an ECL and a PECL device are one in the same. **Figure 3** illustrates the various output termination schemes utilized in typical ECL systems. For best performance the open line technique in **Figure 3** would not be used except for very short interconnect between devices; the definition of short can be found in the various design guides for the different ECL families. In general for the fastest performance and the ability to drive distributive loads the parallel termination techniques are the best choice. However occasions may arise where a long uncontrolled or variable impedance line may need to be driven; in this case the series termination technique would be appropriate. For a more thorough discourse on when and where to use the various termination techniques the reader is referred to the MECL System Design Handbook (HB205/D) and the design guide in the ECLinPS Databook (DL140/D). The parallel termination scheme of **Figure 3** requires an extra V_{TT} power supply for the impedance matching load resistor. In a system which is built mainly in CMOS/TTL this extra power supply requirement may prohibit the use of this technique. The other schemes of **Figure 3** use only the existing positive supply and ground and thus may be more attractive for the CMOS/ TTL based machine.

Parallel Termination Schemes

Because the techniques using an extra V_{TT} power supply consume significantly less power, as the number of PECL devices incorporated in the design increases the more attractive the V_{TT} supply termination scheme becomes. Typically ECL is specified driving 50 Ω into a –2.0 V, therefore for PECL with a V_{CC} supply different than ground the V_{TT} terminating voltage will be V_{CC} –2.0 V. Ideally the V_{TT} supply would track 1:1 with V_{CC}, however in theory this scenario is highly unlikely. To ensure proper operation of a PECL device within the system the tolerances of the V_{TT} and the V_{CC} supplies should be considered. Assume for instance that the nominal case is for a 50 Ω load (R_t) into a +3.0 V supply; for a 10H compatible device with a V_{OHmax} of -0.81 V and a realistic V_{OLmin} of –1.85 V the following can be derived.

$$I_{OHmax} = (V_{OHmax} – V_{TT})/R_t$$
$$I_{OHmax} = (\{5.0 – 0.81\} – 3.0)/50 = 23.8\ mA$$
$$I_{OLmin} = (V_{OLmin} – V_{TT})/R_t$$
$$I_{OLmin} = (\{5.0 – 1.85\} –3.0)/50 = 3.0\ mA$$

If +5% supplies are assumed a V_{CC} of V_{CCnom} –5% and a V_{TT} of V_{TTnom} +5% will represent the worst case. Under these conditions, the following output currents will result.

$$I_{OHmax} = (\{4.75 – 0.81\} – 3.15)/50 = 15.8\ mA$$
$$I_{OLmin} = (\{4.75 – 1.85\} – 3.15)/50 = 0\ mA$$

Using the other extremes for the supply voltages yields:

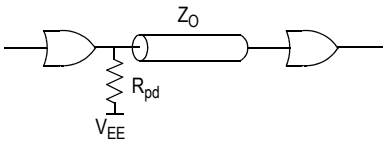
$$I_{OHmax} = 31.8\ mA$$
$$I_{OLmin} = 11\ mA$$

The changes in the I_{OH} currents will affect the DC V_{OH} levels by ≈±40mV at the two extremes. However in the vast majority of cases the DC levels for ECL devices are well centered in their specification windows, thus this variation will simply move the level within the valid specification window and no loss of worst case noise margin will be seen. The I_{OL} situation on the other hand does pose a potential AC problem. In the worst case situation the output emitter follower could move into the cutoff state. The output emitter followers of ECL devices are designed to be in the conducting “on” state at all times. If cutoff, the delay of the device will be increased due to the extra time required to pull the output emitter follower out of the cutoff state. Again this situation will arise only under a number of simultaneous worst case situations and therefore is highly unlikely to occur, but because of the potential it should not be overlooked.

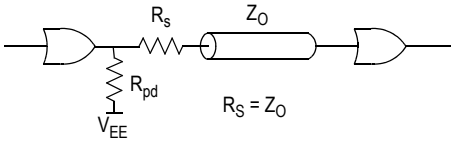
Thevenin Equivalent Termination Schemes

The Thevenin equivalent parallel termination technique of **Figure 3** is likely the most attractive scheme for the CMOS/TTL designer who is using a small amount of ECL. As mentioned earlier this technique will consume more power, however the absence of an additional power supply will more than compensate for the extra power consumption. In addition, this extra power is consumed entirely in the external resistors and thus will not affect the reliability of the IC. As is the case with standard parallel termination, the tolerances of the V_{TT} and V_{CC} supplies should be addressed in the design phase. The following equations
provide a means of determining the two resistor values and the resulting equivalent V_{TT} terminating voltage.

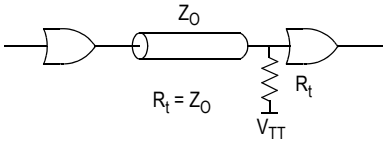
$$R1 = R2\ (\{V_{CC} - V_{TT}\}/\{V_{TT} - V_{EE}\})$$
$$R2 = Z_O\ (\{V_{CC} - V_{EE}\}/\{V_{CC} - V_{TT}\})$$
$$V_{TT} = V_{CC}\ (R2/\{R1 + R2\})$$



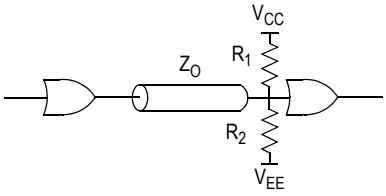
Open Line Termination



Series Termination



Parallel Termination



Thevenin Parallel Termination

Figure 3. Termination Techniques for ECL/PECL Devices

For the typical setup:

V_{CC} = 5.0 V; V_{EE} = GND; V_{TT} = 3.0 V; and Z_O = 50 Ω

R2 = 50 ({5–0}/{5–3}) = 125 Ω
R1 = 125 ({5–3}/{3–0}) = 83.3 Ω

Checking for V_{TT}:

V_{TT} = 5 (125/{125–83.3}) = 3.0 V

Because of the resistor divider network used to generate V_{TT} the variation in V will be intimately tied to the variation in V_{CC}. Differentiating the equation for V_{TT} with respect to V_{CC} yields:

$$dV_{TT}/dV_{CC} = R2/(R1 + R2)\ dV_{CC}$$

Again for the nominal case this equation reduces to:

$$\Delta V_{TT} = 0.6\ \Delta V_{CC}$$

So that for $\Delta V_{CC} = \pm 5\% = \pm 0.25$ V, $\Delta V_{TT} = \pm 0.15$ V.

As mentioned previously the real potential for problems will be if the V_{OL} level can potentially put the output emitter follower into cutoff. Because of the relationship between the V_{CC} and V_{TT} levels the only situation which could present a problem will be for the lowest value of V_{CC}. Applying the equation for I_{OLmin} under this condition yields:

$$I_{OLmin} = (\{V_{OLmin} - V_{TT}\}/R_t$$
$$I_{OLmin} = (\{4.75 - 1.85\} - 2.85)/50 = 1.0\ mA$$

From this analysis it appears that there is no potential for the output emitter follower to be cutoff. This would suggest that the Thevenin equivalent termination scheme is actually a better design to compensate for changes in V_{CC} due to the fact that these changes will affect V_{TT}, although not 1:1 as would be ideal, in the same way. To make the design even more immune to potential output emitter follower cutoff the designer can design for nominal operation for the worst case situation. Since the designer has the flexibility of choosing the V_{TT} level via the selection of the R1 and R2 resistors the following procedure can be followed.

Let V_{CC} = 4.75 V and $V_{TT} = V_{CC} - 2.0$ V = 2.75 V

Therefore:

R2 = 119 Ω and R1 = 86 Ω thus:
I_{OHmax} = 23 mA and I_{OLmin} = 3.0 mA

Plugging in these values for the equations at the other extreme for V_{CC} = 5.25 V yields:

V_{TT} = 3.05 V, I_{OHmax} = 28 mA and I_{OLmin} = 5.2 mA

Although the output currents are slightly higher than nominal, the potential for performance degradation is much less and the results of any degradation present will be significantly less dramatic than would be the case when the output emitter follower is cutoff. Again in most cases the component manufactures will provide devices with typical output levels; typical levels significantly reduces any chance of problems. However it is important that the system designer is aware of where any potential problems may come from so they can be dealt with during the initial design.

Differential ECL Termination

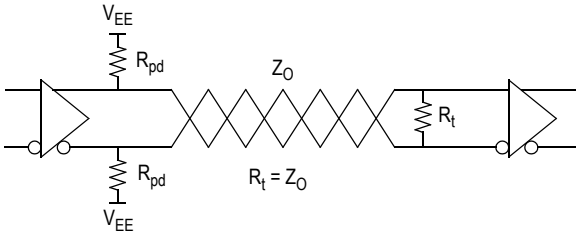
Differential ECL outputs can be terminated using two different strategies. The first strategy is to simply treat the complimentary outputs as independent lines and terminate them as previously discussed. For simple interconnect between devices on a single board or short distances across the backplane this is the most common method used. For interconnect across larger distances or where a controlled impedance backplane is not available the differential outputs can be distributed via twisted pair of ribbon cable (use of ribbon cable assumes every other wire is a ground so that a characteristics impedance will arise). **Figure 4** illustrates common termination techniques for twisted pair/ ribbon cable applications. Notice that Thevenin equivalent termination techniques can be extended to twisted pair and ribbon cable applications as pictured in **Figure 4**. However for twisted pair/ribbon cable applications the standard termination technique picture in **Figure 4** is somewhat simpler and also does not require a separate termination voltage supply. If however the Thevenin techniques are necessary for a particular application the following equations can be used.

$R1 = R2 = Z_O/2$

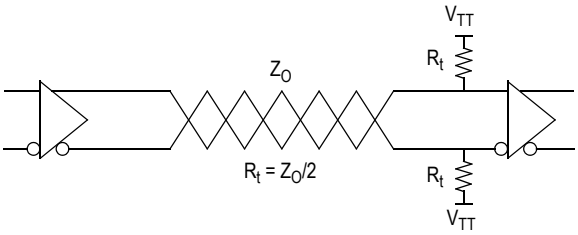
$R3 = R1\ (V_{TT} - V_{EE})/(V_{OH} + V_{OL} - 2V_{TT})$

$V_{TT} = (R3\{V_{OH} + V_{OL}\} + R1\{V_{EE}\})/(R1 + 2R3)$

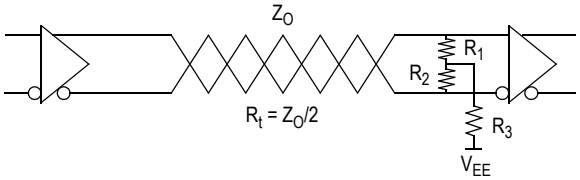
where V_{OH}, V_{OL}, V_{EE} and V_{TT} are PECL voltage levels.



Standard Twisted Pair Termination



Parallel Twisted Pair Termination



Thevenin Twisted Pair Termination

Figure 4. Twisted Pair Termination Techniques

Plugging in the various values for V_{CC} will show that the V_{TT} tracks with V_{CC} at a rate of approximately 0.7:1. Although this rate is approaching ideal it would still behoove the system designer to ensure there are no potential situations where the output emitter follower could become cutoff. The calculations are similar to those performed previously and will not be repeated. The same equations with the change $R1 = R2 = Z_O$ can be used to calculate a “Y” termination for differential outputs into separate microstrip, strip or coaxial cables.

NOISE AND POWER SUPPLY DISTRIBUTION

Since ECL devices are top rail referenced it is imperative that the V_{CC} rail be kept as noise free and variation free as possible. To minimize the V_{CC} noise of a system liberal bypassing techniques should be employed. Placing a bypass capacitor of 0.01μF to 0.1 μF on the V_{CC} pin of every device will help to ensure a noise free V_{CC} supply. In addition when using PECL in a system populated heavily with CMOS and TTL logic the two power supply planes should be isolated as much as possible. This technique will help to keep the large current spike noise typically seen in CMOS and TTL drivers from coupling into the ECL devices. The ideal situation would be multiple power planes; two dedicated to the PECL V_{CC} and ground and the other two to the CMOS/TTL V_{CC} and ground. However if these extra planes are not feasible due to board cost or board thickness constraints common planes with divided subplanes can be used (**Figure 5**). In either case the planes or sub planes should be connected to the system power via separate paths. Use of separate pins of the board connectors is one example of connecting to the system supplies.

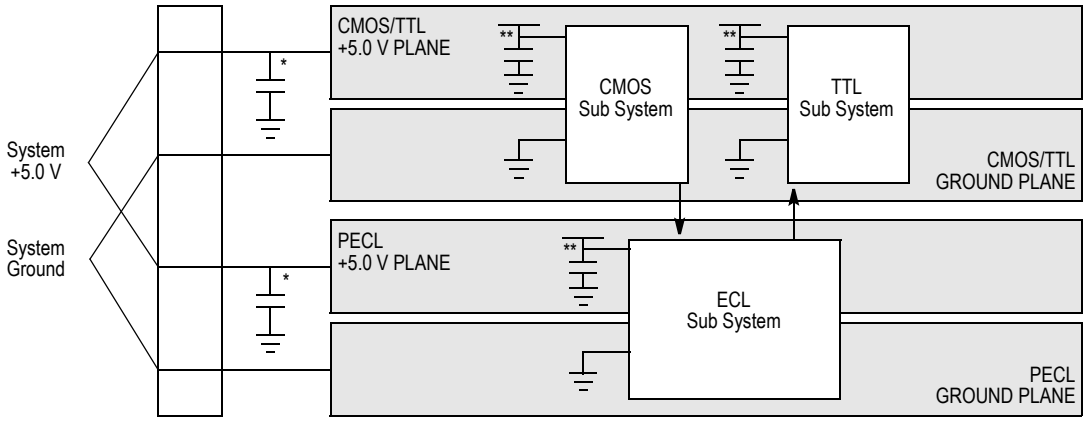
For single supply translators or dual supply translators which share common power pins the package pins should be connected to the ECL V_{CC} and ground planes to ensure the noise introduced to the part through the power plane is minimal. For translating devices with separate TTL and ECL power supply pins, the pins should be tied to the appropriate power planes.

Another concern is the interconnect between two cards with separate connections to the V_{CC} supply. If the two boards are at the opposite extremes of the V_{CC} tolerance, with the driver being at the higher limit and the receiver at the lower limit, there is potential for soft saturation of the receiver input. Soft saturation will manifest itself as degradation in AC performance. Although this scenario is unlikely, again the potential should be examined. For situations where this potential exists there are devices available which are less susceptible to the saturation problem. This variation in V_{CC} between boards will also lead to variations in the input switching references. This variation will lead to switching references which are not ideally centered in the input swing and cause rise/fall skew within the receiving device. Obviously the later skew problem can be eliminated by employing differential interconnect between boards.

When using PECL to drive signals across a backplane, situations may arise where the driver and the receiver are on different power supplies. A potential problem exists if the receiver is powered down independent of the driver. **Figure 6**, represents a generic driver/receiver pair. A current path exists through the receiver's V_{CC} plane when the receiver is powered-down and the driver is powered-on, as shown in

Figure 6. If the receiver has ESD protection, the current will flow though the ESD diode to V_{CC}. If the receiver has NO ESD protection, the current will flow through the input transistor and emitter-follower base-collector junctions to V_{CC}. The amount of current flow, in either case, will be enough to damage both the driver and receiver devices. Either of these situations could lead to degradation of the reliability of the devices. Because different devices have different ESD protection schemes, and input architectures, the extent of the potential problem will vary from device to device.

Another issue that arises in driving backplanes is situations where the input signals to the receiver are lost and present an open input condition. Many differential input devices will become unstable in this situation, however, most of the newer designs, and some of the older designs, incorporate internal clamp circuitry to guarantee stable outputs under open input conditions. All of the ECLinPS (except for the E111), ECLinPS Lite, and H600 devices, along with the MC10125, 10H125 and 10114 will maintain stable outputs under open input conditions.



* Low frequency bypass at the board input
** High frequency bypass at the individual device level

Figure 5. Power Plane Isolation in Mixed Logic Systems

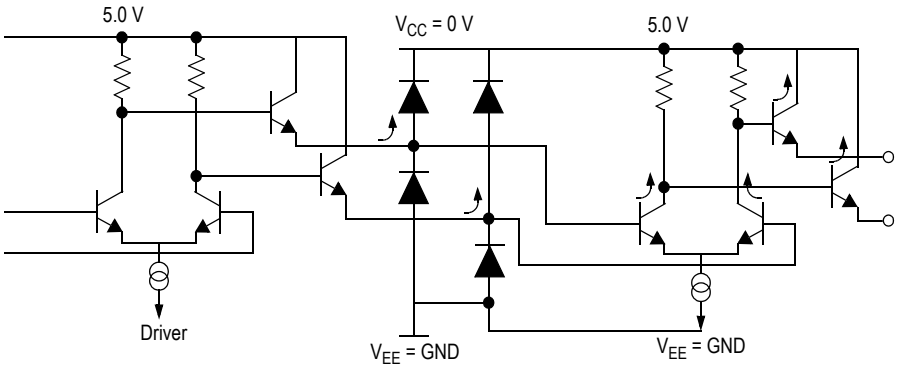


Figure 6. Generic Driver/Receiver Pair

CONCLUSION

The use of ECL logic has always been surrounded by clouds of misinformation; none of those clouds have been thicker than the one concerning PECL. By breaking through this cloud of misinformation the traditional CMOS/TTL designers can approach system problems armed with a complete set of tools. For areas within their designs which require very high speed, the driving of long, low impedance lines or the distribution of very low skew clocks, designers can take advantage of the built in features of ECL. By incorporating this ECL logic using PECL methodologies this inclusion need not require the addition of more power supplies to unnecessarily drive up the cost of their systems. By following the simple guidelines presented here CMOS/TTL designers can truly optimize their designs by utilizing ECL logic in areas in which they are ideally suited. Thus bringing to market products which offer the ultimate in performance at the lowest possible cost.

AN1545

Thermal Data for MPC Clock Drivers

By: Todd Pearson
Applications Engineering

INTRODUCTION

This application note provides general information on thermal and related reliability issues with respect to the MPC family of clock driver products. In addition, methods are presented to estimate power dissipation and junction temperatures for the MPC product family.

Package Choice

The Motorola Timing Solutions products are offered in a variety of surface mount plastic packages. These packages include the 16 and 20 lead SOIC, 20 and 28 lead PLCC and the 32 and 52 lead TQFP packages. The bulk of the newer products are being introduced in the SOIC and TQFP packages with the PLCC being used for the older mature products.

The surface mount plastic packages were selected as the optimum combination of performance, physical size and thermal handling in a low cost standard package. While more exotic packages exist to improve the thermal and electrical performance the cost of these are prohibitive for many applications.

Long Term Failure Mechanisms in Plastic Packages

When analyzing a design for its long term reliability it is important that the dominant failure mechanisms are well understood. Although today's plastic packages are as reliable as ceramic packages under most environmental conditions, as the junction temperature increases a failure mode unique to plastic packages becomes a significant factor in the long term reliability of the device.

Modern plastic package assembly utilizes gold wire bonded to aluminum bonding pads throughout the electronics industry. Because plastic packages use injection molding the bond wires used must be extremely ductile to keep from breaking or being pulled from the bond pad during the injection process. Gold wire has far better ductility than aluminum wire and therefore is used in the process of plastic packaging. Aluminum is the metal used in the majority of low cost digital IC processes for transistor and bond wire interconnect. As the temperature of the silicon (junction temperature) increases an intermetallic forms between the gold and aluminum interface. This intermetallic formation results in a significant increase in the impedance of the wire bond and can lead to performance failure of the affected pin. With this relationship between intermetallic formation and junction temperature established, it is incumbent on the designer to ensure that the junction temperature for which a device will operate is consistent with the long term reliability goals of the system.

Reliability studies were performed at elevated ambient temperatures (125°C) from which an arrhenius equation relating junction temperature to bond failure was established. The application of the equation yields **Table 1**. This table relates the junction temperature of a device in a plastic package to the continuous operating time before 0.1% bond failure (1 failure per 1000 bonds). Note that this equation only holds for continuous elevated junction temperature levels, as the curve is quite steep if a system cycles through a temperature range but spends a relatively short amount of time at the extreme the numbers provided in this table will grossly underestimate the lifetime of the device based solely on the worst case junction temperature seen.

Table 1. Package Junction Temperatures

Junction Temperature (°C)	**Time** (Hours)	**Time** (Years)
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.1
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

The Motorola Timing solutions products are designed with chip power levels that permit acceptable reliability levels, in most systems, under conventional 500lfpm (2.5m/s) airflow. However because of their flexibility and programmability there may be some situations where special thermal considerations may be required.

Thermal Management

In any system design proper thermal management is essential to establish the appropriate trade-off between performance, density, reliability and cost. In particular the designer should be aware of the reliability implication of continuously operating semiconductor devices at high junction temperatures.

The increasing popularity of plastic, small outline surface mount packages is putting a greater emphasis on the need for better thermal management of a system. This is due to the fact that the newer SMD packages generally require less board space than their first generation brethren. Thus designs incorporating the latest generation SMD packaging technologies have a higher thermal density. To optimize the thermal management of a system it is imperative that the user understand all of the variables which contribute to the junction temperature of the device.

The variables involved in determining the junction temperature of a device are both supplier and user defined. The supplier, through lead frame design, mold compounds, die size and die attach can positively impact the thermal resistance and thus, the junction temperature of a device. Motorola continually experiments with new package designs and assembly techniques in an attempt to further enhance the thermal performance of its products.

It can be argued that the user has the greatest control of the variables which commonly impact the thermal performance of a device. Ambient temperature, air flow and related cooling techniques are the obvious user controlled variables, however PCB substrate material, layout density, amount of exposed copper and weight of copper used in the power planes can all have significant impacts on the thermal performance of a system.

PCB substrates all have different thermal characteristics, these characteristics should be considered when exploring the PCB alternatives. Users should also account for the different power dissipation of the different devices in their systems and space them accordingly. In this way the heat load is spread across a larger area and “hot spots” do not appear in the layout. Copper interconnect and power planes act as heat radiators, therefore significant thermal dissipation can be achieved by paying special attention to the copper elements of a PCB. The thermal resistance of copper (package leadframes are made from copper) is significantly lower than that of the epoxy used for the body of plastic packages. As a result the dominant mode of heat flow out of a package is through the leads. By employing techniques at the board level to enhance the transfer of this heat from the package leads to the PCB one can reduce the effective thermal resistance of the plastic package. Copper interconnect traces on the top layer of the PCB are excellent radiators for transferring heat to the ambient air, especially if these traces are exposed to even moderate air flow. In addition using thick copper power planes not only reduces the electrical resistance but also enhances their thermal carrying capabilities. The power planes can be thermally enhanced further by employing special edge connectors which draw the heat from the planes and again dissipate it into the ambient. Finally, the use of thermal conductive epoxies between the underneath of a device and thermal vias to a power plane can accelerate the transfer of heat from the device to the PCB where once again it can more easily be passed to the ambient.

The advent of small outline SMD packaging and the industry push towards smaller, denser designs makes it incumbent on the designer to provide for the removal of thermal energy from the system. Users should be aware that they control many of the variables which impact the junction temperatures and, thus, to some extent, the long term reliability of their designs.

Calculating Junction Temperature

Since the reliability of a device is directly related to junction temperature and that temperature cannot be measured directly there needs to be a means of calculating the approximate junction temperature from measurable parameters. There are two equations which can be used:

$$T_J = T_A + PD\theta_{JA} \text{ or } T_J = T_C + PD\theta_{JC}$$

where:

T_J = Junction Temperature
T_A = Ambient Temperature (°C)
T_C = Case Temperature (°C)
PD = Internal Power Dissipation of the Device (W)
θ_{JA} = Avg Pkg Thermal Resistance (Junction – Ambient)
θ_{JC} = Avg Pkg Thermal Resistance (Junction –Case)

The θ_{JC} numbers are determined by submerging a device in a liquid bath and measuring the temperature rise of the bath, it therefore represents an average case temperature. The difficulty in using this method arises in the determination of the case temperature in an actual system. The case temperature is a function of the location on the package at which the temperature is measured. Therefore, to use the θ_{JC} method the case temperature would have to be measured at several different points and averaged to represent the T_C of the device. This in practice could prove difficult and relatively inaccurate. To alleviate this problem manufacturers will sometimes provide a θ_{Jref} value for a package. This number represents the thermal resistance between the die and a specific spot on the package (usually the top dead center). This measure of thermal resistance typically has a much wider standard deviation than the standard resistance parameters and therefore is sometimes avoided, however it is the most easily measured parameter from which junction temperatures can be calculated.

The θ_{JA} method of estimating junction temperature is the most widely used. To use this method one need only measure the ambient air temperature in the vicinity of the device in question and calculate the internal power dissipation of that device. The total power dissipation in a device is made up of two parts; the static power and the dynamic power. The two components can be calculated separately and then added together. Another source of power is the termination power as clock drivers are generally used to drive terminated transmission lines. For an ECL output this can be significant however for CMOS outputs the termination load current is pulled through very little voltage (the output HIGH and LOW voltages are very near the rail) so that most of the power is dissipated in the actual load. With this in mind we will address calculating power for ECL and CMOS/BiCMOS separately.

Because clock drivers generally drive transmission lines we will not assume any lumped capacitive load at the outputs. Lumped capacitive loads on outputs add significantly to the power dissipated on chip, when however the capacitive loads are at the end of transmission lines they are buffered from the driving device and thus do not add to the power dissipation above that attributed to driving the transmission line. Note that for the purpose of power dissipation calculations it is not equivalent to
calculate the distributed capacitance of a transmission line and treat it as a lumped load at the output of the device. This technique will significantly overestimate the calculated power of a device.

Calculating Power Dissipation in CMOS/BiCMOS Devices

The total power dissipated in a device can be represented as follows:

$$P_D = I_{CC}(\text{static})*V_{CC} + I_{CC}(\text{dynamic})*V_{CC} + n(I_{OH}*(V_{CC} - V_{OH}) + I_{OL}*(V_{OL}))/2$$

In general rather than using dynamic I_{CC} numbers the dynamic power is calculated using power dissipation capacitance numbers (C_{PD}). Using C_{PD} numbers the above equation becomes:

$$P_D = I_{CC}(static)*V_{CC} + C_{PD}*V_{CC}^2*f + n(I_{OH}*(V_{CC} - V_{OH}) + I_{OL}*(V_{OL}))/2$$

As mentioned previously since the output logic levels are very nearly rail to rail, the third part of the above equation can be ignored. Note that although this assumption may be true for series terminated lines it may not be true for parallel termination where the relatively large DC currents will drive the output voltage levels away from the rails. If we assume series termination then the equation reduces to the following:

$$P_D = I_{CC}(static)*V_{CC} + C_{PD}*V_{CC}^2*f$$

The dynamic dissipation may be a function of the number of outputs switching, if this is the case a CPD number may be provided for each output buffer. In this case the equation would expand to:

$$P_D = I_{CC}(static)*V_{CC} + C_{PD}(internal)*V_{CC}^2*f + C_{PD}(output)*V_{CC}^2*f*n$$

where n = number of outputs at the given frequency f.

Finally for a CMOS device the $I_{CC}(static) = 0$ and for a BiCMOS device which utilizes ECL gates internal the $C_{PD}(internal) = 0$ so that the equations reduce to:

$$\text{CMOS } P_D = C_{PD}(internal)*V_{CC}^2*f + C_{PD}(output)*V_{CC}^2*f*n$$

$$\text{BiCMOS } P_D = I_{CC}(static)*V_{CC} + C_{PD}(output)*V_{CC}^2*f*n$$

Calculating Power Dissipation in ECL Devices

Starting from the same basic equation:

$$P_D = I_{CC}(static)*V_{CC} + I_{CC}(dynamic)*V_{CC} + n(I_{OH}*(V_{CC} - V_{OH}) + I_{OL}*(V_{CC} - V_{OL}))/2$$

For ECL devices the static current is equal to the dynamic current (I_{CC} is independent of frequency) therefore the equation reduces to:

$$P_D = I_{CC}*V_{CC} + n(I_{OH}*(V_{CC} – V_{OH}) + I_{OL}*(V_{CC} – V_{OL}))/2$$

The above equation assumes a 50% duty cycle on a single ended output and thus takes the average of the high state and low state power dissipation. For differential outputs it is simpler to calculate the power per output pairs. Since the pairs are always in complementary states the output power for the pair is simply the addition of the low state and high state power consumption. The only time one will see a difference between a single ended and differential output calculation is under worst case conditions. For say an 18 single ended output device the worst case condition would be for all 18 to be in the worst case logic state for power dissipation purposes. For a device on the other hand with 9 pairs of complimentary outputs (18 total) only 9 of the outputs can be in the worst case condition at a time so that the worst case power dissipation of a complimentary output device will be less than a device with an equivalent number of single ended outputs.

The only issue left is determining I_{OL} and I_{OH}. These values are a function of the termination technique and the pull down voltage used. The currents are easily calculated based on the V_{OH}/V_{OL} levels the pull down resistance and the pull down voltage used. For a standard termination of 50Ω to a voltage of 2.0 V below V_{CC}:

$$I_{OH} = (V_{CC} - 0.98) – (V_{CC} – 2.0)/50 = 20.4 \text{ mA}$$

$$I_{OL} = (V_{CC} – 1.7) - (V_{CC} – 2.0)/50 = 6.0 \text{ mA}$$

Thermal Resistance of Plastic Packages

With the power estimates calculated the θ_{JA} of the appropriate package is the only required parameter left to estimate the junction temperature of a device. The θ_{JA} number for a package is expressed in °C per Watt (°C/W) and is used to determine the temperature elevation of the die (junction) over the external ambient temperature. Standard lab measurements of this parameter for the various timing solution packages are provided in the graphs of **Figure 1** through **Figure 3**.

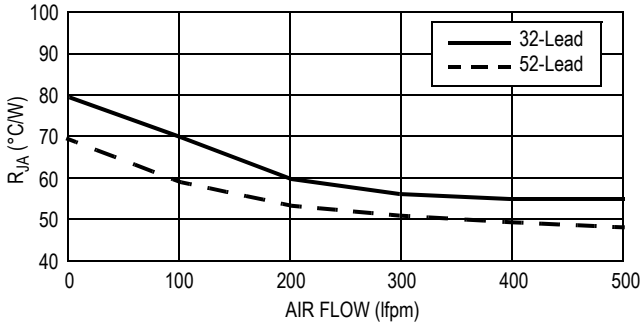


Figure 1. Thermal Resistance of the TQFP Packages

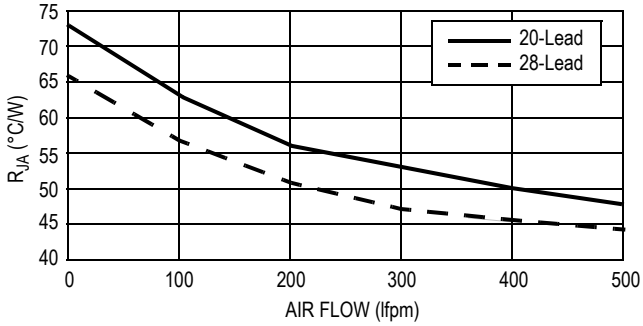


Figure 2. Thermal Resistance of the PLCC Packages

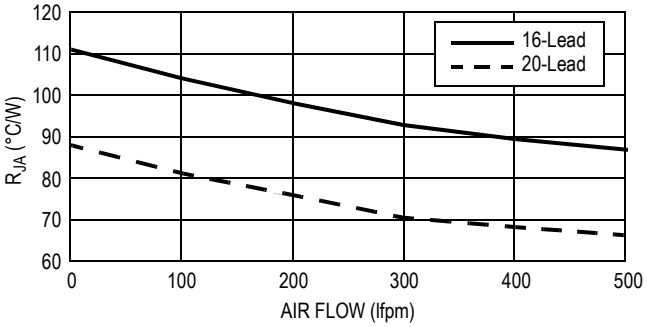


Figure 3. Thermal Resistance of the SOIC Packages

Junction Temperature Calculation Example

As an example the junction temperature of the MPC951 will be calculated. The static I_{CC} of the MPC951 is 95 mA and the C_{PD} per output is 25 pf. From these numbers the following results:

P_D = 95 mA*3.3 V + 3.3 V*3.3 V*25 pf*f *n =
315 mW + 2.72 e–10*f*n

Assume we will configure all 9 outputs to the same frequency, the curve in **Figure 4** shows the power dissipation vs frequency for the MPC951.

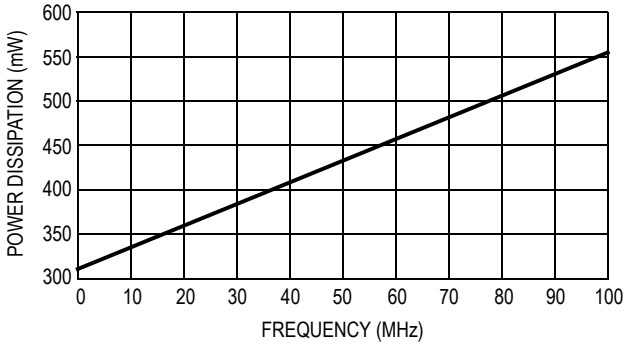


Figure 4. MPC951 Junction Temperature Calculation

Assume that one is building a design with all nine outputs operating at 66 MHz. From the graph this corresponds to a power dissipation of 470 mW. The MPC951 is packaged in the 32 lead TQFP; from the θ_{JA} chart (assume zero air flow) the thermal resistance of the package is 97°C/W. Plugging these into the T_J equation yields the following:

$T_J = T_A + 80°C/W*0.470\ W = T_A + 38°C$.

For a worst case ambient temperature of 70°C the resulting junction temperature would be 108°C. From the MTBF table this would correspond to a lifetime of greater than nine years, a lifetime which is well within the requirements of most systems. If however the user needed a little higher performance of 100 MHz on the outputs the T_J would be:

$T_J = T_A + 80°C/W*0.555W = T_A + 44°C$

Under these conditions the worst case junction temperature would be 114°C and the worst case lifetime would be approaching 4 years. This may not be a satisfactory lifetime and the user would have to do some thermal management to reduce the junction temperature. Obvious enhancements would be providing airflow or perhaps reducing the maximum ambient specifications. If airflow was added (200lfpm) the junction temperature would reduce to:

$T_J = T_A + 60°C/W * 0.555W = T_A + 33°C$

This drops the junction temperature down into the same range as the 66 MHz output case.

The second example will use an ECL output device; the MC100LVE111. The device has 9 differential output pairs and an I_{CC} of 65 mA. Assume that the outputs are terminated 50 Ω to 2.0 V below V_{CC}.

P_D = 65 mA * 3.3 V + 9((0.98*1.02/50)+(1.7*0.3/50)) =
215 mW + 270 mW = 485 mW

The MC100LVE111 is packaged in the 28 lead PLCC; from the θ_{JA} tables the θ_{JA} at 500lfpm is 45°C/W. This yields the following approximate junction temperature:

$T_J = T_A + 45°C/W*0.485\ W = T_A + 22°C$

For a maximum ambient of 70°C the LVE111 exhibits more than satisfactory long term reliability for most systems under standard operating conditions.

Note in both cases the most efficient way to lower the junction temperature is to reduce the ambient temperature of the system. Unit changes in ambient temperature result in unit changes in junction temperature no other parameter is this tightly coupled to junction temperature.

Limitations to Junction Temperature Calculations

The use of the previously described technique for estimating junction temperatures is intimately tied to the measured values of the θ_{JA} of the package. Since this parameter is a function of not only the package, but also the test fixture the results may not be applicable for every environmental condition. As mentioned previously the θ_{JA} of a package in a system could be somewhat higher or lower depending on the thermal design of the board.

In addition the reliability numbers derived for the intermetallic formation assumes constant usage at the specific conditions. In the real world devices will not be exposed to worst case conditions continuously but rather will cycle between the worst case and a lower junction temperature. The MTBF table does not take into account this cycling so that simply calculating the worst case junction temperature and applying it to the table directly will significantly underestimate the long term reliability of the device. Because reliability and environmental conditions are statistical in nature it is important that statistical analysis be applied to any long term reliability studies done on the clock driver products.

Order number: AN1934
Rev 0, 09/2001

AN1934

Effects of Skew and Jitter on Clock Tree Design

By: Don Aldridge and Tom Borr
Applications Engineering

ABSTRACT

This application note discusses the parametrics of skew and jitter as these terms apply to PLL clock drivers and clock buffers. The application note covers the definition of the various types of skew and jitter, the measurement techniques and values associated with these parameters, and concludes with an example clock tree design and analysis of the skew and jitter.

INTRODUCTION

At first glance, clock distribution trees are relatively simple. As shown in **Figure 1**, a typical clock distribution tree consists of a clock source and a series of clock distribution buffers that deliver multiple copies of the clock source to many locations in an electronic system. The clock source may be a crystal oscillator (**Figure 1**) or an external clock source. This clock source may be at the desired frequency or may need to be translated to the desired frequency or frequencies as part of the clock tree circuitry. The clock tree will consist of some combination of PLL clock drivers and/or fanout buffers providing multiple outputs. The clock tree may consist of several devices or be composed of a single integrated circuit. Individual clock outputs deliver the clock signal to various locations on a PC board.

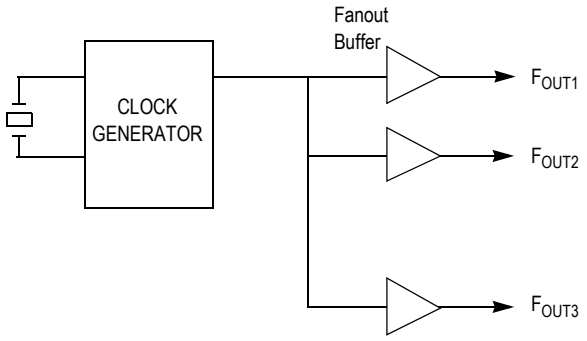


Figure 1. Typical Clock Distribution Tree

After a more detailed look at the requirements of the clock system and the data sheet specifications of the devices used to implement the clock tree, the design appears a bit more complicated and requires a more detailed analysis. The specifications that are most important for this type of analysis are usually found in the AC parameter portion of the clock driver data sheet and consist of parameters such as propagation delay, skew, and jitter.

This application note discusses these parameters by reviewing the definition, the measurement techniques, and their effects on system performance. The application note concludes with the analysis of a typical clock distribution tree based upon these parameters.

Standards for Skew, Jitter Definitions, and Notations

The reference used to determine the standards for skew, jitter definitions, and notations for this application note are the EIA specification EIA/JESD65. This EIA specification documents the current industry standard for these parameters. This document is available in a downloadable PDF format at the web site of: http://www.jedec.org/.

Clock Driver Devices

Clock driver devices consist of both clock fanout buffers and PLL based clock generators. Typical fanout buffers are shown in **Figure 2** and consist of an input buffer driving many outputs though individual output buffers. The specific devices shown are the MPC942C and MPC942P which offer 18 LVCMOS outputs and have either a LVCMOS input or a LVPECL input. Some fanout buffers have an optional internal divider network to produce an input clock divided by two. A Phase Lock Loop device is shown in **Figure 4** and may or may not have built-in fanout buffers. It is not the intention of this application note to explain all of the fundamentals of a PLL; however, a quick review of the components is covered.

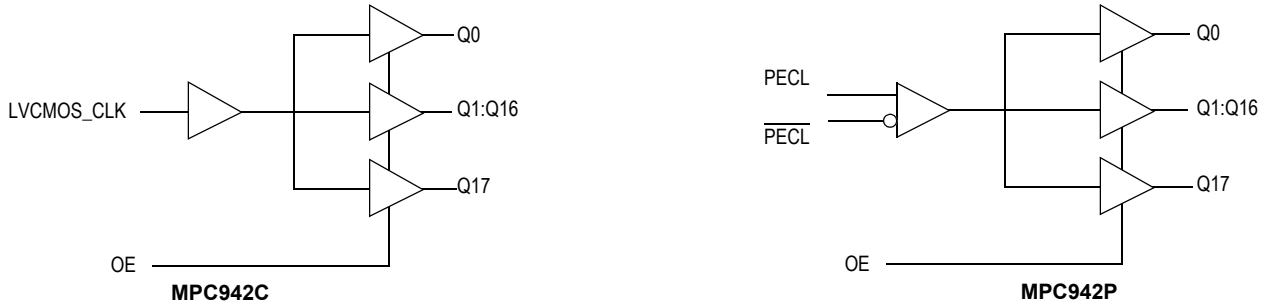
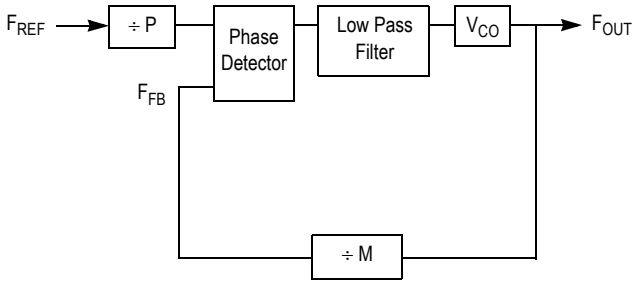


Figure 2. Fanout Buffer

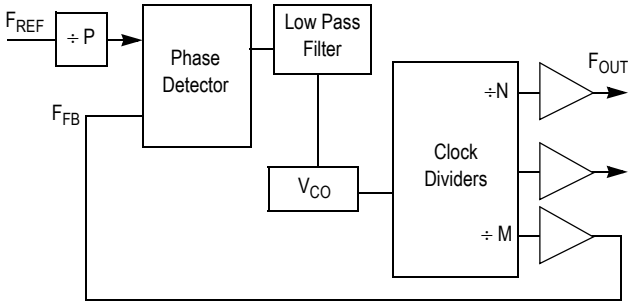
A basic PLL clock architecture (**Figure 3**) consists of a phase detector, a low pass filter, a $V_{CO,}$ and (in this diagram) two divider networks. Both dividers are at the inputs of the phase detector. The input to the clock driver, or the reference frequency, may be external or sourced from a crystal oscillator that is included as part of the clock driver architecture. This input frequency may be divided by an optional P divider block and then applied to the input of the phase detector. The phase detector produces a correction signal based upon the difference in phase in its two inputs. The correction signal or the output of the phase detector is filtered and applied to the input of the voltage controlled oscillator; V_{CO}. The output of the V_{CO} is applied to the M divider and becomes feedback and the second of the two inputs to the phase detector. When the loop is in "lock," the two inputs to the phase detector are the same frequency and the same phase. The output frequency, or $F_{OUT,}$ is the reference frequency divided by P and then multiplied by M and will continually track the reference frequency.

With a few additions to the basic PLL clock architecture, we can create a multi-frequency and multi-clock distribution device as shown in **Figure 4**. The more complex divider network shown provides the M divide value for the feedback path to the input of the phase detector and, also, the N divider divides down the V_{CO} frequency to the desired system frequency or frequencies. Multiple outputs from the clock divider may provide for the generation of multiple frequencies. Note that fanout buffers are included for each output to provide the required system clock drive. Also note that an equivalent fanout buffer is included for the feedback path. The feedback connection for the PLL is external to the device and thus equalizes the delay through the main clock outputs. As is discussed later, the external feedback path may also include compensating trace delay which allows the phase of F_{OUT} clock to be advanced forward or backward with respect to the input clock.



$F_{OUT} = (F_{REF} / P) * M$

Figure 3. Basic PLL



$F_{OUT} = (F_{REF} / P) * (M/N)$

Figure 4. PLL Based Clock Driver

Clock Driver Parametrics

The clock driver parameters that are of interest in this application note are Buffer Propagation Delay, Zero Reference Delay, Skew, Jitter, and PLL Bandwidth and Jitter. These parameters are typically found in the AC parameter portion of a clock driver data sheet.

Fanout buffers have output skew, jitter, and propagation delay. PLL clock driver devices are characterized with jitter, output skew, and an effective input to output propagation delay called Zero Reference Phase Delay. In a clock tree design, the parameters that complicate the analysis is skew between the outputs of a clock fanout buffer and edge or frequency jitter. Jitter commonly is generated in the very early stages of a clock tree and potentially at each stage of the clock tree. These jitter sources may or may not be cumulative and be passed to the outputs.

Buffer Propagation Delay

Clock distribution buffers have a propagation delay from input to output. Typical values for this delay are in the order of a few nanoseconds. Data sheet specifications may be given for a single propagation delay or as separate values given for a low to high edge; versus a high to low edge. The low to high edge value and the high to low edge value should be very similar but not necessarily the same. The notation for propagation delay is t_{pd}. Also the notations of t_{plh} and t_{phl} are used to indicate the propagation delay for a low to high transition and a high to low transition of a waveform, respectively.

Reference Zero Delay

Reference Zero Delay is the JEDEC term for the effective PLL buffer delay. This parameter is also referred to as Static Phase Offset (or SPO). The JEDEC notation is $t_{(\phi)}$. The value of SPO is defined as the average difference in phase between the input reference clock and the feedback input signal, when the PLL is locked. The value of the Reference Zero Delay can be compensated for by including PC board trace delay in the feedback path of the PLL. Specially constructed PLL clock drivers called Zero-delay Buffers make use of this occurrence and can produce a clock edge at the output that is exactly in phase with the input.

Skew

Clock fanout buffers and PLL clock drivers with built-in fanout buffers offer multiple outputs. These clock outputs are routed across a PC board to various devices. A typical fanout buffer may have as many as 18 to 20 clock outputs. Typically, these outputs are designed to drive a 50 ohm cable or a 50 ohm PC board trace. Ideally, all of the outputs are timed such that clock edges on each output switch at exactly the same time. However, real life devices do not. Small amounts of skew exist between the high to low or low to high transition on one output as compared to another output. For systems that require synchronization between data and clocks or multiple clocks on the PC board, this skew is a bad thing. Clock integrated circuit designers try to minimize the amount of skew in a device. However, skew does exist and the device data sheet usually specifies the amount of skew.

This output skew is typically defined in three ways: output-to-output, process, or part-to-part skew.

Output-to-output skew is defined as the skew between the various output edges on a single device. Process skew is defined as the skew between the same output pin on two different devices. Finally, the part-to-part skew is defined as the skew between any output on two different devices. **Figure 5** illustrates output skew types for both single-ended and differential output waveforms. Typically, both output-to-output and part-to-part skew are specified on a data sheet. The JEDEC specification states that the skew values are to be determined with the outputs driving identical specified loads.

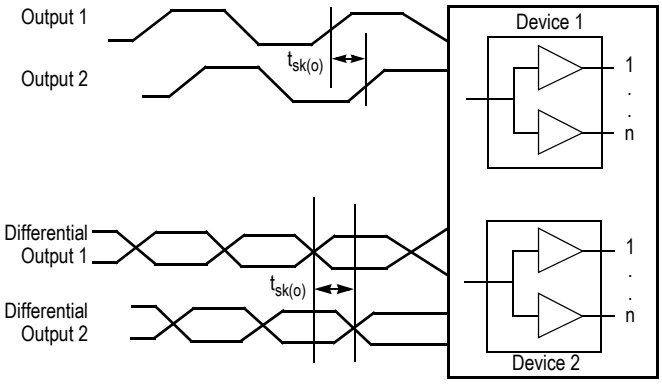


Figure 5. Output-to-Output Skew

Jitter

Jitter is a deviation of the edge location on the output of the clock buffer. As with skew, jitter is a bad thing and is usually measured in picoseconds. There are three categories of jitter that are of interest: cycle-to-cycle, period, and phase jitter.

Cycle-to-cycle jitter is the difference in the period of any two adjacent clock cycles. The difference is reported as an absolute value according to the JEDEC specification. However, quite often a ± value is used. The JEDEC symbol for cycle-to-cycle jitter is $t_{jit(cc)}$. Cycle-to-cycle is usually measured over some large sampling of cycles and specified as the maximum difference. **Figure 6** shows the measurement and calculation of cycle-to-cycle jitter.

In PLL based systems, the value of the cycle-to-cycle jitter is usually small since the PLL does not quickly respond to changes on its input. Since cycle-to-cycle jitter is the difference in the period from one cycle to the next, this jitter is at the clock frequency. This jitter is also referred to as short term jitter.

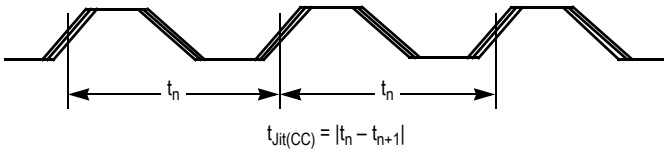


Figure 6. Cycle-to-Cycle Jitter

Clock integrated circuits have an inherent jitter generated within the device. In addition, external sources contribute to this jitter. Specifically, power supply noise may be a source of jitter in both PLL based and non-PLL based clock driver devices. Power supply design, power supply filtering, and board layout contributes to the overall jitter values measured on the output of the clock device.

The second type of jitter is period jitter, which is defined in the JEDEC specification as the deviation in cycle time of a signal with respect to an ideal period. **Figure 7** shows the definition and calculation of period jitter. This jitter type is reported as an absolute maximum value as measured over a long time period. The JEDEC symbol for period jitter is $t_{jit(per)}$. The long time period varies from measurement system to measurement system. Typical time periods are 64 microseconds which, at a frequency of 100 MHz or so, yields many (6400) clock cycle period values. This type of jitter represents the random movement in the instantaneous output frequency or output period of the clock source.

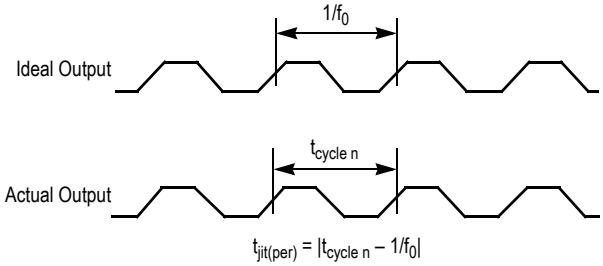


Figure 7. Period Jitter

The last jitter type covered is that of phase jitter. Phase jitter is associated with PLL based clock drivers. The JEDEC specification notation is $t_{jit(\phi)}$. This value represents the input to output jitter associated with a PLL clock driver. The value is given as an absolute value of the range or variation in the difference between the phase of the reference input and the phase of the feedback input to the integrated circuit. (See **Figure 8**.)

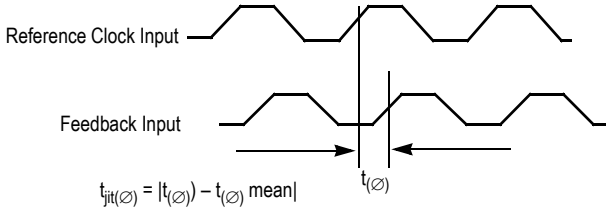


Figure 8. Phase Jitter

Jitter Values and Data Sheets

Definitions of the various types of jitter and the equations for calculating the values are necessary for an understanding of jitter and how it relates to a clock design. However, another important factor in understanding clock drivers is the metrics and methods used of the published specifications. These metrics may vary from manufacturer to manufacturer and also within a manufacturer's clock driver offering. The values may be given as RMS values or as a peak-to-peak value. They may be listed as typicals or as actual maximum values. Understanding of the background of the jitter values on a data sheet are necessary for circuit design as well as comparing clock driver devices.

Jitter measurements, whether cycle-to-cycle period or phase, are measured over some large number of samples. The data for a typical device, when plotted, represents a classic distribution Gausian or bell shaped curve where most of the clock cycles are close to the ideal frequency (in the case of period jitter) with fewer and fewer devices having increasing deviation from the ideal period.

In classical statistics, the distance from the center of the Gausian curve is defined in values of standard deviation or sigma; and the higher the sigma multiplier, the higher the confidence level is that a device will not exhibit a jitter value greater than a predefined amount.

Data sheet specifications that list RMS values imply a 1 sigma deviation above the mean and 1 sigma deviation below the mean or a total of 2 sigma confidence level. **Table 1** lists these confidence factors for ±1 sigma through ±6 sigma. If data sheet values are specified as RMS values and higher levels of confidence are desired, then the data sheet values for jitter must be multiplied by the desired confidence factor.

Figure 9 shows the Gausian distribution curve and sigma points for a device with an output frequency of 400 MHz (period of 2.5 ns). A value of ±3 sigma or 6 sigma gives a confidence level or a probability that the clock edge is within the distribution of 0.9970007%. The ±3 sigma limits define the upper period limit of approximately 2.52 ns and the lower period limit of approximately 2.48 ns.

Figure 10 shows actual measurements made for the period jitter of a 400 MHz clock device.

In this example, the mean period is 2.49921 ns (approximately 2.5 ns) with the standard deviation being 6.48 ps and the peak-to-peak jitter being 57 ps. This data was captured with a sample size of 13100 samples.

Table 1. Confidence Factor

Sigma	Value	Confidence Factor
±1	(2 sigma)	0.68268948
±2	(3 sigma)	0.95449988
±3	(6 sigma)	0.99730007
±4	(8 sigma)	0.99993663
±5	(10 sigma)	0.99999943
±6	(12 sigma)	0.99999999

RMS values for jitter look better on the data sheet than peak-to-peak. However, peak-to-peak values may be needed for clock jitter analysis. If RMS values are specified, peak-to-peak values may be derived based upon the required system reliability for the specific applications. If the other cases where peak values are specified, these values may be used directly. However, the question that must be asked in order to use the manufacturer's peak-to-peak values is what level of uncertainty is being specified. These parameters may be specified differently on each manufacturer data sheet. Therefore, care must be taken to insure that when one is comparing values, the values are specified and measured in a similar fashion.

The above discussion assumes the jitter measurements have the classic Gausian curve or statistical distribution. This would be the case if the jitter is completely random. However, clock driver devices may have internal mechanisms that produce jitter that deviates from the classic bell curve. In this case, the total jitter is composed of the addition of a series of bell curves providing a more complex distribution. With care, the terms of RMS and the various sigma levels may still apply.

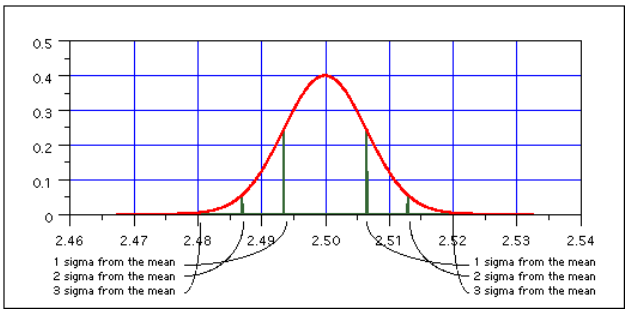


Figure 9. Classic Gausian Distribution Curve

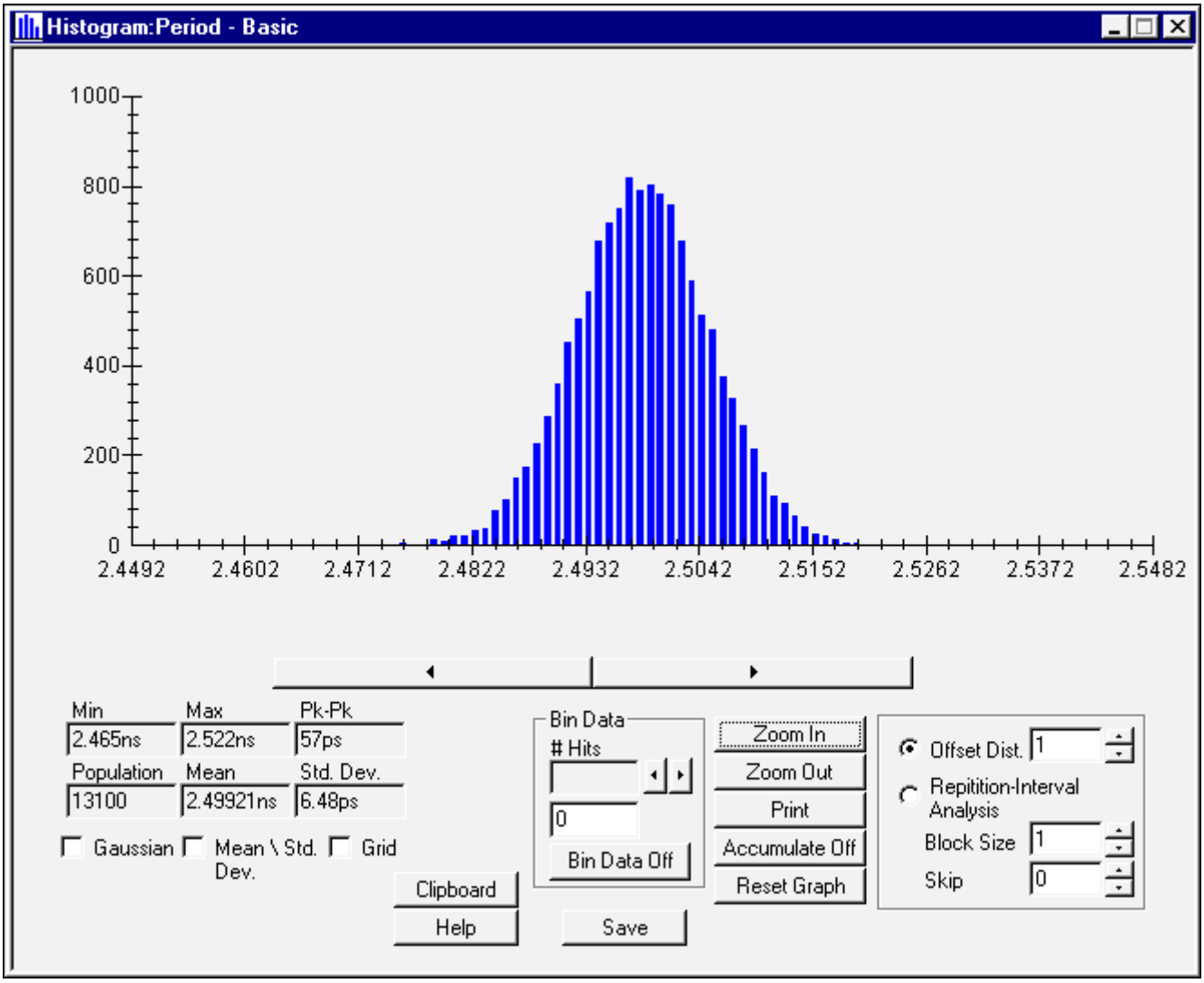


Figure 10. Period Jitter for Typical PLL Clock Device with F_{OUT} = 400 MHz

PLL Bandwidth and Jitter

The PLL based clock driver locks on to a reference frequency and maintains an output frequency based upon that reference frequency. If the reference frequency changes, the PLL attempts to follow the change in the reference frequency. However, if the change is faster than the PLL can follow, the PLL based clock driver acts as a low pass filter and ignores or effectively filters out the higher frequency changes on its input. As with any low pass filters, the PLL has a cutoff frequency, or bandwidth, associated with it. This bandwidth becomes important to our clock tree design. High frequency noise and jitter will not pass through the PLL.

The actual bandwidth of the locked PLL is dependent on many factors, including the feedback divider ratio. The higher the divide ratio, the lower the bandwidth. Thus, those PLL clock driver devices that have selectable feedback divide ratios will have varying bandwidth values. Bandwidth may or may not be specified by the PLL clock driver manufacturer. If not specified, the information is usually available on request.

Figure 11 is a typical PLL frequency modulation bandwidth waveform. Note the cutoff frequency is about 300 kHz. As mentioned before, the cutoff frequency will vary with a change in the divide ratio in the feedback loop. Bandwidths of PLL-based clock drivers vary from low values of a few kHz to higher values of a MHz or more depending upon the intended application of the device. Clock synthesizers typically have the lowest bandwidth. Bandwidths of these devices are in the order of 30 to 50 kHz. Clock generators are next with bandwidths of a few hundred kHz. The devices with the highest bandwidth are the Zero-Delay-Buffers. The bandwidths of these devices are typically a MHz and above.

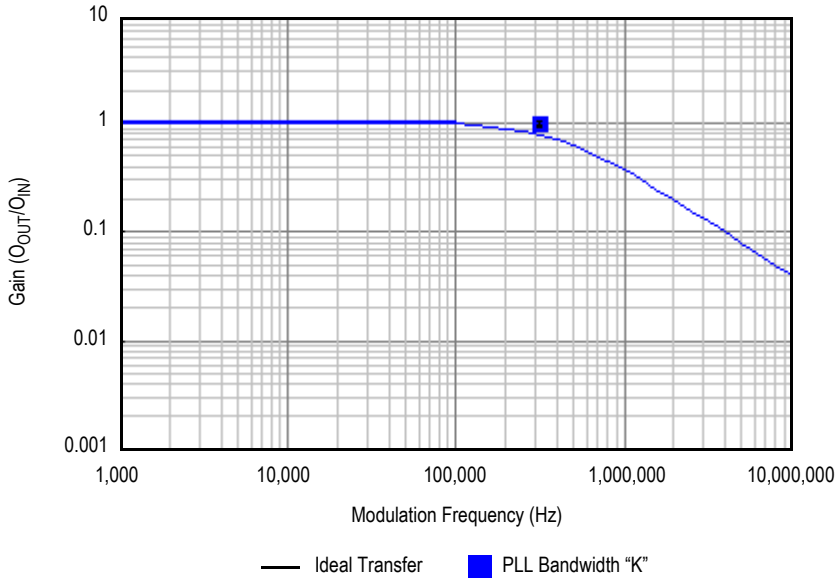


Figure 11. PLL Bandwidth

Clock Tree Application Example Analysis

Figure 12 shows an example clock tree application which is used to show the effects of skew and jitter in a system. The goal of this design is to provide multiple phase aligned HSTL and LVCMOS outputs. The reference for this clock tree is a crystal oscillator while the outputs of the tree provide both HSTL and LVCMOS to various system locations. The tree starts with a crystal oscillator in the MC12430 integrated circuit. The MC12430 is a PLL based clock synthesizer that allows very fine control of the output frequency in 1 MHz steps.

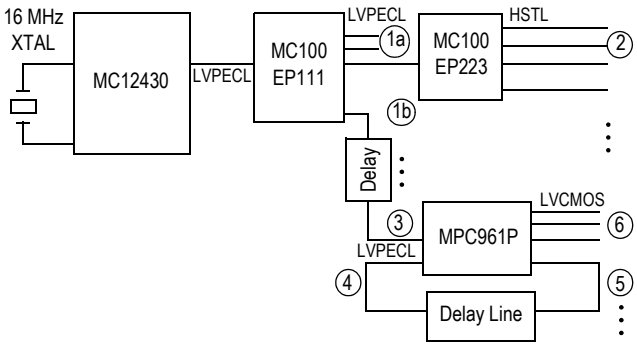


Figure 12. Example Clock Tree

The LVPECL output of the MC12430 drives the LVPECL input to the MC100EP111 fanout buffer.

The MC100EP111 consists of 10 LVPECL differential pairs of which one pair is connected to a MC100EP223 input and another pair connected to the MPC961P input. The MC100EP223 fanout buffer provides HSTL outputs while the MPC961P is a PLL-based clock generator that provides several LVCMOS outputs. Notice there is an introduced delay from the LVPECL output of the EP111 to the LVPECL input of the MPC961P zero-delay buffer. This introduced delay is due to backplane or cable distance which will skew the LVCMOS outputs to later than the HSTL outputs. To compensate for this delay, the MPC961P zero-delay buffer is used in conjunction with a PC board delay line in the feedback path.

Figure 13 provides an analysis of the example clock tree for the situation where we have no (or choose to ignore both) jitter and skew in the devices. Later, in **Figure 14**, an analysis with both jitter and skew is shown. The circled numbers in **Figure 12** are used as reference points on the clock analysis waveforms.

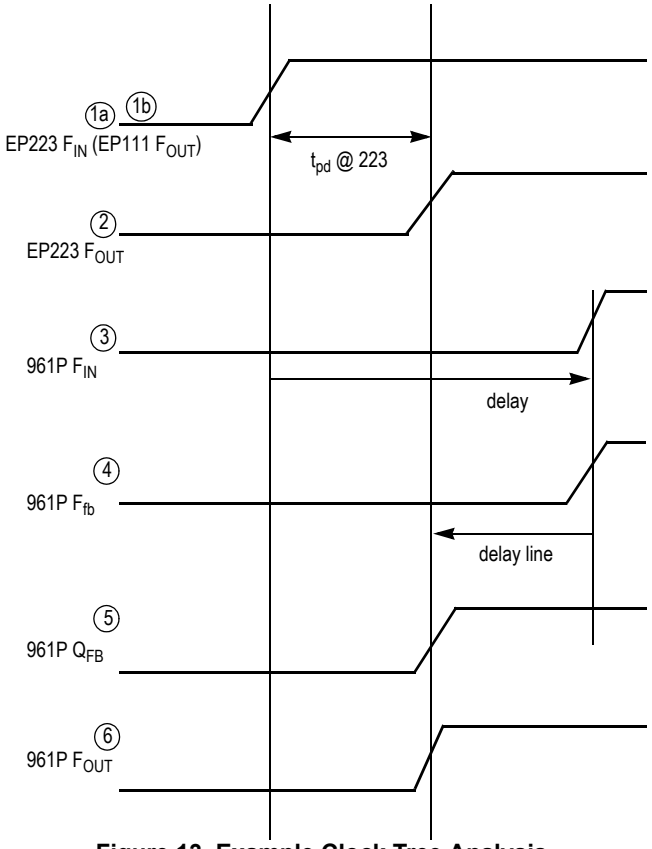


Figure 13. Example Clock Tree Analysis without Jitter and Skew

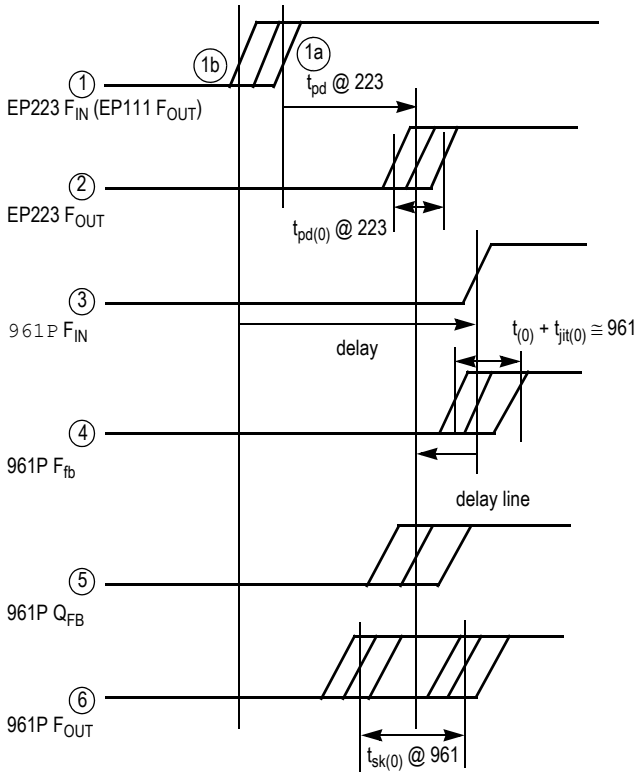


Figure 14. Example Clock Tree Analysis with Jitter and Skew

The first analysis of the clock tree is with the assumption that there is zero output-to-output skew and zero jitter. With zero skew between the outputs of the MC100EP111, the signals 1a and 1b are identical. The waveform at point 2 is delayed due to propagation delay, t_{pd}, of the MC100EP223.

The waveform at point 3 is delayed due to the delay associated with the backplane or cable distribution. By using the MPC961P zero-delay buffer and placing the appropriate trace delay in the feedback path of the PLL, we can compensate for the backplane trace and bring the waveform for points 5 and 6 back in line with the output of the MC100EP223.

Next, we will do the same analysis but we will include the output skew on the MC100EP111, the MC100EP223, and the phase jitter for the MPC961. (See **Figure 14**.)

Initially, we have the output-to-output skew for the EP111. We will assume that the output connected to the MC100EP223 is the slowest and thus the longest delay output and that the output connected through the delay line to the input of the MPC961C is the fastest or shortest delay output. This analysis must also be done for the opposite situation; where the MPC961P is connected to the slowest output and the MC100EP223 is connected to the fastest output.

The waveform at point 2 is delayed from point 1a by the propagation delay, t_{pd}, of the MC100EP223 as we had in **Figure 13**. However, by including the output-to-output skew for the MC100EP223, we find uncertainty in the location of point 2 as shown in the waveform of point 2 of **Figure 14**.

Point 3 shows the waveform arriving at the input to the MPC961P. Point 4 is the feedback input to the MPC961P and, in the ideal case, is exactly the same as point 3. However, in this situation, we have the uncertainty caused by the combination of the static phase offset, $t_{(\phi)}$ and the phase jitter for the MPC961P. **Figure 14** depicts these two values added together. The waveform of point 5 now moves back in time due to the delay line in the feedback path of the PLL such that the nominal output now coincides with the HSTL outputs of point 2. Point 6 shows the added uncertainty of the outputs due to the output-to-output skew from the MPC961P. Note that **Figure 14** is not to scale and the magnitudes of the skew and jitter are actually much smaller than indicated.

Table 2 lists the skew and jitter values for the 3 devices used in the example. The MC100EP111 has a specification for output-to-output skew. The MPC961P has parametric values for Static Phase Offset, phase jitter and output-to-output skew. The MC100EP223 has values for propagation delay and output-to-output skew.

Table 2. Confidence Factor

Device	Parameter
MC100EP111	tsk(o): 70 ps
MPC961P	$t_{(\varnothing)}$: -50 to 225 ps $t_{jit(\varnothing)}$ ÂF ~ 100 ps $t_{sk(o)}$ ÂFÂ @ 150 ps
MC100EP223	t_{pd}: estimated 700 ps $t_{sk(o)}$: estimated 50 ps

A similar analysis can be done for the case where the MC100EP111 outputs connected to the MC100EP223 and MPC961P are reversed in time. Thus, the MC100EP111 output connected to the MC100EP223 is the fastest and the output connected to the MPC961P is the slowest.

One last comment on the example is that the jitter associated with the clock source, MC12429, was not mentioned in the analysis. This value was ignored for this example due to the fact that all of the clock outputs are derived from the same source, and jitter that occurs on one output would show up on all outputs. Applications that have clock outputs derived from different sources, or have the clock source compared to a frequency standard, would mandate the need to include the source jitter in the analysis.

SUMMARY

Skew and jitter are real characteristics of clock driver devices and may or may not be of importance to a clock tree design. Understanding data sheet values and applying this knowledge to clock tree design can sometimes be a real challenge. With a bit of analysis, one can determine which parameters are critical to a specific clock tree design and be able to compare the values of these parameters from one device/vendor to another. Lastly, data sheet values of jitter are often measured in a lab environment under the best of conditions. Real designs with clock drivers on PC boards with other digital circuitry, noisy power supplies, long traces, and other clock sources can make the overall jitter worse. Careful design practices are a must for the best clock driver design.

Order number: AN1939
Rev 0, 11/2001

AN1939

Clock Driver Primer — Functionality and Usage

By: Don Aldridge and Tom Borr
Applications Engineering

ABSTRACT

This application note focuses on the fundamentals of clock drivers, including definitions, applications, and characteristics of integrated devices. This application note is intended for the system designer that is tasked with creating a clock source for a microprocessor-based system. Although the clock may be a small portion of the system schematic, its design becomes a fundamental contributor to the overall system performance.

INTRODUCTION

Tucked away in the corner of a complex microprocessor PC board is the clock source that provides the timing for the entire PC board. This clock source may be simple or it may be complex. It may only consist of a crystal, a couple of integrated circuits, and some traces on the PC board. It may also be very complex with many clock outputs, zero-delay buffers and precise timing delays that are built into the PC board. This application note covers the basics of a clock tree design for microprocessor applications. These basics include the definitions of terms used in clock driver applications, how Phase Locked Loops (PLL) work, what makes the basic PLL into a clock driver, what distinguishes one clock driver from another, and how to select the appropriate devices for a specific application. Also, this application note covers a few of the clock tree design “gotchas.”

Applications for clock trees abound in the electronics for telecommunications and computer systems. The system requirements are for clocks of several megahertz to hundreds of megahertz. There are many common frequencies that need to be generated based upon the application for the clock. Frequencies of 33 MHz, 66 MHz, 100 MHz, and others are common in most applications. **Figure 1** shows two clock trees. A simple clock tree on the left that has a crystal input of 16.66 MHz and a 200 MHz output, but is selectable from 25 MHz to 400 MHz. The clock on the right is more complex, with 16 MHz as its input, and provides as its output several clock outputs of varying drive levels. To compensate for the delay in routing the clock across a backplane or PC board, a zero-delay buffer is used to provide a clock with aligned edges.

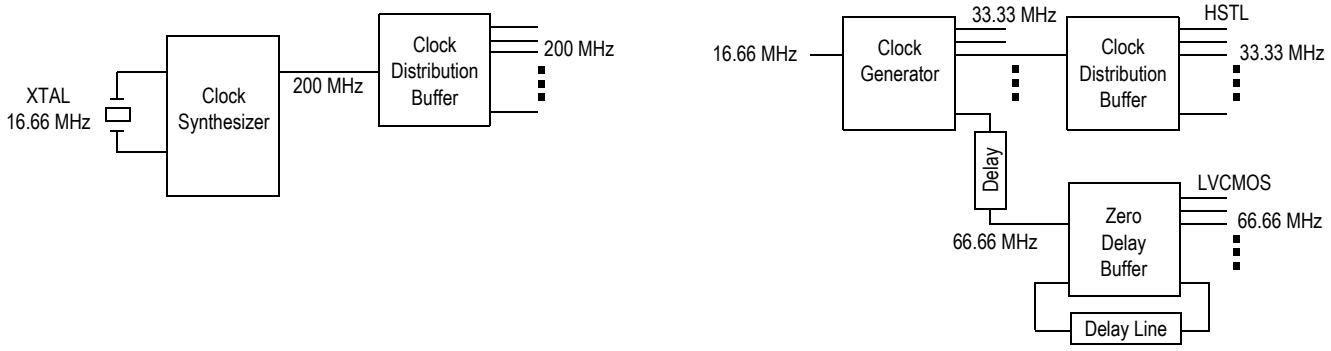


Figure 1. Typical Clock Trees

PLL CLOCK DEVICES

The Basic Phase Locked Loop

A phase locked loop or PLL is one of the fundamental elements of clock drivers. Although PLLs get used in many different electronic circuit applications, their usage in clock driver circuits dictate certain unique characteristics. It is not the intention of this application note to have complete coverage of phase lock loops. However, the fundamental operation of the PLL circuitry for clock driver applications is covered.

A phase locked loop has, as its input, a clock frequency source of which the PLL locks on to and produces, as its output, another clock signal. The output clock may be at the same frequency as the input or at some multiple of the input frequency. If the input clock should change in frequency or phase, the output clock follows this change.

A basic PLL clock architecture consists of a phase detector, a low pass filter, and a voltage-controlled oscillator or VCO, which are connected as shown in **Figure 2**. In addition to these blocks, the PLL has a frequency divider network which, in **Figure 2**, is called the M divider. This divider network is connected between the output of the VCO and one of the inputs of the phase detector. The other input to the phase detector is the reference frequency to which the PLL is to lock. The output of the PLL is F_{OUT}, which is the clock that is distributed throughout the clock tree system.

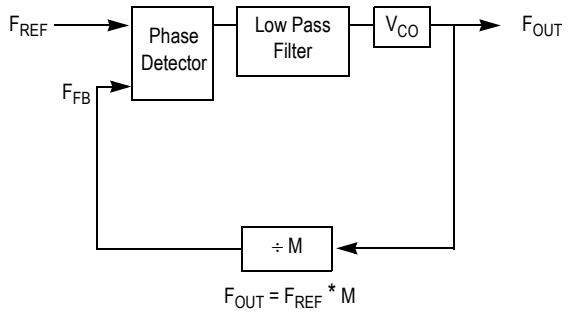


Figure 2. Basic Phase Locked Loop (PLL)

The phase detector has two inputs which are compared and used to produce a correction or error signal based upon the difference in the phase of those two inputs. One of these inputs is the previously mentioned reference frequency. The other input is the feedback signal from the VCO/divider network.

The PLL correction signal, which is the output of the phase detector, is filtered and applied to the input of a voltage-controlled oscillator or VCO. This filtered correction signal sets the VCO frequency. The output of the VCO is applied to the M (or feedback) divider and becomes the second of the two inputs to the phase detector. When the loop is in “lock,” the two inputs to the phase detector are the same frequency and the same phase. This is due to the phase detector correction signal approaching zero and thus stabilizing the input control voltage to the VCO. The VCO output frequency, or F_{OUT}, becomes the reference frequency multiplied by M and continually tracks the reference frequency. The equation for F_{OUT} is the reference frequency multiplied by M. If M is 1, then the output frequency is the same as the input reference frequency.

By changing the value of M, the VCO frequency changes in increments of the reference frequency. Thus a lower reference frequency input can be multiplied up to the desired output frequency.

The VCO has a limited frequency range over which it can operate. The input frequency multiplied by the feedback divide value must produce a frequency that is within the allowable range of the VCO. If this condition is not met, the VCO is considered to be “railed” high or “railed” low and the PLL is no longer in lock.

Basic PLL Clock Driver

Figure 3 depicts additions to the previous basic PLL Clock Architecture circuitry, which creates a multi-frequency and multi-clock distribution source. The more complex divider network on the output of the VCO provides the M divide value for the feedback path to the input of the phase detector and also divides down the VCO frequency to the desired system frequency or frequencies.

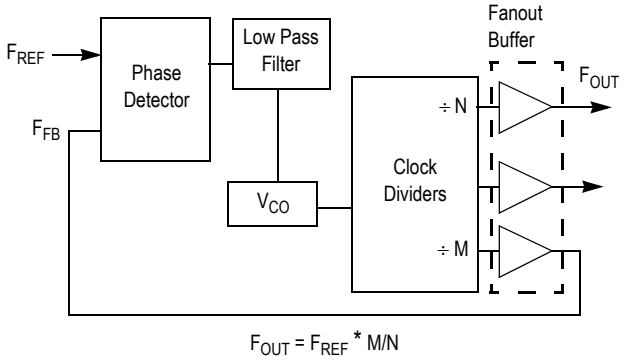


Figure 3. PLL Based Clock Generator

The outputs from this example clock generator provide multiple outputs and multiple frequencies for distribution in the application. Fanout buffers are included for each output to provide the required system drive. Also, if the device has a special feedback output, then an equivalent fanout buffer is included for the feedback path. The feedback connection may be external to the device, and this buffer equalizes the delay through the main clock outputs. By incorporating the M divider with the output dividers, the phase relationship is known between the input reference clock and the output clock(s). Also, both the feedback divider and the output divider(s) may be selectable; this allows the user to adjust the output frequency or frequencies.

Later in this application note, we will discuss how the external feedback path may also include some PC board trace delay. Design of this external trace delay allows the phase of the output clock to be aligned forward or backward (relative to the input clock phase).

A Look at an Actual Clock Driver — MPC9351

Next, let's look at an actual clock driver. **Figure 4** is the block diagram of a typical clock driver, the MPC9351. This device has a PLL block which contains the phase detector and VCO. The input to the MPC9351 can be either a differential clock on the PCLK and ~PCLK inputs or on the single ended input TCLK. The MPC9351 has a total of nine LVCMOS level outputs for system clock usage.

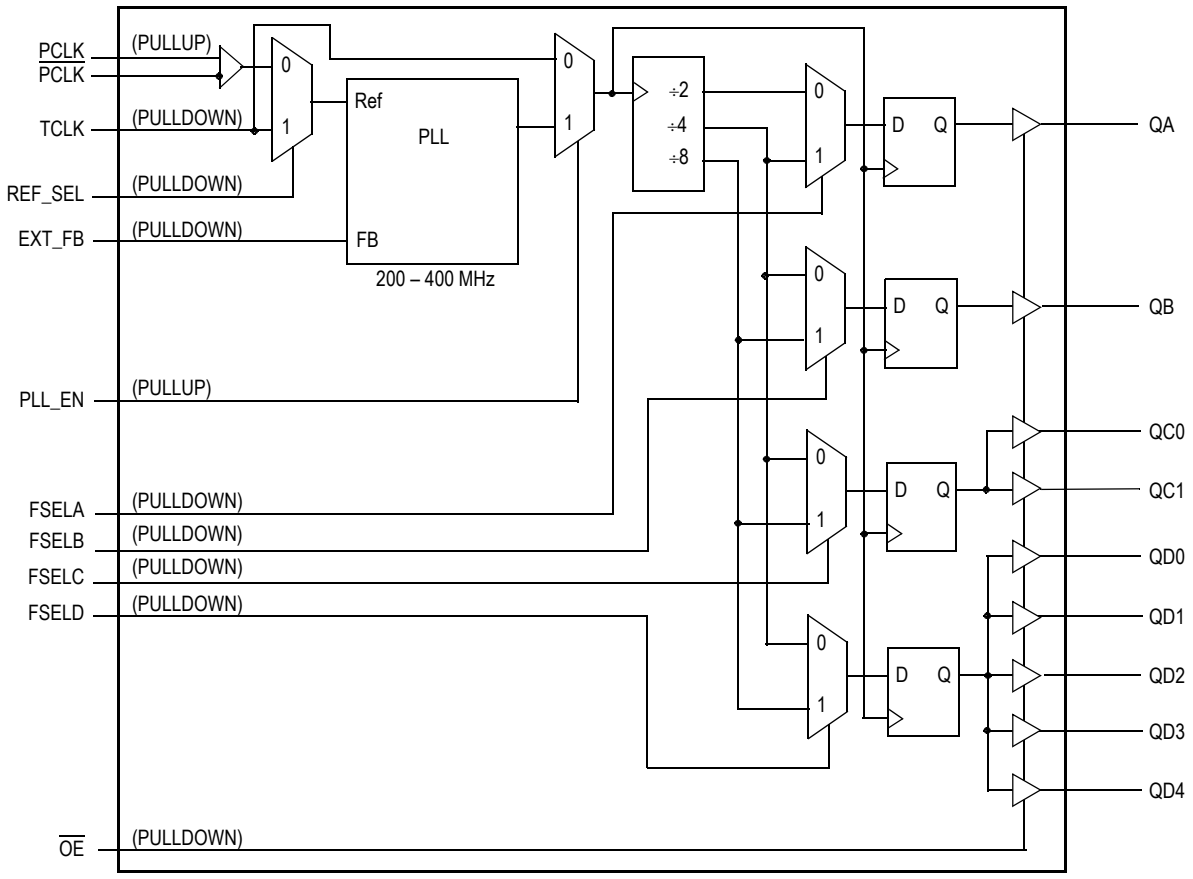
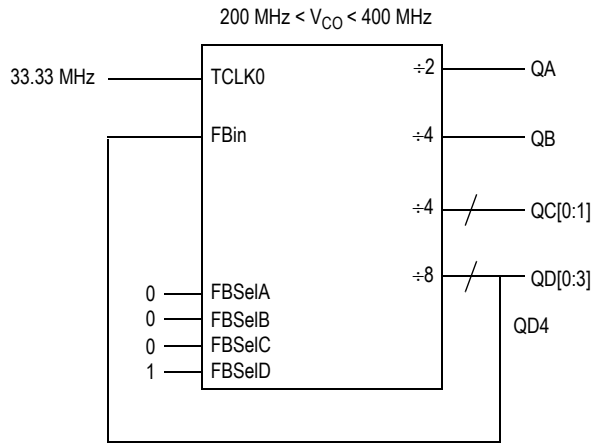


Figure 4. MPC9351 Clock Generator Block Diagram

Of special interest is the divider network and output circuitry. The VCO output of the MPC9351 is available through four banks of outputs where each bank of outputs has a selectable divide value. The first bank of outputs (labeled QA) consists of a single output. This output may provide a clock output frequency of the VCO frequency divided by either 2 or 4. The second bank of outputs (labeled QB) also consists of a single output which can be at the VCO frequency divided by 4 or 8. The third bank of 2 outputs (labeled QC0 and QC1) has the same selectable divide values of 4 or 8. Lastly, the fourth bank has four outputs (labeled QD0 – QD4) with the same divide by either 4 or 8. Although this clock driver does not have specific outputs for the feedback, typically one of the QD outputs would be used for the feedback input to the PLL. The FSELA through FSELD inputs are used to select the output divide ratios for each of the four banks.

A typical connection of the MPC9351 is shown in **Figure 5**. Here, a 33.33 MHz input frequency is multiplied by the feedback divide value of 8 which produces a VCO frequency of 266 MHz. This is in the allowable range of the MPC9351 VCO. The 266 MHz VCO frequency is then divided by 2 for the QA output to produce 133 MHz. Separately, the 266 MHz VCO frequency is divided by 4 for the QB output. Likewise, the 266 MHz VCO is divided by 4 for the QC outputs. This provides one clock output at 133 MHz, four clock outputs at 66.66 MHz, and four clock outputs at 33.33 MHz.



V_{CO} = 33.33 MHz * 8 = 266.66 MHz
QA = 266.66 / 2 = 133 MHz
QB = 266.66 / 4 = 66.66 MHz
QC0:1 = 266.66 / 4 = 66.66 MHz
QD0:3 = 266.66 / 8 = 33.33 MHz

Figure 5. MPC9351 Clock Generator Application

Clock Drivers — The Differences

The Motorola Advanced Clock Driver Selector Guide (SG392) has over 30 PLL clock driver devices. Each of these devices is similar in functionality but each is unique in features and the specifics of their functionality. These devices differ in the number of outputs, how the outputs are divided into banks, what feedback divider ratios are offered, and whether the device has crystal oscillator circuitry or uses an external reference input. The devices differ on whether they have differential or single-ended outputs, the frequency range of the VCO, the output duty cycle, and whether the device has an input divider for the reference. Also, the AC electrical specifications of jitter, skew, and bandwidth vary from one device to the next. The next few sections discuss some of these characteristics.

Outputs

Typically, a clock driver output is used to deliver a timing signal source to a single location in a design. If multiple locations require clock signals then multiple outputs are used. This simplifies the electrical design and the PC board design. For example, the usage of individual clock outputs eliminates the requirement of matching PC board trace lengths and worrying about trace stubs that one would have to consider when routing a single clock output to many different locations of a PC board.

Application requirements of multiple outputs result in clock drivers with different numbers of outputs. Some devices have a few outputs while others have as many as 21 individual outputs. In addition to the number of outputs, the grouping of these outputs into banks differ from one device to the next. Grouping the outputs into banks, with taps to the output divider at different values in the divider chain, allows the device to produce different output frequencies. Therefore, a device may be configured with one bank of outputs to provide a high frequency processor clock, a second bank to provide PCI clock outputs, and a third to provide specific frequencies associated with various I/O peripherals.

Input/Output Voltage Levels

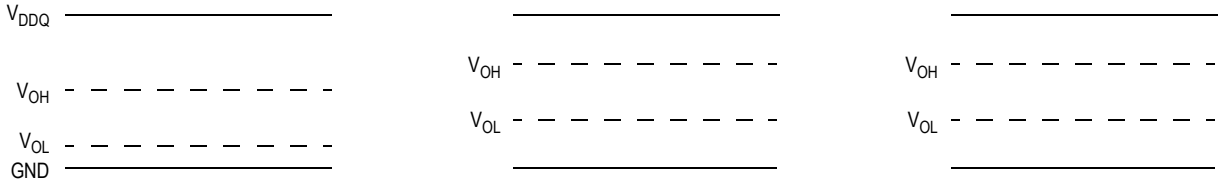
The voltage threshold levels on the input and output of the clock driver differ from one clock driver to the next. Popular logic voltage levels are LVCMOS, LVPECL and HSTL. Also, the clock drivers may have one level for the input clock and a different level for the output clock. Some clocks offer a selection of input levels. For instance, a clock input selection pin would allow the user to select between a differential pair of LVPECL inputs or a single-ended LVCMOS input.

LVCMOS is usually used as a single ended input or output. It is specified at 3.3, 2.5, and 1.8 Volts. The voltage levels are compatible to many of the inputs to microprocessors, FPGA or ASIC devices, and peripheral devices. LVCMOS is specified in JEDEC specifications EIA/JESD36 and 80.

LVPECL is typically used in differential input and output signaling. It is the low voltage, 3.3 V, version of the 5 V PECL logic specification. (PECL is the positive level specification for ECL logic.) The signal swing is approximately 600 mV and is centered at 1 volt below the supply voltage. The differential nature of LVPECL offers advantages over single ended levels. These advantages are discussed later in this application note.

The logic level specification of HSTL stands for High Speed Transceiver Logic. It is specified in EIA/JESD8-6 and is titled “A 1.5 V Output Buffer Supply Voltage Based Interface Standard for Digital Integrated Circuits.” It may be used as a single-ended logic interface but is more commonly used as a differential signal. HSTL has a differential voltage value Vx and common mode voltage Vcmr.

Figure 6 shows the output levels for LVCMOS, LVPECL, and HSTL. For the LVCMOS clocks, the voltage levels of 3.3, 2.5, and 1.8 are shown with the output drive levels as taken from the JEDEC specifications. Other JEDEC specifications also specify LVCMOS drive levels; however, the specifications shown here have the capability of driving 50 ohm transmission lines as would be used in clock distribution.



LVCMOS			
V_{DDQ}	= 3.3	2.5	1.8
V_{OH}	= 2.0	1.8	1.6
V_{OL}	= 0.55	0.6	0.2
V_{TT}	= V_{DDQ}/2	V_{DDQ}/2	V_{DDQ}/2
I	= 24 mA	8 mA	100 μA

LVPECL	
V_{DDQ}	= 3.3
V_{OH}	= V_{DDQ} – 1.025
V_{OL}	= V_{DDQ} – 1.62
V_{TT}	= V_{DDQ} – 2
I	= mA

HSTL	
V_{DDQ}	= 1.5
V_{OH}	= V_{DDQ} – 0.5
V_{OL}	= 0.5
V_{TT}	= V_{DDQ}/2
I	= mA

Figure 6. Logic Levels

AC Characteristics — Skew and Jitter

Two important, but often misunderstood, characteristics of clock drivers are output skew and jitter. Output skew is the difference in the timing of coincident edges between outputs for multiple outputs of a clock driver. Jitter is a deviation in the frequency or period of the output clock from the specified frequency or period.

There are three different types of skew defined per the JEDEC specifications. Output-to-output skew is defined as the skew between the various output edges on a single device. Process skew is defined as the skew between the same output pin on different devices due to process variation. Finally, part-to-part skew is defined as the skew between any output on two different devices. **Figure 7** illustrates output skew types for both single-ended and differential output waveforms. Typically, both output-to-output and part-to-part skew is specified on a data sheet.

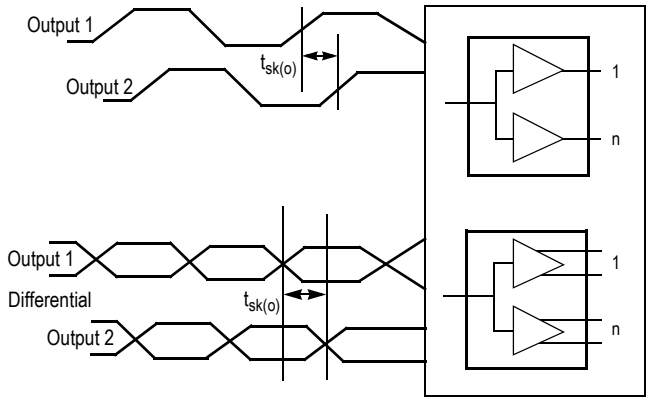


Figure 7. Output Skew

Jitter is a deviation of the edge location on the output of the clock buffer. There are three categories of jitter that are of interest: cycle-to-cycle, period, and phase jitter. One, two or all three may be specified on a clock driver data sheet. The first two are associated with both PLL and non-PLL clock drivers. The third, phase jitter, is only associated with PLL based clock drivers.

Cycle-to-cycle jitter is the difference in time between the periods of any two adjacent clock cycles. Period jitter is the deviation of time of individual periods of a signal with respect to an ideal period. Phase jitter represents the timing variation of the output with respect to the input associated with a PLL clock driver. **Figure 8** shows the three types of jitter along with the associated mathematical definitions.

Additional details of skew and jitter may be found in the Motorola Application Note, AN1934.

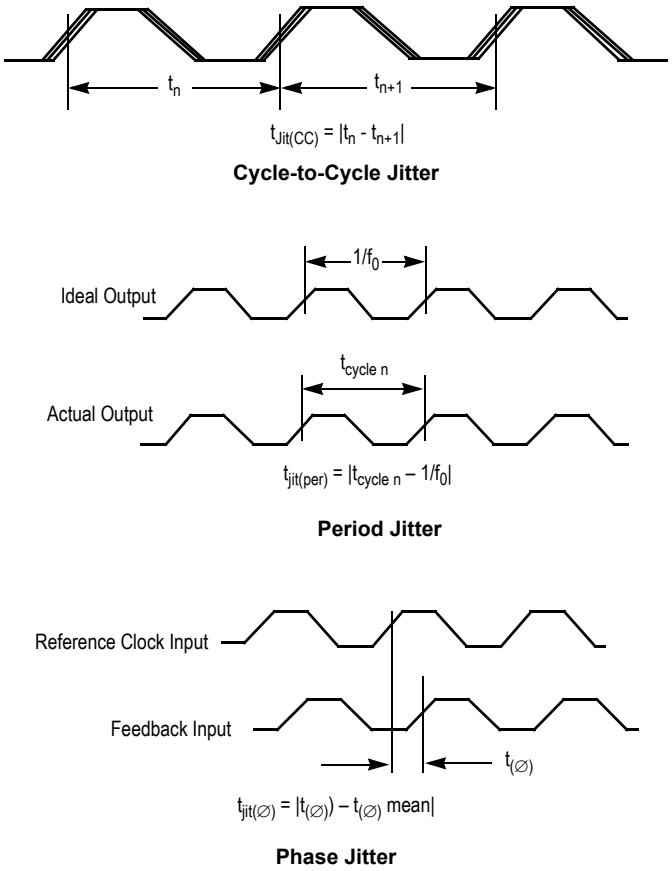


Figure 8. Clock Jitter

AC Characteristics — Tracking Bandwidth

PLL clock drivers lock on to an input reference frequency and remain locked to that frequency. If that reference frequency varies, the PLL will follow that frequency and remain locked to the new input frequency. However, if the input frequency varies at a rate faster than the PLL can keep up with, then the output frequency will not track the input reference change and the PLL with appear to ignore the variation in the input frequency. The point that the PLL does not follow input frequency changes defines the upper bound of the PLL bandwidth.

The bandwidth of a PLL has a transfer characteristic much like a transfer characteristic of a lowpass filter. The bandwidth characteristic can be used to an advantage in certain clock applications. Higher frequency noise or jitter on the reference clock input can be filtered by this characteristic. Input jitter above the bandwidth will not pass to the output of the VCO while input jitter below the bandwidth will pass through to the output.

Bandwidth of the PLL clock driver varies based upon the actual design of the PLL. One of the components that affect the bandwidth is the feedback divide ratio. **Figure 9** shows a typical PLL clock generator and its bandwidth curves. PLL clock drivers that have selectable feedback divide ratios also have variable bandwidths. Higher divide ratios lower the bandwidth of the PLL clock driver.

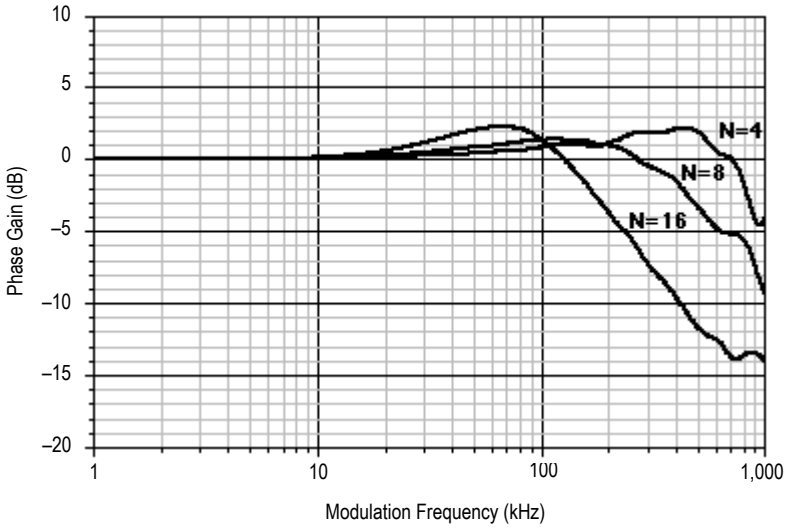


Figure 9. PLL Clock Generator Bandwidth

PLL Clock Driver Categories

Motorola PLL clock drivers are sorted into three different categories. The three categories are frequency synthesizers, clock generators, and zero-delay buffers. Although the categories are based upon the intended application, each category also reflects some uniqueness of the AC characteristics of the PLL.

Frequency Synthesizers

The first category of PLL based clock drivers is clock synthesizers. Clock synthesizers usually start with a low frequency clock source, which may come from an external source or from a crystal oscillator. This low frequency source may be further divided to produce an even lower PLL input reference frequency. With the use of the PLL, the low frequency reference frequency is multiplied up to the desired output frequency. If the device has a crystal oscillator as a reference, the oscillator circuitry would typically be part of the IC circuitry with the only required external component that of a crystal.

The clock synthesizer usually has output frequency steps with fine granularity or resolution such as 1 MHz. The overall output frequency of the clock synthesizer may be as high as 850 MHz. Examples of Motorola clock synthesizers are MPC9229, MPC9230, and MPC9239. The MPC9229 and MPC9230 each start with a midrange clock source, typically 16 MHz. This input frequency is divided by 16, which then becomes a 1 MHz input reference to the PLL. A programmable feedback divider then effectively multiplies this reference to the VCO frequency. The VCO frequency is then divided to produce the desired output frequency, as shown in **Figure 10**.

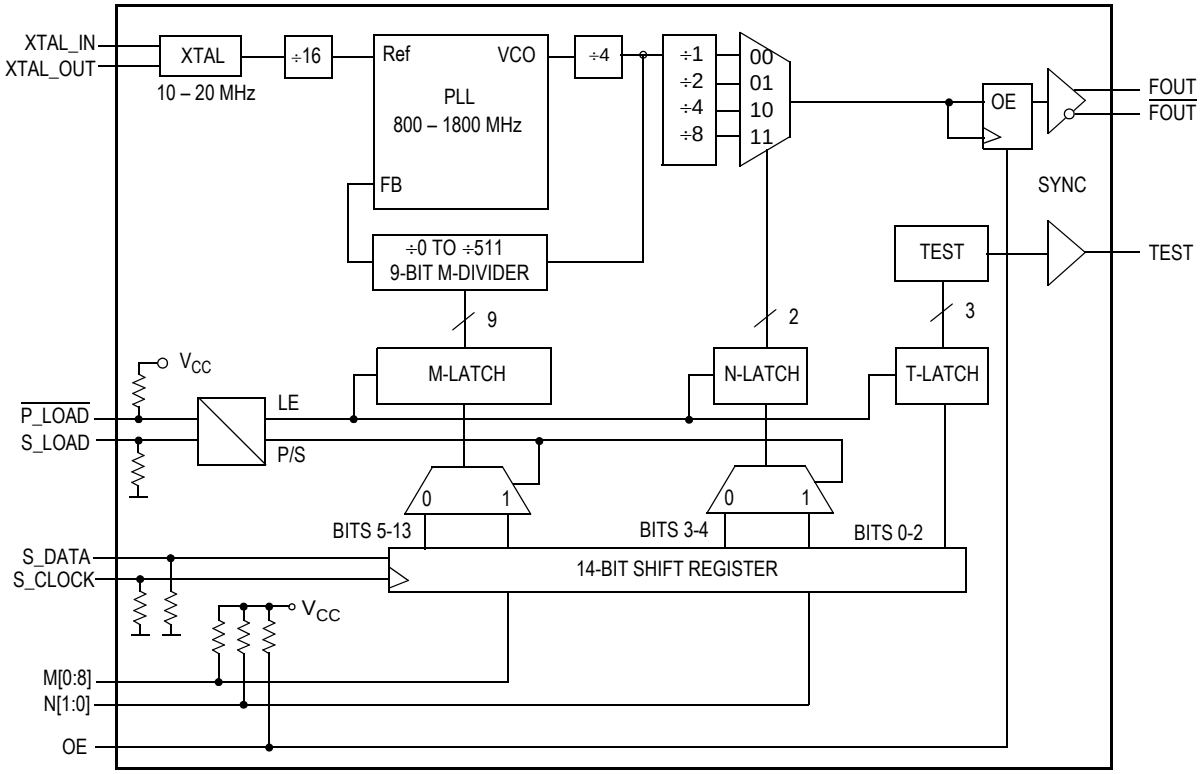


Figure 10. MPC9229 Frequency Synthesizer

A frequency synthesizer usually has a limited number of outputs; either one or two. The output frequency may be configurable in the user application. The ability to change the output frequency in small steps allows the circuit designer to do frequency margining. This is a technique where the system frequency is gradually increased/decreased while analyzing system performance.

The bandwidth of frequency synthesizers is usually the lowest of the three clock driver categories. Typical bandwidths for clock synthesizers are usually 30 to 50 kHz.

The clock synthesizer allows the system design to use a low frequency and low cost crystal oscillator and multiply the frequency up to the actual desired frequency, thus reducing the cost of the high frequency clock generation.

Clock Generators

Clock generators are used to generate clocks that are synchronous and phase aligned to an input reference clock. The category of clock generators make up the largest portion of Motorola's portfolio of the three categories of PLL based devices.

These devices typically have multiple outputs which are often grouped into multiple banks of outputs. Each bank can be set up for a different frequency. The previously discussed MPC9351 device is in the category of clock generators and, as we saw from the block diagram, it had nine outputs which were spread across four banks of outputs.

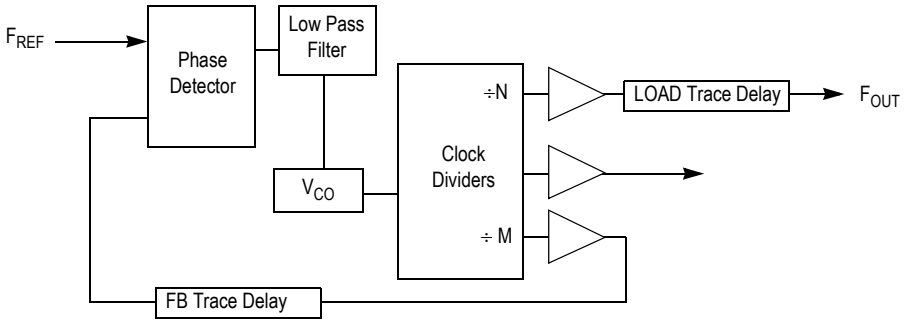
The output frequency adjustment step is usually more coarse than with the clock synthesizer. The reference frequency for a clock generator might be 15, 20, or 25 MHz, which would set the frequency step to a minimum of 15, 20, or 25 MHz. In some applications the previously discussed clock synthesizer might be used to generate the input clock for clock generators. Some clock generators have a crystal oscillator circuitry built-in.

The bandwidth of a clock generator is higher than that of a clock synthesizer and may be in the range of 300 to 500 kHz. This is considered to be a midrange bandwidth device. Clock generators maintain a phase relationship between the input clock and the output clock.

Zero-Delay Buffers

The third category of PLL clock drivers is zero-delay buffers. The concept of a zero-delay clock buffer for clock distribution may be a bit foreign, but with the use of a PLL, the concept is quite possible. The category of zero-delay buffers offers a higher bandwidth PLL than the clock generator category. Typical bandwidths are 1 to 2 MHz.

The zero-delay buffer maintains a known and precise phase relationship between the input and output clock waveforms. By adjustment of the feedback path delay, the output clock waveform may be aligned exactly to the input clock. This feedback path delay would typically be produced by the length of the PC board trace. Knowing the characteristics of the PC board material and the construction of the trace on the board can produce precise delays. Typical trace delays might be 1 to 2 ns per foot. Thus, a few inches of PC board trace can shift a clock output relative to the clock input by a significant amount. **Figure 11** shows a zero-delay buffer and the equations that define the effective delay of the clock through the device. The parameter of $t(\phi)$ is the effective delay of the zero-delay buffer. The Load Trace Delay shown on one of the clock outputs is the normal trace delay that is produced by routing the clock across the PC board. The effect of this delay can be effectively eliminated with the use of a zero-delay buffer.



$$Ref\_to\_output\_delay = t_{(\varnothing)} - (t_{FB\_DELAY} - t_{LOAD\_DELAY})$$

or

$$Ref\_to\_output\_delay = t_{(\varnothing)} + (t_{LOAD\_DELAY} - t_{FB\_DELAY})$$

Figure 11. Zero-Delay Buffer

Although the zero-delay clock buffer is PLL based and shares many of the same characteristics with the clock generator, it typically has better jitter and skew performance.

Clock Distribution Buffers

In addition to the PLL based clock drivers, Motorola offers a number of devices classified as distribution buffers. There are two categories: LVCMOS single-ended output and differential clock output buffers.

Figure 12 shows two of the LVCMOS output devices. The MPC961C and the MPC961P have the same number of outputs with the same output AC characteristics; however, they differ on the type of inputs. The MPC961C has LVCMOS inputs while the MPC961P has LVPECL compatible inputs. The devices can distribute an “at frequency” clock to many locations on a PC board. Some of these clock buffers offer a built-in divider block to be able to optionally divide the input clock by two. Care should be used when using this optional divider as a half frequency output can induce additional noise and thus cause jitter to the full frequency clock.

Figure 12. LVCMOS Clock Buffers, MPC942C and MPC42P

As previously mentioned, one of these categories of clock buffers have differential outputs. These outputs, and typically the input, are LVPECL or HSTL levels. Differential input and output signals offer many advantages as are discussed in the following section. An example of a differential output buffer is the MC100ES6111 differential clock driver shown in **Figure 13**. It has LVPECL inputs and 10 pairs of LVPECL outputs.

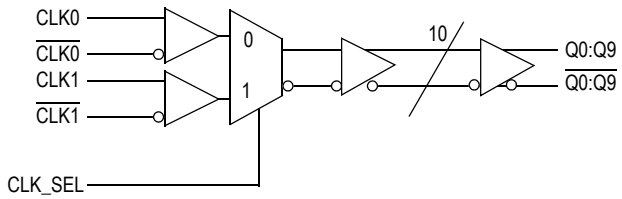


Figure 13. Differential Output Buffer MC100ES6111

Clock Redundancy

Some systems require a backup or redundant clock to be generated. **Figure 14** shows two applications of a redundant clock system.

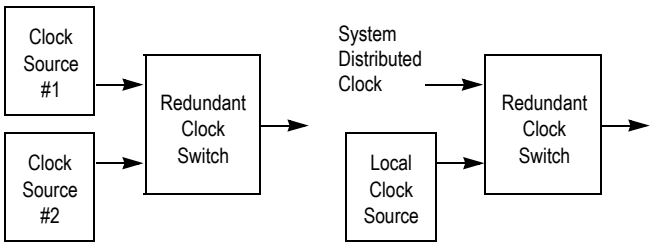


Figure 14. Redundant Clock Applications

The diagram on the left of **Figure 14** shows a redundant main clock being sourced from two different central clock generation points and distributed over a cable or backplane. In this application, the redundant clock switch assures that a clock is available in the event of a removed clock board or a dead clock source.

The diagram on the right of **Figure 14** shows a locally generated clock is available as a backup clock and must be switched in when the main clock fails. The redundant clock switch must make the transition from the current clock source to the backup clock in a smooth manner. While the transition takes place, the output of the clock generator must be stable with no disruption in the clock signal. The generation of runt pulses or short cycle clock periods must be avoided.

Motorola offers the MPC9993 Intelligent Dynamic Clock Switch as shown in **Figure 15**. The input clock sources come through the differential pair inputs of CLK0 and CLK1. The device automatically selects the good input and supplies this to the PLL. On detection of a clock failure, the device smoothly switches to the second input and continues to supply a clock to the PLL. A clock failure is defined as the input clock pins stuck high or low for at least one clock period. Status outputs from the Dynamic Switch Logic provide an indication of the current clock source.

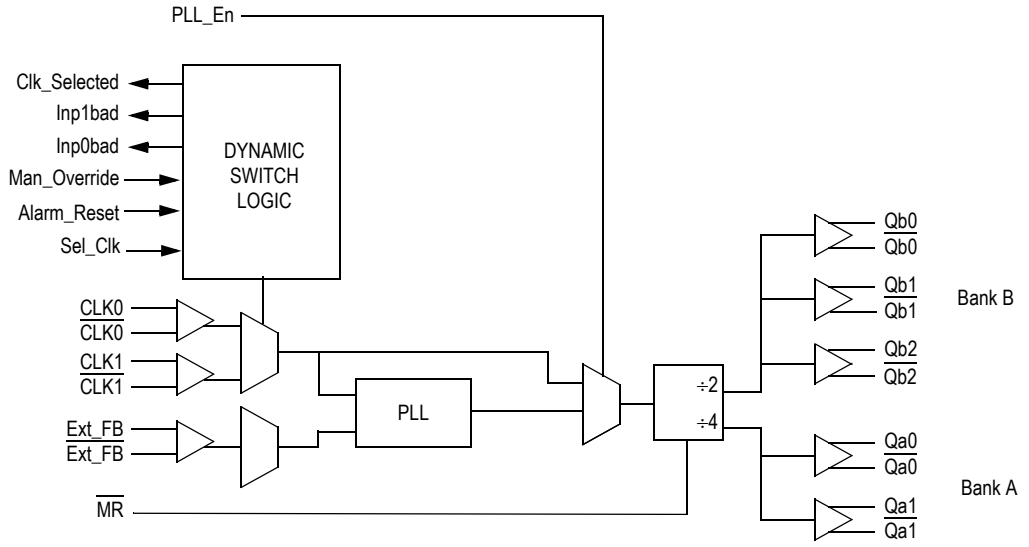


Figure 15. MPC9993 Redundant Clock Generator

The specification for the MPC9993 lists the maximum rate of period change as this clock switch is made. The data sheet also lists the typical delta period/cycle of 200ps/cycle. An actual clock switch may take as many as 100 to 200 clock cycles to complete. And as a result, the output will appear to be a “graceful” change from one clock source to the next. The automatic valid clock reference detection function may optionally be disabled and the clocks may be selected/switched manually.

The multiple outputs of the MPC9993 provide drive capability for several application system interfaces for the output clock as well as providing the feedback input to the PLL. The VCO for this device runs at 4X the input clock frequency. The outputs of the MPC9993 are grouped into two banks. Bank A is the input clock divided by 4 and has two outputs. The output of this bank is typically used for the feedback to the phase detector. Bank B consists of 3 separate outputs and is the input reference divided by 2.

Figure 16 shows a possible connection for a redundant clock system using the MPC9993. The main clock reference comes externally from the system while the backup clock comes from a MPC9229 crystal oscillator based source. One pair of the differential Bank A outputs are routed back to the EXT_FB inputs. The remaining Bank A pair of outputs and Bank B outputs are available for system usage.

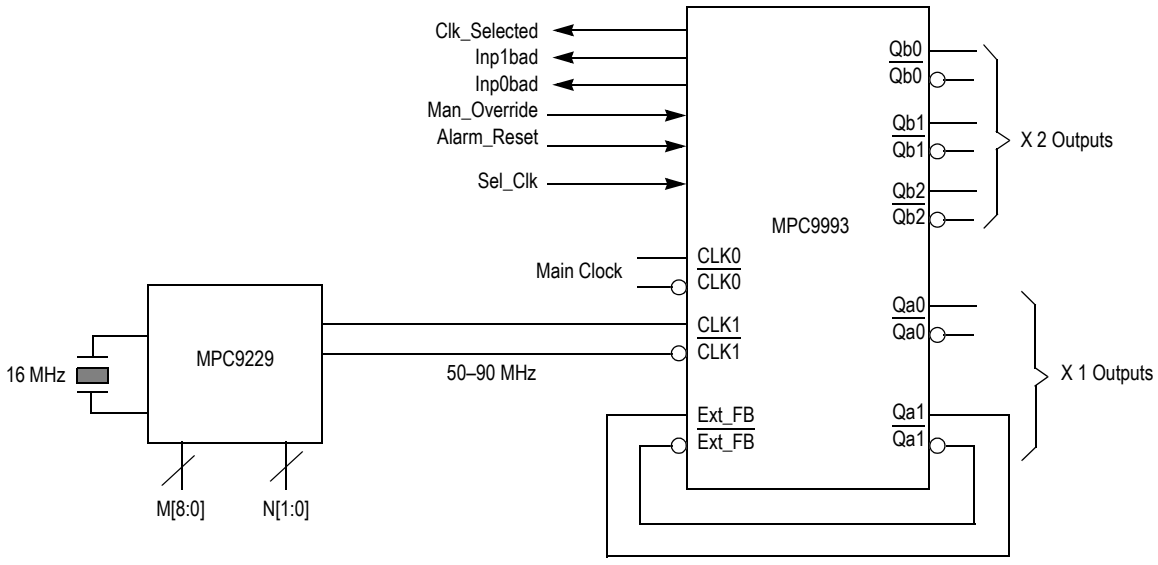


Figure 16. MPC9993 Redundant Clock Application

Figure 17 shows the “switchover” from the current clock to the backup clock. Clock A and Clock B represent the two available clock sources. When Clock A fails, this triggers the switch to Clock B. The MPC9993 slowly slews to the phase of Clock B and, after many input clock cycles, the output clock is in phase with Clock B.

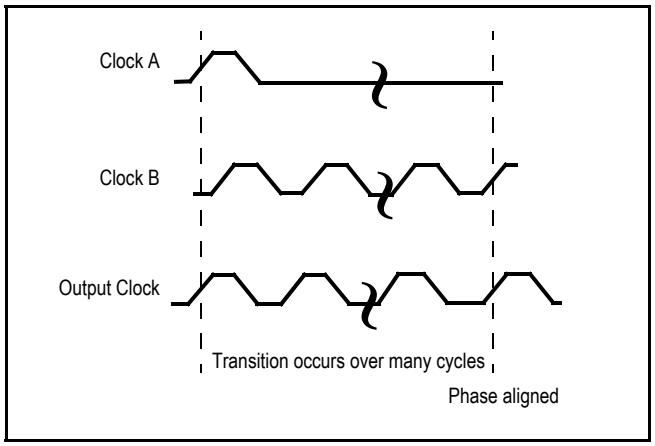


Figure 17. MPC9993 Clock Switch

Clock Tree Design and Layout

Clock performance can be predicted by understanding the clock functionality and data sheet parameters for jitter and skew, but the overall clock performance is highly dependent on design of the clock circuitry and its environment on the PC board. The following sections point out areas of clock design that need special attention to ensure the best clock performance obtainable from the design. The first of these topics is that of power supplies.

Power Supplies

Noisy power supplies have an affect on clock trees by generating jitter on the clock outputs. This is due to the noise on the power supply affecting the input-switching threshold and/or modulating the input control voltage to the VCO. Many of the Motorola clock generators offer separate PLL power pins, allowing for the isolation of the PLL power from the output driver supply. Use lots of high quality filter caps and (physically) place them as close to the clock driver package as possible.

Most of the PLL clock driver devices are analog devices. These drivers are designed with separate power supply connections for the outputs and the PLL analog circuitry. The example shown in Figure 18 separates out the analog supply, V_{CCA}, from the supply driving the rest of the chip. A simple RC filter decreases the noise injected into the analog supply pin, minimizing the jitter due to power supply noise. The value of R_S must be calculated based up the maximum I_{CCA} current. Filter caps should be of high quality for best overall frequency characteristics. Noisy power supplies may significantly compromise good clock tree designs on paper.

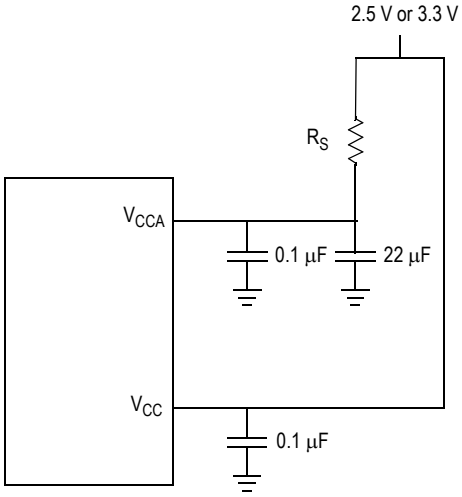


Figure 18. Power Supply Filtering

PC Board Trace Impedance Matching

In system applications utilizing high frequency clocks and/or microprocessor bus speeds, the PC board traces are characteristic transmission lines and must be treated appropriately. Termination of the transmission line must be done in order to minimize reflections and maintain proper signals in the system. Either parallel termination or series termination may terminate clock-signaling lines. Each method has advantages.

Parallel termination places a resistor on the load end of the transmission line. The value of the termination resistor is equal to the impedance of the transmission line. Figure 19 depicts the parallel termination on a clock line with the associated waveform of a clock edge propagating down the line. Since the parallel termination is equal to the characteristic impedance of the line, there is no reflection when the clock edge reaches the load.

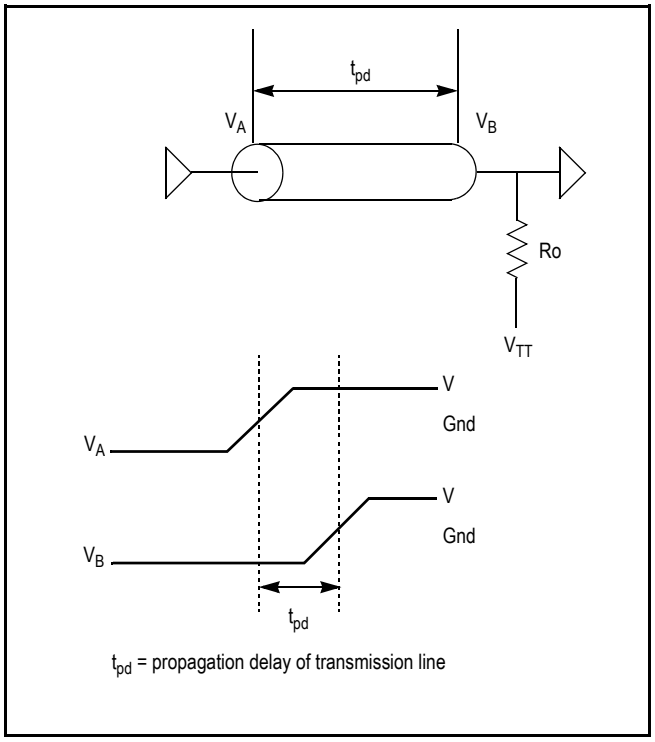


Figure 19. Parallel Termination with Waveform

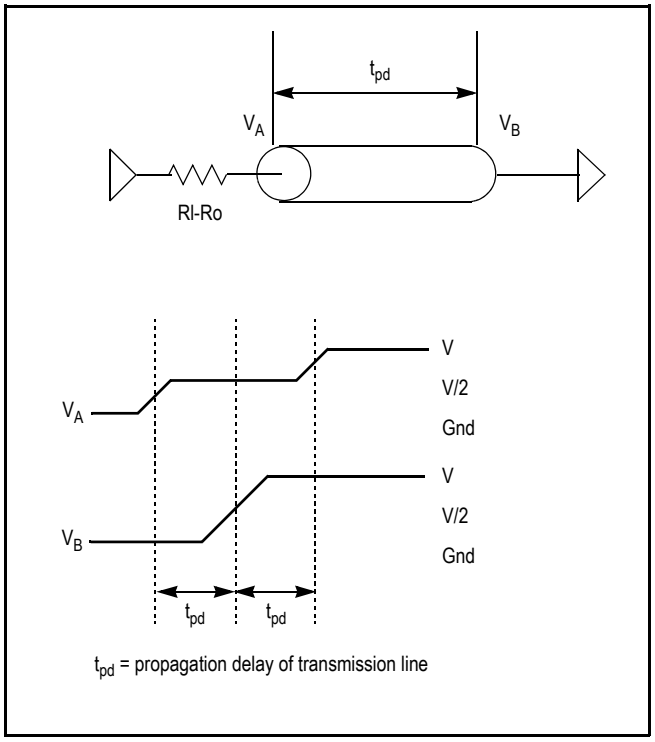


Figure 20. Series Termination with Waveform

Series termination places a resistor on the source end of the transmission line and in series with the transmission line. The resistor value is chosen such that the output impedance of the clock driver output buffer, plus this resistor, equals the characteristic impedance of the transmission line. No termination impedance is placed at the load end of the transmission line.

Figure 20 shows the waveform of a clock edge as it appears on the output of the clock driver and as it propagates down the transmission line. As the clock edge starts down the transmission line, the series resistor and the impedance of the transmission line act as a voltage divider causing an edge of amplitude V/2 to be propagated. After t_{pd} time period, the edge arrives at the load end of the transmission line. This point appears to be an open line to the propagated edge causing a reflection of the edge of amplitude V/2 to be sent back to the source. On arrival at the source, the reflected waveform encounters the series termination which damps the reflected voltage and the waveform establishes a steady state. Since the voltage at the source is V and the voltage at the load is also V, there is no current flow down the transmission line other than the initial charging of the line.

The advantage of series termination is that there is no steady state loading on the line and thus the steady state drive requirements of the clock driver is low.

Single-Ended Verses Differential Clock Lines

Distribution of clock signals via differential paths has several advantages over single-ended clocks. Most of these advantages relate to noise immunity.

Even though the differential clock complicates the routing of the PC board by doubling the number of traces, differential clocks may ease the PC board layout due to ground plane issues.

All currents are in the signal traces for the differential pair and not in the underlying ground plane. Thus, the effects of breaks or discontinuities in the PC board ground plane within the vicinity of the clock drive circuitry are minimized. In addition, since one output or the other is always driving a signal, the constant supply current leads to V_{CC}/Ground Bounce reduction.

There are many detailed references dealing with the subject of PC board layout and transmission line characteristics, which should be consulted for additional information.

Steps in Selecting a Clock Driver

Now that we have looked at the definitions, characteristics, and categories of clock driver devices, the question is, “How do I choose the devices or devices that fit into my application?” The following list of questions should be answered in order to understand what type of clock drivers are required.

1. What are the input and output requirements for logic levels in the application?
2. Does the application have or require differential input or output?
3. What is the clock source? Is it externally provided? What is the frequency?
4. Is a PLL based clock driver required?
5. What are the output frequency requirement(s)?
6. What number of outputs at each frequency is required?

Once these user application questions are answered, the next step in the clock design is to consult the Advanced Clock Driver Selector Guide for devices that match these requirements. If a PLL clock driver is needed, determine the feedback divide ratio and determine if the allowable VCO range is met. Once the VCO frequency is determined, next determine the output divide ratios required meeting output frequency requirement(s). Once a potential device has been selected, evaluate the jitter and skew specifications of that device based upon the system parametrics.

SUMMARY

Whether the clock design is simple or complex, the performance of the clock circuitry can best be optimized by an understanding of the parameters of the clock devices involved in the design. Many parameters may be of little or no importance to the design; however, the designer should understand these parameters and make that determination. Finally, clock tree design should be given proper attention to ensure the reliability of the system design.

Clock Driver Resources

AN1934/D — Effects of Skew and Jitter on Clock Tree Design

DL207/D — Advanced Clock Drivers Device Data Book

SG392/D — Advanced Clock Drivers Selector Guide

Order number: AN1933
Rev 0, 07/2004

AN1993

Clock Generation for PowerQUICC III

By: Don Aldridge

INTRODUCTION

The MPC8560/40 or PowerQUICC III processors are the latest in a family of communications and control processor devices produced by the Motorola Semiconductor Networking and Communications Systems Group. These processors provide high-end computing and networking communications platforms for Telecom, Networking, and other communications applications. The purpose of this document is to discuss clock requirements for this family of microprocessors and to provide reference methods to generate these clocks. Included in this document is the introduction and discussion of a single-chip clock generator designed specifically to meet the PowerQUICC III clock requirements.

POWER QUICC III CLOCK REQUIREMENTS

The clock requirements for the MPC8560/40 or PowerQUICC III family are three-fold and consist of:

1. A system clock for the processor CPU.
2. A RapidIO™ interface clock
3. One or more communications clocks for Ethernet, Gigibit Ethernet etc.

All three of these clock inputs are typically independent of each other in both frequency and phase. Also, the exact frequency of each clock is overall system dependent.

The system clock input of the PowerQUICC III drives the main CPU or what is referred to as the e500 core. The exact frequency of this input clock is set by the system bus frequency requirement and is at a lower frequency than the core frequency. This bus frequency is then internally multiplied by the PowerQUICC III architecture to the final CPU frequency. **Figure 1** shows the system clock generation circuitry internal to the MPC8560 PowerQUICC III. The system clock input is labeled SYSCLK/PCI_CLK and the PowerQUICC III internally multiplies this input frequency to the desired internal CPU frequency with an internal PLL (Phase Lock Loop). This multiplication is actually performed in a two-step process with two separate PLLs. The intermediate clock frequency, labeled CCB_clk is the core complex clock and is also referred to as the platform clock. This clock is used by the synchronous system logic of the PowerQUICC III. The e500 core clock is labeled core_clk and is generated from the CCB_clk with a separate internal PLL.

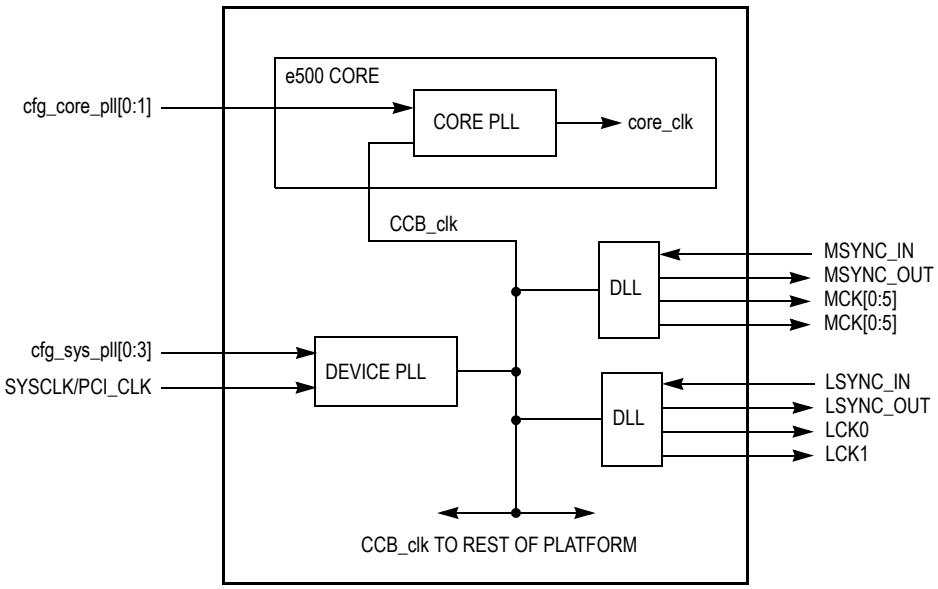


Figure 1. PowerQUICC III System Clock

Configuration inputs to the PowerQUICC III are used for setting the ratio of the CCB_clk to the SYSCLK and for setting the ratio of the core_clk to the CCB_clk. Details of these inputs and the allowable clock configurations are found in the PowerQUICC III Electrical Characteristics document. The SYSCLK frequency may range from 16 MHz up to 133 MHz. The system clock for the PowerQUICC III is a single-ended 3.3 V LVCMOS voltage input.

The RapidIO™ transmit clock input sets the data rate for the RapidIO™ data transfer bus. This clock input is a differential LVDS clock and may be configured for up to 500 MHz. This single differential LVDS input pair to the PowerQUICC III is used to drive the entire RapidIO™ circuitry. **Figure 2** shows the RapidIO™ clock circuitry internal to PowerQUICC III.

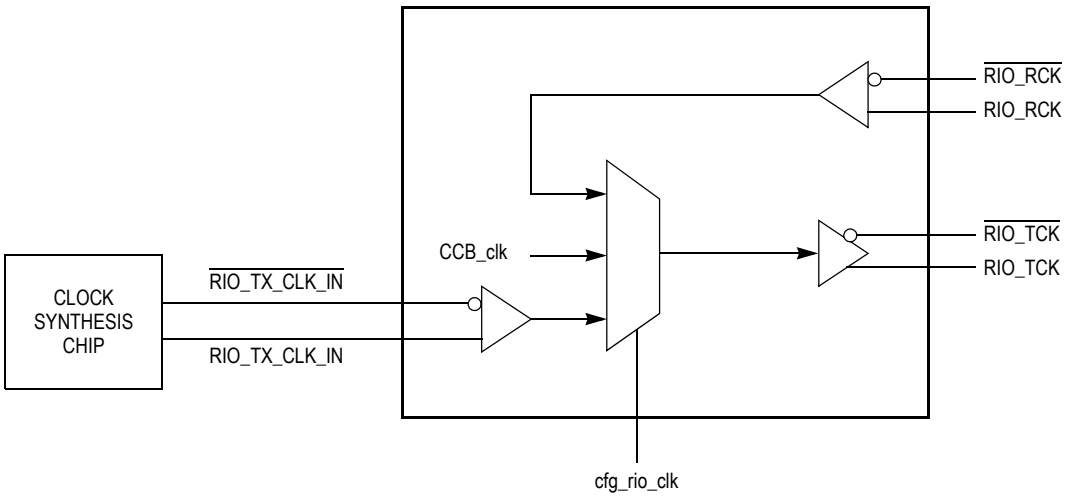


Figure 2. PowerQUICC III RapidIO™ Transmit Clock

The Gigibit Ethernet Interface input clock requirement is a LVCMOS clock at 125 MHz. This clock may be sourced directly to the PowerQUICC III or more typically comes from the externally supplied “PHY” for the Gigibit Ethernet Interface. The input frequency to the PHY may be at 125 MHz or as is quite often the case, derived from a lower frequency such as 25 MHz. The PHY then provides the 125 MHz required by the Gigibit Ethernet clock input. The data sheet for the desired PHY should be consulted for this information.

Other communication interfaces for the PowerQUICC III may require other clock inputs, however these frequencies vary and are dependent on the specific communications interface.

The PowerQUICC III memory clock requirements are handled by two DLLs (Delay Lock Loop) contained in the PowerQUICC III. The PowerQUICC III has two memory bus types, which are main and local memory. Main memory uses DDR memory and local memory uses SDRAM memory. The Main Memory DLL has six differential clock outputs for connection to memory modules. In addition a delay loop for adjusting the timing of the clock waveforms is provided. This delay loop consists of an MSYNC_OUT output and a MSYNC_IN input. A trace on the PC board will be used to connect the MSYNC_OUT to the MSYNC_IN with the trace length based upon specific board layout. The length of delay loop trace is used to adjust the edge timing of the memory clock at the clock module input. The Local Memory DLL has two LVCMOS clock outputs and similar delay loop input and output signals.

CLOCK GENERATOR FOR THE POWERQUICC III

Deriving these clocks for the PowerQUICC III may be done in a variety of ways. A separate crystal oscillator, at the required frequency, for each clock input may be considered. Crystal oscillators are available in a wide range of frequencies up to approximately 150 MHz. If multiple copies of a specific clock are required, the oscillator output should be buffered with a clock fanout buffer such as the MPC9443 1:16 fanout buffer, or the MPC9446 1:10 fanout buffer.

Also a PLL based clock generator or frequency synthesizer may be used to produce the desired clock tree by multiplying a lower frequency oscillator to the desired frequency or frequencies. Recommended clock generators are the MPC9772/3 or the MPC9600. The MPC9772/3 are 12 output LVCMOS output clock generators. The MPC9772 accepts either a LVCMOS clock input or has a crystal oscillator requiring only a user supplied crystal for frequency selection. The MPC9773 accepts either a differential LVPECL clock or a single-ended LVCMOS clock input. The MPC9600 PLL based clock generator has a total of 21 clock outputs and uses either a LVCMOS or LVPECL clock input.

The high frequency requirements of the RapidI/O clock would typically require the use of a clock synthesizer. Devices such as the MPC9239 are capable of producing up to 900 MHz clocks. This synthesizer uses as a reference a 16 MHz user-supplied crystal and has a single LVPECL output. This output may be programmed to any frequency across its output range

in 16 MHz steps. A special derivative of this synthesizer, the MPC9259, provides LVDS outputs matching the input requirements of the PowerQUICC III.

Motorola has created a clock generator specifically for the PowerQUICC III. The following information provides details on this single PLL based clock generator/fanout buffer that supplies all of the PowerQUICC III clock inputs. This unique clock generator/fanout buffer is the MPC9850 and is discussed in the following section.

MPC9850 CLOCK GENERATOR

The MPC9850 has been designed to supply the clocking requirements for the MPC8560/MPC8540 PowerQUICC III processor series in a single low cost package. This clock uses commonly available reference sources for the clock source and is packaged in a 100-ball MAPBGA package. This package is targeted for both low cost and high functionality applications. **Figure 3** shows a block diagram of the MPC9850.

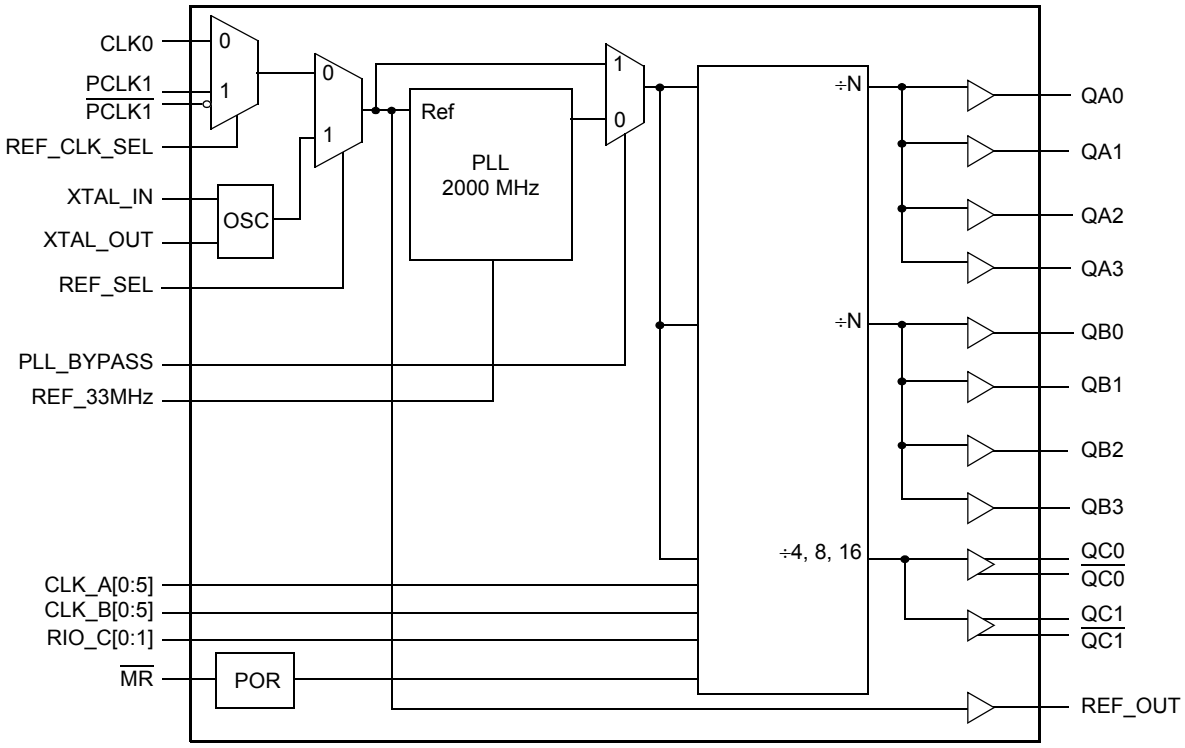


Figure 3. MPC9850 Block Diagram

The MPC9850 has a total of 8 LVCMOS outputs divided into two banks of four outputs per bank. Output Bank A and B provides LVCMOS output clocks and each bank is selectable between 3.3 V and 2.5 V operation. The two banks are independently programmable to any of the large selection of output frequencies. Commonly used system frequencies available include 16, 33, 50, 66, 83, 100, 111, 125, 133, 166 and 200 MHz. A series of six (for each bank) frequency selection pins are used for configuration of the output frequency on each bank. A table in the data sheet lists the programming values for the above listed commonly used system frequencies. Additional output frequencies are available from the MPC9850. Although not listed in the table the programming configuration of the additional frequencies can be calculated with a simple output frequency equation as shown in the MPC9850 data sheet. These two banks of outputs would typically provide the system clock for the PowerQUICC III with additional outputs available for other system frequency inputs.

A third bank of outputs, Bank C, delivers the RapidIO™ clock output of up to 500 MHz. Output levels on this bank provide the required LVDS I/O levels. LVDS (short for Low Voltage Differential Signaling) provides a differential clock drive that is intended for higher frequency clock distribution. Two frequency configuration pins are used to select between the three standard RapidIO™ frequencies of 125, 250 or 500 MHz. A fourth frequency of 50 MHz is used for factory test.

The clock input for the MPC9850 may be provided by any one of 3 source types. These are either a single-ended LVCMOS reference, a LVPECL differential reference or an crystal oscillator. For crystal oscillator operation an externally supplied crystal is connected to the MPC9850s internal oscillator. The frequency source may be either 25 MHz or 33 MHz. For crystal oscillator operation a 25 MHz crystal must be supplied. The crystal should be specified as a fundamental mode crystal with a 20 pF load. The reference output is also buffered to an output pin for system usage.

The MPC9850 is a PLL (phase locked loop) based clock generator. PLL based clock generators work by multiplying a low frequency reference to a frequency that is typically higher than the highest desired output frequency. This higher frequency is then divided down to the desired output frequency or frequencies. Using the high frequency capabilities of SiGe:C

technology, the MPC9850 PLL multiplies the 25 or 33 MHz reference input to 2000 MHz. The multiplication factor is either 80, for a 25 MHz reference or 66 for a 33 MHz reference. By using configurable output dividers the 2000 MHz VCO frequency is divided to the required output frequency(s). Separate dividers are used for output banks A and B, thus making these two output banks independently configurable.

The MPC9850 requires no external loop filter components for the PLL. Each output is capable of driving a single 50-ohm transmission line for clock distribution on the PC board. Proper termination of each output is required to minimize transmission line reflections.

The 100 lead MAPBGA package provides an optimal number of power and ground connections to minimize jitter, output skew and ground bounce. The package pitch is 1.0 mm spacing to ease PC board layout and manufacturing.

PowerQUICC III CLOCK SYSTEM CONFIGURATION

Figure 4 shows the MPC9850 clock generator supplying the clocks to a MPC8560/40 PowerQUICC III processor system. In this application the MPC9850 supplies a 66 MHz system clock, a 500 MHz RapidIO™ clock and a 25 MHz Gigabit Ethernet PHY clock.

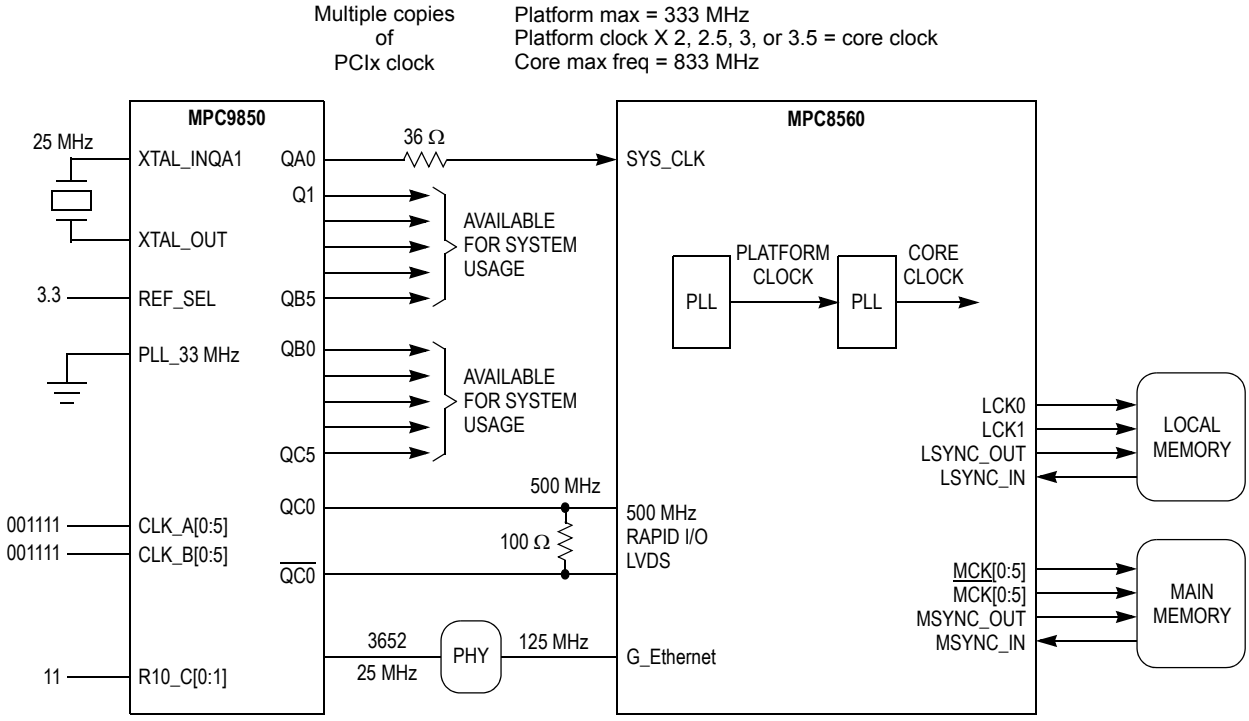


Figure 4. System Block Diagram MPC8560/40 w/MPC9850 Clock Generator

For this reference design, the clock source is a 25 MHz reference, generated by a crystal attached to the MPC9850's XTAL_IN and XTAL_OUT oscillator pins. The crystal requirements are parallel resonance fundamental crystal with a specified load capacitance of 20pf. This crystal is of a standard frequency and load specifications and readily available from most any crystal manufacturer or electronics parts supplier. The REF_SEL input is configured for a crystal oscillator source and the Ref_33MHz pin is configured for a 25 MHz reference frequency.

Output banks A and B drive the processor system. The bank A output, QA0, is connected to the PowerQUICC III SYS_CLK input leaving the remainder of Bank A and all of Bank B for other system clock applications. Both banks are configured for 66 MHz; however, Bank B could be configured for 33 MHz if the 33-MHz PCI clock is needed. All outputs should be properly terminated for the PC trace impedance. Termination may be either series or parallel terminated. In this design, series termination is used and based upon a board trace impedance of 50 ohms, a 36-ohm series resistor is used. For optimum signal integrity it is recommended that any unused outputs be terminated. If not terminated, these unused outputs should remain completely unconnected to any PC board trace. Transmission line termination will be further discussed in a following paragraph.

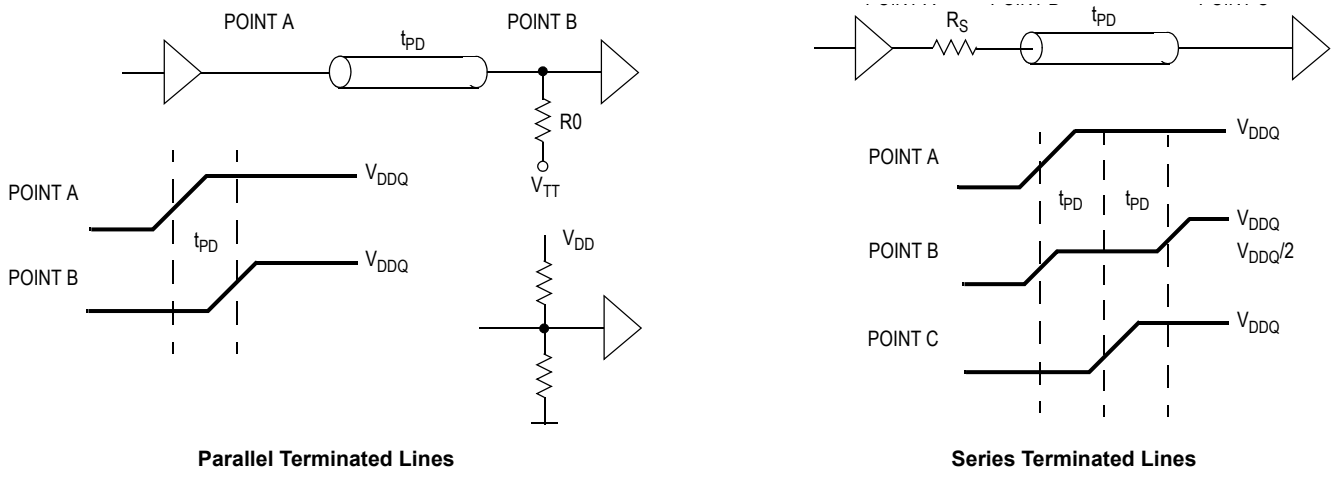
The RapidIO™ input of the PowerQUICC III is connected to one of the two Bank C outputs and is configured for a 500 MHz clock. This output should be terminated with a differential connection of a 100-ohm resistor at the input of the MPC8560/40.

The REF_OUT output of the MPC9850 is used to supply a 25 MHz reference to the input of the typical user selected Gigibit Ethernet PHY. This reference clock output is a buffered copy of the input reference and does not go through the clock generator PLL. This provides a frequency accurate and jitter free source for Ethernet applications.

TRANSMISSION LINES

As previously mentioned, all clock outputs should be properly terminated according to the PC board transmission line characteristics. Either series or parallel termination method may be used. The above reference design uses the popular series termination technique.

Series termination uses a small valued resistor in series with the clock driver output. This resistor is located close to the clock output. The value of this resistor is chosen in conjunction with the output impedance of the clock driver output such that the sum of the driver output impedance plus the series resistor equals the PC board characteristic impedance. A clock driver output impedance of approximately 14 to 18 ohms would be combined with 32 to 36 ohms to match a 50-ohm transmission line. The far end of the clock transmission line directly connects to the high impedance input of the microprocessor or other receiver input. For series termination, there is no resistor at the clock receiver input. Series termination relies on the fact that there is a high impedance at the far end of the transmission line and a 100% waveform reflection occurs when the clock edge reaches the far end of the transmission line. Advantages of series termination are a single resistor requirement and the steady state current draw due to the transmission line is zero. Disadvantages are the resistor value is dependant on the clock driver output impedance.



Parallel Terminated Lines **Series Terminated Lines**

Figure 5. Transmission Line Termination

Parallel termination uses a termination resistor equal to the characterization impedance of the PC board transmission line and is located at the receiver end of the transmission line. This resistor is located at the input of the PowerQUICC III input and is connected from the input to a constant voltage source referred to as V_{TT}. V_{TT} for a LVCMOS input is typically defined as $V_{DD}/2$. The parallel termination resistor value is independent of the output impedance of the clock driver output. Therefore, for a 50 ohm PC board trace impedance the parallel termination would use 50-ohm termination resistors. If a V_{TT} source is not readily available a Thevenin equivalent resistor combination may be used instead. This requires two resistors, one from input to V_{DD} and one from input to GND. The advantage of parallel termination is the independence of the resistor value from the clock driver output. The disadvantages are the requirement of the V_{TT} supply or two resistors, and the large steady state current draw of the transmission line.

Termination of the LVDS differential output requires a 100-ohm resistor. This resistor is located at the LVDS receiver input and is connected between the differential inputs.

Unused outputs should either be terminated (recommended) or left unconnected. If unconnected, the output pins of the MPC9850 should not have any PC board trace connected to them.

POWER SUPPLIES

The MPC9850 operates from a 3.3 V supply with either a 3.3 V or 2.5 V supply for the output drive. The power supply connections should be made with heavily bypassed supply planes. The MPC9850 has four types of power supply pins. These are V_{DD}, V_{DDOA}, V_{DDOB}, and the V_{DDA} pin.

V_{DD} is the main supply of 3.3 V to the MPC9850. The MAPBGA package provides several V_{DD} leads and all should be connected to the 3.3 V supply plane. The V_{DD} power plane should be heavily bypassed with small valued and small physical size capacitors with good high frequency characteristics. The capacitors should be located as close to the MPC9850 package as possible.

V_{DDOA} and V_{DDOB} are used to supply either 3.3 V or 2.5 V to Banks A and B output drivers. As with V_{DD} the MPC9850 has several pins dedicated to V_{DDOA} and V_{DDOB}, and all should be connected to the desired supply and properly bypassed.

Two V_{DDA} pins are used to supply a separate and noise filtered 3.3 V supply voltage to the analog sections of the MPC9850. These pins should be connected to the 3.3 V supply through the recommended RC filter for the best isolation of PC board generated power supply noise.

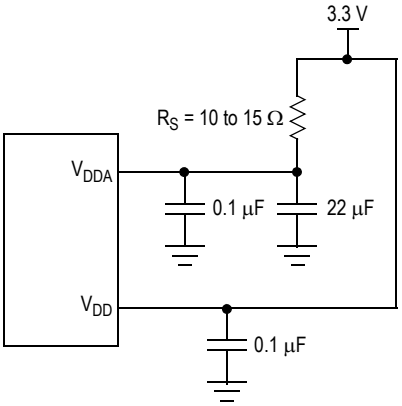


Figure 6. V_{DD} Analog Supply Pin

SUMMARY AND SUPPORT OF OTHER MICROCONTROLLERS AND MICROPROCESSORS

The MPC9850 was designed to supply the entire clock input requirements to a PowerQUICC III processor. Although the MPC9850 was specifically designed for the PowerQUICC III, many features make this clock generator applicable to other PowerPC, PowerQUICC or other industry standard microprocessors. The selectable output frequencies of the MPC9850 are also the system frequencies typically found in other processor based system designs.

In addition to the MPC9850, low cost derivatives of the MPC9850 are available. These are the MPC9855 and the MPC9817. The MPC9855 is a MPC9850 pin compatible clock generator that provides the same functionality of the MPC9850 without the RapidIO™ clock outputs. The MPC9817 clock generator is designed to provide common PCI clock frequencies in a low-cost 20-pin SSOP package. The device offers a single bank of 5 clock outputs that maybe configured for 25, 33, 50 or 66 MHz. The MPC9817 also offers a single bank of 3 outputs that provide the 25 MHz for I/O applications.

References

(1) MPC8560 User Manual
(2) MPC8560 Electrical Characteristics Guide
(3) MPC9443 Fanout Buffer Data Sheet
(4) MPC9446 Fanout Buffer Data Sheet
(5) MPC9772 Clock Generator Data Sheet
(6) MPC9773 Clock Generator Data Sheet
(7) MPC9600 Clock Generator Data Sheet
(8) MPC9239 Clock Synthesizer Data Sheet
(9) MPC9259 Clock Synthesizer Data Sheet
(10) MPC9850 Clock Generator Data Sheet
(11) MPC9855 Clock Generator Data Sheet
(12) MPC9817 Clock Generator

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Technical Information Center
3-20-1, Minami-Azabu, Minato-ku
Tokyo 106-0047, Japan
0120 191014 or +81 3 3440 3569
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

DL207
Rev. 2
8/2004