



STY130NF20D

N-channel 200 V, 0.010 Ω , 130 A, Max247
STripFET™ II with fast recovery diode Power MOSFET

Preliminary Data

Features

Type	V _{DSS}	R _{DS(on)} max	I _D
STY130NF20D	200 V	< 0.012 Ω	130 A

- Exceptional dv/dt capability
- 100% avalanche tested

Application

- Switching applications

Description

This Power MOSFET is produced using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. The STY130NF20D offers extremely fast switching performance thanks to the intrinsic fast body diode, making the device ideal for hard switching topologies.

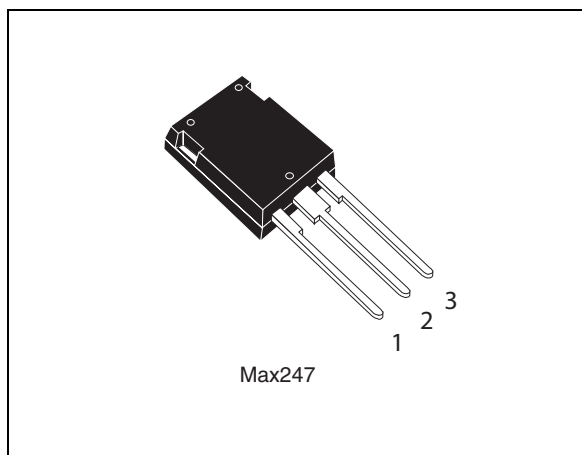


Figure 1. Internal schematic diagram

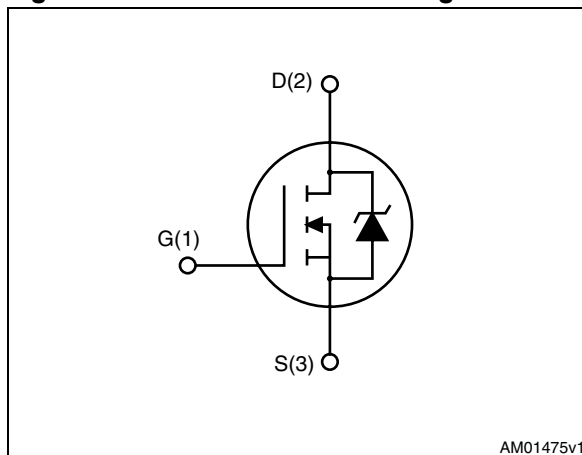


Table 1. Device summary

Order code	Marking	Package	Packaging
STY130NF20D	130NF20D	Max247	Tube

Contents

1	Electrical ratings	3
2	Electrical characteristics	4
3	Test circuit	6
4	Package mechanical data	7
5	Revision history	9

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	200	V
V_{GS}	Gate-source voltage	± 20	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	130	A
$I_D^{(1)}$	Drain current (continuous) at $T_C=100\text{ }^\circ\text{C}$	75.6	A
$I_{DM}^{(2)}$	Drain current (pulsed)	520	A
$P_{TOT}^{(2)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	450	W
	Derating factor	TBD	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	25	V/ns
T_J T_{stg}	Operating junction temperature Storage temperature	- 55 to 150	$^\circ\text{C}$

1. The value is rated according $R_{thj-pcb}$
2. Pulse width limited by safe operating area
3. $I_{SD} \leq 30\text{ A}$, $di/dt \leq \text{TBD A}/\mu\text{s}$, $V_{DD} \leq 80\% V_{(BR)DSS}$

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	TBD	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	$^\circ\text{C}/\text{W}$
T_L	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive ⁽¹⁾	TBD	A
E_{AS}	Single pulse avalanche energy ⁽²⁾	TBD	mJ

1. Pulse width limited by T_{jmax}
2. Strating $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	200			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{max rating}$, $V_{DS} = \text{max rating @ } 125\text{ °C}$			10 100	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 21\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$, $I_D = 65\text{ A}$		0.010	0.012	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs}	Forward transconductance	$I_D = 130\text{ A}$, $V_{DS} = 150\text{ V}$		TBD		
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$		9900		pF
C_{oss}	Output capacitance			2000		pF
C_{rss}	Reverse transfer capacitance			450		pF
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 130\text{ A}$		390		nC
Q_{gs}	Gate-source charge	$V_{GS} = 4.5\text{ V}$		TBD		nC
Q_{gd}	Gate-drain charge	(see Figure 3)		TBD		nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 400\text{ V}$, $I_D = 65\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 2)		TBD		ns
t_r	Rise time			TBD		ns
$t_{d(off)}$	Turn-off delay time			TBD		ns
t_f	Fall time			TBD		ns

Table 8. Source drain diode

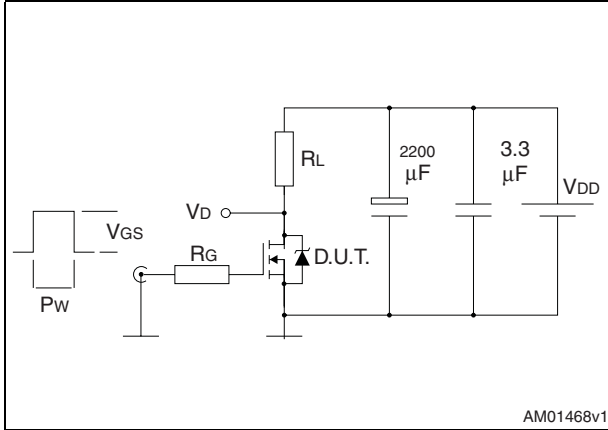
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				130	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				520	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 65\text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 65\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 100\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$		TBD		ns
Q_{rr}	Reverse recovery charge			TBD		nC
I_{RRM}	Reverse recovery current			TBD		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 μs , duty cycle 1.5%

Test circuit

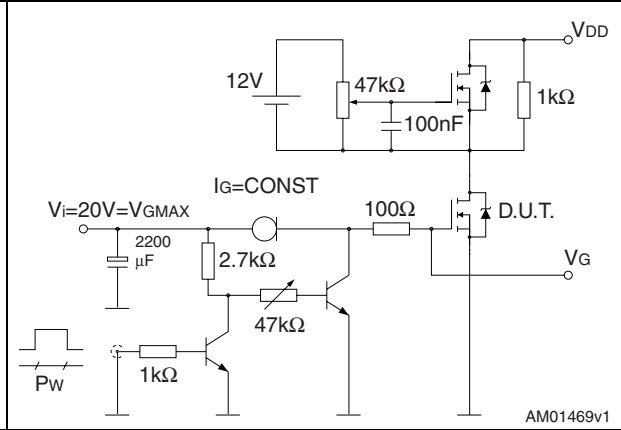
3 Test circuit

Figure 2. Switching times test circuit for resistive load



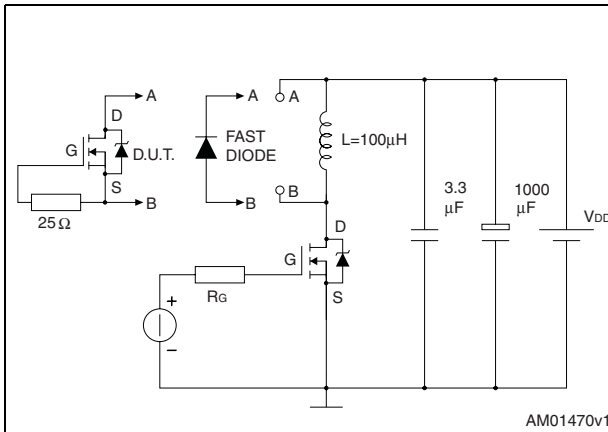
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Figure 3. Gate charge test circuit



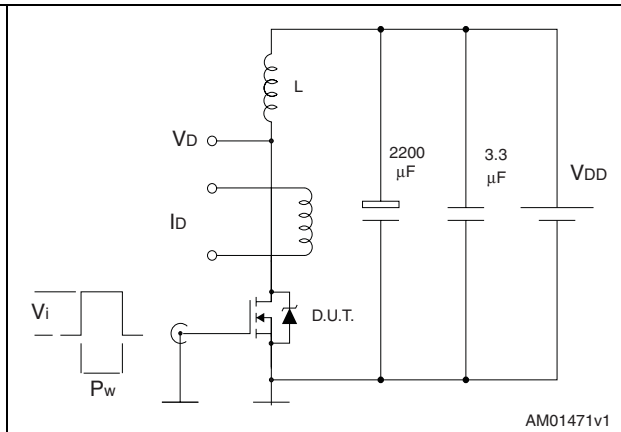
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Figure 4. Test circuit for inductive load switching and diode recovery times



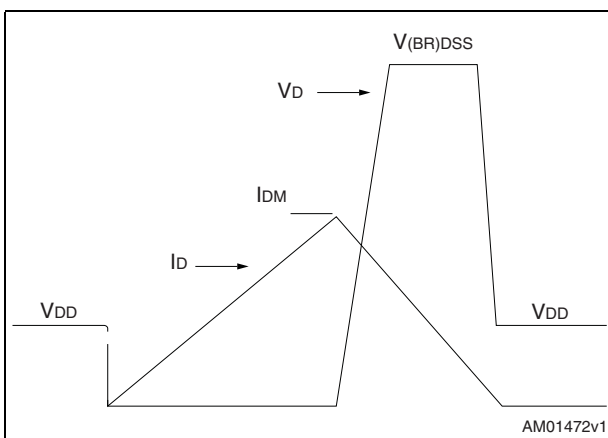
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Figure 5. Unclamped inductive load test circuit



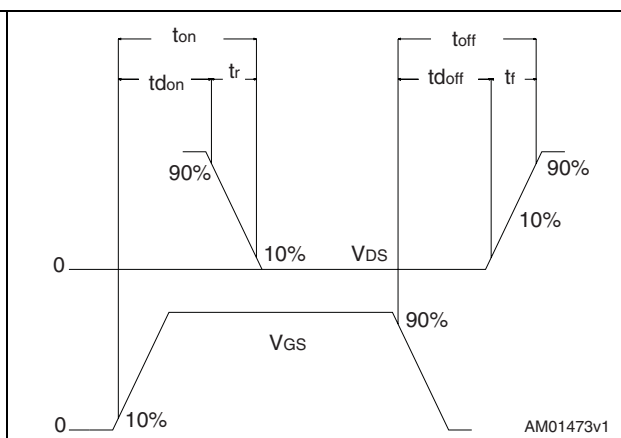
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Figure 6. Unclamped inductive waveform



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Figure 7. Switching time waveform



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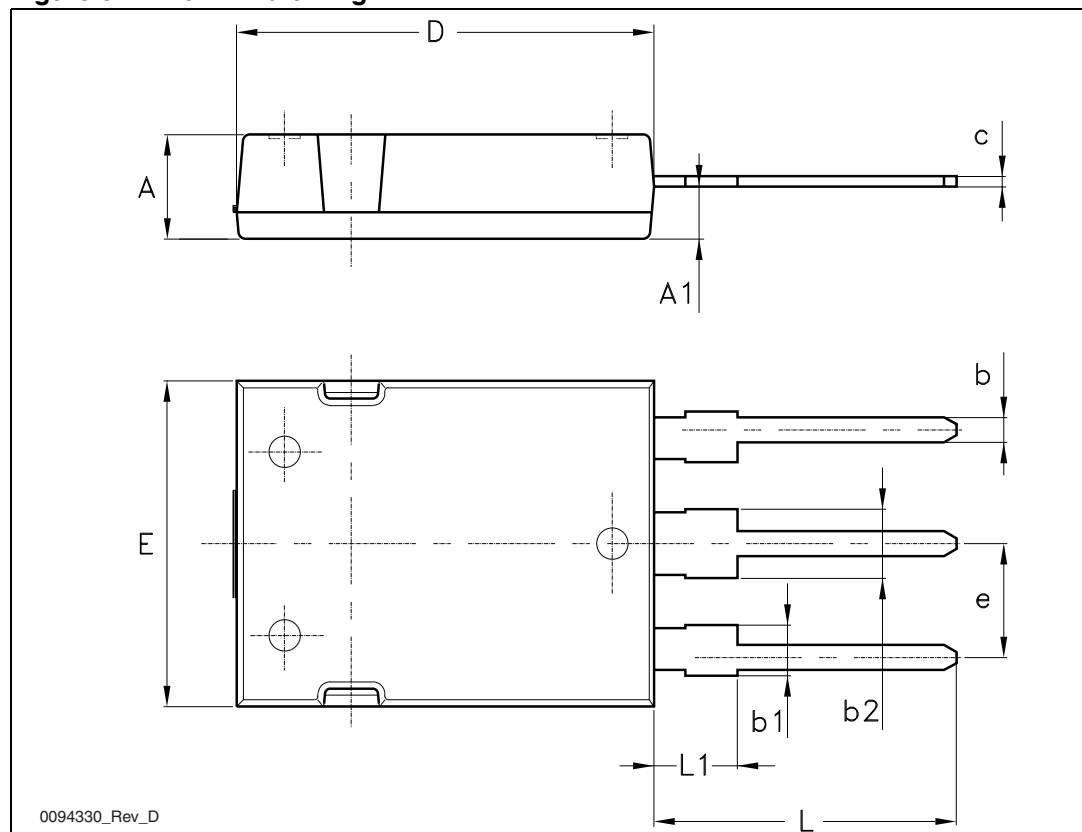
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Table 9. Max247 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.70		5.30
A1	2.20		2.60
b	1.00		1.40
b1	2.00		2.40
b2	3.00		3.40
c	0.40		0.80
D	19.70		20.30
e	5.35		5.55
E	15.30		15.90
L	14.20		15.20
L1	3.70		4.30

Figure 8. Max247 drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
27-Jan-2009	1	First release

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