TRANSYS ELECTRONICS LIMITED

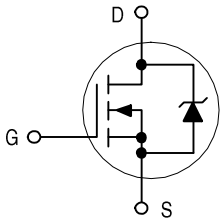
IRF530

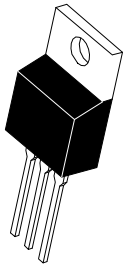
TMOS POWER FET
14 AMPERES
100 VOLTS
$R_{DS(on)}$ = 0.140 Ω

Power Field Effect Transistor

N–Channel Enhancement–Mode Silicon Gate

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- I_{DSS} and $V_{DS(on)}$ Specified at Elevated Temperature





TO-220AB

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	100	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	100	Vdc
Gate–to–Source Voltage — oltage — Single Pulse ($t_p \le 50$ μS)	V_{GS} V_{GSM}	±20 ±25	Vdc Vdc
Drain Current — Current — Continuous @ 100° Current — Single Pulse ($t_p \le 10$ μS)	I_D I_D I_{DM}	14 10 49	Adc Apk
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	78 0.63	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain–to–Source Avalanche Energy — STARTING T_J = 25°C (V_{DD} = 75 V, V_{GS} = 10 V, PEAK I_L = 14 A, L = 1.0 mH, R_G = 25 Ω)	E_{AS}	98	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction–to– Resistance — Junction–to–	$R_{\theta JC}$ $R_{\theta JA}$	1.60 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–to–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 0.25 mAdc)	$V_{(BR)DSS}$	100	—	—	Vdc
Temperature Coefficient (Positive)		—	112	—	V/°C
Zero Gate Voltage Drain Current (V_{DS} = 100 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
(V_{DS} = 100 Vdc, V_{GS} = 0 Vdc, T_J = 125°C)		—	—	100	
Gate–Body Leakage Current (V_{GS} = ±20 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS(1)					
Gate Threshold Voltage Cpk ≥ 2.0(3) (V_{DS} = V_{GS}, I_D = 0.25 mA)	$V_{GS(th)}$	2.0	2.9	4.0	Vdc
Threshold Temperature Coefficient (Negative)		—	6.2	—	mV/°C
Static Drain–to–Source On–Resistance Cpk ≥ 2.0(3) (V_{GS} = 10 Vdc, I_D = 8.0 Adc)	$R_{DS(on)}$	—	0.098	0.140	Ohms
Drain–to–Source On–Voltage (V_{GS} = 10 Vdc, I_D = 14 Adc)	$V_{DS(on)}$	—	—	—	Vdc
(V_{GS} = 10 Vdc, I_D = 8.0 Adc, T_J = 125°C)		—	—	—	
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 8.0 Adc)	g_{FS}	4.0	7.4	—	Mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance (V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	—	700	800	pF
Output Capacitance	C_{oss}	—	200	500	
Transfer Capacitance	C_{rss}	—	65	150	
SWITCHING CHARACTERISTICS(2)					
Turn–On Delay Time (V_{DS} = 36 Vdc, I_D = 8.0 Adc, V_{GS} = 10 Vdc, R_G = 15 Ω)	$t_{d(on)}$	—	9.0	30	ns
Rise Time	t_r	—	47	75	
Turn–Off Delay Time	$t_{d(off)}$	—	33	40	
Fall Time	t_f	—	34	45	
Gate Charge (V_{DS} = 80 Vdc, I_D = 14 Adc, V_{GS} = 10 Vdc)	Q_T	—	26	40	nC
	Q_1	—	5.0	—	
	Q_2	—	13	—	
	Q_3	—	11	—	
SOURCE–DRAIN DIODE CHARACTERISTICS					
Forward On–Voltage (I_S = 14 Adc, V_{GS} = 0 Vdc)	V_{SD}	—	0.92	1.5	Vdc
(I_S = 14 Adc, V_{GS} = 0 Vdc, T_J = 125°C)		—	0.80	—	
Reverse Recovery Time (I_S = 14 Adc, dI_S/dt = 100 A/μS)	t_{rr}	—	103	—	nS
	t_a	—	78	—	
	t_b	—	25	—	
Reverse Recovery Stored Charge	Q_{RR}	—	0.46	—	μC
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die)	L_d	—	3.5	—	nH
Internal Source Inductance (Measured from screw on tab to source bond pad)	L_s	—	7.5	—	

(1) Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

(2) Switching characteristics are independent of operating junction temperature.

(3) Reflects typical values. $Cpk = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{sigma}} \right|$

TYPICAL ELECTRICAL CHARACTERISTICS

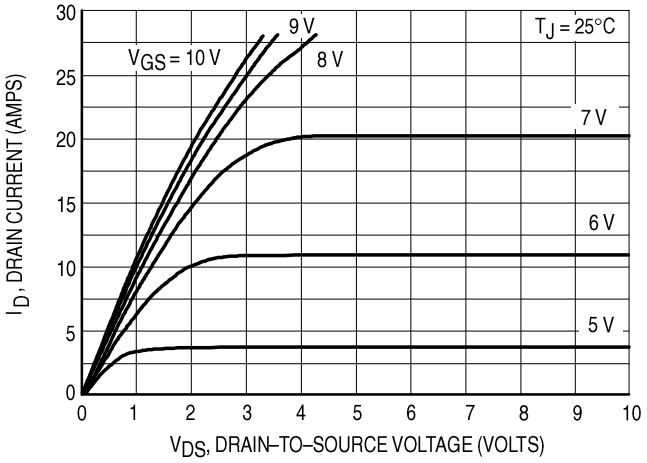


Figure 1. On–Region Characteristics

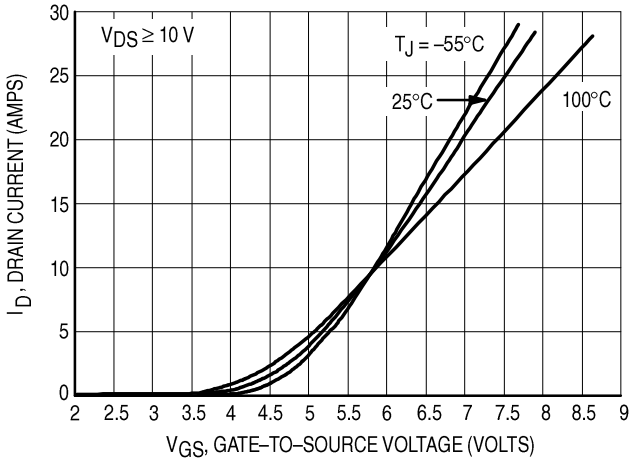


Figure 2. Transfer Characteristics

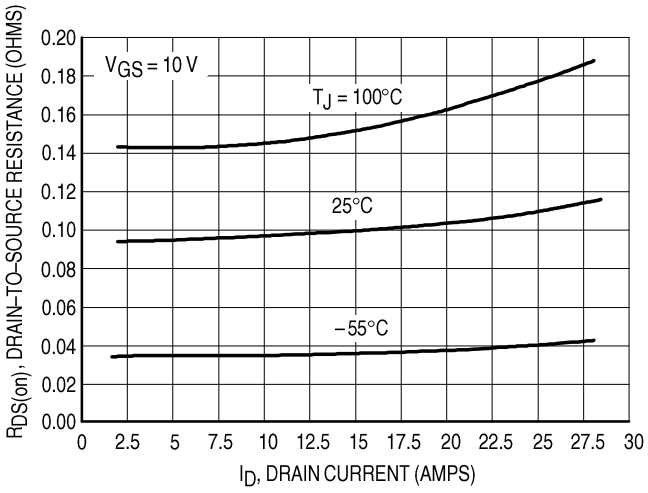


Figure 3. On–Resistance versus Drain Current and Temperature

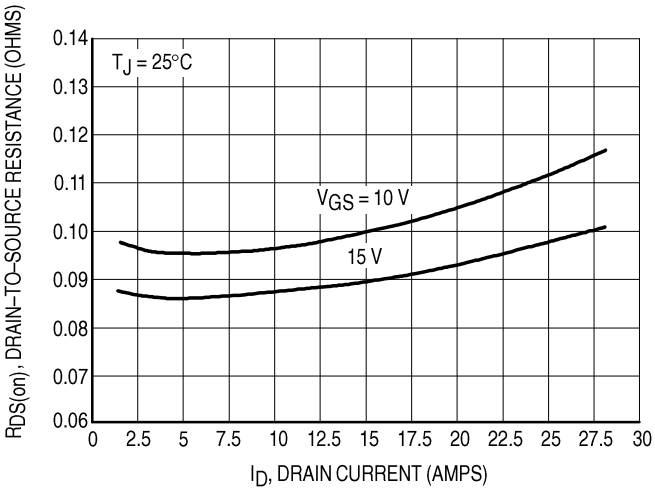


Figure 4. On–Resistance versus Drain Current and Gate Voltage

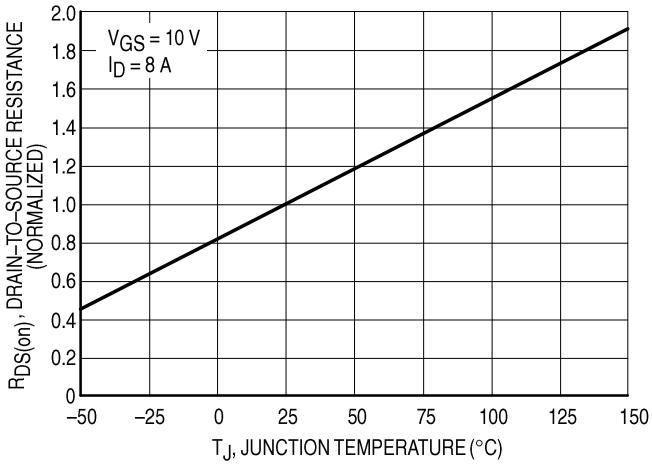


Figure 5. On–Resistance Variation with Temperature

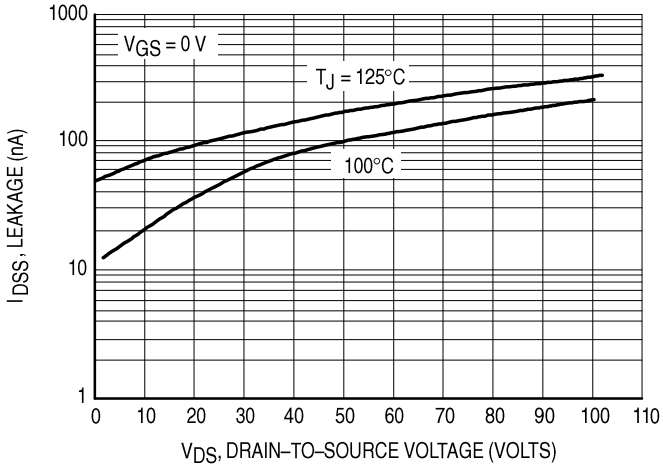


Figure 6. Drain–To–Source Leakage Current versus Voltage

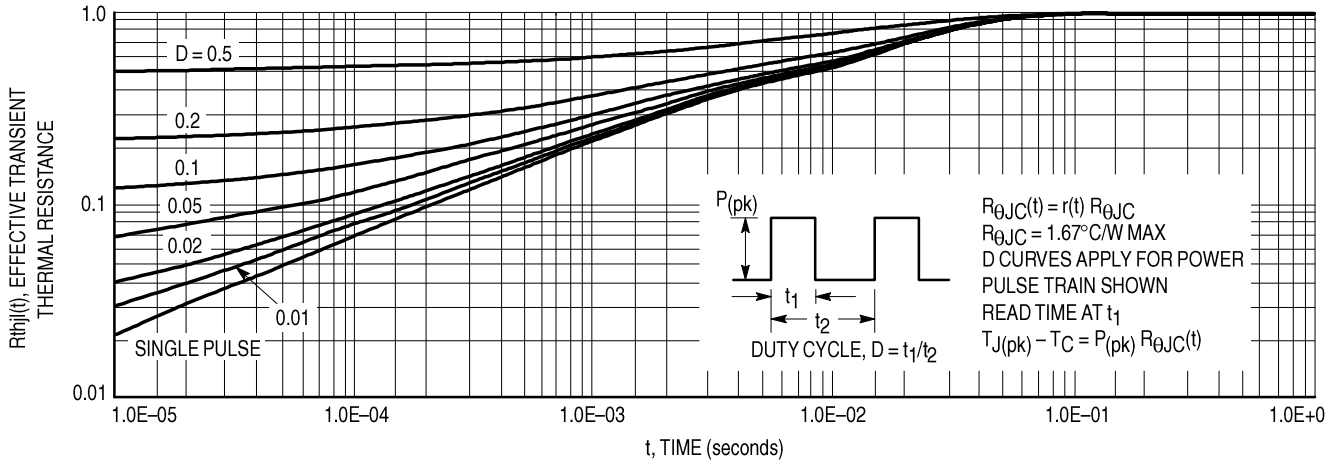
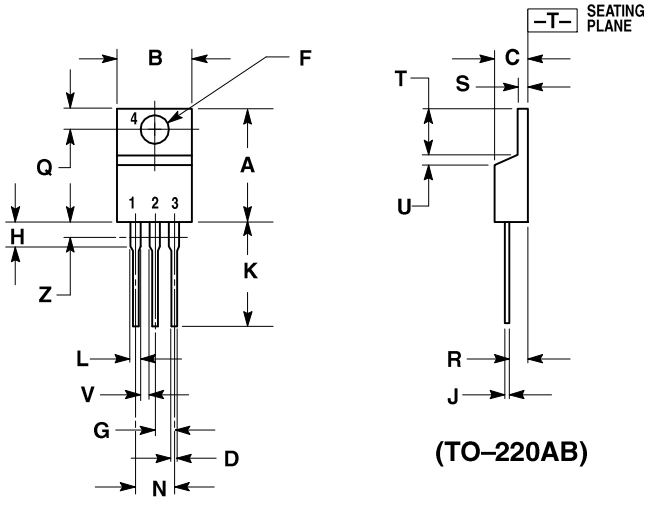


Figure 13. Thermal Response

PACKAGE DIMENSIONS



(TO–220AB)

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	—	1.15	—
Z	—	0.080	—	2.04