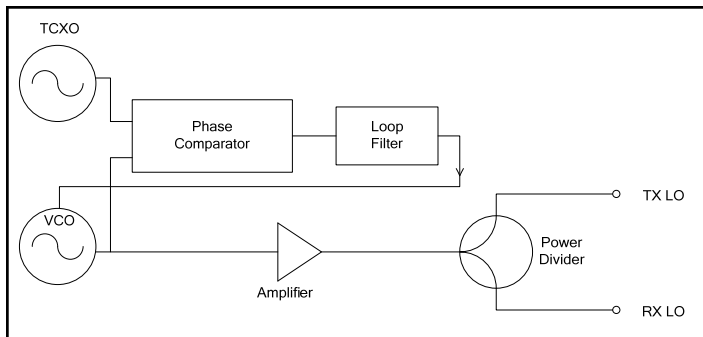


## Features

- Fully Integrated VCO, PLL, Loop Filter
- Includes TCXO with <10 PPM Stability
- Low Phase Noise
- High Performance, Low Cost
- Covers US, European and Japanese RFID Bands
- Lead-Free Land Grid Array Package
- Tape and Reel Packaging Available
- 260°C Reflow Compatible
- RoHS\* Compliant

## Functional Block Diagram



## Description

This synthesizer design integrates a high performance VCO, PLL IC, and discrete loop filter into a surface mount package. A high stability frequency reference is also included. This SMT package provides electrical shielding, easy PCB assembly, and repeatable performance.

## Applications

These synthesizers are well suited for applications where small size and high performance is required. This synthesizer is specifically targeted for the RFID market in the United States, European, and Japanese bands. This synthesizer can also be used for other applications in these frequency ranges.

## Ordering Information<sup>1, 4</sup>

Model No.	Band	Frequency	Package
MASY-007028-0001TR	US	902 - 928 MHz	Tape and Reel
MASY-007028-000100	US	902 - 928 MHz	Bulk
MASY-007028-0001TB	US	902 - 928 MHz	Sample Board <sup>2</sup>
MASY-007028-SW01TB	US	902 - 928 MHz	Sample Board <sup>3</sup>
MASY-007028-0001TR	European	865 - 868 MHz	Tape and Reel
MASY-007028-000100	European	865 - 868 MHz	Bulk
MASY-007028-0001TB	European	865 - 868 MHz	Sample Board <sup>2</sup>
MASY-007028-SW01TB	European	865 - 868 MHz	Sample Board <sup>3</sup>
MASY-007028-0002TR	Japanese	950 - 956 MHz	Tape and Reel
MASY-007028-000200	Japanese	950 - 956 MHz	Bulk
MASY-007028-0002TB	Japanese	950 - 956 MHz	Sample Board <sup>2</sup>
MASY-007028-SW02TB	Japanese	950 - 956 MHz	Sample Board <sup>3</sup>

1. The US and European bands share the same part. The listings are separated to illustrate the different frequencies.
2. This is the synthesizer installed on a sample board. This does not include the evaluation software or the test cable.
3. This is the synthesizer installed on a sample board. It also includes software (including a brief manual on how to use the software), and a cable to interface with a Windows™ based PC having a parallel port.
4. Reference Application Note M513 for reel size information.

\* Restrictions on Hazardous Substances, European Union Directive 2002/95/EC.

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## Electrical Specifications – US & European Bands<sup>5</sup>

$T_A = +25^\circ\text{C}$ ,  $Z_o = 50 \Omega$ ,  $V_{DD1} = 3.3\text{V}$ ,  $V_{DD2} = 3.3\text{V}$

Parameter	Test Conditions	Units	Min	Typ	Max
Frequency Range	US Band	MHz	902	-	928
	European Band	MHz	865	-	868
Frequency Stability	Over $T_{op}$ <sup>6</sup>	ppm	-	-	10
RF Output Power	At 25°C Over $T_{op}$ <sup>6</sup>	dBm	+4.0	-	+6.2
		dBm	+3.0	-	+7.5
Phase Noise	SSB at 100 Hz offset from carrier	dBc/Hz	-	-72	-
	SSB at 1 KHz offset from carrier	dBc/Hz	-	-75	-
	SSB at 10 KHz offset from carrier	dBc/Hz	-	-80	-
	SSB at 100 KHz offset from carrier	dBc/Hz	-	-112	-
	SSB at 200 KHz offset from carrier	dBc/Hz	-	-121	-
	SSB at 1 MHz offset from carrier	dBc/Hz	-	-135	-
	SSB at 2 MHz offset from carrier	dBc/Hz	-	-140	-
	SSB at 3 MHz offset from carrier	dBc/Hz	-	-142	-
Phase Jitter	From 10 kHz to 100 kHz using brick wall filter	deg rms	-	0.34	-
Harmonic Suppression	2nd	dBc	-	-35	-20
	3rd and higher	dBc	-	-35	-25
	1.25 * Fo	dBc	-	-80	-60
	1.5 * Fo	dBc	-	-85	-60
	Sub-harmonics	dBc	-	-80	-60
Spurious Suppression (Non-Harmonic)	Phase comparison frequency (± 50 KHz)	dBc	-	-65	-
Spurious Suppression (Non-Harmonic)	Reference breakthrough (± 16 MHz)	dBc	-	-80	-
Frequency Lock Time	Over Fout, PFD frequency = 50 KHz, Loop bandwidth = 5 KHz Measured to within ± 1 kHz Measured to within ± 10 Hz	us	-	700	-
		us	-	800	-
VDD1 <sup>7</sup>	Recommended Operating Condition	V	+3.00	+3.30	+3.45
IDD1 <sup>10</sup>	Recommended Operating Condition	mA	-	45	60
VDD2 <sup>8</sup>	Recommended Operating Condition	V	+3.00	+3.30	+3.45
IDD2	Recommended Operating Condition	mA	-	25	35
RF Impedance	At RX_LO and TX_LO <sup>9</sup>	Ω	-	50	-
Isolation	Between RX_LO and TX_LO	dB	-	20	-
Step Size	Over $T_{op}$ <sup>6</sup>	KHz	-	50	-
Output Frequencies	For US RFID readers, there are 50 equally spaced frequencies. The minimum and maximum frequencies are to the right. There are 49 steps with a step size of 500 KHz. For European RFID readers, there are 15 equally spaced frequencies. The minimum and maximum frequencies are to the right. There are 14 steps with a step size of 200 KHz	MHz	902.750	-	927.250
		MHz	865.100	-	867.900
PLL Programming	3-wire serial CMOS in accordance with Analog Devices ADF4360-7.				

## Electrical Specifications – Japanese Band<sup>5</sup>:

$T_A = +25^\circ\text{C}$ ,  $Z_o = 50 \Omega$ ,  $V_{DD1} = 3.3\text{V}$ ,  $V_{DD2} = 3.3\text{V}$

Parameter	Test Conditions	Units	Min	Typ	Max
Frequency Range	Japanese Band	MHz	952	-	954
Frequency Stability	Over $T_{op}$ <sup>6</sup>	ppm	-	-	10
RF Output Power	At $25^\circ\text{C}$ Over $T_{op}$ <sup>6</sup>	dBm dBm	+4.0 +3.0	-	+6.2 +7.5
Phase Noise	SSB at 100 Hz offset from carrier SSB at 1 KHz offset from carrier SSB at 10 KHz offset from carrier SSB at 100 KHz offset from carrier SSB at 200 KHz offset from carrier SSB at 1 MHz offset from carrier SSB at 2 MHz offset from carrier SSB at 3 MHz offset from carrier	dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz	- - - - - - - -	-74 -76 -81 -113 -120 -134 -136 -142	- - - - - - - -
Phase Jitter	From 10 kHz to 100 kHz using brick wall filter	deg rms	-	0.34	-
Harmonic Suppression	2nd 3rd and higher 1.25 * $F_o$ 1.5 * $F_o$ Sub-harmonics	dBc dBc dBc dBc dBc	- - - - -	-35 -35 -80 -85 -80	-20 -25 -60 -60 -60
Spurious Suppression (Non-Harmonic)	Phase comparison frequency ( $\pm 200$ KHz)	dBc	-	-75	-
Spurious Suppression (Non-Harmonic)	Reference breakthrough ( $\pm 16$ MHz)	dBc	-	-80	-
Frequency Lock Time	Over $F_{out}$ , PFD frequency = 200 KHz, Loop bandwidth = 5 KHz Measured to within $\pm 1$ kHz Measured to within $\pm 10$ Hz	us us	- -	700 800	- -
VDD1 <sup>7</sup>	Recommended Operating Condition	V	+3.00	+3.30	+3.45
IDD1 <sup>10</sup>	Recommended Operating Condition	mA	-	45	60
VDD2 <sup>8</sup>	Recommended Operating Condition	V	+3.00	+3.30	+3.45
IDD2	Recommended Operating Condition	mA	-	20	35
RF Impedance	At RX_LO and TX_LO <sup>9</sup>	$\Omega$	-	50	-
Isolation	Between RX_LO and TX_LO	dB	-	20	-
Step Size	Over $T_{op}$ <sup>6</sup>	KHz	-	200	-
Output Frequencies	For Japanese RFID readers, there are 9 equally spaced frequencies. The minimum and maximum frequencies are to the right. There are 8 steps with a step size of 200 KHz.	MHz	952.200	-	953.800
PLL Programming	3-wire serial CMOS in accordance with Analog Devices ADF4360-7.				

- All specification limits are indicated values @  $25^\circ\text{C}$  and apply over  $F_{out}$  unless otherwise indicated.
- $T_{op} = -30^\circ\text{C}$  to  $+70^\circ\text{C}$  operating temperature.
- VDD1 is the bias for the TCXO, VCO, and the synthesizer.
- VDD2 is the bias for the amplifier.
- Opposite port is terminated in 50 ohms.
- IDD1 includes approximately 10 mA which drives an optional external Lock Detector LED.

## Pin Configuration

Pin No.	Function	Pin No.	Function
1	GND	21	GND
2	GND	22	GND
3	GND	23	GND
4	GND	24	GND
5	RX_LO	25	CLK
6	GND	26	DATA
7	GND	27	LE
8	TX_LO	28	VDD1 <sup>11</sup>
9	GND	29	MUXOUT
10	GND	30	CE
11	VDD1 <sup>11</sup>	31	GND
12	GND	32	VDD1 <sup>11</sup>
13	GND	33	GND
14	GND	34	GND
15	GND	35	VDD2
16	GND	36	GND
17	GND	37	GND
18	GND	38	GND
19	GND	39	GND
20	GND	40	GND

11. Pins 11, 28, and 32 are not tied together on the synthesizer. They all must be tied together on the PC Board

## Absolute Maximum Ratings <sup>12,13</sup>

Parameter	Absolute Maximum
VDD1 to GND	-0.3V to +3.9V
VDD2 to GND	-0.3V to +6.0V
CLK, DATA, LE, MUXOUT	-0.3V to VDD1 + 0.3V
Operating Temperature	-30°C to +70°C
Storage Temperature	-40°C to +125°C

12. Exceeding any one or combination of these limits may cause permanent damage to this device.  
13. M/A-COM does not recommend sustained operation near these survivability limits.

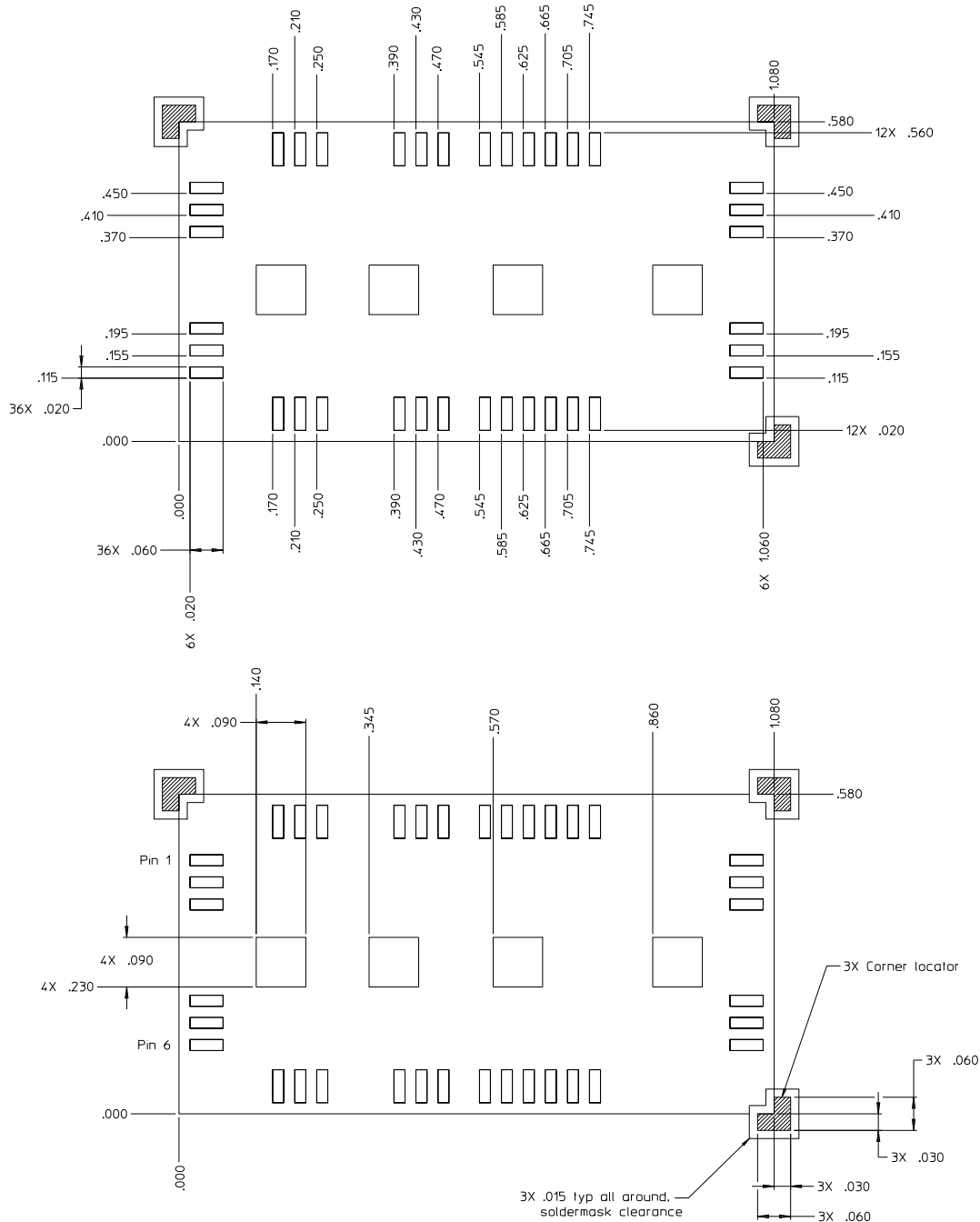
## Handling Procedures

Please observe the following precautions to avoid damage:

## Static Sensitivity

Silicon and Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

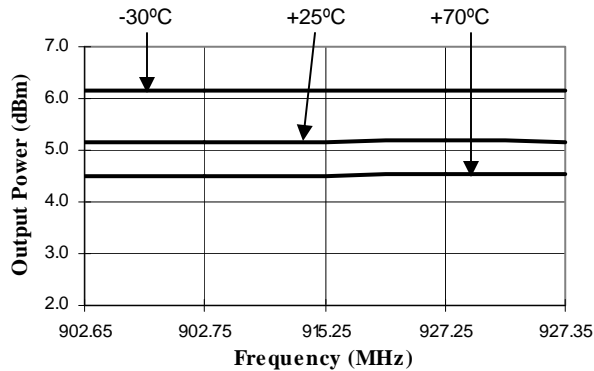
## Recommended PCB Configuration <sup>14,15,16</sup>



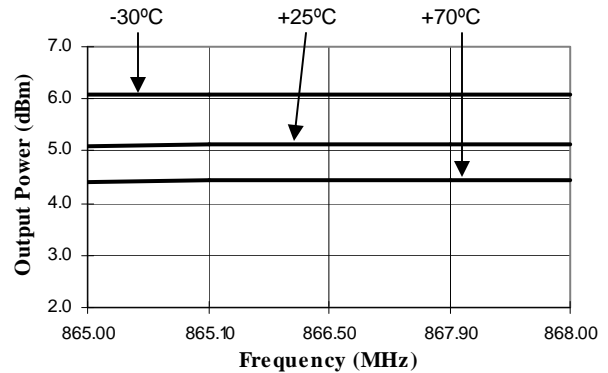
14. Corner locators are needed for manual placement and are strongly recommended.
15. Soldermask should be line to line with the pads on the bottom of the part.
16. Soldermask should be cleared 15 mils outside the corner locators. This ensures that they are easily visible.

## Typical Performance Curves

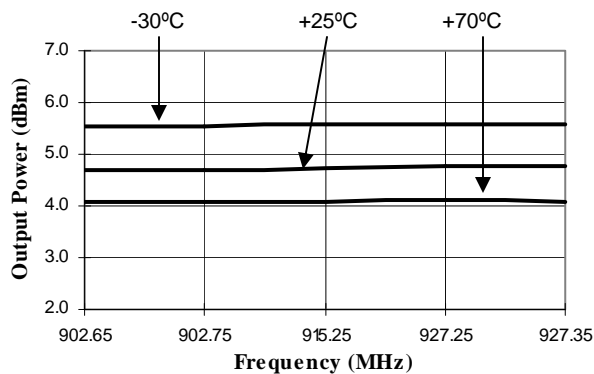
**Output Power vs. Temperature: VDD1 & VDD2 = 3.3V  
MASY-007028-000100, US Band**



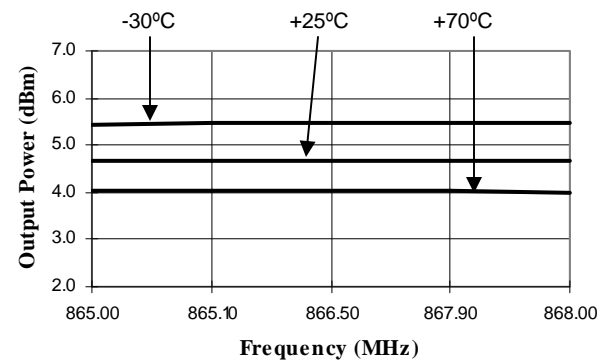
**Output Power vs. Temperature: VDD1 & VDD2 = 3.3V  
MASY-007028-000100, European Band**



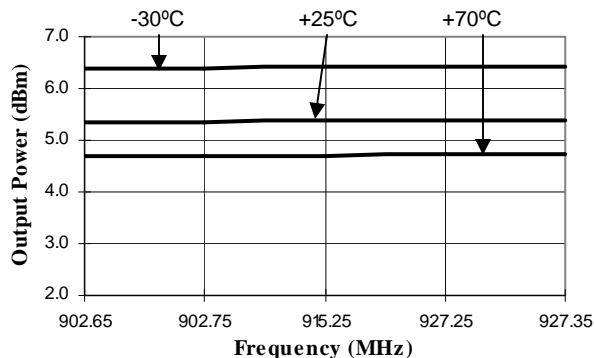
**Output Power vs. Temperature: VDD1 & VDD2 = 3.0V  
MASY-007028-000100, US Band**



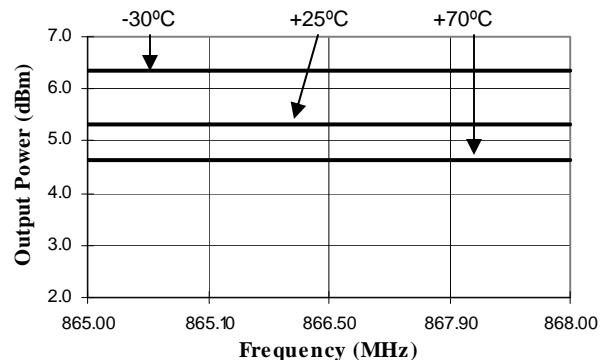
**Output Power vs. Temperature: VDD1 & VDD2 = 3.0V  
MASY-007028-000100, European Band**



**Output Power vs. Temperature: VDD1 & VDD2 = 3.45V  
MASY-007028-000100, US Band**

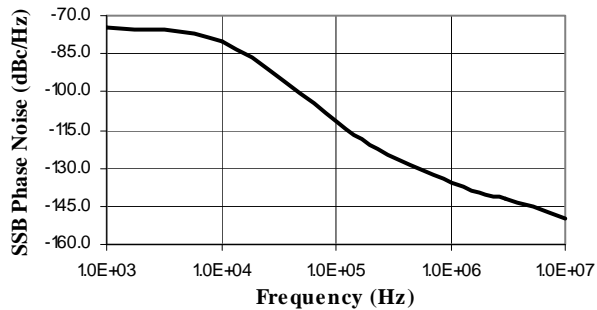


**Output Power vs. Temperature: VDD1 & VDD2 = 3.45V  
MASY-007028-000100, European Band**

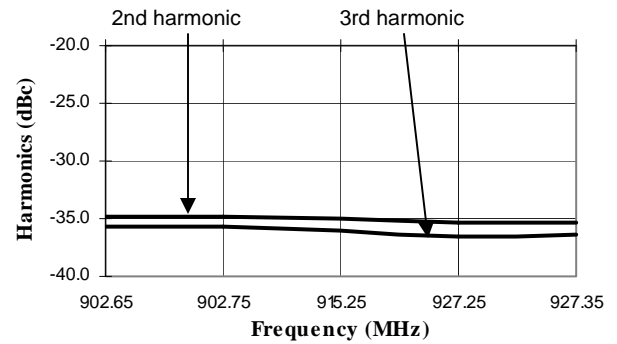


## Typical Performance Curves

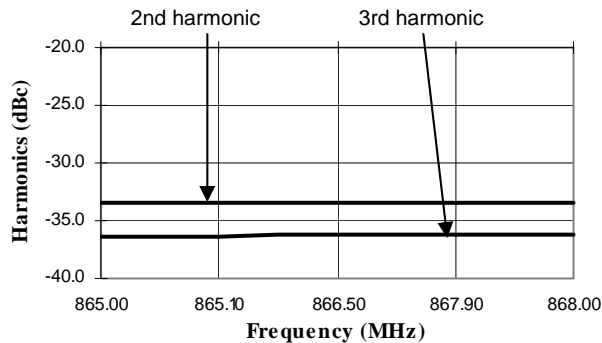
**SSB Phase Noise**  
MASY-007028-000100, US & European Band



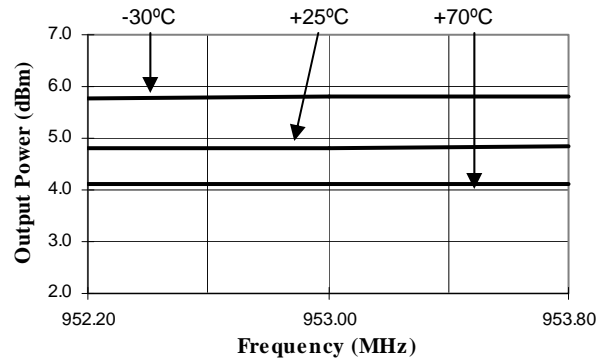
**Harmonics vs. Frequency: VDD1 & VDD2 = 3.3V, 25°C**  
MASY-007028-000100, US Band



**Harmonics vs. Frequency: VDD1 & VDD2 = 3.3V, 25°C**  
MASY-007028-000100, European Band

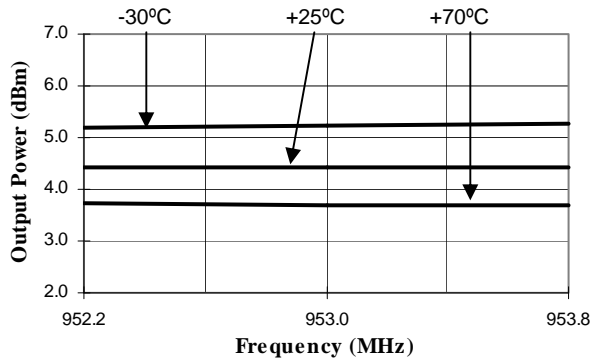


**Output Power vs. Temperature: VDD1 & VDD2 = 3.3V**  
MASY-007028-000200, Japanese Band

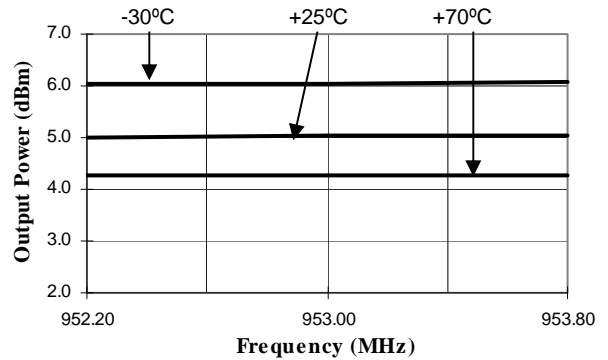


## Typical Performance Curves

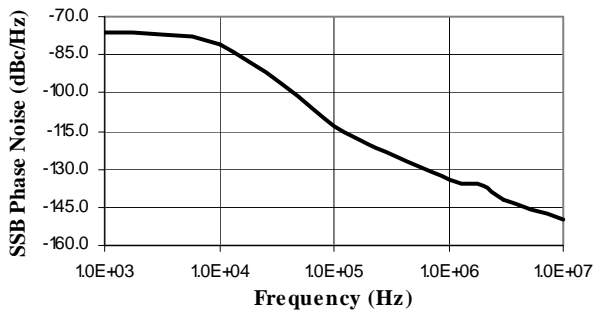
**Output Power vs. Temperature: VDD1 & VDD2 = 3.0V**  
MASY-007028-000200, Japanese Band



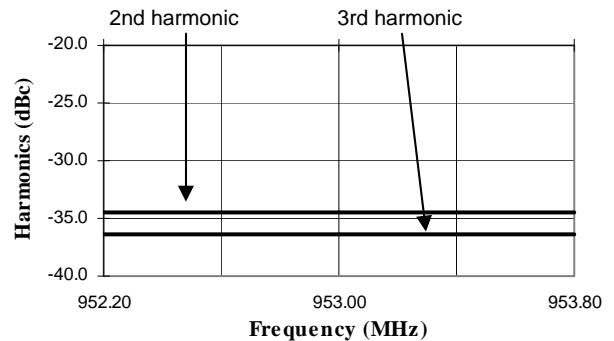
**Output Power vs. Temperature: VDD1 & VDD2 = 3.45V**  
MASY-007028-000200, Japanese Band



**SSB Phase Noise**  
MASY-007028-000200, Japanese Band



**Harmonics vs. Frequency: VDD1 & VDD2 = 3.3V, 25°C**  
MASY-007028-000200, Japanese Band





## Sample Board Pin Configuration

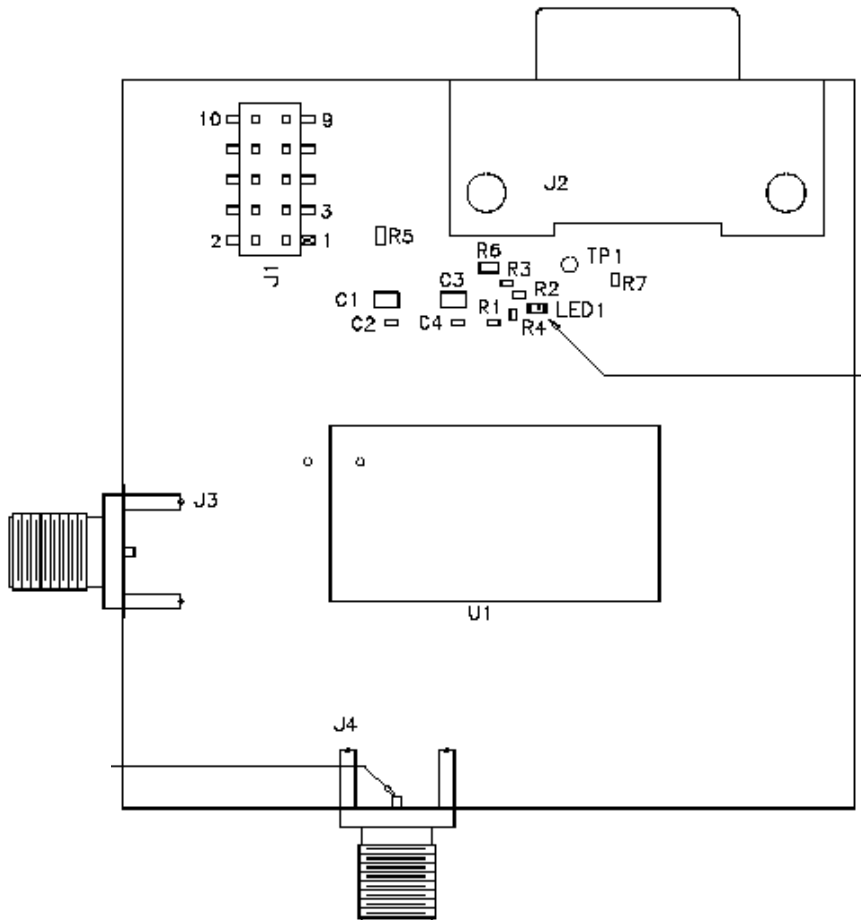
### Pin Configuration J1

Pin No.	Function	Pin No.	Function
1	GND	6	VDD1
2	GND	7	LE
3	CE	8	VDD2
4	MUXOUT	9	J2-6 (D4)
5	SCOPE-TRIGGER <sup>18</sup>	10	GND

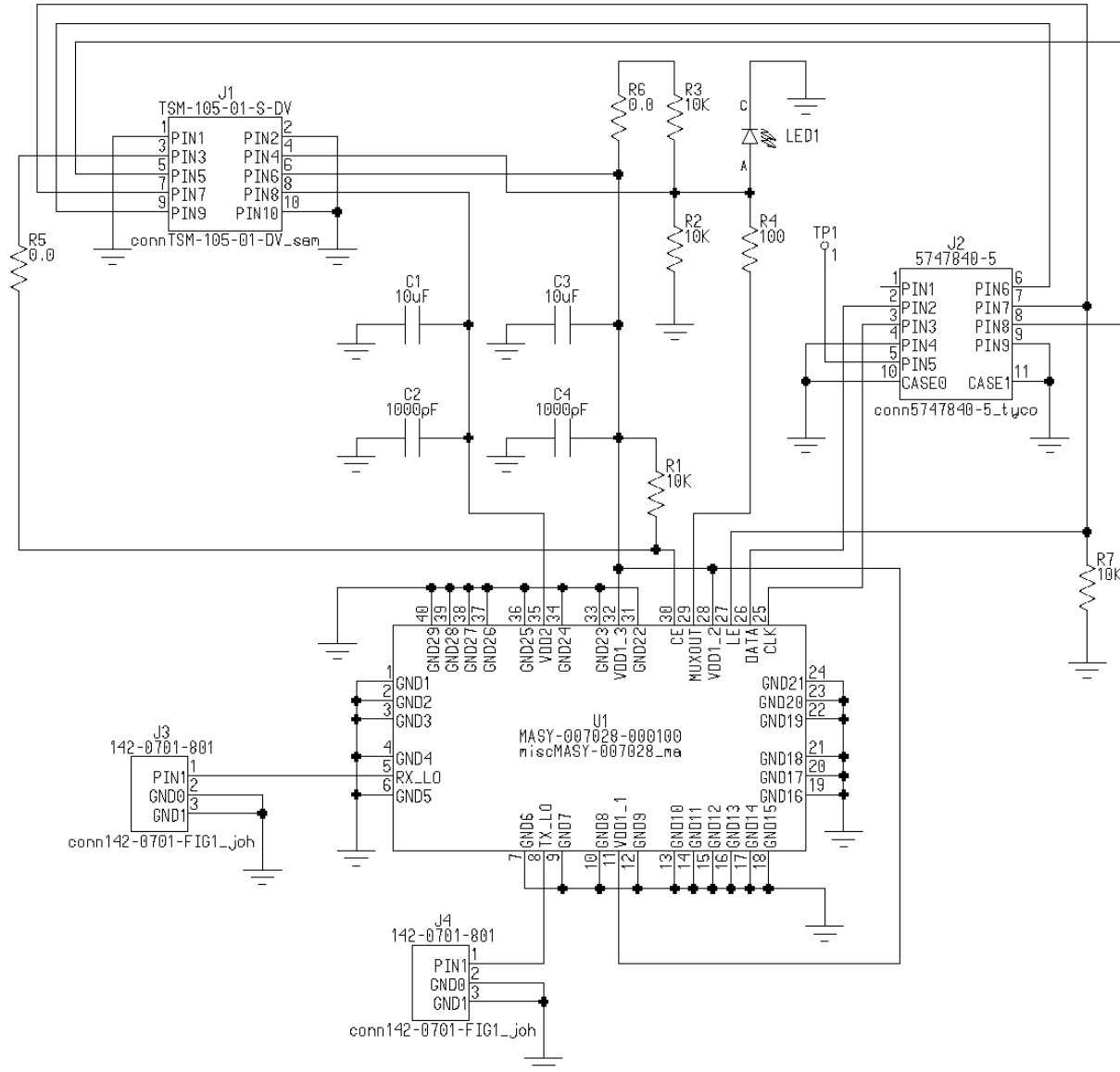
### Pin Configuration J2<sup>17</sup>

Pin No.	Function
1	NC
2	DATA
3	CLK
4	GND
5	TP1 (D5) <sup>19</sup>
6	D4 <sup>19</sup>
7	LE
8	SCOPE-TRIGGER
9	GND

17. J2 is Tyco Electronics P/N 5747840-5.  
 18. This signal is provided by the test software supplied with the sample boards. The signal comes in on the cable from the parallel port of the computer.  
 19. D4 and D5 are uncommitted PC Parallel Port data bits.



## Sample Board Schematic and Bill of Material



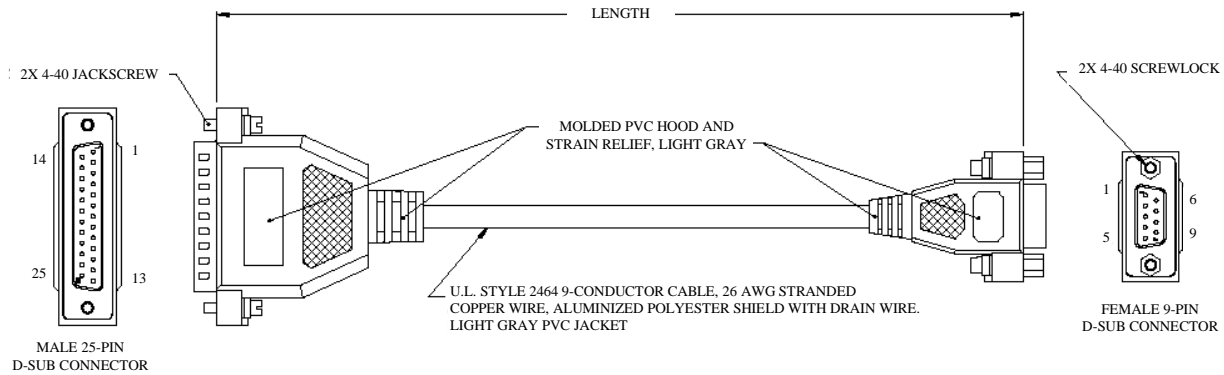
Qty	Part Number	Description	Reference Designator
1		Resistor, 100 ohm, 1%, 1/16W, 0402	R4
3		Resistor, 10K, 1%, 1/16W, 0402	R1, R2, R3, R7
2		Capacitor, 1000pF, 10%, 50V, 0402, COG	C2, C4
2		Capacitor, 10 uF, 10%, 6.3V, 0805, X5R	C1, C3
1	1000026283-0000001	LED, 0603, Green (Ledtronics)	LED1
2	142-0701-801	Connector, SMA, End Launch Jack	J3, J4
1	5747840-5	Connector, 9P, 90 Deg, Plug, Through (Tycoelectronics)	J2
1	MASY-007028-000100	RFID Synthesizer (M/A-COM)	U1
2	RK73Z-1JT	Resistor, 0 ohm, 1.0A MAX, 0603	R5, R6
1	TSM-105-01-S-DV	Connector, Termstrip, 10P_2R, .230 Post Height	J1

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## Test Cable that is provided with MASY-007028-SWxxTB<sup>20,21</sup>

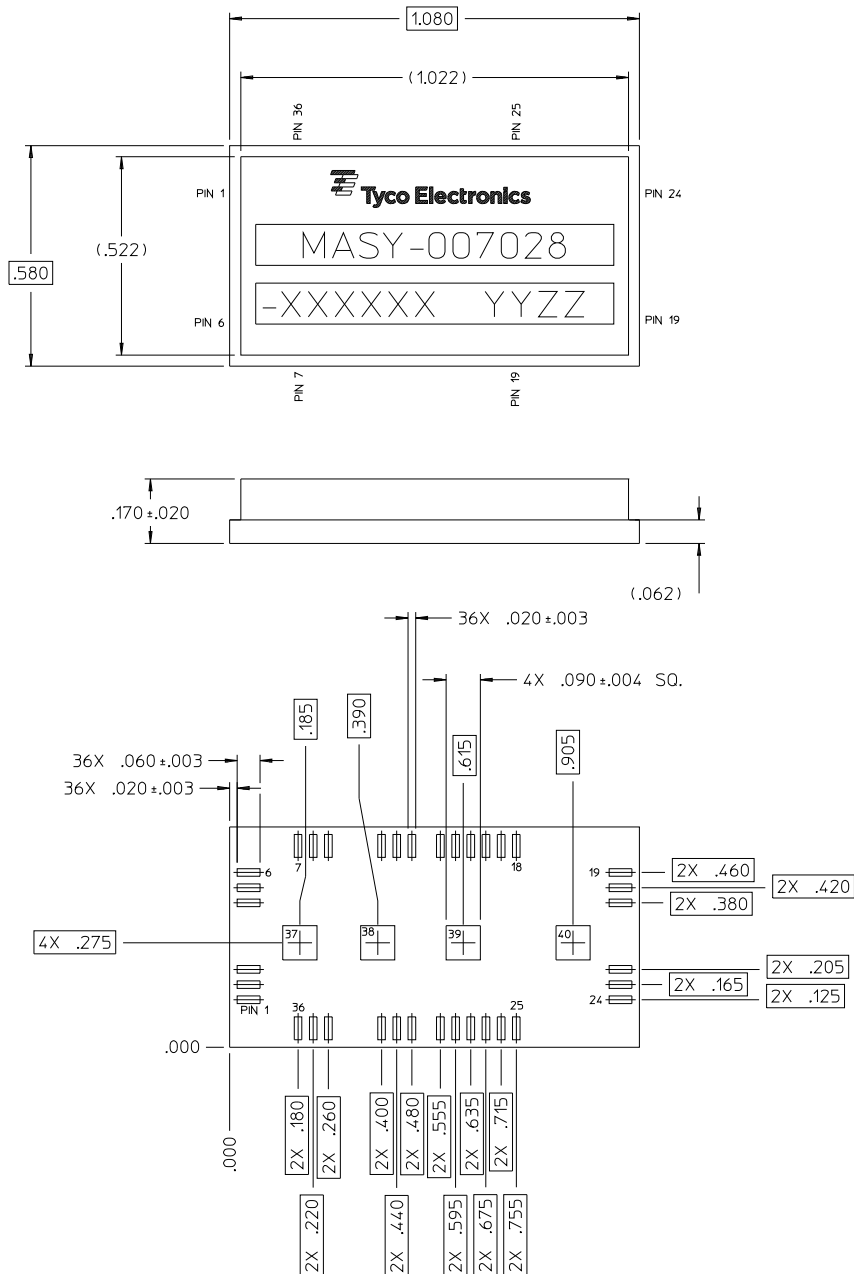


- 20. Length is 72 inches
- 21. Connector pins are gold.

### Wiring Chart

DB25M	DB9F
PIN 8	PIN 1
PIN 3	PIN 2
PIN 2	PIN 3
PIN 20	PIN 4
PIN 7	PIN 5
PIN 6	PIN 6
PIN 4	PIN 7
PIN 5	PIN 8
PIN 22	PIN 9
SHELL	SHELL

## Land Grid Array Outline Drawing†



The PC Board Configuration contains detailed pad sizes and locations.

† Reference Application Note M538 for lead-free solder reflow recommendations.