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SSI 73M450L/1450/2450
Universal Asynchronous Receiver/Transmitter

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DESCRIPTION

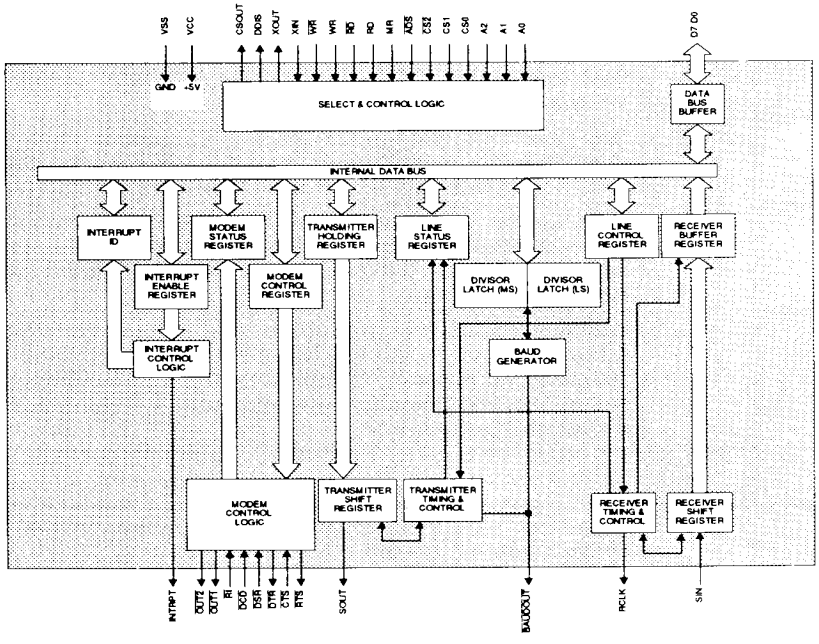
The SSI 73M450L is a Universal Asynchronous Receiver/Transmitter (UART) circuit which is pin- and function-compatible with industry-standard 16C450-type UARTs. It is primarily used in the interface between the serial data port and the parallel peripheral bus in 8-bit microprocessor systems. The SSI 73M450L is available in either a 40-pin DIP or 44-pin PLCC package.

The SSI 73M1450 and SSI 73M2450 are 28-pin versions of the SSI 73M450L. The difference between these versions is that the SSI 73M2450 adds a µPRST pin at the expense of the XOUT pin. See Figure 13 on page 31 for detail. All versions are designed in CMOS for low-power quiescent operation and require a single 5V supply.

FEATURES

- **Compatible with industry standard UARTs**
- **Static CMOS with oscillator shutdown for low-power operation**
- **High drive current allows direct connection to a PC bus**
- **Full double buffering**
- **Independent control of transmit, receive, line status and data set interrupts**
- **Contains modem control function including CTS, RTS, DSR, DTR, RI and DCD**
- **Programmable serial interface characteristics include:**
  - **5, 6, 7 or 8-bit characters**
  - **even, odd or no-parity bit generation and detection**
  - **1, 1 1/2 or 2 stop-bit generation**
  - **baud rate generation (dc to 56K baud)**
- **Full status reporting capabilities**
- **Available in 40-pin DIP, 44-and 28-pin PLCC packages**

BLOCK DIAGRAM



PIN DESCRIPTION

BUS INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{ADS}$	I	Address Strobe: The rising edge of this signal is used for latching the Register Address and Chip Select inputs, thus facilitating interface to a multiplexed Address/Data bus. If not required, $\overline{ADS}$ should be tied permanently low.
CS0, CS1, $\overline{CS2}$	I	Chip Select: The UART is selected when CS0 and CS1 are high and $\overline{CS2}$ is low. Chip selection is complete when the decoded chip select signal is latched with an active (low) $\overline{ADS}$ input. This enables communication between the UART and the CPU.
A0-2	I	Register Select Address: These pins determine which of the UART registers is being selected during a read or write on the UART Data Bus. The contents of the DLAB bit in the UART's Line Control Register (see Table 1) also controls which register is referenced.
RD, $\overline{RD}$	I	Read Strobe: A request to read status information or data from a selected register may be made by pulling RD high or $\overline{RD}$ low while the chip is selected. Since only one input is required for a read, tie either RD permanently low or $\overline{RD}$ permanently high if not used.
WR, $\overline{WR}$	I	Write Strobe: A request to write control words or data into a selected register may be made by pulling WR high or $\overline{WR}$ low while the chip is selected. Since only one input is required for a write, tie either WR permanently low or $\overline{WR}$ permanently high if not used.
D0-7	I/O	UART Data Bus (three-state): This bus provides bi-directional communications between the UART and the CPU; data, control words and status information are transferred via this bus.
CSOUT	O	Chip Select Out: When high, indicates that the chip has been selected by active CS0, CS1 and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic "1." CSOUT goes low when the chip is deselected.
DDIS	O	Driver Disable: Goes low when the CPU is reading data from the UART. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and UART on the D0-D7 Data Bus) at all times, except when the CPU is reading data.
INTRPT	O	Interrupt: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag, Received Data Available, Transmitter Holding Register Empty and Modem Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

DATA I/O

SIN	I	Serial Input: Input for serial data from the communications link (peripheral device, modem or data set).
SOUT	O	Serial Output: Output for serial data to the communications link (peripheral device,modem or data set). This signal is set high upon a Master Reset.

MODEM CONTROL

NAME	TYPE	DESCRIPTION
$\overline{RTS}$	O	Request To Send: This output is programmed by bit 1 of the Modem Control Register and is used in modem handshaking to signify that the UART has data to transmit. This signal is set high upon Master Reset or during loop mode operation.
$\overline{CTS}$	I	Clear To Send: A modem status input whose condition corresponds to the complement of the CTS bit (bit 4) of the Modem Status Register. When $\overline{CTS}$ is low, it indicates that communications have been established and that data may be transmitted.
$\overline{DTR}$	O	Data Terminal Ready: This output is programmed by bit 0 of the Modem Control Register, and is used in modem handshaking to signify that the UART is available to communicate. This signal is set high upon Master Reset or during loop mode operation.
$\overline{DSR}$	I	Data Set Ready: A modem status input whose condition corresponds to the complement of the DSR bit (bit 5) of the Modem Status Register. When $\overline{DSR}$ is low, it indicates that the modem is ready to establish communications.
$\overline{DCD}$	I	Data Carrier Detect: A modem status input whose condition corresponds to the complement of the DCD bit (bit 7) of the Modem Status Register. When DCD is low, it indicates that the modem is receiving a carrier.
$\overline{RI}$	I	Ring Indicator: A modem status input whose condition corresponds to the complement of the RI bit (bit 6) of the Modem Status Register. When $\overline{RI}$ is low, it indicates that a telephone ringing signal is being received.
$\overline{OUT1}$ $\overline{OUT2}$	O O	Output 1, 2: User designated outputs that can be set to an active low by setting bit 2 ($\overline{OUT1}$) or bit 3 ($\overline{OUT2}$) of the Modem Control Register high. These output signals are set high upon Master Reset or during loop mode operation.

PIN DESCRIPTION (Continued)

GENERAL & CLOCKS

NAME	TYPE	DESCRIPTION
VCC	I	+5V Supply, ±10%: Bypass with 0.1 µF capacitor to VSS.
VSS	I	System Ground.
MR	I	Master Reset: When high, this input clears all UART control logic and registers, except for the Receiver Buffer, Transmitter Holding and Divisor Latches; also, the state of output signals SOUT, INTRPT, $\overline{OUT1}$, $\overline{OUT2}$, $\overline{RTS}$ and $\overline{DTR}$ are affected by an active MR input. This input is buffered with a TTL-compatible Schmitt Trigger.
XIN, XOUT	I/O	External System Clock I/O: These two pins connect the main timing reference (crystal or signal clock) to the UART. Additionally, XIN may be driven by an external clock source.
RCLK	I	Receiver Clock: This input is the 16X baud rate clock for the receiver section of the chip.
$\overline{BAUDOUT}$	O	Baud Generator Output: 16X clock signal for the transmitter section of the UART, equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. May also be used for the receiver section by tying this output to the RCLK input of the chip.
NC	-	No Connection: These pins have no internal connection and may be left floating.
INTRPT	O	Interrupt: In the 28-pin versions of this chip, the INTRPT pin can be forced into a high impedance state by resetting to 0 the OUT2 bit (D3) of the Modem Control Register. INTRPT pin operation is enabled by setting the the OUT2 bit to 1.
XIN, XOUT	I/O	External System Clock: The XOUT pin is not available on the SSI 73M2450 and therefore must be driven by an external clock connected to the XIN pin.
µPRST	O	Microprocessor Reset: This output signal is used to provide a hardware reset to a local controller. This pin becomes active high when the MR pin is pulled high or the OUT1 bit (D2) of the Modem Control Register is set to 1. The µPRST function is available only on the SSI 73M2450.

TABLE 1: Control Register Address Table

DLAB	A2	A1	A0	REGISTER
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	Modem Control
X	1	0	1	Line Status
X	1	1	0	Modem Status
X	1	1	1	Scratch
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

TABLE 2: UART Reset Functions

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	Master Reset	All bits low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is high; bits 1 & 2 are low; bits 3-7 are permanently low
Line Control Register	Master Reset	All bits low
Modem Control Register	Master Reset	All bits low
Line Status Register	Master Reset	All bits low, except bits 5 & 6 are high
Modem Status Register	Master Reset	Bits 0-3 are low; bits 4-7 = input signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{OUT2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT1}$	Master Reset	High
µPRST	Master Reset/set OUT1 bit	High during active Master Reset/OUT1 bit; low afterwards

CONTROL REGISTER OVERVIEW

REGISTER		REGISTER ADDRESS (A2-A0) & DLAB	DATA BIT NUMBER							
			D7	D6	D5	D4	D3	D2	D1	D0
RECEIVER BUFFER REGISTER (READ ONLY)	RBR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
TRANSMIT HOLDING REGISTER (WRITE ONLY)	THR	000 DLAB = 0	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
INTERRUPT ENABLE REGISTER	IER	001 DLAB = 0	0	0	ENABLE SSI MODE	0	ENABLE MODEM STATUS INTERRUPT	ENABLE REC. LINE STATUS INTERRUPT	ENABLE THR EMPTY INTERRUPT	ENABLE REC. DATA AVAILABLE INTERRUPT
INTERRUPT ID REGISTER (READ ONLY)	IIR	010 DLAB = X	0	0	0	0	0	INTERRUPT ID BIT 1	INTERRUPT ID BIT 0	"0" IF INTERRUPT PENDING
LINE CONTROL REGISTER	LCR	011 DLAB = X	DIVISOR LATCH ACCESS (DLAB)	SET BREAK	STICK PARITY	EVEN PARITY SELECT (EPS)	PARITY ENABLE (PEN)	NUMBER OF STOP BITS (STB)	WORD LENGTH SELECT 1 (WLS1)	WORD LENGTH SELECT 0 (WLS0)
MODEM CONTROL REGISTER	MCR	100 DLAB = X	SSI MODE OSC OFF	0	0	LOOP	OUT2	OUT1	REQUEST TO SEND (RTS)	DATA TERMINAL READY (DTR)
LINE STATUS REGISTER	LSR	101 DLAB = X	0	TRANSMIT-TER EMPTY (TEMT)	TRANSMIT HOLDING REGISTER EMPTY(THRE)	BREAK INTERRUPT (BI)	FRAMING ERROR (FE)	PARITY ERROR (PE)	OVERRUN ERROR (OE)	DATA READY (DR)
MODEM STATUS REGISTER (READ ONLY)	MSR	110 DLAB = X	DATA CARRIER DETECT (DCD)	RING INDICATOR (RI)	DATA SET READY (DSR)	CLEAR TO SEND (CTS)	DELTA DATA CARR. DETECT (DDCD)	TRAILING EDGE RING INDICATOR (TERI)	DELTA DATA SET READY (DDSR)	DELTA CLEAR TO SEND (DCTS)
SCRATCH REGISTER	SCR	111 DLAB = X	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (LS)	DLL	000 DLAB = 1	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIVISOR LATCH (MS)	DLM	001 DLAB = 1	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8

REGISTER BIT DESCRIPTIONS

RECEIVER BUFFER REGISTER (RBR) (READ ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This read only register contains the parallel received data with start, stop, and parity bits (if any) removed. The high order bits for less than 8 data bits/character will be set to 0.

TRANSMIT HOLDING REGISTER (THR) (WRITE ONLY)
UART ADDRESS: A2 - A0 = 000, DLAB = 0

This write only register contains the parallel data to be transmitted. The data is sent LSB first with start, stop, and parity bits (if any) added to the serial bit stream as the data is transferred.

INTERRUPT ENABLE REGISTER (IER)
UART ADDRESS: A2 - A0 = 001, DLAB = 0

This 8-bit register enables the four types of interrupts of the UART to separately activate the chip Interrupt (INTRPT) output signal. This register also allows access to the chip's special SSI mode which contains the oscillator disable function. It is possible to totally disable the interrupt system by resetting bits D0 through D3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and Modem Status Registers.

The chip's SSI mode can be activated by setting bit D5. Once in the SSI mode, the chip can be placed in a power shut-down state by setting bit D7 in the Modem Control Register.

BIT	NAME	COND.	DESCRIPTION
D0	Received Data	1	This bit enables the Received Data Available Interrupt when set to logic 1.
D1	Transmitter Holding	1	This bit enables the Transmitter Holding Register
	Register Empty		Empty Interrupt when set to logic 1.
D2	Receiver Line Status Interrupt	1	This bit enables the Receiver Line Status Interrupt when set to logic 1.
D3	Modem Status	1	This bit enables the Modem Status Interrupt when set to logic 1.
D4	Not used	0	Always logic 0.
D5	SSI Mode	0	Disables chip's SSI Mode; normal operation.
		1	Enables chip's SSI mode. In this mode, chip can be placed into power shut-down by setting bit D7 in modem control register.
D6-D7	Not used	0	Always logic 0.

INTERRUPT ID REGISTER (IIR) (READ ONLY)
UART ADDRESS: A2 - A0 = 010

The IIR register gives prioritized information as to the status of interrupt conditions. When accessed, the IIR freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The order of interrupt priorities is shown in the table below.

BIT	NAME	COND.	DESCRIPTION
D0	Interrupt Pending	0	This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine.
		1	When bit 0 is a logic 1, no interrupt is pending.
D1, D2	Interrupt ID bits 0, 1	Table below	These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in the following table.
D3 - D7	Not Used	0	These five bits of the IIR are always logic 0.

INTERRUPT PRIORITY TABLE

D2	D1	D0	PRIORITY	TYPE	SOURCE	RESET
0	0	1	-	None	None	N/A
1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receive Data Available	Receive Data Available	Reading the Rcvr. Buffer Register
0	1	0	Third	Transmit Holding Register Empty	Transmit Holding Register Empty	Reading IIR Register (if source of interrupt) or Writing to Transmit Holding Register
0	0	0	Fourth	Modem Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Det.	Reading the Modem Status Register

LINE CONTROL REGISTER (LCR)
UART ADDRESS: A2 - A0 = 011

The user specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the user may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics.

BIT	NAME	COND.		DESCRIPTION
D0	Word Length Select 0 (WLS0)			Bits D0 and D1 select the number of data bits per character as shown:
D1	Word Length Select 1 (WLS1)	D1	D0	Word Length
		0	0	5 bits
		0	1	6 bits
		1	0	7 bits
		1	1	8 bits
D2	Number of Stop Bits (STB)	0 or 1		This bit specifies the number of stop bits in each transmitted character. If bit 2 is a logic 0, one stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one-and-a-half stop bits are generated. If bit 2 is a logic 1 when either a 6, 7, or 8-bit word length is selected, two stop bits are generated. The receiver checks the first stop bit only, regardless of the number of stop bits selected.
D3	Parity Enable (PEN)	1		This is the Parity Enable (PEN) bit. When set to a logic 1, a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and stop bit of the serial data. (The parity bit is used to produce an even or odd number of 1's when the data word bits and the parity bit are summed).
D4	Even Parity Select (EPS)	1 or 0		This is the Even Parity Select (EPS) bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1's is transmitted or checked in the data word bits and parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1's is transmitted or checked.

LINE CONTROL REGISTER (LCR) (Continued)

BIT	NAME	COND.		DESCRIPTION
D5	Stick Parity	1 or 0		This is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the parity bit is transmitted and checked by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.
		D5	D4	Parity
		0	0	ODD Parity
		0	1	EVEN Parity
		1	0	MARK Parity
		1	1	SPACE Parity
D6	Set Break	1		This is the Break Control bit. When set to a logic 1, the serial out (SOUT) is forced to a logic 0 state. The break is disabled by setting bit 6 to a logic 0. This bit acts only on SOUT and has no effect on the transmitter logic. See note below.
D7	Divisor Latch Access Bit (DLAB)	1		The Divisor Latch Access Bit (DLAB) must be set high (logic 1) to access the Divisor Latches of the baud generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

NOTE: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0's pad character in response to THRE.
2. Set break in response to the next THRE.
3. Wait for the Transmitter to be idle. (TEMT = 1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

MODEM CONTROL REGISTER (MCR)
UART ADDRESS: A2 - UA0 = 100

The Modem Control Register controls the interface with the modem, data set or peripheral device. Bits D1 and D0 are also available as read only bits in the UART Control Register in the Modem Registers.

BIT	NAME	COND.	DESCRIPTION
D0	DTR	1	This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.
D1	RTS	1	This bit controls the Request to Send ($\overline{RTS}$) output. When bit 1 is set to a logic 1, the $\overline{RTS}$ output is forced to a logic 0. When bit 1 is reset to a logic 0, the $\overline{RTS}$ output is forced to a logic 1.
D2	OUT1	1	This bit controls the Output 1 ($\overline{OUT1}$) signal, which is an auxiliary user-designated output. When bit 2 is set to a logic 1, the $\overline{OUT1}$ output is forced to a logic 0. When bit 2 is reset to a logic 0, the $\overline{OUT1}$ output is forced to a logic 1. On the SSI 73M2450 only, this bit controls the µPRST output. When bit D2 is set to a logic 1, the µPRST output is forced to a logic 1. When bit D2 is reset to logic 0, µPRST is forced to logic 0.
D3	OUT2	0	This bit controls the Output 2 ($\overline{OUT2}$) signal, which is an auxiliary user-designated output. When bit 3 is set to a logic 1, the $\overline{OUT2}$ output is forced to a logic 0. When bit 3 is reset to a logic 0, $\overline{OUT2}$ output is forced to a logic 1. On the 28-pin versions, this bit controls the INTRPT pin. When bit D3 is set to a logic 1, the INTRPT output is enabled. When bit D3 is reset to logic 0, the INTRPT pin is forced into a high impedance state.
D4	LOOP	1	This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occurs: the transmitter Serial Output (SOUT) is set to the logic 1 state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four Modem Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$ and $\overline{RI}$) are disconnected; the four Modem Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT1}$ and $\overline{OUT2}$) are internally connected to the four Modem Control inputs, and the Modem Control output pins are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART. In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the Modem Control Register instead of the four Modem Control inputs. The interrupts are still controlled by the Interrupt Enable Register.
D5-D6		0	These bits are permanently set to logic 0.
D7	SSi Mode Osc. off	1	This bit is active in the SSi Mode only. When D7 is set the UART oscillator is turned off placing the UART in a power shutdown state. All UART memory is retained during power shutdown.
		0	Resetting this bit enable the oscillator and powers up the UART.

LINE STATUS REGISTER (LSR)
UART ADDRESS: A2 - A0 = 101

This register provides status information to the CPU concerning the data transfer. Bits 1-4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected. The Line Status Register is intended for read operation only. Writing to this register is not recommended as this operation is used for factory testing.

BIT	NAME	COND.	DESCRIPTION
D0	DR	1	The Data Ready (DR) bit is set to a 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. DR is reset to 0 by reading the data in the Receiver Buffer Register.
D1	OE	1	The Overrun Error (OE) bit indicates that the data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. OE is reset to 0 whenever the CPU reads the contents of the Line Status Register.
D2	PE	1	The Parity Error (PE) bit indicates that the received character did not have the correct parity. PE is reset to 0 whenever the CPU reads the Line Status Register.
D3	FE	1	The Framing Error (FE) bit indicates that the received character did not have a valid stop bit. FE is reset to 0 whenever the CPU reads the contents of the Line Status Register.
D4	BI	1	The Break Interrupt (BI) bit indicates that a break has been received. A break occurs whenever the received data is held to 0 for a full data word (start + data + stop). BI is reset to 0 whenever the CPU reads the Line Status Register.
D5	THRE	1	The Transmit Holding Register Empty (THRE) is set to a logic 1 when a character is transferred from the Transmit Holding Regsiter into the Transmit Shift Register, indicating that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the THRE Interrupt enable is set high. THRE is reset to 0 when the CPU loads a character into the Transmit Holding Register.
D6	TEMT	1	The Transmit Empty (TEMT) indicates that both the Transmit Holding Register and the Transmit Shift Registers are empty. TEMT is reset to 0 whenever the TSR or THR contains a data character.
D7	-	0	Always zero.

MODEM STATUS REGISTER (MSR) (READ ONLY)
UART ADDRESS: A2 - A0 = 110

This register provides the current state of the control signals from the modem or peripheral device. In addition, four bits provide change information. Whenever bit 0, 1, 2 or 3 is set to logic 1, a Modem Status Interrupt is generated; reset to logic 0 occurs whenever they are read. In Loop Mode CTS, DSR, RI and DCD are taken from RTS, DTR, OUT1, and OUT2 in the Modem Control Register respectively.

BIT	NAME	COND.	DESCRIPTION
D0	DCTS	1	The Delta Clear to Send (DCTS) bit indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.
D1	DDSR	1	The Delta Data Set Ready (DDSR) bit indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.
D2	TERI	1	The Trailing Edge of the Ring Indicator (TERI) detect bit indicates that the $\overline{RI}$ input to the chip has changed from an Off (logic 0) to an On (logic 1) condition.
D3	DDCD	1	The Delta Data Carrier Detect (DDCD) bit indicates that the $\overline{DCD}$ input to the chip has changed state.
D4	CTS	1	This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.
D5	DSR	1	This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is the equivalent of DTR in the MCR.
D6	RI	1	This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT1 in the MCR.
D7	DCD	1	This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT2 in the MCR.

SCRATCH REGISTER (SCR)
ADDRESS: A2 - A0 = 111

This 8-bit Read/Write Register does not control the UART in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

DIVISOR LATCH (LS) (DLL)
ADDRESS: A2 - A0 = 000, DLAB = 1

This register contains the least significant byte of the divisor which is used to control the rate of the programmable baud generator.

DIVISOR LATCH (MS) (DLM)
ADDRESS: A2 - A0 = 001, DLAB = 1

This register contains the most significant byte of the divisor which is used to control the rate of the programmable baud generator.

PROGRAMMABLE BAUD GENERATOR

The UART contains a programmable Baud Generator that is capable of taking any clock input (DC to 4 MHz) and dividing it by any divisor from 1 to 2^{16}-1. The output frequency of the Baud Generator is 16 x the Baud [divisor # = (frequency input)/(baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

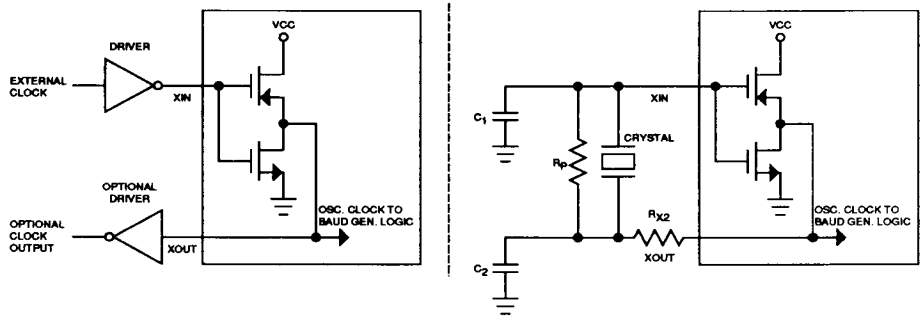
Tables 3 and 4 illustrate the use of the Baud Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below, the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

TABLE 3: Baud Rates Using 1.8432 MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	2304	-
75	1536	-
110	1047	0.026
134.5	857	0.058
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.69
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	-
56000	2	2.86

TABLE 4: Baud Rates Using 3.072 MHz Crystal

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16 X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL
50	3840	-
75	2560	-
110	1745	0.026
134.5	1428	0.034
150	1280	-
300	640	-
600	320	-
1200	160	-
1800	107	0.312
2000	96	-
2400	80	-
3600	53	0.628
4800	40	-
7200	27	1.23
9600	20	-
19200	10	-
38400	5	-



NOTE: R_p function is to bias the crystal; RX_2 function is to lower power and reduce crystal overdrive.

FIGURE 1: Typical Clock Circuits

TYPICAL CRYSTAL OSCILLATOR NETWORK

CRYSTAL	RP	RX2	C1	C2
1.8 MHz	1 MΩ	1.5K	10-30 pF	40-60 pF
4 MHz	1 MΩ	0	10-30 pF	40-60 pF

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS
(TA = -40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted. Operation above absolute maximum ratings may permanently damage the device.)

PARAMETER	CONDITIONS	RATING
VCC Supply Voltage		+7V
Storage Temperature		–65°C to 150°C
Lead Temperature	Soldering, 10 sec.	260°C
Applied Voltage		–0.3 to Vcc + 0.3

DC CHARACTERISTICS
(TA = –40°C to +85°C, VCC = 5V ± 10%, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VILX	Clock input Low voltage		–0.5		0.8	V
VIHX	Clock input High Voltage		2.0		Vcc	V
VIL	Input Low Voltage		–0.5		0.8	V
VIH	Input High Voltage		2.0		Vcc	V
VOL	Output Low Voltage	IOL = 4.0 mA (except XOUT)			0.4	V
VOH	Output High Voltage	IOH = 5.0 mA on all outputs except XOUT	2.4			V
ICC	Average Power Supply	See Note 1		5	10	mA
	Current	See Note 2			50	µA
IIL	Input Leakage	VCC=5.25V, VSS=0V. All other pins floating.			±10	µA
ICL	Clock Leakage	VIN=0V, 5.25V			±10	µA
IOZ	3-State Leakage	VCC=5.25V, VSS=0V, VOUT=0V, 5.25V 1) Chip deselected 2) Chip & write mode selected			±20	µA
VILMR	MR Schmitt VIL				0.8	V
VIHMR	MR Schmitt VIH		2.0			V

Note 1: VCC = 5.25V, TA = 25°C; No loads on outputs. SIN, $\overline{DSR}$, $\overline{DCD}$, $\overline{CTS}$, $\overline{RI}$ = 2.4V. All other inputs = 0.4V. Baud Rate Gen. = 4 MHz; Baud Rate = 50 KHz.
Note 2: VCC = 5.5V, TA = –40°C; No output load; CMOS-level inputs, XIN = Vcc

CAPACITANCE
(TA = 25°C, VCC = VSS = 0V, fc = 1 MHz, unmeasured pins returned to VSS)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
CXTAL2	Clock Input Capacitance			15	20	pF
CXTAL1	Clock Output Capacitance			20	30	pF
CI	Input Capacitance			6	10	pF
CO	Output Capacitance			10	20	pF

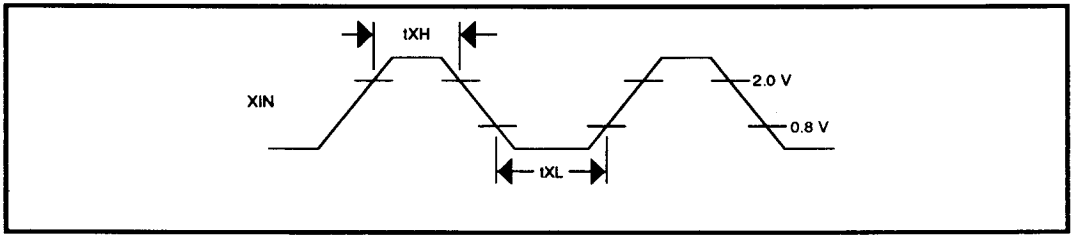


FIGURE 2: External Clock Input* (4 MHz Maximum)

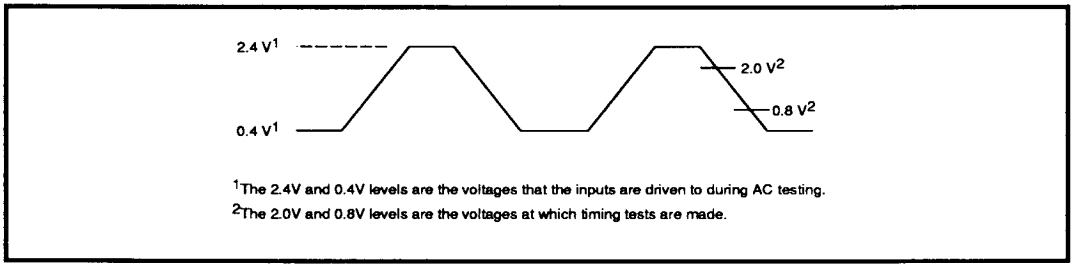


FIGURE 3: AC Test Points*

*All timings are referenced to valid 0 and valid 1.

AC CHARACTERISTICS (TA = -40°C to +85°C, VCC = 5V ±10%, unless otherwise noted.)

READ & WRITE CYCLE (Refer to Figures 4 & 5)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tADS	Address Strobe Width		60		ns
tAS	Address Setup Time		60		ns
tAH	Address Hold Time		0		ns
tCS	Chip Select Setup Time		60		ns
tCH	Chip Select Hold Time		0		ns
tCSC	Chip Select Output Delay from Select	100 pF load See Note 3		100	ns
tAR	READ Delay from Address		60		ns

READ & WRITE CYCLE (Continued)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tRD	READ Strobe Width		125		ns
tRC	Read Cycle Delay		175		ns
RC	Read Cycle	See Note 1	360		ns
tRDD	READ to Driver Disable Delay	100 pF load See Note 2		60	ns
tRVD	Delay from READ to Data	100 pF load		125	ns
tHZ	READ to Floating Data Delay	100 pF load See Note 2	0	100	ns
tRA	Address Hold Time from READ	See Note 3	20		ns
tAW	WRITE Delay from Address	See Note 3	60		ns
tWR	WRITE Strobe Width		100		ns
tWC	Write Cycle Delay		200		ns
WC	Write Cycle=tAW+tWR+tWC		360		ns
tDS	Data Setup Time		40		ns
tDH	Data Hold Time		40		ns
tWA	Address Hold Time from WRITE	See Note 3	20		ns
tMRW	Master Reset Pulse Width		5		µs
tXH	Duration of Clock High Pulse	External Clock (4 MHz max.)	100		ns
tXL	Duration of Clock Low Pulse	External Clock (4 MHz max.)	100		ns

Note 1: RC = tAR + tRD + tRC

Note 2: Charge and discharge time is determined by VOL, VOH and the external loading.

Note 3: Applicable only when $\overline{ADS}$ is tied low.

READ occurs when both read (RD, $\overline{RD}$) and chip select (CS0, CS1, $\overline{CS2}$, latched by $\overline{ADS}$) are asserted.

WRITE occurs when both write (WR, $\overline{WR}$) and chip select (CS0, CS1, $\overline{CS2}$, latched by $\overline{ADS}$) are asserted.

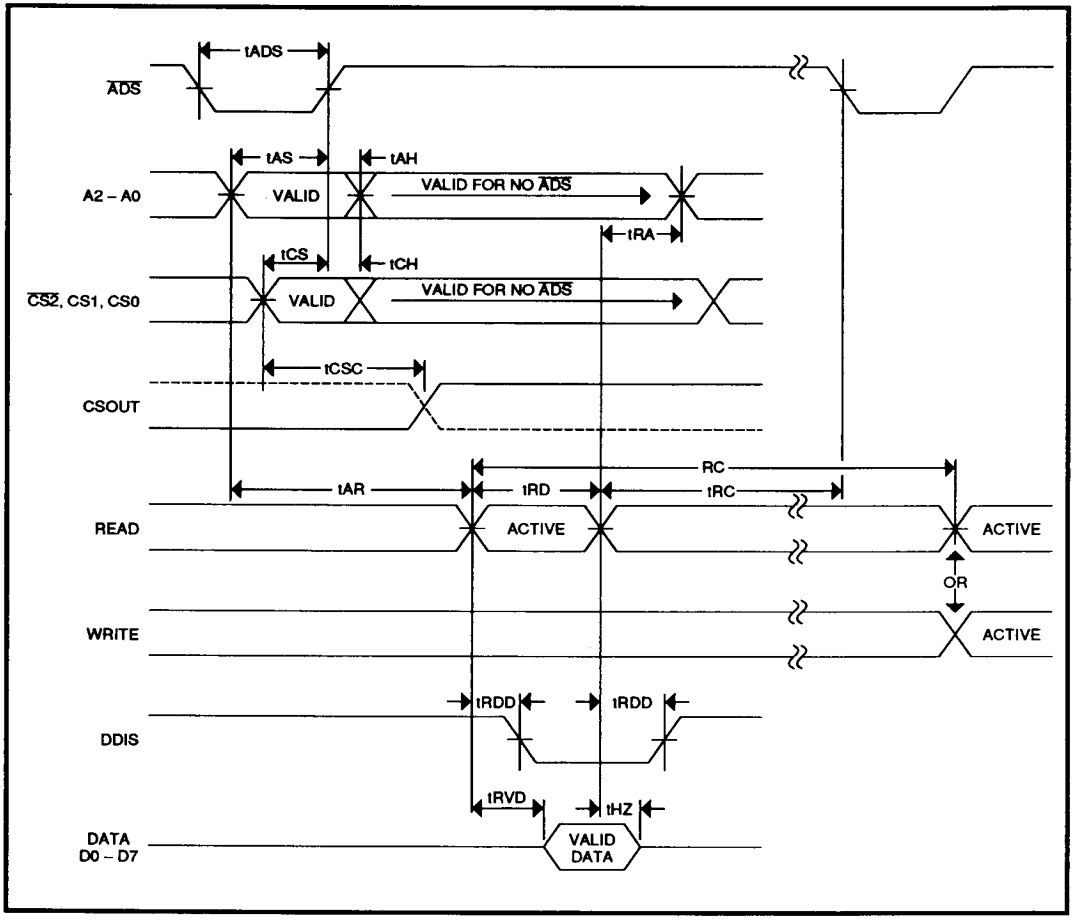


FIGURE 4: Read Cycle Timing

NOTE: READ occurs when both read (RD, $\overline{RD}$) and chip select (CS0, CS1, $\overline{CS2}$, latched by $\overline{ADS}$) are asserted.

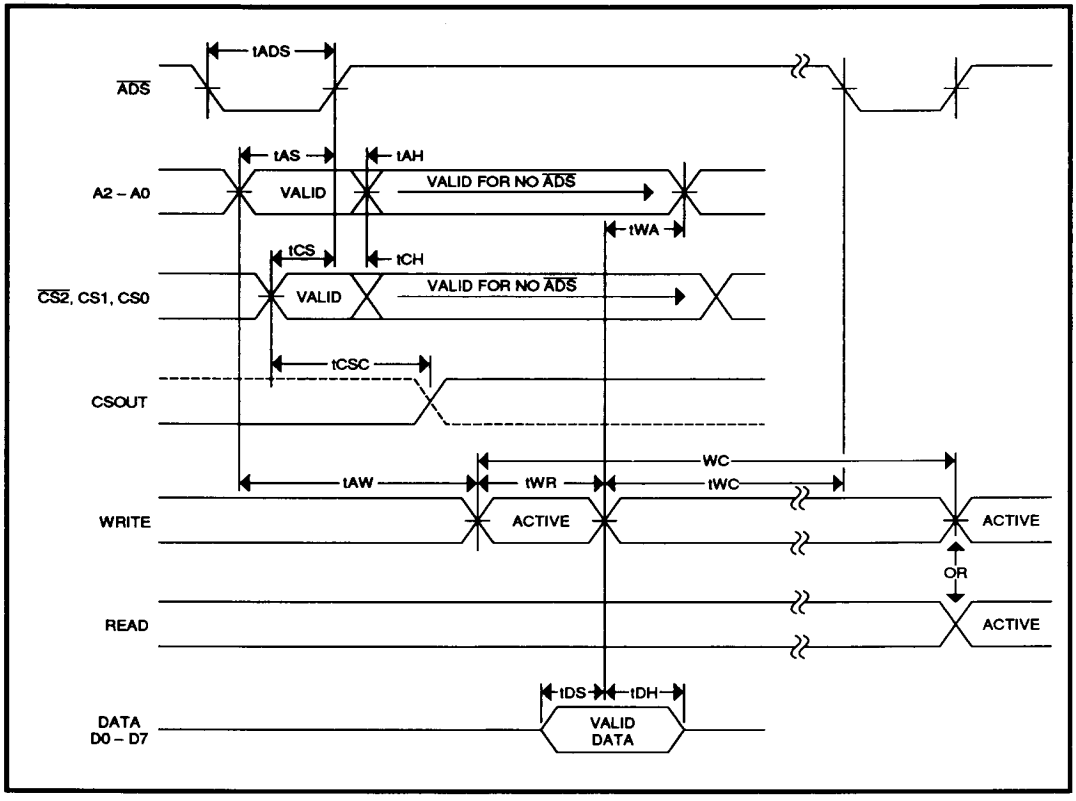


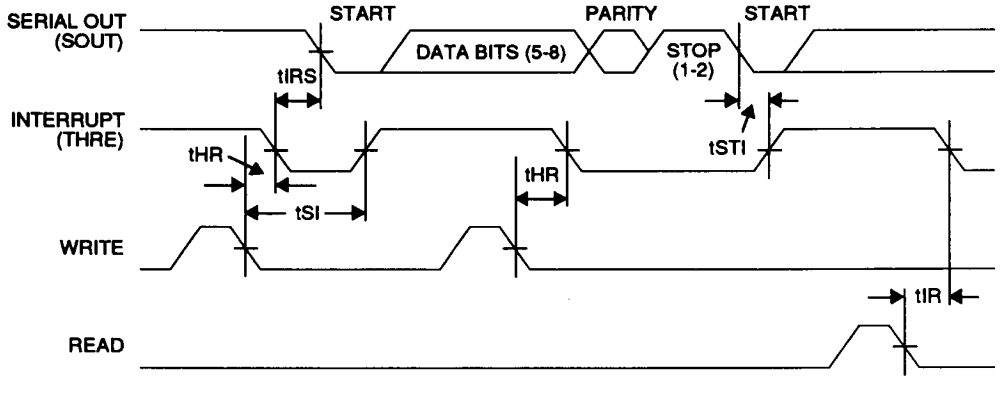
FIGURE 5: Write Cycle Timing

NOTE: WRITE occurs when both write (WR, $\overline{WR}$) and chip select (CS0, CS1, $\overline{CS2}$, latched by $\overline{ADS}$) are asserted.

AC CHARACTERISTICS (Continued)

TRANSMITTER (Refer to Figure 6.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tHR	Delay from the end of WRITE to the negation of Interrupt	100 pF load		175	ns
tIRS	Delay form Initial INTR Reset to Transmit Start		24	40	BAUDOUT cycles
tSI	Delay from Initial Write to Interrupt		16	32	BAUDOUT cycles
tSTI	Delay from Stop to Interrupt (THRE)		8	8	BAUDOUT cycles
tIR	Delay from the end of READ to the negation of Interrupt	100 pF load		250	ns



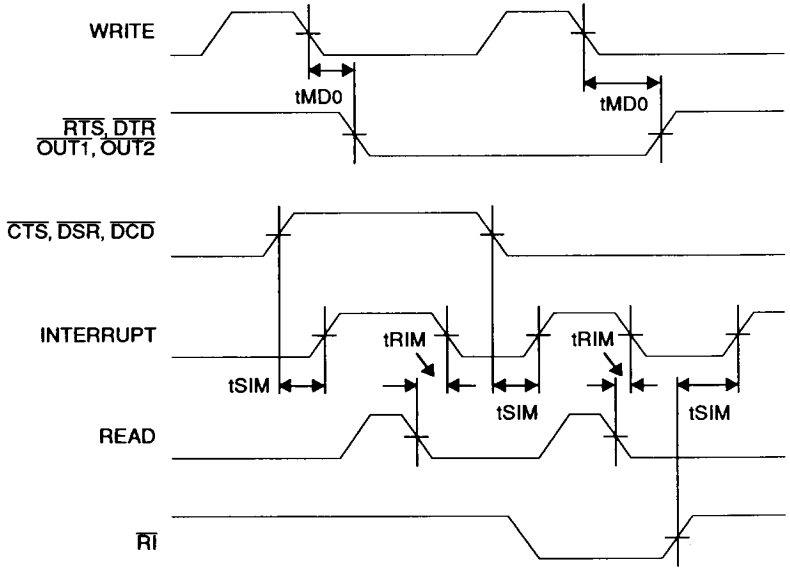
NOTES:
1. SEE WRITE CYCLE TIMING; WRITE IS A PRODUCT OF WR, $\overline{WR}$ AND CS0, CS1, $\overline{CS2}$
2. SEE READ CYCLE TIMING; READ IS A PRODUCT OF RD, $\overline{RD}$ AND CS0, CS1, $\overline{CS2}$

FIGURE 6: Transmitter Timing

AC CHARACTERISTICS (continued)

MODEM CONTROL (Refer to Figure 7.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tMDO	Delay from WRITE MCR to Output	100 pF load		200	ns
tSIM	Delay to Set Interrupt from Modem Input	100 pF load		250	ns
tRIM	Delay to Interrupt negation from READ	100 pF load		250	ns



NOTES:
1. SEE WRITE CYCLE TIMING; READ OCCURS WHEN BOTH READ (RD, $\overline{RD}$) AND CHIP SELECT (CS, CS1, $\overline{CS2}$, LATCHED BY $\overline{ADS}$) ARE ASSERTED.
2. SEE READ CYCLE TIMING; WRITE OCCURS WHEN BOTH WRITE (WR, $\overline{WR}$) AND CHIP SELECT (CS, CS1, $\overline{CS2}$, LATCHED BY $\overline{ADS}$) ARE ASSERTED.

FIGURE 7: Modem Controls Timing

AC CHARACTERISTICS (Continued)

BAUD GENERATOR (Refer to Figure 8.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
N	Baud Divisor		1	2^{16}-1	
tBLD	Baud Output Negative Edge Delay	100 pF load		125	ns
tBHD	Baud Output Positive Edge Delay	100 pF load		125	ns
tLW	Baud Output Down Time	fX=2 MHz, div. by 2, 100 pF load	425		ns
tHW	Baud Output Up Time	fX=3 MHz, div. by 3, 100 pF load	250		ns

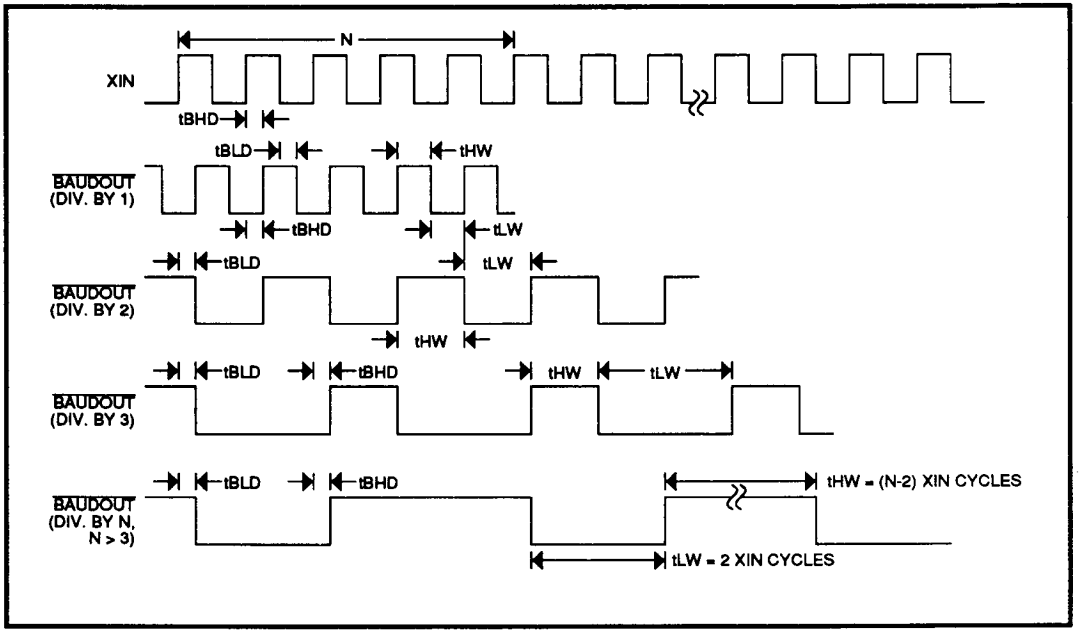
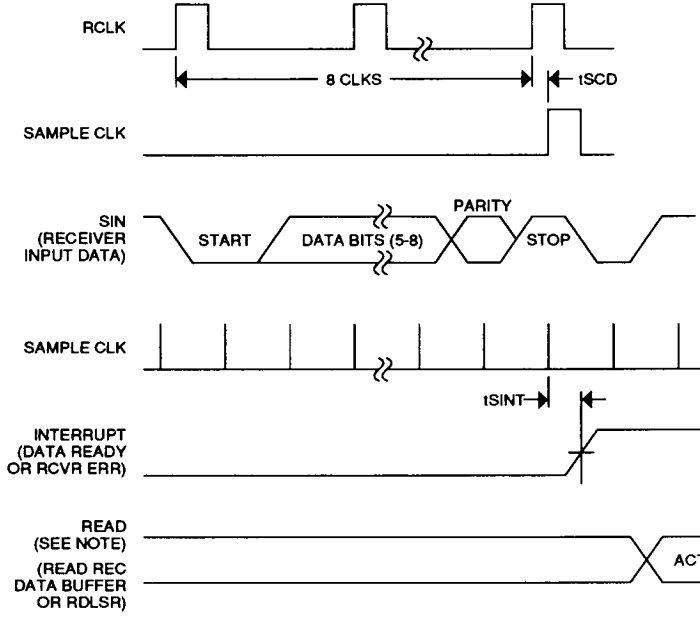


FIGURE 8: $\overline{\text{BAUDOUT}}$ Timing

AC CHARACTERISTICS (Continued)

RECEIVER (Refer to Figure 9.)

PARAMETER		CONDITIONS	MIN	MAX	UNITS
tSCD	Delay from RCLK to Sample Time			2	µs
tSINT	Delay from Stop to Set Interrupt	RCLK=tXH & tXL		1	RCLK cycles
tRINT	Delay from READ (READ RBR, READ LSR to Interrupt negation	100 pF load		1	µs



NOTE: SEE READ CYCLE TIMING; READ OCCURS WHEN BOTH READ (RD, $\overline{RD}$) AND CHIP SELECT (CS, CS1, $\overline{CS2}$, LATCHED BY $\overline{ADS}$) ARE ASSERTED.

FIGURE 9: Receiver Timing

SSI 73M450L TIMING COMPARED TO PCMCIA PC CARD STD. - RELEASE 2.0

ITEM	SYMBOL	IEEE	MIN	MAX	SSI 73M450L			
					SSI	MIN	MAX	UNITS
Data Setup before IOWR	t su (IOWR)	tDVIWL	60		TDS	30		ns
Data Hold following IOWR	t h (IOWR)	tIWHDX	30		TDH	30		ns
IOWR Width Time	t w IOWR	tIWLIWH	165		TWR	80		ns
Address Setup before IOWR	t su A (IOWR)	tAVIWL	70		TAW	30		ns
Address Hold following IOWR	t h A (IOWR)	tIWHAX	20		TWA	20		ns
CE Setup before IOWR	t su CE (IOWR)	tELIWL	5			Any		
CE Hold following IOWR	t h CE (IOWR)	tIWHEH	20			Any		
REG Setup before IOWR	t su REG (IOWR)	tRGLIWL	5					
REG Hold following IOWR	t h REG (IOWR)	tIWHRGH	0					
IOIS16 Delay Falling from Address	t d IOIS16 $(ADR)_1$	tAVISL		35				
IOIS16 Delay Rising from Address	t d IOIS16 $(ADR)_2$	tAVISH		35				
Wait Delay Falling from IOWR	t d WAIT (IOWR)	tIWLWTL		35				
Wait Width Time	t w WAIT	tWLWTH		12,000				
NOTE: The maximum load on WAIT, INPACK and IOIS16 are 1 LSTTL with 50 pF total load.								

TABLE 5: I/O Output (WRITE) Timing Specification for All 5V I/O Cards

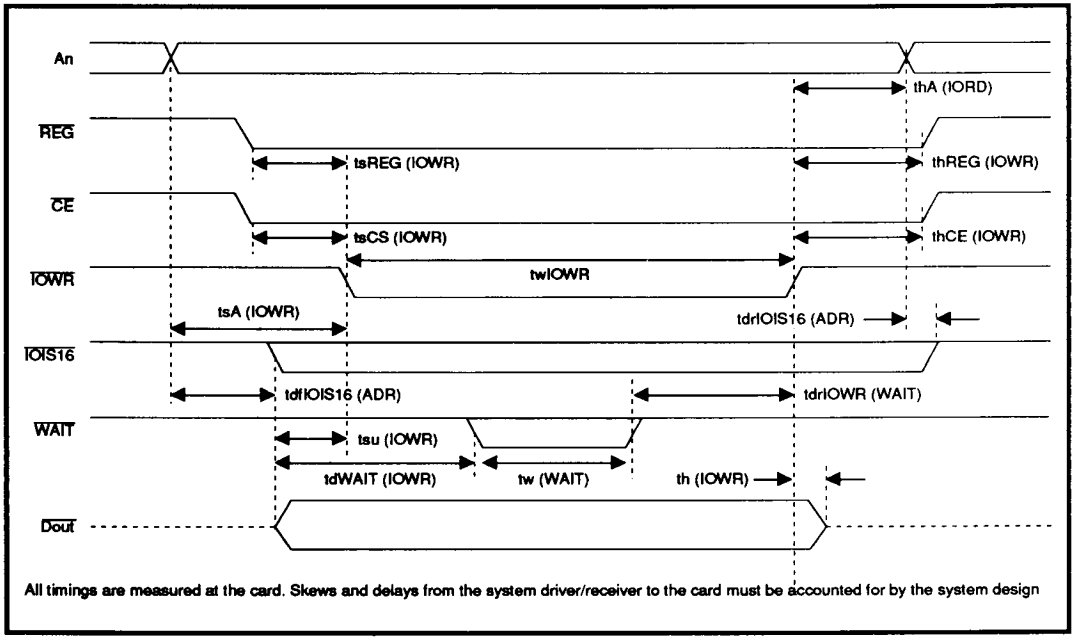


FIGURE 10: I/O Output Timing Specification (WRITE)

SSI 73M450L TIMING COMPARED TO PCMCIA PC CARD STD. - RELEASE 2.0

ITEM	SYMBOL	IEEE	MIN	MAX	SSI 73M450L			
					SSI	MIN	MAX	UNITS
Data Delay after IORD	t d (IORD)	tIGLQV		100	TRVD		80	ns
Data Hold following IORD	t h (IORD)	tIGHQX	0		THZ	0		ns
IORD Width Time	t w IORD	tIGLIGH	165		TRD	80		ns
Address Setup before IORD	t su A (IORD)	tAVIGL	70		TAR	30		ns
Address Hold following IORD	t h A (IORD)	tIGHAX	20		TRA	20		ns
CE Setup before IORD	t su CE (IORD)	tELIGL	5			Any		
CE Hold following IORD	t h CE (IORD)	tIGHEH	20			Any		
REG Setup before IORD	t su REG (IORD)	tRGLIGL	5					
REG Hold following IORD	t h REG (IORD)	tIGHRGH	0					
INPACK Delay Falling from IORD	t d INPACK (IORD)	tGLIAL	0	45				
INPACK Delay Rising from IORD	t d INPACK (IORD)	tIGHIAH		45				
IOIS16 Delay Falling from Address	t d IOIS16 $(ADR)_1$	tAVISL		35				
IOIS16 Delay Rising from Address	t d IOIS16 $(ADR)_2$	tAVISH		35				
Wait Delay Falling from IORD	t d WAIT (IORD)	tIGLWTL		35				
Data Delay from Wait Rising	td(WAIT)	tWTHQV		35				
Wait Width Time	t w WAIT	tWLWTH		12,000				
NOTE: The maximum load on WAIT, INPACK and IOIS16 are 1 LSTTL with 50 pF total load.								

TABLE 6: I/O Output (READ) Timing Specification for All 5V I/O Cards

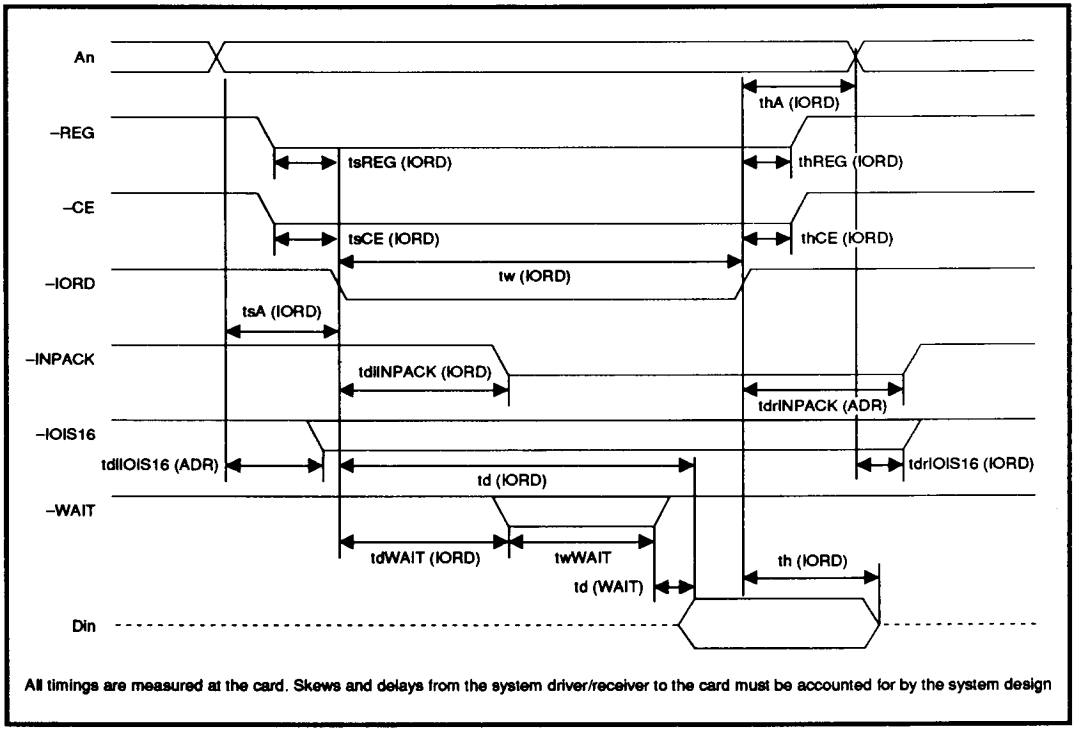


FIGURE 11: I/O Output Timing Specification (READ)

APPLICATIONS INFORMATION

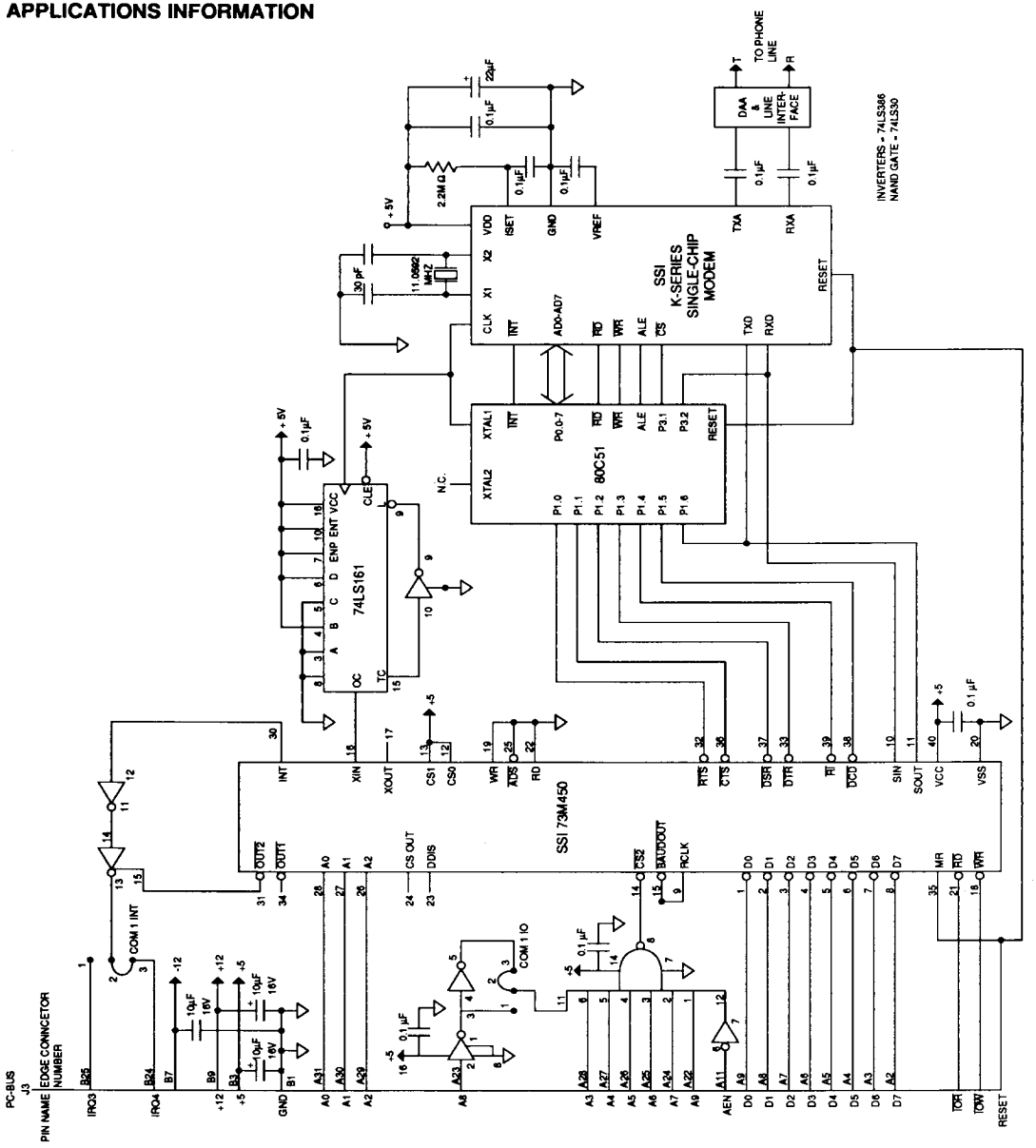
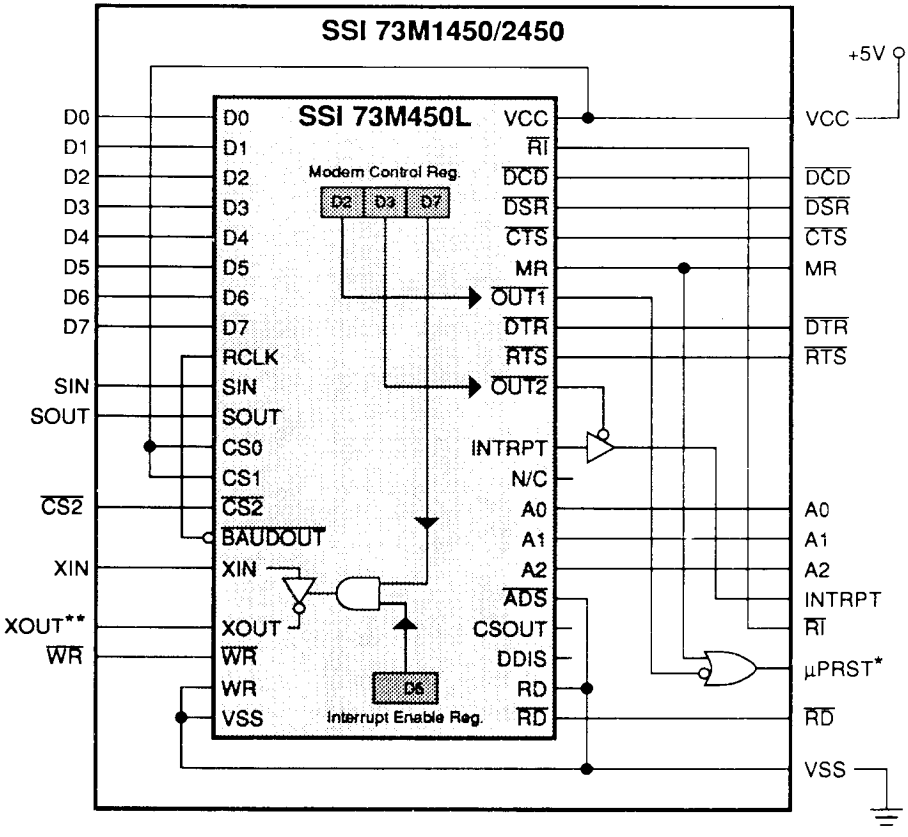


FIGURE 12: Typical Application showing Modem Interface to PC-Bus via SSI 73M450 UART

APPLICATIONS INFORMATION (continued)

28-PIN VERSION

The 73M450L is available in two 28-pin configurations: SSI 73M1450 and SSI 73M2450. The relation between these two products and the 40-pin version is shown in the accompanying diagram. Note that the only difference between the 73M1450 and 73M2450 is that the 73M2450 adds the µPRST pin at the expense of the XOUT pin.

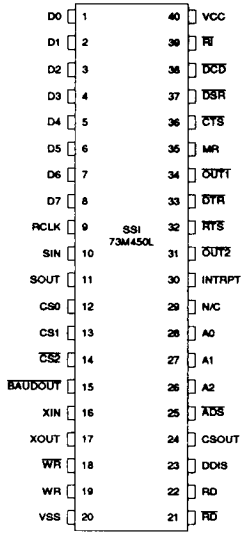


*SSI 73M2450 only.
**SSI 73M1450 only.

FIGURE 13: Adapter Diagram Showing Internal Connections and Bond-outs from 40-pin to 28-pin Packages

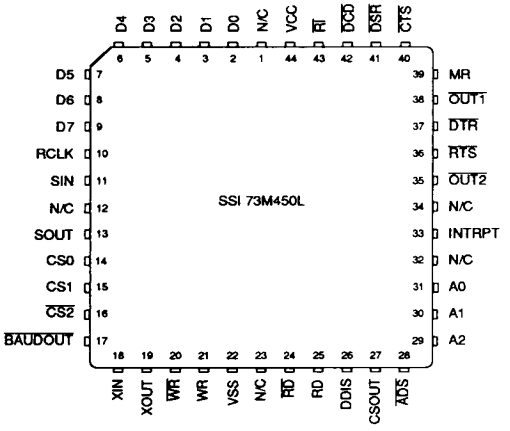
PACKAGE PIN DESIGNATIONS

(Top View)

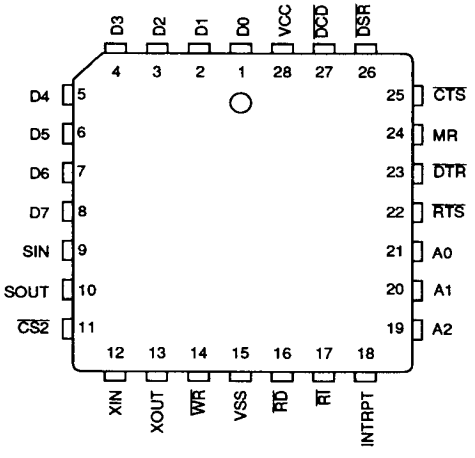


SSI 73M450L 40-Pin DIP

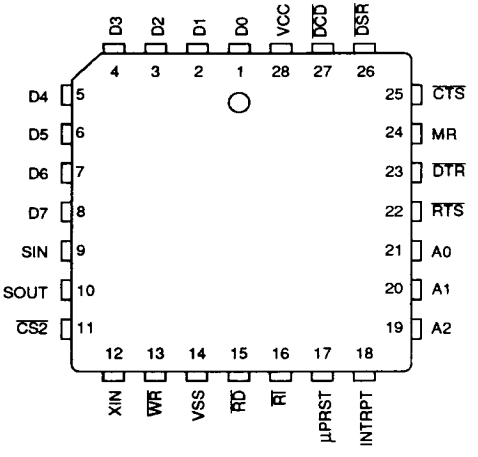
CAUTION: Use handling procedures necessary for a static sensitive component.



SSI 73M450L 44-Pin PLCC



SSI 73M1450 UART
28-Pin PLCC



SSI 73M2450 UART
28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 73M450L	40-pin PDIP	73M450L-IP	73M450-IP
	44-pin PLCC	73M450L-IH	73M450-IH
SSI 73M1450	28-pin PLCC	73M1450-IH	73M1450-IH
SSI 73M2450	28-pin PLCC	73M2450-IH	73M2450-IH

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