NEC Electronics Inc.

μPD70P322 16-Bit Microcomputer: Single-Chip, CMOS, With EPROM for V25/V35 Modes

Description

The μPD70P322 is a 16-bit, single-chip CMOS microcomputer operable as a μPD70322 (V25™) or a μPD70332 (V35™). The mask ROM of the V25/V35 is replaced in the μPD70P322 by an EPROM.

Ordering Information

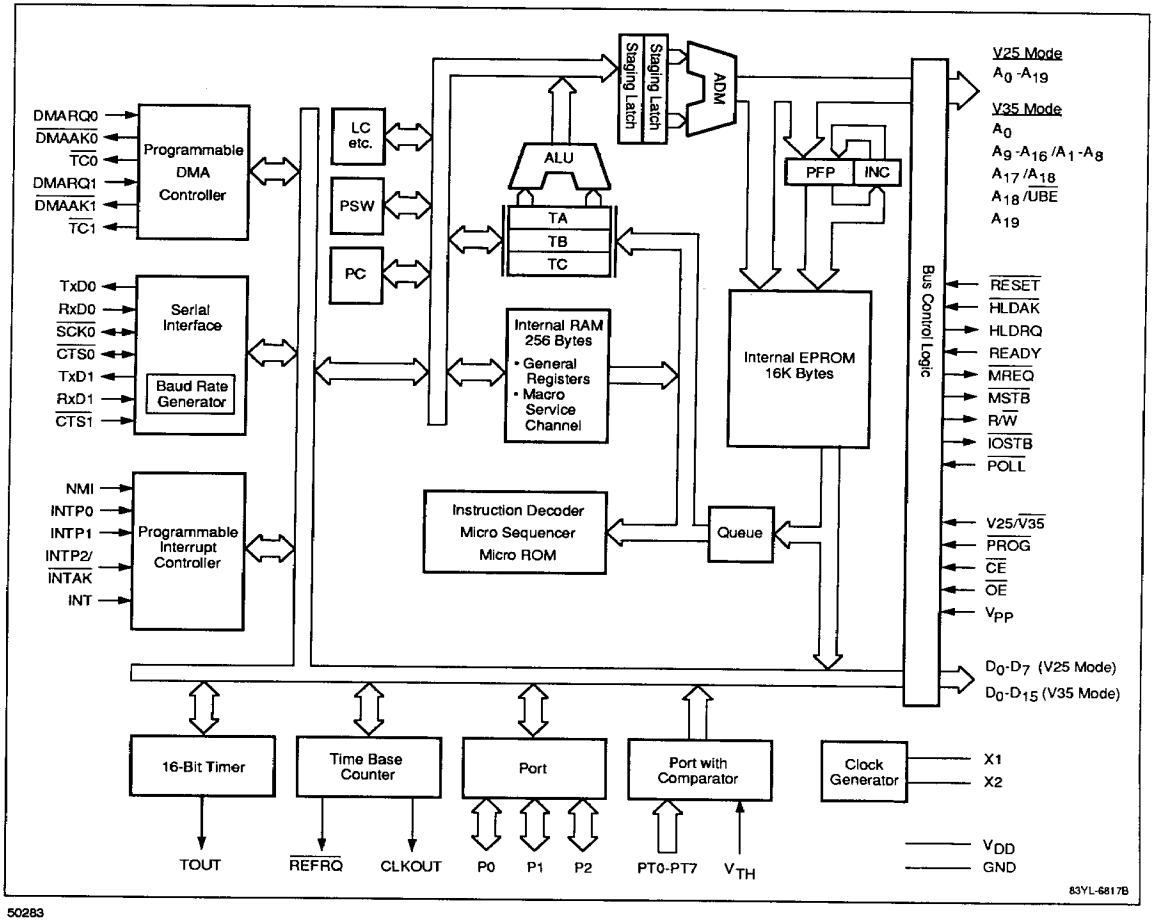
Part Number	Ext Input Frequency	Int System Clock	Package
μPD70P322KE-8	16 MHz	8 MHz	84-pin ceramic LCC with quartz window

V25 and V35 are trademarks of NEC Corporation

Features

- Reprogrammable EPROM appropriate for system evaluation of V25 or V35
- V25 mode (μPD70322 equivalent)
  - Internal 16-bit architecture
  - External 8-bit data bus
- V35 mode (μPD70332 equivalent)
  - Internal 16-bit architecture
  - External 16-bit data bus

μPD70P322 Block Diagram



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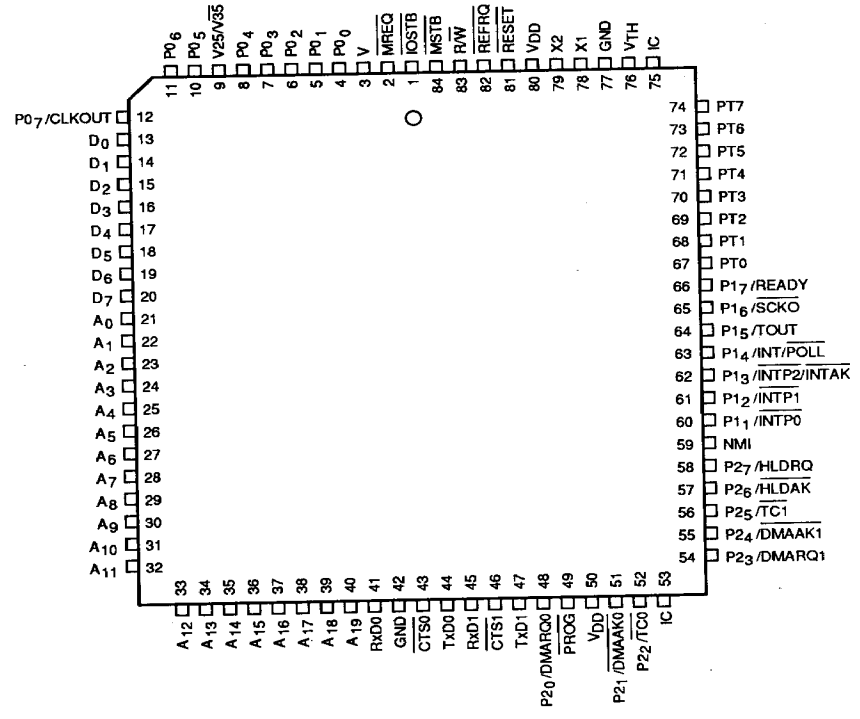
Pin Configurations

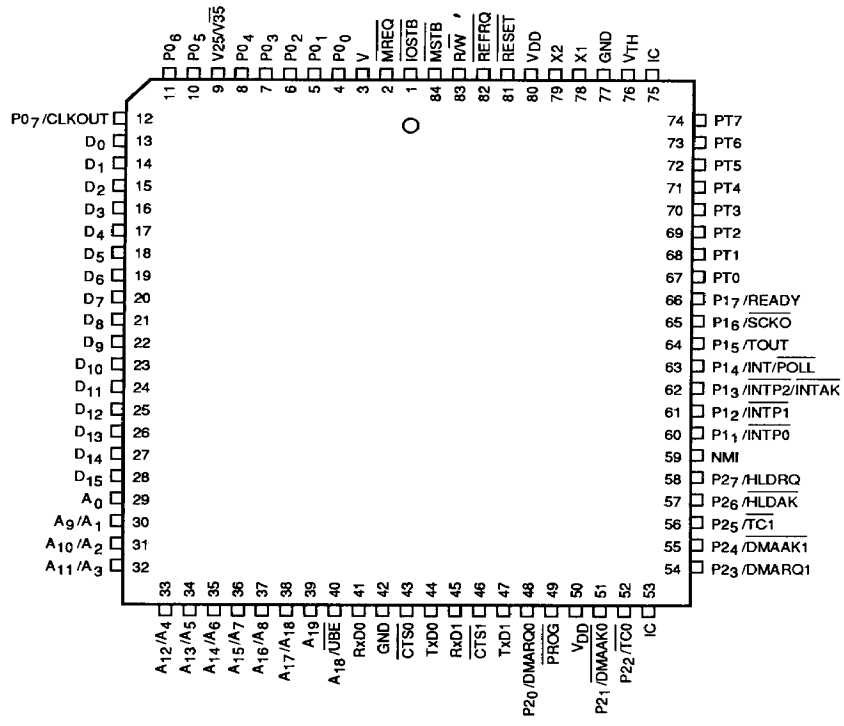
84-Pin LCC, V25 Mode



Pin	Symbol	Connect to
3	V	V_{DD}
9	V25/$\overline{V35}$	High level (H)
49	$\overline{PROG}$	High level (H)
53, 75	IC	High level through pullup resistor

83YL-6794B

84-Pin LCC, V35 Mode



Pin	Symbol	Connect to
3	V	V_{DD}
9	V25/$\overline{V35}$	Low level (L)
49	$\overline{PROG}$	High level (H)
53, 75	IC	High level through pullup resistor

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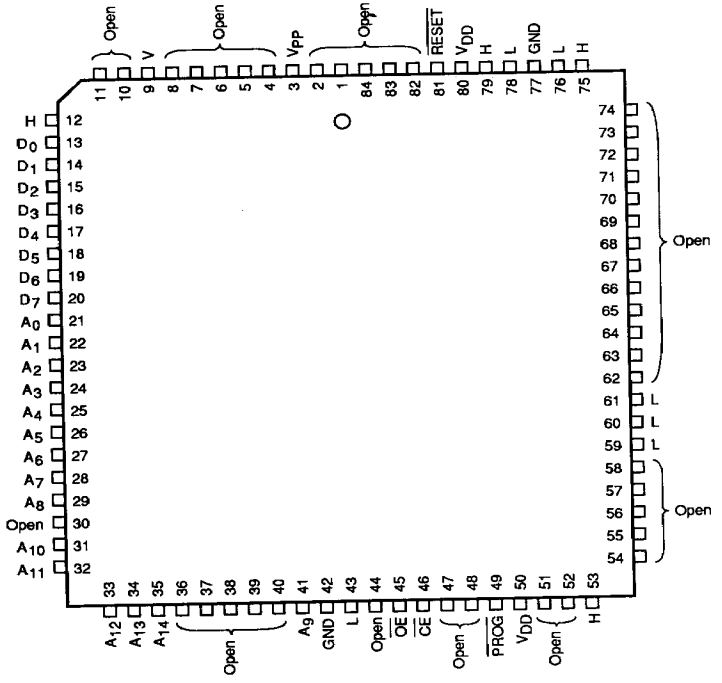
84-Pin LCC, EPROM Programming Mode



Pin	Symbol	Connect to
9	V	V_{DD}
49	$\overline{PROG}$	Low level through pullup resistor
	L	Low level through pullup resistor
	H	High level through pullup resistor
	Open	Do not connect to these pins.

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Pin Identification, V25/V35 Mode

Symbol	I/O	Function	Also Used For
Port Pins			
$P0_0$-$P0_6$	I/O	Input or output mode can be specified per bit	—
$P0_7$			CLKOUT
($P1_0$) NMI	In	Non-maskable interrupt; cannot be used as a general-purpose port pin.	—
$P1_1$	In	Port 1 input lines	$\overline{INTP0}$
$P1_2$			$\overline{INTP1}$
$P1_3$			$\overline{INTP2}$
$P1_4$	I/O	Input or output mode can be specified per bit.	$\overline{POLL}$/INT
$P1_5$			TOUT
$P1_6$			$\overline{SCK0}$
$P1_7$			READY
$P2_0$	I/O	Input or output mode can be specified per bit	DMARQ0
$P2_1$			$\overline{DMAAK0}$
$P2_2$			$\overline{TC0}$
$P2_3$			$\overline{DMARQ1}$
$P2_4$			$\overline{DMAAK1}$
$P2_5$			$\overline{TC1}$
$P2_6$			$\overline{HLDAK}$
$P2_7$			HLDRQ
PT0-PT7	In	Comparator input	—
Pins Other Than Port			
A_0	Out	V35 mode. Selects low-order memory bank	—
A_1-A_{19}	Out	V35 mode. Address bus	—
A_0-A_{19}	Out	V25 mode. Address bus	—
CLKOUT	Out	System clock	$P0_7$
$\overline{CTS0}$	I/O	Asynchronous mode: send instruction input I/O interface mode: receive clock input/output	—
$\overline{CTS1}$	In	Send instruction input	—
D_0-D_7	I/O	V25 mode. 8-bit data bus	—
D_0-D_{15}	I/O	V35 mode. 16-bit data bus	—
$\overline{DMAAK0}$	Out	DMA acknowledge	$P2_1$
$\overline{DMAAK1}$			$P2_4$
DMARQ0	In	DMA request	$P2_0$
DMARQ1			$P2_3$
$\overline{HLDAK}$	Out	Hold acknowledge	$P2_6$
HLDRQ	In	Hold request	$P2_7$
INT	In	External interrupt request	$P1_4$/$\overline{POLL}$

Symbol	I/O	Function	Also Used For
$\overline{INTAK}$	Out	Interrupt acknowledge	$P1_3$/$\overline{INTP2}$
$\overline{INTP0}$	In	External interrupt request	$P1_1$
$\overline{INTP1}$			$P1_2$
$\overline{INTP2}$			$P1_3$/$\overline{INTAK}$
$\overline{IOSTB}$	Out	I/O access strobe	
$\overline{MREQ}$	Out	Indicates memory bus cycle start	
$\overline{MSTB}$	Out	Memory access strobe	
$\overline{POLL}$	In	Wait insertion	$P1_4$/INT
READY	In	External ready	$P1_7$
$\overline{REFRQ}$	Out	DRAM refresh pulse	
$\overline{RESET}$	In	Chip reset	
R/$\overline{W}$	Out	Indicates read cycle/write cycle	
RxD0, RxD1	Out	Serial data	
$\overline{SCK0}$	Out	Serial clock	$P1_6$
$\overline{TC0}$	Out	Indicates DMA completion	$P2_2$
$\overline{TC1}$			$P2_5$
TOUT	Out	Timer output	$P1_5$
TxD0, TxD1	In	Serial data	
$\overline{UBE}$	Out	V35 mode. Selects high-order memory bank	
V25/$\overline{V35}$	In	V25 or V35 mode selection	
X1, X2	In	Internal oscillator: connect crystal or ceramic resonator to X1 and X2. External clock: connect opposite-phase clock inputs to X1 and X2.	
V_{DD}	In	+5-volt power supply pin (both V_{DD} pins are connected)	
V_{TH}	In	Comparator reference voltage	
GND		Ground pin (both GND pins are connected)	

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Pin Identification, EPROM Programming Mode

Symbol	I/O	Function
A_0-A_{14}	In	Address bus
$\overline{CE}$	In	Chip enable
D_0-D_7	I/O	Data bus
$\overline{OE}$	In	Output enable
$\overline{PROG}$	In	EPROM programming mode setting
$\overline{RESET}$	In	EPROM mode setting
V_{PP}	In	Write power supply pin
V_{DD}	In	+5-volt power supply pin (both V_{DD} pins are connected
GND	—	Ground pin (both GND pins are connected)

EPROM PROGRAMMING

The three basic modes of the μPD70P322 are controlled by the level at the $\overline{PROG}$, V25/$\overline{V35}$, and $\overline{RESET}$ pins. (H = high level; L = low level; x = don't care).

Mode	$\overline{PROG}$	V25/$\overline{V35}$	$\overline{RESET}$
V25	H	H	x
V35	H	L	x
Program	L	x	L

Table 1 lists the operations that take place in programming mode and the conditions at the power and control pins. Table 2 lists the recommended conditions at pins not used in programming mode.

Table 1. Conditions at Pins Used in Programming Mode

Operation Mode	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}
Read	L	L	+5 V	+5 V
Output disable	L	H		
Standby	H	x		
Program	L	H	+12.5 V	+6 V
Program verify	x	L		
Program inhibit	H	H		

Notes:

(1) $\overline{PROG}$ and $\overline{RESET}$ = L

(2) Apply voltage to V_{DD} before V_{PP}. Remove voltage from V_{PP} before V_{DD}.

(3) Never apply more than 13.5 V to V_{PP} even with overshoot.

(4) x = L or H

(5) With A_{14} set to 1 (addresses 4000H-7FFFH), write ROM data. At verification, output data should be FFH. Thus, it is invalid to write program setting A_{14} to 1.

Table 2. Conditions at Pins Not Used in Programming Mode

Connection	Pins
Pullup resistor	12, 53, 75, 79
Pulldown resistor	43, 59-61, 76, 78
Pullup or pulldown	9
No connection	1-2, 4-8, 10-11, 30, 36-40, 47-48, 51-52, 54-58, 62-74, 82-84

EPROM Write Procedure

Figure 1 is the flowchart and figure 2 is the timing diagram for the following EPROM write procedure.

Note: The protection seal on the quartz window of the μPD70P322 must be in place.

(1) Apply +6 volts to the V_{DD} pins and +12.5 volts to the V_{PP} pin.

(2) Supply initial address A_{13}-A_0.

(3) Supply write data D_7-D_0.

(4) Apply 1-ms program pulse (active low) to $\overline{CE}$ pin.

(5) Change to verify operation mode. If data can be written normally, go to step (8).

(6) If data cannot be written normally, repeat steps (3) to (5).

(7) If data cannot be written after 25 repetitions, declare the device faulty. Stop the write operation.

(8) Supply write data.

(9) Increment address.

(10) Repeat steps (3) to (9) until the end address is reached.

EPROM Read Procedure

With the μPD70P322 set up for read operation (table 1), the EPROM contents are read into the external data bus according to the procedure below. Figure 3 is a simplified timing diagram.

(1) Apply +5 volts to the V_{DD} pins.

(2) Apply +5 volts to the V_{PP} pins.

(3) Input the address of the data to be read to pins A_{13}-A_0.

(4) Perform read mode operation.

(5) Output data to pins D_7-D_0.

EPROM Erasure

Data in the EPROM is erased by exposing the quartz window in the ceramic package to light having a wavelength shorter than 400 nm, including ultraviolet rays, direct sunlight, and fluorescent light.

Note: To prevent unintentional erasure, the protection seal on the quartz window should not be removed except for EPROM erasure.

Typically, data is erased by 254-nm ultraviolet rays. A minimum lighting level of 15 W•s/cm^2 (ray intensity x exposure time) is required to completely erase the EPROM. Erasure by an ultraviolet lamp rated at 12 mW/cm^2 takes about 15 to 20 minutes. The time may be prolonged because of a degraded lamp, dirty window, etc. Remove any filter on the lamp and place the device within 2.5 cm of the lamp tubes.

Figure 1. EPROM Write Procedure Flowchart

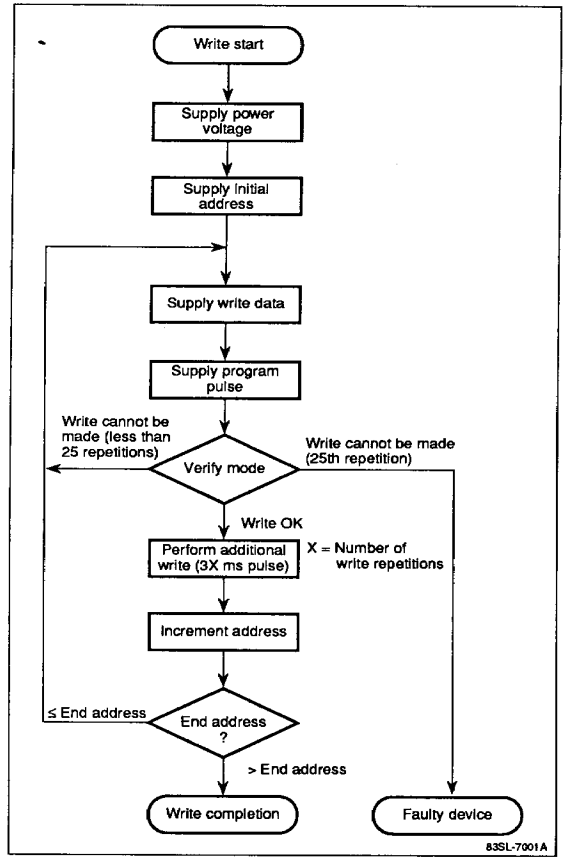

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Figure 2. EPROM Write and Verify Timing

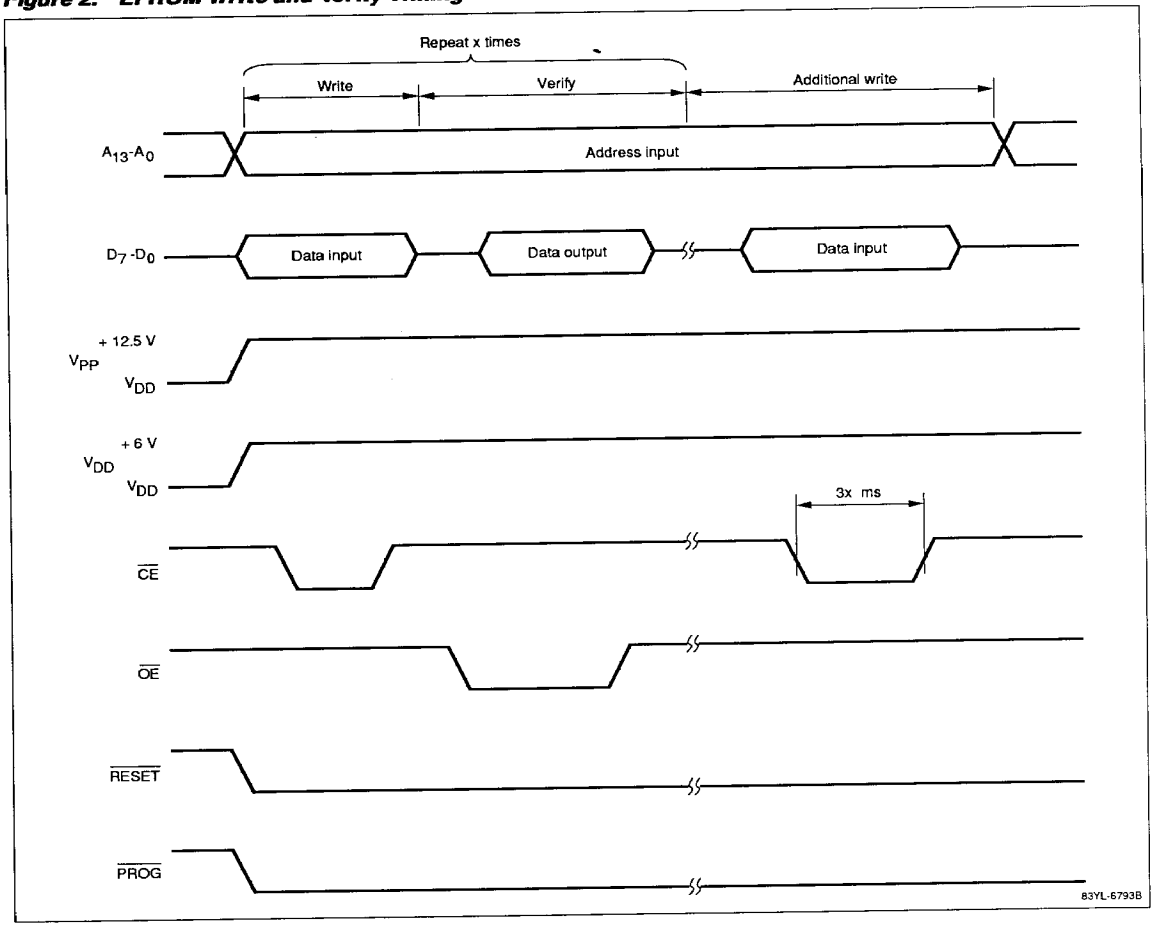
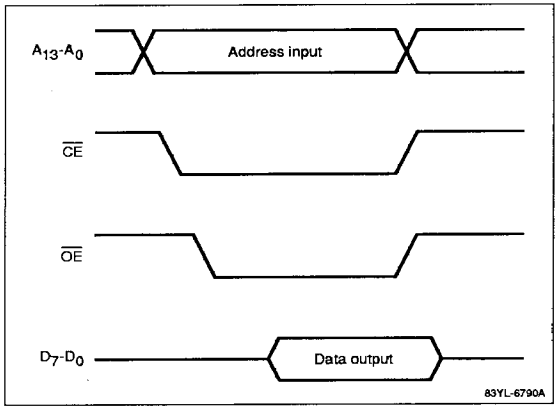


Figure 3. EPROM Read Timing



INSTALLATION

Direct soldering to pins of the μPD70P322 is not allowed. The device must be installed in a socket.

ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings

T_A = 25°C

Supply voltage, V_{DD}	−0.5 to +7.0 V
Input voltage, V_I	−0.5 to V_{DD}+0.5 ≤ +7.0 V
Output voltage, V_O	−0.5 to V_{DD}+0.5 ≤ +7.0 V
Threshold voltage, V_{TH}	−0.5 to V_{DD}+0.5 ≤ +7.0 V
Output current low, I_{OL}	Each output pin 4.0 mA (total 50 mA)
Output current high, I_{OH}	Each output pin −2.0 mA (total −20 mA)
Operating temperature range, T_{OPT}	−40 to +85°C
Storage temperature range, T_{STG}	−65 to +150°C

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage.

Capacitance

T_A = 25°C; V_{DD} = 0 V

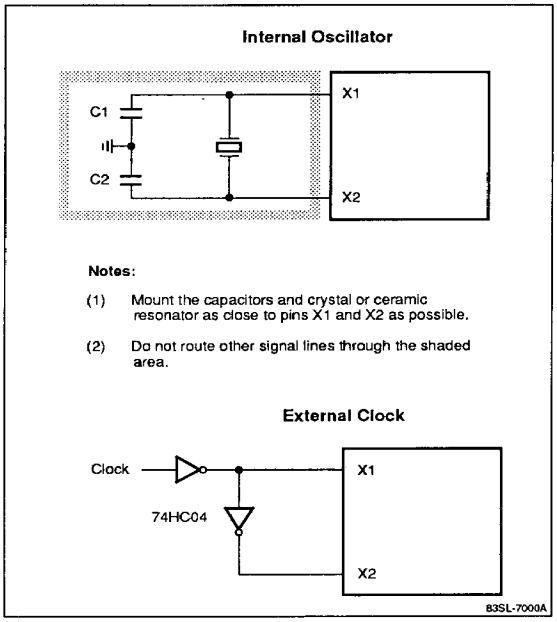
Parameter	Symbol	Max	Unit	Conditions
Input capacitance	C_I	10	pF	f_C = 1 MHz; unmeasured pins returned to ground
Output capacitance	C_O	20	pF	
I/O capacitance	C_{IO}	20	pF	

System Clock

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10%; V_{SS} = 0 V; V_{TH} = 0 to V_{DD} + 1

	μPD70P322		μPD70P322-8		
Parameter	**Min**	**Max**	**Min**	**Max**	**Unit**
Internal Oscillator					
Frequency, f_{XX}	4	10	4	16	MHz
External Clock					
Frequency, f_X	4	10	4	16	MHz
Rise/fall time, t_R/t_F	0	10	0	10	ns
X1 input, high/low level width, t_{OH}/t_{OL}	35	250	20	250	ns

System Clock Control Circuit



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Recommended Oscillator Components

Ceramic Resonator (Note 1)		Capacitors	
Manufacturer	Product No.	C1 (pF)	C2 (pF)
Kyocera	KBR-10.0M	33	33
Murata Mfg.	CSA.10.0MT	47	47
	CSA16.0MX040	30	30
TDK	FCR10.M2S	30	30
	FCR16.0M2S	15	6

Crystal (Note 2)		Capacitors	
Manufacturer	Product No.	C1 (pF)	C2 (pF)
Kinseki	HC-49/U	15	15
	HC-43/U	15	15

Notes:

(1) Ceramic resonator product no. includes the frequency: 10.0 or 16.0 MHz.

(2) Crystal frequencies: 10, 16 MHz.

DC Characteristics 1; V25/V35 Mode

T_A = −10 to +70°C; V_{DD} = +5.0 V ±10 %

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input voltage, low	V_{IL}	0		0.8	V	
Input voltage, high	V_{IH1}	2.2		V_{DD}	V	All except $\overline{RESET}$, $P1_0$/NMI, X1, X2
	V_{IH2}	0.8 V_{DD}		V_{DD}	V	$\overline{RESET}$, $P1_0$/NMI, X1, X2
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 1.6 mA
Output voltage, high	V_{OH}	V_{DD} − 1.0			V	I_{OH} = −0.4 mA
Input current	I_{IN}			±20	μA	$\overline{EA}$, $P1_0$/NMI; V_{IN} = 0 to V_{DD}
Input leakage current	I_{LI}			±10	μA	All except $\overline{EA}$, $P1_0$/NMI; V_{IN} = 0 to V_{DD}
Output leakage current	I_{LO}			±10	μA	V_O = 0 to V_{DD}
V_{TH} supply current	I_{TH}		0.5	1.0	mA	V_{TH} = 0 to V_{DD}
V_{DD} supply current, μPD70P322	I_{DD1}		50	100	mA	Operation mode
	I_{DD2}		20	40	mA	HALT mode
	I_{DD3}		10	30	μA	STOP mode
V_{DD} supply current, μPD70P322-8	I_{DD1}		65	120	mA	Operation mode
	I_{DD2}		25	50	mA	HALT mode
	I_{DD3}		10	30	μA	STOP mode

DC Characteristics 2; EPROM Program Operation

T_A = 25 ±5°C; V_{DD} = 6.0 ±0.25 V; V_{PP} = 12.5 ±0.3 V

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Input voltage, high	V_{IH}	2.2		V_{DD} + 0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LI}			10	μA	V_{IH} = 0 to V_{DD}
Output voltage, high	V_{OH}	V_{DD} − 1			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 1.6 mA
V_{DD} supply current	I_{DD}		40		mA	
V_{PP} supply current	I_{PP}		30		mA	$\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}

DC Characteristics 3; EPROM Read Operation

T_A = 25 ±5°C

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Power supply voltage	V_{DD}	4.5	5.0	5.5	V	
Write power supply voltage	V_{PP}				V	$V_{PP} = V_{DD}$
Input voltage, high	V_{IH}	2.2		V_{DD} + 0.3	V	
Input voltage, low	V_{IL}	−0.3		0.8	V	
Input leakage current	I_{LI}			10	μA	V_{IN} = 0 to V_{DD}
Output voltage, high	V_{OH}	V_{DD} − 1			V	I_{OH} = −400 μA
Output voltage, low	V_{OL}			0.45	V	I_{OL} = 1.6 mA
Output leakage current	I_{LO}			10	μA	V_{OUT} = 0 to V_{DD}; $\overline{OE}$ = V_{IH}
V_{DD} supply current	I_{DD}			40	mA	$\overline{CE}$ = V_{IL}; V_{IN} = V_{IH}
V_{PP} supply current	I_{PP}		1	100	μA	$V_{PP} = V_{DD}$

AC Characteristics 1; V25/V35 Mode

T_A = −10 to +70°C; f_{CLK} = 0.5 to 5 MHz with V_{DD} = 5 V ±10%; f_{CLK} = 5 to 8 MHz with V_{DD} = 5 V ±5%

		70P322		70P322-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Conditions
Input rise, fall times	t_{IR}, t_{IF}		20		20	ns	Except X1, X2, $\overline{RESET}$, NMI
Input rise, fall times (Schmitt)	t_{IRS}, t_{IFS}		30		30	ns	$\overline{RESET}$, NMI
Output rise, fall times	t_{OR}, t_{OF}		20		20	ns	Except CLKOUT
X1 cycle time	t_{CYX}	98	250	62	250	ns	
X1 width, low	t_{WXL}	35		20		ns	
X1 width, high	t_{WXH}	35		20		ns	
X1 rise, fall times	t_{XR}, t_{XF}		20		20	ns	
CLKOUT cycle time	t_{CYK}	200	2000	125	2000	ns	CLKOUT = $f_X/2$
CLKOUT width, low	t_{WKL}	0.5T − 15		0.5T − 15		ns	T = t_{CYK}
CLKOUT width, high	t_{WKH}	0.5T − 15		0.5T − 15		ns	
CLKOUT rise, fall times	t_{KR}, t_{KF}		15		15	ns	

AC Characteristics 2; V25 Mode

T_A = −10 to +70°C; C_L = 100 pF (max); T = t_{CYK}; n = number of wait states inserted
f_{CLK} = 0.5 to 5 MHz with V_{DD} = 5 V ±10%; f_{CLK} = 5 to 8 MHz with V_{DD} = 5 V ±5%

Parameter	Symbol	Min	Max	Unit	Conditions
Address delay time	t_{DKA}		90	ns	
Address valid to input data valid	t_{DADR}		(n+1.5)T − 90	ns	
$\overline{MREQ}$ to data delay time	t_{DMRD}		(n+1)T − 75	ns	
$\overline{MSTB}$ to data delay time	t_{DMSD}		(n+0.5)T − 75	ns	
$\overline{MREQ}$ to $\overline{TC}$ delay time	t_{DMRTC}		0.5T + 50	ns	
$\overline{MREQ}$ to $\overline{MSTB}$ delay time	t_{DMRMS}	0.5T − 35	0.5T + 35	ns	
$\overline{MREQ}$ width, low	t_{WMRL}	(n+1)T − 30		ns	
Address hold time	t_{HMA}	0.5T − 30		ns	
Input data hold time	t_{HMDR}	0		ns	
Next control setup time	t_{SCC}	T − 25		ns	
$\overline{TC}$ width, low	t_{WTCL}	2T − 30		ns	

AC Characteristics 2; V25 Mode (cont)

Parameter	Symbol	Min	Max	Unit	Conditions
Address data output	t_{DADW}		0.5T + 50	ns	
$\overline{MREQ}$ delay time	t_{DAMR}	0.5T – 30		ns	
$\overline{MSTB}$ delay time	t_{DAMS}	T – 30		ns	
$\overline{MSTB}$ width, low	t_{WMSL}	(n+0.5)T – 30		ns	
Data output setup time	t_{SDM}	(n+1)T – 50		ns	
Data output hold time	t_{HMDW}	0.5T – 30		ns	
$\overline{IOSTB}$ delay time	t_{DAIS}	0.5T – 30		ns	
$\overline{IOSTB}$ to data input	t_{DISD}		(n+1)T – 90	ns	
$\overline{IOSTB}$ width, low	t_{WISL}	(n+1)T – 30		ns	
Address hold time	t_{HISA}	0.5T – 30		ns	
Data input hold time	t_{HISDR}	0		ns	
Output data setup time	t_{SDIS}	(n+1)T – 50		ns	
Output data hold time	t_{HISDW}	0.5T – 30		ns	
Next DMARQ setup time	t_{SDADQ}		T	ns	Demand mode
DMARQ hold time	t_{HDADQ}	0		ns	Demand mode
$\overline{DMAAK}$ read width, low	t_{WDMRL}	(n+1.5)T – 30		ns	
$\overline{DMAAK}$ to $\overline{TC}$ delay time	t_{DDATC}		0.5T + 50	ns	
$\overline{DMAAK}$ write width, low	t_{WDMWL}	(n+1)T – 30		ns	
$\overline{REFRQ}$ delay time	t_{DARF}	0.5T – 30		ns	
$\overline{REFRQ}$ width, low	t_{WRFL}	(n+1)T – 30		ns	
Address hold time	t_{HRFA}	0.5T – 30		ns	
$\overline{RESET}$ width, low	t_{WRSL1}	30		ms	STOP mode release/Power-on reset
$\overline{RESET}$ width, low	t_{WRSL2}	5		μs	System reset
$\overline{MREQ}$, $\overline{IOSTB}$ to READY setup time	t_{SCRY}		(n – 1)T – 100	ns	n ≥ 2
$\overline{MREQ}$, $\overline{IOSTB}$ to READY hold time	t_{HCRY}	(n – 1)T		ns	n ≥ 2
$\overline{HLDAK}$ output delay time	t_{DKHA}		80	ns	
BUS control float to $\overline{HLDAK}$ ↓	t_{CFHA}	T – 50		ns	
$\overline{HLDAK}$ ↑ to control output time	t_{DHAC}	T – 50		ns	
HLDRQ ↓ to control output time	t_{DHQC}	3T + 30		ns	
$\overline{HLDAK}$ width, low	t_{WHAL}	T		ns	
HLDRQ setup time	t_{SHQK}	30		ns	
HLDRQ to $\overline{HLDAK}$ delay time	t_{DHQHA}		3T + 160	ns	
HLDRQ width, low	t_{WHQL}	1.5T		ns	
INTP, DMARQ setup time	t_{SIQK}	30		ns	
INTP, DMARQ width, high	t_{WIQH}	8T		ns	
INTP, DMARQ width, low	t_{WIQL}	8T		ns	
$\overline{POLL}$ setup time	t_{SPLK}	30		ns	
NMI width, high	t_{WNIH}	5		μs	
NMI width, low	t_{WNIL}	5		μs	
$\overline{CTS}$ width, low	t_{WCTL}	2T		ns	

AC Characteristics 2; V25 Mode (cont)

Parameter	Symbol	Min	Max	Unit	Conditions
INT setup time	t_{SIRK}	30		ns	
INT hold time	t_{HIAIQ}	0		ns	
$\overline{INTAK}$ width, low	t_{WIAL}	2T – 30		ns	
$\overline{INTAK}$ delay time	t_{DKIA}		80	ns	
$\overline{INTAK}$ width, high	t_{WIAH}	T – 30		ns	
$\overline{INTAK}$ to data delay time	t_{DIAD}		2T – 130	ns	
$\overline{INTAK}$ to data hold time	t_{HIAD}	0	0.5T	ns	
$\overline{SCK0}$ cycle time	t_{CYTK}	1000		ns	
$\overline{SCK0}$ (TSCK) width, high	t_{WSTH}	450		ns	
$\overline{SCK0}$ (TSCK) width, low	t_{WSTL}	450		ns	
TxD delay time	t_{DTKD}		210	ns	
TxD hold time	t_{HTKD}	20		ns	
$\overline{CTS0}$ (RSCK) cycle time	t_{CYRK}	1000		ns	
$\overline{CTS0}$ (RSCK) width, high	t_{WSRH}	420		ns	
$\overline{CTS0}$ (RSCK) width, low	t_{WSRL}	420		ns	
RxD setup time	t_{SRDK}	80		ns	
RxD hold time	t_{HKRD}	80		ns	

4c

AC Characteristics 3; V35 Mode

T_A = −10 to +70°C; C_L = 100 pF (max); T = t_{CYK}; n = number of wait states inserted
f_{CLK} = 0.5 to 5 MHz with V_{DD} = 5 V ±10%; f_{CLK} = 5 to 8 MHz with V_{DD} = 5 V ±5%

Parameter	Symbol	Min	Max	Unit	Conditions
Address delay time	t_{DKA}		90	ns	
Address valid to input data valid	t_{DADR}		(n+1.5)T – 90	ns	
$\overline{MREQ}$ to data delay time	t_{DMRD}		(n+2)T – 75	ns	
$\overline{MSTB}$ to data delay time	t_{DMSD}		(n+1)T – 75	ns	
$\overline{MREQ}$ to $\overline{TC}$ delay time	t_{DMRTC}		0.5T + 50	ns	
$\overline{MREQ}$ to $\overline{MSTB}$ delay time	t_{DMRMS1}	T – 35	T + 35	ns	Read operation
	t_{DMRMS2}	(n + 1)T – 35	(n + 1)T + 35	ns	Write operation
	t_{DMRMS}	0.5 T – 30		ns	
$\overline{MREQ}$ width, low	t_{WMRL}	(n+2)T – 30		ns	
Address hold time	t_{HMA}	0.5T – 30		ns	
Input data hold time	t_{HMDR}	0		ns	
Next control setup time	t_{SCC}	T – 25		ns	
$\overline{TC}$ width, low	t_{WTCL}	2T – 30		ns	
Address data output	t_{DADW}		0.5T + 50	ns	
$\overline{MREQ}$ delay time	t_{DAMR}	0.5T – 30		ns	
R/$\overline{W}$ to $\overline{MSTB}$ delay time	t_{DRMS}	0.5T – 30		ns	
	t_{DWMS}	(n + 0.5)T – 30		ns	
$\overline{MSTB}$ width, low	t_{WMSL1}	(n + 1)T – 30		ns	Read operation
	t_{WMSL2}	T – 30		ns	Write operation

AC Characteristics 3; V35 Mode (cont)

Parameter	Symbol	Min	Max	Unit	Conditions
Data output setup time	t_{SDM}	(n+2)T – 50		ns	
Data output hold time	t_{HMDW}	0.5T – 50		ns	
$\overline{IOSTB}$ delay time	t_{DMRIS}	T – 35		ns	
$\overline{IOSTB}$ to data input	t_{DISD}		(n + 1) T – 90	ns	
$\overline{IOSTB}$ width, low	t_{WISL}	(n+1)T – 30		ns	
Address hold time	t_{HISA}	0.5T – 30		ns	
Data input hold time	t_{HISDR}	0		ns	
Output data setup time	t_{SDIS}	(n+2)T – 50		ns	
Output data hold time	t_{HISDR}	0		ns	
Next DMARQ setup time	t_{SDADQ}		T	ns	Demand mode
DMARQ hold time	t_{HDADQ}	0		ns	Demand mode
$\overline{DMAAK}$ read width, low	t_{WDMRL}	(n+1.5)T – 30		ns	
$\overline{DMAAK}$ to $\overline{TC}$ delay time	t_{DDATC}		0.5T + 50	ns	
$\overline{DMAAK}$ write width, low	t_{WDMWL}	(n+2)T – 30		ns	
$\overline{REFRQ}$ delay time	t_{DARF}	0.5T – 30		ns	
$\overline{REFRQ}$ width, low	t_{WRFL}	(n+1)T – 30		ns	
Address hold time	t_{HRFA}	0.5T – 30		ns	
$\overline{RESET}$ width, low	t_{WRSL1}	30		ms	STOP mode release/Power-on reset
$\overline{RESET}$ width, low	t_{WRSL2}	5		μs	System reset
$\overline{MREQ}$, $\overline{IOSTB}$ to READY setup time	t_{SCRY}		nT – 100	ns	n ≥ 2
$\overline{MREQ}$, $\overline{IOSTB}$ to READY hold time	t_{HCRY}	nT		ns	n ≥ 2
$\overline{HLDAK}$ output delay time	t_{DKHA}		80	ns	
BUS control float to $\overline{HLDAK}$ ↓	t_{CFHA}	T – 50		ns	
$\overline{HLDAK}$ ↑ to control output time	t_{DHAC}	T – 50		ns	
HLDRQ ↓ to control output time	t_{DHQC}	3T + 30		ns	
$\overline{HLDAK}$ width, low	t_{WHAL}	T		ns	
HLDRQ setup time	t_{SHQK}	30		ns	
HLDRQ to $\overline{HLDAK}$ delay time	t_{DHQHA}		3T + 160	ns	
HLDRQ width, low	t_{WHQL}	1.5T		ns	
INTP, DMARQ setup time	t_{STQK}	30		ns	
INTP, DMARQ width, high	t_{WIQH}	8T		ns	
INTP, DMARQ width, low	t_{WIQL}	8T		ns	
$\overline{POLL}$ setup time	t_{SPLK}	30		ns	
NMI width, high	t_{WNIH}	5		μs	
NMI width, low	t_{WNIL}	5		μs	
$\overline{CTS}$ width, low	t_{WCTL}	2T		ns	
INT setup time	t_{SIRK}	30		ns	
INT hold time	t_{HAIQ}	0		ns	
$\overline{INTAK}$ width, low	t_{WIAL}	2T – 30		ns	
$\overline{INTAK}$ delay time	t_{DKIA}		80	ns	

AC Characteristics 3; V35 Mode (cont)

Parameter	Symbol	Min	Max	Unit	Conditions
$\overline{INTAK}$ width, high	t_{WIAH}	T – 30		ns	
$\overline{INTAK}$ to data delay time	t_{DIAD}		2T – 130	ns	
$\overline{INTAK}$ to data hold time	t_{HIAD}	0	0.5T	ns	
$\overline{SCK0}$ cycle time	t_{CYTX}	1000		ns	
$\overline{SCK0}$ (TSCK) width, high	t_{WSTH}	450		ns	
$\overline{SCK0}$ (TSCK) width, low	t_{WSTL}	450		ns	
TxD delay time	t_{DTKD}		210	ns	
TxD hold time	t_{HTKD}	20		ns	
$\overline{CTS0}$ (RSCK) cycle time	t_{CYRK}	1000		ns	
$\overline{CTS0}$ (RSCK) width, high	t_{WSRH}	420		ns	
$\overline{CTS0}$ (RSCK) width, low	t_{WSRL}	420		ns	
RxD setup time	t_{SRDK}	80		ns	
RxD hold time	t_{HKRD}	80		ns	

AC Characteristics 4; EPROM Program Operation

T_A = 25 ±5°C, V_{DD} = 6.0 ±0.25 V; V_{PP} = 12.5 ±0.3 V

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Parameter	Symbol	Min	Typ	Max	Unit	Condition
Address setup time to $\overline{CE}$ ↓	t_{AS}	2			μs	
$\overline{OE}$ setup time	t_{OES}	2			μs	
Data input setup time to $\overline{CE}$ ↓	t_{DS}	2			μs	
Address retention time	t_{AH}	2			μs	
Data input retention time	t_{DH}	2			μs	
$\overline{OE}$ to data output float delay	t_{DF}	0		1	μs	
V_{PP} setup time to $\overline{CE}$ ↓	t_{VPS}	2			μs	
V_{DD} setup time to $\overline{CE}$ ↓	t_{VDS}	2			μs	
Initial program pulse width	t_{PW}	0.95	1.0	1.05	ms	
Additional program pulse width	t_{OPW}	2.85		78.75	ms	
$\overline{OE}$ to data output delay time	t_{OE}			2	μs	

AC Characteristics 5; EPROM Read Operation

T_A = 25 ±5°C, V_{DD} = 5.0 ±0.5 V; V_{PP} = V_{DD}

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Address to data output delay time	t_{ACC}			2	μs	$\overline{CE}$ = $\overline{OE}$ = V_{IL}
$\overline{CE}$ to data output delay time	t_{CE}			2	μs	$\overline{OE}$ = V_{IL}
$\overline{OE}$ to data output delay time	t_{OE}			1	μs	$\overline{CE}$ = V_{IL}
$\overline{OE}$ to data output float delay	t_{DF}	0		1	μs	$\overline{CE}$ = V_{IL}
Address to output retention	t_{OH}	0			μs	$\overline{CE}$ = $\overline{OE}$ = V_{IL}

Figure 4. EPROM Program Operation Timing

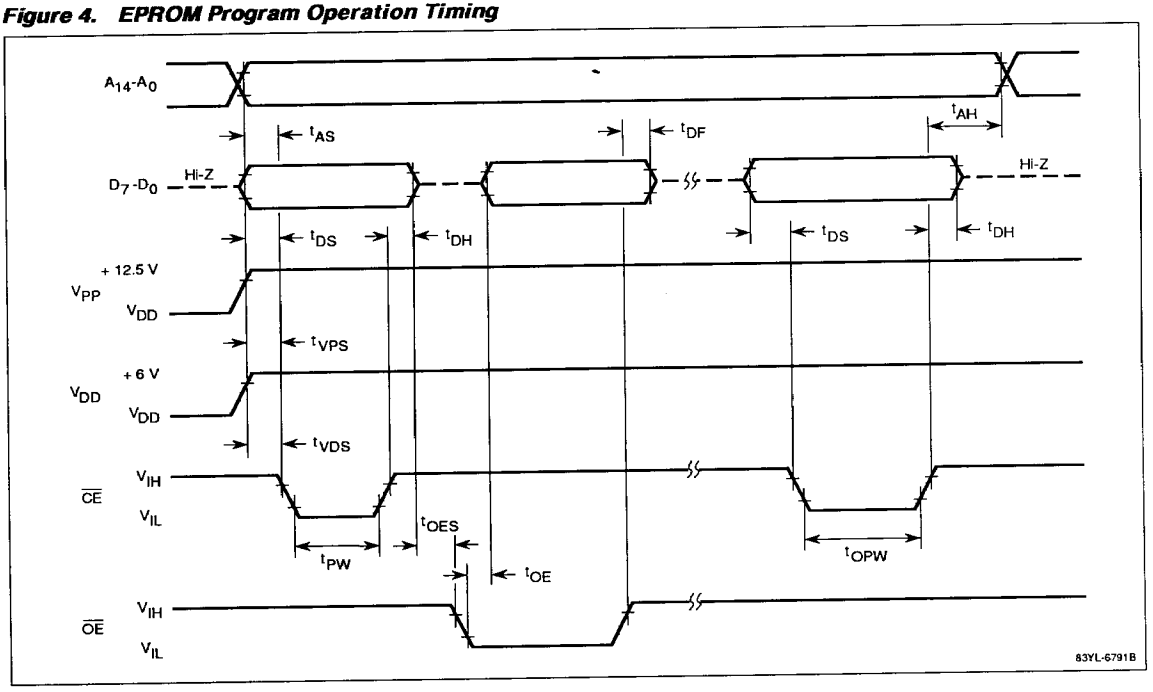
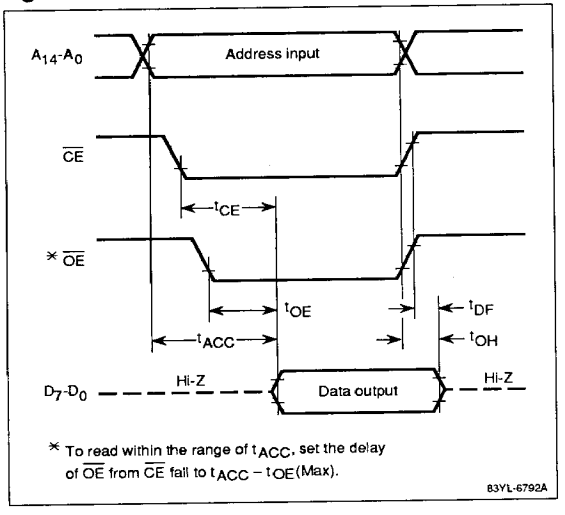


Figure 5. EPROM Read Operation Timing



Comparator Characteristics

T_A = −10 to 70°C; f_{CLK} = 0.5 to 5 MHz with V_{DD} = 5 V ±10%; f_{CLK} = 5 to 8 MHz with V_{DD} = 5 V ±5%

Parameter	Symbol	Min	Max	Unit
Accuracy	VA_{COMP}	–	±100	mV
Threshold voltage	V_{TH}	0	V_{DD}+0.1	V
Comparison time	t_{COMP}	64	65	t_{CYK}
PT input voltage	V_{IPT}	0	V_{DD}	V

Data Memory STOP Mode; Low Supply Voltage Data Retention

T_A = −10 to +70°C

Parameter	Symbol	Min	Max	Unit
Data retention supply voltage	V_{DDDR}	2.5	5.5	V
V_{DD} rise, fall time	t_{RVD}, t_{FVD}	200		μs