CYPRESS SEMICONDUCTOR

PRELIMINARY

CYM7232
CYM7264
DRAM Accelerator Module

Features

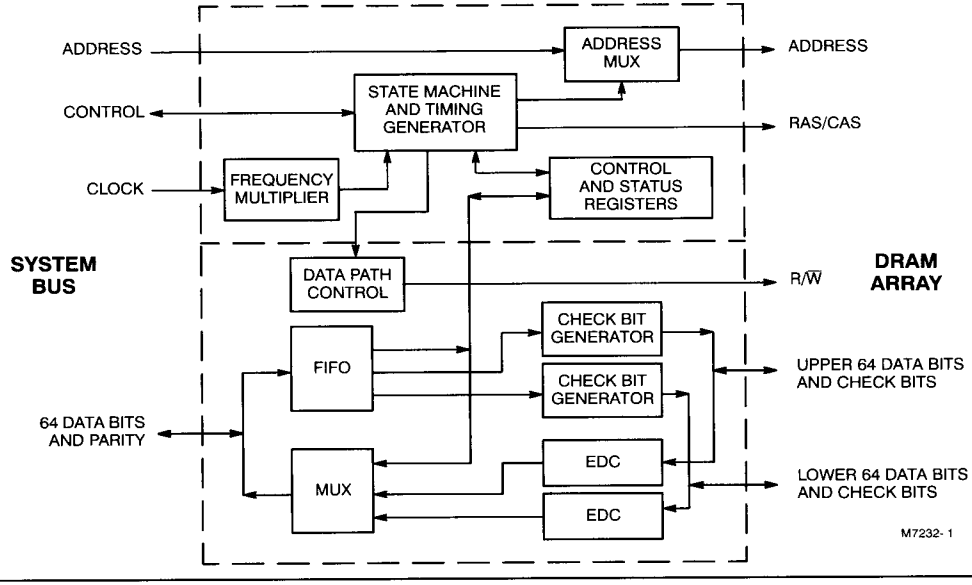
- **4-megabyte to 1-gigabyte control capability**
- **32- or 64-bit bus interface (M7232 only)**
- **32- or 64-bit EDC versions**
  - **— 1-bit correct; 2-bit detect**
- **Multiplexed or non-multiplexed bus**
- **i486, Pentium™, i860, 68040, 88110, Power PC, SPARC, and MIPS compatible**
- **Synchronous bus interface**
- **25-, 33-, and 40-MHz versions**
- **Error-logging facilities**
- **Cache line fill burst support; posted writes**
- **Cache line write-back support; write FIFO**
- **High performance**
  - **— 25-ns writes**
  - **— 175-, 25-, 50-, 25-ns burst read/80-ns DRAMs**
- **Automatic refresh with scrubbing**
- **Multiprocessor compatible**
  - **— Inhibited reads and writes**
  - **— Reflective reads**
  - **— Reads for ownership**
- **Bus parity generation and checking**
- **Very small size**

Functional Description

The CYM7232 and the CYM7264 consist of a full-function DRAM controller and a pipelined/FIFO data multiplexer/demultiplexer with error correction for cache-based, uniprocessor, and multiprocessor systems memory control. The CYM7232 performs 32-bit Error Detection and Correction (EDC) while CYM7264 performs 64-bit EDC. They both connect to the system bus through a 64-bit-wide data bus, and a 36-bit wide address bus. The CYM7232 also supports 32-bit system buses. The bus transfer control signals support i486, Pentium, i860, 68040, 88110, SPARC MBus, MIPS R4000, or other interfaces. The controller module interfaces to the DRAM array through a 16-byte-wide data bus plus check bits, a 12-bit row/column address bus, four $\overline{RAS}$ outputs, four $\overline{CAS}$ outputs, and four read/write control lines.

During write operations, data passes from the system bus through a FIFO array that acts as an incoming queue. Writes occur at the system bus speed until the FIFO is full (sixteen 64-bit words). The FIFO supports cache-line copy-back and fill operations, reducing system bus traffic to a minimum. The module supports posted writes, by suspending the actual write to DRAM until the cache-line read is completed during cache-line write-back. This speeds cache-line fill operations. The module pipelines a 16-byte-wide DRAM access into the data path for EDC, and multiplexes the data to the system bus during reads. This supports high-speed burst line fills with error corrected data. Reads and writes may be inhibited for multiprocessor support. Inhibited reads may be turned into reflective reads, and inhibited writes may be turned into reads-for-ownership.

Logic Block Diagram



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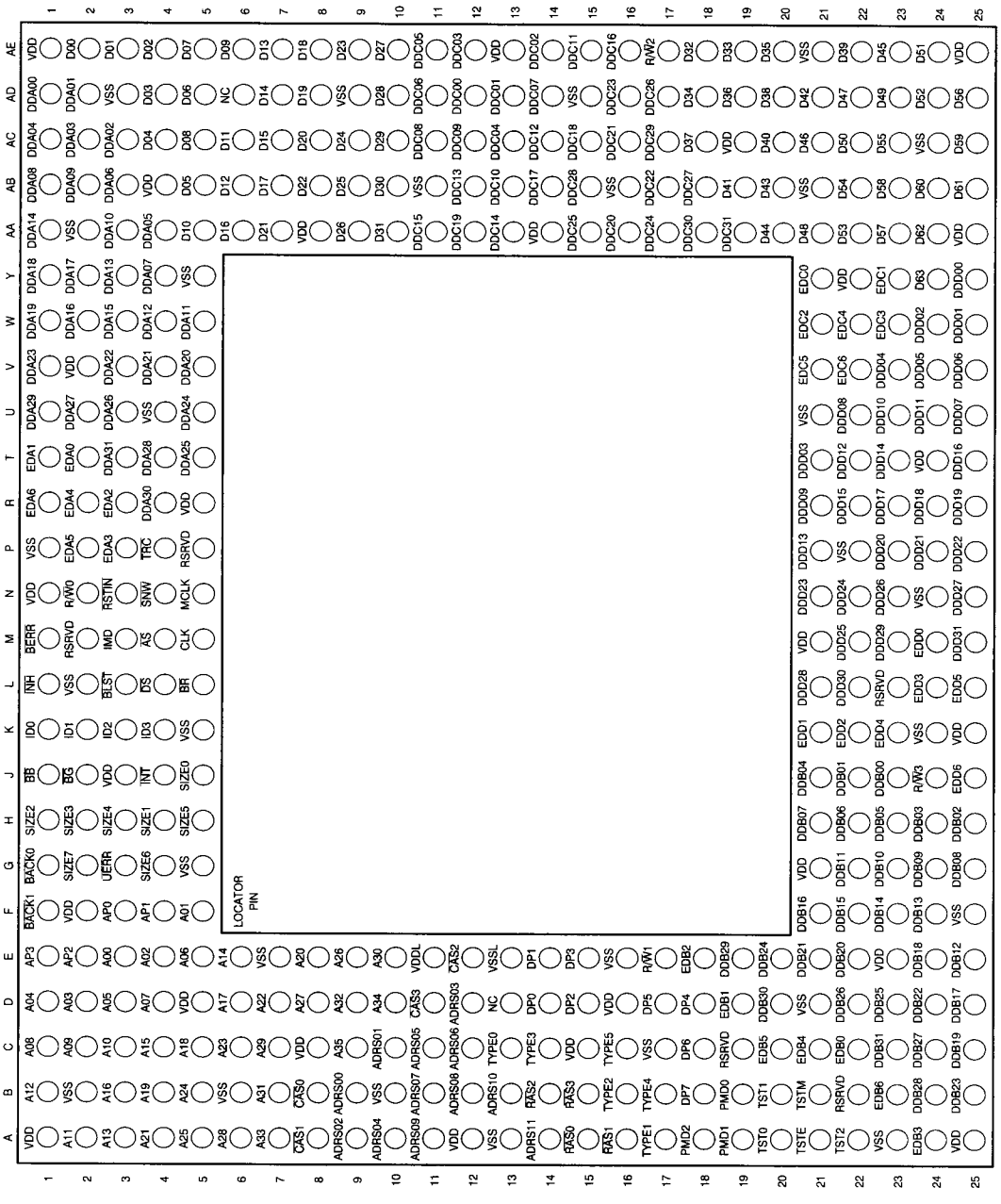
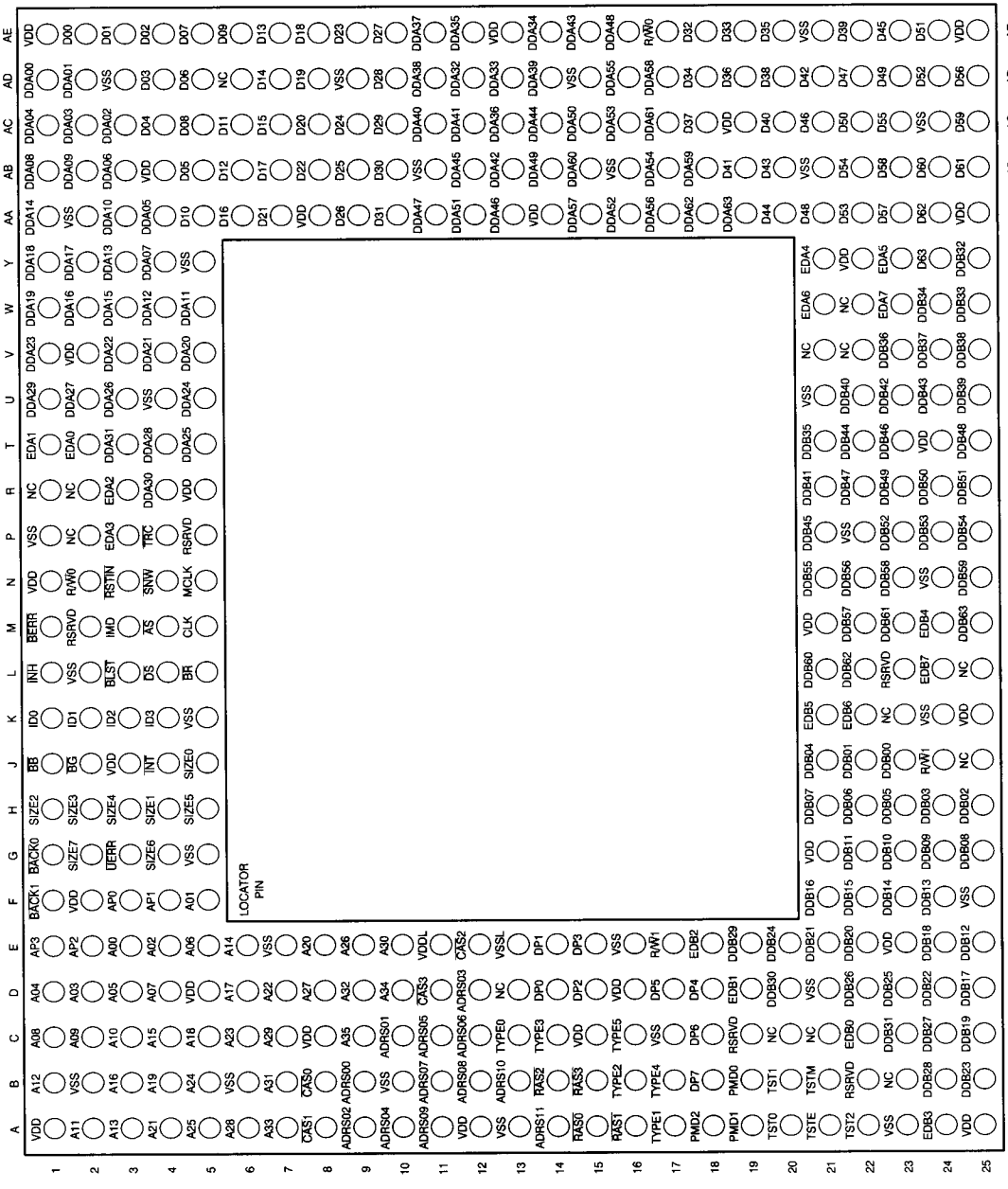
Pin Configuration: CYM7232 Top View



Pin Configuration: CYM7264 Top View



Overview

Cypress Semiconductor offers two DRAM control subsystem module types: the CYM7232, which supports 32-bit EDC, and the CYM7264, which supports 64-bit EDC. The modules are very similar in functionality and architecture, with minor differences to support the EDC variation. Both modules support four blocks of DRAMs for a total capacity of 1 gigabyte of data storage. The CYM7232 divides the memory blocks into four 32-bit-wide data banks, each with 7 check bits, which provide a 156-bit-wide data path to the DRAM array. The CYM7264 divides the memory blocks into two banks of 64-bit-wide data, each with 8 check bits, for a total DRAM interface of 144 bits.

The CYM7232 can be programmed and wired for use with 32-bit system buses, and the operation is very similar to use in 64-bit systems.

The modules support multiplexed address/data buses as well as separate address and data buses for applications such as the SPARC MBus architecture. This datasheet includes a detailed MBus Operation section.

The modules are offered in high-speed and standard speed versions. The high-speed version may be programmed for 100 MHz DRAM timing resolution, while the standard speed version may be programmed for 80-MHz DRAM timing resolution.

System Bus Modes

The modules include selectable bus modes that support a variety of processors and cache controllers. Programmability includes the byte-ordering protocol (big endian/little endian); burst length is configurable for SPARC MBus, 88K or 68040 SIZE, or i86 and i860 byte enables. A data strobe initiates the bus handshake for systems where the bus master must indicate when it can supply or accept data; bus acknowledge signals are programmable to be early (active in the bus cycle preceding the data) or normal (active in the cycle in which the data transfer takes place). The early modes support the Motorola 88K family of microprocessors. Other programmable options allow optimization of the acknowledge timing to the system requirements.

General Description of Bus Transactions

The fully synchronous bus interface uses the rising edge of the system bus clock. Every system transaction has an address/control phase and one or more data phases.

Address Phase

During the address/control phase, which is specified by the assertion of the Address Strobe for one bus clock cycle, the address and nature (size and type) of the transaction is supplied over the system bus to the module.

Data Phase

During the data phase, which is specified by the assertion of the data strobe for one or more bus clock cycles, one or more data words is transferred over the system bus.

Data Write

The module supports four different write modes. Data strobe will be interpreted differently depending on the mode. Data strobe may be permanently asserted, asserted one clock early, or in real-time. Systems using Real-Time Data Strobe mode must monitor the Bus Request/FIFO Empty output and postpone data strobe assertion until the write FIFOs are empty. These systems do not require bus acknowledges since the FIFOs are empty when the data phase begins. The module will not respond with bus acknowledge (real-time data strobe case) or will assert bus acknowledge one cycle before, or during the same cycle, as the data transfer.

Write Data Flow

During system bus writes and reflective read operations, two identical sets of FIFOs buffer the incoming data. One set is used during normal write transactions, and the second set is used exclusively during reflective read transactions. In the CYM7232, each set contains four FIFOs that are 32 bits wide by 8 words deep. In the CYM7264, each set contains two FIFOs that are 64 bits wide by 8 words deep. During writes, the module demultiplexes the incoming data into the appropriate FIFO according to the address and burst order. As soon as the required data falls through the FIFOs, a write to DRAM commences. This process continues until completion of the burst. When the inhibit signal and transform cycle inputs are asserted during a read, the module demultiplexes the write data into the appropriate reflective FIFO. These FIFOs operate in an identical fashion to the normal write FIFOs.

During writes to DRAM, the module appends the demultiplexed data with associated error detection and correction check bits. For the 32-bit EDC version, the demultiplexed data word consists of four sets of 32 data bits plus their 7 associated error check bits for a total of 156 bits. For the 64-bit EDC version, the data word consists of two sets of 64 data bits plus their 8 associated error check bits for a total of 144 bits.

Data Phase Read

During read operations the module suspends data transfer until two clocks after the assertion of data strobe and the closing of the snoop window, whichever occurs last. The data transfer continues at the system bus speed. In systems where the master does not regulate the data flow, data strobe may be permanently asserted.

The module offers options for both early and real-time bus acknowledge for reads. At fast system bus clocks, wait states may be inserted to delay the bus acknowledge, allowing the data to propagate through the error-detection and correction logic.

Read Data Flow

The module reads 128 bits of data and the corresponding EDC check bits in parallel from the DRAM. The data then passes simultaneously through parallel error correction circuitry to a multiplexer that selects the corrected or uncorrected data. The module appends parity to the data and routes it to the system bus. The CYM7232 transfers the data in 32-bit packets, and the CYM7264 transfers 64-bit packets, which makes the CYM7264 incompatible with 32-bit system buses.

Burst Last

The module allows any read or write burst transaction to terminate prematurely with the assertion of Burst last.

Data Alignment

The data path portion of the module contains data buffers and demultiplexers on writes and multiplexers and error correctors on reads. The bus interface is 64 data bits wide and the DRAM interface is 128 data bits wide.

Bus Alignment

All data flowing between the DRAM controller and the system data bus is assumed to be aligned to the bus width. When a system bus transaction crosses aligned boundaries, the processor or cache controller must split the transaction into multiple operations and issue an address phase for each portion. The misaligned transactions cannot, therefore, be bursts.

DRAM Alignment

The DRAM controller stores data into memory on 128-bit aligned boundaries. Transactions over the system bus of 16 bytes or less are assumed to be aligned within a 128-bit DRAM page. This implies that a single DRAM transaction will be associated with bus transactions of 16 bytes or less. Burst transactions exceeding 16 bytes may be misaligned to the DRAM storage boundary. Such transactions will involve transfers of 4, 8, or 12 bytes between controller and DRAM during the first cycle of the burst (i.e., not all DRAM banks will be involved in the first data transfer). The DRAM address will wrap around within the burst boundary as more data is transferred. The final data transfer will include the bank(s) omitted during the first cycle of the DRAM transfer. The nature of the misalignment will depend on the defined burst order (i.e., sequential or Intel).

I/O Operations

The internal command and status registers are accessed through I/O transactions. The ID inputs select between Memory, I/O transactions, or the Indirect Address register. The Indirect Address register points to the desired command and status I/O registers. I/O read and write transactions follow the same bus acknowledge and data strobe protocols as memory operations.

I/O operations may be inhibited prior to the closure of the snoop window.

Multiprocessor Support

The modules provide complete multiprocessing support. Any operation may be inhibited or aborted, including I/O operations.

Reflective Read Operations

A reflective read transaction occurs when a main memory read operation is inhibited and transformed into a write. Such transactions can occur in a multiprocessor environment when a processor's cache controller requests a line from main memory. The particular main memory line may be stale with the only valid copy contained in another processor's snooping cache. The cache line owner will inhibit the main memory, and then fetch and supply the data to the requesting processor's cache. Simultaneously, the data is copied into FIFO buffers inside the controller module for later transfer to DRAM. The memory read operation is thereby transformed into a memory write operation.

Reads For Ownership

The address space of a copy-back cache-based system will typically be partitioned into distinct regions. Some of these regions will be cachable and others (typically peripheral I/O registers and some small portion of memory) will not be cachable. Whenever a processor begins a write operation to a particular address location, the cachability status of that location must be determined. Should the write operation result in a miss within a cachable region of main memory, a line would be fetched. The DRAM controller module permits a write to begin into DRAM before the cachability status is completely determined. When the status of the address in question is resolved the operation can be inhibited and transformed into a read of a cache line.

Write Operations

Address Phase

A write operation is initiated when Address Strobe ($\overline{AS}$) is asserted and an address and all appropriate control signals meet the set-up conditions to the rising edge of CLK. This is the address phase of the transaction. The control signals that accompany the address during the address phase include SIZE and TYPE inputs. The address and certain control information is strobed into the Address-Control register in the cycle in which $\overline{AS}$ is asserted. If address parity check is enabled, the lowest 32 bits of the system bus address is checked for byte parity. The control signals are not parity checked. If parity is error-free, the address and other control information is used to initiate the requested transaction. If address parity is enabled and an address bus parity error is detected, the Address Bus Parity Error (ABE) bit is set in the status register, the Bus Error ($\overline{BERR}$) output is asserted, and the write operation is aborted. This action takes place whether or not the address is decoded to address the DRAM controller.

Data Phase

Data placed on the bus is clocked into the Write Data FIFO on a rising CLK edge. The system will use $\overline{DS}$ (Data Strobe) to signal the onset of a write transaction. Once $\overline{DS}$ is asserted, it must remain asserted throughout the bus operation. The system must continue to assert the write data until it is acknowledged (except in the no acknowledge mode). If the SIZE[7:0] control indicated a non-burst transfer, the write transaction is terminated upon the acceptance of the data. When SIZE[7:0] control inputs indicate a burst transaction, the module will continue the write transaction by accepting data until the transaction is terminated. The transaction is terminated by one or more of the following events: the bus responds by asserting Burst Last ($\overline{BLST}$) or the burst length indicated by SIZE or the programmed default burst length is reached.

During the data phase, data is checked for valid parity (if data parity checking is enabled). Parity is checked over individual bytes. Should a data bus parity error occur, data is clocked into the Write Data FIFO (but is later discarded) and the Bus Error output ($\overline{BERR}$) is asserted. After parity check, data flows into the Write Data FIFO and is subsequently written into the DRAM memory. When a parity error occurs, the entire word that would have been written to DRAM with the byte(s) incurring the parity error is discarded. The discarded word consists of bits over which the EDC algorithm is applied. It is therefore 32 (CYM7232) or 64 (CYM7264) bits in length. Recovery schemes must consequently rewrite more than the byte(s) incurring the parity error. Subsequent data transferred to the FIFO is written to DRAM even though a previous data word may have incurred a parity error.

Burst operations are supported up to the full FIFO depth. The FIFO permits these operations to take place at the full bus speed. If the Write Data FIFO contains data from a previous write (FIFO not Empty), the address and control information is accepted into the controller's internal Write Address register, but the data phase cannot begin until the previous write is completed to DRAM. $\overline{BACK}$ remains three-state until the FIFO is available for the new write. The system must use the Bus Request/FIFO Empty ($\overline{BR}/\overline{FE}$) output to determine if the controller is capable of accepting data when using the No Bus Acknowledge Mode.

Posted Writes

Posted writes support fast cache line fills. A posted write is accomplished by issuing the Posted Write encoding in the TYPE input during the address phase. The module accepts the write data as usual and holds the data in the Write Data FIFO. After the next read transaction is completed, the actual write of the data to DRAM is accomplished. The posted write operation allows a cache controller to purge a cache line and fetch the new cache line as rapidly as possible by postponing the DRAM access for the write. Posted writes must be followed by a read operation.

When the address of the posted write is in the same burst address region as that of the following read, a memory incoherency can result. To resolve the incoherency, the module compares the

Posted Writes (continued)

address of the posted write with that of the read for address bits A7 and higher. (A[6:0] span the longest possible burst). If the compare shows equal, the posted write is performed before the read. Posted writes may not be inhibited.

Byte Writes

Single byte and partial word transfers are supported by a read-modify-write DRAM memory cycle. The old word is accessed and combined with the new data under control of the address and SIZE inputs. A new set of EDC check bits is generated and the modified data and new check bits are written back to the memory to complete the read-modify-write cycle. In the 32-bit EDC version, a read-modify-write cycle occurs for all writes less than 32 bits. In the 64-bit EDC version, a read-modify-write cycle occurs for all writes less than 64 bits.

Inhibited Write Operations

A write operation may be inhibited at any time prior to the end of the snoop window by asserting Inhibit, $\overline{INH}$. When Inhibit is recognized, the module write operation is aborted and the module plays no further role in the bus transaction. Note that the system may perform data writes to the controller prior to the close of the snoop window and prior to the assertion of Inhibit. In these cases, the data will not be written to the DRAM and the write FIFO will be cleared upon recognition of the Inhibit. When data transfers occur prior to a write inhibit there must be at least two bus clock cycles between the close of the snoop window and the address strobe of the following transaction.

An inhibited write may also be converted into a read for ownership. This option is enabled by asserting the $\overline{TRC}$ input (Transform Cycle) along with the Inhibit. When Inhibit is recognized, the module write operation is transformed into a read operation. After Inhibit is recognized and before the read is completed, any data written to the Write FIFO is purged.

Write Snoop Window

The snoop window is determined by an internal counter that is programmable by the system or by an external input, $\overline{SNW}$. The snoop window source is selectable by driving $\overline{UERR}$ as an input when $\overline{RSTIN}$ is asserted. Refer to the signal descriptions for programming details. The write into the DRAM is postponed until the snoop window closes. This prevents data from an inhibited write operation from corrupting main memory data. Long snoop window intervals may cause performance degradation.

Read Operations

Address Phase

A read operation begins with the address phase similar to write operations.

Data Phase

The DRAM interface accesses 128 data bits from the memory simultaneously with their related check bits. The addressed 64-bit word (or the first word of the burst) is pipelined to the system bus and simultaneously to the error check logic. The data is accessed from DRAM but the transfer over the system bus is suspended until two clock cycles after the snoop window closes or two clock cycles after Data Strobe is asserted, whichever occurs last. The appropriate Bus Acknowledge is asserted as dictated by the selected modes. Byte-wide parity is appended to the data as it exits the module onto the system bus.

During bursts, data is pipelined consecutively over the bus until the transaction is terminated. Transactions may be terminated by Burst Last ($\overline{BLST}$) or when the burst length indicated by SIZE or the default burst length is reached.

The error detection logic generates check bits that are compared with the check bits from the memory. The exclusive NOR of the generated check bits and the check bits from the memory form the syndrome bits. When the two sets of check bits are identical, no errors have occurred in the data. Should the comparison show a difference, the Error Detector decodes the syndrome bits, identifying the type of error (single-bit correctable, double-bit detectable, or uncorrectable multi-bit error). The Error Position Decoder creates a 32-bit word that is used to correct the defective bit for single-bit errors.

Should the data contain an error, the appropriate status bits are set in the Interrupt Status register. An interrupt is generated when enabled. Whenever an error occurs, the syndrome bits are saved in the Syndrome FIFO allowing the syndrome to be read by the system. This output can be used to determine which bit was defective. The corrected data is not written back into the memory array but is corrected later as part of the refresh/scrubbing operations.

Inhibited Read Operations

Read operations may be inhibited. This action is required in multiprocessor systems when a main memory read must be terminated to allow a snooping cache to supply data to the requesting cache. A read operation may be inhibited prior to the close of the snoop window by asserting $\overline{INH}$. When an Inhibit is recognized, the module read operation is aborted and the module plays no further role in the bus transaction.

Reflective Reads

Inhibited reads may also be reflective. This option is enabled by asserting Transform Cycle ($\overline{TRC}$) simultaneously with $\overline{INH}$. When a transformed Inhibit is recognized, the module read operation is changed into a write operation. $\overline{INH}$ and $\overline{TRC}$ must be asserted within the snoop window. After Inhibit is recognized, $\overline{BACK}$ and the Data Bus become inputs. $\overline{BACK}$ are now used as a synchronous write enable to strobe the bus data into the Reflective Read FIFO. As the slave in the transaction, the snooping cache must supply $\overline{BACK}$. The timing of the $\overline{BACK}$ input to strobe data into the reflective FIFO is either early or real-time following the Bus Acknowledge mode selection for reads.

The Reflective FIFO is an image of the normal Write Data FIFO and is devoted exclusively to reflective read operations. Upon inhibit, the data bus is kept three-stated, allowing the snooping cache to drive the bus with the requested data. The module accepts the data into the Reflective Read FIFO at the full bus speed. A mechanism is required to prevent overrun of the reflective FIFO during consecutive transformed reads. As soon as the Inhibit is recognized, the module asserts Bus Request ($\overline{BR}$) in order to become the bus master in the next address phase. The system responds with Bus Grant ($\overline{BG}$). When the bus is acquired, the module asserts Bus Busy ($\overline{BB}$) until the reflective FIFO data is written to the DRAM and the module is capable of accepting another read. Since $\overline{BR}$ provides status of the availability of the reflective FIFO, the output may be used to delay the address phase of the next operation.

Read Snoop Window

As with writes, the snoop window may originate from either of two sources, one internal and the other external. On reads, the assertion of the bus acknowledge to transfer the data to the system is postponed until at least two clocks after the snoop window closes.

I/O Operations

Access to the internal Command and Status registers is controlled by the ID input. The details of the ID control are given in the Pin Description section. When the ID code for memory is input, all transactions access DRAM. The ID input can also point to the Indirect Address register. When the ID input specifies an I/O register, the Command and Status register accessed is the one pointed to by the Indirect Address register. The register address, position on the system bus, and the bit definition for each of the Command and Status registers is given in the Internal Registers section.

I/O register access follows the same Data Strobe and Bus Acknowledge modes as invoked for memory transactions with a few exceptions. In the Real-Time Data Strobe mode for writes, the $\overline{BR/FE}$ output plays no role and the transaction is acknowledged with the controller asserting $\overline{BACK}$. In all writes, system bus data must be valid at least one clock cycle before it is accepted. The controller delays $\overline{BACK}$ to meet this criterion. In all reads, data is always transferred in the second clock cycle after the snoop window closes or Data Strobe is asserted, whichever occurs last.

I/O operations may be inhibited. The duration of the I/O snoop window may be set externally or internally as in reads.

Write Bus Acknowledge and Data Strobe Modes

There are four modes of bus handshake: Early Data Strobe/Early Bus Acknowledge, Real-Time Data Strobe, Early Data Strobe/Real-Time Bus Acknowledge, and MBus. These modes are invoked by driving the $\overline{BACK}$ and $\overline{UERR}$ pins during Reset with a specific pattern. *Table 1* is a summary of the modes and their operation.

Early Data Strobe / Early Bus Acknowledge Mode

Data Strobe may be asserted at any time during or after the address phase. In *Table 1*, the cycle in which Data Strobe is asserted is designated cycle N. Data Strobe, once asserted, must remain asserted throughout the transaction. The FIFO may not be empty when the system asserts Data Strobe. If the FIFO goes empty in cycle N + k, the controller will assert Bus Acknowledge ($\overline{BACK}$) in the cycle following the one in which the FIFO goes empty (N + k + 1). The controller accepts the write data in the cycle following the one in which it asserted Bus Acknowledge (cycle N + k + 2). If the FIFO is empty when the Data Strobe is asserted, then k = 0. The controller would then assert Bus Acknowledge in the cycle following the one in which Data Strobe was asserted (cycle N + 1). Data is accepted in the following cycle (N + 2). If the transfer is a burst, Bus Acknowledge continues to be asserted until one cycle before the last data transfer.

Real-Time Data Strobe Mode

Writes are performed by programming the $\overline{BR/FE}$ output to include the status of the write data FIFO. The system may begin the write transaction with the address phase, but may not assert Data Strobe until the FIFO is known to be empty. In *Table 1*, the controller asserts $\overline{BR/FE}$ in cycle N. The system responds with Data Strobe in cycle N + k (k greater than or equal to 1) and the controller accepts the data in the same cycle. If the transaction is a burst, data is accepted each clock cycle thereafter until the burst is terminated. Data Strobe, once asserted, must remain asserted throughout the transaction.

Early Data Strobe/Real-Time Bus Acknowledge Mode

Data is accepted one clock cycle after Data Strobe is asserted in this mode. Bus Acknowledge is asserted in the same cycle in which the data is accepted (real-time Bus Acknowledge). Referring to *Table 1*, the system asserts Data Strobe in cycle N. The FIFO goes empty in cycle N + k. If the FIFO is already empty, k is 0. The controller asserts Bus Acknowledge and accepts the data in the next cycle (N + k + 1).

Table 1. Write Bus Acknowledge and Data Strobe Modes

Mode	Write Action	Write Cycle
Early $\overline{DS}$ Early $\overline{BACK}$	System asserts $\overline{DS}$	N
	Cntrlr FIFO goes empty	N+k, (k ≥ 0)
	Cntrlr asserts $\overline{BACK}$	N+k+1
	Cntrlr accepts DATA	N+k+2
Real-Time $\overline{DS}$, No $\overline{BACK}$	Cntrlr asserts $\overline{BR/FE}$	N
	Systems asserts $\overline{DS}$, Cntrlr accepts DATA	N+k (k ≥ 1)
Early $\overline{DS}$, Real-Time $\overline{BACK}$	System asserts $\overline{DS}$	N
	Cntrlr FIFO goes empty	N+k (k ≥ 0)
	Cntrlr asserts $\overline{BACK}$, Cntrlr accepts DATA	N+k+1
MBus, $\overline{DS}$ Gnded	System asserts AS	N
	Cntrlr FIFO goes empty	N+k (k ≥ 0)
	Cntrlr asserts $\overline{BACK}$ Cntrlr accepts DATA	N+k+1

MBus Mode

Data Strobe is permanently asserted in MBus mode. The controller operates as if it were in Early Data Strobe mode. The system asserts Address Strobe in cycle 0. The FIFO goes empty in cycle k. If the FIFO is already empty, k is 0. The controller asserts Bus Acknowledge and accepts the data in the next cycle (k + 1).

Read Operating Modes

The module offers several programmable options to control the data transfer during memory-read operations. Wait states may be inserted to allow additional propagation delay through the EDC path. Error correction can be disabled for diagnostic purposes. As in write operations, Data Strobe may be used to regulate transfers over the system interface. Finally, Bus Acknowledges may be programmed to occur one clock early or in real time with respect to the corresponding data transfer. The timing of the Bus Acknowledges is shown in *Figure 1*.

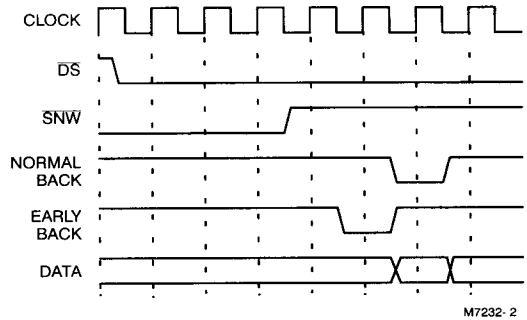


Figure 1. Early and Normal Bus Acknowledge Modes for Reads

Read Early BACK Mode

The Read Early BACK data transfer is triggered by the assertion of Data Strobe and closure of the snoop window (whichever occurs last) in cycle N. Data Strobe, once asserted, must remain asserted throughout the transaction. When read data is about to become available, $\overline{BACK}$[1] is asserted (cycle N + k). Read data is supplied to the bus in cycle N + k + 1.

Read Real-Time BACK Mode

The Read Real-Time BACK Mode begins when both Data Strobe is asserted and the snoop window is closed (cycle N). The controller responds with data and the corresponding Bus Acknowledge in cycle N + k + 2.

Wait States

The controller module may be programmed to insert wait states in the data path. This guarantees extra data set-up time when using error correction in system environments with fast bus clocks. The controller delays the Bus Acknowledges accordingly. Wait states may be inserted in either early or real-time Bus Acknowledge systems.

Acknowledge on Burst Reads

Read burst acknowledges will not generally be contiguous. The assertion of the acknowledge on long bursts (above 16 bytes) will be interrupted as more data is fetched from adjacent 128-bit DRAM pages. During a burst pause, the acknowledge is deasserted and then three-stated one-half clock later.

Bus Acknowledges in Transformed Transactions

When a read is transformed, the operation internal to the controller becomes a write. Bus Acknowledge becomes an input and is used as a strobe to clock the data into the reflective FIFO on each data transfer. The controller will treat the strobe derived from the incoming bus acknowledge as an early strobe when programmed in the early bus acknowledge mode. Otherwise the controller assumes that the data is aligned with the corresponding strobe derived from the incoming bus acknowledge.

When a write is transformed, the operation converts to a read. In this case, the controller behaves according to the invoked read mode. Transformed operations use a preprogrammed default burst length to specify their burst duration.

Bus Acknowledge Timing Characteristics

The Bus Acknowledge control signals are bidirectional and may be driven by the controller or another device on the system bus. Therefore there are times when no device will be driving this signal line. At high bus speeds, pull-ups may not be sufficient to guarantee that the Bus Acknowledge line will revert in a sufficiently short time to the deasserted state after the controller has ceased driving the line. To guarantee the state of the $\overline{BACK}$ signal lines at the end of a transaction, the controller first drives the outputs HIGH (deasserted) in the first half of the clock cycle in which Bus Acknowledge is to be deasserted and then three-states these outputs in the second half of this clock cycle. To insure that the Bus Acknowledge signal lines remain in the deasserted state when no device is driving them for long periods, pull-ups should be employed. At the beginning of a transaction cycle, Bus Acknowledge remains three-stated until it is to be asserted. Thus in the first acknowledge cycle of a transaction, $\overline{BACK}$ becomes driven and asserted at the same time. $\overline{BACK}$ continues to be driven until the end of the transaction cycle and terminates as described above.

Burst Last

Any read or write burst transaction may be terminated prematurely with the assertion of $\overline{BLST}$. $\overline{BLST}$ must be asserted during the clock cycle in which the last piece of data is transferred. Systems that require the data bus to go three-state in the next cycle must also deassert Data Strobe ($\overline{DS}$) when asserting $\overline{BLST}$. Burst last may not be used in Early Back mode or to prematurely terminate a transformed operation.

Inhibits and Snoop Window

Certain constraints apply to the system's assertion of inhibits and the closing of the snoop window.

The inhibit signal must not be asserted until at least two clocks after the address phase (i.e., if $\overline{AS}$ is asserted in bus clock N, inhibit may not be asserted until N + 2 or later).

Table 2. Read Bus Acknowledge Modes

Mode	Read Action	Read Cycle
Early BACK no wait states	System asserts DS and closes SNW by cycle N	N
	Cntrlr asserts BACK	N + k ($k \geq 2$)
	Cntrlr supplies data	N + k + 1
Early BACK with wait states	System asserts DS and closes SNW by cycle N	N
	Cntrlr asserts BACK	N + k + 1 ($k \geq 2$)
	Cntrlr supplies data	N + k + 2
Real Time BACK no wait states	System asserts DS and closes SNW by cycle N	N
	Cntrlr asserts BACK and supplies data	N + k ($k \geq 2$)
Real Time BACK with wait states	System asserts DS and closes SNW by cycle N	N
	Cntrlr asserts BACK and supplies data	N + k + 1 ($k \geq 2$)

Inhibits and Snoop Window (continued)

There must be a minimum of one bus clock cycle between the close of a transaction's snoop window and the address strobe of the next transaction (i.e., if the snoop window is deasserted on the system bus during bus clock N, the next transaction's address strobe must not be asserted until N + 2). This scenario would most likely occur when the first transaction is inhibited but not transformed.

DRAM Interface

The DRAM array is 128 data bits wide. This data is subdivided into banks: 4 banks of 32 bits each for the 32-bit EDC version and two banks of 64 bits each for the 64-bit EDC version. Each bank includes the associated error check bits: 7 bits for the 32-bit EDC version and 8 bits for the 64-bit EDC version. The DRAM array is divided in depth into blocks. Each block may be populated with different DRAM chip sizes, however, all DRAM chips in a given block must have the same depth. From one to four blocks may be populated with DRAM, however there are certain restrictions as given in other sections.

The DRAM interface consists of a bidirectional data bus for each DRAM bank, plus a bidirectional bus for the associated error detection and correction check bits. There is also a set of bank-associated write/read control outputs. The DRAM blocks are controlled by separate $\overline{RAS}$ and $\overline{CAS}$ control outputs. There is one $\overline{RAS}$ and one $\overline{CAS}$ for each block. The entire DRAM array is addressed through one set of 12 row/column multiplexed address lines. The row/column partition is dictated by the DRAM that populates a particular block.

Latch Requirements

Transparent latches are required between the R/W signals issued by the controller module and the DRAM. These latches guarantee that the R/W signals to the DRAM are stable while CAS is asserted. The latch is transparent when CAS is HIGH and closed when CAS is LOW. The latches can also be used to buffer R/W lines to the DRAM. A 74ABT373 or equivalent is recommended.

There are two alternatives for the latches:

1. One quad latch is devoted to each DRAM block. Each quad latch is enabled by the CAS for that block. R/W[3:0] is connected to the four inputs of the quad latch and the outputs of the quad latch are connected to the R/W inputs of the appropriate DRAM bank in that block. Refer to part (a) in *Figure 2*.
2. One quad latch is devoted to all of the DRAM blocks. the quad latch is enabled by the logical OR of CAS[3:0]. R/W[3:0] is connected to the four inputs of the quad latch and the outputs of the quad latch are connected to the R/W inputs of the appropriate DRAM bank for all of the blocks. Refer to part (b) in *Figure 2*.

DRAM Interface for the 32-Bit EDC

The controller supports an organization of DRAM that is 156 bits wide (four banks each consisting of 32 bits of data plus 7 error check bits) and up to four blocks deep. Each block is controlled by separate $\overline{RAS}$ and $\overline{CAS}$ signals ($\overline{RAS}$[3:0], $\overline{CAS}$[3:0]). Each Bank is controlled by separate read/write signals (R/$\overline{W}$[3:0]). The DRAM address outputs from the controller module consists of a 12-bit row/column multiplexed bus. This bus is intended to drive a symmetrical set of address driver devices, which in turn drive the DRAM array address lines. Timing for the $\overline{RAS}$ and $\overline{CAS}$ outputs as well as other DRAM related timing is programmable. A representation of the DRAM organization is shown in *Figure 3*.

Each square in *Figure 3* represents a bank of memory that is 32 data bits wide plus 7 check bits. A block is a column of four banks totalling 128 data bits wide plus 28 check bits. Each block is controlled by dedicated $\overline{RAS}$ and $\overline{CAS}$ signals. With 12 multiplexed row/column address lines, each bank can be up to 16 megabits deep. The row/column address multiplexing is programmable. The controller supports 256K-, 1M-, 4M-, and 16M-deep DRAMs.

DRAM Interface for the 64-Bit EDC

This controller supports an organization of DRAM that is 144 bits wide (two banks each consisting of 64 bits of data plus 8 error check bits) and up to four blocks deep. Each block is controlled by separate $\overline{RAS}$ and $\overline{CAS}$ signals ($\overline{RAS}$[3:0], $\overline{CAS}$[3:0]). Each bank is controlled by separate read/write signals (R/$\overline{W}$[1:0]). Address outputs, $\overline{RAS}$ and $\overline{CAS}$ outputs and DRAM timing is identical to that in the 32-bit EDC version. A representation of the DRAM organization is shown in *Figure 4*.

Each square in *Figure 4* represents a bank of memory that is 64 data bits wide plus 8 check bits. A block is a column of two banks totaling 128 data bits wide plus 16 check bits. Each block is controlled by dedicated $\overline{RAS}$ and $\overline{CAS}$ signals. With 12 multiplexed row/column address lines, each bank can be up to 16 megabits deep. As in the 32-bit EDC version, the row/column address multiplexing is programmable. The controller supports 256K-, 1M-, 4M-, and 16M-deep DRAMs.

DRAM Block Placement

There are four physical DRAM blocks. Each block may be populated with an array of DRAMs that are 128 bits wide by 256K, 1M, 4M, or 16M deep. Physical block population need not be contiguous.

An array of five registers are used to specify the DRAM configuration. At power-up, the controller module is programmed with the Base address (the starting address of the entire memory array) and the Logical Block Displacement and Population (the address gap between logical blocks and their respective DRAM sizes). Finally, the physical/logical mapping is assigned and each block's RAS/CAS address split point is specified.

During operation, an incoming memory address is evaluated. Once the controller determines that this address is valid, the appropriate RAS signal for the selected block is asserted. The controller will remain inactive if the comparison is invalid. Refer to the register description for programming details.

DRAM Interface Signals

CYM7232 – 32-bit EDC

The module interface to the DRAM array is made through the signals described below.

DDA[31:0] – Data Bus (Bank 0). DDA[31:0] forms a 32-bit data bus that is connected to bank 0 in every populated block.

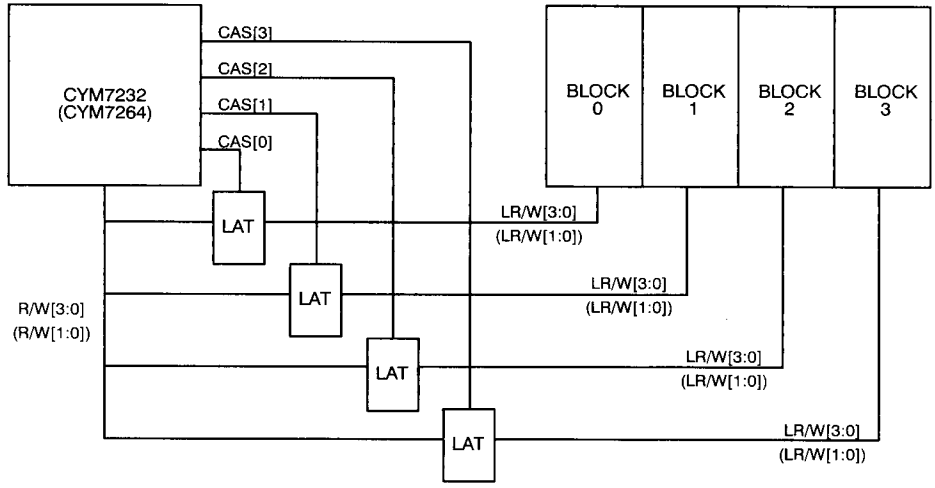
DDB[31:0] – Data Bus (Bank 1). DDB[31:0] forms a 32-bit data bus that is connected to bank 1 in every populated block.

DDC[31:0] – Data Bus (Bank 2). DDC[31:0] forms a 32-bit data bus that is connected to bank 2 in every populated block.

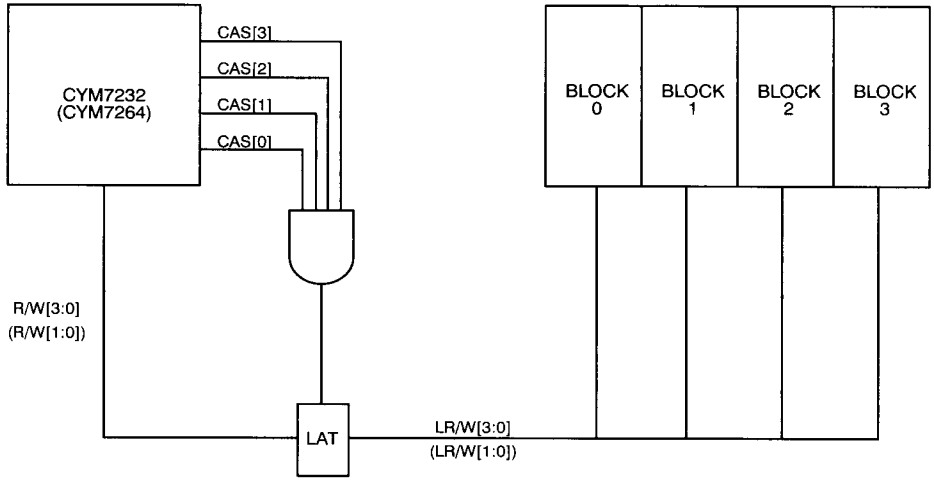
DDD[31:0] – Data Bus (Bank 3). DDD[31:0] forms a 32-bit data bus that is connected to bank 3 in every populated block.

EDA[6:0] – Check Bus (Bank 0). EDA[6:0] forms a 7-bit error check bit bus that is associated with the data on DDA[31:0].

EDB[6:0] – Check Bus (Bank 1). EDB[6:0] forms a 7-bit error check bit bus that is associated with the data on DDB[31:0].



(a)



(b)

Figure 2. R/W Latch Configurations

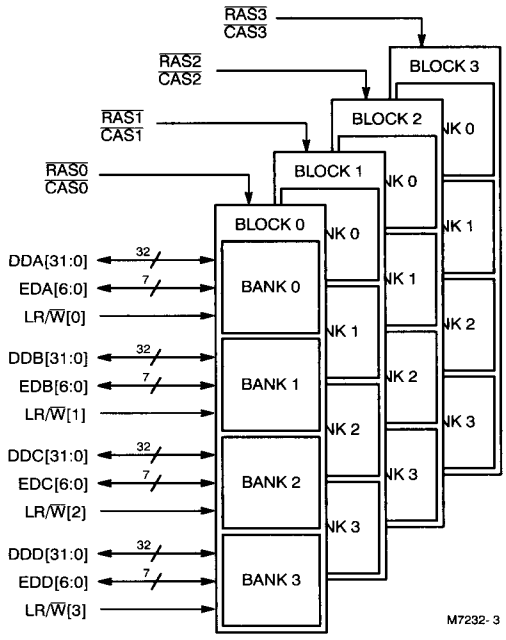


Figure 3. DRAM Configuration for the CYM7232

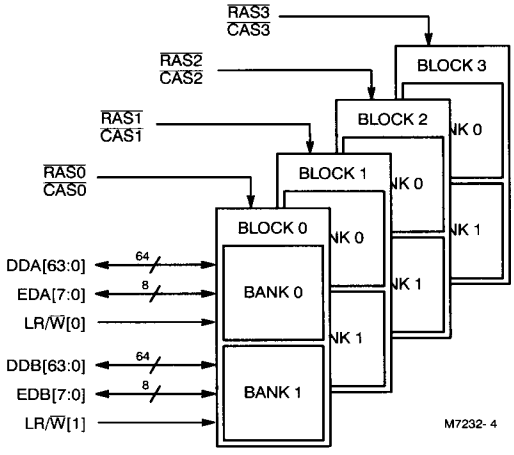


Figure 4. DRAM Configuration for the CYM7264

CYM7232 – 32-bit EDC (continued)

EDC[6:0] – Check Bus (Bank 2). EDC[6:0] forms a 7-bit error check bit bus that is associated with the data on DDC[31:0].

EDD[6:0] – Check Bus (Bank 3). EDD[6:0] forms a 7-bit error check bit bus that is associated with the data on DDD[31:0].

ADRS[11:0] – Address Bus. ADRS is a 12-bit row/column multiplexed address bus that supplies the address to the DRAM to access the proper 128-bit data word. The multiplexing is programmable for different depths of DRAM.

R/$\overline{W}$[3:0] – Read/Write Control. R/$\overline{W}$[3:0] are the read/write controls for the four banks of the DRAM array. R/$\overline{W}$0 controls read/write for all blocks of DDA[31:0], R/$\overline{W}$1 controls read/write for all blocks of DDB[31:0], R/$\overline{W}$2 controls read/write for all blocks of DDC[31:0], and R/$\overline{W}$3 controls read/write for all blocks of DDD[31:0].

$\overline{RAS}$[3:0] – These signals are the four $\overline{RAS}$ outputs to control each block of the DRAM.

$\overline{CAS}$[3:0] – These signals are the four $\overline{CAS}$ outputs to control each block of the DRAM.

The address bus, ADRS[11:0], RAS[3:0], CAS[3:0] should be connected through a set of drivers to the appropriate DRAM inputs. R/$\overline{W}$[3:0] should be connected through a set of latches, gated by the appropriate CAS to the DRAM R/W controls. The driver configuration is dependent upon the capacitance that must be driven.

The data bus, check bus, and read/write control signals are connected across the DRAM array. DDA[31:0] and EDA[6:0] are connected to the data I/O of all the Bank 0 DRAMs. The Bank 0 DRAMs are the top row of DRAMs in *Figure 3*. LR/$\overline{W}$0 is connected to the Write Control input of all the Bank 0 DRAMs. DDB[31:0] and EDB[6:0] are connected to the data I/O of all the Bank 1 DRAMs. The bank 1 DRAMs are the second row of DRAMs. LR/$\overline{W}$1 is connected to the Write Control input of all the Bank 1 DRAMs. This connection pattern continues with Banks 2 and 3.

$\overline{RAS}$0 and $\overline{CAS}$0 are connected to the $\overline{RAS}$ and $\overline{CAS}$ inputs respectively of all of the DRAMs of Block 0. Block 0 is the left column of DRAMs in the array in *Figure 3*. Note that each block consists of Banks 0 through 3. Similarly, $\overline{RAS}$1 and $\overline{CAS}$1 are connected to the $\overline{RAS}$ and $\overline{CAS}$ inputs respectively of all of the DRAMs of Block 1. This connection pattern continues through Block 3.

CYM7264 – 64-bit EDC

The module interface to the DRAM array is made through the signals described below.

DDA[63:0] – Data Bus (Bank 0). DDA[63:0] forms a 64-bit data bus that is connected to bank 0 in every populated block.

DDB[63:0] – Data Bus (Bank 1). DDB[63:0] forms a 64-bit data bus that is connected to bank 1 in every populated block.

EDA[7:0] – Check Bus (Bank 0). EDA[7:0] forms an 8-bit error check bit bus that is associated with the data on DDA[63:0].

EDB[7:0] – Check Bus (Bank 1). EDB[7:0] forms an 8-bit error check bit bus that is associated with the data on DDB[63:0].

ADRS[11:0] – Address Bus. ADRS is a 12-bit row/column multiplexed address bus that supplies the address to the DRAM to access the proper 128-bit data word. The multiplexing is programmable for different depths of DRAM.

CYM7264 – 64-bit EDC (continued)

R/$\overline{W}$[1:0] – Read/Write Control. R/$\overline{W}$[1:0] are the read/write controls for the two banks of the DRAM array. R/$\overline{W}$0 controls read/write for all blocks of DDA[63:0], R/$\overline{W}$1 controls read/write for all blocks of DDB[63:0].

$\overline{RAS}$[3:0] – These signals are the four $\overline{RAS}$ outputs to control each block of the DRAM.

$\overline{CAS}$[3:0] – These signals are the four $\overline{CAS}$ outputs to control each block of the DRAM.

The address bus, ADRS[11:0], RAS[3:0], CAS[3:0] should be connected through a set of drivers to the appropriate DRAM inputs. R/W[1:0] should be connected through a set of latches, gated by the appropriate CAS to the DRAM R/W controls. The driver configuration is dependent upon the capacitance that must be driven.

The data bus, check bus, and read/write control signals are connected across the DRAM array. DDA[64:0] and EDA[7:0] are connected to the data I/O of all the Bank 0 DRAMs. The Bank 0 DRAMs are the top row of DRAMs in *Figure 4*. LR/$\overline{W}$0 is connected to the Write Control input of all the Bank 0 DRAMs. DDB[63:0] and EDB[7:0] are connected to the data I/O of all the Bank 1 DRAMs. LR/$\overline{W}$[1] is connected to the read / write control inputs of all of the DRAMs of Bank 1.

$\overline{RAS}$0 and $\overline{CAS}$0 are connected to the $\overline{RAS}$ and $\overline{CAS}$ inputs respectively of all of the DRAMs of block 0. Block 0 is the left column of DRAMs in the array in *Figure 4*. Note that each block consists of Bank 0 and Bank 1. Similarly, $\overline{RAS}$1 and $\overline{CAS}$1 are connected to the $\overline{RAS}$ and $\overline{CAS}$ inputs respectively of all of the DRAMs of block 1.

DRAM Timing

The system bus clock rate determines the DRAM timing through an internal (X2, X4) phase locked loop, or an externally generated multiple clock (X1, X2, X3, X4 applied to MCLK input). Along with the multiplier selection, the appropriate VCO is selected to generate either a 66-MHz, 80-MHz, or 100-MHz internal clock. This selection is shown in *Table 3*. There are two versions, –H and –S. The –H version permits the use of the higher clock frequency multiples for maximum performance.

Table 3. Required PLL Frequency

Bus Clock (MHz)	Phase Lock Loop Frequency (MHz) – H	Phase Lock Loop Frequency (MHz) –S
40	80	80
33	66 (int), 99 (ext)	66
25	100	50 (ext)

The phase lock loops should be operated close to their center frequency to guarantee operation. For deviations from the bus clock frequencies listed in *Table 3*, consult Command Register 4 (programming of VCO[1:0]). Refer to the CLM[1:0] field in the Command register for programming details.

DRAM timing is fully programmable through internal registers. The resolution of the timing is equal to the period of the internal clock. (This is normally twice the bus clock frequency for 40-MHz bus speeds.) The parameters listed in *Table 4* are programmable.

Refer to the timing diagrams at the end of this data sheet for the timing definitions. Refer to the Register Descriptions for details.

Table 4. DRAM Programmable Timing Parameters

Parameter	Description
t_{AR}	Address to $\overline{RAS}$ assertion
t_{RAM}	$\overline{RAS}$ to multiplexed address
t_{MAC}	Multiplexed address to $\overline{CAS}$
t_{RAS}	$\overline{RAS}$ pulse width
t_{RPR}	$\overline{RAS}$ pre-charge width
t_{CP}	$\overline{CAS}$ pre-charge width
t_{DC}	FIFO data delay to $\overline{CAS}$
t_{RIN}	$\overline{RAS}$ completion during non-reflective inhibit
t_{ENR}	Enable delay on read
t_{ENW}	Enable delay on write

Refresh and Scrubbing

Refresh requirements vary depending on the density and organization of the DRAM chips in the system. However, rows must be refreshed at the same interval (approximately every 15 microseconds the next row is refreshed). The refresh requests are generated by two cascaded counters. A programmable 7-bit counter divides CLK down to create a 1-MHz clock signal. This clock is further divided by a 4-bit, modulo 15 counter, to generate a refresh request every 15 µsec. These refresh requests are synchronously arbitrated with memory requests.

The 26-bit Scrub Address counter is comprised of three smaller counters: the least significant 12 bits form a row scrub counter, the middle two bits form a block counter, and the most significant 12 bits form a column address counter.

All four banks of a given block are scrubbed simultaneously at a particular address. All error correction channels in the controller are used in parallel (4 channels in CYM7232, 2 channels in CYM7264). While one of the four DRAM blocks is scrubbed, the other three blocks undergo normal refresh. The 2-bit Scrub Block counter advances after all rows in a particular block are scrubbed. Finally, the column address is incremented so that all rows and blocks of the next column are refreshed and scrubbed. A fully populated memory using 16-Mbit devices to achieve 1-gigabyte capacity is scrubbed in little more than 15 minutes. When an error is detected during scrubbing operations, the correction address will be copied from the Refresh Address counter to the Error Location register. (Note that when an error occurs in a normal read operation, the corrected data is not written back into the memory array. Data is corrected inside the DRAMs during scrubbing cycles only.) When an error occurs during refresh/scrubbing operations the refresh cycle (i.e., a read to check for errors) is turned into a scrub cycle (i.e., read-modify-write to correct the errors).

Each block of memory may be populated with different sized DRAM components however, all banks within a given block must be populated with the same depth memory chip. For simplicity, the Refresh Address counter treats every block as if it were populated with DRAMs of maximum (16-Mbit) capacity. When refreshing smaller memories, the same address location will be scrubbed multiple times before the counter advances to the next location.

Refresh Modes

There are two modes of refresh/scrubbing. The four $\overline{RAS}$ signals are staggered differently in each mode. Staggering prevents noise problems when switching current simultaneously to multiple blocks of DRAM.

Staggered $\overline{RAS}$

The onset of each $\overline{RAS}$ signal is staggered by one bus clock (four bus clocks overall) in the first mode. Once all $\overline{RAS}$ lines are asserted a single $\overline{CAS}$ signal is selected for presentation to the scrubbed block of memory. The strobe signal used to enable clocking of the scrubbed data into the controller is also delayed by an amount equal to the staggered $\overline{RAS}$ delay.

Mutually Exclusive $\overline{RAS}$

Some SIMMs are constructed with multiple sections of $\overline{RAS}$ enabled DRAM (i.e., common $\overline{CAS}$ lines across sections) The controller offers a second non-overlapping $\overline{RAS}$ refresh mode that supports these SIMMs. This is essential so that the $\overline{CAS}$ that is asserted for the scrub operation will enable only the required SIMM section. Should this type of DRAM SIMM be used, pairs of blocks would be $\overline{RAS}$ enabled during refresh or normal DRAM accesses. Each block pair would share a common $\overline{CAS}$. The controller may be configured to internally OR the appropriate $\overline{CAS}$ pairs to produce a single $\overline{CAS}$ output for each pair of blocks. Refresh in the non-overlapping $\overline{RAS}$ mode is longer than that of the staggered $\overline{RAS}$ refresh mode. Refer to the Register Descriptions for details.

Initialization

The DRAM is initialized when the INIT command is given. The DRAMs are energized with 15 $\overline{RAS}$ only cycles. All of DRAM can then optionally be filled with zeros and the associated error check bits.

Diagnostic Features

For diagnostic purposes, the DRAM error check bits may be read or written by the system. The error check bits may be accessed by reading the EDC registers at any time. The error check bit fields will contain the error check bits from the previous DRAM read cycle. Error check bits may be directly written to DRAM by first writing the desired check bits to the Write Check Bit register and then setting the appropriate control bit in the Command register. All subsequent DRAM writes will write the check bits from this register. Clearing the control bit will return the check bit source to the data path's write error check bit generation circuitry.

Bus Interface Signal Description

D[63:0] – Data. During the data phase, D[63:0] contains the transactions data. The system data bus signals are equipped with holding buffers. These buffers use a weak feedback buffer combined with an input buffer to form a latch. The latch holds the last value driven on the bus.

DP[7:0] – Data Parity. During the data phase, DP[7:0] reflects the parity of the transaction's data. During the address phase, DP[7:0] is ignored and the outputs are three-stated. Data parity is checked only over those bytes that are enabled. During a data phase write, DP[7:0] are inputs, receiving the parity as transferred across the bus. During a data phase read, DP[7:0] are outputs, indicating the parity of the data that has been applied to the bus. The parity output is enabled only when the relevant data byte is enabled. The parity outputs remain three-stated when the parity is disabled. The parity's sense (i.e., odd/even and enable/disable) is specified by the Parity Mode bits, PM[2:0]. DP[7:0] are assigned as given in *Table 5*.

The system data bus parity signals are equipped with holding buffers similar to those used by the system data bus.

Table 5. Data Parity Assignments

Data Parity	Data Byte
DP[0]	D[7:0]
DP[1]	D[15:8]
DP[2]	D[23:16]
DP[3]	D[31:24]
DP[4]	D[39:32]
DP[5]	D[47:40]
DP[6]	D[55:48]
DP[7]	D[63:56]

PMD[2:0] – Parity Mode. The Parity Mode bits specify the parity computation algorithm and identify those signals that participate in the parity computation. They must be hardwired for the correct configuration. The parity mode selection is applied to both the address and data buses. These bits are defined below.

PM2
- 0 – Even Parity Computed (sum of bits in byte and parity bit is even.)
- 1 – Odd Parity Computed (sum of bits in byte and parity bit is odd.)

PM1
- 0 – Data Parity Disabled
- 1 – Data Parity Computed

PM0
- 0 – Address Parity Disabled
- 1 – Address Parity Computed

A[35:0] – Address. During the address phase, the system will supply the transaction's address on A[35:0] and assert $\overline{AS}$.

AP[3:0] – Address Parity. During the address phase, the lowest 32 bits of the transaction's address can be checked for parity. The system can generate a set of parity inputs AP[3:0] that correspond to A[31:0]. Parity is not supported for A[35:32]. The parity's sense (i.e., odd/even and enable/disable) is specified by the Parity Mode bits, PM[2:0]. Note that the parity mode bits also define the parity mode for the data bus. AP[3:0] are assigned as given in *Table 6*.

Table 6. Address Parity Assignments

Address Parity	Address Byte
AP[0]	A[7:0]
AP[1]	A[15:8]
AP[2]	A[23:16]
AP[3]	A[31:24]

TYPE[5:0] – Transaction Type. During the address phase, TYPE[5:0] specify the Transaction Type (see *Table 7*). These are synchronous inputs. Note that the TYPE input may be changed on a transaction by transaction basis, consequently, different processors may be mixed within the system.

TYPE0 – Read/Write. When 0, this bit indicates the transaction is a write. When 1, this bit indicates the transaction is a read.

Table 7. Type Interpretation

Type Bits						Data Size	Transaction Type
5	4	3	2	1	0		
0	0	X	X	X	0	Any	Write
0	X	X	X	X	1	Any	Read
1	0	X	X	X	0	Default Burst	Write
1	X	X	X	X	1	Default Burst	Read
X	X	X	X	0	X	≥ Bus Width	Sequential Burst Order
X	X	X	X	1	X	≥ Bus Width	Intel Burst Order
X	X	X	0	X	X	Any	Size [3:0] are Size Bits
0	X	X	1	X	X	≤ Bus Width	Size [7:0] are Byte Enables
X	X	0	X	X	X	Any	Little-Endian Bus
X	X	1	X	X	X	Any	Big-Endian Bus
0	1	X	X	X	0	Any	Posted Write
1	1	X	X	X	0	Default Burst	Posted Write

TYPE1 – Burst Order. Given a system bus of width N bytes (N = 4 or 8), any transaction as specified by the SIZE input which is greater than N constitutes a burst. Thus transactions of double words (8 bytes) and larger are bursts for a 32-bit bus and transactions of 16 bytes and larger are bursts for a 64-bit bus. The maximum burst length is 128 bytes. During bursts the lowest order bits of the address input are ignored. AD[1:0] are ignored for a 32 bit bus system and AD[2:0] are ignored for a 64 bit bus system. This is the alignment constraint.

The next higher set of address inputs are loaded into a counter, which generates the proper address as the burst proceeds. The counter length is given in *Table 8*. The generated burst address will wrap around at the cache line end and complete the burst access for the remainder of the cache line.

Table 8. Burst Counter Length

Burst Length (bytes)	Burst Counter Length for 32-Bit Bus (bits)	Burst Counter Length for 64-Bit Bus (bits)
8	1	Not Burst
16	2	1
32	3	2
64	4	3
128	5	4

A new address, in which the burst counter serves as the lowest portion, is formed. The counter extends the length of address bits as shown in *Table 8* and starts at AD2 for a 32-bit system bus and at AD3 for a 64-bit system bus. All higher address bits (above the counter) remain fixed throughout the burst transaction and are not affected by rollover of the burst counter. As an example, for a 64-bit system bus and a SIZE of 64 bytes, the system ignores AD[2:0], fixing these bits at 0. AD[5:3] form the internal burst counter starting from the address as transferred over the system bus, and AD[35:6] remain fixed as originally input. This address generation is shown for this example in *Table 9*.

Table 9. Burst Address Example

AD[35:6] Fixed	AD[5:3] Counter	AD[2:0] 000

When TYPE1 = 0 the burst order is sequential. Subsequent addresses are generated by sequentially incrementing the bits of the address within the range of the burst counter as determined above. After reaching the address in which all burst counter bits are ones, the counter wraps around to zero. Higher-order addresses remain fixed.

When TYPE1 = 1 the burst counter increments in the non-sequential fashion characteristic of Intel processors. In all other respects, the address for the burst is the same as that in the sequential case. The non-sequential burst counter algorithm extends the Intel scheme to any length burst. The nonsequential counting starts at the address specified by the address bus input. The counter bits are then incremented in the following fashion:

1. the lowest-order bit always toggles,
2. a bit toggles only if the next lowest order bit in the counter is toggling for the second time (independent of its value).

For example, if the burst counter is 3 bits in length (AD[5:3] as above) and begins at address 101, then the counting sequence is

101, 100, 111, 110, 001, 000, 011, 010

Notice that in this counting sequence, higher-order bits change the least often and therefore result in a minimum number of DRAM page mode accesses.

TYPE2 – SIZE Interpretation. The SIZE bits have two alternative interpretations. When TYPE2 = 0, the transaction length in bytes is given by the value of SIZE[3:0]. When TYPE2 = 1, the byte(s) that are enabled in the transaction are specified when their respective size bits are asserted LOW (e.g., SIZE[N] means BYTE[N] participates in the transaction). For elaboration see the SIZE[7:0] definition.

TYPE3 – Little Endian/Big Endian. Processors may define the position of BYTE 0 on the bus in either of two ways. Either BYTE 0 appears as the lowest byte on the bus (D[7:0] – little endian, TYPE3 = 0) or BYTE 0 appears as the highest byte on the bus (big endian – D[M:M–7], where M = Bw – 1. Bw is the bus width in bits, TYPE3 = 1). For elaboration see the definition of the SIZE[7:0] bits.

TYPE4 – Write Posting. When TYPE4 = 1, the write data is posted into the Write FIFO, where it remains until the next read is completed. This can be used to postpone the actual DRAM write until after the DRAM read is completed, thereby speeding cache line fills.

TYPE5 – Default Burst Mode. When TYPE5 = 0, the transaction's size is specified by SIZE[7:0] (which are interpreted according to TYPE2). When TYPE5 = 1, the transaction's size is specified by the default burst size programmed into the Command register. The burst size defaults to this value regardless of TYPE5 during reflective reads transformed into writes and writes transformed to reads for ownership.

SIZE[7:0] – Transaction Size. During the address phase, SIZE[3:0] specify the number of bytes to be transferred during a bus transaction. These are synchronous inputs. SIZE[7:4] are an extended size control used to support byte enabled transfers. The expanded definition is compatible with i486, i860, SPARC, MIPS, 88K and 68040 processors. The interpretation of SIZE is determined by TYPE2 as in *Table 10* through *Table 16*. Note that for size specifications that are larger than the system bus size, the Transaction Size specifies the internal burst address generation wraparound.

Two interpretations are offered in the above table to support SPARC MBus and Motorola 88K processors.

Table 10. Size Interpretation with TYPE2 = 0, SIZE[7:4] = XXXX

SIZE 3	SIZE 2	SIZE 1	SIZE 0	Transaction Size
0	0	0	0	Byte
0	0	0	1	Halfword (2 Bytes)
0	0	1	0	Word (4 Bytes)
0	0	1	1	Doubleword (8 Bytes)
0	1	0	0	16-Byte Burst
0	1	0	1	32-Byte Burst
0	1	1	0	64-Byte Burst
0	1	1	1	128-Byte Burst
1	0	0	0	32-Byte Burst
1	0	0	1	32-Byte Burst
1	0	1	0	64-Byte Burst
1	0	1	1	64-Byte Burst
1	1	0	0	Doubleword (8 Bytes)
1	1	0	1	Word (4 Bytes)
1	1	1	0	Halfword (2 Bytes)
1	1	1	1	Byte

Table 11. 64 Bit Bus Address Interpretation Size = 1 Byte

A2	A1	A0	Byte #	Big Endian	Little Endian
0	0	0	0	D[63:56]	D[7:0]
0	0	1	1	D[55:48]	D[15:8]
0	1	0	2	D[47:40]	D[23:16]
0	1	1	3	D[39:32]	D[31:24]
1	0	0	4	D[31:24]	D[39:32]
1	0	1	5	D[23:16]	D[47:40]
1	1	0	6	D[15:8]	D[55:48]
1	1	1	7	D[7:0]	D[63:56]

Table 12. 64 Bit Bus Address Interpretation Size = 2 Bytes

A2	A1	A0	Halfword #	Big Endian	Little Endian
0	0	X	0	D[63:48]	D[15:0]
0	1	X	1	D[47:32]	D[31:16]
1	0	X	2	D[31:16]	D[47:32]
1	1	X	3	D[15:0]	D[63:48]

Table 13. 64 Bit Bus Address Interpretation Size = 4 Bytes

A2	A1	A0	Word #	Big Endian	Little Endian
0	X	X	0	D[63:32]	D[31:0]
1	X	X	1	D[31:0]	D[63:32]

Table 14. 32 Bit Bus Address Interpretation Size = 1 Byte

A2	A1	A0	Byte #	Big Endian	Little Endian
X	0	0	0	D[31:24]	D[7:0]
X	0	1	1	D[23:16]	D[15:8]
X	1	0	2	D[15:8]	D[23:16]
X	1	1	3	D[7:0]	D[31:24]

Table 15. 32 Bit Bus Address Interpretation Size = 2 Bytes

A2	A1	A0	Half-Word #	Big Endian	Little Endian
X	0	X	0	D[31:16]	D[15:0]
X	1	X	1	D[15:0]	D[31:16]

Table 16. Size Interpretation with TYPE2 = 1

Size[x]								Byte
7	6	5	4	3	2	1	0	
X	X	X	X	X	X	X	0	D[7:0]
X	X	X	X	X	X	0	X	D[15:8]
X	X	X	X	X	0	X	X	D[23:16]
X	X	X	X	0	X	X	X	D[31:24]
X	X	X	0	X	X	X	X	D[39:32]
X	X	0	X	X	X	X	X	D[47:40]
X	0	X	X	X	X	X	X	D[55:48]
0	X	X	X	X	X	X	X	D[63:56]

Processors generally require their byte enable signals to be contiguous. No checking is performed to distinguish invalid combinations from valid combinations.

$\overline{AS}$ – Address Strobe. This signal is asserted by the bus master during the address phase of the transaction. The address and transaction attributes are strobed into the Controller Module during the address phase. The address phase is one clock cycle long and is normally followed by one or more data phases.

$\overline{DS}$ – Data Strobe. This signal is asserted by the bus master to begin the data phase of the transaction. Data strobe is recognized in certain modes and can be used by the system to delay the onset of the transaction. If the transaction is a burst, data strobe can not be used to interrupt or delay individual data phases of the burst. Data Strobe may be permanently asserted in those applications that do not need this function. Refer to the section on Bus Acknowledge and Data Strobe Modes for details.

$\overline{BLST}$ – Burst Last. The burst length is specified by SIZE[3:0] or the programmed default burst length by way of the TYPE input during the address phase of every transaction. $\overline{BLST}$ may be used by the bus master to override the default or SIZE specified burst length by prematurely terminating the bus transaction. $\overline{BLST}$ must be asserted in the same cycle as the last data transfer.

$\overline{INH}$ – Inhibit. This signal may be asserted by a cache controller in multiprocessing environments to abort a bus transaction already in progress. When $\overline{INH}$ is received before the snoop window ends, the operation is terminated. If the transaction is a memory read, no data is transferred over the system bus while the snoop window is open. If the transaction is a memory write and data has already been transferred, the internal FIFOs are cleared. Inhibit may be used to prematurely terminate I/O opera-

tions before data is transferred. $\overline{INH}$ should not be asserted after the snoop window closes.

$\overline{TRC}$ – Transform Cycle. This signal, when asserted along with $\overline{INH}$, transforms an inhibited read cycle into a write cycle (reflective) or an inhibited write cycle into a read cycle (read-for-ownership). Transformed transactions use the programmed default burst length and ignore the SIZE specified in the original transaction. The burst begins at the address specified at the transaction start.

$\overline{SNW}$ – Snoop Window. This input may be used to define the duration of the snoop window. Operations may be inhibited and transformed in any cycles in which this signal is asserted. As an alternative, the duration of the snoop window may be defined by an internal counter.

$\overline{RSTIN}$ – Reset In. This signal is used to reset the controller. The signal must last for at least 16 clocks. This signal is internally synchronized to the bus clock.

$\overline{BACK}$[1:0] – Bus Acknowledge. These signals supply the transaction acknowledge to the bus master. They are defined in *Table 17*. These signals also receive acknowledges from the system during reflective reads thereby acting as data strobes. During system reset $\overline{BACK}$[1:0] act as inputs to program bus acknowledge modes and select the source of the snoop window signal.

$\overline{BACK}$[1:0] are used as inputs during Reset to select the Bus Acknowledge and Data Strobe modes. $\overline{BACK}$[1:0] must be driven according to *Table 18* when Reset is asserted to invoke the desired mode.

$\overline{UERR}$ – Uncorrectable Error Interrupt. This signal indicates the presence of an unrecoverable error condition on a read operation. The signal is asserted at the same time as the associated acknowledge is sent to the system bus. As with $\overline{BACK}$[1:0], $\overline{UERR}$ may serve as an input. The signal must be driven to select the source of the Snoop Window signal during system reset. $\overline{UERR}$ should be pulled up with a 1K-ohm resistor to V_{CC}.

Table 17. $\overline{BACK}$[1:0] Outputs

$\overline{BACK}$1	$\overline{BACK}$0	Definition
0	1	Valid Data Transfer
1	1	Wait States
Three-state	Three-state	Idle Cycles

Table 18. $\overline{BACK}$[1:0] Inputs When $\overline{RSTIN}$ is Asserted

$\overline{BACK}$1	$\overline{BACK}$0	$\overline{DS}$ Mode	$\overline{BACK}$ Mode
0	0	MBus ($\overline{DS}$ Gnd)	With Data
0	1	Early $\overline{DS}$ (1 Clk)	With Data
1	0	Real-Time $\overline{DS}$	None (Uses $\overline{BR}$/$\overline{FE}$)
1	1	Early $\overline{DS}$ (2 Clks)	Early $\overline{BACK}$ (1 Clk)

Table 19. $\overline{UERR}$ Inputs When $\overline{RSTIN}$ is Asserted

$\overline{UERR}$ ($\overline{SNW}$)	Snoop Window Source
0	External
1	Internal

When a read is inhibited and transformed into a write, the $\overline{BACK}$[1:0] signals become inputs and are used to strobe the bus data into the Reflective FIFO. *Table 20* gives the interpretation of the $\overline{BACK}$[1:0] inputs when the reflective writes are in progress.

Table 20. $\overline{BACK}$[1:0] Inputs as Reflective Reads are Transformed Into Writes

$\overline{BACK}$1	$\overline{BACK}$0	Definition
0	1	Valid Data Transfer
1	1	Idle Cycle
Other	Modes	Invalid

$\overline{BERR}$ – Bus Error. This signal indicates that a parity error condition has occurred during the address or data phase of a transaction. This signal is asynchronous (i.e., it will occur one cycle after the corresponding address parity error or two cycles after the corresponding data parity error). $\overline{BERR}$ may be programmed to last for one clock cycle or until cleared. Due to the nature of $\overline{BERR}$ internal to the module, the controller will log a parity error in its status register if any other device pulls $\overline{BERR}$ LOW.

$\overline{BR}$/$\overline{FE}$ – Bus Request/FIFO Empty. This signal will be issued by the controller during reflective read transactions. $\overline{BR}$ from the main memory system should be interpreted as the highest priority request for bus mastership to the system's arbiter. In this case $\overline{BR}$/$\overline{FE}$ works in conjunction with $\overline{BG}$ and $\overline{BB}$ to effect this mastership. Additional system bus transactions will be prevented until the ongoing write (resulting from the reflective read) to main memory has completed. Systems having more elaborate protocols for acknowledging data transfers between a requesting cache and a cache data owner can use this signal to prevent the next transaction from overwriting the reflective data path inside the controller.

This output may also be programmed to include the empty status of the FIFOs. $\overline{BR}$/$\overline{FE}$ will then be asserted if either the reflective FIFO or the normal write FIFO are not empty. This output may be used by systems that assess the availability of the controller before the data phase is initiated and pause until the controller becomes available.

$\overline{BG}$ – Bus Grant. This signal is asserted by the external arbiter in response to a $\overline{BR}$, to indicate that the controller has been granted ownership of the bus.

$\overline{BB}$ – Bus Busy. This signal is asserted by the controller for the duration of its bus ownership. The controller will acquire the bus as it completes the main memory write transaction during reflective read operations. When Bus Arbitration is disabled, this bidirectional pin may be used as an output to report read status. When the controller module begins a read operation, $\overline{BB}$ will be asserted indicating that the host can expect data in several clock cycles (actual number of clock cycles depends on programmed DRAM timings).

Table 21. ID[3:0] in Generic Mode

ID3	ID2	ID1	ID0	DRAM Mode Selection
0	0	X	X	Not Selected
0	1	0	0	Not Selected
0	1	0	1	I/O Registers
0	1	1	0	Indirect Address Register
0	1	1	1	Not Selected
1	X	X	X	Memory

ID[3:0] – Identification. The Identification bits are synchronous inputs recognized during the address phase. The ID bits are used in conjunction with address signals to define the nature of the bus

transaction and select I/O registers or DRAM memory. For MBus operation refer to *Table 39*. For the generic mode a match is required between ID[3:0] and the fixed values shown in *Table 21*.

CLK – Clock. CLK synchronizes all bus transactions. All transactions are strobed in at the rising edge of clock.

MCLK – Multiple Clock. MCLK may be used to supply a higher-frequency DRAM clock in lieu of using the internal PLLs. MCLK must be an integer multiple of CLK (either 1, 2, 3, or 4). When using the PLLs, MCLK must be tied to CLK.

$\overline{INT}$ – Interrupt. This signal indicates that the module has a pending interrupt that requires service. This output remains asserted until the interrupting condition is cleared.

$\overline{IMD}$ – Interface Mode. When tied LOW, the controller operates in the MBus mode. When tied HIGH, the controller operates in the generic mode.

Pin Description

Table 22 through *Table 25* summarize the functional pin connections of the controller module. Power and ground connections are not listed.

Table 22. Pin Descriptions

Signal Name	I/O	Description
D[63:0]	I/O	System Data Bus: These lines are used to transfer data to and from the DRAM Module. These lines are normally three-stated except when a valid read cycle is in progress.
DP[7:0]	I/O	Data Bus Parity: These signals follow the direction of the data bus. When the device is driving the data bus (read), data parity is generated and supplied to these pins. When data is entering the device, data parity is checked.
PMD[2:0]	I	Parity Mode: These inputs specify the parity mode for data and address.
A[35:0]	I	System Address Bus: These lines are used to transfer the address to the DRAM module.
AP[3:0]	I	Address Bus Parity: These inputs are examined for address integrity during accesses to the device.
$\overline{AS}$	I	Address Strobe: This input is used to indicate that the bus address and control signals are valid. It is used to enable clocking of the address and control information into the controller.
$\overline{DS}$	I	Data Strobe: This input is used to indicate that the data transaction is to take place.
$\overline{BLST}$	I	Burst Last: This input can be used to terminate a transaction.
$\overline{BACK}$[1:0]	I/O	Bus Acknowledge: These acknowledge signals output the transaction response back to the bus master. During reflective reads, these signals are inputs. During Reset, act as inputs and are used to invoke certain modes.
$\overline{UERR}$	I/O	Uncorrectable Error: This interrupt signal reports an unrecoverable error condition during a read. During reset it acts as an input to select Snoop Window source.
$\overline{RSTIN}$	I	Master Reset: Activating this input causes the module to set all control and status bits to their reset state.
CLK	I	System Bus Clock: This clock is used to synchronize the controller's operation to the system bus clock.
$\overline{BERR}$	O	Bus Error (Three-State): Indicates that a parity error has occurred on the bus. $\overline{BERR}$ is asynchronous.
$\overline{INH}$	I	Inhibit is used to abort read and write operations.
$\overline{SNW}$	I	Snoop Window: Defines the time in which Inhibit can be asserted.
$\overline{TRC}$	I	Transform Cycle: This input reverses the sense of inhibited operations.
TYPE[5:0]	I	Transaction Type: These inputs determine the transaction type.
SIZE[7:0]	I	Transaction Size: These inputs indicate the size of the transaction.
$\overline{INT}$	O	Interrupt (Three-State): This output indicates that an interrupt request is pending.
ID[3:0]	I	Identification: Selects memory or internal registers; positions the module in the address space.
$\overline{BR/FE}$	O	Bus Request/FIFO Empty: Reflects the status of the reflective or write FIFOs.
$\overline{BG}$	I	Bus Grant.
$\overline{BB}$	I/O	Bus Busy: Used to assert bus ownership or to indicate the beginning of a read operation.
ADRS[11:0]	O	DRAM row/column multiplexed address.
R/$\overline{W}$[3:0]	O	DRAM read/write control; one output per bank. (CYM7232 only)
R/$\overline{W}$[1:0]	O	DRAM read/write control; one output per bank. (CYM7264 only)
$\overline{RAS}$[3:0]	O	DRAM row address strobe; one per block.
$\overline{CAS}$[3:0]	O	DRAM column address strobe; one per block.

Table 23. Special Function Signals

Signal Name	I/O	Description
TSTE	I	Test Enable: This input must be set to 1 for proper operation.
TSTM	I	Test Mode.
TST[2:0]	O	Test Outputs.
MCLK	I	Multiple Frequency Clock: Optional input if internal PLLs are not used.
IMD	I	MBus/generic interface mode select.

Table 24. DRAM Data Signals (CYM7232)

Signal Name	I/O	Description
DDA[31:0]	I/O	DRAM data bus interface, Bank 0
EDA[6:0]	I/O	DRAM error check bit bus interface, Bank 0
DDB[31:0]	I/O	DRAM data bus interface, Bank 1
EDB[6:0]	I/O	DRAM error check bit bus interface, Bank 1
DDC[31:0]	I/O	DRAM data bus interface, Bank 2
EDC[6:0]	I/O	DRAM error check bit bus interface, Bank 2
DDD[31:0]	I/O	DRAM data bus interface, Bank 3
EDD[6:0]	I/O	DRAM error check bit bus interface, Bank 3

Table 25. DRAM Data Signals (CYM7264)

Signal Name	I/O	Description
DDA[63:0]	I/O	DRAM data bus interface, Bank 0
EDA[7:0]	I/O	DRAM error check bit bus interface, Bank 0
DDB[63:0]	I/O	DRAM data bus interface, Bank 1
EDB[7:0]	I/O	DRAM error check bit bus interface, Bank 1

Power and Ground Connections

There are two sets of power and ground connections. One set is for the logic and I/O circuitry and is indicated by V_{SS} and V_{DD} in the pin diagram. All V_{SS} pins should be connected to ground and all V_{DD} pins should be connected to the +5 volt supply. There are separate supply connections for the internal phase lock loops. V_{DDL} is the +5 volt supply connection and V_{SSL} is the ground connection for the phase lock loops. For superior noise immunity, V_{SSL} and V_{DDL} should be connected with independent pcb routing. These connections should run to the power supply where it connects to the circuit board on which the controller module resides.

The pinout lists several no connect (NC) pins. These connections should be left open. They may be used in future versions of the controller. IMD should be tied HIGH to invoke the generic bus interface mode or LOW for MBus mode. TSTE must be held HIGH.

32-Bit System Bus Connection

The 32-bit EDC version of the controller (CYM7232) may be connected to a 32-bit system data bus. This is accomplished by tying D0 to D32, D1 to D33 and so forth. The SBS field in the Command register must also be programmed with 0 to invoke the 32-bit system bus mode forcing the controller to multiplex read data onto the system bus and demultiplex write data from the system bus. The controller may be further connected for a multiplexed address/data bus by tying A[31:0] to D[31:0].

If the system bus employs bus parity, then DP0 should be tied to DP4, DP1 tied to DP5 and so forth forming a four-bit parity nibble for the 32-bit system bus.

64-Bit System Bus Connection

The 64-bit EDC version of the controller may only be connected to 64 bit bus systems. Address and data may be multiplexed, as in the 32 bit case, by connecting the module's address bus to a portion of its data bus. Address parity and data parity may also be shared, by connecting the module's address parity bus bits to a portion of its data parity bus.

Internal Registers

Several internal registers are available to set-up the controller and report status to the host. Each register is spaced 16 bytes apart in the address space so that its contents will be accessible on D[7:0] of the data bus regardless of system bus width or orientation (little/big endian). The EDC registers are accessed as 32-bit registers. An internal 8-bit indirect address register is provided to point to the individual I/O locations inside the controller. A register map is provided in *Table 26*.

Table 26. Register Map

Index	Name	R/W	7	6	5	4	3	2	1	0
00 H	Command Register 0	R/W	CIE	RFD						
01 H	Command Register 1	R/W	INIT	WC	AEM	SBS	ES	CLM		RFT
02 H	Command Register 2	R/W	BLP				BLK		DFB	
03 H	Command Register 3	R/W	RCM		BAM		SEN	CAM	RSM	BRM
04 H	Command Register 4	R/W	PLT		VCO		IOSWC			
05 H	Command Register 5	R/W	IE		EDP	EAP	EME	EUE	EDE	ESE
06 H	Command Register 6	R/W	SNWWRCNT				SNWRD CNT			
07 H	Reserved									
08 H	DRAM Timing 0	R/W	RAM				AR			
09 H	DRAM Timing 1	R/W	RAS				MAC			
0A H	DRAM Timing 2	R/W	CP				RPR			
0B H	DRAM Timing 3	R/W	RIN				DC			
0C H	DRAM Timing 4	R/W	ENW				ENR			
0D H	Reserved									
0E H	Reserved									
0F H	Reserved									
10 H	Base Address [7:0]	R/W	BA[27:20]							
11 H	Base Address [15:8]	R/W	BA[35:28]							
12 H	Logical Block Displacement [7:0]	R/W	Reserved		DS2			DS1		
13 H	Logical Block Displacement [15:8]	R/W	Reserved					DS3		
14 H	Reserved									
15 H	Reserved									
16 H	Reserved									
17 H	Reserved									

Table 26. Register Map (continued)

Index	Name	R/W	7	6	5	4	3	2	1	0
18 H	Logical Block Population Code [7:0]	R/W	LPC3		LPC2		LPC1		LPC0	
19 H	Logical Block Population Code [15:8]	R/W	Reserved				LBP3	LBP2	LBP1	LBP0
1A H	Physical/Logical Map [7:0]	R/W	PBL3		PBL2		PBL1		PBL0	
1B H	Reserved									
1C H	Logical Block Mux Position [7:0]	R/W	Reserved		LBMP1			LBMP0		
1D H	Logical Block Mux Position [15:8]	R/W	Reserved		LBMP3			LBMP2		
1E H	Reserved									
1F H	Reserved									
20 H	Error Location Address [7:0]	R	ELA[7:0]							
21 H	Error Location Address [15:8]	R	ELA[15:8]							
22 H	Error Location Address [23:16]	R	ELA[23:16]		ELA[23:16]					
23 H	Error Location Address [31:24]	R	ELA[31:24]							
24 H	EDC Register 0	R								
25 H	EDC Register 1	R								
26 H	Reserved									
27 H	Reserved									
28 H	Syndrome FIFO Flags 0	R								
29 H	Syndrome FIFO Flags 1	R	See Section on Error Status Registers							
2A H	Reserved									
2B H	Reserved									
2C H	Diagnostic Check Bit 0	W								
2D H	Diagnostic Check Bit 1	W								
2E H	Reserved									
2F H	Reserved									
30 H	Silicon Revision	R	Reserved				REV[3:0]			
31 H	Bus Error	W							BEM	BEC
32 H	Interrupt Status Register	R/W		IC	DBE	ABE	MEW	UEW	DEW	SBW

Index Register

IA[7:0] – Index Address. This register's contents points to all other registers inside the controller. During access to the controller's internal byte wide I/O path, little-endian processors should apply an address with A[3:0] = 0 to enable data onto D[7:0] on their system bus. Big-endian processors should apply an address with their A[3:0] = F to enable data onto D[7:0] on their system bus. Access to the internal registers is controlled through the ID bits. For ID3 equal to 1, all accesses occur to memory. For ID3 equal to 0, access is to the internal registers: with ID[2:0] equal to 110, transactions are directed to the Index register, with ID[2:0] equal to 101, transactions are directed to the register pointed to by the Index register. For all other combinations of the ID input, the controller is not selected. ID3 functions as the Memory/IO select and the remaining ID inputs function as selects or chip enables.

This register is not used in MBus mode. See MBus section for details on writing and reading I/O registers.

Command Registers – Write / Read

Command Register 0

Index	7	6	5	4	3	2	1	0
00 H	CIE	RFD						
Default	0	7F (h)						

CIE – Coherent Invalidate Acknowledge Enable. When this bit is set HIGH it enables acknowledges to MBus Coherent Invalidate cycles. BACK[1:0] are generated two clocks after the address phase in which the TYPE bits specify this cycle. Systems requiring different acknowledge delays should set CIE = 0 and use an external PLD to generate the acknowledge. This bit should be set to 0 when in the Generic Mode.

RFD – Refresh Counter Divisor. These bits divide CLK down to 1 MHz. The output of this counter is further divided by a fixed divide "by 15" counter, which produces the 15 microsecond refresh requests. The division factor is the load value plus 1. For example, the divisor load values in decimal for the various bus clock frequencies are:

24	25 MHz
32	33 MHz
39	40 MHz
49	50 MHz

Command Register 1

Index	7	6	5	4	3	2	1	0
01 H	INIT	WC	AEM	SBS	ES	CLM[1:0]		RFT
Default	0	0	0	0	0	0		0

INIT – Initialization. This bit, when set, triggers an initialization of the DRAM memory and its check bits. The contents of the memory are set to zero and the corresponding check bits are set.

WC – Write Check Bits. Enables writing of the EDC check bits from the registers inside the data path.

0	Write EDC check word computed from incoming data.
1	Write EDC check word from check bit register.

AEM – Address Error Mode. Controls assertion of $\overline{\text{BERR}}$ after an address parity error.

0	$\overline{\text{BERR}}$ asserted for one clock
1	$\overline{\text{BERR}}$ asserted until cleared by writing 1 to ABE in Interrupt Status register

SBS – System Bus Size. Specifies the number of data bits in the system bus.

0	32 Bits
1	64 Bits

ES – EDC Size. Specifies the number of data bits in each EDC packet.

0	32 Bits
1	64 Bits

CLM – Clock Multiplier. These bits program the multiplication factor from the incoming bus clock (CLK) to the internal DRAM timing clock. They are defined as follows:

CLM[1:0]	Clock Multiplier
00	X1
01	X2
10	X3
11	X4

RFT – Refresh Test Mode. This bit must be clear for proper operation.

Command Register 2

Index	7	6	5	4	3	2	1	0
02 H	BLP[3:0]				BLK		DFB	
Default	0				0		0	

BLP – Block Population. These bits define which physical blocks are populated. BLP[N] = 1 indicates that Block N is populated. Block population must be contiguous with one exception. BLP0 and BLP2 can be asserted simultaneously with BLP1 and BLP3 deasserted simultaneously when supporting 36- and 40-bit SIMMS populated with two sections of DRAM memory.

BLK – Number of Blocks. These bits specify the total number of populated blocks. 0 (H) = 1 block ... 3 (H) = 4 blocks.

DFB – Default Burst Length. This field defines the default burst length for cache line read/writes. The bus will execute burst transactions with this default length when the appropriate TYPE bit is asserted during the address phase of a transaction or when an operation is transformed. These bits are interpreted as follows:

DFB[1:0]	Default Burst Length
00	16 Bytes
01	32 Bytes
10	64 Bytes
11	128 Bytes

Command Register 3

Index	7	6	5	4	3	2	1	0
03 H	RCM[1:0]		BAM[1:0]		SEN	CAM	RSM	BRM
Default	0		0		0	0	0	0

RCM – Refresh Control Modes. These bits control refresh and the DRAM INIT process for test purposes. RCM must be set to 11 for proper operation. When asserted, RCM[0] enables refresh and RCM[1] enables the INIT process. (The INIT process occurs after DRAM energizing and fills all DRAM with 0.)

Index Register (continued)

BAM[1:0] – Bus Acknowledge Modes. These bits control the operating modes for read operations. BAM0 controls error correction. BAM1 controls the insertion of wait states.

BAM0 – Error Correction Enable

0 Error correction disabled

1 Error correction enabled

When error correction is disabled, reads as a result of Read Modify Write operations are not affected. Consequently, single-bit errors in the read portion of RMW cycles are corrected and merged with the write data. Uncorrectable errors cause the write back portion of RMW cycles to abort. Read Modify Write transactions are not possible in systems configured without DRAM check bits.

BAM1 – Wait State Insertion on Reads

0 No wait states inserted

1 Wait states inserted

The insertion of wait states allows corrected data to meet minimum set-up requirements in high-speed systems. Wait states should be inserted for systems requiring greater system bus set-up time on reads.

SEN – Scrub Enable. This bit enables scrubbing when asserted HIGH.

CAM – $\overline{CAS}$ Assertion Mode

0 $\overline{CAS}$[3:0] independently asserted.

1 $\overline{CAS}$[3:2] "ORed" to produce $\overline{CAS}$2, $\overline{CAS}$[1:0] "ORed" to produce $\overline{CAS}$0. This mode is provided to support some 36- or 40-bit-wide DRAM SIMMs that contain two rows of memory with independent $\overline{RAS}$ and common $\overline{CAS}$.

RSM – $\overline{RAS}$ Stagger Mode (during Refresh/Scrub operations).

0 $\overline{RAS}$[3:0] staggered by one bus clock.

1 $\overline{RAS}$[3:0] staggered to be non-overlapping (mutually exclusive in time). This mode is provided to support some 36- or 40-bit-wide DRAM SIMMs that contain two rows of memory with independent $\overline{RAS}$ and common $\overline{CAS}$. The $\overline{RAS}$ signals must be mutually exclusive when scrubbing these SIMMs.

BRM – Bus Request Mode

0 Bus arbiter ON. $\overline{BR/FE}$ assertion indicates reflective FIFO status only. With bus arbiter ON, $\overline{BR/FE}$ is deasserted with the recognition of Bus Grant ($\overline{BG}$) and Bus Busy ($\overline{BB}$) is asserted after the $\overline{BB}$ pin goes HIGH.

1 Bus arbiter OFF. $\overline{BR/FE}$ assertion combines write FIFO status and reflective FIFO status (logical OR). Both FIFOs must be empty for the $\overline{BR/FE}$ output to be deasserted. With the bus arbiter OFF, $\overline{BG}$ is ignored, the $\overline{BR/FE}$ output simply reflects the combined FIFO status, and $\overline{BB}$ acts as an output signaling the beginning of a read transaction.

Command Register 4

Index	7	6	5	4	3	2	1	0
04 H	PLT[1:0]		VCO[1:0]		IOSWC			
Default	O(h)		O(h)		F(h)			

PLT[1:0] – Phase-Locked Loop Test. This field is for test purposes only. PLT[1:0] should be programmed to 11 when enabling the internal VCOs, otherwise PLT[1:0] = 00.

VCO[1:0] – Voltage Controlled Oscillation Select. This field selects the appropriate VCO for generating the internal multiplied clock.

00 No VCO selected, use external MCLK
01 70-MHz VCO
10 80-MHz VCO
11 100-MHz VCO

The operating range of the VCOs is given in the following table. Each VCO requires a minimum of 20 ms to phase lock to the system bus clock after being enabled.

VCO (MHz)	Operating Range (MHz)
70	65 – 74.9
80	75 – 84.9
100	95 – 104.9

IOSWC – Snoop Window Count. This value programs the duration of the snoop window for I/O operations in bus clock cycles. The snoop window counter is enabled one clock after an address phase on the bus in which the controller is selected. When a 0 is programmed into the counter the snoop window closes immediately (i.e., the cycle after the address phase). The window can be extended up to 16 clocks after the address phase appears on the bus. After power-up the counter defaults to the maximum value. The internal snoop window is selected by driving $\overline{UERR}$ appropriately during reset.

Command Register 5

Index	7	6	5	4	3	2	1	0
05 H	IE	—	EDP	EAP	EME	EUE	EDE	ESE
Default	0	0	0	0	0	0	0	0

IE – Interrupt Enable. This bit must be set to enable interrupts to the system bus.

EDP – Enable Data Bus Parity Interrupt. Enables the interrupt indicating that one of the data bytes has a parity error.

EAP – Enable Address Bus Parity Interrupt. Enables the interrupt indicating that one of the address bytes has a parity error.

EME – Enable Read-Modify-Write Multiple Error Interrupt. Enables the interrupt indicating that a multiple error has occurred on a read-modify-write cycle.

EUE – Enable Uncorrectable Error in Word Interrupt. Enables the interrupt indicating that an uncorrectable error has occurred in a word.

EDE – Enable Double Bit Error in Word Interrupt. Enables the interrupt indicating that a double bit error has occurred in a 32- (64-) bit word.

ESE – Enable Single Bit Error Interrupt. Enables the interrupt indicating that a single bit correctable error has occurred in a 32- (64-) bit word.

Command Register 6

Index	7	6	5	4	3	2	1	0
06 H	SNWWRCNT[3:0]				SNWRDCNT[3:0]			
Default	F(h)				F(h)			

Index Register (continued)

SNWWRCNT specifies the snoop window duration for memory-write transactions and SNWRDCNT specifies the snoop window duration for memory-read transactions. The internal snoop window is used only if selected by driving $\overline{\text{UERR}}$ appropriately during reset. The snoop window counter is enabled one clock after an address phase on the bus in which the controller is selected. When a 0 is programmed into the counter, the snoop window closes immediately (e.g., the cycle after the address phase). the window can be extended up to 16 clocks after the address phase appears on the bus. After reset, the counter defaults to the maximum value.

DRAM Timing Program Registers – Write / Read

DRAM Timing Register 0

Index	7	6	5	4	3	2	1	0
08 H	RAM[3:0]				AR[3:0]			
Default	F(h)				F(h)			

DRAM Timing Register 1

Index	7	6	5	4	3	2	1	0
09 H	RAS[3:0]				MAC[3:0]			
Default	F(h)				F(h)			

DRAM Timing Register 2

Index	7	6	5	4	3	2	1	0
0A H	CP[3:0]				RPR[3:0]			
Default	F(h)				F(h)			

DRAM Timing Register 3

Index	7	6	5	4	3	2	1	0
0B H	RIN[3:0]				DC[3:0]			
Default	F(h)				F(h)			

DRAM Timing Register 4

Index	7	6	5	4	3	2	1	0
0C H	ENW[3:0]				ENR[3:0]			
Default	F(h)				F(h)			

The DRAM Timing Program registers should not be reprogrammed during operation. The user must reset the part and reprogram all DRAM timing before issuing an INIT.

For optimum performance, DC[3:0] should always be programmed to 0001(b). RIN[3:0] = RAS[3:0] – (RAM[3:0] + MAC[3:0]).

All timing values are set with 4-bit values. The time intervals are specified to 10-ns accuracy when the internal clock is running at 100 MHz, 12.5-ns accuracy when the internal clock is running at 80 MHz, 13.3-ns accuracy when the internal clock is running at 75 MHz, or 15.2-ns accuracy when the internal clock is running at 66 MHz. Refer to the timing diagrams for elaboration.

Table 27. DRAM Timing Values

Hex Value	Delay/Width (ns)			
	66 MHz	75 MHz	80 MHz	100 MHz
0	15.2	13.3	12.5	10
1	30.3	26.6	25	20
2	45.5	40	37.5	30
3	60.7	53.3	50	40
4	80	66.6	62.5	50
5	91	80	75	60
6	106	93.3	87.5	70
7	121	106.6	100	80
8	136	120	112.5	90
9	152	133.3	125	100
A	167	146.6	137.5	110
B	182	160	150	120
C	197	173.3	162.5	130
D	212	186.6	175	140
E	227	200	187.5	150
F	242	213.3	200	160

Table 28. DRAM Timing Program[1]

Parameter	Field Name	Description
t_{RAM}	RAM	$\overline{RAS}$ to multiplexed address
t_{AR}	AR	Address to $\overline{RAS}$ assertion
t_{RAS}	RAS	$\overline{RAS}$ pulse width
t_{MAC}	MAC	Multiplexed address to $\overline{CAS}$
t_{CP}	CP	$\overline{CAS}$ pre-charge width
t_{RPR}	RPR	$\overline{RAS}$ pre-charge width
t_{RIN}	RIN	$\overline{RAS}$ completion during non-reflective Inhibit
t_{DC}	DC	FIFO data delay to $\overline{CAS}$
t_{ENR}	ENR	Enable delay on read
t_{ENW}	ENW	Enable delay on write
t_{ACC}	—	DRAM access time (determine by DRAM chips)
t_{CLZ}	—	DRAM $\overline{CAS}$ to Output Low Z (determined by DRAM chips)
t_{CY}	—	Bus CLK period

Note:

1. All timings may be resolved to 1/n of t_{CY}, where n is the phase locked loop multiplier (e.g. 50-MHz systems having a PLL multiplier of 2 with t_{CY} = 20 ns can have DRAM timing resolutions defined to 10 ns). Therefore, unless the timing values are constrained, the DRAM read data could arrive at the data path input pipeline on a 10-ns boundary rather than a bus clock boundary. The controller will automatically extend certain values that are programmed to provide data on a bus clock boundary, whenever necessary.

DRAM Block Assignment Register Array

Five registers are used to map the incoming address to the four physical blocks of DRAM. These registers specify the Base address of the DRAM array, the gaps between blocks, the relationship between physical blocks and logical blocks, the size of memory each block is populated with, and the RAS/CAS address split point in the DRAMs in each block. The module should be re-initialized when any of these registers are changed during operation.

The Base Address register, Logical Block Displacement register, Logical Block Population Code register, and Logical Block MUX Position register are all 2-byte registers. The Physical/Logical Block Map register is a 1-byte register.

Base Address Register

Byte Address 10H, BA[27:20] (Bits 7:0)
Byte Address 11H, BA[35:28] (Bits 15:8)

15	8	7	0
	BA0[35:28]	BA0[27:20]	
Default	00 H	00 H	

BA[35:20] – Base Address of Memory. This entry specifies the base address of the memory. The base address must be evenly divisible by the depth of the largest DRAM device used multiplied by 16. For example, if the largest DRAM device used is 1M deep, then the smallest base address (other than 0) is BA = 0010 (h); BA[23:20] must be 0.

Logical Block Displacement Register

Byte Address 12H, LBD[7:0]
Byte Address 13H, LBD[15:8]

15	11	10	8	7	6	5	3	2	0
	Reserved	DS(3)[2:0]		Reserved	DS(2)[2:0]		DS(1)[2:0]		
Default	0 H	0 H		0 H	0 H		0 H		

DS(N)[2:0] – Address Displacement of logical block (N). This entry specifies the address displacement of logical block (N) from logical block (N – 1). The starting address of logical block (0) is the Base address of the memory. The starting address of logical block (1) is the sum of the Base address and the displacement selected by DS(1). The starting address of logical block (2) is the sum of the starting address of logical block (1) and the displacement selected by DS(2). The starting address of logical block (3) is the sum of the starting address of logical block (2) and the displacement selected by DS(3). The programmed displacement, DS(N), must be equal to or greater than the depth of the memory chips contained in logical block N–1. When the programmed displacement is equal to the memory chips depth, the memory is contiguous.

DS(N)[2:0]	Displacement
000	256K
001	1M
010	4M
011	16M
100	32M
101	64M
110	128M
111	256M

Logical Block Population Code Register
Byte Address 18H, LPCR[7:0]
Byte Address 19H, LPCR[15:8]

	7	6	5	4	3	2	1	0
	LPC3[1:0]		LPC2[1:0]		LPC1[1:0]		LPC0[1:0]	
Default	00 H							

	15	12	11	10	9	8
	Reserved		LBP3	LBP2	LBP1	LBP0
Default	00 H					

LPC(N)[1:0] – Logical Block Population Code. LPC(N)[1:0] specifies the DRAM type in logical block (N).

LPC(N)[1:0]	DRAM Depth
11	16M
10	4M
01	1M
00	256K

The physical blocks may be configured in any order. To obtain a contiguous memory with no overlaps or gaps, the logical blocks must be populated in order with the largest DRAM type in logical block 0, followed by the next largest DRAM type in logical block 1, etc., and the logical block populations must be contiguous (no unpopulated logical blocks between populated blocks).

LBP(N) specifies whether or not the block is populated. LBP(N) = 0 block not populated. LBP(N) = 1 block populated.

Physical/Logical Block Map Register
Byte Address 1AH, PBLR[7:0]

	7	6	5	4	3	2	1	0
	PBL3[1:0]		PBL2[1:0]		PBL1[1:0]		PBL0[1:0]	
Default	00 H							

PBL(N)[1:0] – Physical Block Association. PBL(N)[1:0] specifies the logical block to which physical block N is mapped.

PBL(N)[1:0]	Association
00	Logical Block 0
01	Logical Block 1
10	Logical Block 2
11	Logical Block 3

Logical Block MUX Position Register
Byte Address 1CH, MPR[7:0]
Byte Address 1DH, MPR[15:8]

	7	6	5	3	2	0
	Reserved		LBMP1[2:0]		LBMP0[2:0]	
Default	00 H					

	15	14	13	11	10	8
	Reserved		LBMP3[2:0]		LBMP2[2:0]	
Default	00 H					

LBMP(N)[2:0] specifies the DRAM column address/row address split for logical block (N). The split is specified in terms of the address applied to the DRAM. Note that bus address 4 is DRAM column address 0. All twelve DRAM address bits are valid for all split selections.

LBMP(N)[2:0]	Row/Column Address Split Location
000	8/7
001	9/8
010	10/9
011	11/10
100	12/11
101	unused
110	unused
111	unused

Error Location Register – Read Only

The Error Location register is a 32 bit register that contains the address of the most recent error. This register is read only and is byte addressable only. All bytes appear on D[7:0]. Byte addresses are as follows:

20H ELA[7:0]
21H ELA[15:8]
22H ELA[23:16]
23H ELA[31:24]

Error Location Address [31:0]

	31	0
	ELA[31:0]	
Default	00 H	

The Error Location Address register reports the address location of an error in the DRAM and how the error occurred. When the error ocurs during a read operation the ELA register reports the address as it appeared on the system bus and the physical block wherer the system bus address is mapped. When the error occurs during a refresh, or scrub, operation the ELA reports the physical block and address in row/column format.

Read Error Location Register Format

ELA[31:30] Physical Block in DRAM
ELA[29:28] 00 (Reports Read Error)
ELA[27:4] System Bus Address A[27:4]
ELA[3:0] 0

Refresh/Scrub Error Location Register Format

ELA[31:30] Physical Block in DRAM
ELA[29:28] 01 (Reports Ref. Error)
ELA[27:16] DRAM Row Address
ELA[15:4] DRAM Column Address
ELA[3:0] 0

After a system bus read error, diagnostic software will translate the system bus address to the row/column address inside the DRAM. This mapping will depend on the DRAM configuration.

When the error occurs during refresh, or scrub, diagnostic software will extract the meaningful portion of the row/column address (from the reported row/column address) based on the DRAM population of the particular physical block in error. The

Error Location Register – Read Only (continued)

DRAM array is always refreshed as if populated with 16-Megabit DRAMs in all blocks. Therefore higher order row and column address bits in the internal refresh counter will increment even when they are not required to span the address space within a block. These redundant bits must be ignored in calculating the location of an error which occurred during refresh.

The ELA register is constantly updated with the address of the current transaction. If an error is detected in the read from DRAM, further writing to this register is locked out until the interrupt bit is cleared. (If two successive transactions incur errors and the interrupt bit is not cleared before the address phase of the second transaction, the address of the second error is lost.)

Error Status Registers – CYM7232

The Error Status registers provide information on errors that have occurred during any read operation (including scrubbing and read modify write). The location of these registers on the data bus will depend on the system bus configuration (32 or 64 bits). *Table 29* shows the location of data path registers for the 64-bit system bus.*Table 30* shows the location of the same registers in the 32-bit system bus application.

Table 29. Error Status Register Map for CYM7232 with 64-Bit System Bus

Index	Name	R/W	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
24 H	EDC Register 0	R					CB2	CB0	SYN2	SYN0
25 H	EDC Register 1	R	CB3	CB1	SYN3	SYN1				
26 H	Reserved									
27 H	Reserved									
28 H	Syndrome FIFO Flags 0	R								FL0
29 H	Syndrome FIFO Flags 1	R				FL1				
2A H	Reserved									
2B H	Reserved									
2C H	Diagnostic Check Bit 0	W								DCB0
2D H	Diagnostic Check Bit 1	W				DCB1				
2E H	Reserved									
2F H	Reserved									

Table 30. Error Status Register Map for CYM7232 with 32-Bit System Bus

Index	Name	R/W	31:24	23:16	15:8	7:0
24 H	EDC Register 0	R	CB2	CB0	SYN2	SYN0
25 H	EDC Register 1	R	CB3	CB1	SYN3	SYN1
26 H	Reserved					
27 H	Reserved					
28 H	Syndrome FIFO Flags 0	R				FL0
29 H	Syndrome FIFO Flags 1	R				FL1
2A H	Reserved					
2B H	Reserved					
2C H	Diagnostic Check Bit 0	W				DCB0
2D H	Diagnostic Check Bit 1	W				DCB1
2E H	Reserved					
2F H	Reserved					

EDC Registers

The EDC Registers contain the Read Error Log FIFO and Check Bits fields. The registers are Read Only. The register at address 24 appears on D[31:0] and the register at address 25 appears on D[63:32] when the module is connected a 64 bit system bus. For 32 bit systems, both registers appear on D[31:0].

EDC Register 0

Index	31	30 … 24	23	22 … 16	15	14 … 8	7	6 … 0
24 H		CB2		CB0		SYN2		SYN0
Default		00 H		00 H		Undefined		Undefined

EDC Register 1

Index	31	30 … 24	23	22 … 16	15	14 … 8	7	6 … 0
25 H		CB3		CB1		SYN3		SYN1
Default		00 H		00 H		Undefined		Undefined

This register will appear on D[63:32] of the 64-bit system bus. When used in a 32-bit system bus application, this register will appear on D[31:0].

SYN0, SYN1, SYN2, SYN3 – Syndrome Bits. These bits originate from the outputs of the syndrome FIFO. They reflect the EDC syndrome bits on any memory read error condition (including reads, read bursts, scrubs, and read modify writes). The syndrome outputs contain valid information whenever the FIFO Flag register's corresponding status bits indicate that the FIFOs are not empty. SYN0 contains the syndrome values for errors in DRAM Bank 0. SYN1 contains the syndrome values for errors in DRAM Bank 1, and so forth.

CB0, CB1, CB2, CB3 – Check Bits. These bits reflect the EDC check bits that were present during the previous read operation. CB0 contains the check bits from DRAM Bank 0 for the most recent read. CB1 contains the check bits from DRAM Bank1 for the most recent read and so forth.

Syndrome FIFO Flag Registers

The Syndrome FIFO Flag registers contain the full/empty status of the syndrome FIFOs. The registers are read only (byte addressable only). When the module is used in a 64-bit bus system the register at address 28 appears on D[7:0] and the register at address 29 appears on D[39:32]. In 32-bit system bus operation the register at address 29 will appear on D[7:0].

Syndrome FIFO flag register 0 (32- & 64-bit system bus)

Index	7 … 4	3	2	1	0
28H	Reserved	FSF2	ESF2	FSF0	ESF0
Default	00 H	0	1	0	1

Syndrome FIFO flag register 1 (64-bit system bus)

Index	39 … 36	35	34	33	32
29H	Reserved	FSF3	ESF3	FSF1	ESF1
Default	00 H	0	1	0	1

Syndrome FIFO flag register 1 (32-bit system bus)

Index	7 … 4	3	2	1	0
29H	Reserved	FSF3	ESF3	FSF1	ESF1
Default	00 H	0	1	0	1

ESF0, ESF1, ESF2, ESF3 – Syndrome FIFO Empty Flags. These bits reflect the EDC syndrome FIFO empty status. When set to 1, these bits indicate that the associated FIFO is empty. ESF0 reflects the status of FIFO 0 which stores the syndrome values from DRAM Bank 0. ESF1 reflects the status of FIFO 1 which stores the syndrome values form DRAM Bank 1 and so forth.

FSF0, FSF1, FSF2, FSF3 – Syndrome FIFO Full Flags. These bits reflect the EDC syndrome FIFO full status. When set to 1, these bits indicate that the associated FIFO is full. FSF0 reflects the status of FIFO 0, which stores the syndrome values form DRAM Bank 0. FSF1 reflects the status of FIFO 1, which stores the syndrome values from DRAM Bank 1 and so forth.

Diagnostic Check Bit Registers

Diagnostic Check Bit Register 0 (32- & 64-bit system bus)

Index	7	6	5	4	3	2	1	0
2C H	–	DCB0						
Default	–	00 H						

Diagnostic Check Bit Register 1 (64-bit system bus)

Index	39	38	37	36	35	34	33	32
2D H	–	DCB1						
Default	–	00 H						

Diagnostic Check Bit Register 1 (32-bit system bus)

Index	7	6	5	4	3	2	1	0
2D H	–	DCB1						
Default	–	00 H						

DCB0, DCB1: Check Bit Register – Write only. These bits can be written to override the check bits generated by the write polynomial generator. In a 64-bit system bus configuration, the register at address 2C appears on D[7:0] and the register at address 2D appears on D[39:32]. When used in a 32-bit system bus, the register at address 2D will appear on D[7:0]. Data written into Diagnostic Check Bit register 0 will write into the check bits for DRAM Banks 0 and 2. Data written into Diagnostic Check Bit register 1 will write into the check bits for DRAM Banks 1 and 3. The selection to use EDC computed from the write data or use the EDC as contained in this register is determined by bit WC in the Command register 1.

Error Status Registers – CYM7264

Table 31. Data Path Register Map for CYM7264

Index	Name	R/W	31:24	23:16	15:8	7:0
24 H	EDC Register 0	R		CB0		SYN0
25 H	EDC Register 1	R		CB1		SYN1
26 H	Reserved					
27 H	Reserved					
28 H	Syndrome FIFO Flags 0	R				FL0
29 H	Syndrome FIFO Flags 1	R				FL1
2A H	Reserved					
2B H	Reserved					
2C H	Diagnostic Check Bit 0	W				DCB0
2D H	Diagnostic Check Bit 1	W				DCB1
2E H	Reserved					
2F H	Reserved					

EDC Registers

The EDC Registers contain the Read Error Log FIFO and Check Bits fields. The registers are Read Only. These registers will appear in D[31:0] of the system data bus as shown in *Table 31*.

EDC Register 0

Index	31	24	23	16	15	8	7	0
24 H			CB0				SYN0	
Default	Undefined		00 H		Undefined		Undefined	

EDC Register 1

Index	31	24	23	16	15	8	7	0
25 H			CB1				SYN1	
Default	Undefined		00 H		Undefined		Undefined	

SYN0, SYN1 – Syndrome Bits. These bits reflect the EDC syndrome bits on an error condition. SYN0 contains the syndrome values for errors in DRAM Bank 0. SYN1 contains the syndrome values for errors in DRAM Bank 1.

CB0, CB1 – Check Bits. These bits reflect the EDC check bits that were present during the previous read operation. CB0 contains the check bits read from DRAM Bank 0. CB1 contains the check bits read from DRAM Bank 1.

Syndrome FIFO Flag Registers

Syndrome FIFO Flag Register 0

Index	7	6	5	4	3	2	1	0
28 H	Reserved						FSF0	ESF0
Default	01 H						0	1

Syndrome FIFO Flag Register 1

Index	7	6	5	4	3	2	1	0
29 H	Reserved						FSF1	ESF1
Default	01 H						0	1

ESF0, ESF1 – Syndrome FIFO Empty Flags. These bits reflect the EDC syndrome FIFO Empty status. When set to 1, these bits indicate that the associated FIFO is empty. ESF0 is the flag for Syndrome FIFO 0 and ESF1 is the flag for Syndrome FIFO 1.

FSF0, FSF1 – Syndrome FIFO Full Flags. These bits reflect the EDC syndrome FIFO full status. When set to 1, these bits indicate that the associated FIFO is full. FSF0 is the flag for Syndrome FIFO 0 and FSF1 is the flag for Syndrome FIFO 1.

Diagnostic Check Bit Registers

Diagnostic Check Bit Register 0

Index	7	6	5	4	3	2	1	0
2C H	DCB0							
Default	00 H							

Diagnostic Check Bit Register 1

Index	7	6	5	4	3	2	1	0
2D H	DCB1							
Default	00 H							

DCB0, DCB1 – Check Bit Register. These bits can be written to override the check bits generated by the write polynomial register. Data in DCB0 is written to DRAM Bank 0 and data in DCB1 is written to DRAM Bank 1. The selection to use EDC computed from the write data or use the EDC as contained in this register is determined by bit WC in the Command register Byte 1.

Silicon Revision Code – Read Only

Index	7	6	5	4	3	2	1	0
30 H					REV[3:0]			

REV[3:0] – Silicon Revision. This field gives the revision number of the module's address controller chip.

$\overline{\text{BERR}}$ Control Register – Write Only

Index	7	6	5	4	3	2	1	0
31 H							BEM	BEC

This register controls operation of the $\overline{\text{BERR}}$ output for data parity errors.

BEM – Data Bus Error Mode. When BEM is set, $\overline{\text{BERR}}$ remains asserted till explicitly cleared (when reporting data parity errors). Otherwise $\overline{\text{BERR}}$ is asserted for one clock only.

BEC – Clear Data Bus Error. This bit, when asserted, clears $\overline{\text{BERR}}$ when MBE (above) is set.

There are two BERR registers in the CYM7232 and two in the CYM7264. These locations on the data bus depend on the bus configuration as follows:

CYM7232
- 32-Bit Bus mode – Registers programmed simultaneously at D[7:0]
- 64-Bit Bus mode – Registers located at D[39:32], D[7:0]

CYM7264
- 64-Bit Bus mode – Registers programmed simultaneously at D[7:0]

All registers appear at the same address, 31H.

Interrupt Status Register

Index	7	6	5	4	3	2	1	0
32 H	–	IC	DBE	ABE	MEW	UEW	DEW	SBW
Default	0	0	0	0	0	0	0	0

IC – Initialization Complete. This bit indicates initialization of the DRAM is complete.

DBE – Data Parity Error. This bit indicates that a data bus parity error has occurred over the system bus.

ABE – Address Parity Error. This bit indicates that an address bus parity error has occurred over the system bus.

MEW – Multiple Errors in a Read-Modify-Write. This bit indicates that multiple errors have occurred during a read-modify-write operation.

UEW – Uncorrectable Error in a Word. This bit indicates that an uncorrectable error has occurred in a 32- (64-) bit word.

DEW – Double Error in a Word. This bit indicates that a double bit error has occurred in a 32- (64-)bit word.

SBW – Single Correctable Error. This bit indicates that a single correctable error has occurred in a 32- (64-) bit word.

Interrupt Status register bits ISR[6:0] are latched. Interrupts[5:0] can be cleared individually by writing the register with the desired bit high. Otherwise those status bits remain indefinitely, or until $\overline{\text{RSTIN}}$ is asserted LOW.

Special Characteristics of I/O Registers

The two EDC registers can be accessed with 32-bit reads over the system bus. All other I/O registers must be accessed by reading or writing a single byte at the address location shown. That byte will always be located at the lowest 8 bits of the system's data bus (D[7:0]). Programming registers are read/write for diagnostic purposes. These register's address locations are separated by 16 bytes to support wide system data paths.

Syndrome Decoding

The following tables give the decoding for the syndrome values for the 32- and 64-bit error detection and correction algorithms. *Table 32* gives the syndrome decoding for the 32-bit error-detection and correction algorithm. *Table 33* gives the syndrome decoding for the 64 bit error detection and correction algorithm. In these two tables, U indicates a multiple (greater than 2) bit uncorrectable error, D indicates a double bit error, nm indicates an error in data bit nm, Cn indicates an error in check bit n, and N indicates no error.

Table 32. Syndrome Decoding, 32-bit EDC

S6 S5 S4 S[3:0]	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
0000	U	D	D	0	D	U	U	D
0001	D	U	U	D	U	D	D	16
0010	D	29	7	D	U	D	D	U
0011	U	D	D	U	D	13	23	D
0100	D	28	6	D	U	D	D	17
0101	U	D	D	1	D	12	22	D
0110	U	D	D	U	D	11	21	D
0111	D	27	5	D	U	D	D	C3
1000	D	26	4	D	U	D	D	U
1001	U	D	D	U	D	10	20	D
1010	31	D	D	U	D	9	19	D
1011	D	25	3	D	15	D	D	C2
1100	U	D	D	U	D	8	18	D
1101	D	24	2	D	U	D	D	C1
1110	D	U	U	D	14	D	D	C0
1111	30	D	D	C6	D	C5	C4	N

Table 33. Syndrome Decoding, 64-bit EDC

S7 S6 S5 S4 S[3:0]	0 0 0 0	0 0 0 1	0 0 1 0	0 0 1 1	0 1 0 0	0 1 0 1	0 1 1 0	0 1 1 1	1 0 0 0	1 0 0 1	1 0 1 0	1 0 1 1	1 1 0 0	1 1 0 1	1 1 1 0	1 1 1 1
0000	N	C4	C5	D	C6	D	D	62	C7	D	D	46	D	U	U	D
0001	C0	D	D	14	D	U	U	D	D	U	U	D	U	D	D	30
0010	C1	D	D	U	D	34	56	D	D	50	40	D	U	D	D	U
0011	D	18	8	D	U	D	D	U	U	D	D	U	D	2	24	D
0100	C2	D	D	15	D	35	57	D	D	51	41	D	U	D	D	31
0101	D	19	9	D	U	D	D	63	U	D	D	47	D	3	25	D
0110	D	20	10	D	U	D	D	U	U	D	D	U	D	4	26	D
0111	U	D	D	U	D	36	58	D	D	52	42	D	U	D	D	U
1000	C3	D	D	U	D	37	59	D	D	53	43	D	U	D	D	U
1001	D	21	11	D	U	D	D	U	U	D	D	U	D	5	27	D
1010	D	22	12	D	33	D	D	U	49	D	D	U	D	6	28	D
1011	17	D	D	U	D	38	60	D	D	54	44	D	1	D	D	U
1100	D	23	13	D	U	D	D	U	U	D	D	U	D	7	29	D
1101	U	D	D	U	D	39	61	D	D	55	45	D	U	D	D	U
1110	16	D	D	U	D	U	U	D	D	U	U	D	0	D	D	U
1111	D	U	U	D	32	D	D	U	48	D	D	U	D	U	U	D

MBus Operation

Bus Transactions General Description

System transactions follow the MBus specification January 31st, 1991, Revision 1.2 (Review draft) including Level 2. Only those functions required of a main memory system are implemented. The generic interface is an extension of the MBus specification adapted to a variety of processors. The descriptions of the generic interface are therefore applicable to MBus applications. The intent of this section is not to repeat the MBus specification but to identify those operating characteristics and functions which are invoked with the MBus mode selection.

Module Connections

The SPARC MBus is an address/data multiplexed bus therefore, the address and data pins of the module must be wired together. The controller accommodates the multiplexed bus by storing the address and control information that is presented during the address phase allowing the data on the address pins to change after the deassertion of the address strobe. The module connections to MBus are given in the following tables. Note that some module pins are tied together to the MBus connection. Other connections must be permanently tied to a HIGH or LOW level.

Table 34. MBus Signal Translation

Controller	MBus
CLK	CLK
D[63:0]	MAD[63:0]
A[35:0]	MAD[35:0]
TYPE[3:0]	MAD[39:36]
SIZE[2:0]	MAD[42:40]
$\overline{AS}$	$\overline{MAS}$
$\overline{BACK}$[1]	$\overline{MRDY}$
$\overline{INH}$	$\overline{MIH}$
$\overline{BR}$	$\overline{MBR}$
$\overline{BG}$	$\overline{MBG}$
$\overline{BB}$	$\overline{MBB}$
ID[3:0]	ID[3:0]
$\overline{BERR}$ (Optional)	$\overline{AERR}$
$\overline{RSTIN}$	$\overline{RSTIN}$
$\overline{INT}$	$\overline{INTOUT}$
$\overline{UERR}$	$\overline{MERR}$

Table 35. Extra Signals in MBus

Controller	MBus
IMD	0 (MBus mode)
TYPE[5:4]	0 (Ignored)
SIZE[7:3]	0
$\overline{DS}$	0
$\overline{BLST}$	1
TSTE	1
PMD[2:0]	(Optional)
$\overline{TRC}$	Tied high for non-reflective memory Tied to $\overline{INH}$ for reflective memory

During reset, $\overline{BACK}$[1:0] and $\overline{UERR}$ must be driven to invoke the proper MBus modes. The snoop window source can originate internally. To make these selections, $\overline{UERR}$ and $\overline{BACK}$[1:0] must be driven to binary 100 during Reset. Refer to *Table 18* and *Table 19*.

Bus Interface Signal Description

The bus interface signal descriptions are identical to that given in the generic descriptions except for some minor variations and nomenclature. This section will present only those differences and highlight the nomenclature equivalences.

Transaction Specific Control

Transaction specific control information is contained in fields within the address as specified by MBus. These fields are given in *Table 36.*

Table 36. Multiplexed Bus Address Subfields

Signal Name	Physical Signal	Description
A[35:0]	MAD[35:0]	Physical Address
TYPE[3:0]	MAD[39:36]	Transaction Type
SIZE[2:0]	MAD[42:40]	Transaction Data Size
	MAD[63:43]	Reserved

Parity

Parity is not defined for MBus, however, the controller retains the capability to generate and check parity when configured for MBus.

TYPE[2:0]: Transaction Type

During the address phase, TYPE[2:0] specify the transaction type. TYPE[2:0] are multiplexed bus signals and are directly MBus compatible. The module fully responds to Write, Read, Coherent Read, Coherent Write and Invalidate, and Coherent Read and Invalidate. The response to Coherent Invalidate cycles is programmable. If the Coherent Invalidate Acknowledge Enable in the Command register is 0, the module makes no response to these cycles. This is the default condition after reset. If the Coherent Invalidate Acknowledge Enable in the Command register is 1, the module asserts $\overline{MRDY}$ for Coherent Invalidate cycles but, otherwise, plays no role in the transaction.

Table 37. Transaction Types

Type			Data Size	Transaction Site
2	1	0		
0	0	0	Any	Write
0	0	1	Any	Read
0	1	0	32 Bytes	Coherent Invalidate
0	1	1	32 Bytes	Coherent Read
1	0	0	Any	Coherent Write & Invalidate
1	0	1	32 Bytes	Coherent Read & Invalidate
All Other Combinations				Reserved

TYPE[2:0]: Transaction Size

During the address phase, SIZE[2:0] specify the number of bytes to be transferred during the data phase of the bus transaction. SIZE[2:0] are multiplexed bus signals and are directly MBus compatible.

Table 38. Size Transaction

Size2	Size1	Size0	Transaction Size
0	0	0	Byte
0	0	1	Halfword (2 Bytes)
0	1	0	Word (4 Bytes)
0	1	1	Doubleword (8 Bytes)
1	0	0	16-Byte Burst
1	0	1	32-Byte Burst
1	1	0	64-Byte Burst
1	1	1	128-Byte Burst

Table 39. Address Interpretation in Byte Mode (Size[2:0]=0)

A2	A1	A0	Byte#	Bits
0	0	0	0	D[63:56]
0	0	1	1	D[55:48]
0	1	0	2	D[47:40]
0	1	1	3	D[39:32]
1	0	0	4	D[31:24]
1	0	1	5	D[23:16]
1	1	0	6	D[15:8]
1	1	1	7	D[7:0]

Table 40. Address Interpretation in Halfword mode (Size[2:0]=1)

A2	A1	A0	Halfword#	Bits
0	0	X	0	D[63:48]
0	1	X	1	D[47:32]
1	0	X	2	D[31:16]
1	1	X	3	D[15:0]

Table 41. Address Interpretation in Word Mode (Size[2:0]=2)

A2	A1	A0	Word#	Bits
0	X	X	0	D[63:32]
1	X	X	1	D[31:0]

$\overline{BR}$/$\overline{FE}$ – Bus Request. This signal will be issued by the controller during reflective read transactions. $\overline{BR}$ from the main memory system should be interpreted as the highest priority request for bus mastership to the system's arbiter. Additional system bus transactions will be prevented until the ongoing write (resulting from the reflective read) to main memory has completed. (The original MBus specification has no explicit mechanism for reflective main memories to postpone the next bus transaction while the data being transferred between two caches is simultaneously written to DRAM.)

In the MBus mode, The BRM bit in Command register 3 should be programmed 0 to enable the bus request handshaking. When this is done, $\overline{BR}$ is deasserted upon the recognition of $\overline{BG}$ and is followed by the assertion of $\overline{BB}$. $\overline{BB}$ remains asserted until the Reflective FIFO is empty.

$\overline{BG}$ – Bus Grant. This signal is asserted by the external arbiter in response to a $\overline{BR}$, to indicate that the controller has been granted ownership of the bus.

$\overline{BB}$ – Bus Busy. This signal is asserted by the controller for the duration of its bus ownership. The controller will require the bus as it completes the main memory write transaction during reflective read operations.

ID[3:0] – Identification. The ID field selects various configuration spaces within the MBus address space for access to the Port register and other I/O registers.

Table 42. ID[3:0] Mapping

MBus CONFIGURATION SPACE	ID[3:0]
F/F000/000 H to F/F0FF/FFFF H	0 H reserved for boot PROM
F/F100/0000 H to F/F1FF/FFFF H	1 H
. .	.
F/Fn00/0000 H to F/Fn00/0000 H	n H
. .	.
F/FE00/0000 H to F/FEFF/FFFF H	E H
F/FF00/0000 H to F/FFFF/FFFF H	F H

Internal Registers

Several internal registers are available to set up the DRAM controller and report status to the host. The register's individual bits are defined in the sections describing the generic mode of operation. The registers appear on the MBus exactly as they would in the 64-bit bus generic mode, big-endian operation.

When the MBus mode is invoked, the MBus Port register becomes accessible. Its form, content, and address are defined below. In addition, the Command register 0 contains a control bit specific to MBus operation. This control bit affects the controllers response to MBus coherent invalidate cycles. Addressing of the internal registers is direct in the MBus mode and therefore the index register is not used. The address of each register has the form (in hexadecimal)

FFnxx0mpx

where n is a nibble that is compared to the input on the ID pins, x is a don't care condition, and mp are the two nibbles of the indexed address as given in the register descriptions. For example, if ID[3:0] is A H, then the MBus address for the $\overline{BERR}$ Register is FFAxx031x H.

MBus Port Register – 2 Bytes – Read Only

Address	7	6	5	4	3	2	1	0
FFF H	MR				MV			
Default	0 H				1 H			

Address	15	14	13	12	11	10	9	8
FFE H	MD							
Default	00 H or 01 H							

MV[3:0] – Vendor Code. This specifies the vendor code for MBus compatible devices – 1 H for Cypress Semiconductor.

Internal Registers (continued)

MR[3:0] – Revision Number. This specifies the revision level for MBus compatible devices – 0 H.

MD[7:0] – Device Number. This specifies a unique number that indicates the vendor specific MBus device present at this port.

00H CYM7232
01H CYM7264

MP[31:16] – Reserved for later use.

Specific Programming

For MBus, there will be specific register programming to configure the controller for MBus operation. For convenience, specific fields are listed below along with the load value appropriate to MBus. There are other programming selections that must be made which are dependent upon the specific application.

VCO[1:0]	10	80-MHz DRAM Clock
SBS	1	64-Bit System Bus

Timing

Bus timing diagrams reflect generic applications, however they are applicable to MBus. All of the diagrams must be interpreted for data strobe, $\overline{DS}$, permanently asserted.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 40°C to +125°C
Supply Voltage ..... – 0.3V to +7.0V
Input Voltage ..... – 3.0V to V_{CC} + 0.3V
Output Voltage ..... 0 to V_{CC} Volts

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CYM7232 CYM7264 Min.	CYM7232 CYM7264 Max.	Unit
V_{CC}	Supply Voltage		4.75	5.25	V
T_{AMB}	Ambient Temperature	Commercial	0	70	°C
V_{OH1}	Output HIGH Voltage Type 1	V_{CC} = Min., I_{OH1} = – 8.0 mA	2.4		V
V_{OH2}	Output HIGH Voltage Type 2	I_{OH2} = –12 mA	2.4		V
V_{OL1}	Output LOW Voltage Type 1	V_{CC} = Min., I_{O1L} = 8.0 mA		0.4	V
V_{OH2}	Output LOW Voltage Type 2	I_{OH2} = 12 mA		0.4	V
V_{IH}	Input HIGH Voltage		2.4	V_{CC}+0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.8	V
I_{IN}	Input Leakage Current	V_{CC} = Max., 0 ≤ V_{IN} ≤ V_{SS}		+10	µA
I_{OUT}	Output Leakage Current	V_{CC} = Max., V_{SS} ≤ V_{OUT} ≤ V_{CC}		+10	µA
I_{CC}	Operating Current	Outputs Open, f = f_{MAX}		300	mA

Capacitance

Parameter	Description	Test Conditions	Max.	Unit
C	Capacitance, In, Out, I/O	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	20	pF
CLK	Capacitance, Input		30	pF
$C_{\overline{BERR}}$, $C_{\overline{UERR}}$	Capacitance		30	pF

Output Signals by Type

Output	Description
$\overline{BACK}$[1]	Type 2
$\overline{BERR}$	Type 1
$\overline{BR}$/$\overline{FE}$	Type 2
$\overline{BB}$	Type 2
$\overline{INT}$, $\overline{UERR}$	Type 1
$\overline{RAS}$[3:0]	Type 2
$\overline{CAS}$[3:0]	Type 2
ADRS[11:0]	Type 2
DDA, DDB, DDC, DDD	Type 1
EDA, EDB, EDC, EDD	Type 1
R/$\overline{W}$[3:0]	Type 1
DP[7:0]	Type 1
D[63:0]	Type 1

Type 1 outputs are designed to drive 50-pF loads with a DC drive of 8 mA. Type 2 outputs are designed to drive 50-pF loads with a DC drive of 12 mA. MBus modules are tested with 100-pF loads to guarantee compatibility with the MBus specification.

Data and Data Parity Holding Buffers

The system bus data and data parity pins are equipped with holding buffers. These buffers use a weak feedback buffer combined with the input buffer to form a latch. The latch holds the last value driven on the bus.

Holding Buffer DC Characteristics

Holding 0
V_{IN} = 0.4V — I_{IN} = 160 µA (Max.), 45 µA (Min.)

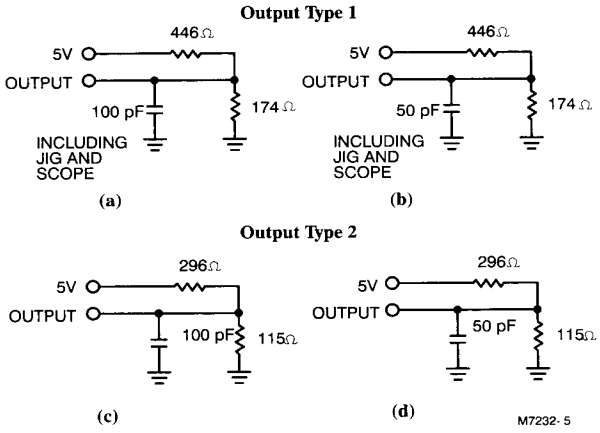
Holding 1
V_{IN} = 2.4V — I_{IN} = − 715 µA (Max.), − 175 µA (Min.)

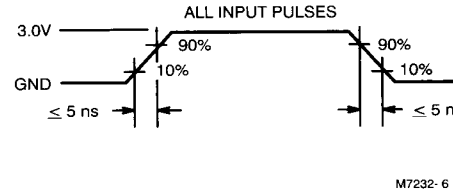
Flipping Current

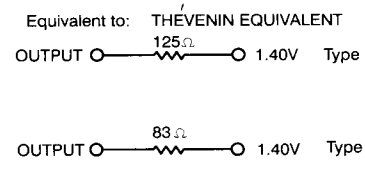
Holding 0
V_{IN} = 2.0V — I_{IN} = 565 µA (Max.)
V_{IN} = 2.4V — I_{IN} = 630 µA (Max.)

Holding 1
V_{IN} = 0.8V — I_{IN} = − 725 µA (Max.)
V_{IN} = 0.4V — I_{IN} = − 730 µA (Max.)

AC Test Loads and Waveforms







AC Timing Characteristics

Description	40/80 MHz		33/66 MHz		25/75 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	
D[63:0], DP[7:0] Output Delay	7	18.5	9	21.5	11	23.5	ns
D[63:0], DP[7:0] Output Hold	3		3.5		3.5		ns
D[63:0], DP[7:0] Input Set-Up	4		5		7		ns
D[63:0], DP[7:0] Input Hold	2.5		2.5		2.5		ns
A[35:0], AP[3:0] Input Set-Up	4		5		7		ns
A[35:0], AP[3:0] Input Hold	2.5		2.5		2.5		ns
TYPE[5:0] Input Set-Up	4		5		7		ns
TYPE[5:0] Input Hold	2.5		2.5		2.5		ns
SIZE[7:0] Input Set-Up	4		5		7		ns
SIZE[7:0] Input Hold	2.5		2.5		2.5		ns
ID[3:0] Input Set-Up	4		5		7		ns
ID[3:0] Input Hold	2.5		2.5		2.5		ns
$\overline{AS}$ Set-Up	4		5		7		ns
$\overline{AS}$ Hold	2.5		2.5		2.5		ns
$\overline{DS}$ Set-Up	4		5		7		ns
$\overline{DS}$ Hold	2.5		2.5		2.5		ns
$\overline{INH}$ Set-Up	4		5		7		ns
$\overline{INH}$ Hold	2.5		2.5		2.5		ns
$\overline{SNW}$ Set-Up	4		5		7		ns
$\overline{SNW}$ Hold	2.5		2.5		2.5		ns
$\overline{TRC}$ Set-Up	4		5		7		ns
$\overline{TRC}$ Hold	2.5		2.5		2.5		ns
$\overline{BG}$ Set-Up	4		5		7		ns
$\overline{BG}$ Hold	2.5		2.5		2.5		ns
$\overline{BR}/\overline{FE}$ Output Delay	7	17.5	9	20.5	11	22.5	ns
$\overline{BR}/\overline{FE}$ Output Hold	3		3.5		3.5		ns
$\overline{BB}$ Output Delay	10	17.5	12	20.5	14	22.5	ns
$\overline{BB}$ Output Hold	3		3.5		3.5		ns
$\overline{BB}$ Input Set-Up	4		5		7		ns
$\overline{BB}$ Input Hold	2.5		2.5		2.5		ns
$\overline{IMD}$ Input Set-Up	10.5		13.5		16.5		ns
$\overline{IMD}$ Input Hold	2.5		2.5		2.5		ns
$\overline{RSTIN}$ Input Set-Up	10.5		13.5		16.5		ns
$\overline{RSTIN}$ Input Hold	5		5		5		ns
$\overline{INT}$ Output Delay	7	18.5	9	21.5	11	23.5	ns
$\overline{INT}$ Output Hold	3		3.5		3.5		ns
$\overline{BERR}$ Output Delay	7	18.5	9	21.5	11	23.5	ns

AC Timing Characteristics (continued)

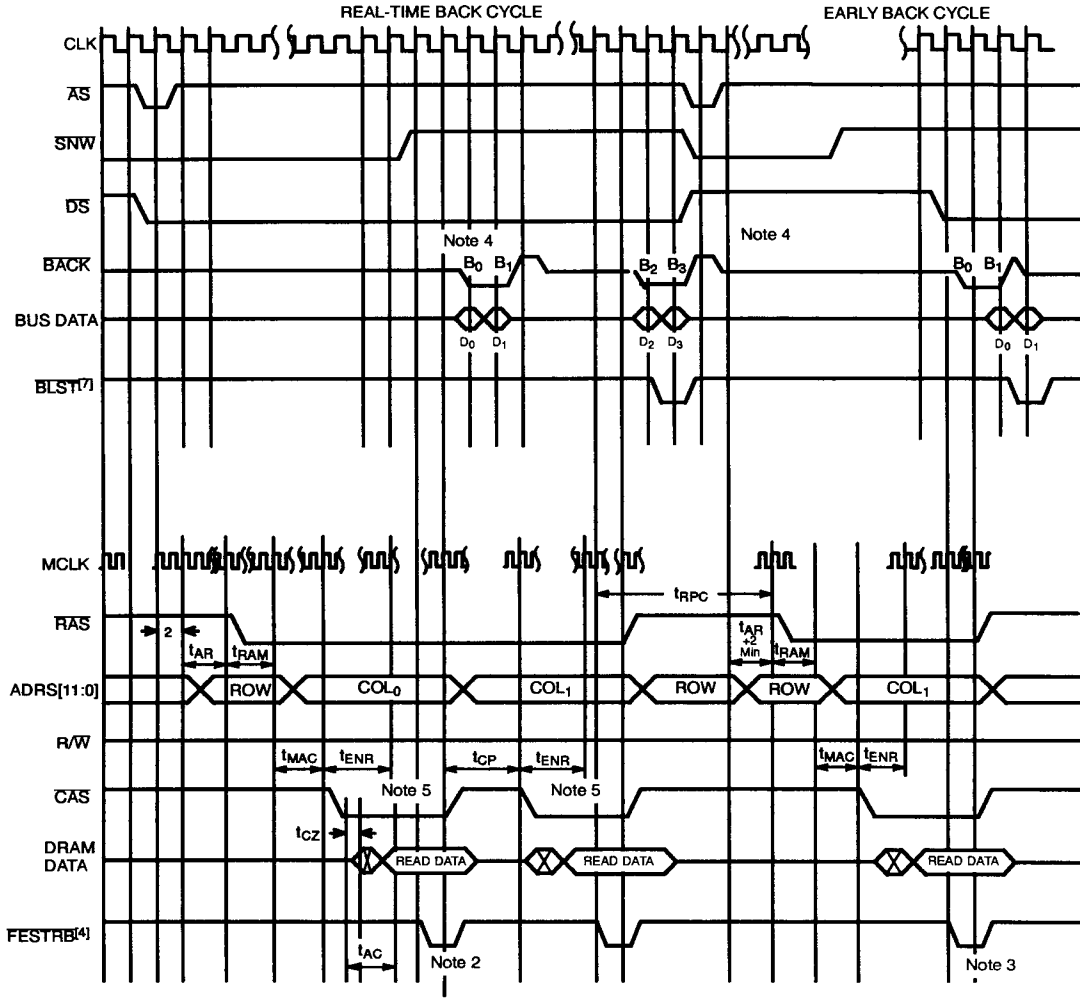
Description	40/80 MHz		33/66 MHz		25/75 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{\text{BERR}}$ Output Hold	3		3.5		3.5		ns
TSTE Input Set-Up	10.5		13.5		16.5		ns
TSTE Input Hold	3		3		3		ns
TSTM Input Set-Up	10.5		13.5		16.5		ns
TSTM Input Hold	3		3		3		ns
$\overline{\text{UERR}}$ Output Delay	7	17.5	9	20.5	11	22.5	ns
$\overline{\text{UERR}}$ Output Hold	3		3.5		3.5		ns
$\overline{\text{UERR}}$ Input Set-Up	7.5		10.5		13.5		ns
$\overline{\text{UERR}}$ Input Hold	2.5		2.5		2.5		ns
$\overline{\text{BACK}}$0 Input Set-Up	4		5		7		ns
$\overline{\text{BACK}}$0 Input Hold	2.5		2.5		2.5		ns
$\overline{\text{BACK}}$0 Output Delay (MBus)		17.5		20.5		22.5	ns
$\overline{\text{BACK}}$0 Output Hold (MBus)	3		3.5		3.5		ns
$\overline{\text{BACK}}$1 Output Delay (Real Time)	9	17.5	11	20.5	13	22.5	ns
$\overline{\text{BACK}}$1 Output Hold (Real Time)	3		3.5		3.5		ns
$\overline{\text{BACK}}$1 Input Set-Up	4		5		7		ns
$\overline{\text{BACK}}$1 Input Hold	2.5		2.5		2.5		ns
$\overline{\text{BACK}}$1 Output Delay (Early)	11	21	13	24	15	26	ns
$\overline{\text{BACK}}$1 Output Hold (Early)	3		3.5		3.5		ns
$\overline{\text{BLST}}$ Input Set-Up	4		5		7		ns
$\overline{\text{BLST}}$ Input Hold	2.5		2.5		2.5		ns
ADRS[11:0] Output Delay	7	16	9	18	11	21	ns
ADRS[11:0] Output Hold	3		3.5		3.5		ns
$\overline{\text{RAS}}$[3:0] Output Delay	7	16	9	18	11	21	ns
$\overline{\text{RAS}}$[3:0] Output Hold	3		3.5		3.5		ns
$\overline{\text{CAS}}$[3:0] Output Delay	7	16	9	18	11	21	ns
$\overline{\text{CAS}}$[3:0] Output Hold	3		3.5		3.5		ns
R/$\overline{\text{W}}$[3:0]/[1:0] Output Delay	7	17.5	9	20.5	11	23.5	ns
R/$\overline{\text{W}}$[3:0]/[1:0] Output Hold	3						ns
DDA[31:0], DDB[31:0], DDC[31:0], DDD[31:0] Output Delay	7	17.5	9	20.5	11	23.5	ns
DDA[31:0], DDB[31:0], DDC[31:0], DDD[31:0] Output Hold	1		3		3		ns
DDA[31:0], DDB[31:0], DDC[31:0], DDD[31:0] Input Set-Up	4		5		7		ns
DDA[31:0], DDB[31:0], DDC[31:0], DDD[31:0] Intput Hold	2.5		2.5		2.5		ns
EDA[6:0], EDB[6:0], EDC[6:0], EDD[6:0] Output Delay	7	17.5	9	20.5	11	23.5	ns
EDA[6:0], EDB[6:0], EDC[6:0], EDD[6:0] Output Hold	1		3		3		ns
EDA[6:0], EDB[6:0], EDC[6:0], EDD[6:0] Input Set-Up	4		5		7		ns
EDA[6:0], EDB[6:0], EDC[6:0], EDD[6:0] Intput Hold	2.5		2.5		2.5		ns
$\overline{\text{BACK}}$[1:0], $\overline{\text{UERR}}$ Input Set-Up During Reset	8		10		12		ns
$\overline{\text{BACK}}$[1:0], $\overline{\text{UERR}}$ Input Hold During Reset	5		5		5		ns

AC Timing Characteristics (continued)

Description	40/80 MHz		33/66 MHz		25/75 MHz		Unit
	Min.	Max.	Min.	Max.	Min.	Max.	
Clock Frequency	20	40	20	33	20	25	MHz
Clock Cycle Time	50	25	50	30	50	40	ns
Clock Rise Time		1.6		1.6		1.6	ns
Clock Fall Time		1.6		1.6		1.6	ns
Clock Symmetry	45	55	45	55	45	55	%
Clock Pulse Width HIGH at 40, 33, and 25 MHz	11	14	13.5	16.5	18	22	ns
Clock Pulse Width LOW at 40, 33, and 25 MHz	11	14	13.5	16.5	18	22	ns
MCLK Frequency	20	80	20	66	20	75	MHz
MCLK Cycle Time	12.5	50	15	50	13.33	50	ns
MCLK Rise Time		1.6		1.6		1.6	ns
MCLK Fall Time		1.6		1.6		1.6	ns
MCLK Symmetry	45	55	45	55	45	55	%
MCLK Pulse Width HIGH at 80, 66, and 75 MHz)	5.5	7	6.5	8.5	6	7.5	ns
MCLK Pulse Width LOW at 80, 66, and 75 MHz)	5.5	7	6.5	8.5	6	7.5	ns
MCLK/CLK Skew	− 1.5	0	− 1.5	0	− 1.5	0	ns

Switching Waveforms

Read

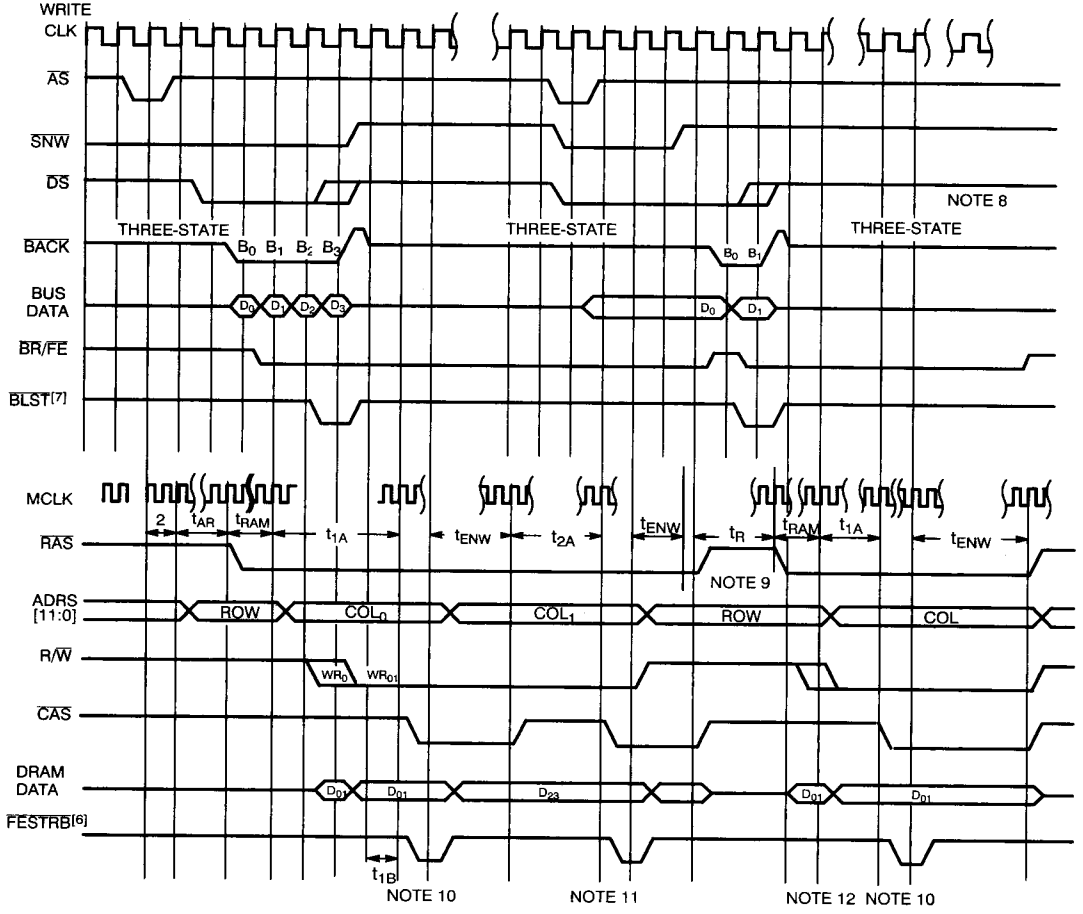


Notes:

2. $\overline{\text{FESTRB}}$ is asserted here following the closure of the snoop window in the previous clock cycle.
3. $\overline{\text{FESTRB}}$ would normally occur after t_{ENR} plus a delay if necessary to align $\overline{\text{FESTRB}}$ to a bus clock boundary. $\overline{\text{FESTRB}}$ is asserted here following the assertion of $\overline{\text{DS}}$ (data strobe) in the previous clock cycle.
4. $\overline{\text{BACK}}$ remains three-stated until it is first asserted. At the middle and end of the transaction, $\overline{\text{BACK}}$ is deasserted in the first half of the clock cycle and then three-stated.
5. $\overline{\text{FESTRB}}$ would normally occur here after t_{ENR}, however, it is automatically delayed by the controller to align to a bus clock boundary.

Switching Waveforms (continued)

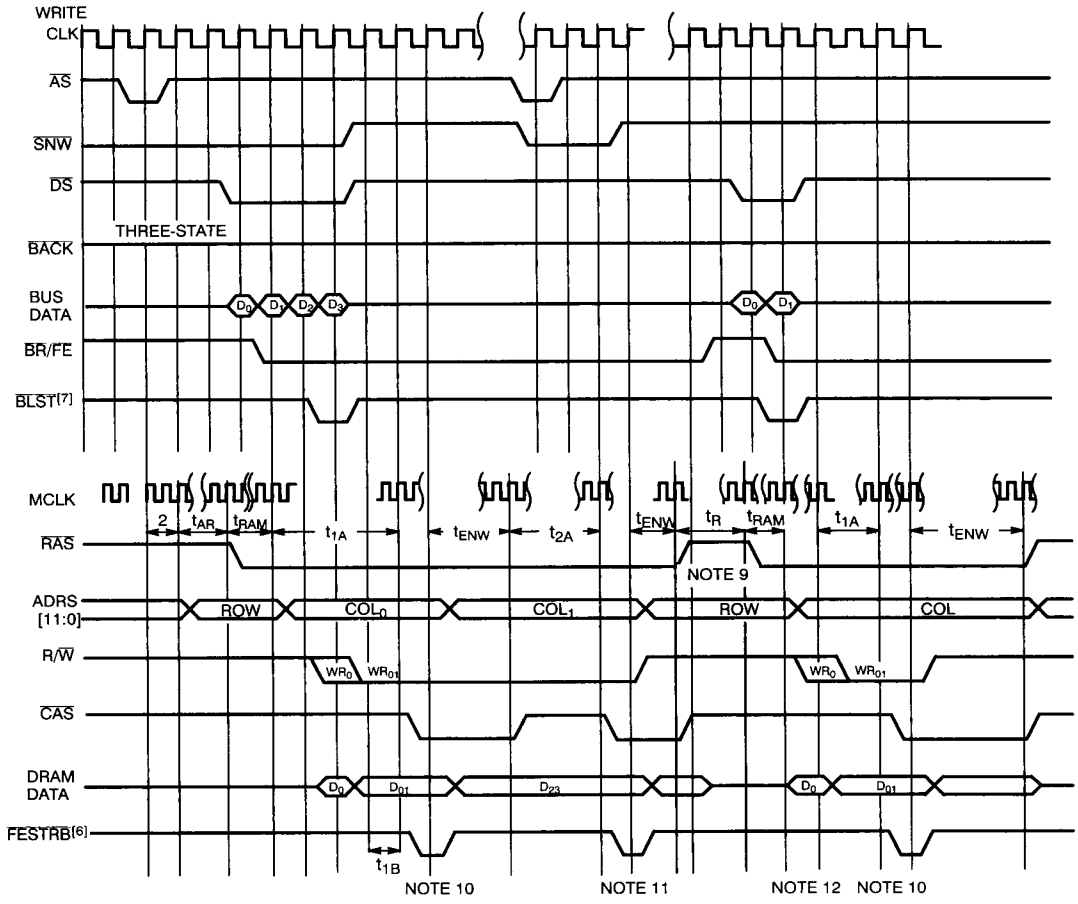
Write – Real-Time Bus Acknowledge/Early Data Strobe



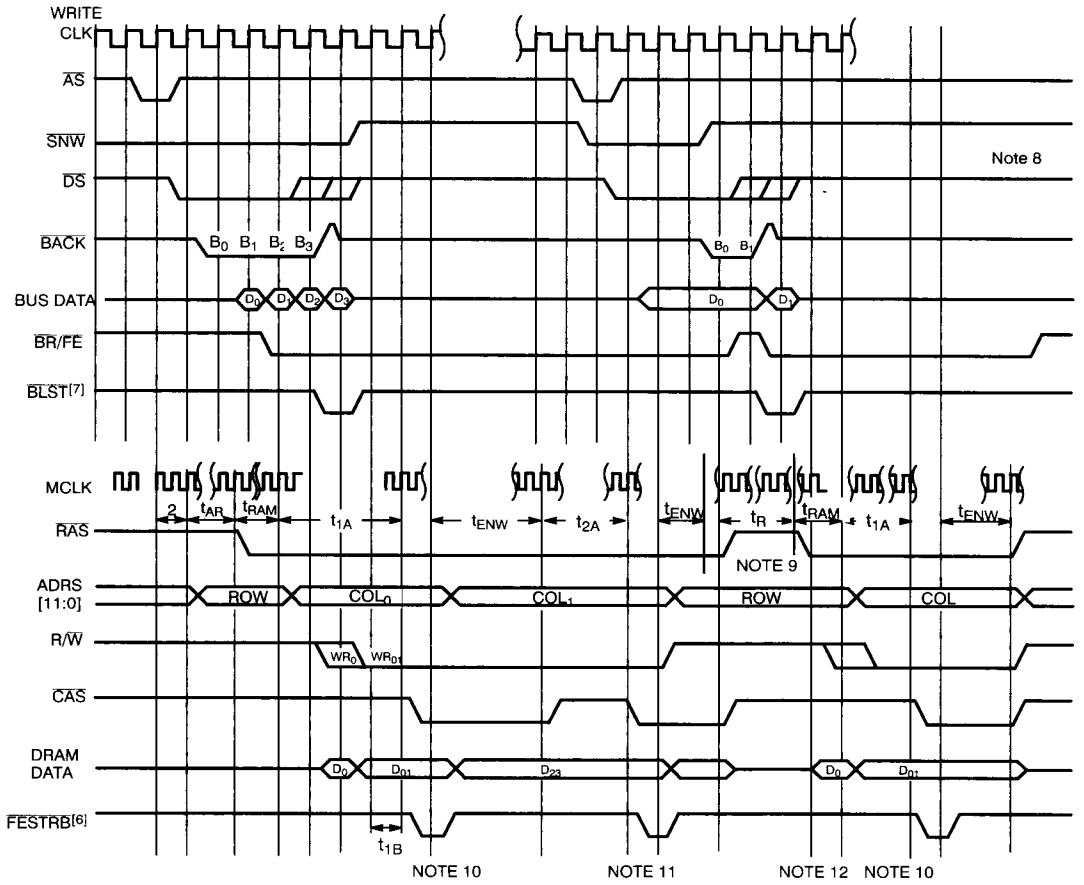
Notes:

6. $\overline{\text{FESTRB}}$ is an internal signal that unclocks the FIFO. $\overline{\text{FESTRB}}$ is one bus clock cycle long.
7. $\overline{\text{BLST}}$ may be internal or external
8. $\overline{\text{DS}}$ may be deasserted in any of the cycles shown.
9. $t_R \geq t_{RPC} + 2$ MCLK
   $t_R \geq t_{AR} + 2$ MCLK
10. The assertion of $\overline{\text{CAS}}$ requires
    t_{CP} to have expired (from previous transaction)
    t_{MAC} have expired ($t_{1A} \geq t_{MAC}$)
    t_{DC} to have expired ($t_{1B} \geq t_{DC}$)
    $\overline{\text{SNW}}$ to have closed 2 bus clocks previous.
11. The assertion of $\overline{\text{CAS}}$ (and all subsequent $\overline{\text{CAS}}$ cycles of the burst) requires
    t_{DC} to have expired
    t_{CP} to have expired ($t_{2A} > t_{CP}$)
    After $\overline{\text{CAS}}$ asserted, $\overline{\text{FESTRB}}$ unclocks the write FIFO presenting the next data page to the DRAM.
12. t_{1A} is measured from the rising edge of the bus clock after t_{RAM} has expired.

Switching Waveforms (continued)
Write – Real-Time Data Strobe

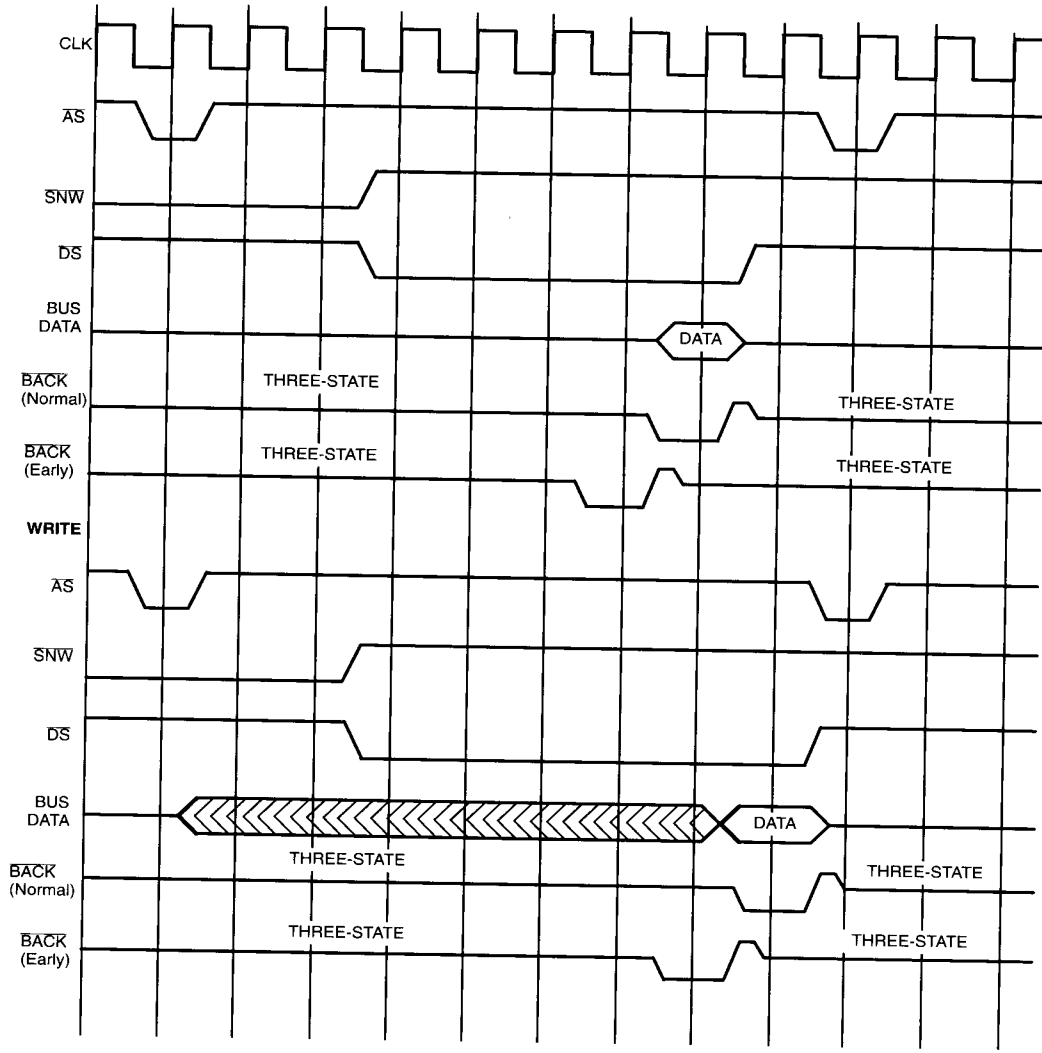


Switching Waveforms (continued)
Write – Early Bus Acknowledge



Switching Waveforms (continued)

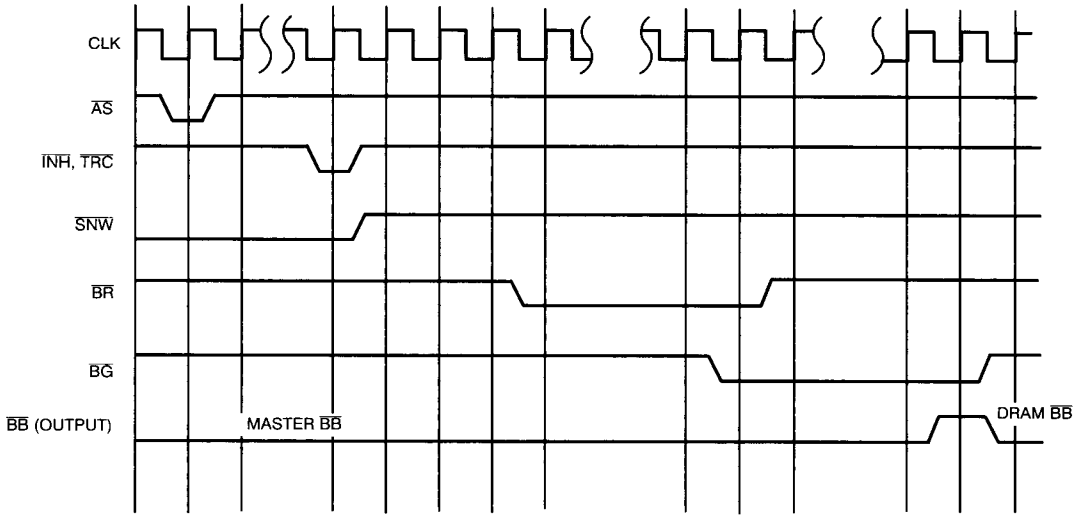
I/O Cycles – Read[13]



Note:
13. Data transfer occurs 5 clock cycles after $\overline{SNW}$ or $\overline{DS}$ whichever occurs last.

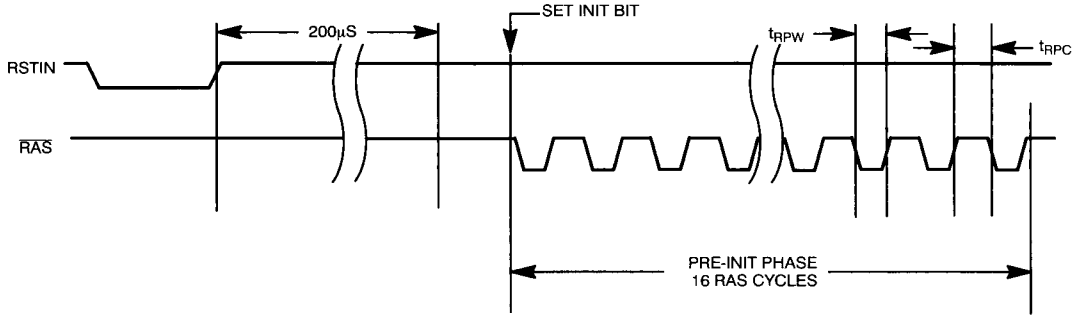
Switching Waveforms (continued)

Arbitration for Bus Mastership During Reflective Read

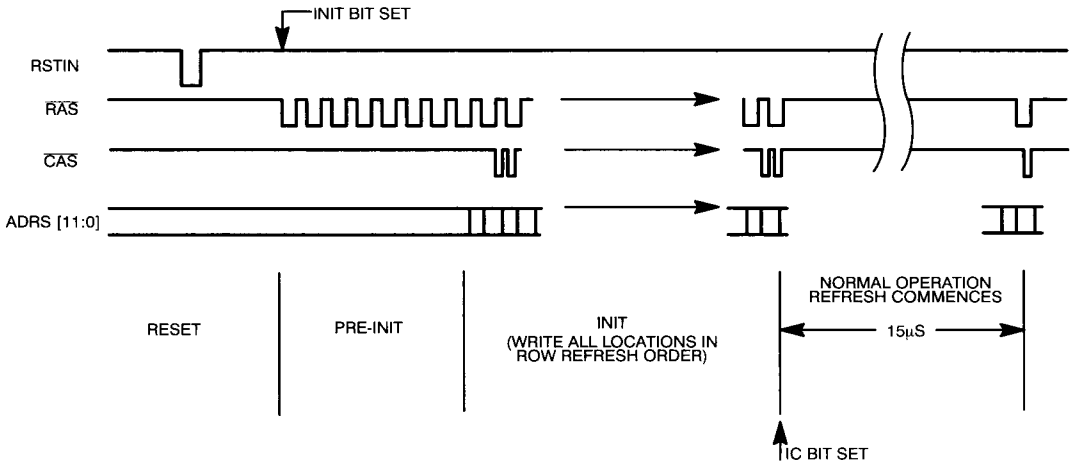


Switching Waveforms (continued)

Pre-initialization



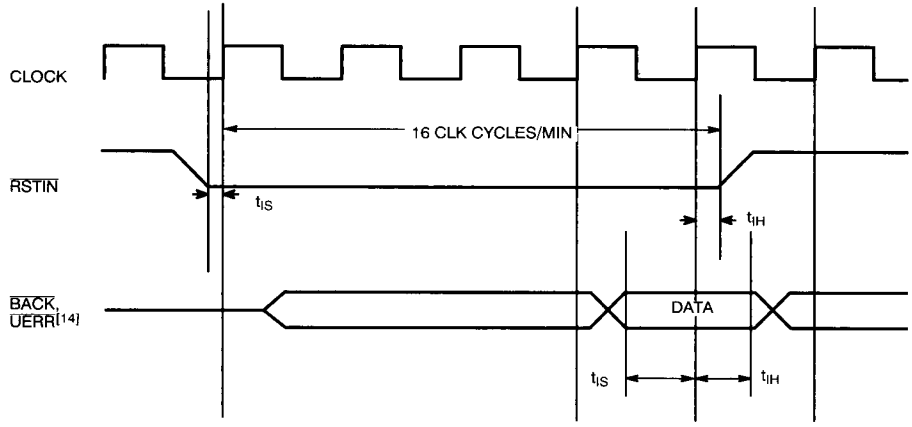
Initialization



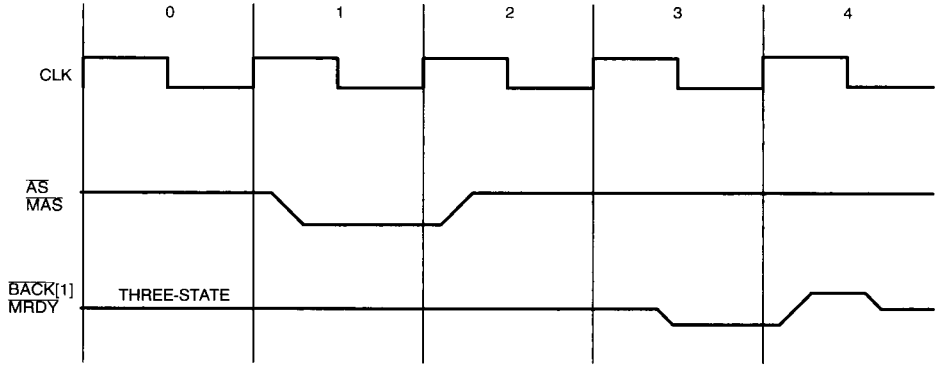
8 MODULES

Switching Waveforms (continued)

Reset Cycle



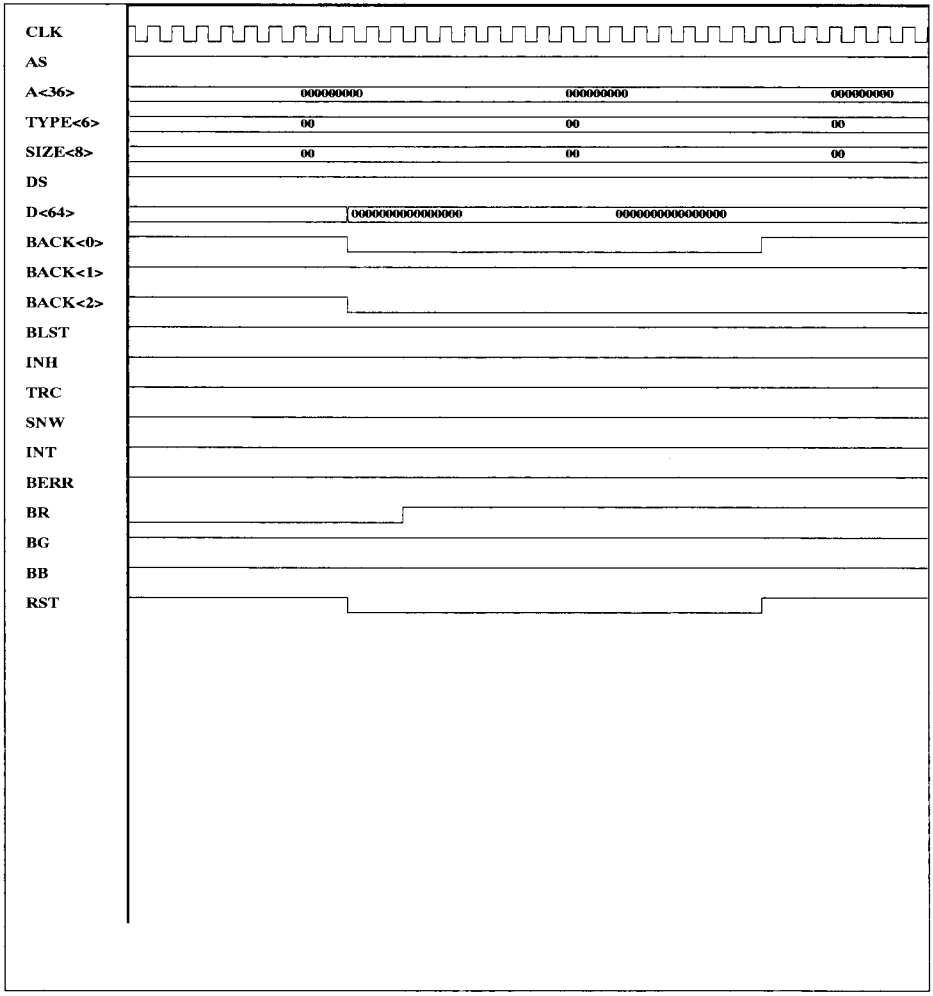
MBus Coherent Invalidate Cycle (CIE set)



Note:
14. BACK and UERR used as input to select bus acknowledge modes and snoop window source during reset.

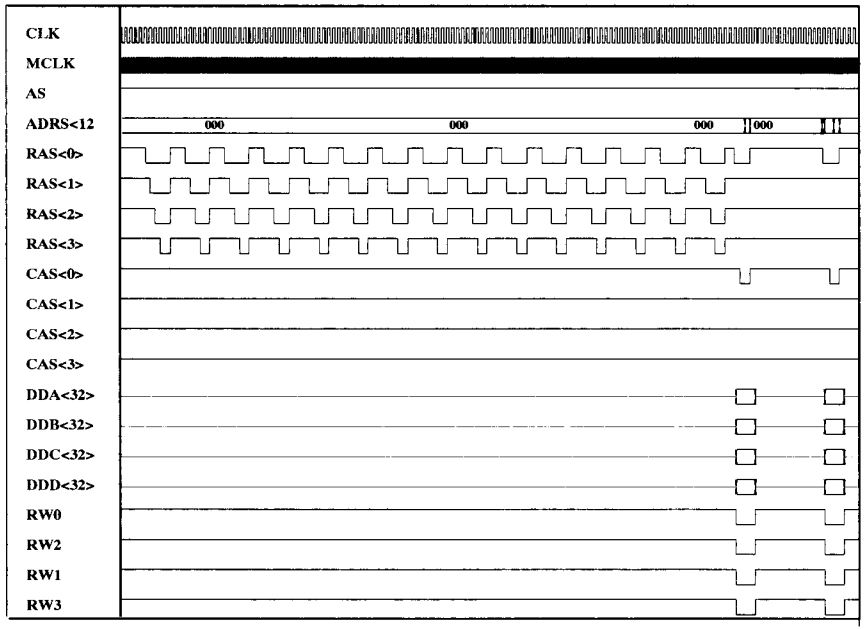
Timing Diagrams

RESET Invoking Mode 10, External Snoop Window

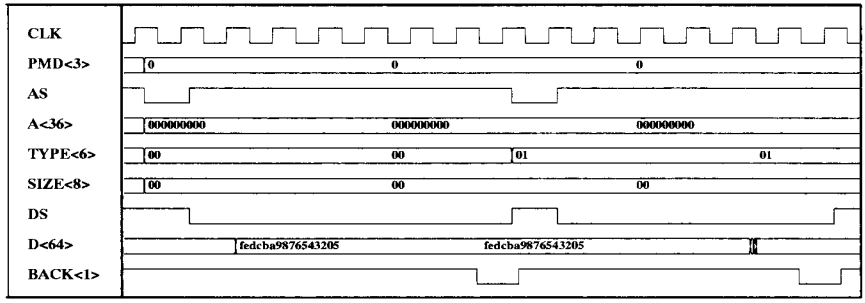


Timing Diagrams (continued)

Preinit Followed by Start of DRAM Init

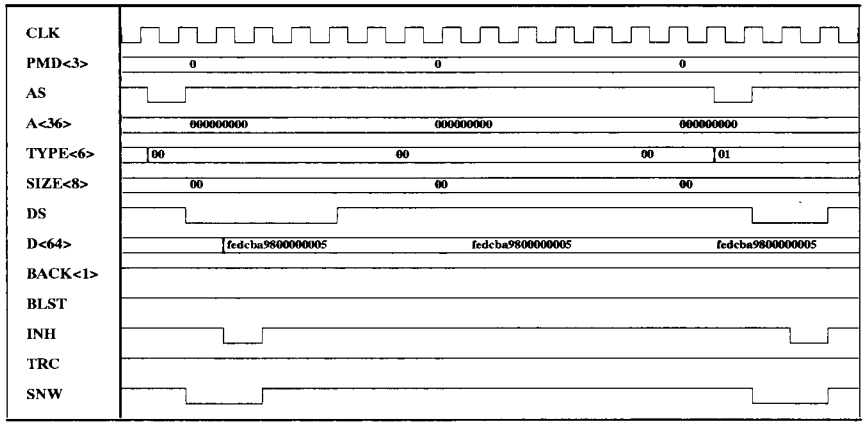


I/O Write Followed by Read, Mode 01

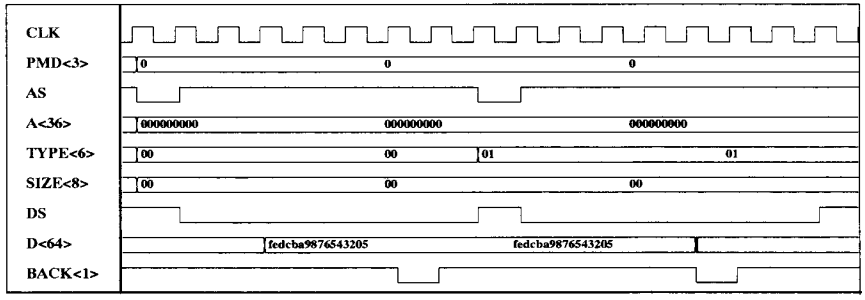


Timing Diagrams (continued)

I/O Write Inhibited Follwed by Read Inhibited



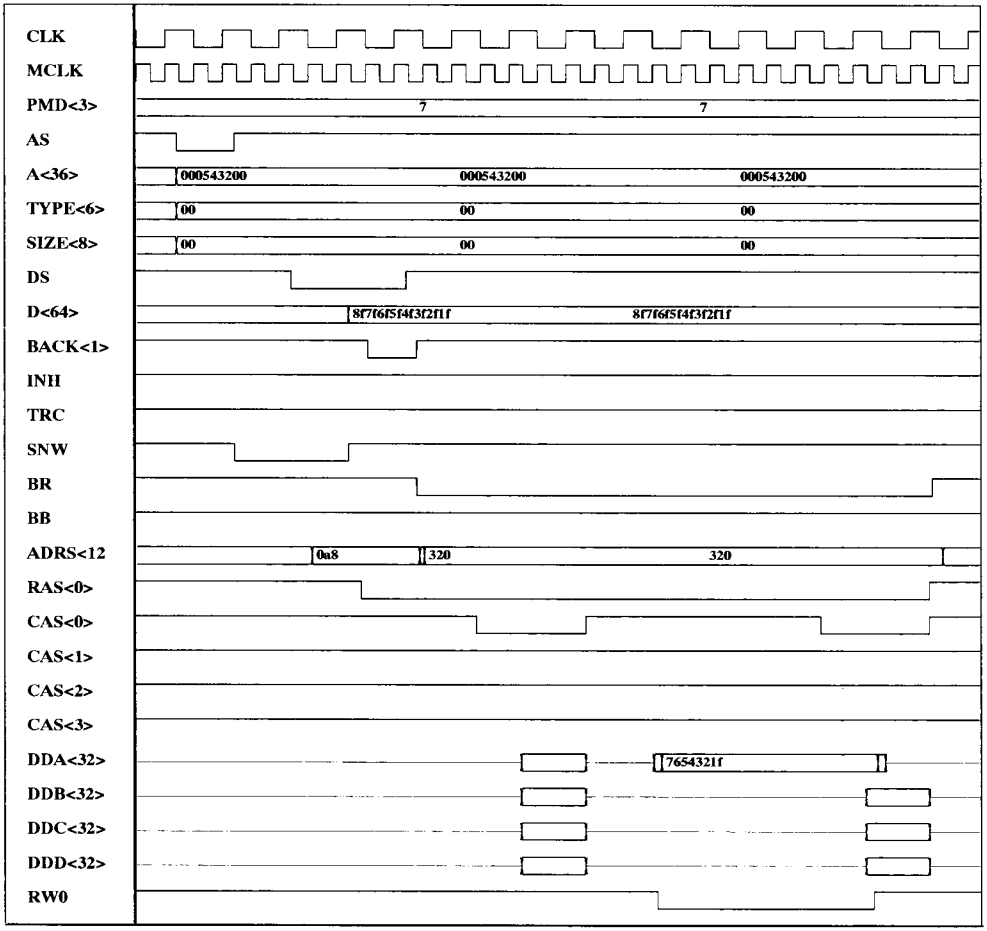
I/O Write Followed by Read, Mode 11



8 MODULES

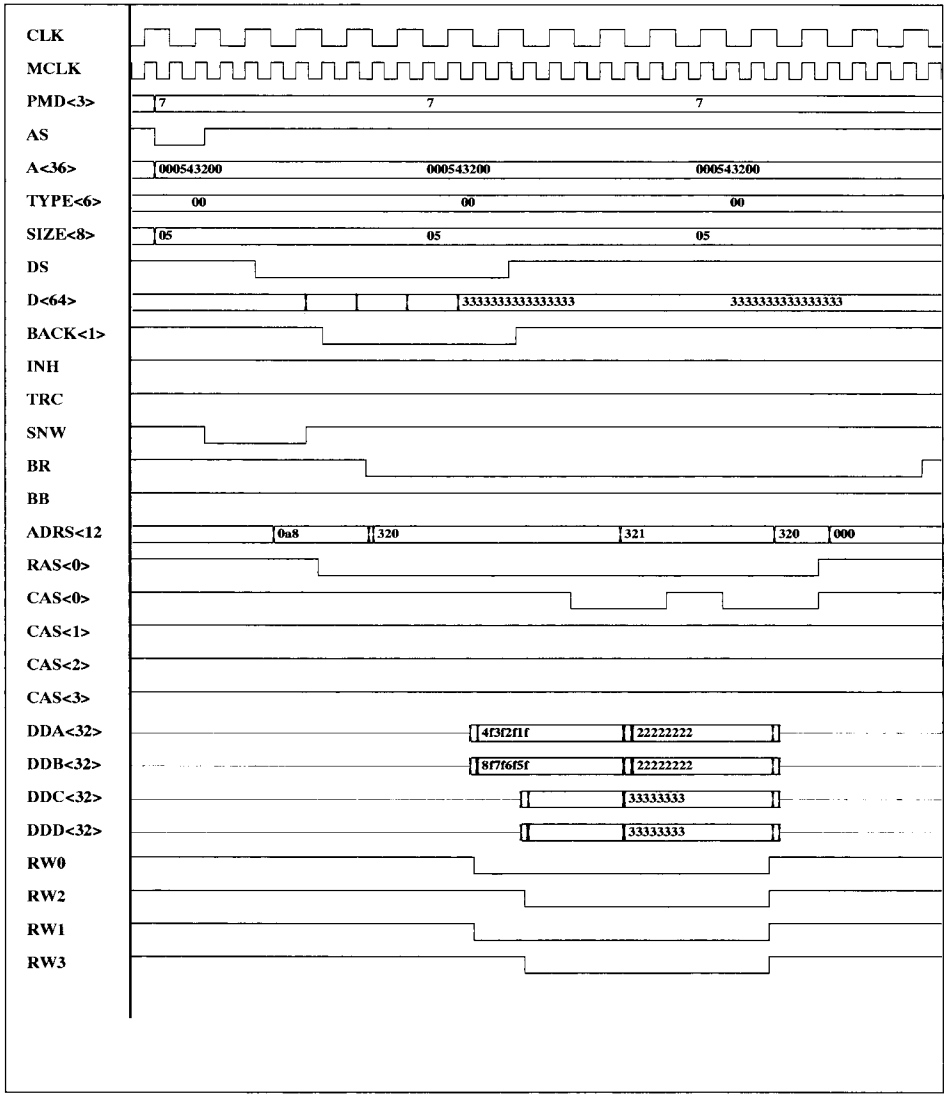
Timing Diagrams (continued)

Read-Modify-Write Mode 01



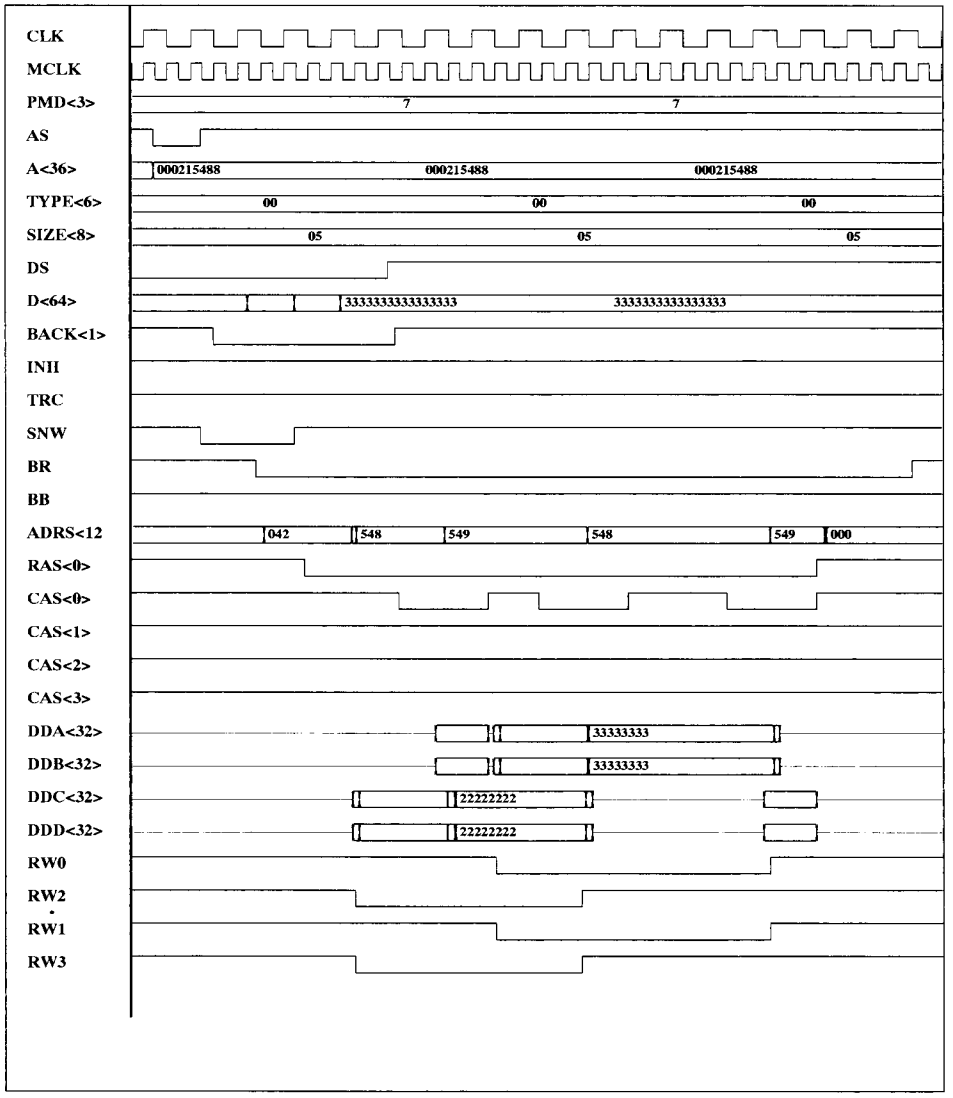
Timing Diagrams (continued)

Write Mode 01, Sequential, 32 Bytes



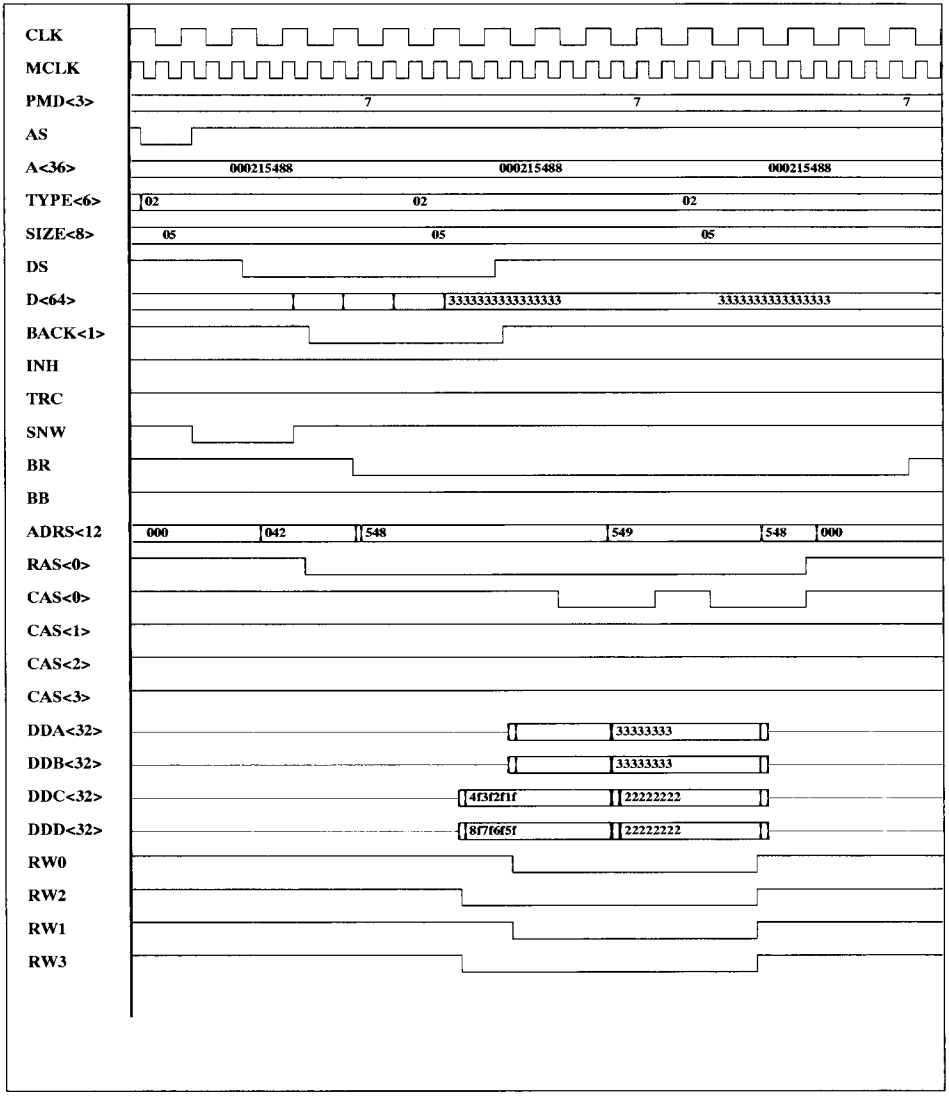
Timing Diagrams (continued)

Write Mode 01, Sequential, Misaligned, 32 Bytes



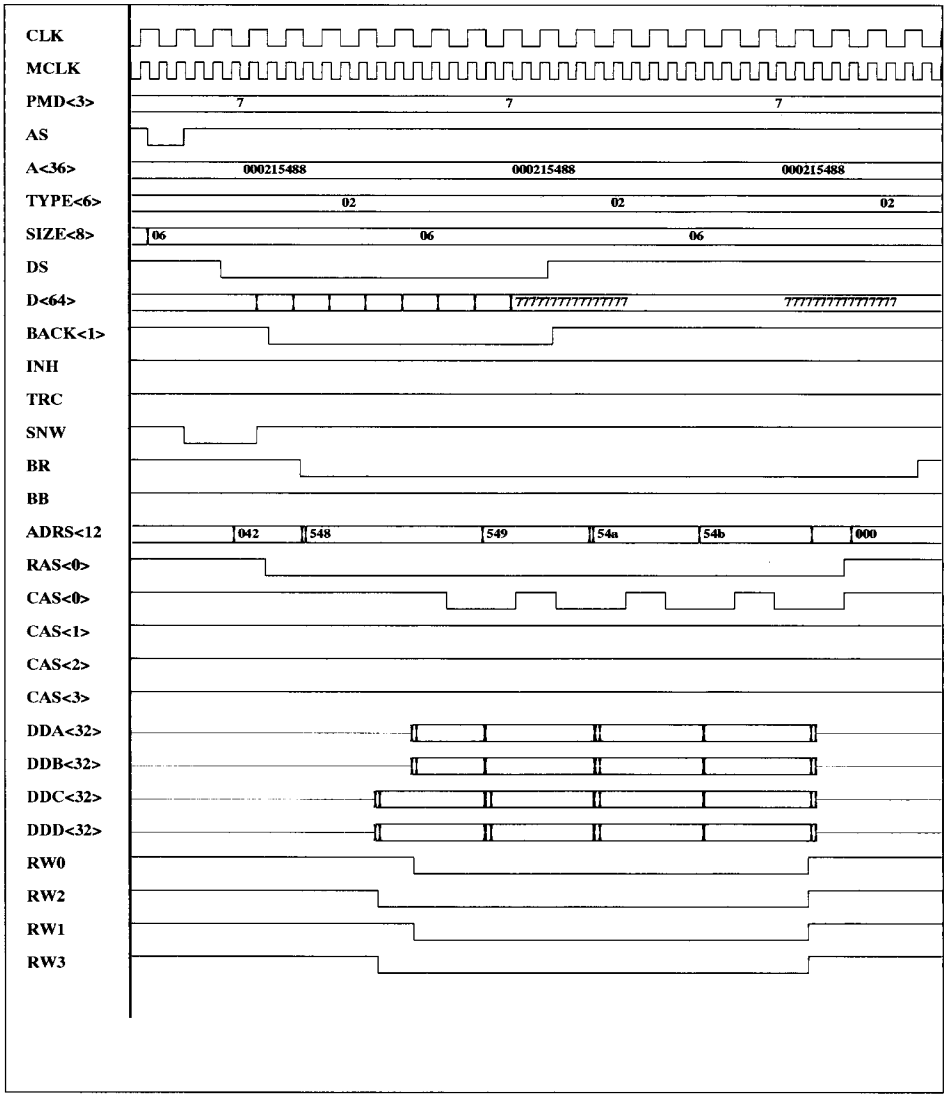
Timing Diagrams (continued)

Write Mode 01, Intel, Misaligned



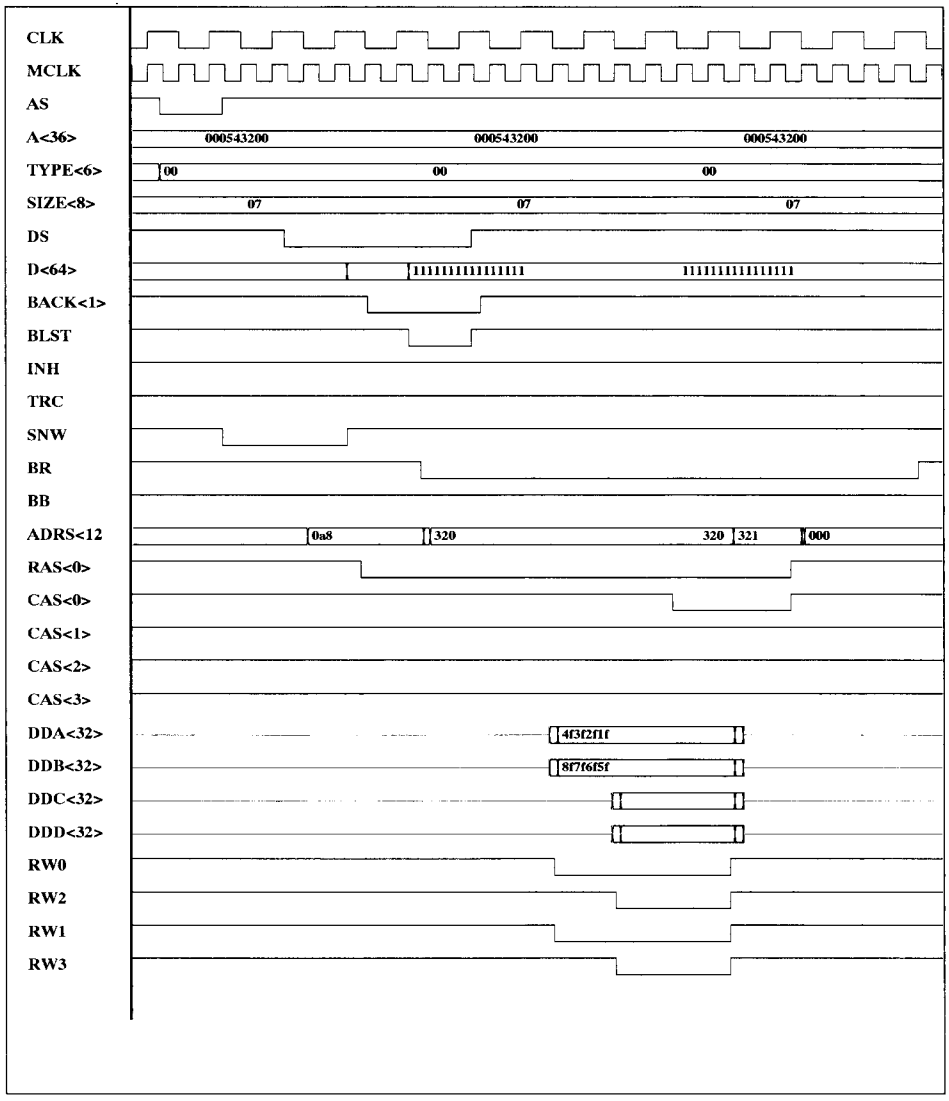
Timing Diagrams (continued)

Write Mode 01, Intel, Misaligned, 64 Bytes



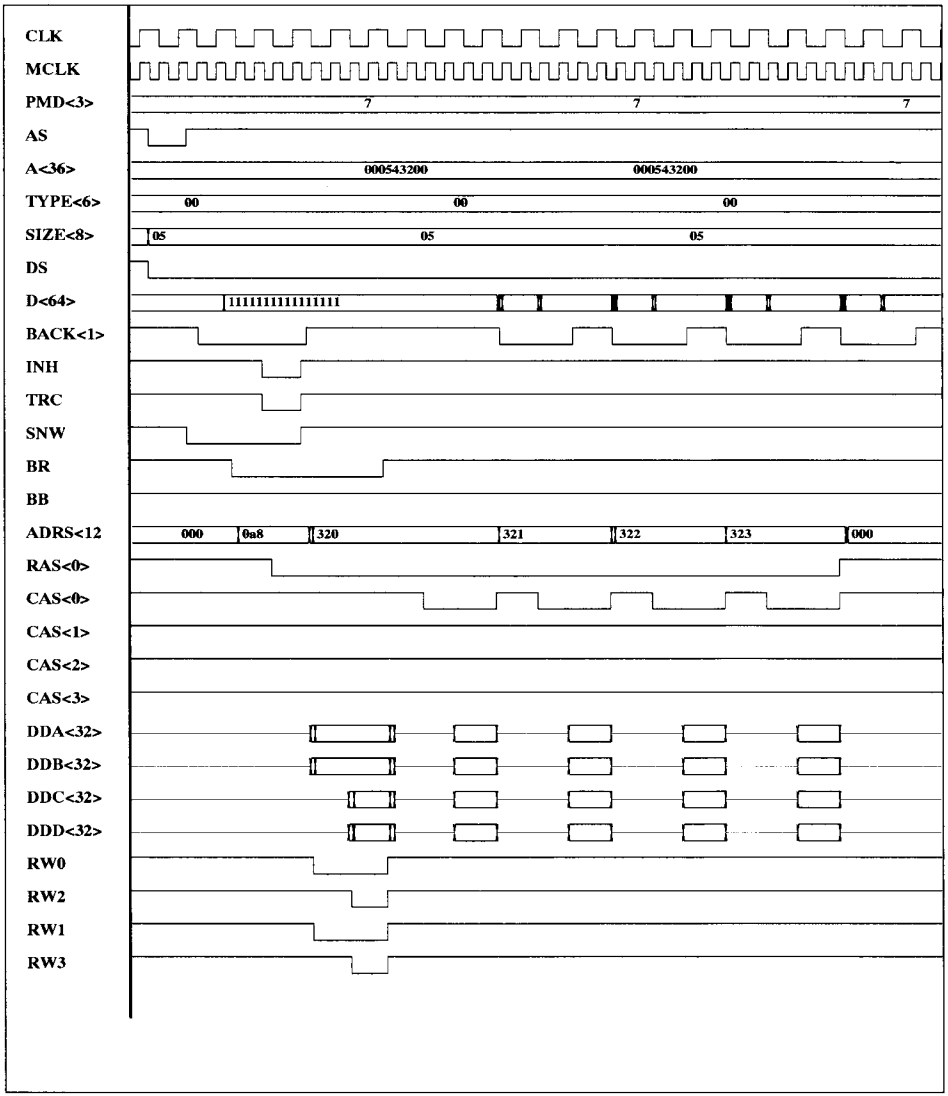
Timing Diagrams (continued)

Write Burst Truncated by BLST, Mode 01



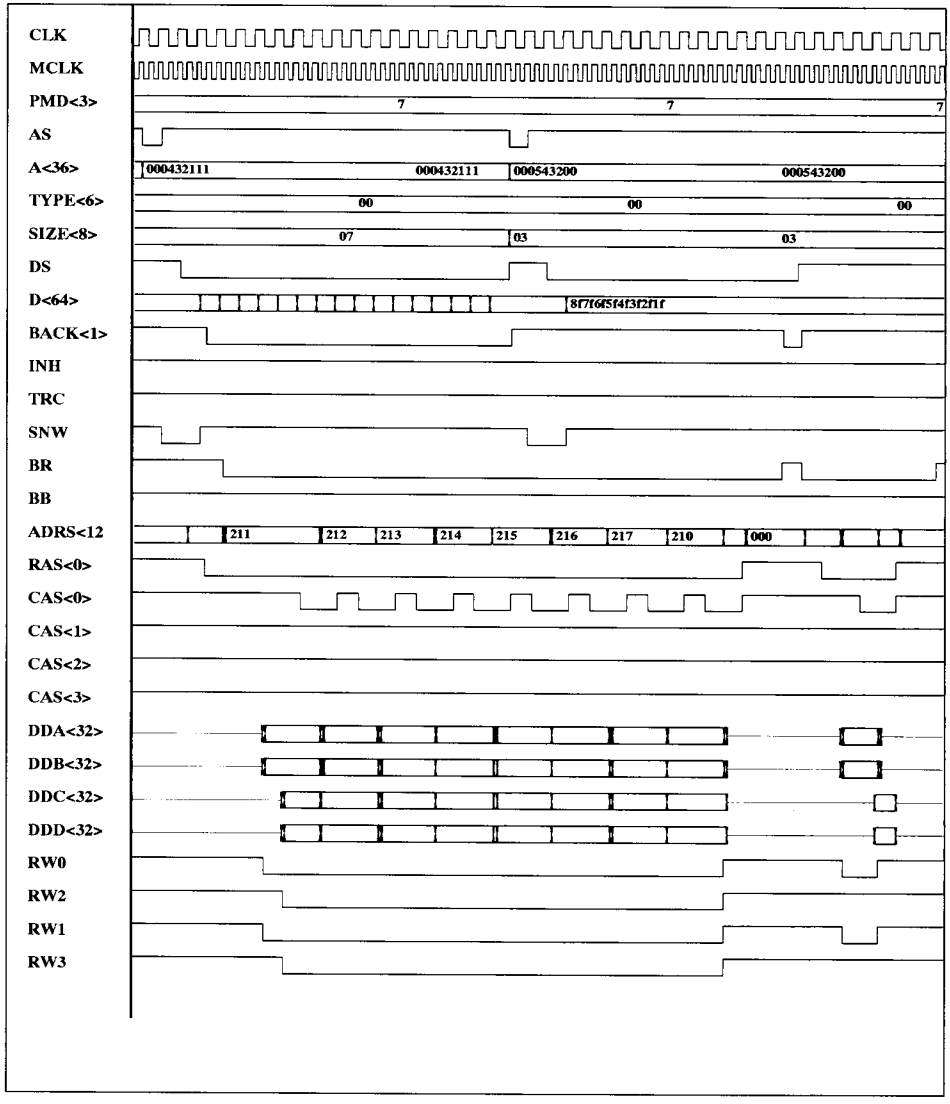
Timing Diagrams (continued)

Write Mode 01, Transformed



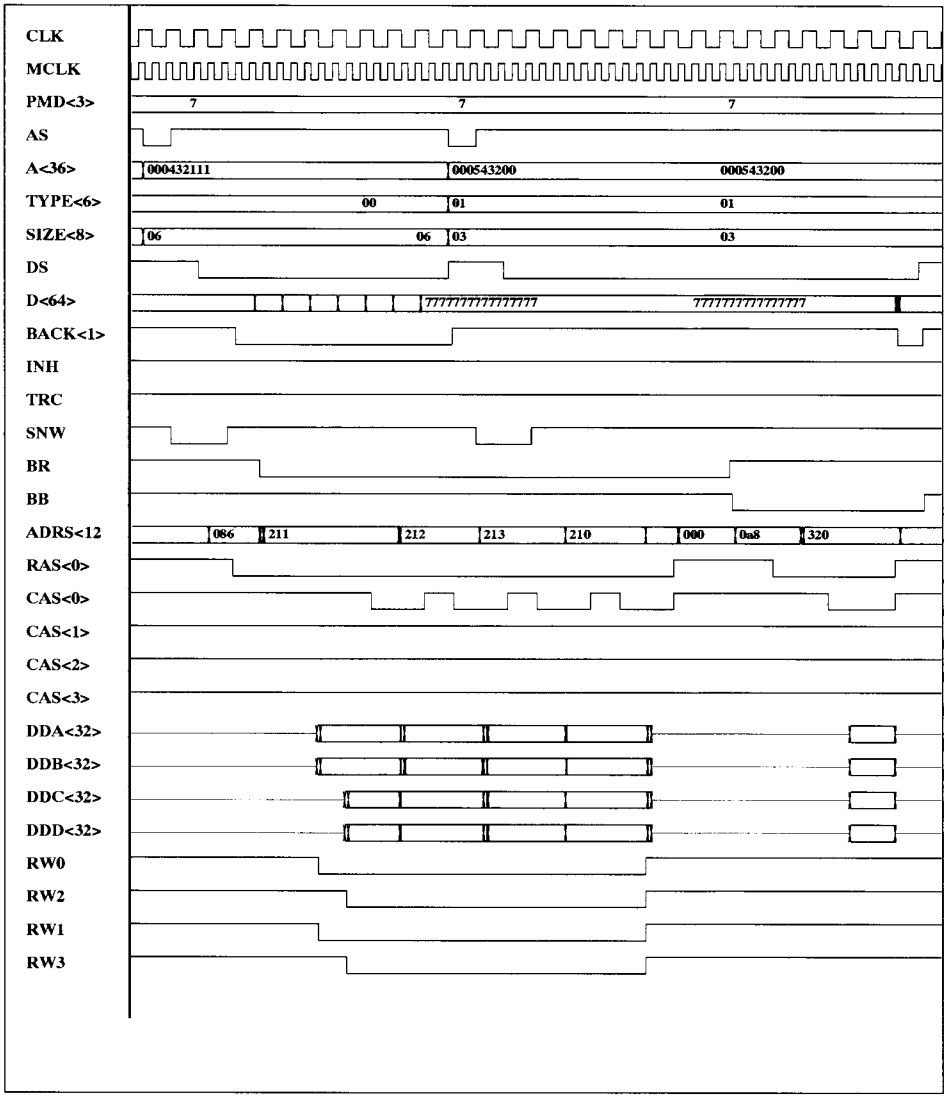
Timing Diagrams (continued)

Write Burst Followed by Write, Mode 01



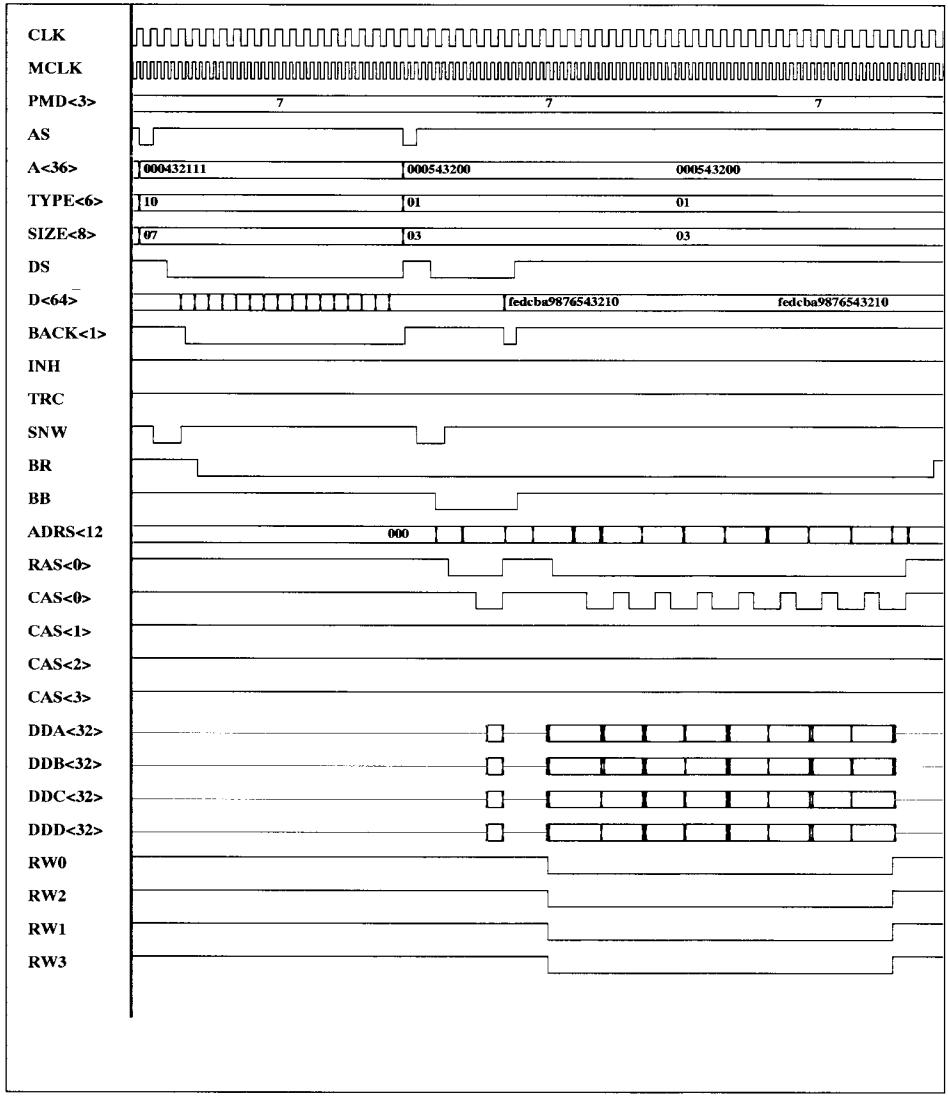
Timing Diagrams (continued)

Write Burst Followed by Read, Mode 01



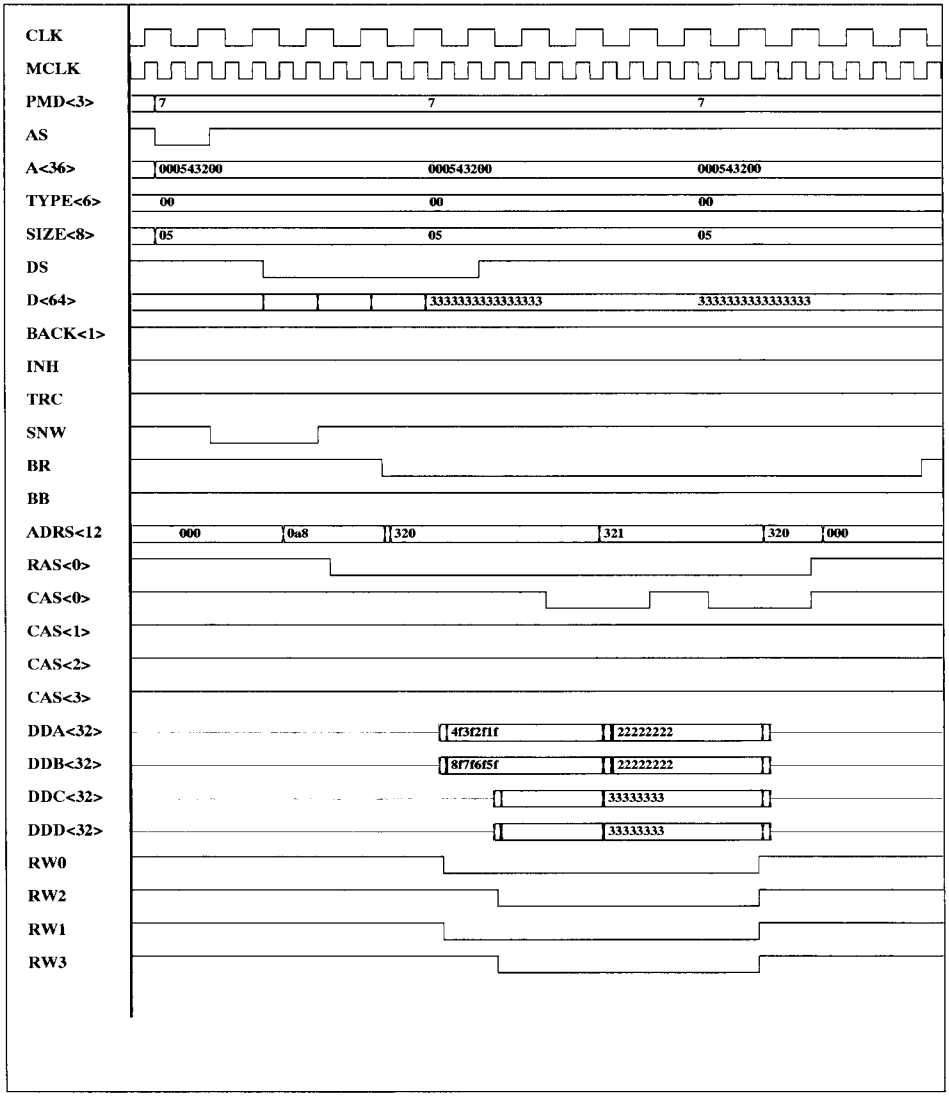
Timing Diagrams (continued)

Write Posted Followed by Read, Mode 01



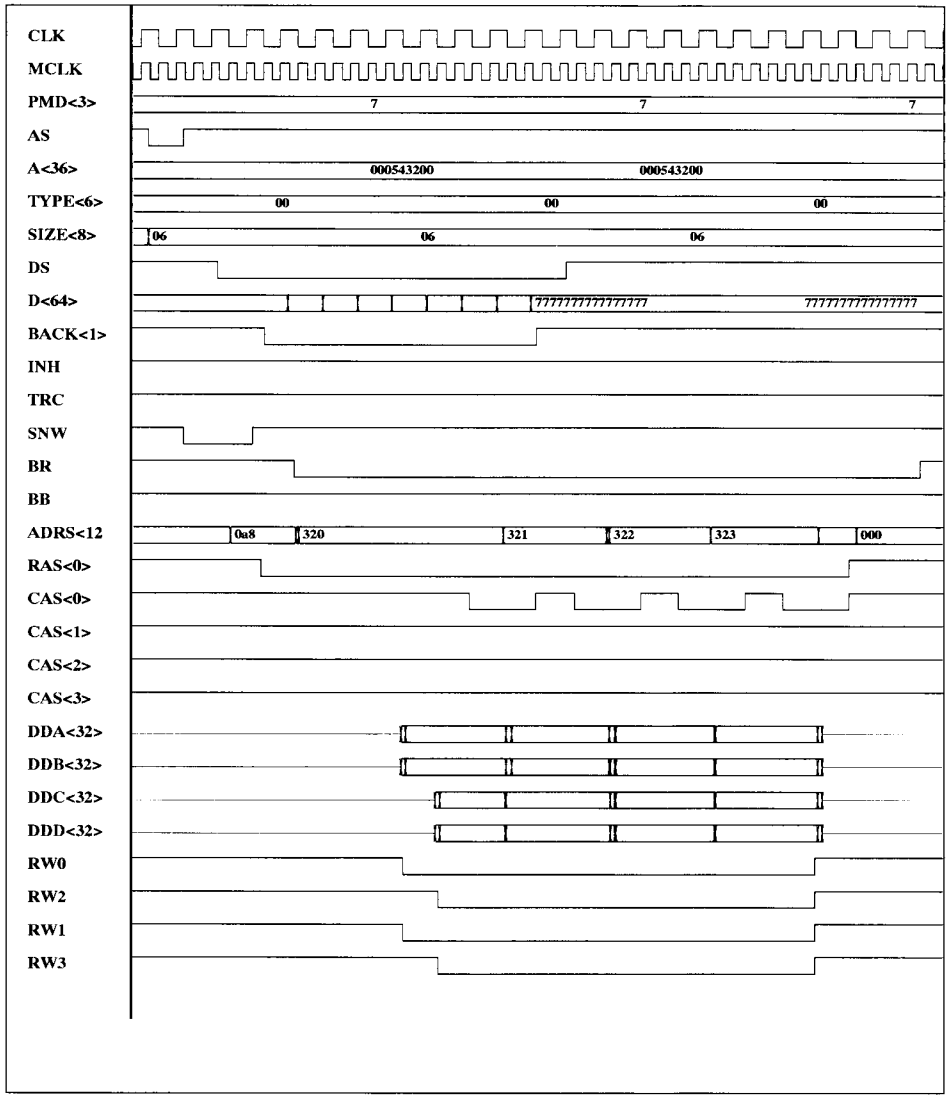
Timing Diagrams (continued)

Write Mode 10 Showing BR as FE



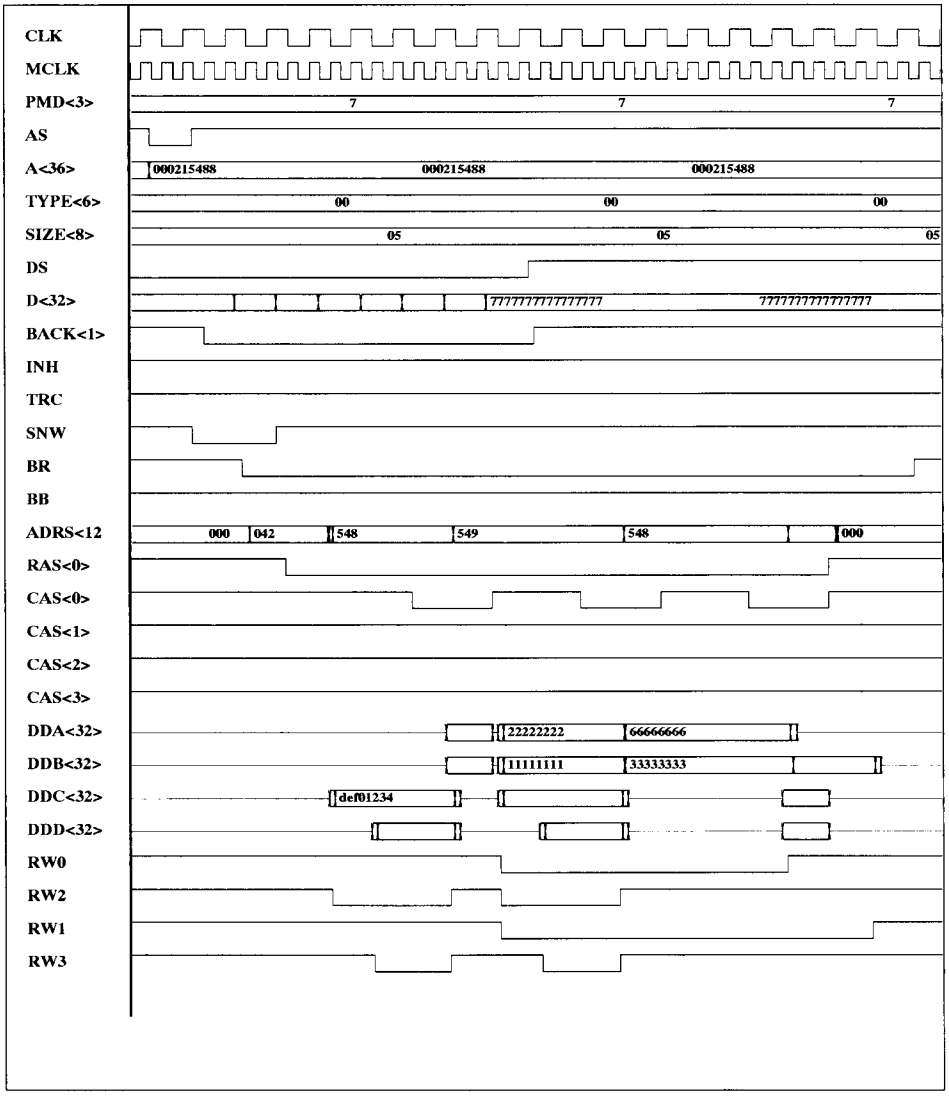
Timing Diagrams (continued)

Write Burst, Mode 11



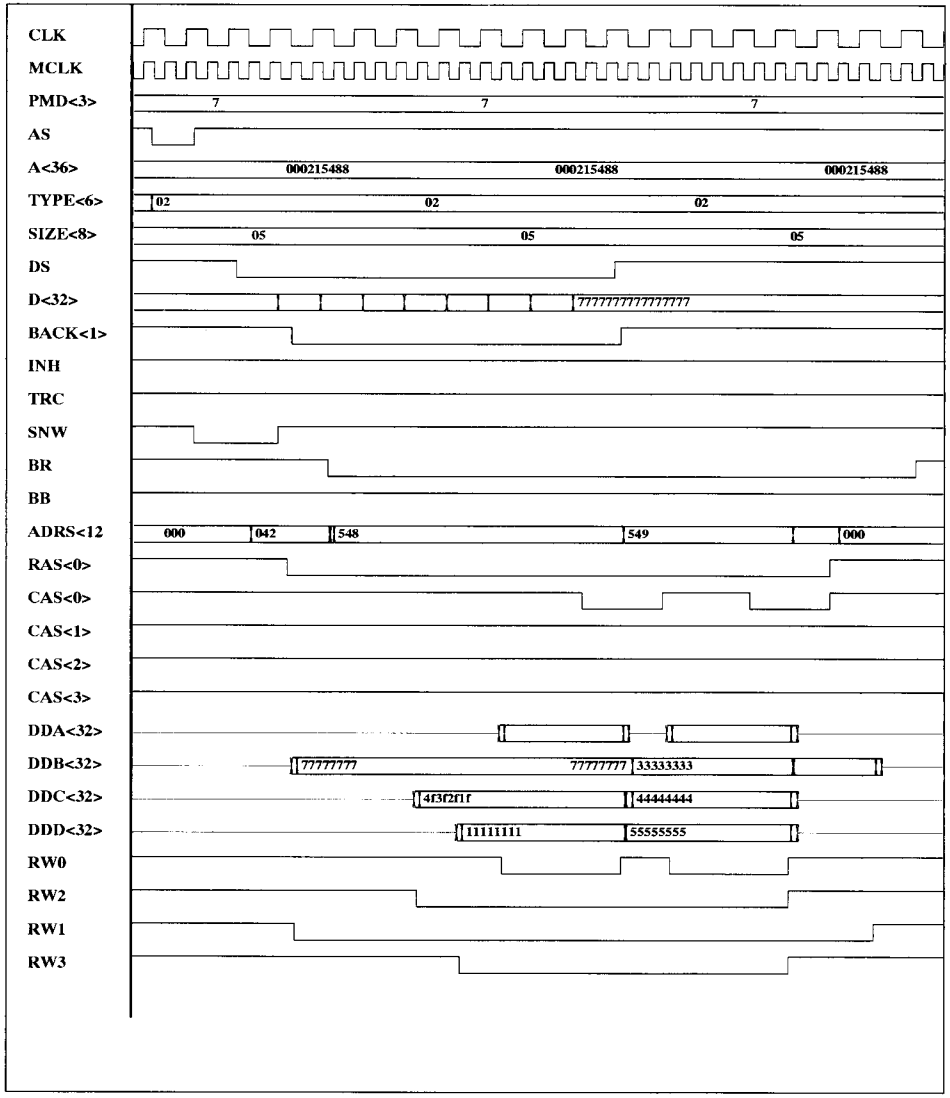
Timing Diagrams (continued)

Write 32 Bytes, Misaligned 32-Bit Bus



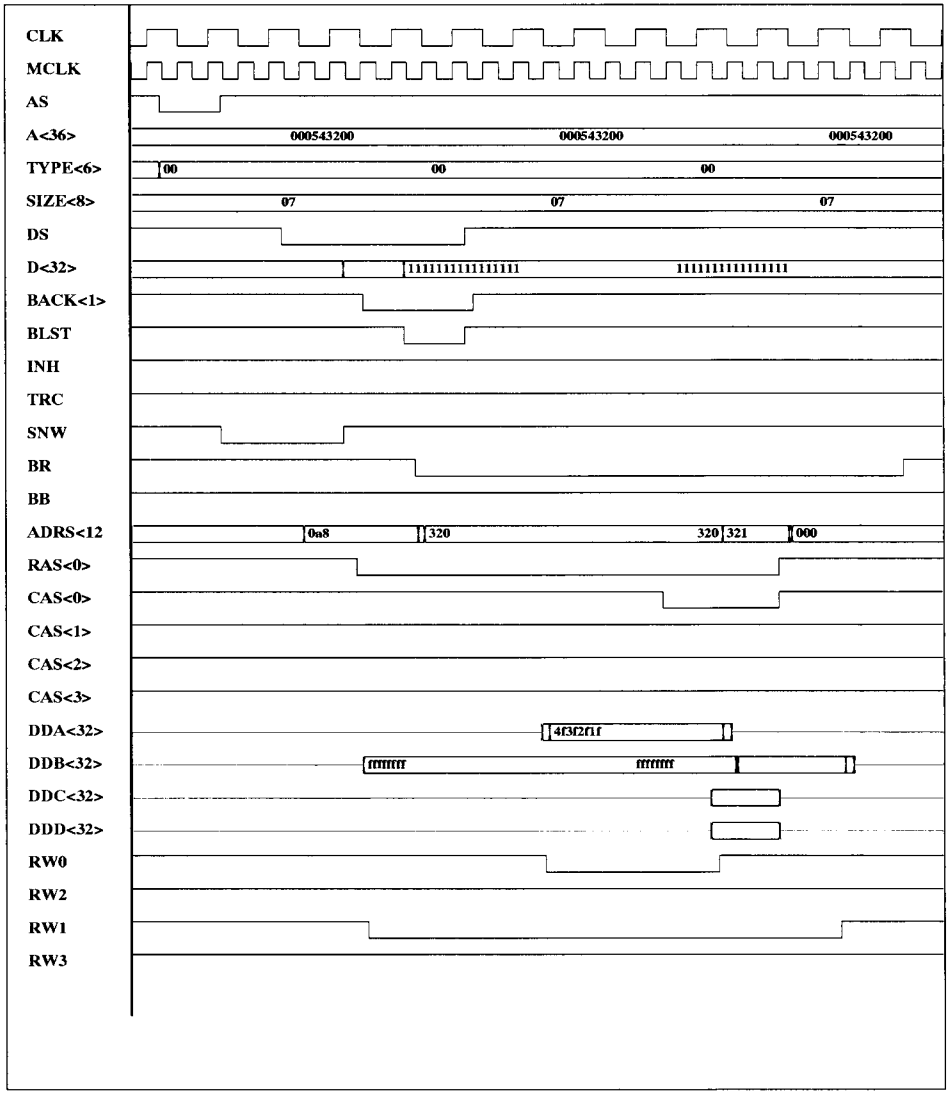
Timing Diagrams (continued)

Write 32 Bytes, Misaligned, Intel Order 32-Bit Bus



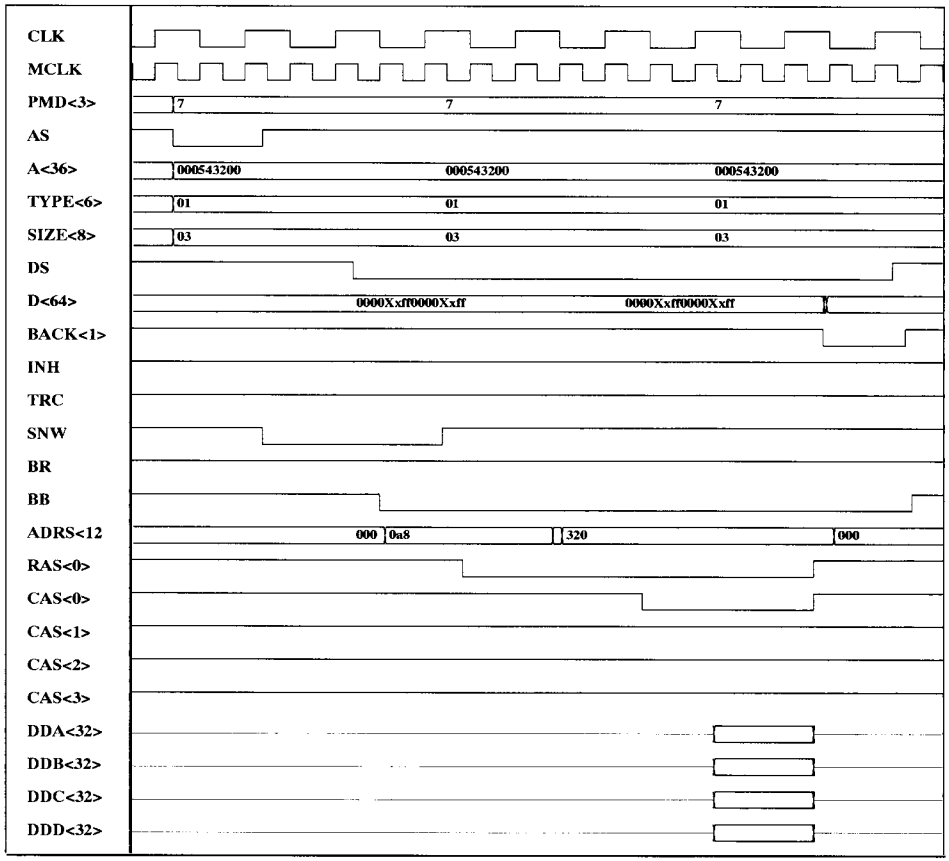
Timing Diagrams (continued)

Write with BLST, 32-Bit Bus



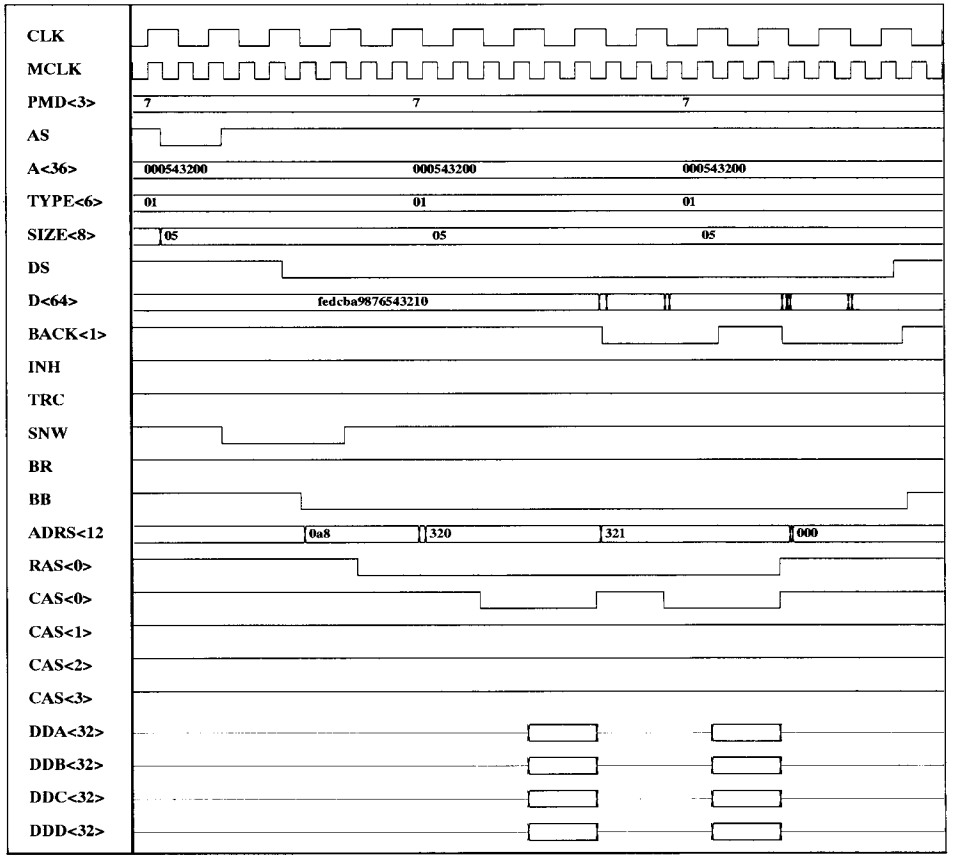
Timing Diagrams (continued)

Read Mode 01, 8 Bytes



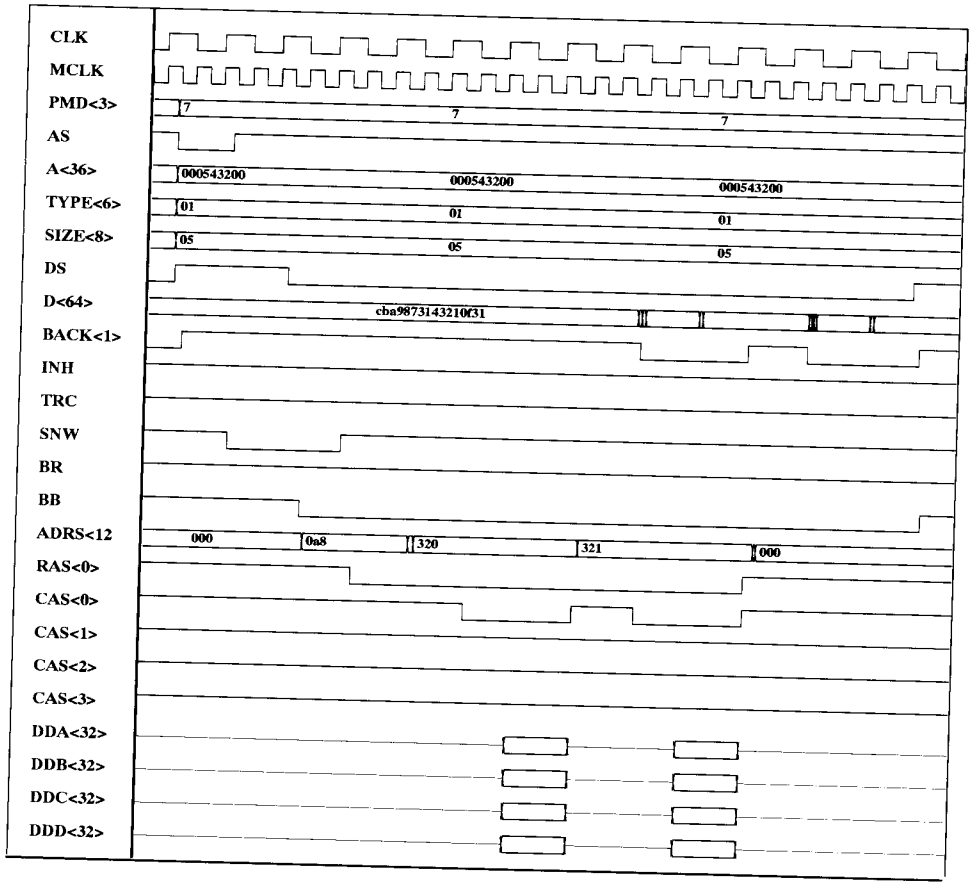
Timing Diagrams (continued)

Read Mode 01, 32 Bytes



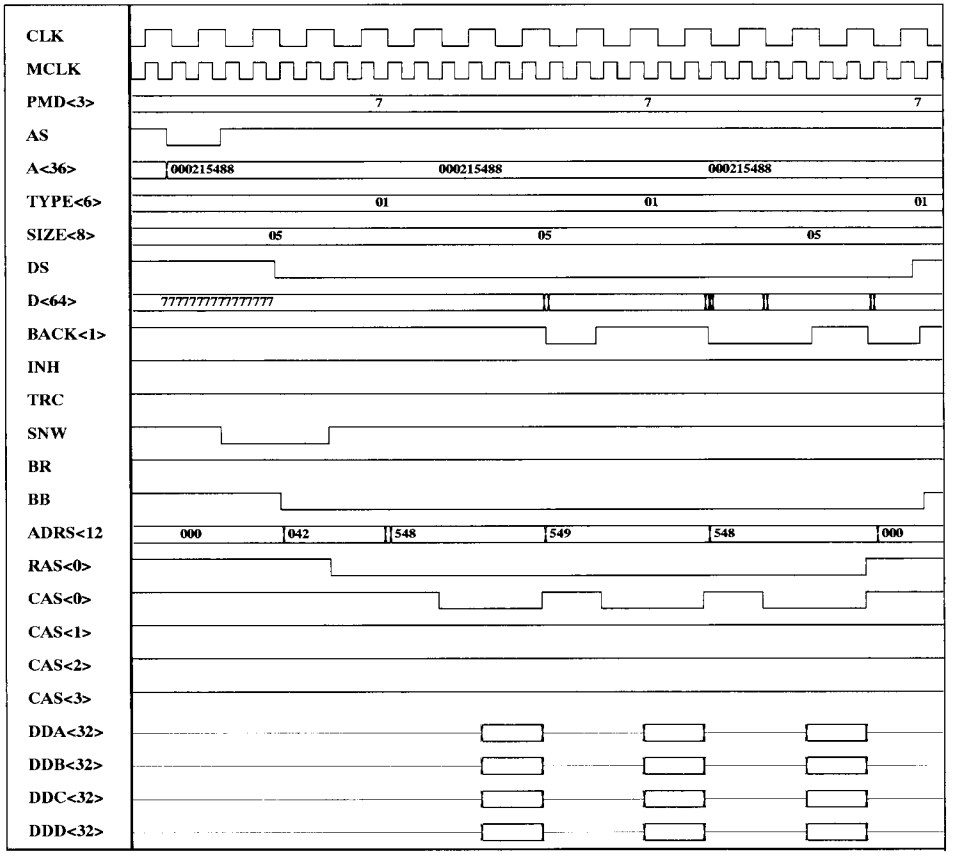
Timing Diagrams (continued)

Read Mode 01, Wait State, 32 Bytes



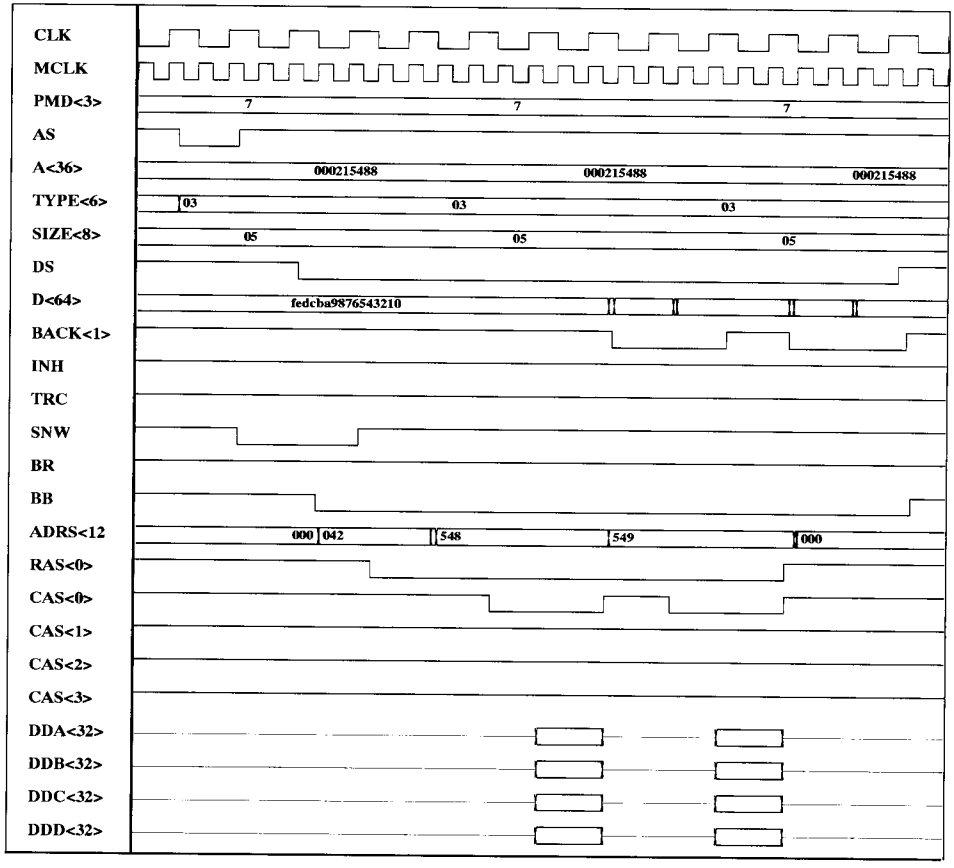
Timing Diagrams (continued)

Read Mode 01, Sequential, Misaligned



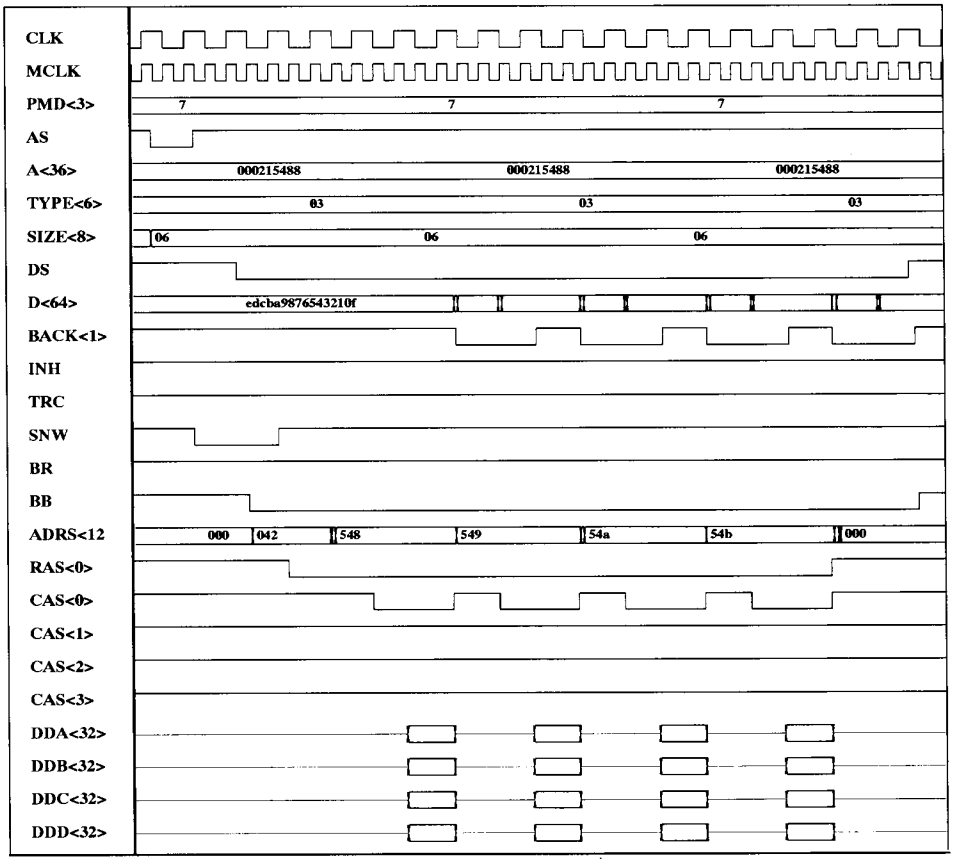
Timing Diagrams (continued)

Read Mode 01, Intel, Misaligned, 32 Bytes



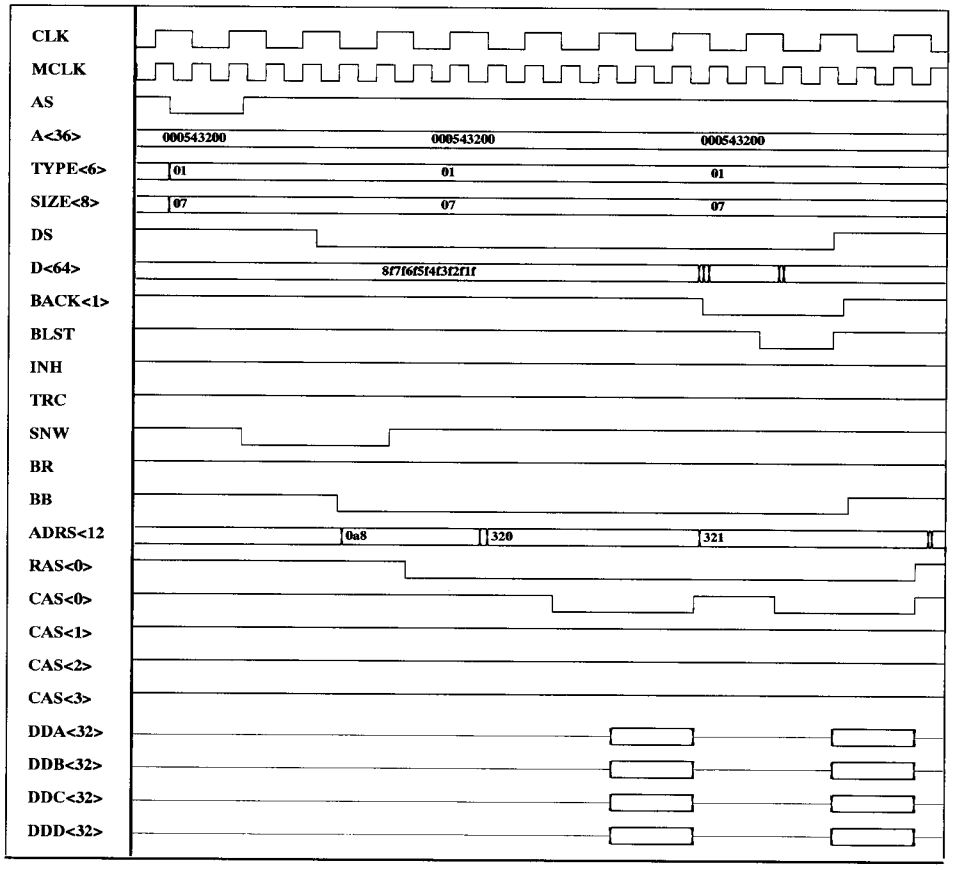
Timing Diagrams (continued)

Read Mode 01, Intel, Misaligned, 64 Bytes



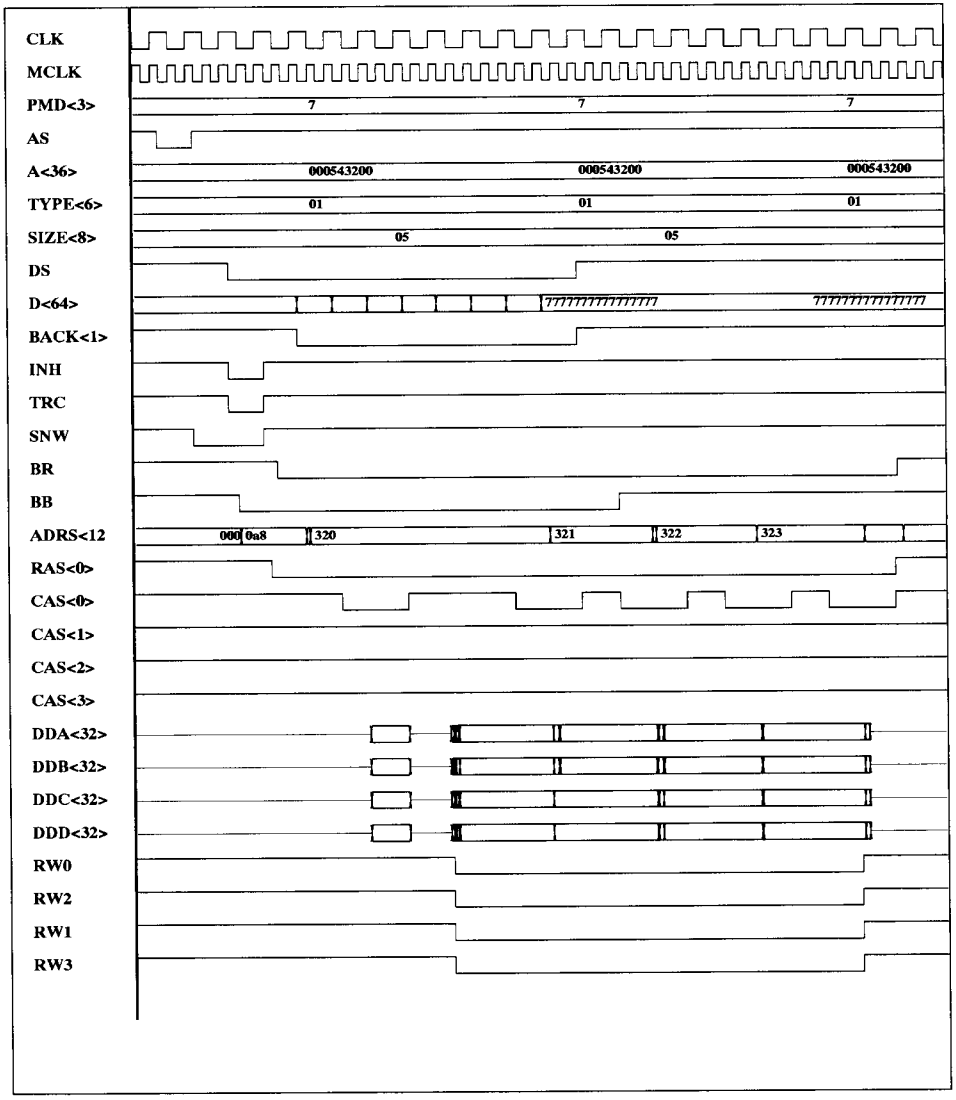
Timing Diagrams (continued)

Read with BLST Mode 01



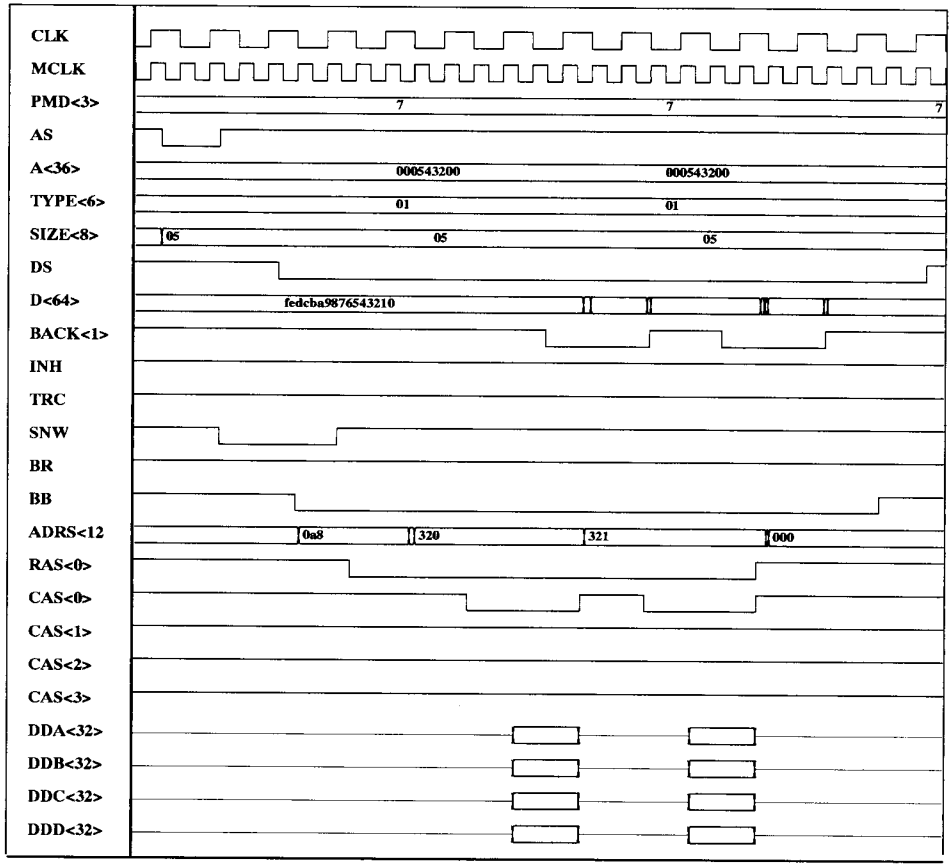
Timing Diagrams (continued)

Read Mode 01, Transformed



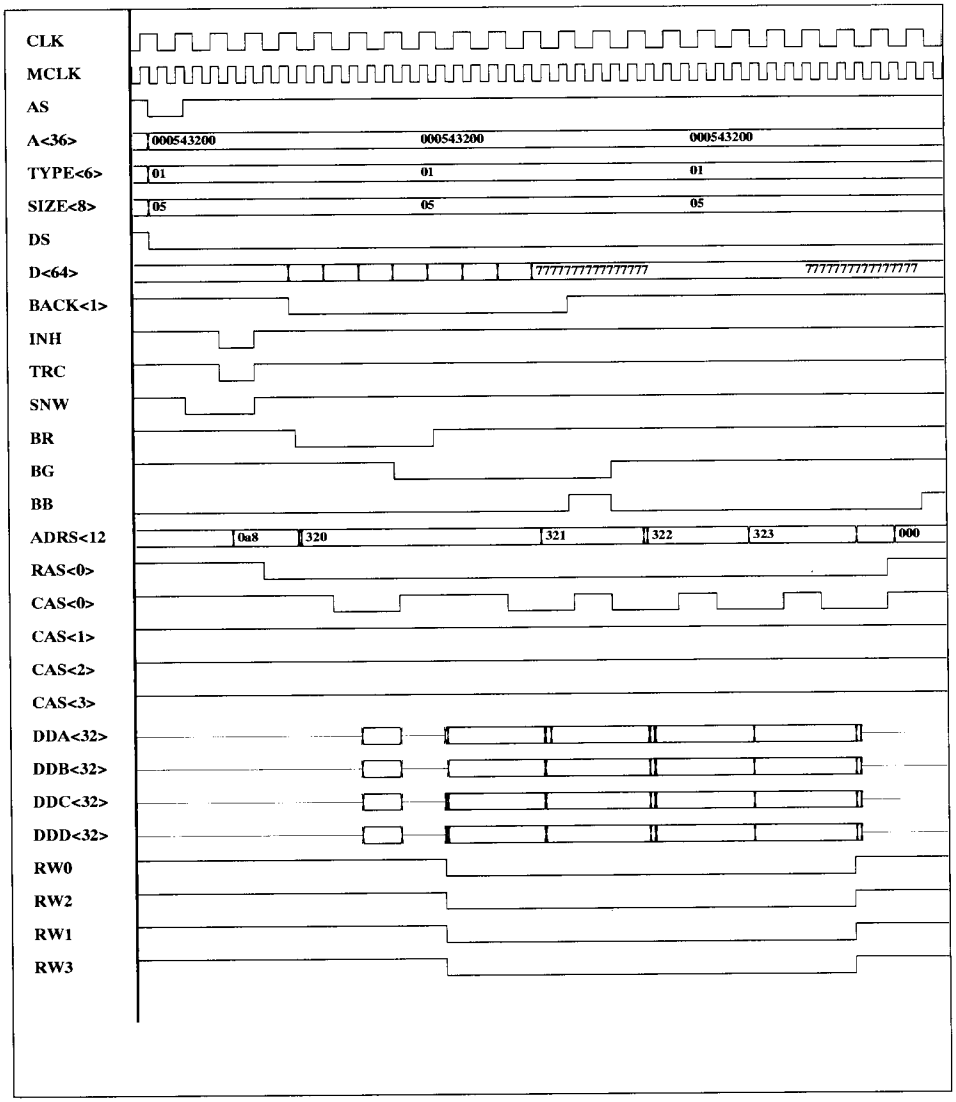
Timing Diagrams (continued)

Read Mode 11



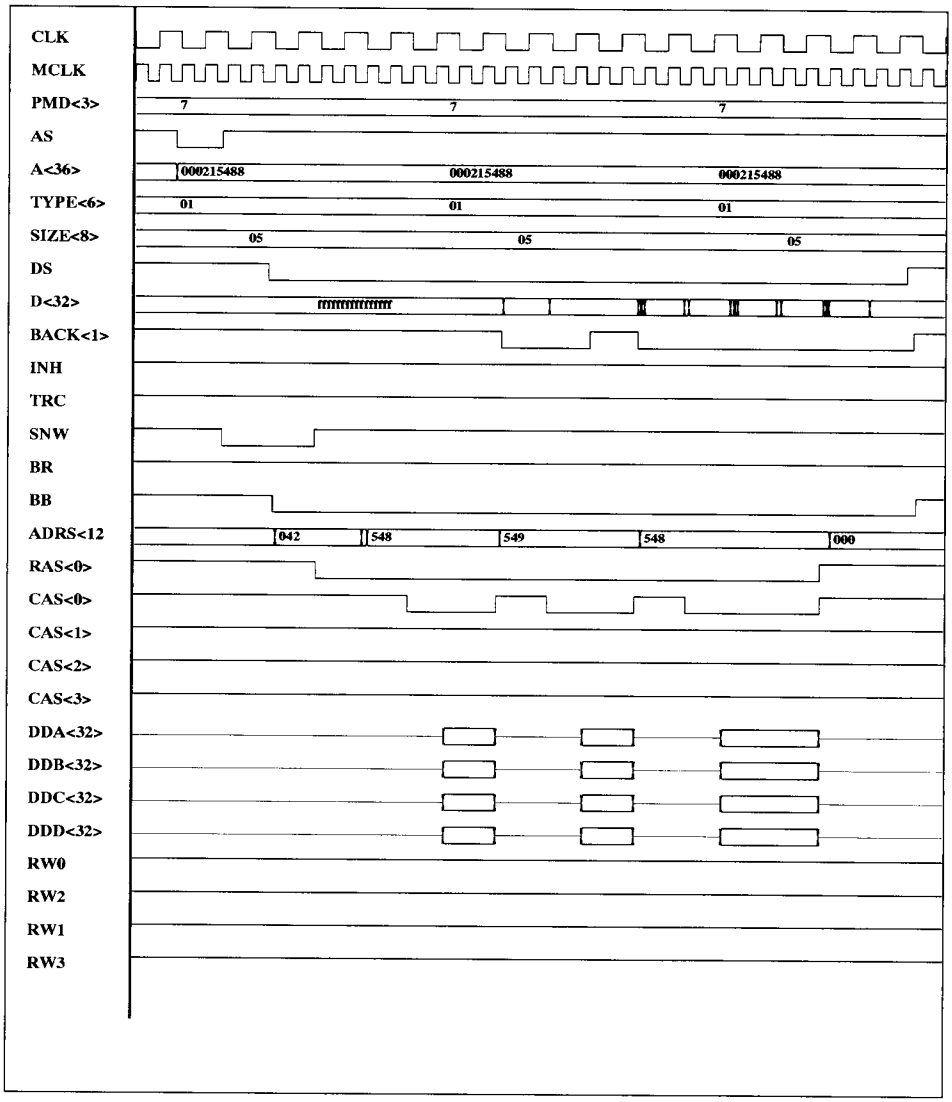
Timing Diagrams (continued)

Reflective Transaction Showing Bus Arbitration



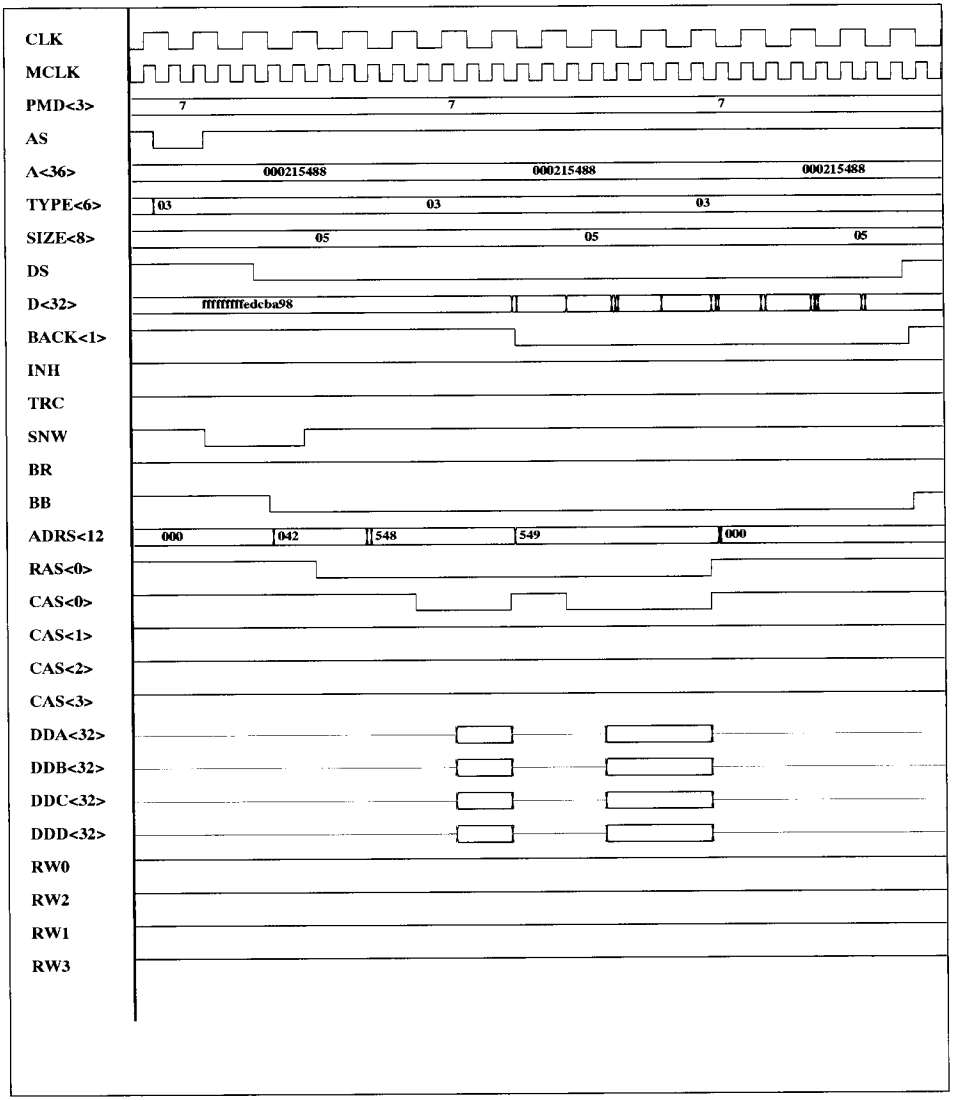
Timing Diagrams (continued)

Read 32 Bytes, Misaligned 32-Bit Bus



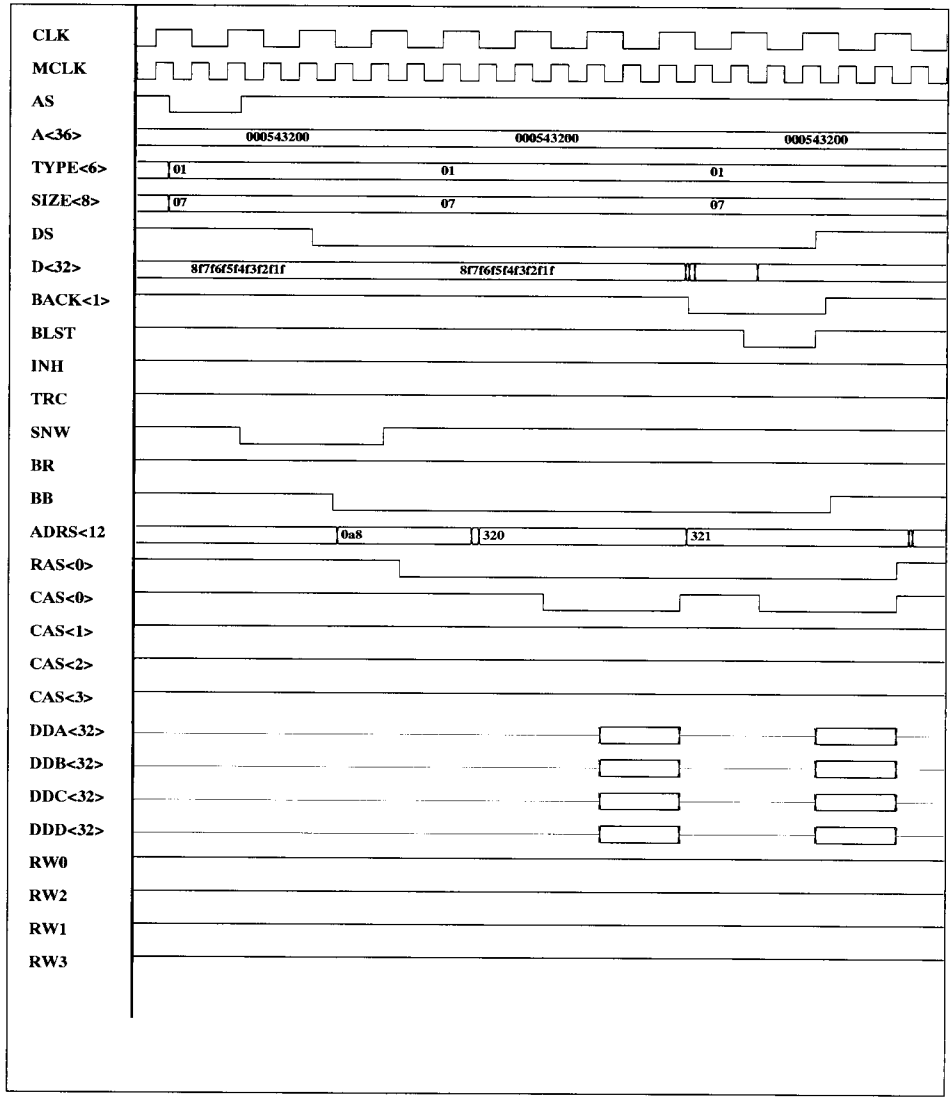
Timing Diagrams (continued)

Read 32 Bytes, Misaligned, Intel Order 32-Bit Bus



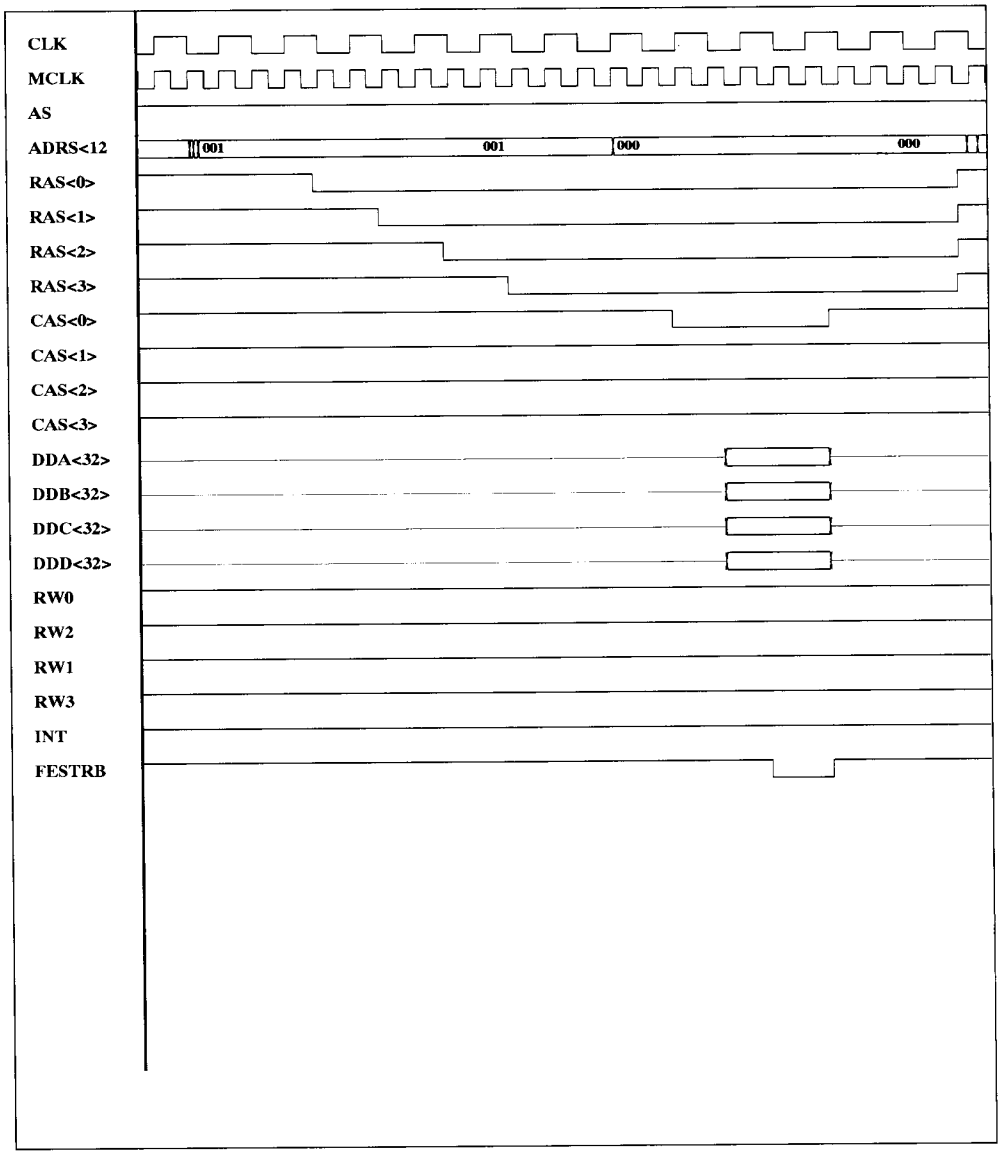
Timing Diagrams (continued)

Read with BLST, 32-Bit Bus



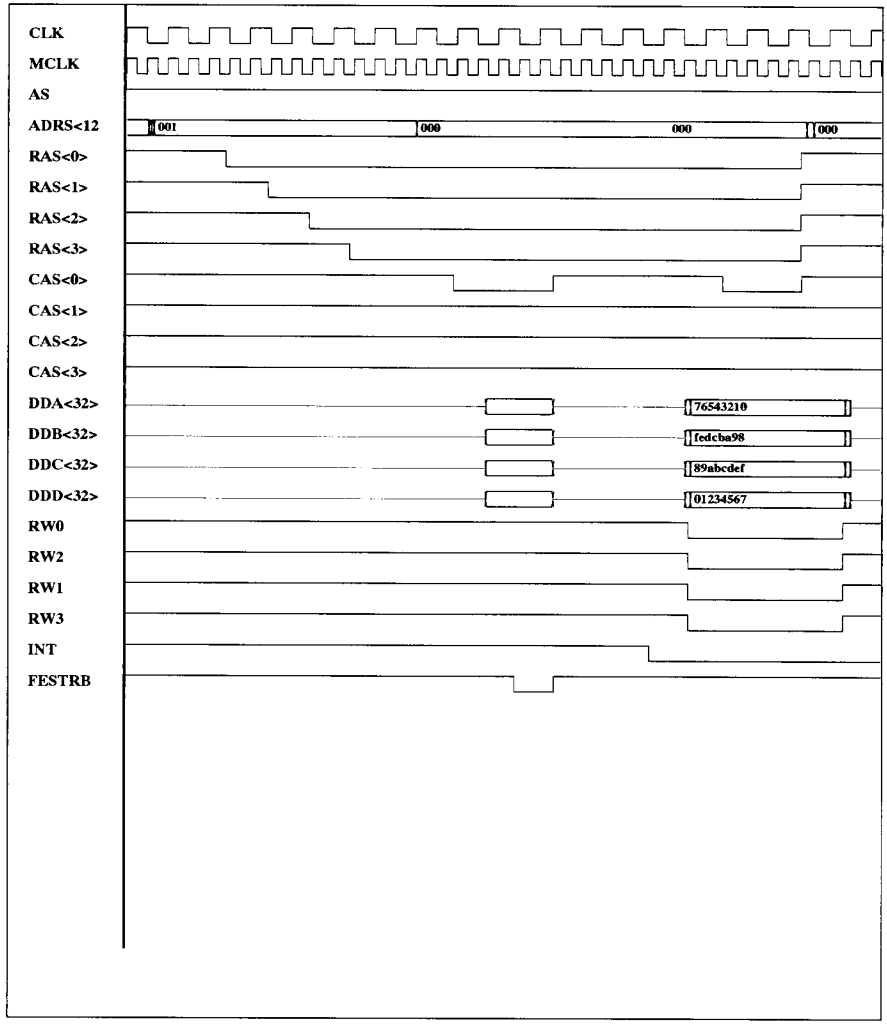
Timing Diagrams (continued)

Refresh, Staggered RAS, No Scrub, No Error in Data



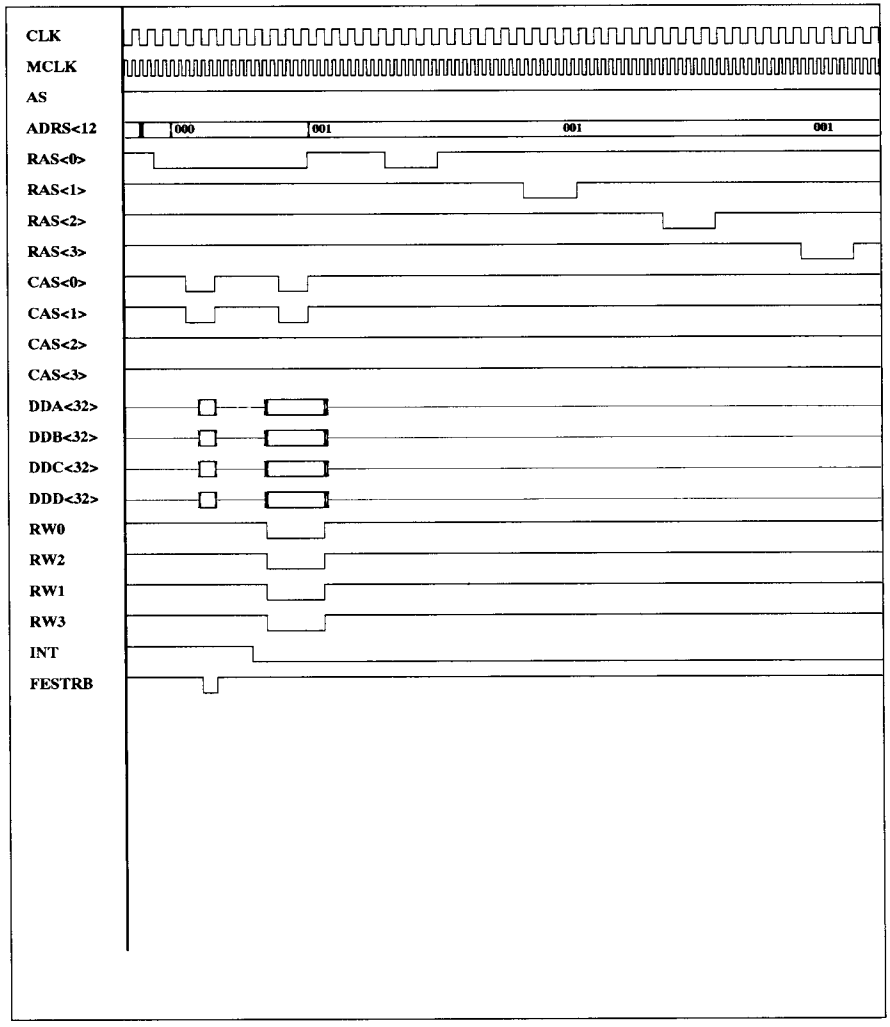
Timing Diagrams (continued)

Refresh, Staggered RAS, Scrub



Timing Diagrams (continued)

Refresh, Mutually Exclusive RAS, Scrub



Power Dissipation

The table below shows the estimated power dissipation for various bus clock frequencies under specific assumptions. The temperatures listed under the air flow column are the maximum ambient air temperature allowed for the frequency at the left and the air flow at the column top.

The assumptions are: DRAM bus load = 50 pF; system bus load = 100 pF; system bus data frequency is ½ of the system clock (NRZ); DRAM bus data frequency is ½ of the system clock (NRZ); and V_{CC} is 5.25V.

The data pattern assumptions are:

Reads: $^2/_3$ of all system bus cycles involve the CYM7232.
$^2/_3$ of all CYM7232 cycles are reads.
½ of the 64-bit system bus will toggle on average.
The CYM7232 drives the system bus $^1/_3$ of the time during a read.

Writes: $^2/_3$ of all system bus cycles involve the CYM7232.
$^1/_3$ of all CYM7232 cycles are writes.
½ of the 64-bit system bus will toggle on average.
The CYM7232 drives the system bus $^1/_6$ of the time during a write.

System Clock Frequency (MHz)	Power (watts)	Air Flow –LFM (C)				
		0	100	200	300	400
25	0.8	70	70	70	70	70
33	1.0	60	60	60	70	70
40	1.2	60	60	60	60	60

Socket Data

Test ZIF Socket: Textool 3M Grid ZIP PGA Kit 25 x 25
Socket Part # 2–0000–06325–170–024–000
PGA Pin (gold plated) Part# 3–0000–02740–006–000–002
PGA Pin (nickel plated) Part# 3–0000–02740–006–000–005

Test Receptacle: Procon Part# 228–401–1001–2525
(uses Millmac 0400 Pins Part# 0400–0–15–01–47–27–0400)

Production Socket: McKenzie Part# PGA401H009B2–2406R

Installation Lubricant: Tech Spray Part# 2111–P (Goldfinger Glove)

Extraction Tool: McKenzie Part# TOLPGAX–41622–001 (CYM7232)
TOLPGAX–41622–002 (CYM7264)

McKenzie, 44370 Old Warm Springs Boulevard, Fremont, CA 94538 (510) 651–2700

Tech Spray, P.O. Box 949, Amarillo, TX 79105 (806) 372–8523

Procon Tech., 1333 Lawrence Expwy., Suite 207, Santa Clara, CA 95051 (408) 246–4456

Textool, 6801 Riverplace Blvd., Austin, TX 78726 (800) 328–0411

Ordering Information

Speed (MHz) Bus/DRAM	Ordering Code	Package Name	Package Type	Operating Range
40/80	CYM7232S–40HGC	HG02	401-Pin PGA Module	Commercial
33/99	CYM7232H–33HGC	HG02	401-Pin PGA Module	Commercial
33/66	CYM7232S–33HGC	HG02	401-Pin PGA Module	Commercial
25/100	CYM7232H–25HGC	HG02	401-Pin PGA Module	Commercial
25/75	CYM7232S–25HGC	HG02	401-Pin PGA Module	Commercial

Speed (MHz) Bus/DRAM	Ordering Code	Package Name	Package Type	Operating Range
40/80	CYM7264S–40HGC	HG03	401-Pin PGA Module	Commercial
33/99	CYM7264H–33HGC	HG03	401-Pin PGA Module	Commercial
33/66	CYM7264S–33HGC	HG03	401-Pin PGA Module	Commercial
25/100	CYM7264H–25HGC	HG03	401-Pin PGA Module	Commercial
25/75	CYM7264S–25HGC	HG03	401-Pin PGA Module	Commercial

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