

Introduction

To maximize throughput in Automated Test Systems (ATE), reducing the time required to make DC measurements is of paramount importance. The limiting factor is often the time the Per-Pin Measurement Unit (PPMU) output takes to settle to the accuracy required to make the measurement. This time is dependent on system factors such as the parasitic capacitance of the Device Under Test (DUT) node and measurement accuracy requirements, as well as the PPMU design and the external Components.

Virtually all PPMU measurements fall into one of two categories: Either a voltage is forced on a DUT pin and the current is measured, or a current is forced and the voltage is measured. Since more PPMU measurements are performed in the Force Voltage/Measure Current mode, this article will deal primarily with this operating mode. (The Force Current/Measure Voltage mode optimization techniques and limiting factors are similar to those described here).

A simplified block diagram of the Edge4707B PPMU is shown in Figure 1. This device consists of a driver amplifier, a selectable external sense resistor, a differential amplifier which outputs a voltage proportional to the current through the sense resistor, and a switch which determines whether the feedback to the driver amplifier comes from the external sense input (force voltage mode) or from the differential amplifier (force current mode). Also included are connections for a number of external compensation capacitors which can be selected to optimize the performance of the part. This document deals primarily with explaining the characteristics of this type of circuit and how to optimize the output waveform for a particular ATE system's requirements.

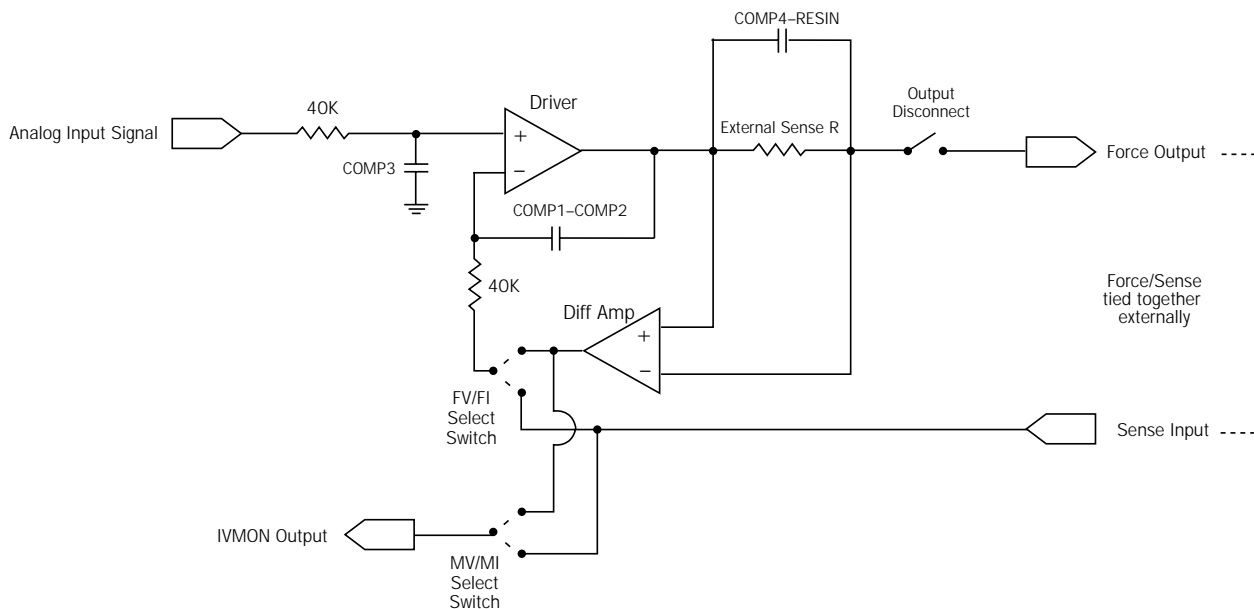


Figure 1. Edge4707B Simplified Block Diagram
 (for more detail, see the functional schematic in the Edge4707B Datasheet)

When making parametric measurements in an ATE system, it is desirable to have both the fastest possible settling time as well as the smallest amount of overshoot and ringing. Unfortunately, this cannot be achieved for several practical reasons. One is that the optimum compensation for one range will not be optimal for the other ranges. Therefore, the optimization must take into account the differences between the signal behavior on each range and how often each range will be used in practice. Since the lowest current range (Range A on the Edge 4707B) is used primarily for characterizing leakage currents, and production pass/fail testing of these low currents is often done on higher current ranges, this range is used the least in many situations. Therefore, the settling time on this range can often be sacrificed to get better performance on other ranges.

There is also a trade-off between faster settling time and lower overshoot and ringing. The compensation capacitors which give the fastest settling times also allow the output to overshoot and ring under some conditions. This is mitigated in part because the settling time on the current measurement (IVMON) output is usually of the greatest concern (for making measurements), whereas the DUT node is the point where overshoot is of most concern (to keep the DUT from being stressed). So the compensation capacitors can be chosen to give the cleanest possible signal at the FORCE output and still give good settling time performance at the IVMON output. Even so, some compromise will almost always have to be made between getting the fastest throughput and lowest amount of overshoot and ringing at the DUT.

The settling time and overshoot/stability characteristics of this circuit will be dealt with separately. Settling time behavior will be addressed first and then stability concerns will be discussed at the end of this paper.

Components of Settling Time Behavior

Settling time and stability in the Edge 4707B (and similar PPMU's) depends on many variables. The magnitude of the voltage step, the capacitance present on the FORCE/SENSE output node, the source impedance of the driver circuit (which is dominated by the resistance of the current

sense resistor), and the desired accuracy of the final measurement all factor heavily in determining the output waveform characteristics.

Settling time can be broken down into three components: 1) Delay time from when the input (either analog or digital) changes to when the output begins to respond, 2) slew time (when the output is changing at its maximum rate), and 3) final settling. The effect of these components and how to minimize their effect will each be discussed in separate sections below.

Delay Time Component

The response time to changing input conditions is usually negligible. The only time this is not the case is when one of the amplifiers has been driven to the power supply rail. The most common case is when the feedback loop is broken for some reason, such as if the load impedance requires more current than the PPMU driver can supply in force voltage mode, or if the load impedance is too high in force current mode, etc. In either of these cases the driver amplifier output goes to the positive or negative rail. The recovery time from this condition is typically 35 μ s, which is not much different from the settling times on the highest ranges, C and D (and even B for small voltage steps). This can significantly increase the settling time if it is allowed to occur.

The best solution is to ensure that the part is operated so the internal driver amplifier never goes to the rails. This is done, in part, by always putting the Edge4707B into high impedance mode (HiZ true) whenever the operating mode or range is changed. It is also important to be sure that the output current range is sufficient to supply the current being drawn by the DUT. If the amount of current draw is extremely variable, it is quicker to start with a higher current range and switch down as necessary rather than to start at a lower current range and switch to a higher current range.

Changing input voltages can also send the driver amplifier output to the rail. This is most likely to occur with large step sizes, fast input slew rates and large load capacitances. This means that the amount of capacitance

on the FORCE output should be kept to a minimum whenever possible. As will be shown later, minimizing this capacitance will also help shorten the settling time for small voltage steps.

Limiting the size of the input voltage steps will almost always keep the output from going to the rail. However, limiting this is not always possible. An alternative is to limit the slew rate of the input signal so it is not faster than the slew rate of the output signal. This can be done by changing the value of the COMP3 capacitor shown in the Figure 1 block diagram. This capacitor, along with the 40 KΩ resistor in series with the input, creates an R-C time constant which effectively limits the slew rate of the signal going into the driver amp. The slew rates at the force output on each of the ranges, with varying compensation capacitors, is shown in Figures 2 through 5. Since the settling time on the lower current ranges (A and B) is much longer than the rail recovery time, keeping the output from going to the rail is less important on these ranges. It is more important to limit the input slew rate when using the higher current ranges, since this will give the greatest settling time improvement.

The maximum slew rates with a ~100pF load capacitance for each range can be found from the data in Figures 2 through 5. On Ranges C and D the maximum slew rates are about 1.1V/μs. If a 100pF capacitor is used for COMP3, then the maximum input slew rate will be 2.5V/μs, and the average slew rate will be 1.25V/μs. 100pF is the recommended value for keeping the output from going to the rail on these ranges. This is the recommended value for this compensation capacitor for most systems.

Ranges A and B have maximum slew rates of about 0.55V/μs. To keep the output from going to the rail on these ranges, the COMP3 capacitor should be increased to about 220pF. Since the rail recovery time on these ranges is significantly less than the settling time for most situations, setting COMP3 to this large a value is normally not recommended since this will slow down the performance on the higher current ranges.

Note that the above calculations are for a relatively small output load capacitance (eg. 100pF). With larger output load capacitance, the output can still go to the rail due to overshoot and ringing. This will be covered in more detail in the Stability Section below.

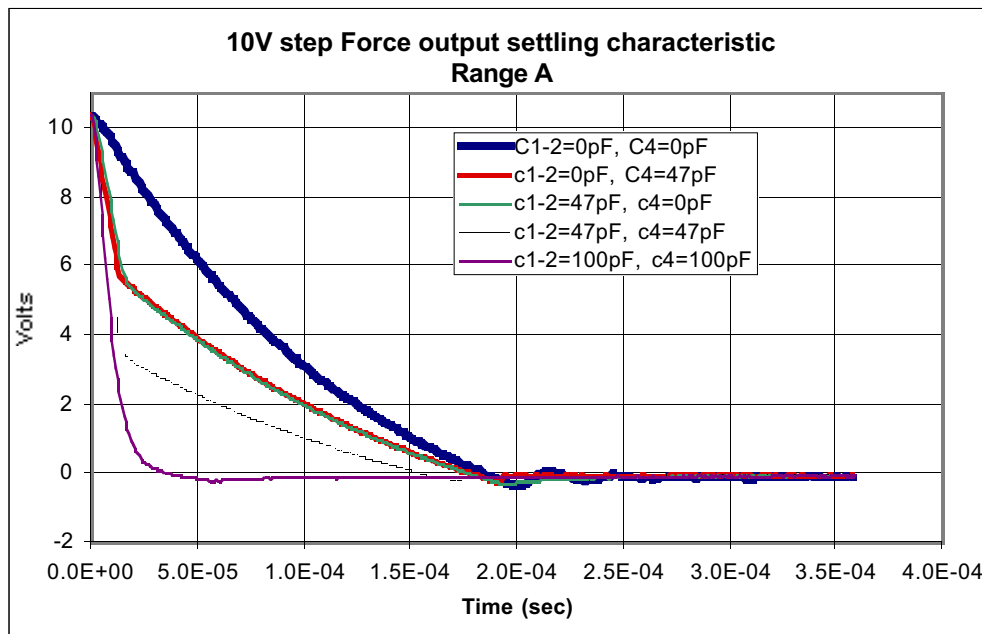


Figure 2. Range A (2μA) Force Output Settling in Force Voltage Mode (CLOAD = 108 pF)

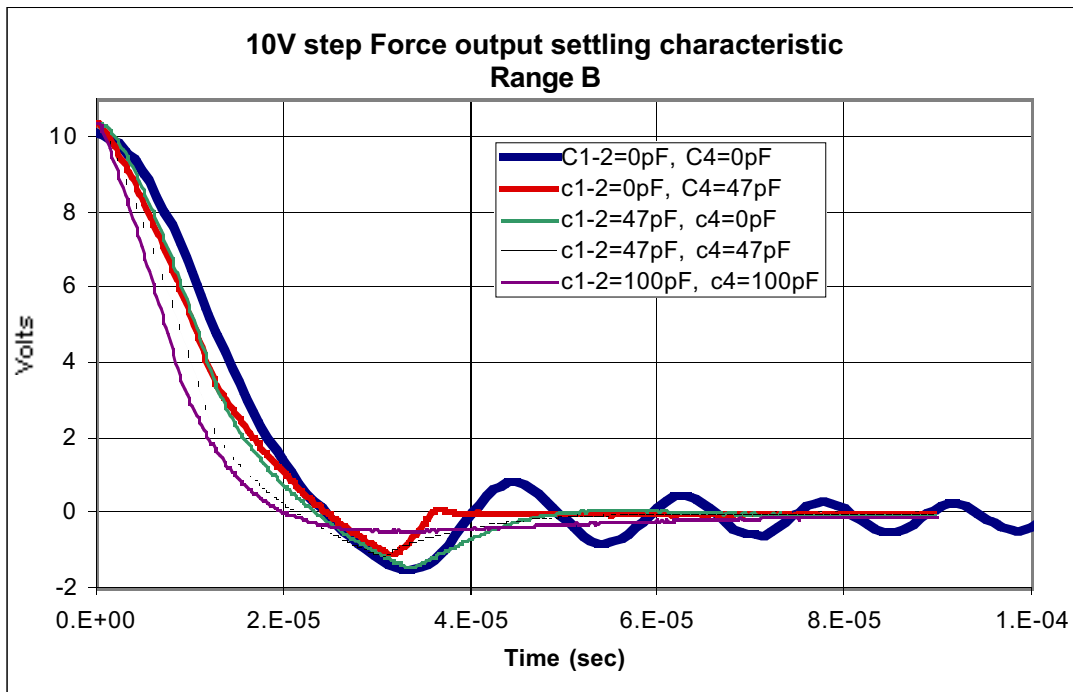


Figure 3. Range B (20 μ A) Force Output Settling in Force Voltage Mode (CLOAD = 108 pF)

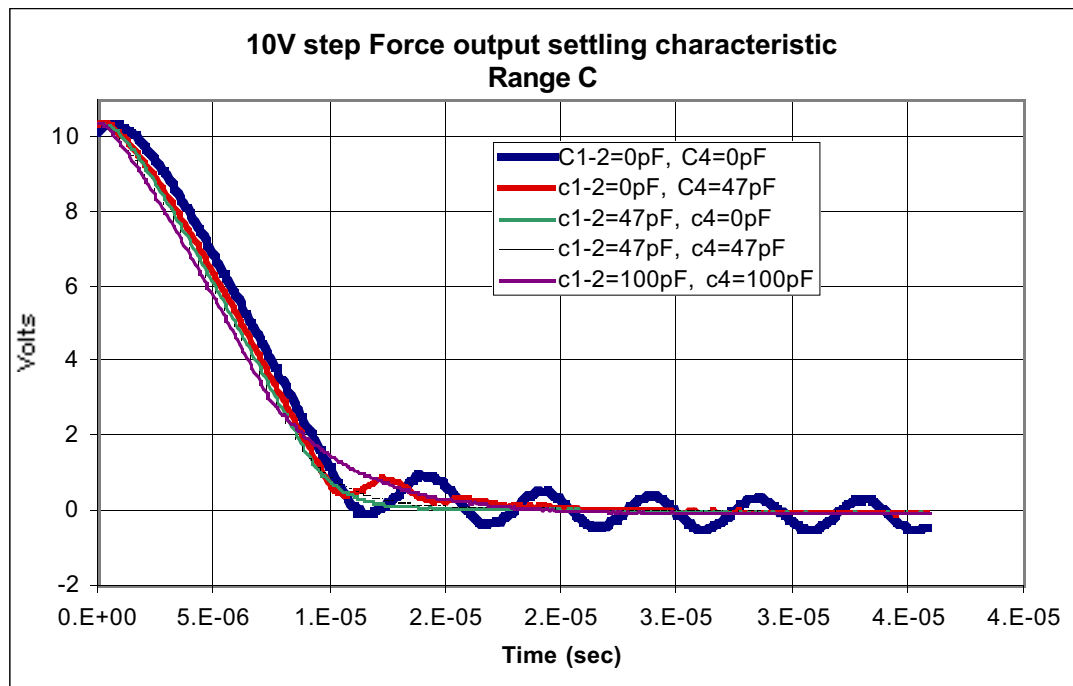


Figure 4. Range C (200 μ A) Force Output Settling in Force Voltage Mode (CLOAD = 108 pF)

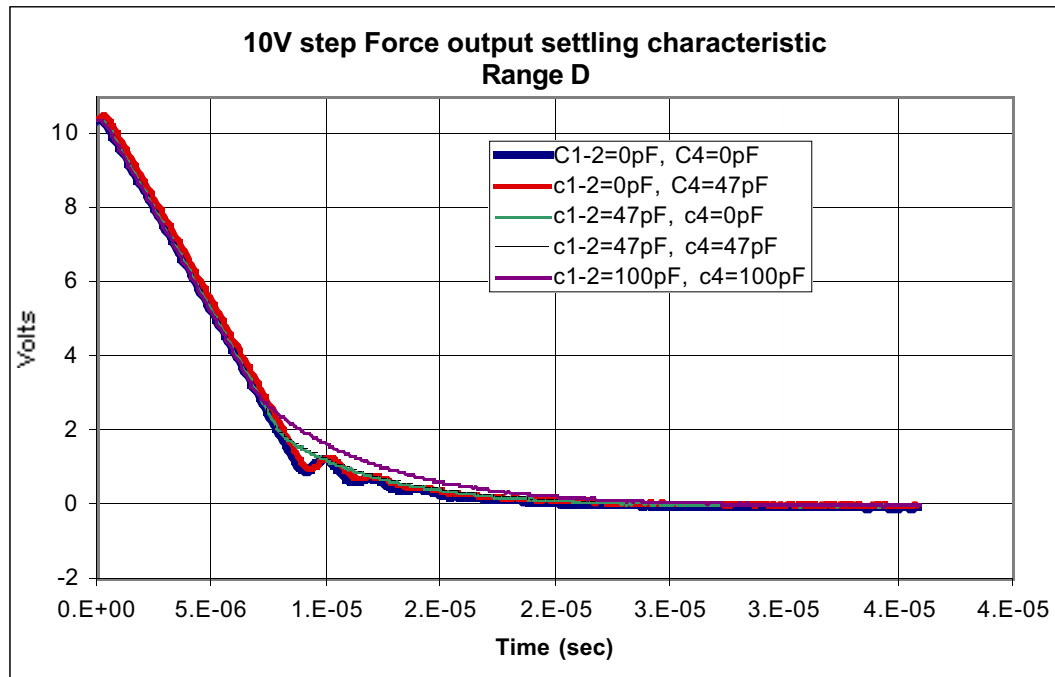


Figure 5. Range D (2mA) Force Output Settling in Force Voltage Mode (CLOAD = 108 pF)

Slew Rate Component

As can be seen from Figures 2 through 5, the values of the compensation capacitors (COMP1-2 and COMP4) have virtually no effect on the output slew rate except on the lowest current range. However, as will be seen later, these capacitors have a marked effect on the final settling time as well as stability on all ranges. Therefore, it is recommended that these capacitors **not** be modified to optimize the Range A slew rate in most applications.

In most situations, the driver amplifier slew rate has the greatest impact on the total settling time when the output voltage step is large and one of the lower current ranges

is selected. Figure 6 shows settling with varying the FORCE output voltage step size. On ranges C and D the step size has little effect on settling time. However, the step size has significant impact on the settling time on the two lower current ranges. To optimize system performance, it is therefore recommended that the voltage step size be minimized on the two lower current ranges whenever possible (Note: all information presented here was obtained using the sense resistors recommended in the Edge4707B data sheet. Any change in these resistor values may significantly change the performance described here).

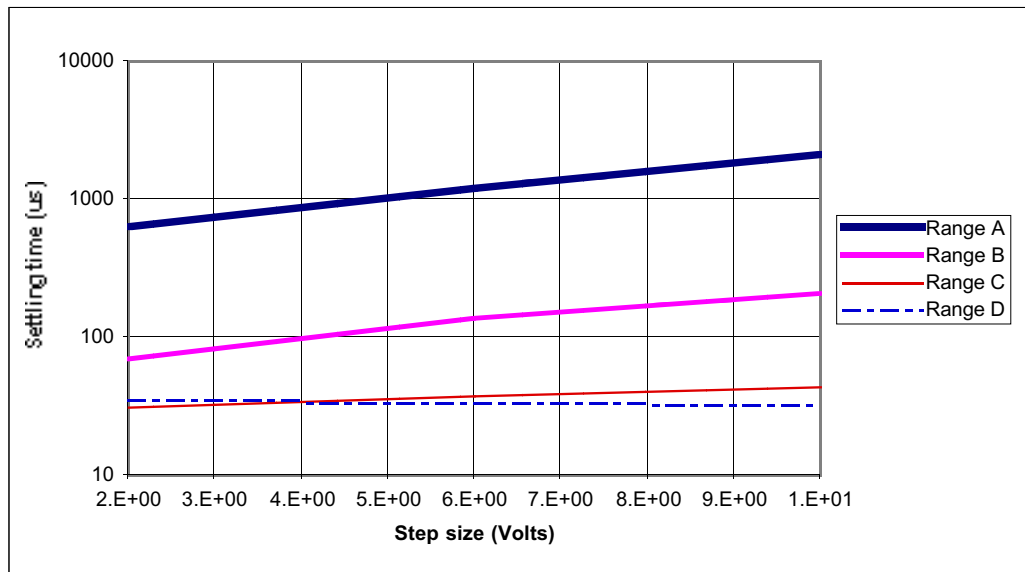


Figure 6. 0.1% IVMON Settling Time vs. Voltage Step Amplitude on Force Output (COMP1-2 = 22 pF, COMP4 = 47 pF, 100 pF Load Capacitance on Force Output)

Final Settling/Small Signal Component

The small signal portion of the settling time is the period when the output voltage is in the vicinity of the final voltage, and the slew rate is decreasing as the output voltage approaches its final value. How long this period is depends on the amount of accuracy desired. Settling times to 12-bit accuracy (0.025%) can take much longer than settling to only 1% accuracy. In this paper, a settling time accuracy of 0.1% of full scale is used as a common standard. In general, the 12-bit settling times of the Edge4707B are not much longer than the 0.1% settling times, except on Range A, which can be considerably longer due to the R-C time constant caused by the large sense resistor.

The small signal portion of the settling time is the one which is most effected by the compensation capacitors. In general, the settling time increases both when the selected compensation capacitors cause a significant amount of overshoot and ringing, or when the capacitors are so large that there is a slow and smooth approach to the final voltage. Finding compensation capacitor values

which cause very little ringing, then increasing their values so the ringing is just barely eliminated will generally give the optimum settling times. Unfortunately, as mentioned earlier, the optimum values will be different for each current range, so compromise values must be selected. The following discussion explains the causes of the ringing and the effect of the different compensation capacitors on the ringing and small signal settling times.

The condition when the output has some overshoot and ringing is called underdamped. This is the case where the compensation capacitors are smaller than optimum. The condition where the output approaches the final value slowly (with no overshoot or ringing) is called overdamped. In this case the compensation capacitors provide much more feedback than is needed, so the output responds slower than optimum. The ideal case is referred to as critically damped. This is when the compensation capacitors are just large enough to keep the circuit from ringing.

The COMP1-2 capacitor shown in Figure 1 provides negative feedback to the Driver Amplifier at short time intervals. This keeps the Driver Amplifier stable until the R-C time constant caused by the sense resistor and capacitance on the FORCE output begins to provide feedback through the SENSE input. Small capacitor values provide less feedback which allows the Driver to operate faster, but also yield more overshoot and ringing at the FORCE and IVMON outputs. If the amplitude of the ringing is larger than the accuracy of the desired measurement, this will increase the time needed before the measurement can be made. Larger capacitors can reduce or eliminate the overshoot, but also slow down the response time, which increases the final settling time. So, as the value of this compensation capacitor is increased (starting at a very low capacitance), the settling time usually increases while the amount of overshoot and ringing increases. Table 1 shows typical IVMON output settling times for a 2V step on FORCE output. As described earlier, the value of this compensation capacitor has less effect on larger step sizes. The optimum capacitor will vary depending on other factors such as load capacitance on the FORCE output, the amount of overshoot which is acceptable in the application, and the accuracy of the desired measurement. Note that since continually decreasing COMP1-COMP2 increases the overshoot and ringing, reducing this capacitor too much will eventually cause increased settling time. If this capacitor is eliminated entirely, settling time becomes infinite on ranges B and C because the ringing never dampens out.

CCOMP1-2 (pF)	Range A (μs)	Range B (μs)	Range C (μs)	Range D (μs)
0	464	61.6	29.8	33.4
22	496	65.2	30.6	34.8
33	536	45.2	31.4	35.8
47	616	66.4	35.6	40.8
68	704	87.6	46.0	50.8
100	792	80.4	68.8	71.6

Table 1. 0.1% Measure Current (IVMON) Settling Time Change with Changing COMP1-2 Capacitance (COMP4 = 22pF, Load Capacitance = 100pF, Force Step Voltage = 2V)

The COMP4 capacitor is in parallel with the external sense resistor when in Force Voltage mode, as shown in Figure 1. This capacitor is disconnected from the circuit by an internal switch when the Edge4707B is in the Force Current mode. The purpose of this capacitor is to allow fast-slewing signals to bypass the sense resistor, which improves the slew rate at the FORCE output. This has the greatest effect when the sense resistor is large, such as on Range A or B. Typical variation of IVMON settling time with changing COMP4 capacitor value is shown in Table 2.

CCOMP4 (pF)	Range A (μs)	Range B (μs)	Range C (μs)	Range D (μs)
22	496	65.2	30.6	34.8
33	524	63.2	30.8	35.6
47	608	69.6	30.4	34.6
68	712	81.6	31.6	35.0
100	792	93.6	32.2	34.6

Table 2. IVMON Settling Time with Changing COMP4 Capacitor Value. (COMP1-2=22, Load Cap=108pF, Force Step Size=2V)

Note that while increasing the size of this capacitor improves the settling time on the lowest current ranges, it can also degrade the settling time on the higher current ranges. The reason is that this capacitor acts as an impedance in parallel with the sense resistor. When the output voltage of the Driver Amplifier suddenly changes, the impedance of this capacitor will be relatively low, so the impedance across which the differential amplifier is measuring will be less than the sense resistor value. After a period of time, the current through the capacitor will decrease and the impedance increase. After enough time has elapsed, the impedance of the parallel capacitor becomes high enough so its contribution can be ignored. Larger capacitors have lower impedances at identical frequencies, so the larger capacitors have longer delay times before their contribution to the measurement impedance can be ignored. This contribution is significant on the higher current ranges primarily due to the shorter settling times of these ranges. The optimum value for this capacitor will then depend on how often the low versus

high current ranges will be used in a test system. Settling times with additional compensation capacitor combinations can be found in Appendix 1.

(Note that as the Force Voltage step size increases, COMP4 makes less difference on settling time in any range. At the largest step sizes (~5V or larger), the slew time is long enough for the impedance of the COMP4 capacitor to become negligible. COMP4 capacitance also makes no difference in the Force Current mode since it is removed from the circuit in this mode. This is done because the source impedance should be as high as possible in the force current mode, while the source impedance should be as low as possible in the Force Voltage mode.)

Table 3 shows the 0.1% settling times associated with various load capacitance on the FORCE output with fixed compensation capacitor values. As expected, this load capacitance has a greater effect on the lower current ranges because of the increased R-C time constant due to the larger sense resistors. This effect can be reduced by using a larger COMP4 capacitance in situations which have large load capacitance on Force.

CFORCE (pF)	Range A (µs)	Range B (µs)	Range C (µs)	Range D (µs)
58	1820	198	43.6	32.8
108	2100	206	44.0	32.6
158	2240	214	45.6	32.4
388	6960	704	87.2	29.8
608	8800	912	122.0	26.0
1298	17000	2160	258.0	44.8

Table 3. Change in Settling Time with Changing Load Capacitance (COMP1-2=22pF, COMP4=47pF, Step Size=10V)

(Side note: The settling time is not increased with IVMON load capacitance up to 3000pF. This is because the output impedance of the IVMON output is much less than the output impedance of the FORCE output.)

Stability

Stability is dependent primarily on having adequate compensation capacitors in the circuit. The amount of compensation required for stability is partially dependent on the amount of capacitance being driven by the driver amplifier. This includes the capacitance on the FORCE/SENSE output node as well as the capacitance on E_SN_IN and E_FC_IN if these are switched in. (See Edge4707B datasheet for description). With no compensation caps, the Edge4707B is only stable on Range D, even with very small output capacitance. Therefore, compensation caps are required in most applications. However, even with compensation caps as small as 22pF, the Edge4707B is stable with a FORCE output load capacitance as large as 1µF. This means that any overshoot and ringing will eventually settle out. This does not mean that there is no overshoot or ringing on the output. In fact, as seen above, there is overshoot and ringing under many different compensation capacitor and load capacitor combinations.

The amount of ringing on the FORCE output is important because it is possible that the voltage overshoot when changing output voltages can go beyond the allowable voltage range on the DUT, causing stress on the part or even failure. For instance, when testing input leakage on a 5V part, it is common to test the leakage at 0V and 5V only. When changing from one voltage to the other, it is desirable to keep the overshoot to less than 0.7V to keep the input voltage from exceeding the maximum allowable voltage relative to VCC and GND.

Since the Edge4707B forces only relatively low currents (<10mA), and since most test devices have ESD protection diodes which can handle much more current than this for short periods of time, this overshoot will not be an issue in most cases. This will be especially true when using the lower current ranges on the Edge4707B. However, if the DUT is especially sensitive, care must be taken in selecting the COMP cap values to keep the overshoot to within acceptable limits.

The amount of overshoot on the FORCE/SENSE output node is dependent on a number of variables. The sense resistor value, voltage step size, compensation capacitor values and load capacitance all influence the amount of

overshoot. Figures 2 through 5 (above) show qualitatively how the amount of overshoot is reduced as the compensation capacitors are increased for each range. Table 4 (below) lists the peak overshoot on each range for a 10V to 0V step, a force load capacitance of 100pF and a variety of compensation capacitors. Note that under these conditions, Range B always has the largest amount of overshoot. As will be shown later, this is not always the case with larger amounts of capacitance on the FORCE output node. But, in designs which have small amounts of Force capacitance < ~200pF), the overshoot on Range B can often be ignored since the compliance current on this range is normally only about 20 μ A, which is insufficient to cause any stress on the vast majority of test devices.

CCOMP1-2 (pF)	CCOMP4 (pF)	Range A (μ s)	Range B (μ s)	Range C (μ s)	Range D (μ s)
22	0	-0.33406	-1.4575	-0.07813	-0.07844
22	22	-0.27938	-1.27781	-0.07	-0.07719
22	47	-0.25906	-1.15	-0.06281	-0.07719
22	100	-0.23281	-0.91625	-0.0675	-0.06281
47	0	-0.29594	-1.43813	-0.05063	-0.04469
47	22	-0.26156	-1.31	-0.03563	-0.04188
47	47	-0.24625	-1.18312	-0.065	-0.04313
47	100	-0.22188	-0.47906	-0.06281	-0.0575
100	0	-0.30594	-1.36281	-0.08031	-0.04438
100	22	-0.28156	-0.88438	-0.075	-0.03125
100	47	-0.26563	-0.69969	-0.07719	-0.03094
100	100	-0.21219	-0.48219	-0.06906	-0.03938

Table 4. Overshoot vs. Compensation Capacitor Values for a 10V-0V Step with 100pF load capacitance.

Figure 7 shows the increasing overshoot on Range B as the amplitude of the voltage step is increased. This change in overshoot happens when the circuit is underdamped and inclined towards overshoot. If the circuit is overdamped so that the output goes to the final voltage without any overshoot at low voltages, there will normally

be no change to an overshoot characteristic with increasing voltage step size. So if guaranteeing no excessive overshoot is needed, then relatively large compensation capacitors should be selected so no overshoot is seen on any range at low voltages. This will ensure no overshoot even with large step sizes.

Overshoot is also a function of output capacitance. Increasing output capacitance can either increase or decrease the amount of overshoot depending on other conditions. Increasing load capacitance increases the R-C time constant of the output node which slows down the response time at the output, which tends to reduce the amplitude of any transients, including overshoot. On the other hand, this reduced response at the output also means there is less signal feedback from the sense line. Less external feedback requires more feedback from the compensation network in order to have the same amount of stability. Since the amount of compensation feedback is fixed with fixed feedback capacitors, this means that circuit characteristic can go from having little or no overshoot to having significant amounts of overshoot as the circuit shifts from being overdamped to being underdamped.

(Note: some overshoot can occur in the overdamped situation when in Force voltage mode due to capacitive coupling to the FORCE output though the COMP4 capacitor. This occurs primarily on Ranges A and B. It cannot be entirely eliminated, but is small enough to be ignored for most applications).

For COMP1-2 capacitance of 22pF and COMP4 capacitance of 47pF, the overshoot on ranges A and B decrease with increasing load capacitance. (See the graph in Figure 8). This indicates that these ranges already have overshoot and ringing due to being underdamped with these compensation capacitors, even with the smallest output capacitance. Therefore, the dominating factor on these ranges is the reduction in overshoot due to the R-C time constant.

The overshoot on ranges C and D is initially zero with small load capacitance, indicating that the circuit is overdamped on these ranges under these conditions. (See Figure 8). As the load capacitance increases, overshoot occurs first

on range C, then on range D as the circuits shift to being underdamped. The amount of overshoot increases until the reduction in amplitude due to the R-C time constant begins to dominate. After this point, the amount of overshoot decreases with increasing load capacitance as seen on ranges A and B.

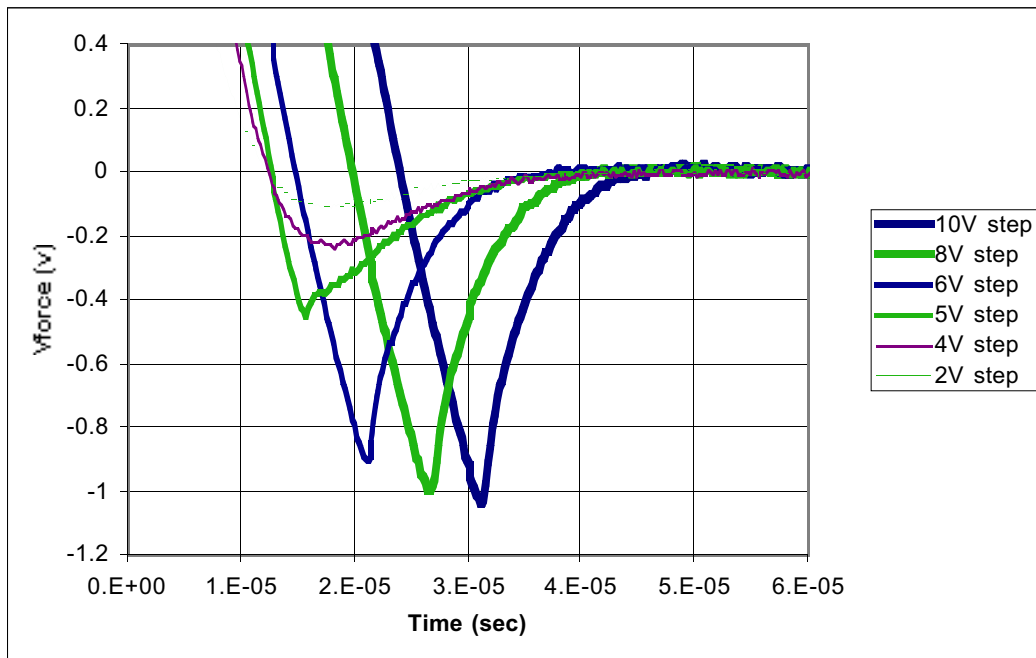


Figure 7. Overshoot vs. input Step Amplitude on Range B (20 μ A) with COMP1-2=22pF, COMP4=47pF and Load Capacitance=100pF

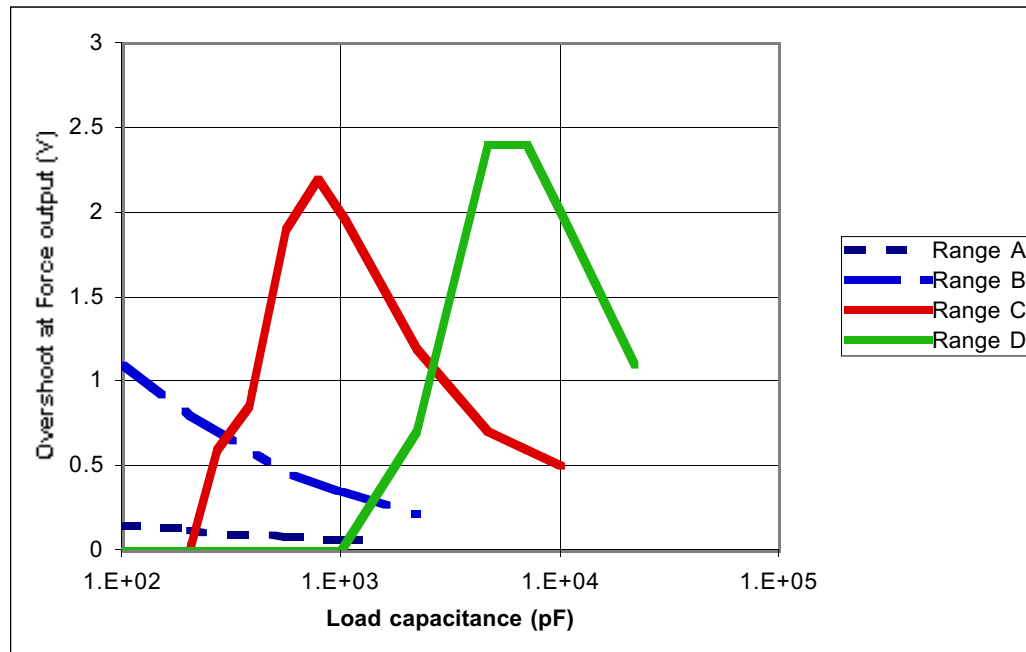


Figure 8. Overshoot as a Function of Force Output Load Capacitance for COMP1-2=22pF and COMP4=47pF, Step Amplitude = 10V.

Examples

Given all the information above, the question now is how to choose the optimum compensation capacitors for a given application. Below are a couple of examples of how to go about this.

Example1:

What compensation capacitors should be used to get the fastest overall settling time in a test system with less than 200pF of capacitance on the DUT node while keeping the overshoot at the DUT to less than 700mV with step sizes as large as 10V?

Since the load capacitance is less than 200pF, Figure 8 shows that Range B will probably have the worst overshoot. The overshoot number in Table 4 confirm this and show three compensation capacitor combinations which will satisfy this requirement: COMP1-2=47pF and

COMP4=100pF, COMP1-2=100pF and COMP4=47pF, COMP1-2=100pF and COMP4=100pF. Since the overshoot using COMP1-2=100pF and COMP4=47pF is only slightly below the 0.7V limit, this option should be discarded as not having enough safety margin. The tables in Appendix 1 show that the settling times using COMP1-2=47 pF and COMP4=100pF are slightly faster than with COMP1-2=100pF (this difference will be greater with smaller step sizes), so COMP1-2=47pF is the preferred value. (Note: to further reduce the amount of overshoot, increasing the COMP4 value should be tried first since Table 4 indicates that increasing this capacitor has a larger effect on the amount of overshoot than the COMP1-2 capacitor.

Example 2:

The test system needs to be designed with compensation capacitors of COMP1-2=22pF and COMP4=47pF in order to get the fastest settling times under most circumstances. However, the user may put a bypass capacitor next to the DUT pin as large as 0.01 μ f. With this capacitance range, what should be the maximum voltage step to keep the overshoot less than 700mV?

Figure 8 indicates that Range D may have as much as 2.5V of overshoot (with a 10V step) within this range of load capacitance. Figure 7 indicates that the change in overshoot is proportional to voltage step size, but not exactly linear. So limiting the step size to 2V will likely limit the maximum overshoot to 0.5V, but this will have to be verified using an EVM board or with the final circuit.

Summary

The bottom line is that there will always be a trade-off between fast settling time, maximum accuracy and keeping overshoot and ringing low enough so there is no risk of damaging DUTs. The final decision on appropriate compensation capacitors for a given design should take all of these factors into account when determining the optimum compensation for a particular design.

Appendix 1.
**Edge4707B Settling Times with
 Various Compensation Capacitors**

(Load Capacitance = 100pF, Voltage Step Size = 10V)

CCOMP1-2 (pF)	CCOMP4 (pF)	Range A (μs)	Range B (μs)	Range C (μs)	Range D (μs)
0	0	0sc	0sc	0sc	31.4
0	22	2160	220	60.4	32.0
0	47	2140	226	45.2	31.6
0	100	2360	242	46.0	31.8

CCOMP1-2 (pF)	CCOMP4 (pF)	Range A (μs)	Range B (μs)	Range C (μs)	Range D (μs)
22	0	2140	210	44.4	31.8
22	22	2340	228	45.6	31.8
22	47	2180	236	46.4	31.6
22	100	2160	232	46.4	31.8

CCOMP1-2 (pF)	CCOMP4 (pF)	Range A (μs)	Range B (μs)	Range C (μs)	Range D (μs)
47	0	2340	226	44.0	31.6
47	22	2340	232	45.2	32.0
47	47	2360	228	46.0	32.0
47	100	2200	238	47.2	32.2

CCOMP1-2 (pF)	CCOMP4 (pF)	Range A (μs)	Range B (μs)	Range C (μs)	Range D (μs)
100	0	2180	222	48.0	37.4
100	22	2280	238	48.0	38.0
100	47	2320	230	48.8	37.8
100	100	2250	242	50.4	38.0