MH32S64PFJ -6, -6L -7,-7L

2147483648-BIT (33554432 - WORD BY 64-BIT)SynchronousDRAM

DESCRIPTION

The MH32S64PFJ is 33554432 - word by 64-bit Synchronous DRAM module. This consists of eight industry standard 16Mx16 Synchronous DRAMs in TSOP and one industory standard EEPROM in TSSOP.

The mounting of TSOP on a card edge Dual Inline package provides any application where high densities and large quantities of memory are required.

This is a socket type - memory modules, suitable for easy interchange or addition of modules.

FEATURES

	Frequency	CLK Access Time (Component SDRAM)
-6,-6L	133MHz	5.4ns(CL=3)
-7,-7L	100MHz	6.0ns(CL=2)

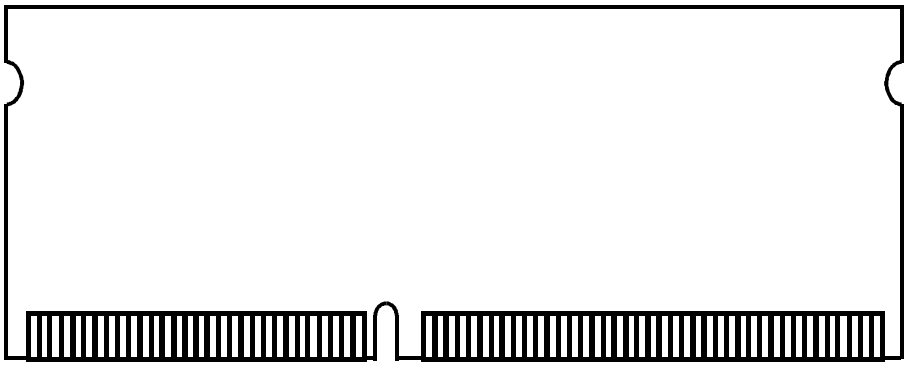
PC133/100 Compliant

- Utilizes industry standard 16M x 16 Synchronous DRAMs TSOP and industry standard EEPROM in TSSOP
- 144-pin (72-pin dual in-line package)
- single 3.3V±0.3V power supply
- Fully synchronous operation referenced to clock rising edge
- 4 bank operation controlled by BA0,1(Bank Address)
- /CAS latency- 2/3(programmable)
- Burst length- 1/2/4/8/Full Page(programmable)
- Burst type- sequential / interleave(programmable)
- Column access - random
- Auto precharge / All bank precharge controlled by A10
- Auto refresh and Self refresh
- 8192 refresh cycle /64ms
- LVTTL Interface

APPLICATION

main memory or graphic memory in computer systems

PCB Outline



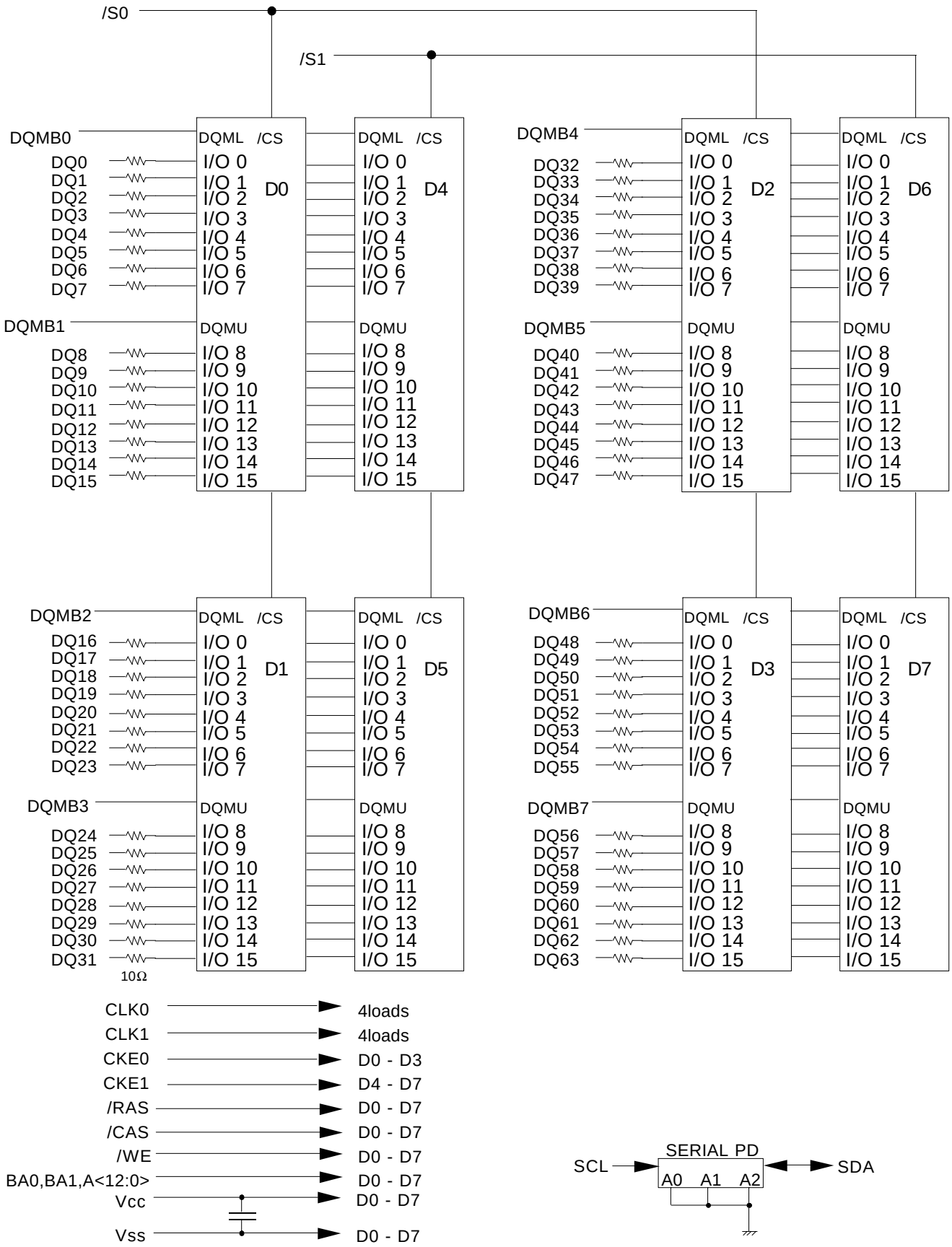
(Front) 1 143
(Back) 2 144

PIN CONFIGURATION

PIN Number	Front side Pin Name	PIN Number	Back side Pin Name	PIN Number	Front side Pin Name	PIN Number	Back side Pin Name
1	Vss	2	Vss	73	Reserved	74	CLK1
3	DQ0	4	DQ32	75	Vss	76	Vss
5	DQ1	6	DQ33	77	Reserved	78	Reserved
7	DQ2	8	DQ34	79	Reserved	80	Reserved
9	DQ3	10	DQ35	81	Vcc	82	Vcc
11	Vcc	12	Vcc	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	Vss	92	Vss
21	Vss	22	Vss	93	DQ20	94	DQ52
23	DQMB0	24	DQMB4	95	DQ21	96	DQ53
25	DQMB1	26	DQMB5	97	DQ22	98	DQ54
27	Vcc	28	Vcc	99	DQ23	100	DQ55
29	A0	30	A3	101	Vcc	102	Vcc
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	Vss	36	Vss	107	Vss	108	Vss
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10	112	A11
41	DQ10	42	DQ42	113	Vcc	114	Vcc
43	DQ11	44	DQ43	115	DQMB2	116	DQMB6
45	Vcc	46	Vcc	117	DQMB3	118	DQMB7
47	DQ12	48	DQ44	119	Vss	120	Vss
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	Vss	56	Vss	127	DQ27	128	DQ59
57	Reserved	58	Reserved	129	Vcc	130	Vcc
59	Reserved	60	Reserved	131	DQ28	132	DQ60
61	CLK0	62	CKE0	133	DQ29	134	DQ61
63	Vcc	64	Vcc	135	DQ30	136	DQ62
65	/RAS	66	/CAS	137	DQ31	138	DQ63
67	/WE	68	CKE1	139	Vss	140	Vss
69	/S0	70	A12	141	SDA	142	SCL
71	/S1	72	A13	143	Vcc	144	Vcc

NC = No Connection

Block Diagram



Serial Presence Detect Table I

Byte	Function described		SPD enrty data	SPD DATA(hex)
0	Defines # bytes written into serial memory at module mfgr		128	80
1	Total # bytes of SPD memory device		256 Bytes	08
2	Fundamental memory type		SDRAM	04
3	# Row Addresses on this assembly		A0-A12	0D
4	# Column Addresses on this assembly		A0-A8	09
5	# Module Banks on this assembly		2BANK	02
6	Data Width of this assembly...		x64	40
7	... Data Width continuation		0	00
8	Voltage interface standard of this assembly		LVTTL	01
9	SDRAM Cycletime at Max. Supported CAS Latency (CL). Cycle time for CL=3	-6	7.5ns	75
		-7	10ns	A0
10	SDRAM Access from Clock tAC for CL=3	-6	5.4ns	54
		-7	6ns	60
11	DIMM Configuration type (Non-parity,Parity,ECC)		Non-PARITY	00
12	Refresh Rate/Type		self refresh(7.8125uS)	82
13	SDRAM width,Primary DRAM		x16	10
14	Error Checking SDRAM data width		N/A	00
15	Minimum Clock Delay,Back to Back Random Column Addresses		1	01
16	Burst Lengths Supported		1/2/4/8/Full page	8F
17	# Banks on Each SDRAM device		4bank	04
18	CAS# Latency		2/3	06
19	CS# Latency		0	01
20	Write Latency		0	01
21	SDRAM Module Attributes		non-buffered,non-registered	00
22	SDRAM Device Attributes:General		Precharge All,Auto precharge	0E
23	SDRAM Cycle time(2nd highest CAS latency) Cycle time for CL=2	-6	10ns	A0
		-7	10ns	A0
24	SDRAM Access form Clock(2nd highest CAS latency) tAC for CL=2	-6	6ns	60
		-7	6ns	60
25	SDRAM Cycle time(3rd highest CAS latency)		N/A	00
26	SDRAM Access form Clock(3rd highest CAS latency)		N/A	00
27	Precharge to Active Minimum		20ns	14
28	Row Active to Row Active Min.	-6	15ns	0F
		-7	20ns	14
29	RAS to CAS Delay Min		20ns	14
30	Active to Precharge Min	-6	45ns	2D
		-7	50ns	32

Serial Presence Detect Table II

31	Density of each bank on module		128MByte	20
32	Command and Address signal input setup time	-6	1.5ns	15
		-7	2ns	20
33	Command and Address signal input hold time	-6	0.8ns	08
		-7	1ns	10
34	Data signal input setup time	-6	1.5ns	15
		-7	2ns	20
35	Data signal input hold time	-6	0.8ns	08
		-7	1ns	10
36-61	Superset Information (may be used in future)		option	00
62	SPD Revision		rev 1.2B	12
63	Checksum for bytes 0-62		Check sum for -6	BA
			Check sum for -7	21
64-71	Manufactures Jedec ID code per JEP-108E		MITSUBISHI	1CFFFFFFFFFFFFFF
72	Manufacturing location		Miyoshi,Japan	01
			Tajima,Japan	02
			NC,USA	03
			Germany	04
73-90	Manufactures Part Number		MH32S64PFJ-6	4D48333253363450464A2D36202020202020
			MH32S64PFJ-6L	4D48333253363450464A2D364C2020202020
			MH32S64PFJ-7	4D48333253363450464A2D37202020202020
			MH32S64PFJ-7L	4D48333253363450464A2D374C2020202020
91-92	Revision Code		PCB revision	rrrr
93-94	Manufacturing date		year/week code	yyww
95-98	Assembly Serial Number		serial number	ssssssss
99-125	Manufacture Specific Data		option	00
126	Intetl specification frequency		100MHz	64
127	Intel specification CAS# Latency support	-6,-7	CL=2/3,AP,CK0,1	CF
128+	Unused storage locations		open	00

The -6, -7 indicate also -6L, -7L.

PIN FUNCTION

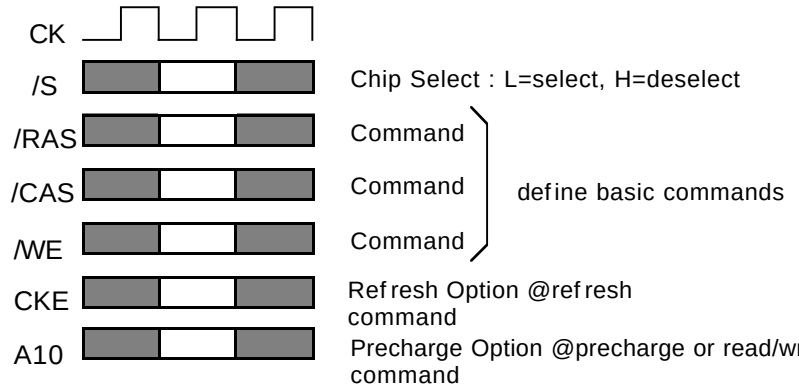
CLK0, CLK1	Input	Master Clock:All other inputs are referenced to the rising edge of CK
CKE0 CKE1	Input	Clock Enable:CKE controls internal clock.When CKE is low,internal clock for the following cycle is ceased. CKE is also used to select auto / self refresh. After self refresh mode is started, CKE E becomes asynchronous input.Self refresh is maintained as long as CKE is low.
/S0, /S1	Input	Chip Select: When /S is high,any command means No Operation.
/RAS,/CAS,/WE	Input	Combination of /RAS,/CAS,/WE defines basic commands.
A0-12	Input	A0-12 specify the Row/Column Address in conjunction with BA0,1.The Row Address is specified by A0-12.The Column Address is specified by A0-8.A10 is also used to indicate precharge option.When A10 is high at a read / write command, an auto precharge is performed. When A10 is high at a precharge command, both banks are precharged.
BA0,1	Input	Bank Address:BA0,1 is not simply BA.BA specifies the bank to which a command is applied.BA0,1 must be set with ACT,PRE,READ,WRITE commands
DQ0-63	Input/Output	Data In and Data out are referenced to the rising edge of CLK
DQMB0-7	Input	Din Mask/Output Disable:When DQMB is high in burst write.Din for the current cycle is masked.When DQMB is high in burst read,Dout is disabled at the next but one cycle.
Vdd,Vss	Power Supply	Power Supply for the memory mounted module.
SCL	Input	Serial clock for serial PD
SDA	Output	Serial data for serial PD

BASIC FUNCTIONS

The MH32S64PFJ provides basic functions,bank(row)activate,burst read / write, bank(row) precharge,and auto / self refresh.

Each command is defined by control signals of /RAS,/CAS and /WE at CLK rising edge. In addition to 3 signals,/S,CKE and A10 are used as chip select,refresh option,and precharge option,respectively.

To know the detailed definition of commands please see the command truth table.



Activate(ACT) [/RAS =L, /CAS = /WE =H]

ACT command activates a row in an idle bank indicated by BA.

Read(READ) [/RAS =H,/CAS =L, /WE =H]

READ command starts burst read from the active bank indicated by BA.First output data appears after /CAS latency. When A10 =H at this command,the bank is deactivated after the burst read(auto-precharge,**READA**).

Write(WRITE) [/RAS =H, /CAS = /WE =L]

WRITE command starts burst write to the active bank indicated by BA. Total data length to be written is set by burst length. When A10 =H at this command, the bank is deactivated after the burst write(auto-precharge,**WRITEA**).

Precharge(PRE) [/RAS =L, /CAS =H,/WE =L]

PRE command deactivates the active bank indicated by BA. This command also terminates burst read / write operation. When A10 =H at this command, both banks are deactivated(precharge all, **PREA**).

Auto-Refresh(REFA) [/RAS =/CAS =L, /WE =CKE =H]

PEFA command starts auto-refresh cycle. Refresh address including bank address are generated internally. After this command, the banks are precharged automatically.

COMMAND TRUTH TABLE

COMMAND	MNEMONIC	CKE n-1	CKE n	/S	/RAS	/CAS	/WE	BA0,1	A10	A0-9, 11-12	note
Deselect	DESEL	H	X	H	X	X	X	X	X	X	
No Operation	NOP	H	X	L	H	H	H	X	X	X	
Row Adress Entry & Bank Activate	ACT	H	X	L	L	H	H	V	V	V	
Single Bank Precharge	PRE	H	X	L	L	H	L	V	L	X	
Precharge All Bank	PREA	H	X	L	L	H	L	X	H	X	
Column Address Entry & Write	WRITE	H	X	L	H	L	L	V	L	V	
Column Address Entry & Write with Auto-Precharge	WRITEA	H	X	L	H	L	L	V	H	V	
Column Address Entry & Read	READ	H	X	L	H	L	H	V	L	V	
Column Address Entry & Read with Auto Precharge	READA	H	X	L	H	L	H	V	H	V	
Auto-Refresh	REFA	H	H	L	L	L	H	X	X	X	
Self-Refresh Entry	REFS	H	L	L	L	L	H	X	X	X	
Self-Refresh Exit	REFSX	L	H	H	X	X	X	X	X	X	
		L	H	L	H	H	H	X	X	X	
Burst Terminate	TERM	H	X	L	H	H	L	X	X	X	
Mode Register Set	MRS	H	X	L	L	L	L	L	L	V	1

H =High Level, L = Low Level, V = Valid, X = Don't Care, n = CLK cycle number

NOTE:
1.A7-8,11-12 = L, A0-6,A9 = Mode Address

FUNCTION TRUTH TABLE

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action
IDLE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TBST	ILLEGAL*2
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA,RA	ACT	Bank Active,Latch RA
	L	L	H	L	BA,A10	PRE/PREA	NOP*4
	L	L	L	H	X	REFA	Auto-Refresh*5
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode Register Set*5
ROW ACTIVE	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TBST	NOP
	L	H	L	H	BA,CA,A10	READ/READA	Begin Read,Latch CA, Determine Auto-Precharge
	L	H	L	L	BA,CA,A10	WRITE/ WRITEA	Begin Write,Latch CA, Determine Auto-Precharge
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	Precharge/Precharge All
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	X	TBST	Terminate Burst
	L	H	L	H	BA,CA,A10	READ/READA	Terminate Burst,Latch CA, Begin New Read,Determine Auto-Precharge*3
	L	H	L	L	BA,CA,A10	WRITE/WRITEA	Terminate Burst,Latch CA, Begin Write,Determine Auto-Precharge*3
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	Terminate Burst,Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action
WRITE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	X	TBST	Terminate Burst
	L	H	L	H	BA,CA,A10	READ/READA	Terminate Burst,Latch CA, Begin Read,Determine Auto-Precharge*3
	L	H	L	L	BA,CA,A10	WRITE/ WRITEA	Terminate Burst,Latch CA, Begin Write,Determine Auto-Precharge*3
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	Terminate Burst,Precharge
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
READ with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL
	L	H	L	L	BA,CA,A10	WRITE/ WRITEA	ILLEGAL
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE with AUTO PRECHARGE	H	X	X	X	X	DESEL	NOP(Continue Burst to END)
	L	H	H	H	X	NOP	NOP(Continue Burst to END)
	L	H	H	L	X	TBST	ILLEGAL
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL
	L	H	L	L	BA,CA,A10	WRITE/ WRITEA	ILLEGAL
	L	L	H	H	BA,RA	ACT	Bank Active/ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action
PRE - CHARGING	H	X	X	X	X	DESEL	NOP(Idle after tRP)
	L	H	H	H	X	NOP	NOP(Idle after tRP)
	L	H	H	L	X	TBST	ILLEGAL*2
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA,RA	ACT	ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	NOP*4(Idle after tRP)
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
ROW ACTIVATING	H	X	X	X	X	DESEL	NOP(Row Active after tRCD
	L	H	H	H	X	NOP	NOP(Row Active after tRCD
	L	H	H	L	X	TBST	ILLEGAL*2
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA,RA	ACT	ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
WRITE RE-COVERING	H	X	X	X	X	DESEL	NOP
	L	H	H	H	X	NOP	NOP
	L	H	H	L	X	TBST	ILLEGAL*2
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL*2
	L	L	H	H	BA,RA	ACT	ILLEGAL*2
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL*2
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

FUNCTION TRUTH TABLE(continued)

Current State	/S	/RAS	/CAS	/WE	Address	Command	Action
RE-	H	X	X	X	X	DESEL	NOP(Idle after tRC)
FRESHING	L	H	H	H	X	NOP	NOP(Idle after tRC)
	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA,RA	ACT	ILLEGAL
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL
MODE	H	X	X	X	X	DESEL	NOP(Idle after tRSC)
REGISTER	L	H	H	H	X	NOP	NOP(Idle after tRSC)
SETTING	L	H	H	L	BA	TBST	ILLEGAL
	L	H	L	X	BA,CA,A10	READ/WRITE	ILLEGAL
	L	L	H	H	BA,RA	ACT	ILLEGAL
	L	L	H	L	BA,A10	PRE/PREA	ILLEGAL
	L	L	L	H	X	REFA	ILLEGAL
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL

ABBREVIATIONS:
H = Hige Level, L = Low Level, X = Don't Care
BA = Bank Address, RA = Row Address, CA = Column Address, NOP = No Operation

NOTES:
1. All entries assume that CKE was High during the preceding clock cycle and the current clock cycle.
2. ILLEGAL to bank in specified state; function may be legal in the bank indicated by BA, depending on the state of that bank.
3. Must satisfy bus contention, bus turn around, write recovery requirements.
4. NOP to bank precharging or in idle state.May precharge bank indicated by BA.
5. ILLEGAL if any bank is not idle.

ILLEGAL = Device operation and / or date-integrity are not guaranteed.

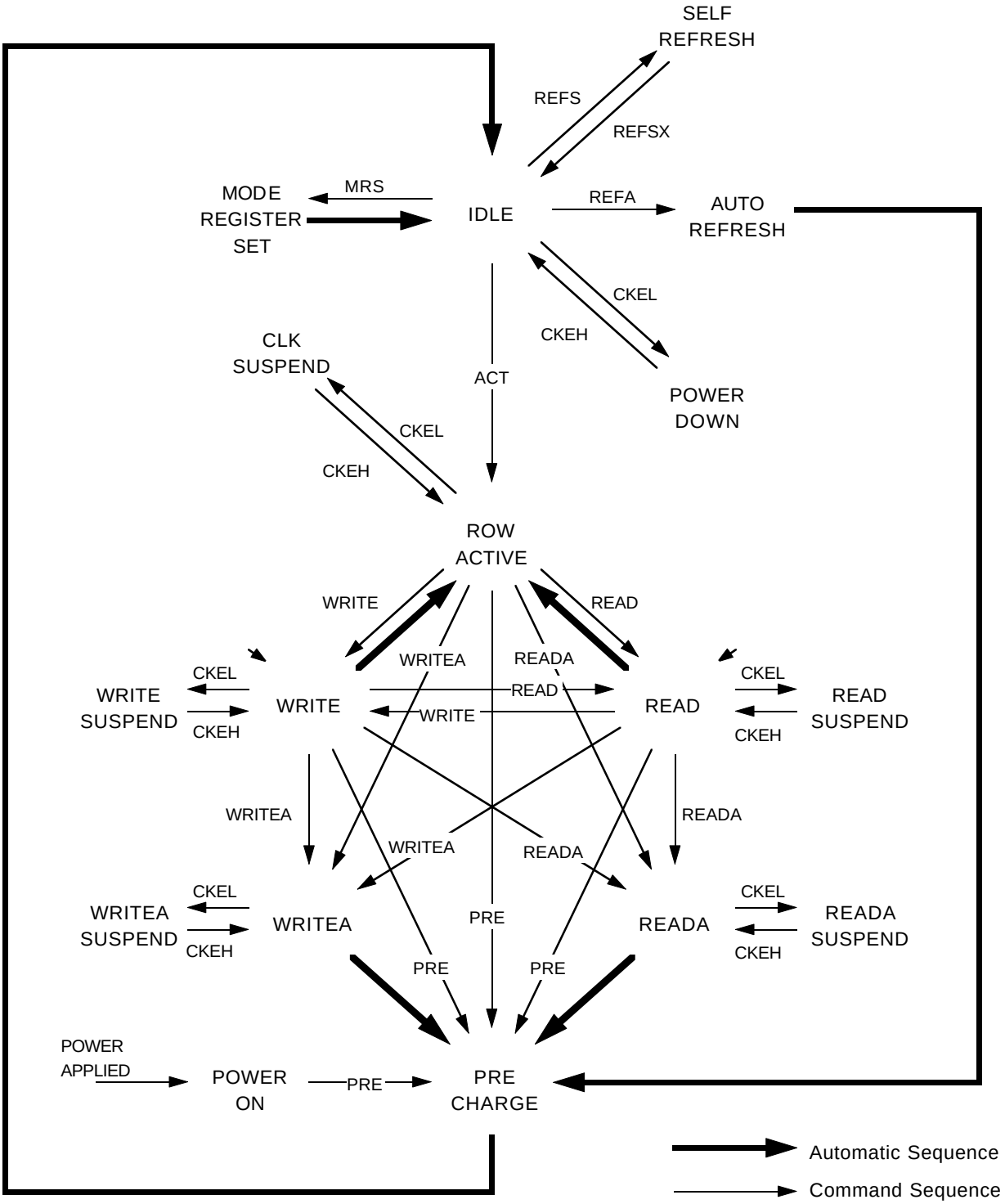
FUNCTION TRUTH TABLE FOR CKE

Current State	CK n-1	CK n	/S	/RAS	/CAS	/WE	Add	Action
SELF - REFRESH*1	H	X	X	X	X	X	X	INVALID
	L	H	H	X	X	X	X	Exit Self-Refresh(Idle after tRC)
	L	H	L	H	H	H	X	Exit Self-Refresh(Idle after tRC)
	L	H	L	H	H	L	X	ILLEGAL
	L	H	L	H	L	X	X	ILLEGAL
	L	H	L	L	X	X	X	ILLEGAL
	L	L	X	X	X	X	X	NOP(Maintain Self-Refresh)
POWER DOWN	H	X	X	X	X	X	X	INVALID
	L	H	X	X	X	X	X	Exit Power Down to Idle
	L	L	X	X	X	X	X	NOP(Maintain Self-Refresh)
ALL BANKS IDLE*2	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	L	L	L	H	X	Enter Self-Refresh
	H	L	H	X	X	X	X	Enter Power Down
	H	L	L	H	H	H	X	Enter Power Down
	H	L	L	H	H	L	X	ILLEGAL
	H	L	L	H	L	X	X	ILLEGAL
	H	L	L	L	X	X	X	ILLEGAL
	L	X	X	X	X	X	X	Refer to Current State = Power Down
ANY STATE other than listed above	H	H	X	X	X	X	X	Refer to Function Truth Table
	H	L	X	X	X	X	X	Begin CK0 Suspend at Next Cycle*3
	L	H	X	X	X	X	X	Exit CK0 Suspend at Next Cycle*3
	L	L	X	X	X	X	X	Maintain CK0 Suspend

ABBREVIATIONS:
H = High Level, L = Low Level, X = Don't Care

NOTES:
1. CKE Low to High transition will re-enable CK and other inputs **asynchronously**.
   A minimum setup time must be satisfied before any command other than EXIT.
2. Power-Down and Self-Refresh can be entered only form the All banks idle State.
3. Must be legal command.

SIMPLIFIED STATE DIAGRAM



POWER ON SEQUENCE

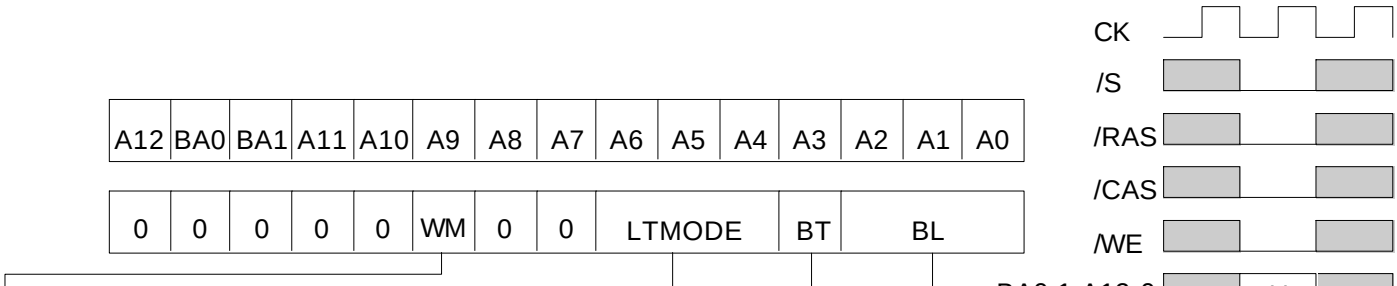
Before starting normal operation, the following power on sequence is necessary to prevent a SDRAM from damaged or malfunctioning.

1. Clock will be applied at power up along with power.Attempt to maintain CKE high,DQM0-7 high and NOP condition at the inputs along with power.
2. Maintain stable power, stable cock, and NOP input conditions for a minimum of 200us.
3. Issue precharge commands for all banks. (PRE or PREA)
4. After all banks become idle state (after tRP), issue 8 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.

After these sequence, the SDRAM is idle state and ready for normal operation.

MODE REGISTER

Burst Length, Burst Type and /CAS Latency can be programmed by setting the mode register(MRS). The mode register stores these date until the next MRS command, which may be issued when both banks are in idle state. After tRSC from a MRS command, the SDRAM is ready for new command.



A12	BA0	BA1	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	0	0	0	0	WM	0	0	LTMODE			BT	BL		

	CL	/CAS LATENCY
LATENCY MODE	0 0 0	R
	0 0 1	R
	0 1 0	2
	0 1 1	3
	1 0 0	R
	1 0 1	R
	1 1 0	R
	1 1 1	R

	BL	BT= 0	BT= 1
BURST LENGTH	0 0 0	1	1
	0 0 1	2	2
	0 1 0	4	4
	0 1 1	8	8
	1 0 0	R	R
	1 0 1	R	R
	1 1 0	R	R
	1 1 1	FP	R

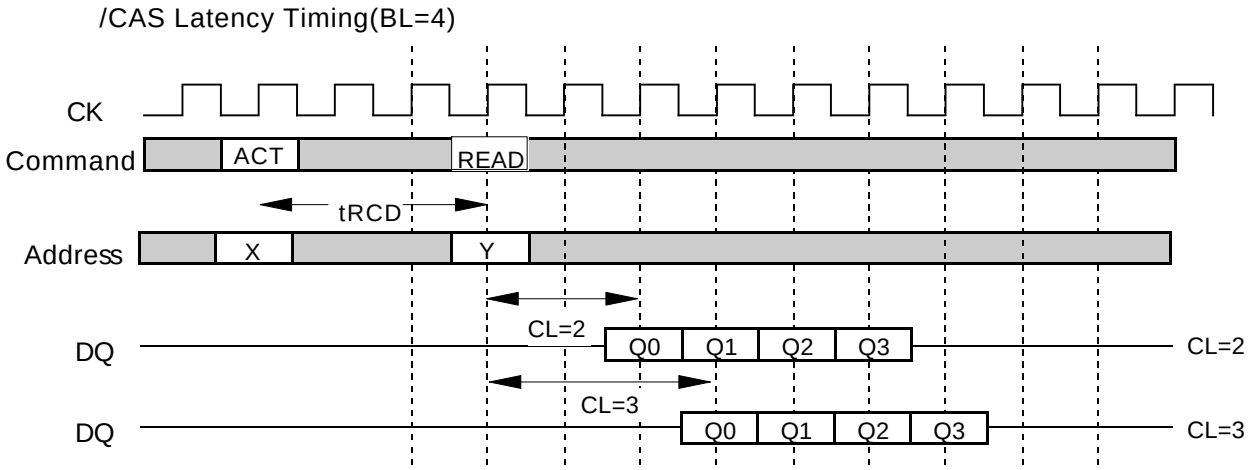
WRITE MODE	0	BURST
	1	SINGLE BIT

BURST TYPE	0	SEQUENTIAL
	1	INTERLEAVED

R:Reserved for Future Use
FP: Full Page

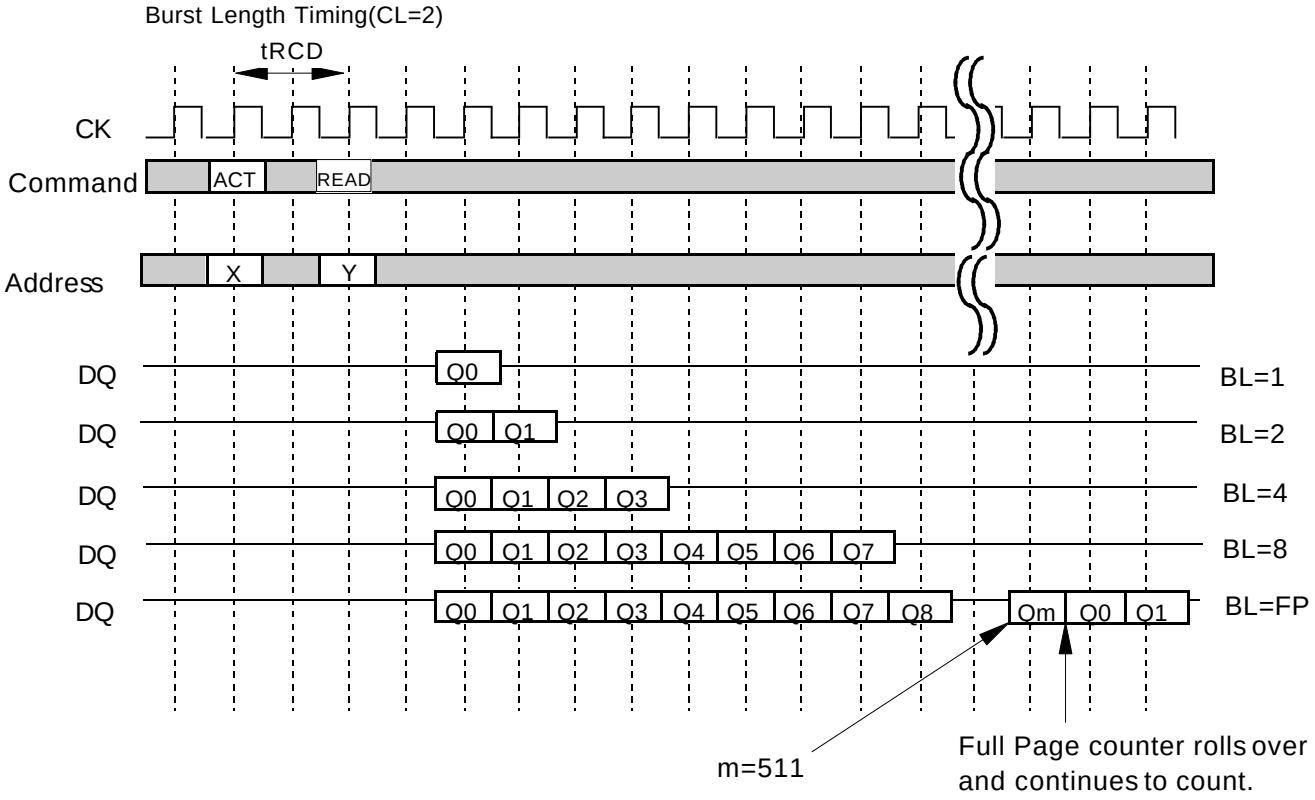
[/CAS LATENCY]

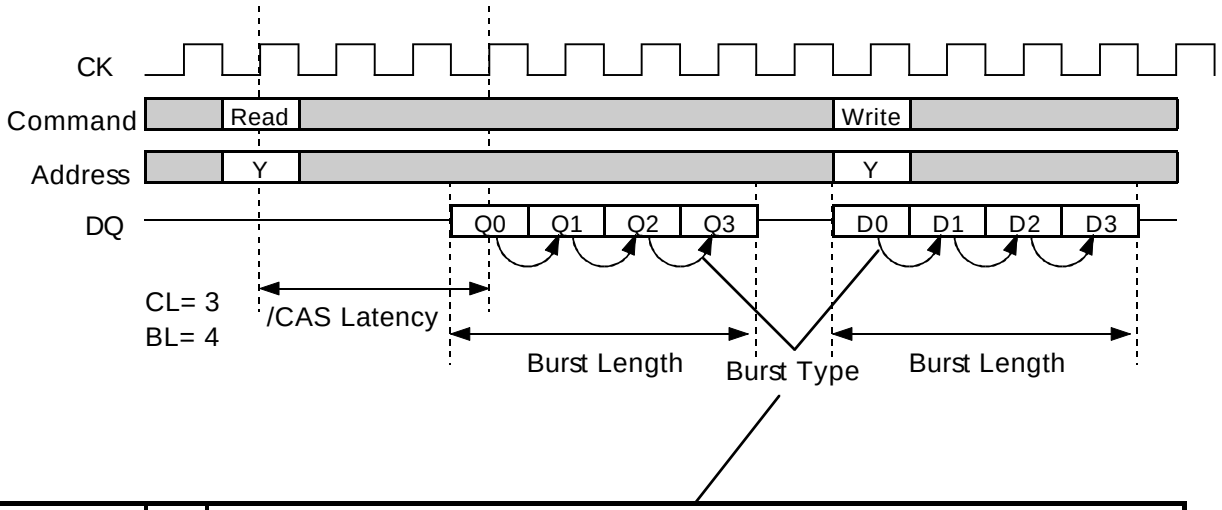
/CAS latency,CL,is used to synchronize the first output data with the CLK frequency,i.e.,the speed of CLK determines which CL should be used.First output data is available after CL cycles from READ command.



[BURST LENGTH]

The burst length,BL,determines the number of consecutive wrutes or reads that will be automatically performed after the initial write or read command.For BL=1,2,4,8,full page the output data is tristated(Hi-Z) after the last read.For BL=FP (Full Page),the TBST (Burst Terminate) command should be issued to stop the output of data.





Initial Address			BL	Column Addressing															
A2	A1	A0		Sequential								Interleaved							
0	0	0	8	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1		1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0		2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1		3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0		4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1		5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0		6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1		7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0
-	0	0	4	0	1	2	3					0	1	2	3				
-	0	1		1	2	3	0					1	0	3	2				
-	1	0		2	3	0	1					2	3	0	1				
-	1	1		3	0	1	2					3	2	1	0				
-	-	0	2	0	1							0	1						
-	-	1		1	0							1	0						

OPERATION DESCRIPTION

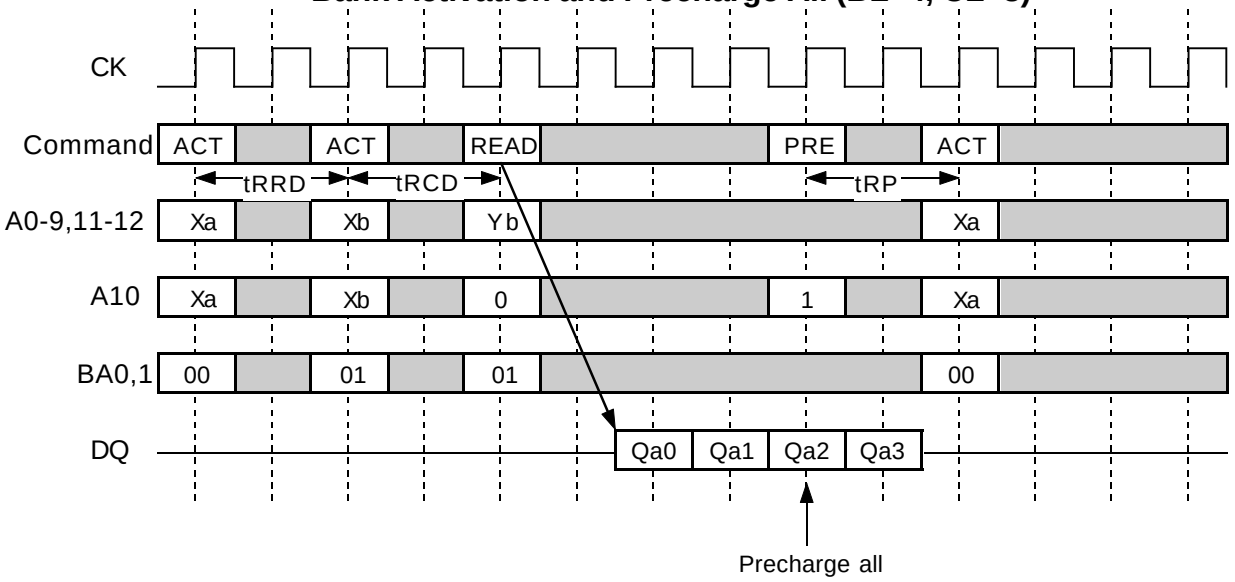
BANK ACTIVATE

One of four banks is activated by an ACT command.
An bank is selected by BA0-1. A row is selected by A0-12.
Multiple banks can be active state concurrently by issuing multiple ACT commands.
Minimum activation interval between one bank and another bank is tRRD.

PRECHARGE

An open bank is deactivated by a PRE command.
A bank to be deactivated is designated by BA0-1.
When multiple banks are active, a precharge all command (PREA, PRE + A10=H) deactivates all of open banks at the same time. BA0-1 are "Don't Care" in this case.
Minimum delay time of an ACT command after a PRE command to the same bank is tRP.

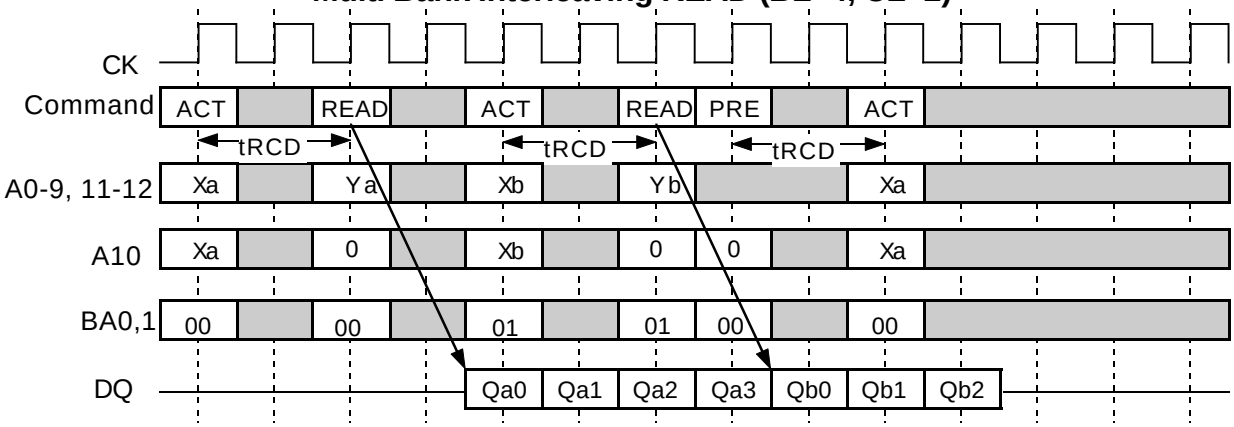
Bank Activation and Precharge All (BL=4, CL=3)



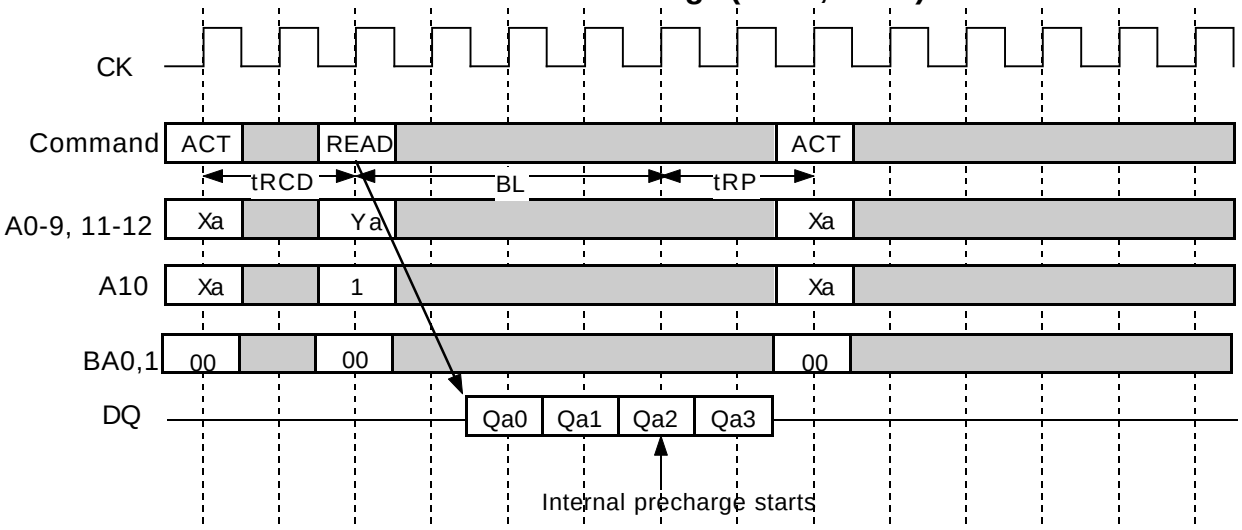
READ

A READ command can be issued to any active bank. The start address is specified by A0-8 (x16) . 1st output data is available after the /CAS Latency from the READ. The consecutive data length is defined by the Burst Length. The address sequence of the burst data is defined by the Burst Type. Minimum delay time of a READ command after an ACT command to the same bank is tRCD.
When A10 is high at a READ command, auto-precharge (READA) is performed. Any command (READ, WRITE, PRE, ACT, TBST) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at the BL after READA. The next ACT command can be issued after (BL + tRP) from the previous READA. In any case, tRCD+BL > tRASmin must be met.

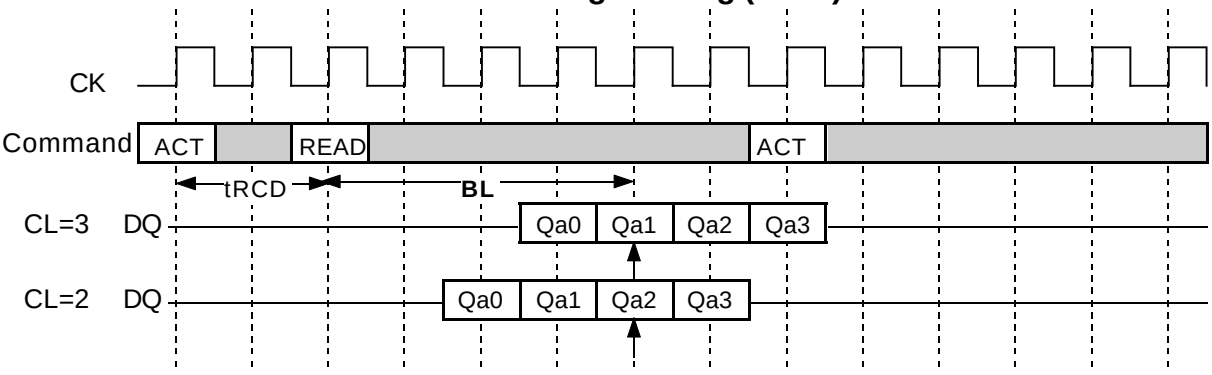
Multi Bank Interleaving READ (BL=4, CL=2)



READ with Auto-Precharge (BL=4, CL=2)



READ Auto-Precharge Timing (BL=4)

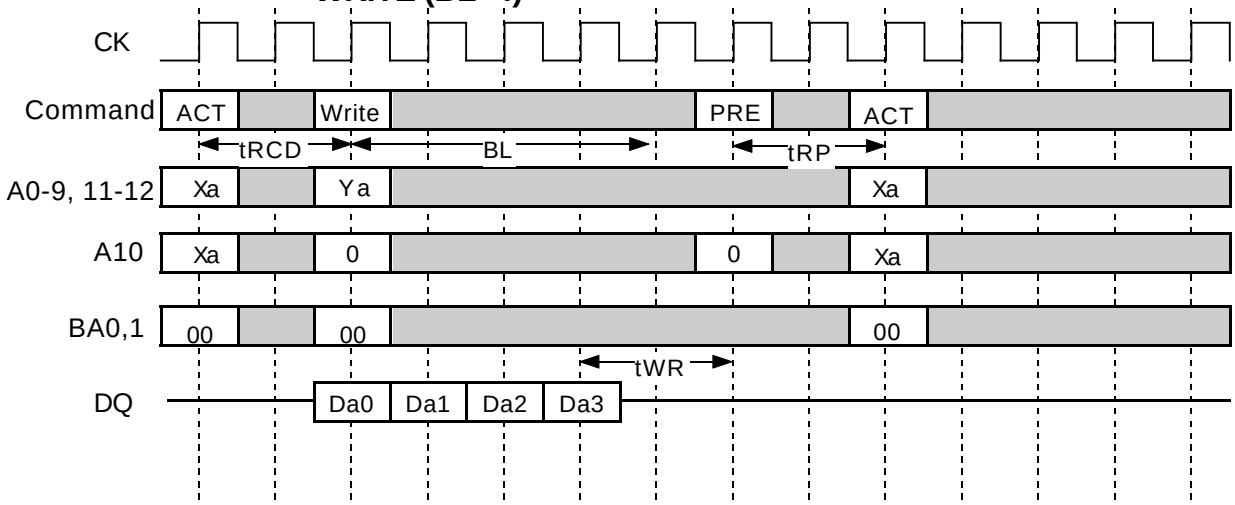


Internal Precharge Start Timing

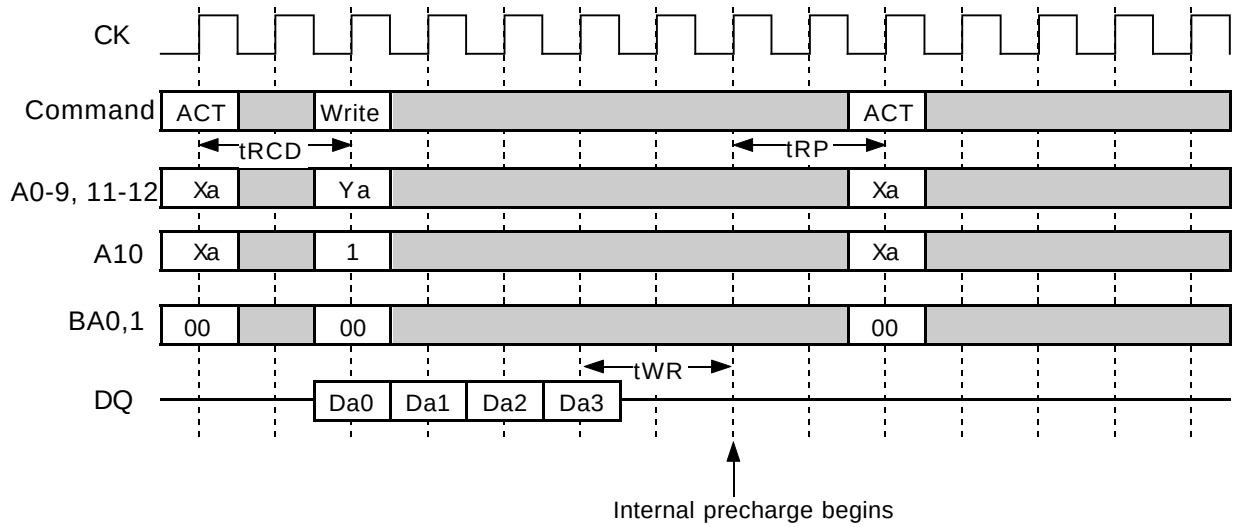
WRITE

A WRITE command can be issued to any active bank. The start address is specified by A0-8 (x16). 1st input data is set at the same cycle as the WRITE. The consecutive data length to be written is defined by the Burst Length. The address sequence of burst data is defined by the Burst Type. Minimum delay time of a WRITE command after an ACT command to the same bank is tRCD. From the last input data to the PRE command, the write recovery time (tWR) is required. When A10 is high at a WRITE command, auto-precharge (WRITEA) is performed. Any command (READ, WRITE, PRE, ACT, TBST) to the same bank is inhibited till the internal precharge is complete. The internal precharge starts at tWR after the last input data cycle. The next ACT command can be issued after (BL + tWR -1 + tRP) from the previous WRITEA. In any case, tRCD + BL + tWR -1 > tRASmin must be met.

WRITE (BL=4)



WRITE with Auto-Precharge (BL=4)

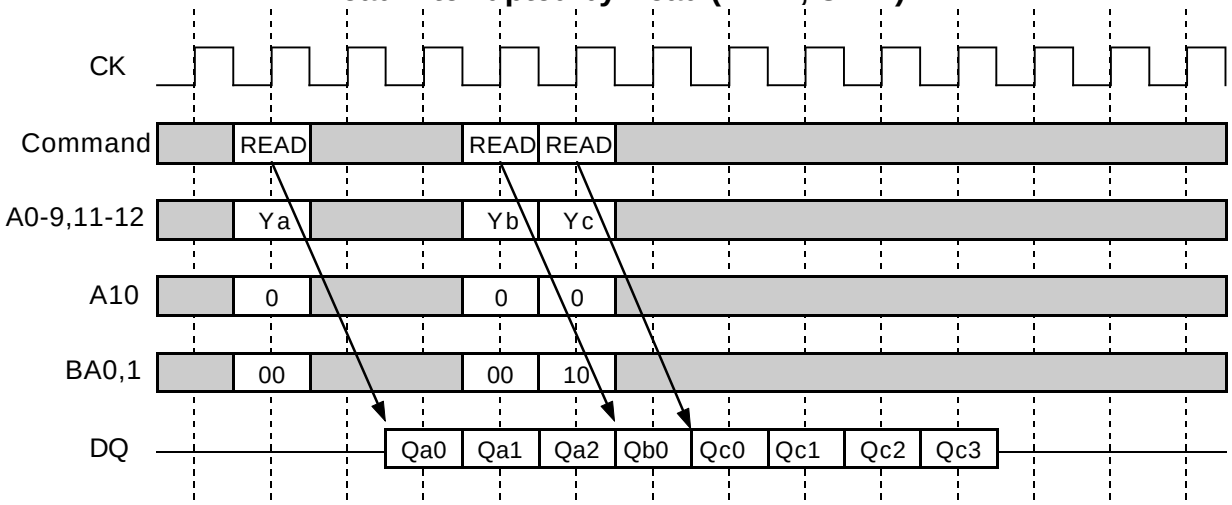


BURST INTERRUPTION

[Read Interrupted by Read]

Burst read option can be interrupted by new read of the same or the other bank. Random column access is allowed READ to READ interval is minimum 1 CK

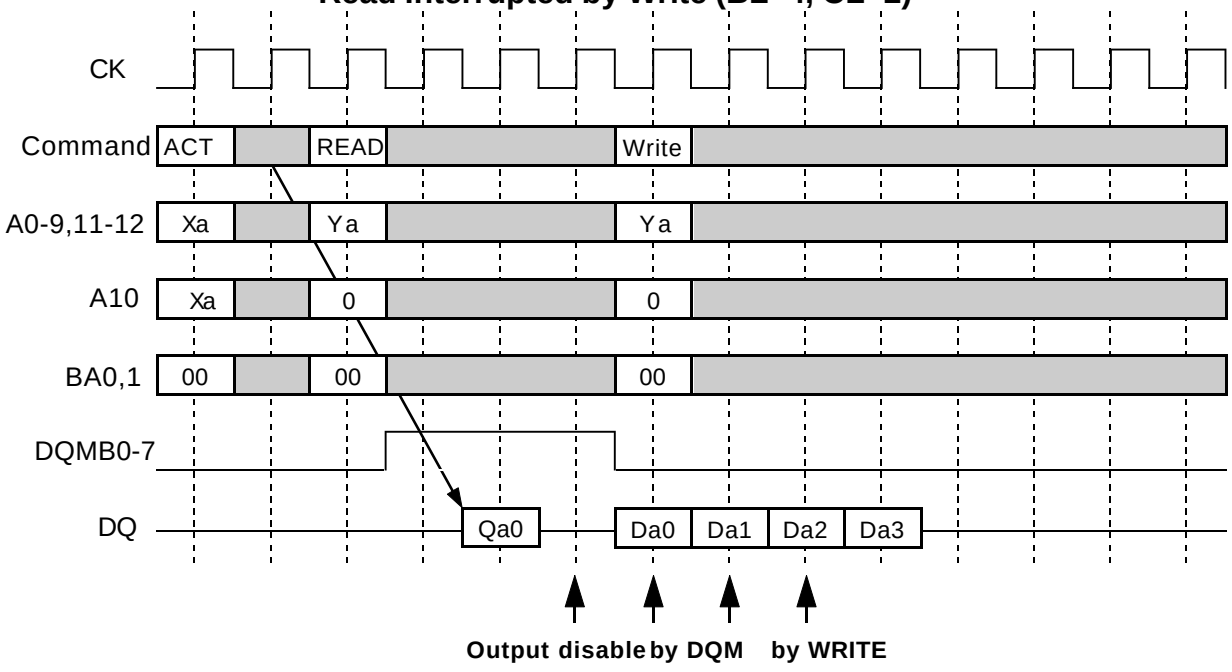
Read Interrupted by Read (BL=4, CL=2)



[Read Interrupted by Write]

Burst read operation can be interrupted by write of the same or the other bank. Random column access is allowed. In this case, the DQ should be controlled adequately by using the DQMB0-7 to prevent the bus contention. The output is disabled automatically 2 cycle after WRITE assertion.

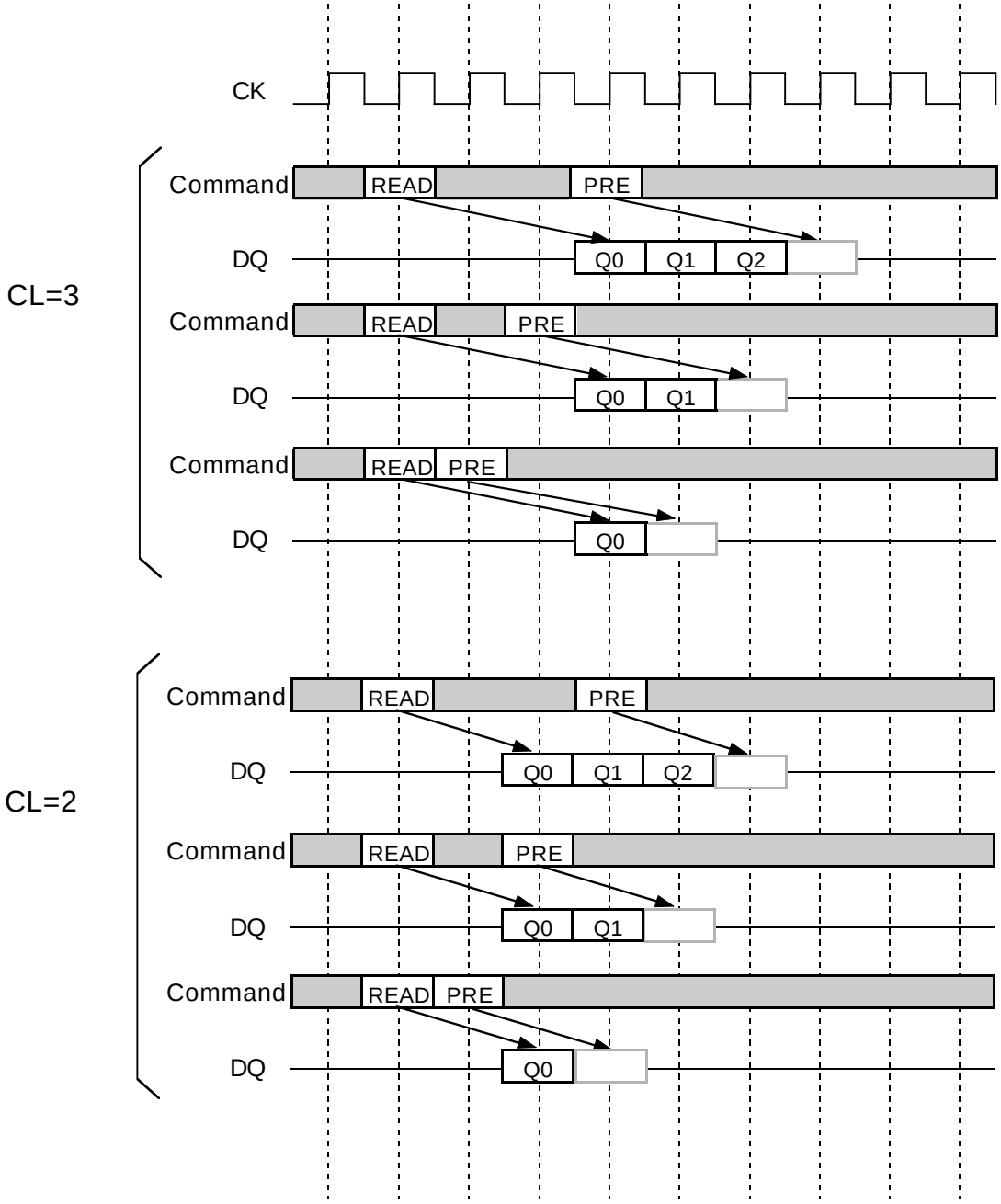
Read Interrupted by Write (BL=4, CL=2)



[Read Interrupted by Precharge]

Burst read operation can be interrupted by precharge of the same or the other bank. Read to PRE interval is minimum 1 CK. A PRE command output disable latency is equivalent to the /CAS Latency.As a result, READ to PRE interval determines valid data length to be output.The figure below shows examples of BL=4.

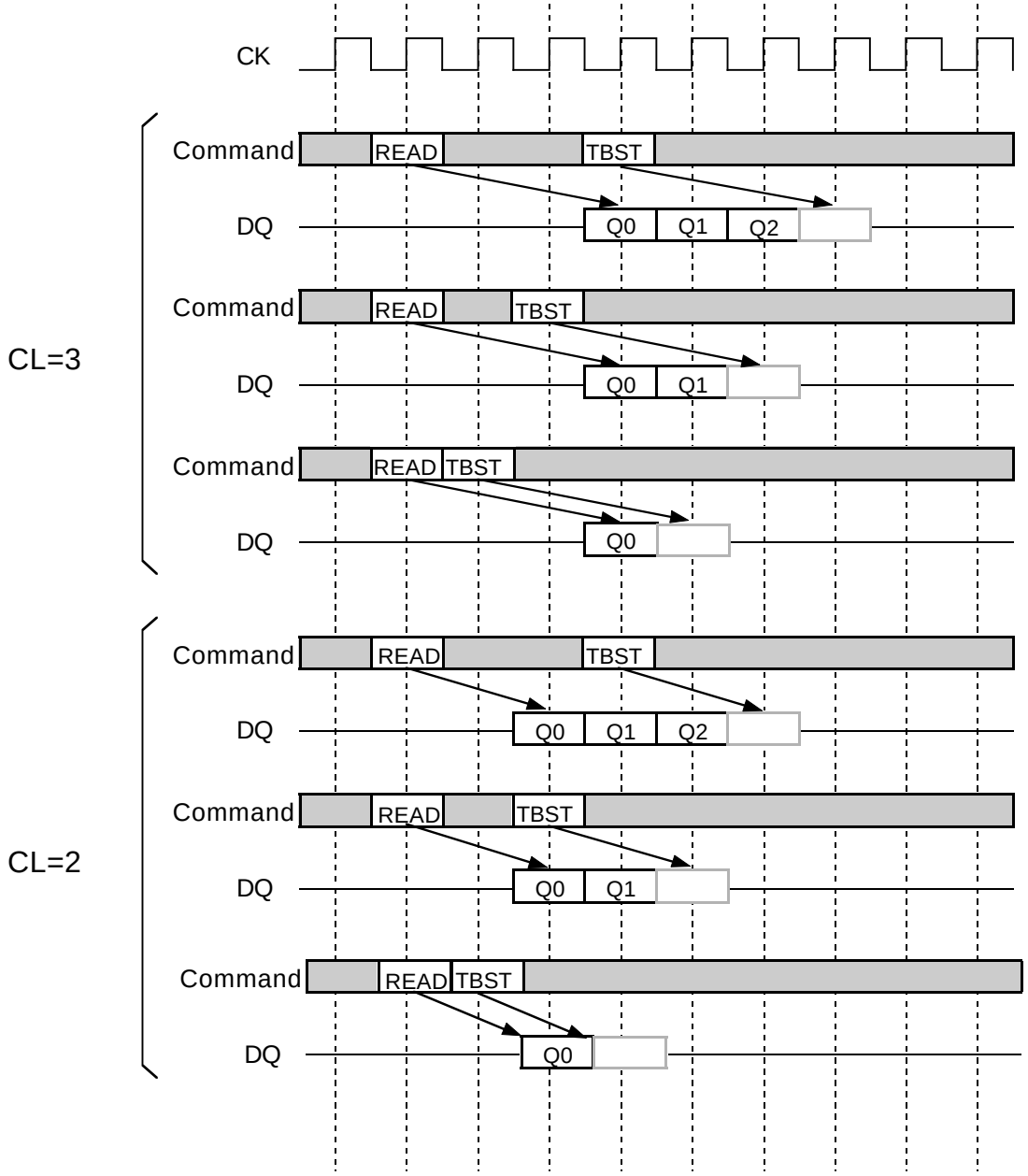
Read Interrupted by Precharge (BL=4)



[Read Interrupted by Burst Terminate]

Similarly to the precharge, burst terminate command,TBST, can interrupt burst read operation and disable the data output. READ to TBST interval is minimum of 1 CK. TBST is mainly used to interrupt FP bursts.The figure below show examples, of how the output data is terminated with TBST.

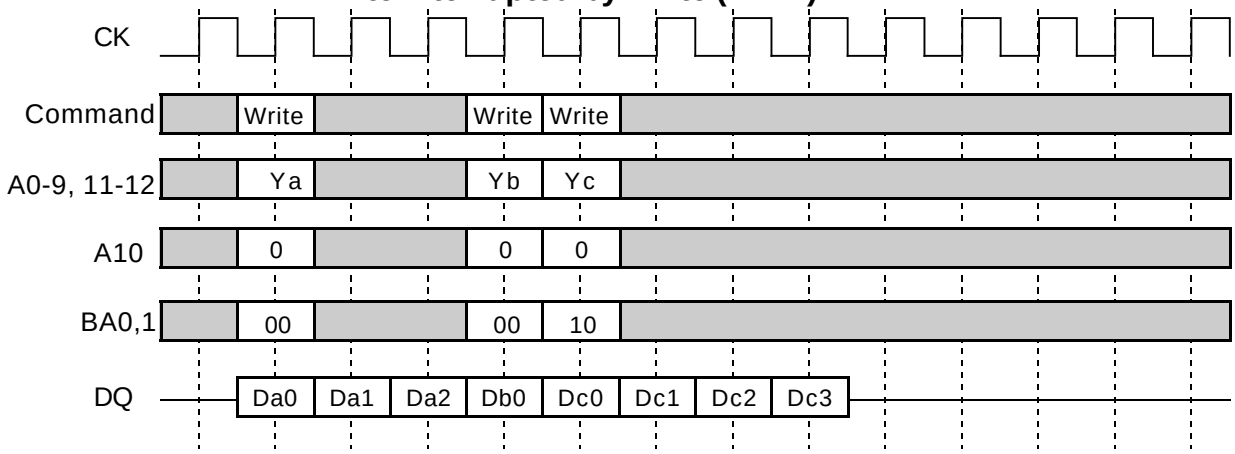
Read Interrupted by Terminate (BL=4)



[Write Interrupted by Write]

Burst write operation can be interrupted by new write of the same or the other bank. Random column access is allowed. WRITE to WRITE interval is minimum 1 CK.

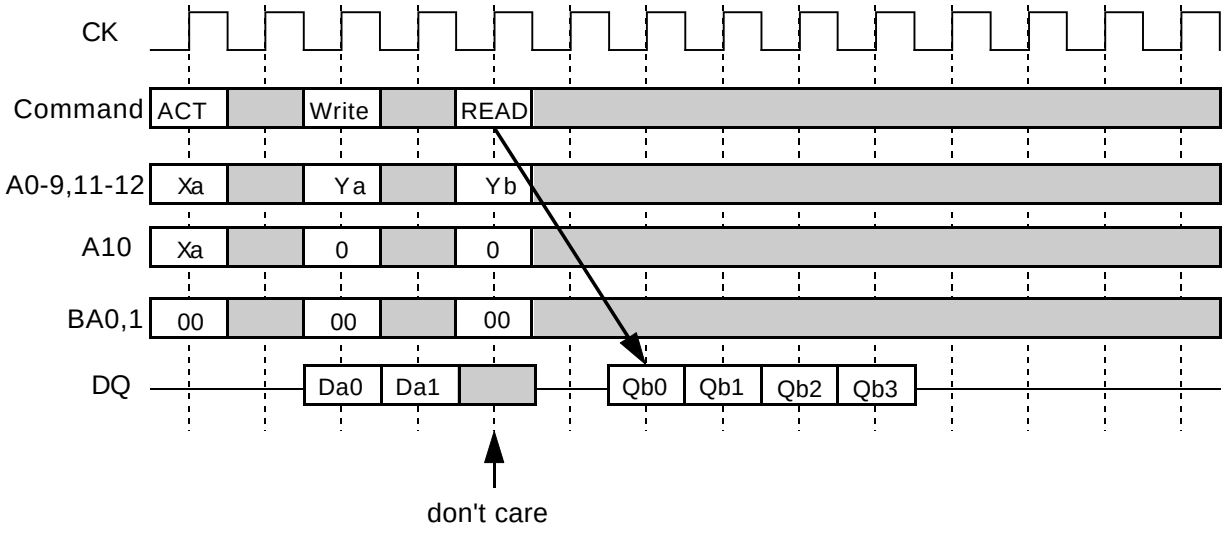
Write Interrupted by Write (BL=4)



[Write Interrupted by Read]

Burst write operation can be interrupted by read of the same or the other bank. Random column access is allowed. WRITE to READ interval is minimum 1 CK. The input data on DQ at the interrupting READ cycle is "don't care".

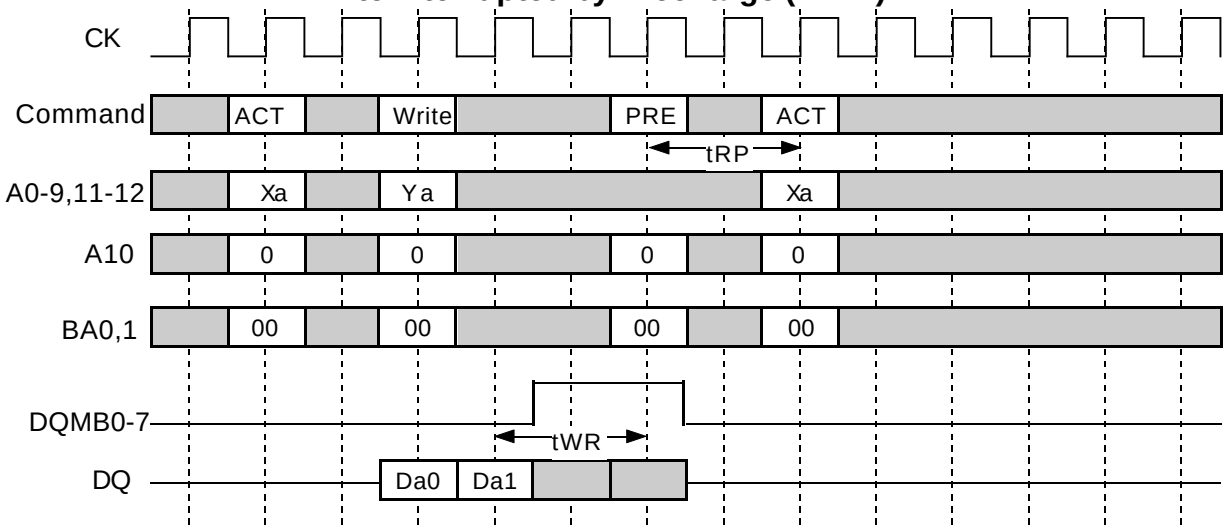
Write Interrupted by Read (BL=4, CL=2)



[Write Interrupted by Precharge]

Burst write operation can be interrupted by precharge of the same bank. Random column access is allowed. Because the write recovery time(tWR) is required from the last data to PRE command.

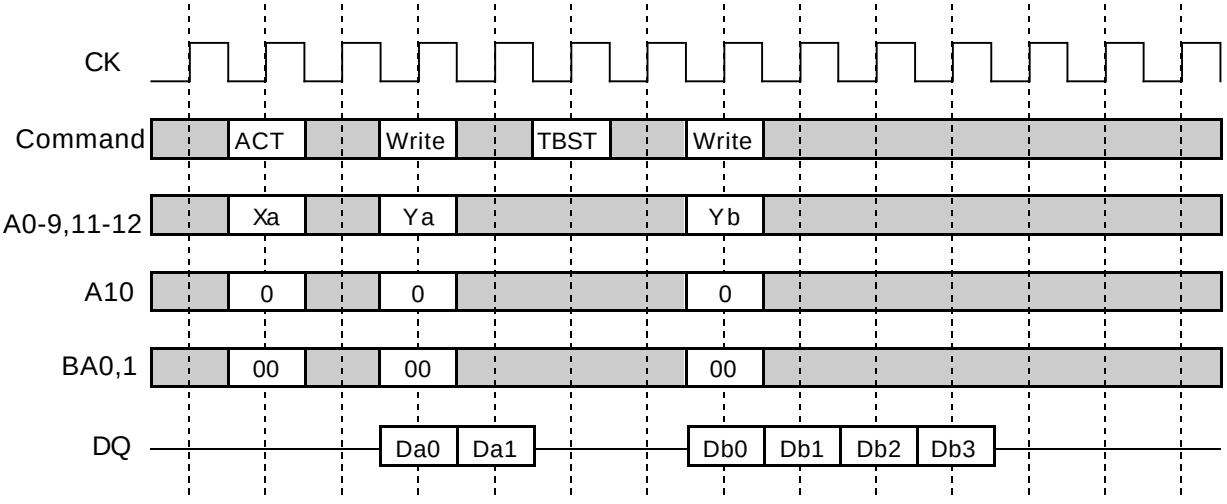
Write Interrupted by Precharge (BL=4)



[Write Interrupted by Burst Terminate]

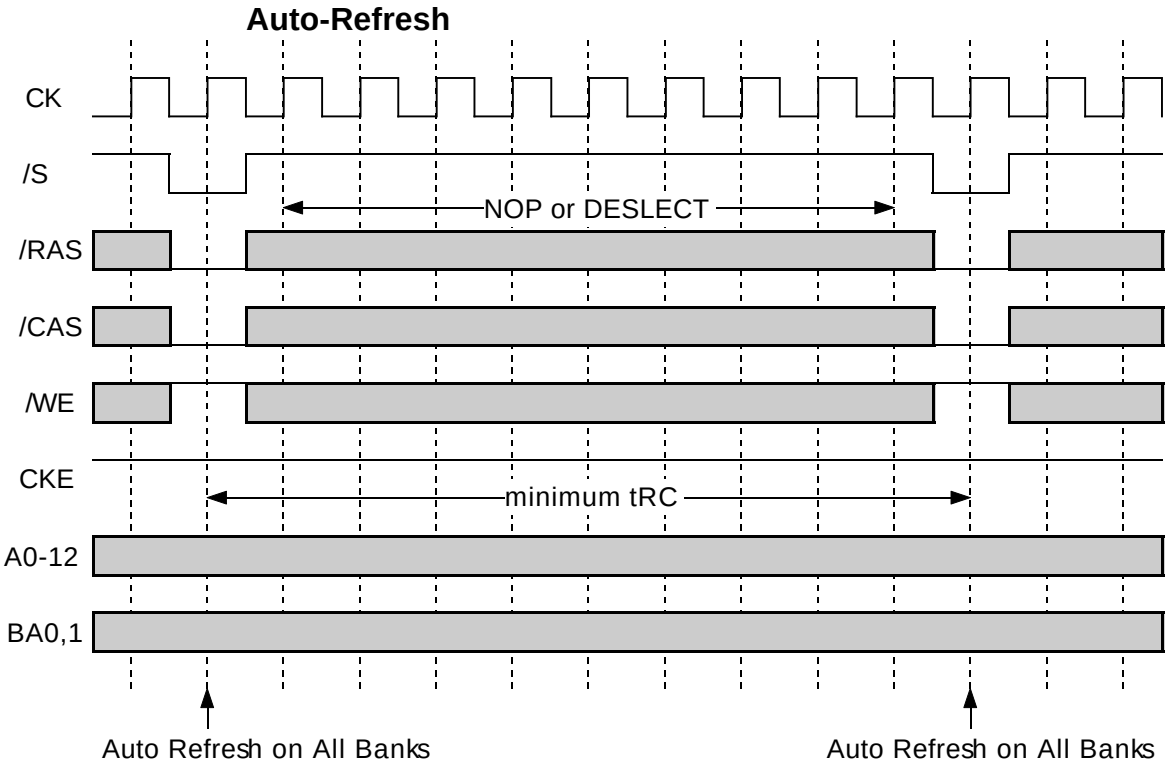
A burst terminate command TBST can terminate burst write operation. In this case, the write recovery time is not required and the bank remains active (Please see the waveforms below).The WRITE to TBST minimum interval is 1CK.

Write Interrupted by Burst Terminate (BL=4)



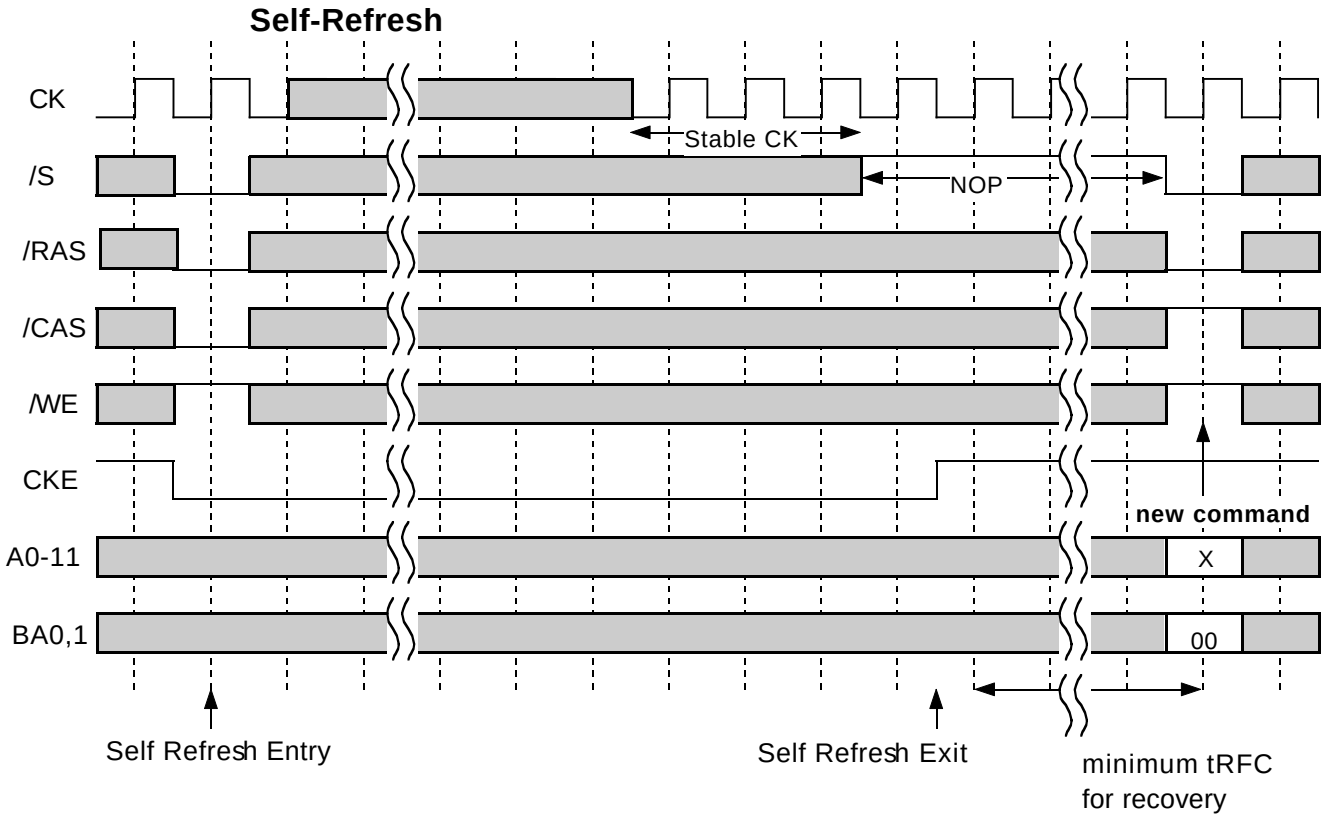
AUTO REFRESH

Single cycle of auto-refresh is initiated with a REFA(/CS=/RAS=/CAS=L, /WE=/CKE=H) command. The refresh address is generated internally. 4096 REFA cycle within 64ms refresh 128Mbit memory cells. The auto-refresh is performed on 4bank alternately(ping-pong refresh). Before performing an auto-refresh, both banks must be in the idle state. Additional commands must not be supplied to the device before tRC from the REFA command.



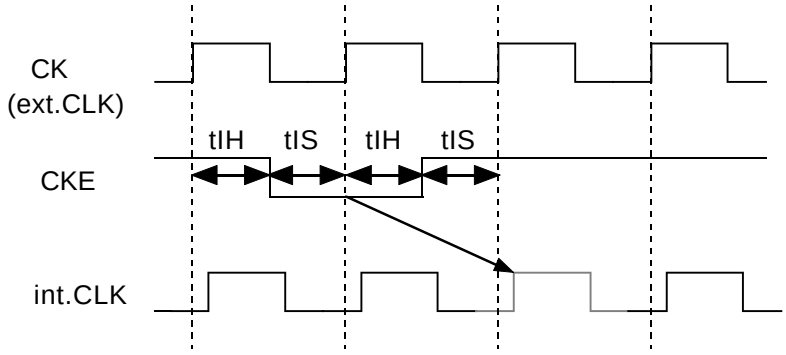
SELF REFRESH

Self-refresh mode is entered by issuing a REFS command (/CS=/RAS=/CAS=L, /WE=H, CKE=L). Once the self-refresh is initiated, it is maintained as log as CKE is kept low.During the self-refresh mode, CKE is asynchronous and the only enabled input , all other inputs including CK are disabled and ignored, so that power consumption due to synchronous inputs is saved. To exit the self-refresh, supplying stable CK inputs, asserting DESEL or NOP command and then asserting CKE(REFSX) for longer than tSRX. After tRC from REFSX all banks are in the idle state and a new command can be issued after tRC, but DESEL or NOP commands must be asserted till then.

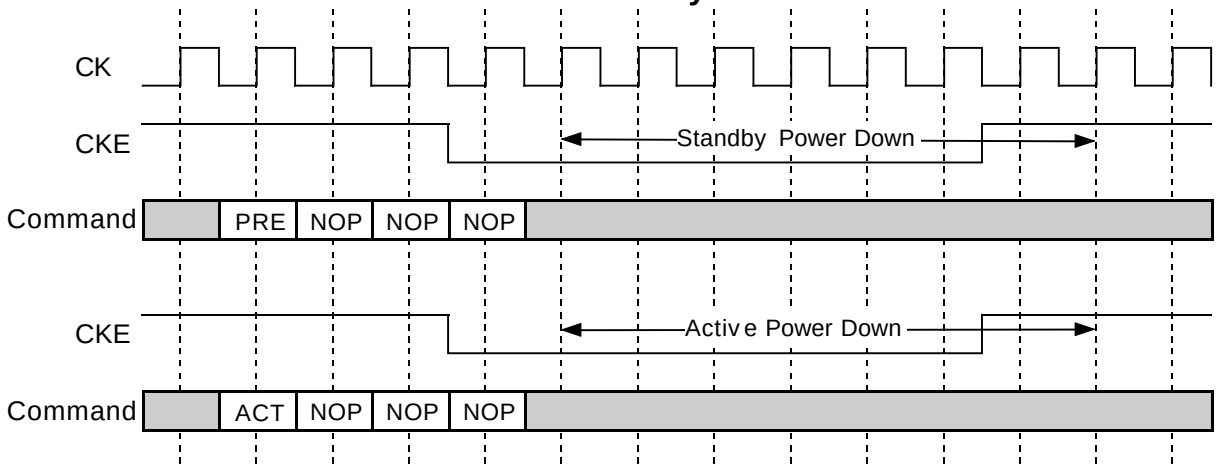


CLK SUSPEND and POWER DOWN

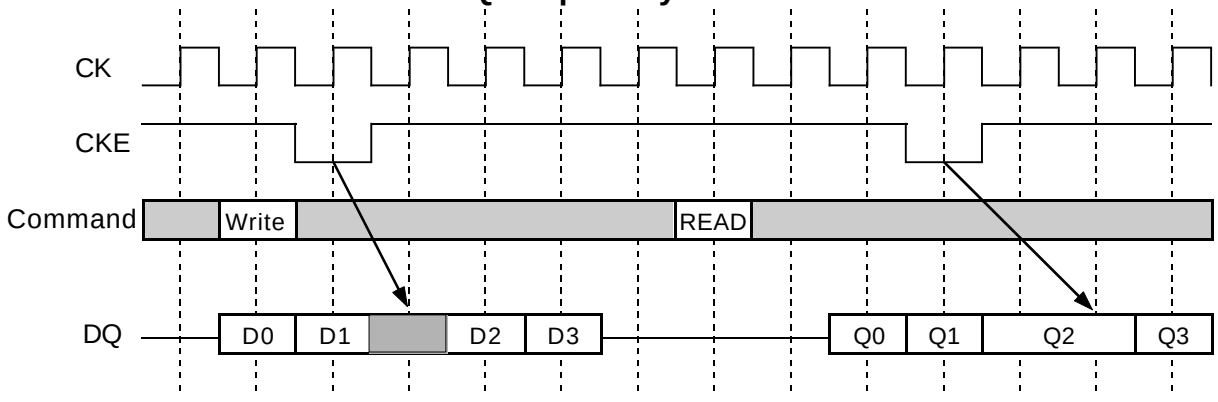
CKE controls the internal CLK at the following cycle. Figure below shows how CKE works. By negating CKE, the next internal CLK is suspended. The purpose of CLK suspend is power down, output suspend or input suspend. CKE is a synchronous input except during the self-refresh mode. CLK suspend can be performed either when the banks are active or idle, but a command at the following cycle is ignored.



Power Down by CKE



DQ Suspend by CKE

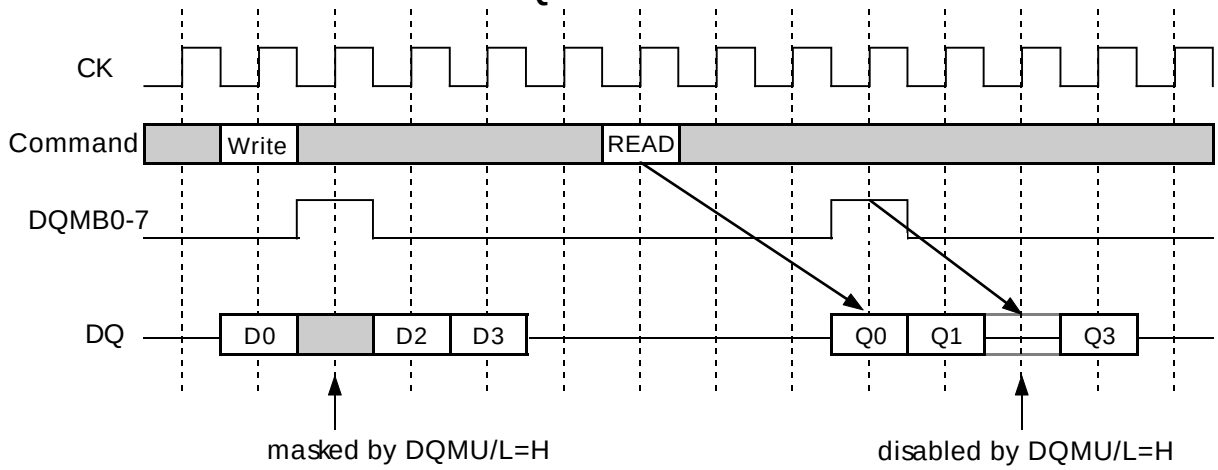


DQM CONTROL

DQMB0-7 is a dual function signal defined as the data mask for writes and the output disable for reads. During writes, DQMB0-7 masks input data word by word. DQMB0-7 to write mask latency is 0.

During reads, DQMB0-7 forces output to Hi-Z word by word. DQMB0-7 to output Hi-Z latency is 2.

DQM Function



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition	Ratings	Unit
Vdd	Supply Voltage	with respect to Vss	-0.5 ~ 4.6	V
VI	Input Voltage	with respect to Vss	-0.5 ~ Vdd+0.5	V
VO	Output Voltage	with respect to Vss	-0.5 ~ VddQ+0.5	V
IO	Output Current		50	mA
Pd	Power Dissipation	Ta=25°C	8	W
Topr	Operating Temperature		0 ~ 70	°C
Tstg	Storage Temperature		-40 ~ 100	°C

RECOMMENDED OPERATING CONDITION

(Ta=0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
Vdd	Supply Voltage	3.0	3.3	3.6	V
Vss	Supply Voltage	0	0	0	V
VIH	High-Level Input Voltage all inputs	2.0		Vdd+0.3	V
VIL	Low-Level Input Voltage all inputs	-0.3		0.8	V

Note:* VIH (max) = 5.5V for pulse width less than 10ns.
VIL (min) = -1.0V for pulse width less than 10ns.

CAPACITANCE

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits(max.)	Unit
CI(A)	Input Capacitance, address pin	VI = Vss f=1MHz Vi=25mVrms	58	pF
CI(C)	Input Capacitance, control pin		50	pF
CI(K)	Input Capacitance, CK pin		40	pF
CI/O	Input Capacitance, I/O pin		22	pF

AVERAGE SUPPLY CURRENT from Vdd

(Ta=0 ~70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, Output Open, unless otherwise noted)

Parameter	Symbol	Test Condition		Limits (max)		Unit	Note
				-6,-6L	-7,-7L		
Operating current one bank active (discrete)	Icc1	tRC=min.tCLK=min, BL=1, CL=3		500	440	mA	*1
Idle Standby Current in Normal Mode	Icc2N	tCLK=min, CKE>VIHmin		200	160	mA	*2,3
	Icc2NS	tCLK=L, CKE>VIHmin		48	48	mA	*2,4
Idle Standby Current in Power Down Mode	Icc2P	tCLK=min, CKE<VILmax		12	8	mA	*2
	Icc2PS	CLK= L, CKE<VILmax		8	8	mA	
Active Standby Current in Normal Mode	Icc3N	tCLK=min, CKE>VIHmin		240	200	mA	*3,5
	Icc3NS	CLK=L, CKE=>VIHmin		120	120	mA	*4,5
Burst Operating Current	Icc4	tCLK=min, BL=4, gapless data		580	480	mA	*5
Auto-Refresh Current	Icc5	tRFC=min, tCLK=min		1440	1360	mA	
Self-Refresh Current	Icc6	CKE <VILmax	6,7	24	24	mA	
			6L,7L	16	16	mA	

Notes
1. addresses are charged 3 times during tRC, only 1 bank is active & all other banks are idle
2. all banks are idle
3. input signals are charged one time during 3xtCLK
4. input signals are stable
5. all banks are active

AC OPERATING CONDITIONS AND CHARACTERISTICS

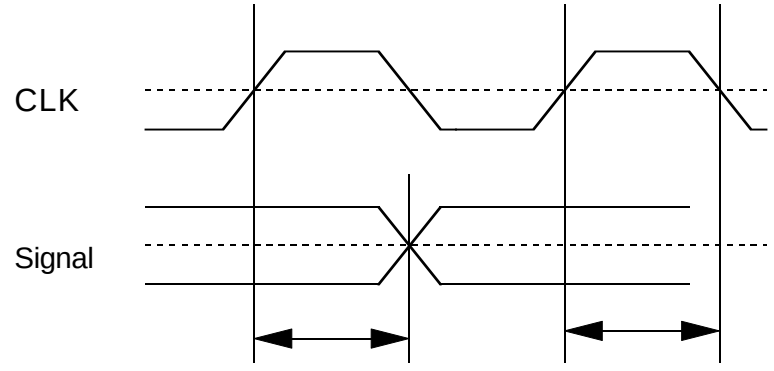
(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test Condition	Limits		Unit
			Min.	Max.	
VOH(DC)	High-Level Output Voltage(DC)	IOH=-2mA	2.4		V
VOL(DC)	Low-Level Output Voltage(DC)	IOL=2mA		0.4	V
IOZ	Off-stare Output Current	Q floating VO=0 ~ Vdd	-20	20	uA
Ii	Input Current	VIH=0 ~ Vdd+0.3V	-80	80	uA

AC TIMING REQUIREMENTS (SDRAM Component)

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)
Input Pulse Levels: 0.8V to 2.0V
Input Timing Measurement Level: 1.4V

Symbol	Parameter		Limits				Unit
			-6,-6L		-7,-7L		
			Min.	Max.	Min.	Max.	
tCLK	CK cycle time	CL=2	10		10		ns
		CL=3	7.5		10		ns
tCH	CK High pulse width		2.5		3		ns
tCL	CK Low pilse width		2.5		3		ns
tT	Transition time of CK		1	10	1	10	ns
tIS	Input Setup time(all inputs)		1.5		2		ns
tIH	Input Hold time(all inputs)		0.8		1		ns
tRC	Row cycle time		67.5		70		ns
tRFC	Refresh Cycle time		75		80		ns
tRCD	Row to Column Delay		20		20		ns
tRAS	Row Active time		45	120K	50	120K	ns
tRP	Row Precharge time		20		20		ns
tWR	Write Recovery time		15		20		ns
tRRD	Act to Act Deley time		15		20		ns
tRSC	Mode Register Set Cycle time		15		20		ns
tREF	Refresh Interval time			7.8		7.8	us



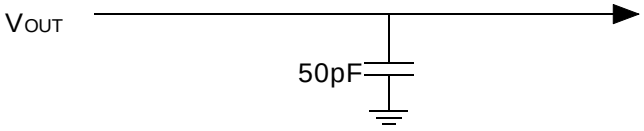
Any AC timing is referenced to the input signal crossing through 1.4V.

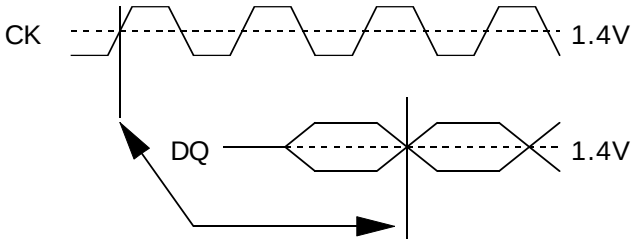
SWITCHING CHARACTERISTICS (SDRAM Component)

(Ta=0 ~ 70°C, Vdd = 3.3 ± 0.3V, Vss = 0V, unless otherwise noted)

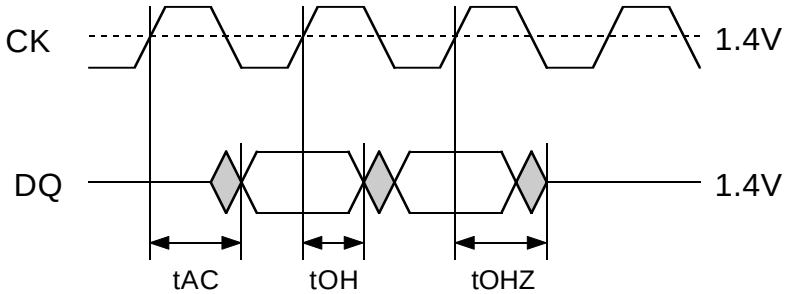
Symbol	Parameter		Limits				Unit
			-6,-6L		-7,-7L		
			Min.	Max.	Min.	Max.	
tAC	Access time from CK	CL=2		6		6	ns
		CL=3		5.4		6	ns
tOH	Output Hold time from CK		3		3		ns
tOLZ	Delay time, output low impedance from CK		0		0		ns
tOHZ	Delay time, output high impedance from CK		3	6	3	6	ns

Output Load Condition

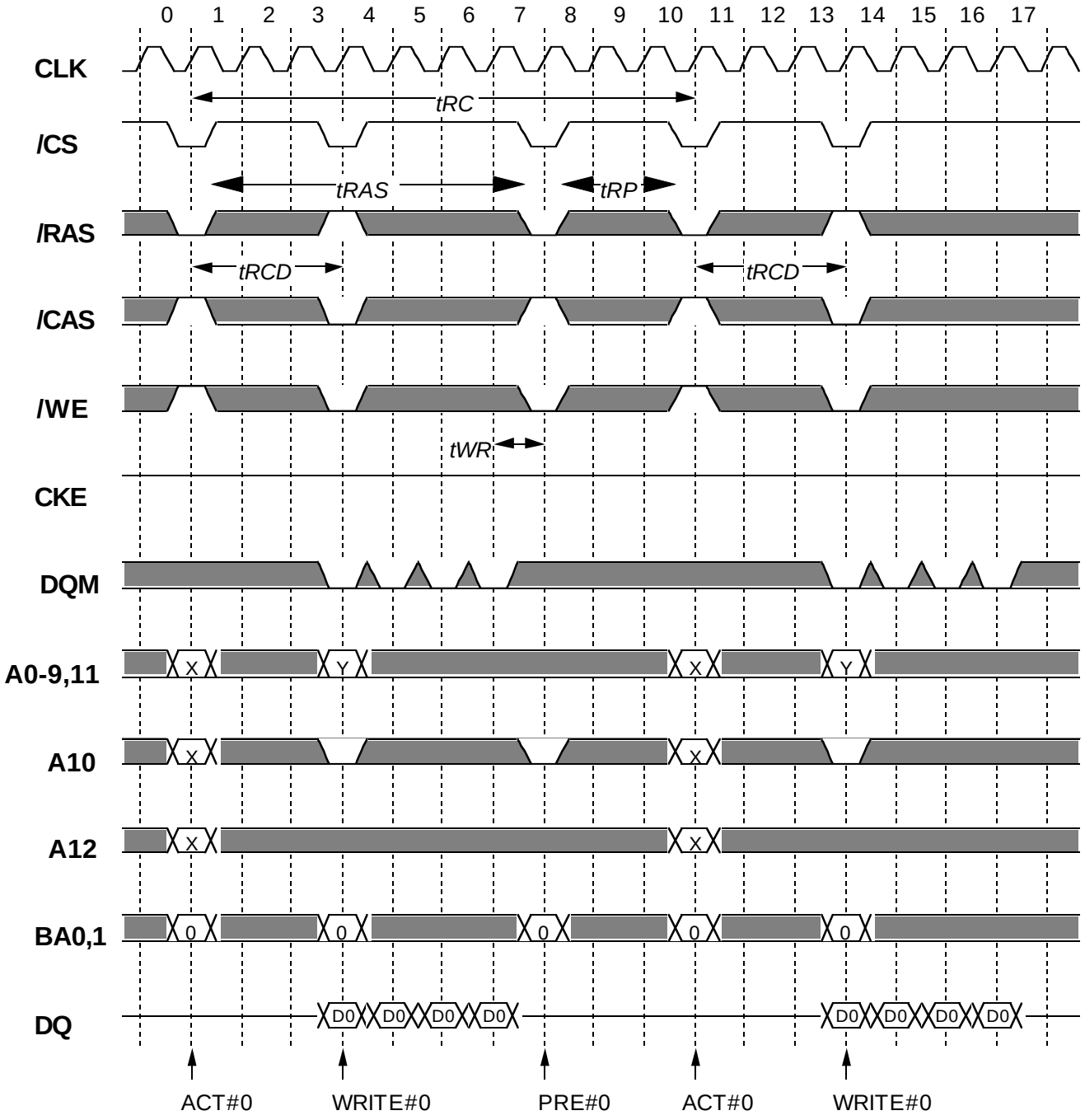




Output Timing Measurement Reference Point

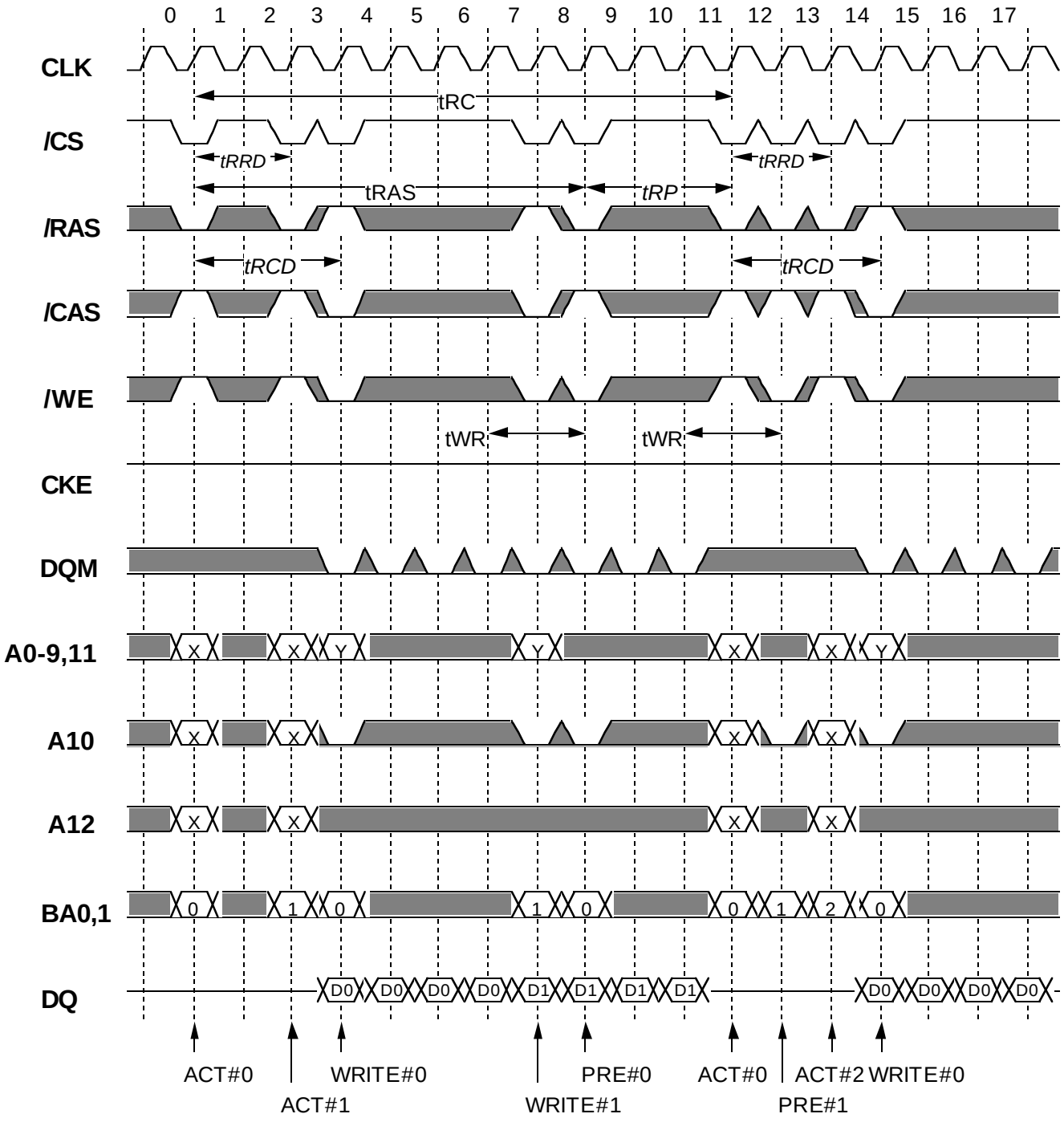


Burst Write (single bank) @BL=4



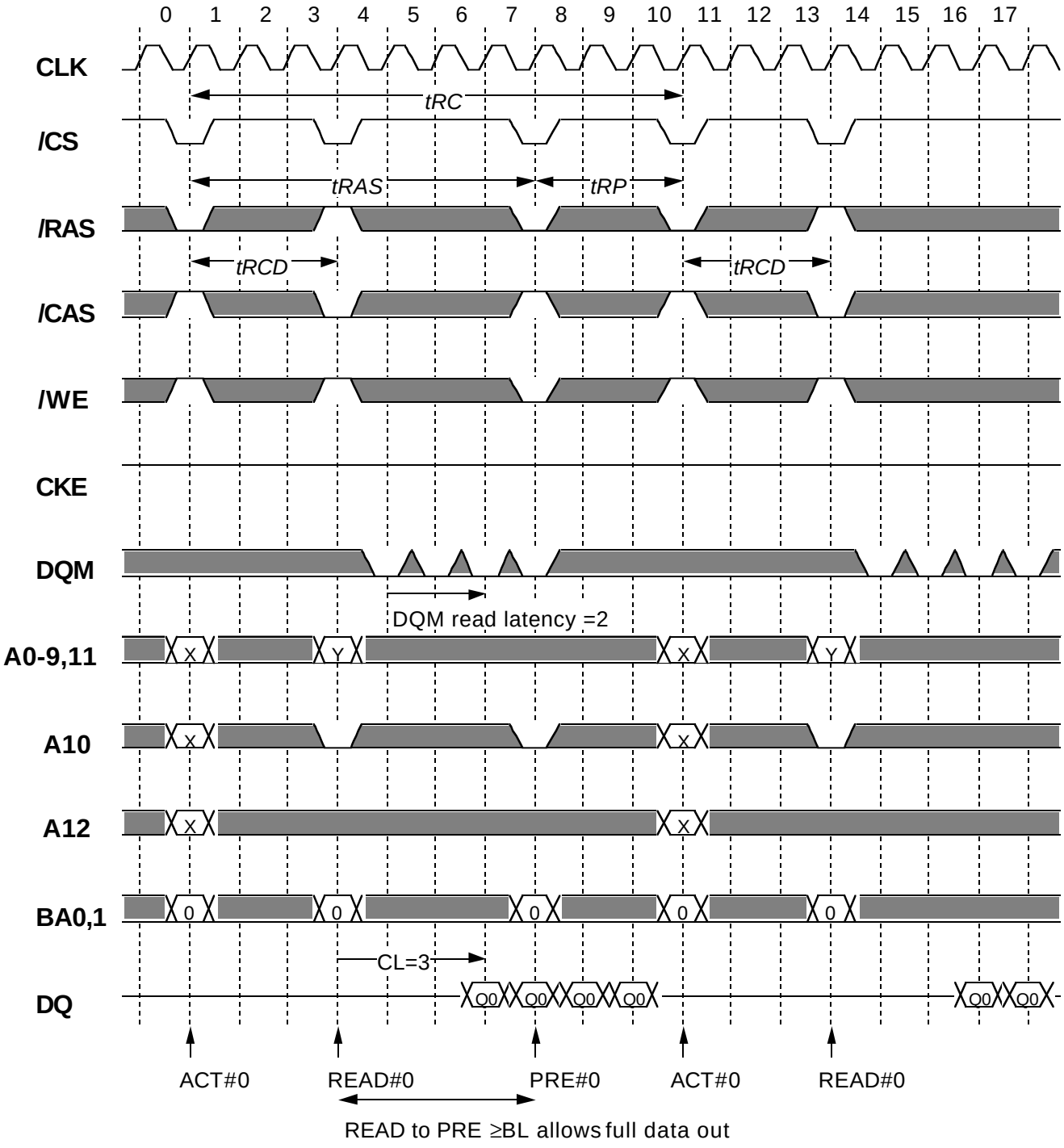
Italic parameter indicates minimum case

Burst Write (multi bank) @BL=4



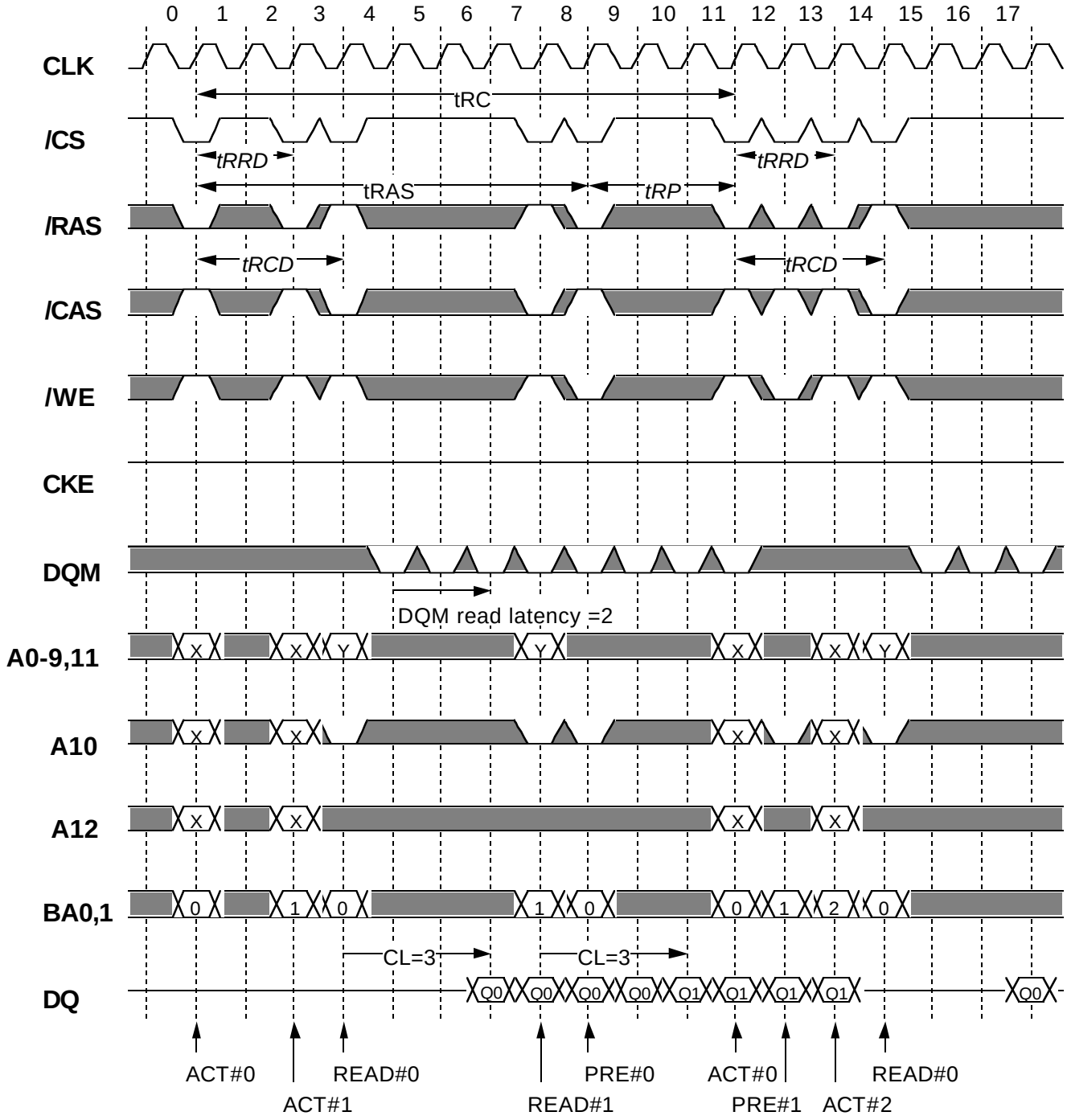
Italic parameter indicates minimum case

Burst Read (single bank) @BL=4 CL=3



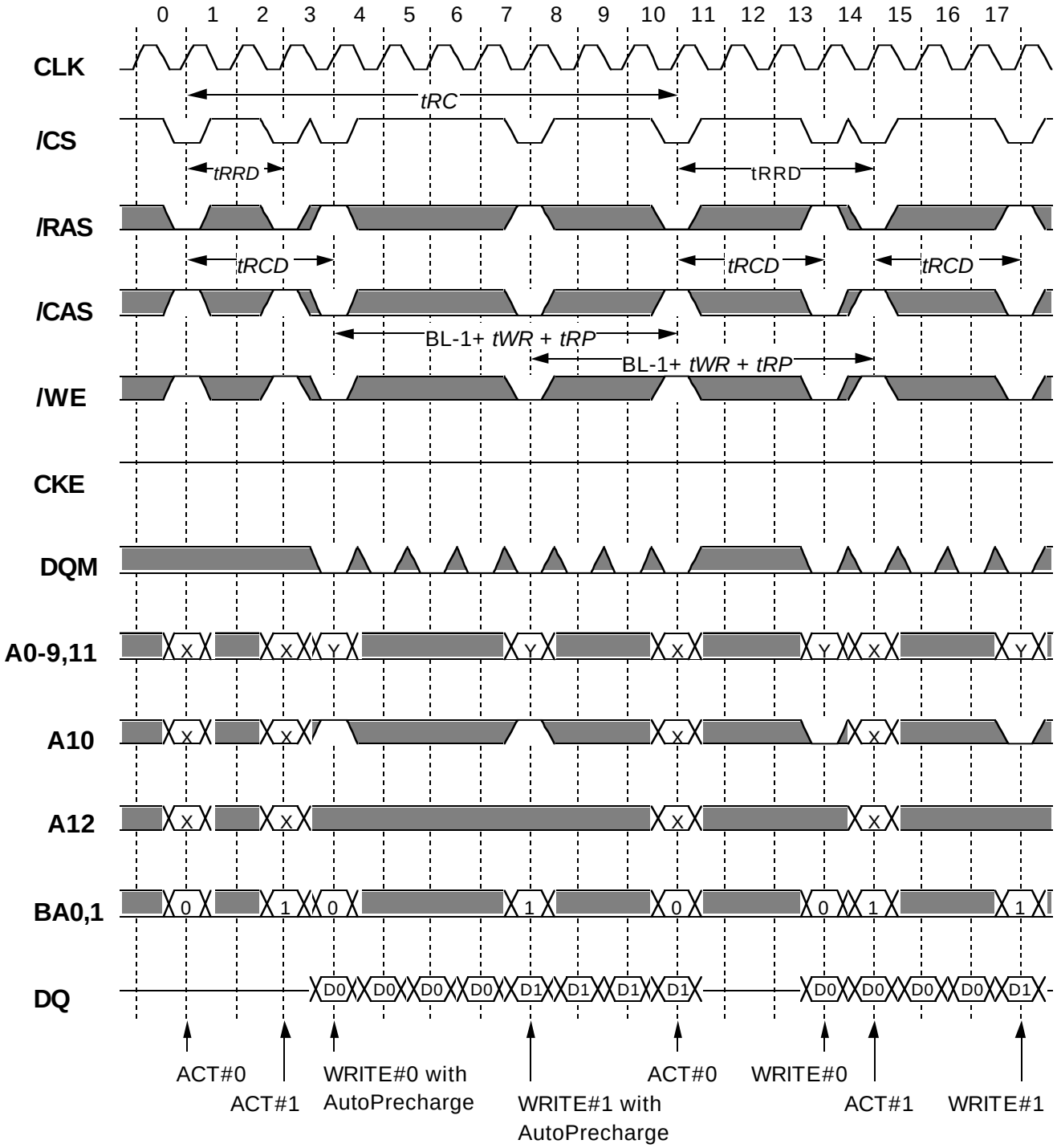
Italic parameter indicates minimum case

Burst Read (multiple bank) @BL=4 CL=3



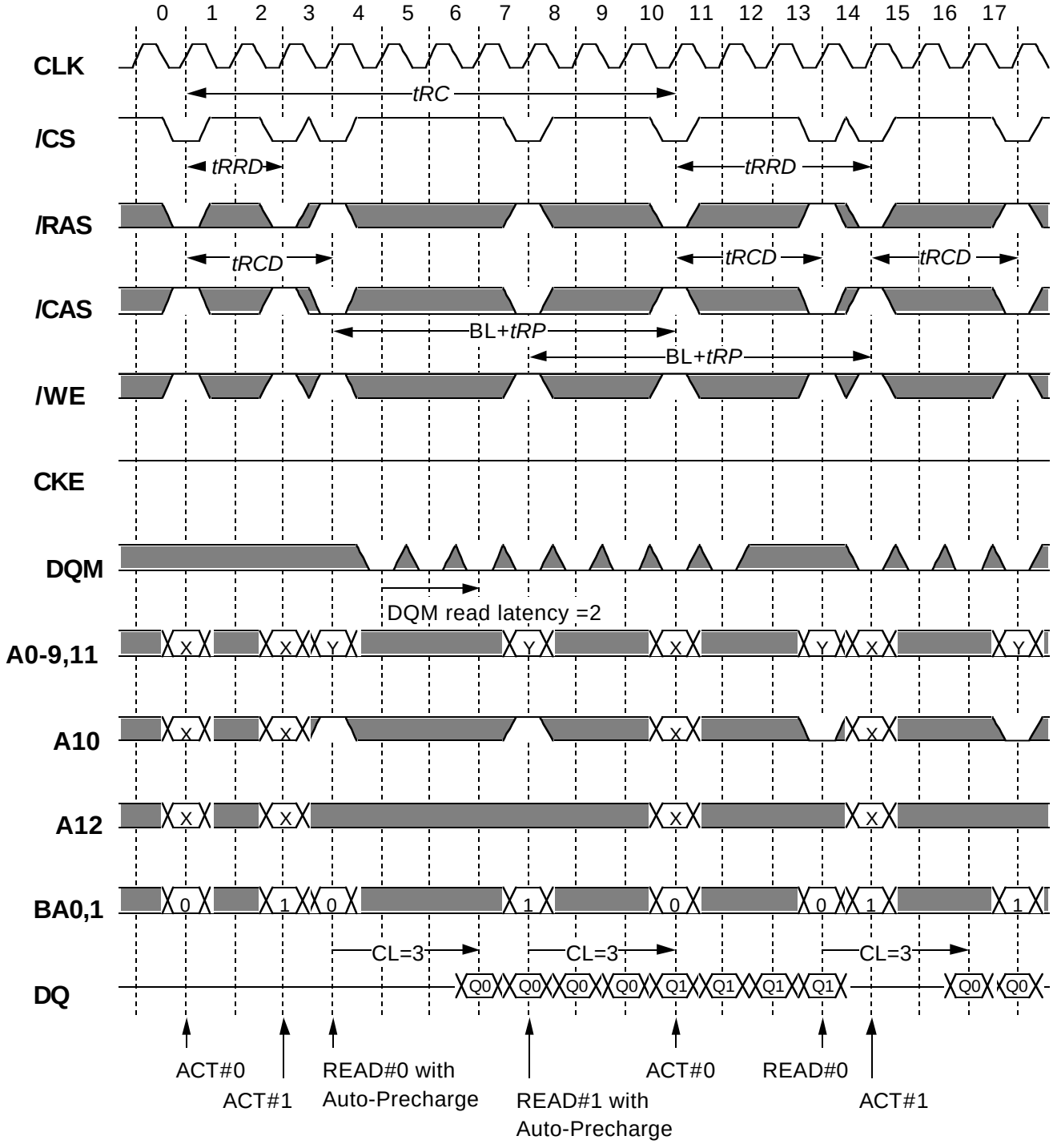
Italic parameter indicates minimum case

Burst Write (multi bank) with Auto-Precharge @BL=4



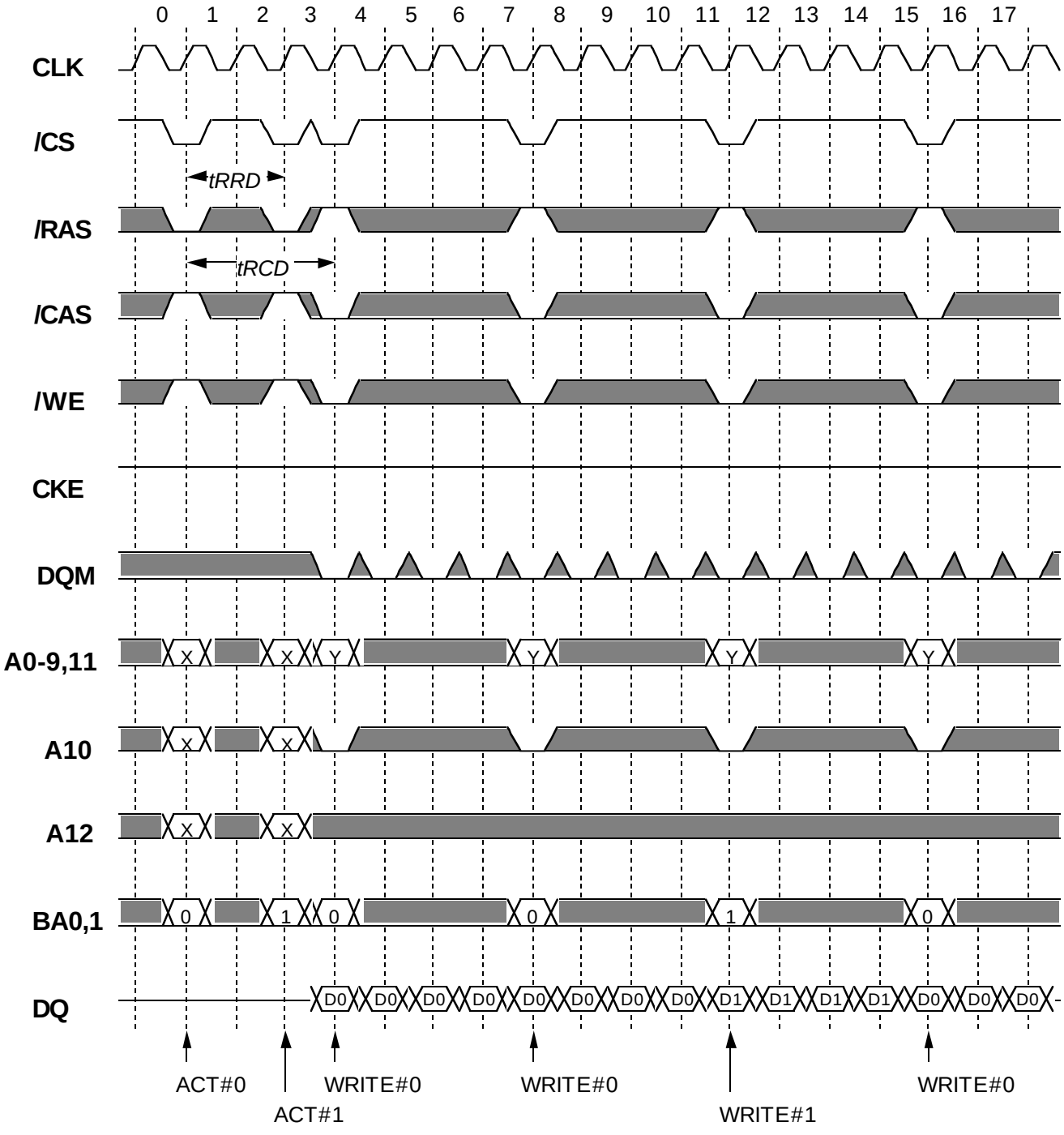
Italic parameter indicates minimum case

Burst Read (multiple bank) with Auto-Precharge @BL=4 CL=3



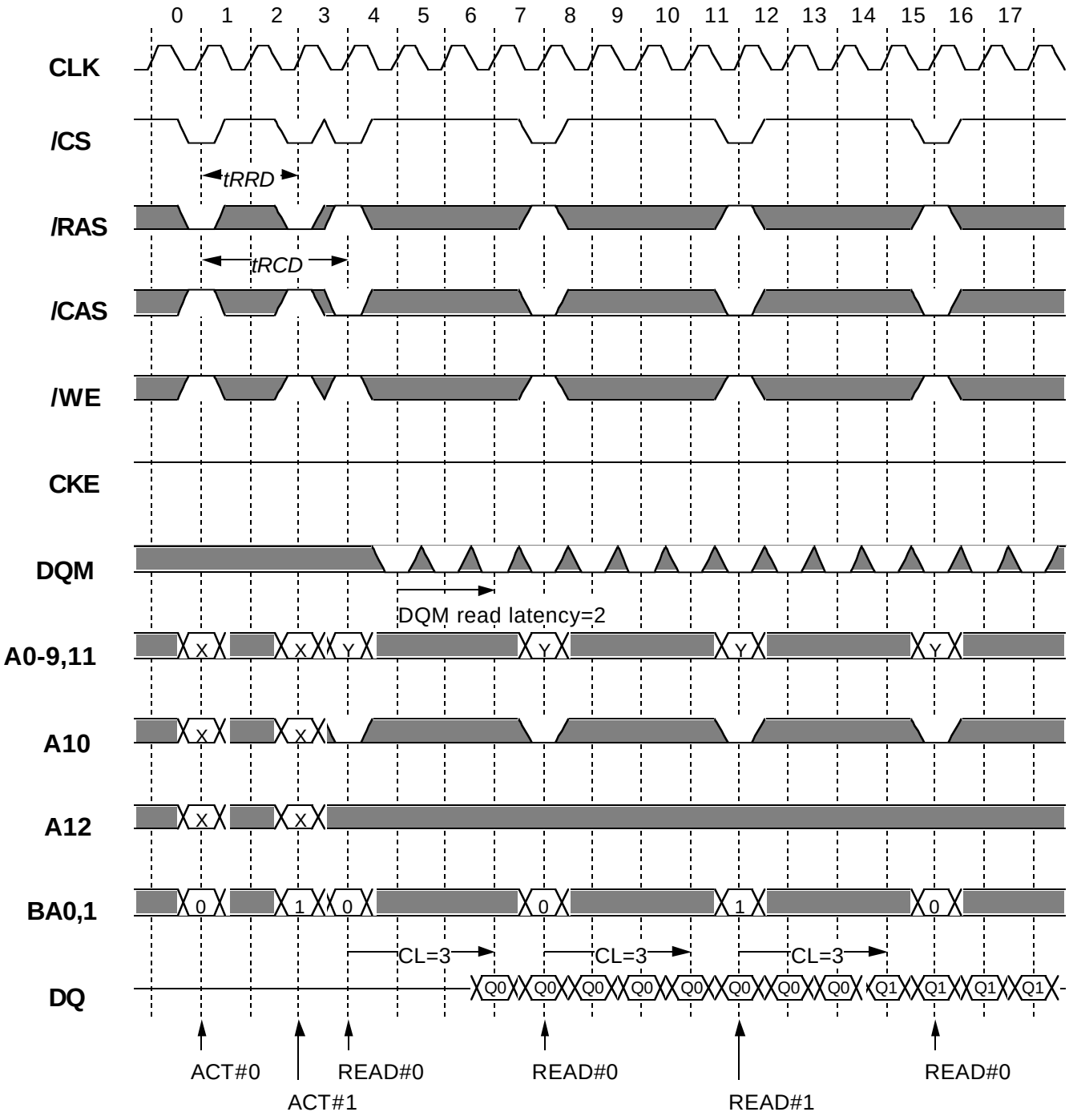
Italic parameter indicates minimum case

Page Mode Burst Write (multi bank) @BL=4



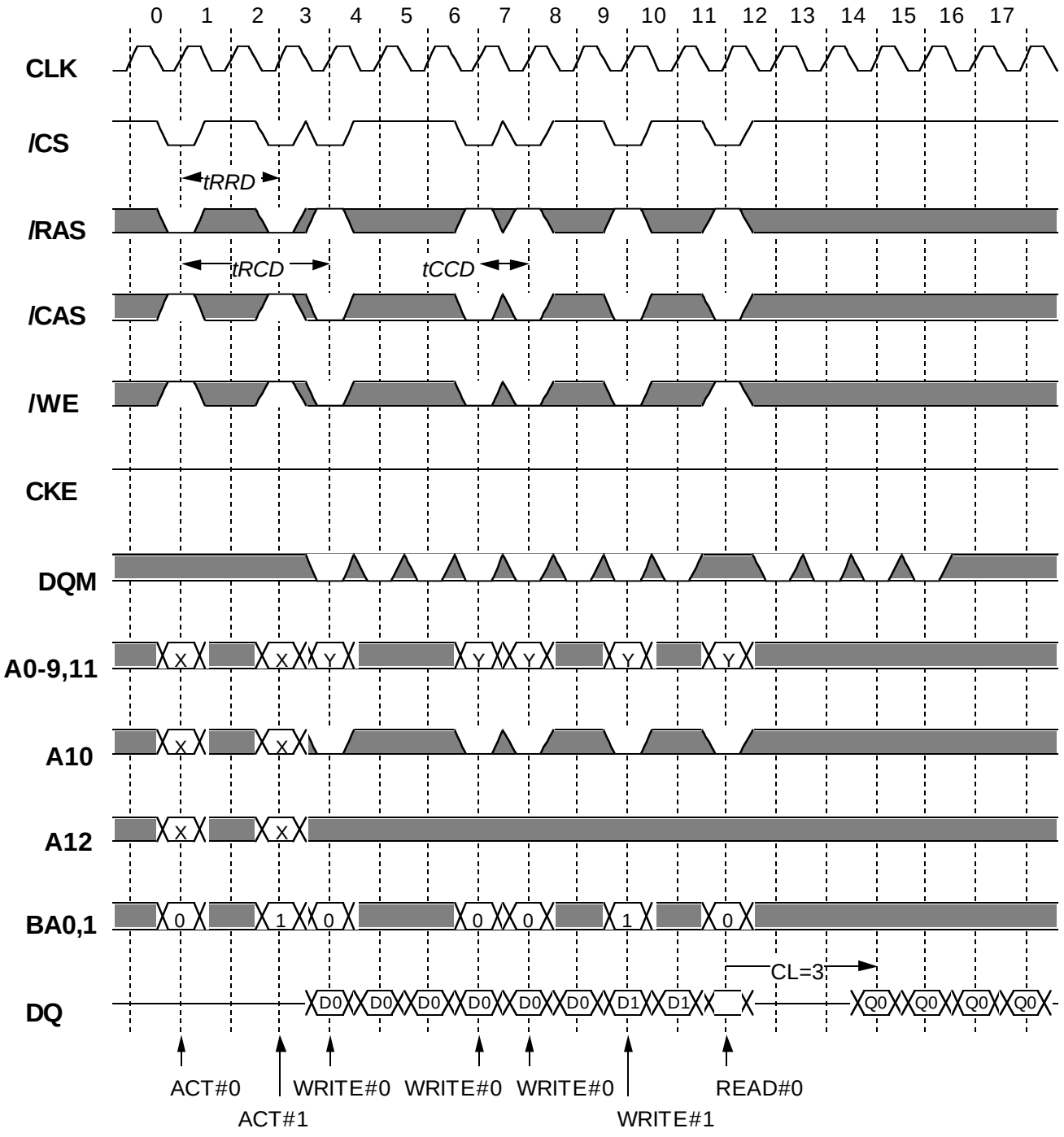
Italic parameter indicates minimum case

Page Mode Burst Read (multi bank) @BL=4 CL=3



Italic parameter indicates minimum case

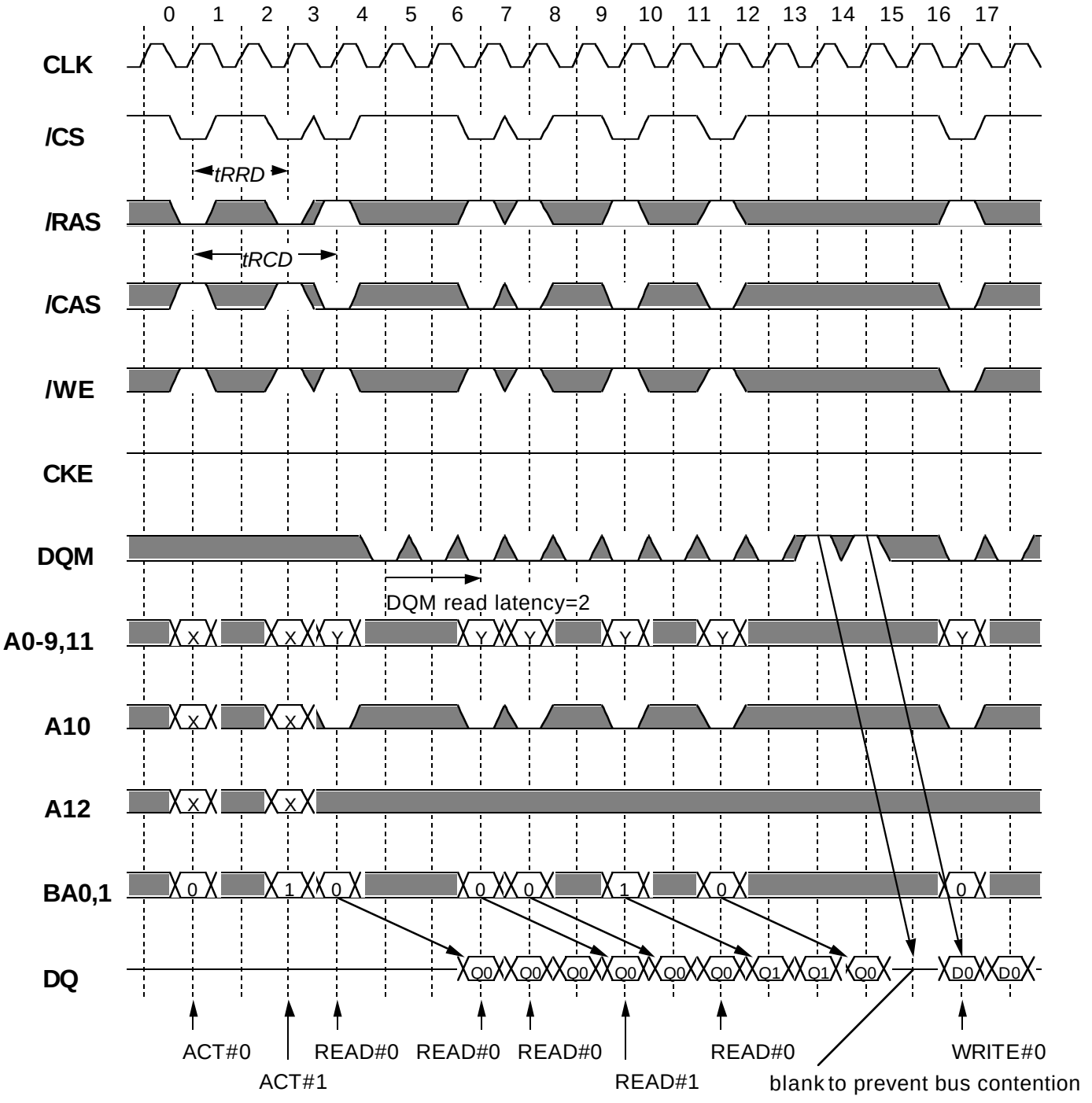
Write Interrupted by Write / Read @BL=4



Burst Write can be interrupted by Write or Read of any active bank.

Italic parameter indicates minimum case

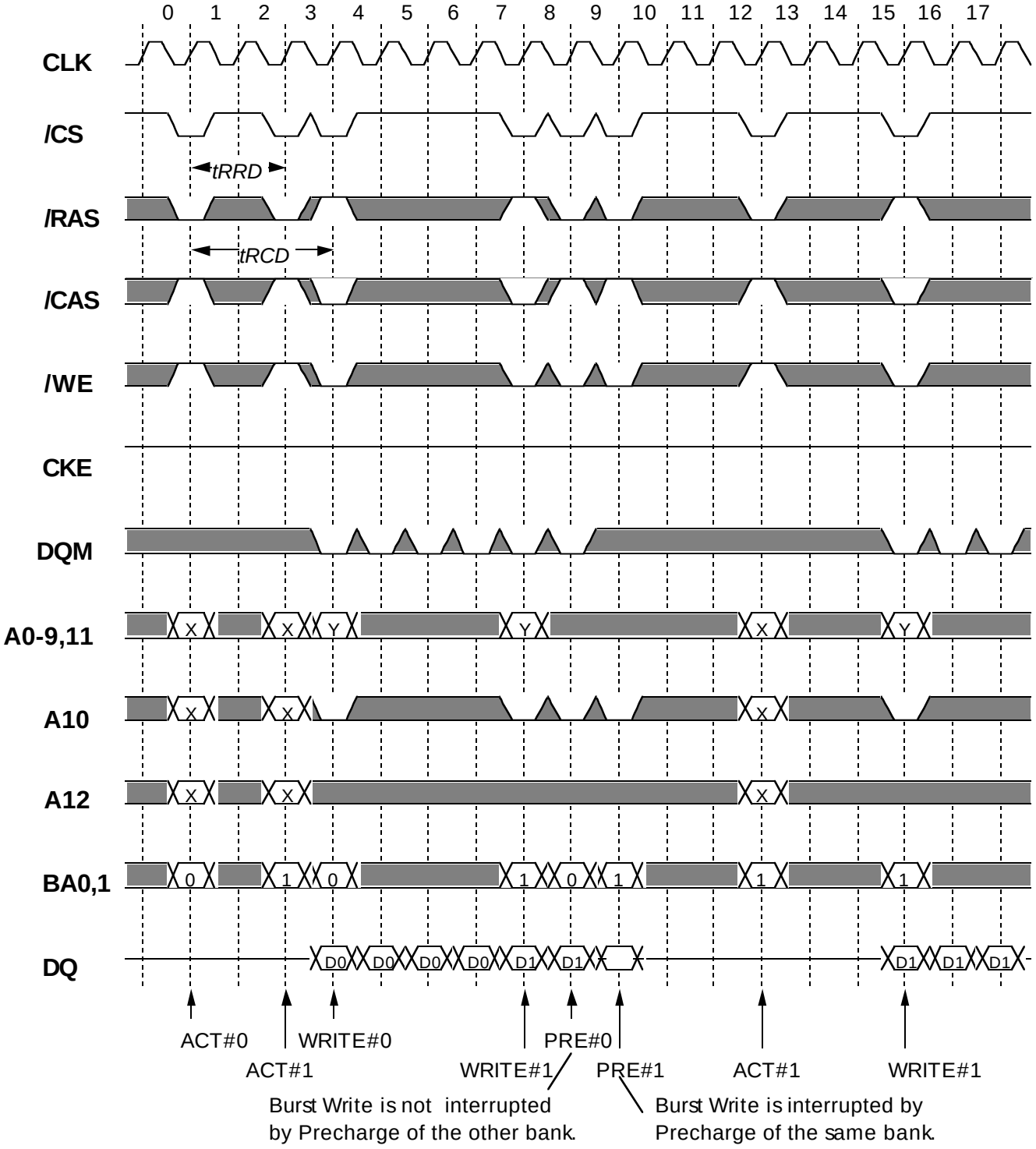
Read Interrupted by Read / Write @BL=4 CL=3



Burst Read can be interrupted by Read or Write of any active bank.

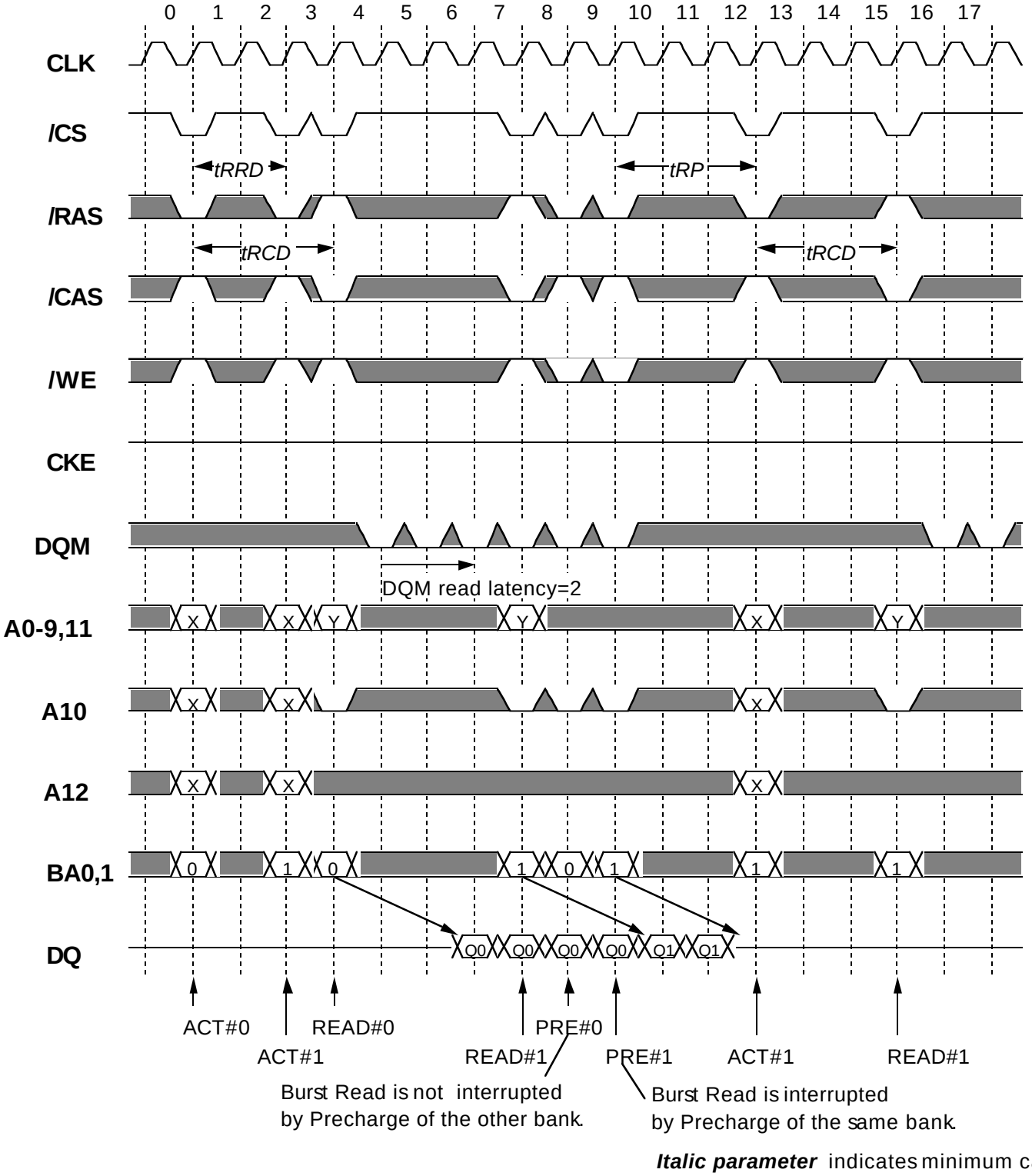
Italic parameter indicates minimum case

Write Interrupted by Precharge @BL=4



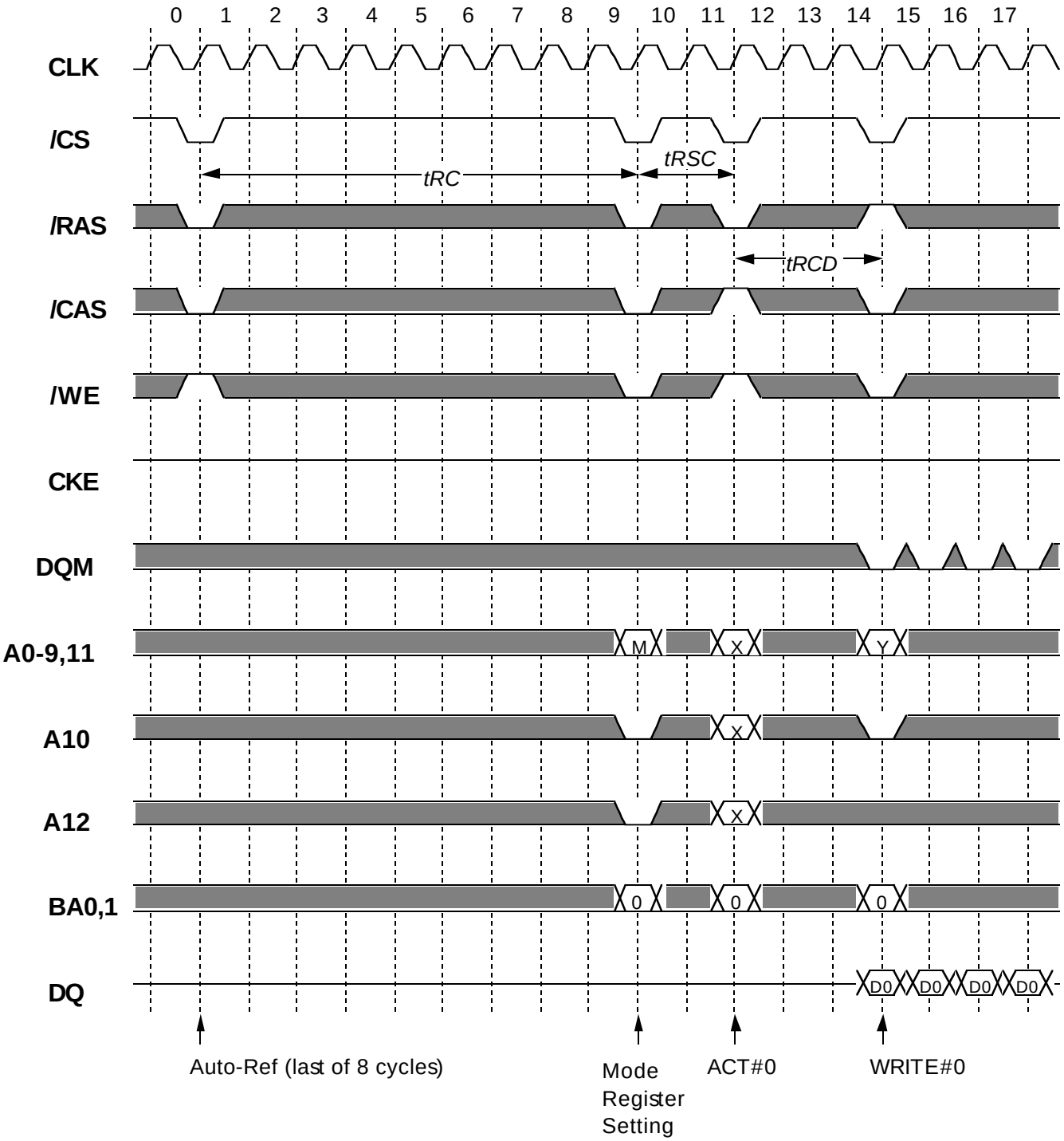
Italic parameter indicates minimum case

Read Interrupted by Precharge @BL=4 CL=3



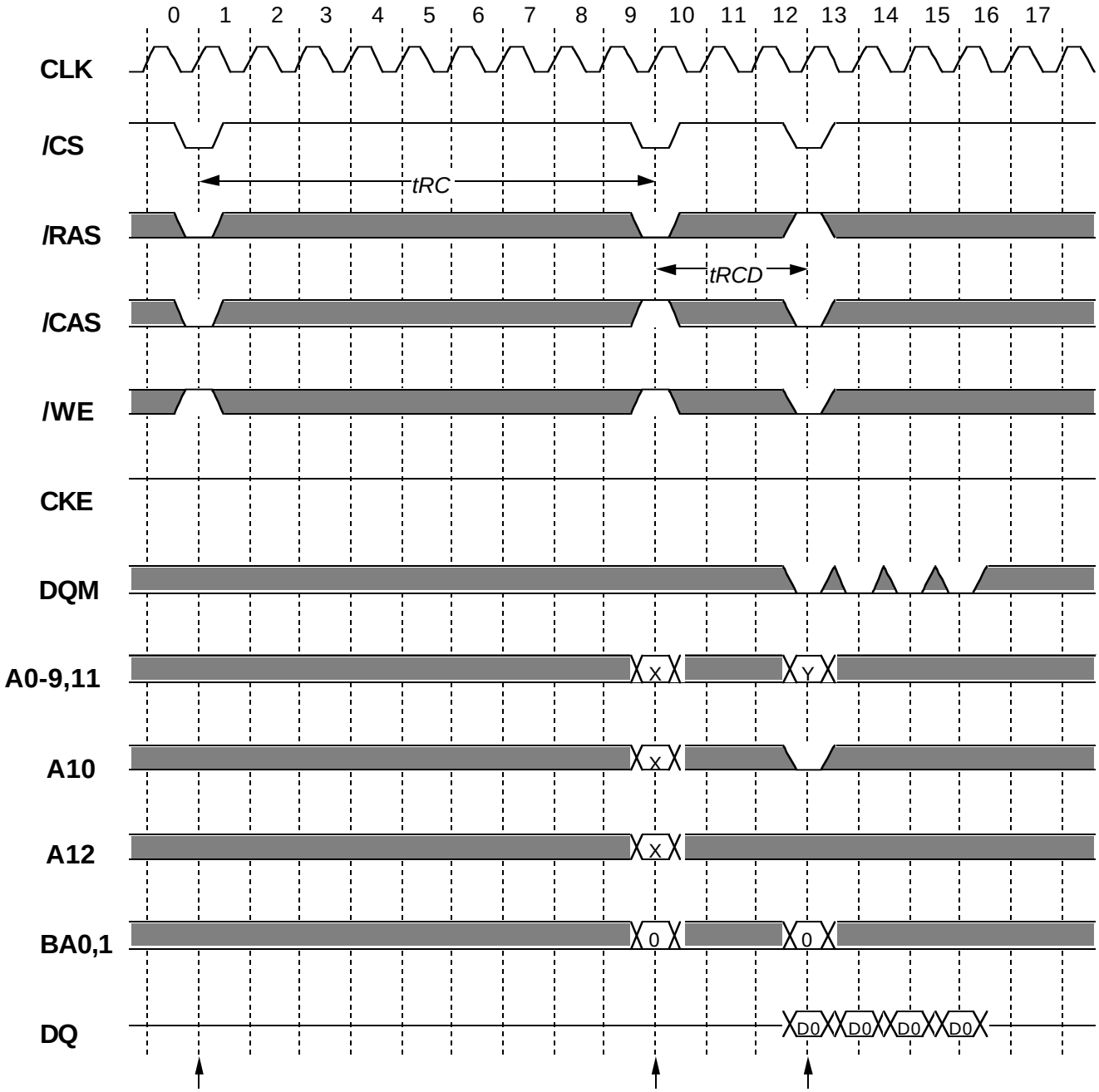
Italic parameter indicates minimum case

Mode Register Setting



Italic parameter indicates minimum case

Auto-Refresh @BL=4

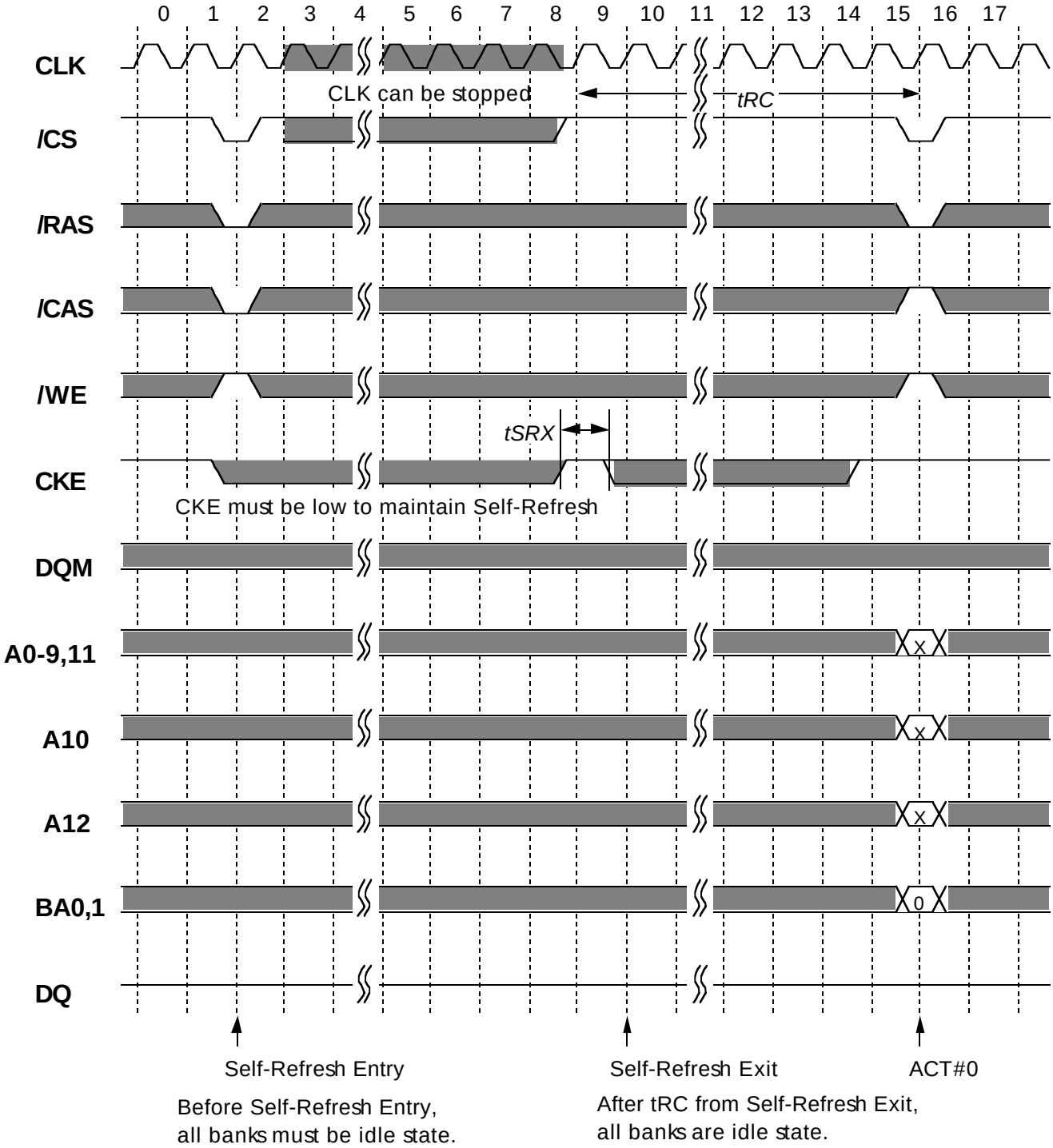


Before Auto-Refresh,
all banks must be idle state.

After tRC from Auto-Refresh,
all banks are idle state.

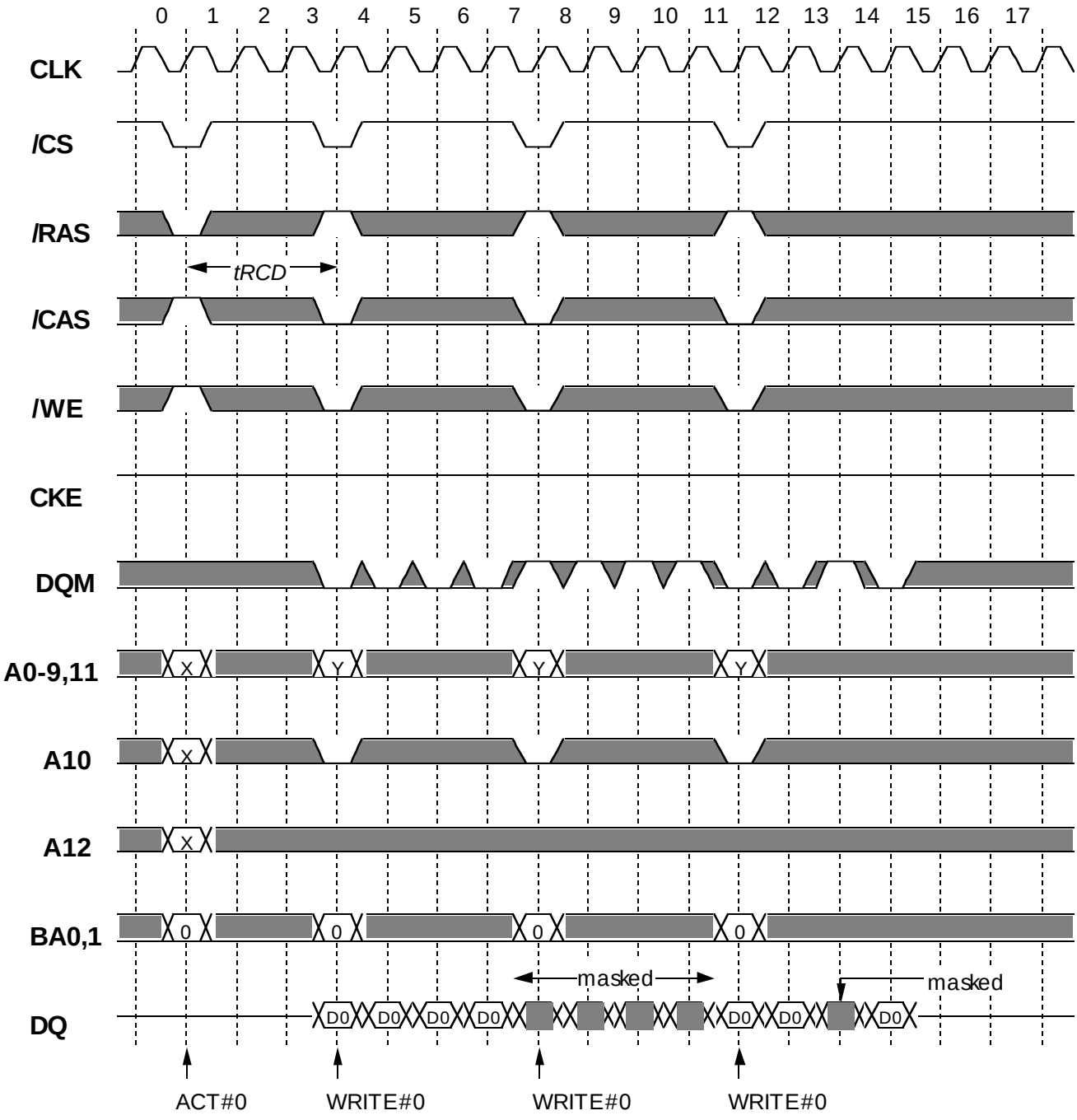
Italic parameter indicates minimum case

Self-Refresh



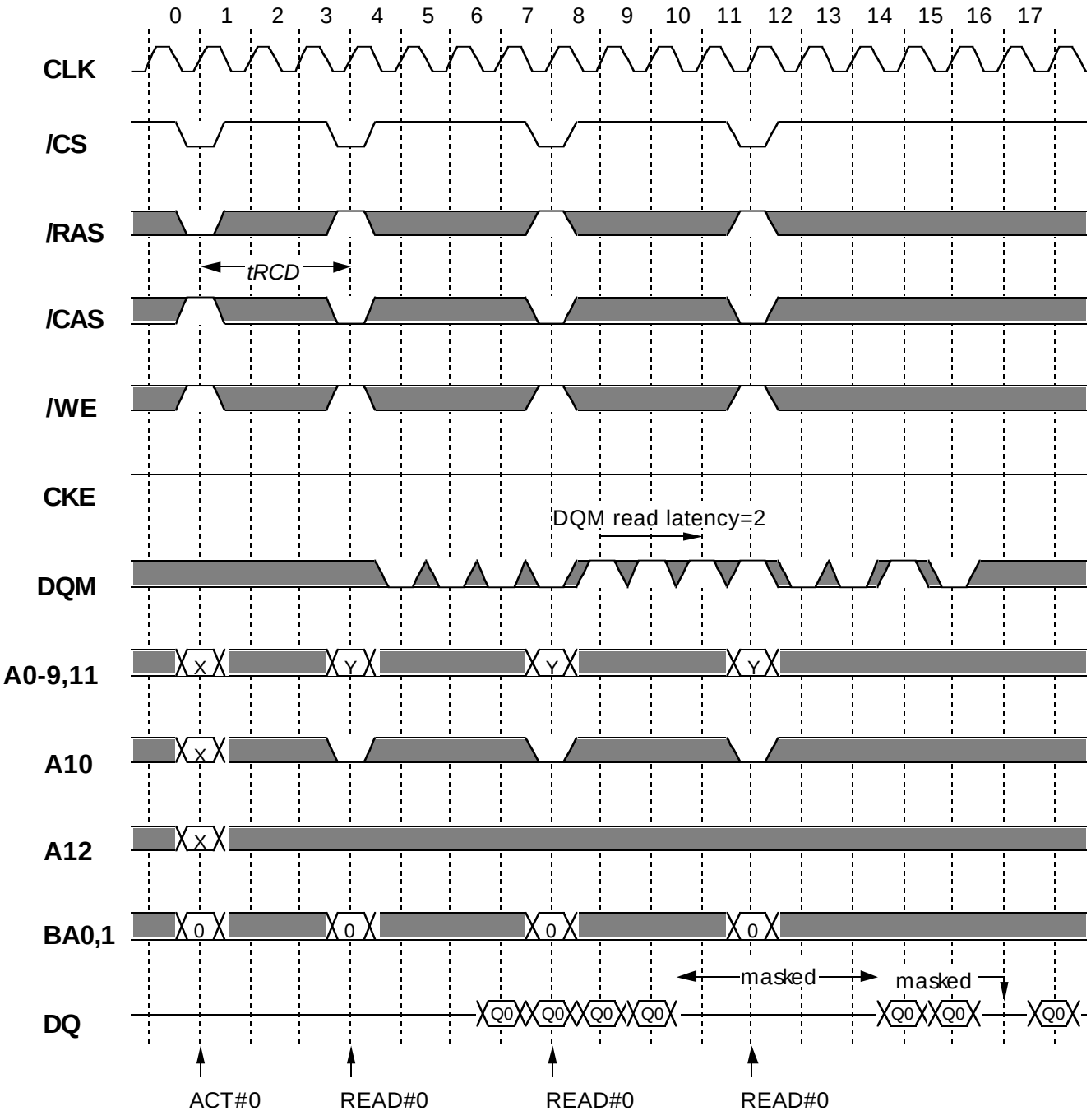
Italic parameter indicates minimum case

DQM Write Mask @BL=4



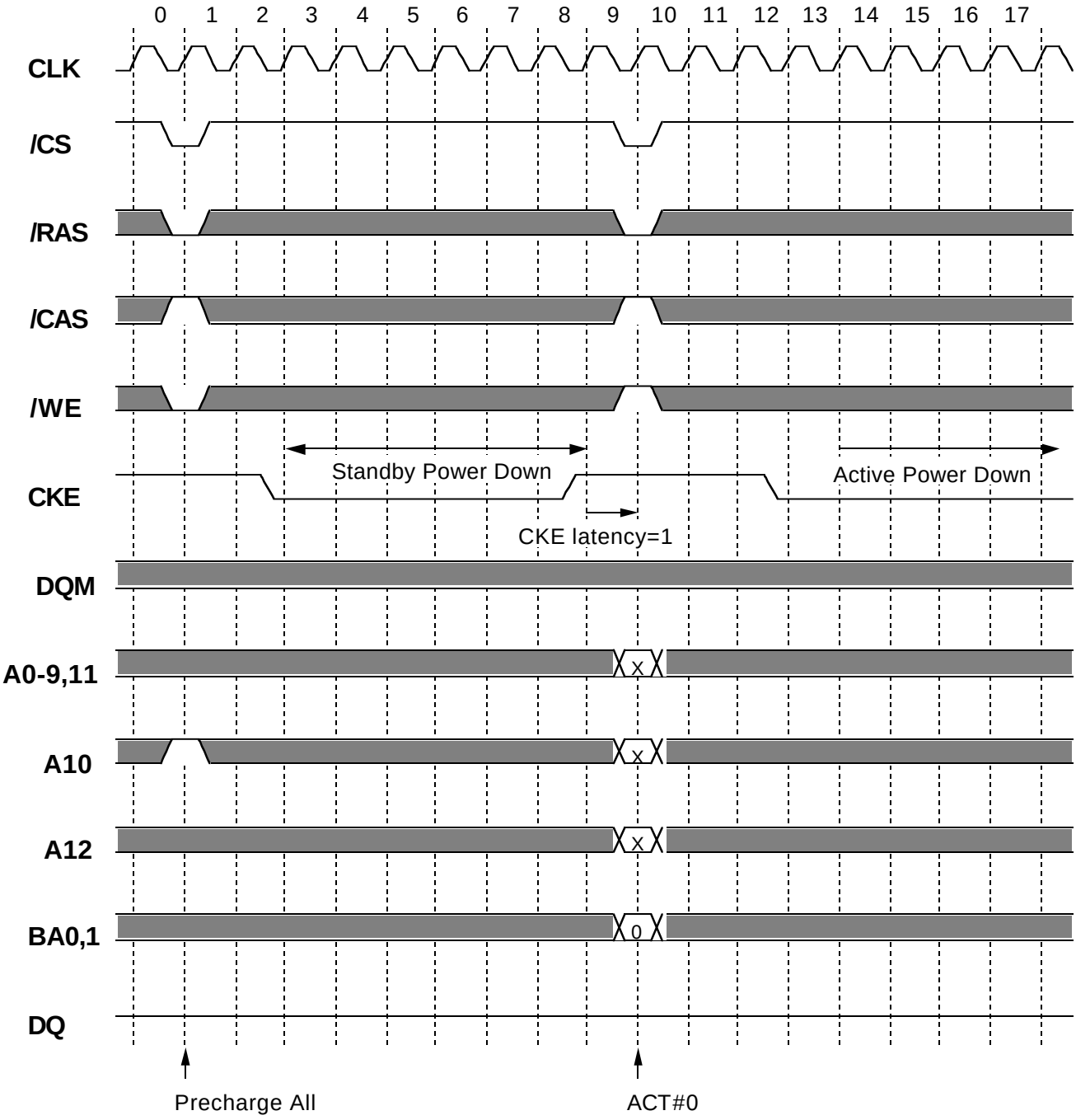
Italic parameter indicates minimum case

DQM Read Mask @BL=4 CL=3



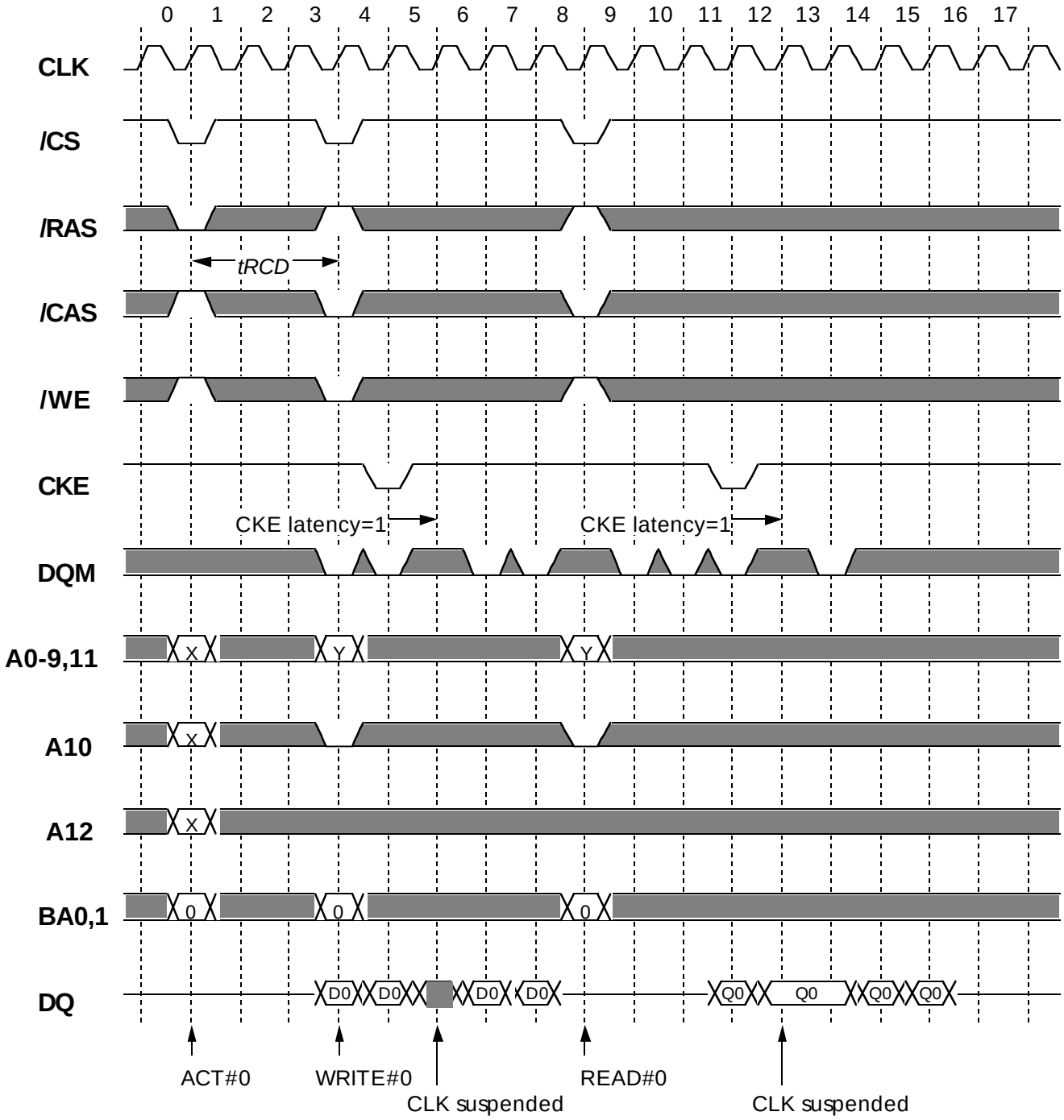
Italic parameter indicates minimum case

Power Down



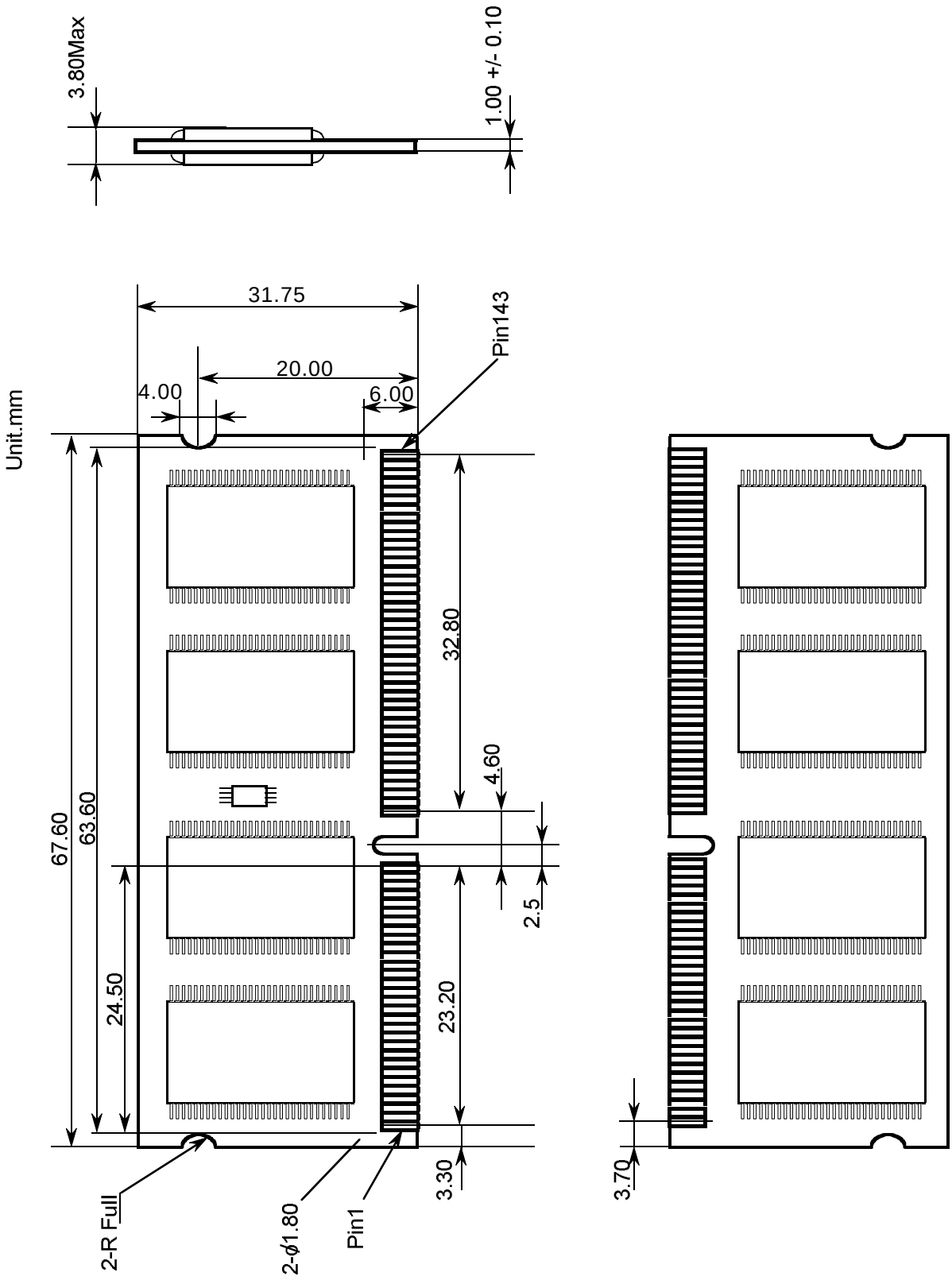
Italic parameter indicates minimum case

CLK Suspend @BL=4 CL=3



Italic parameter indicates minimum case

OUTLINE


3.80Max
1.00 +/- 0.10
31.75
20.00
4.00
6.00
Pin143
Unit.mm
32.80
4.60
2.5
67.60
63.60
24.50
23.20
3.30
3.70
2-R Full
2-ϕ1.80
Pin1

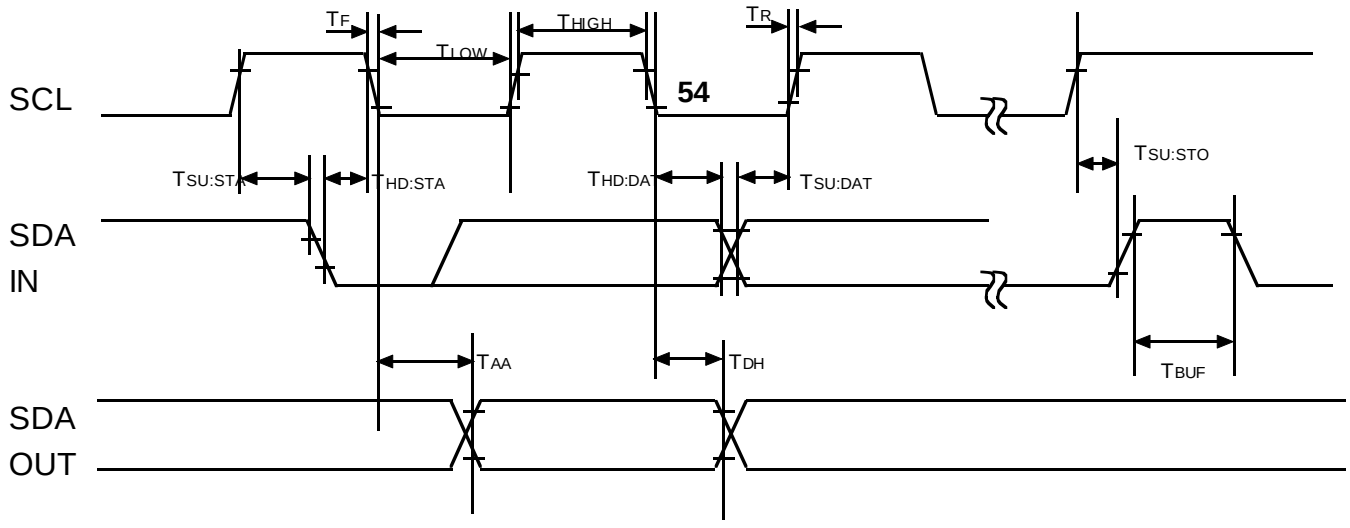
EEPROM Components A.C. and D.C. Characteristics

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
Vcc	Supply Voltage	3.0	3.3	3.6	V
Vss	Supply Voltage	0	0	0	V
VIH	Input High Voltage	Vddx0.7			V
VIL	Input Low Voltage	-0.3		Vccx0.3	V
VOL	Output Low Voltage			0.4	V

EEPROM A.C.Timing Parameters (Ta=0 to 70C)

Symbol	Parameter	Limits		Units
		Min.	Max.	
fSCL	SCL Clock Frequency		80	KHz
TI	Noise Supression Time Constant at SCL, SDA inputs		100	ns
TAA	SCL Low to SDA Data Out Valid	0.3	7.0	us
TBUF	Time the Bus Must Be Free before a New Transmission Can Start	6.7		us
THD:STA	Start Condition Hold Time	4.5		us
TLOW	Clock Low Time	6.7		us
THIGH	Clock High Time	4.5		us
TSU:STA	Start Condition Setup Time	6.7		us
THD:DAT	Data In Hold Time	0		us
TSU:DAT	Data In Setup Time	500	1	ns
TR	SDA and SCL Rise Time		1	us
TF	SDA and SCL Fall Time		300	ns
TSU:STO	Stop Condition Setup Time	6.7		us
TDH	Data Out Hold Time	300		ns
TWR	Write Cycle Time		15	ms

tWR is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle.



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