

**DESCRIPTION**

The NN511000 series is a high performance CMOS Dynamic Random Access Memory organized as 1,048,576 words by 1 bit. The NN511000 series is fabricated with advanced CMOS technology and designed with innovative design techniques resulting in high speed, extremely low power and wide operating margins at both component and system levels.

The NN511000 series features a high speed page mode operation in which a high speed read, write or read-write is performed on any column address along a row address.

An extremely short row address capture time and an asynchronous column address decoder relax the timing constraints associated with address multiplexing.

The outputs are tri-stated by CAS which, in essence, acts as an output enable independent of RAS with very fast CAS to output access time.

Refresh is accomplished by performing RAS only refresh cycles, hidden refresh cycles, CAS before RAS refresh cycles, or normal read or write cycles on the 512 address combinations of A0 to A8 during a 8 ms period.

Multiplexed address inputs permit The NN511000 series to be packaged in a standard 18-pin plastic DIP, 26-pin plastic SOJ, 20-pin plastic ZIP and 24 pin TSOP TYPE I. The package sizes provide high system bit densities and are compatible with widely available automated testing and insertion equipment. System level features include single power supply of 5V ±10% tolerance and direct interface with high performance TTL logic families.

**FEATURES**

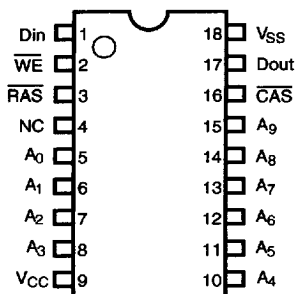
- 1,048,576 × 1 bit Organization
- Single 5V ±10% Power Supply
- Performance Ranges

Parameter	-40	-45	-50	-60	-70
Max. RAS Access Time (t <sub>RAC</sub> )	40ns	45ns	50ns	60ns	70ns
Max. CAS Access Time (t <sub>CAC</sub> )	13ns	15ns	15ns	15ns	20ns
Max. Column Address Access Time (t <sub>AA</sub> )	25ns	25ns	27ns	30ns	35ns
Min. Read/Write Cycle Time (t <sub>RC</sub> )	80ns	80ns	90ns	110ns	130ns

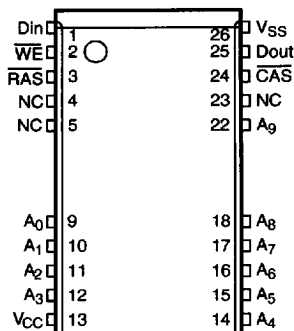
- Fast Page Mode Operation
- Low Power Operation
  - Low Standby Current (CMOS level inputs)
    - Standard 1mA
    - L version 50µA
- 512 Refresh Cycles
  - Standard distributed across 8ms
  - L version distributed across 128ms
- All inputs/Outputs and Clocks fully TTL and CMOS compatible
- Refresh Modes
  - RAS only, CAS before RAS, Hidden Refresh
- High Reliability Packages
  - Plastic 18pin DIP (P18DP-1A0)
  - Plastic 20pin ZIP (P20ZP-2B0)
  - Plastic 26pin SOJ (P26SJ-2A6)
  - Plastic 24pin TSOP TYPE I (P24TV-5B4)

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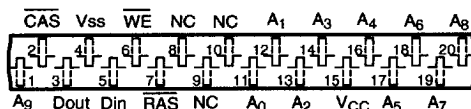
**PIN CONFIGURATION (TOP VIEW)**



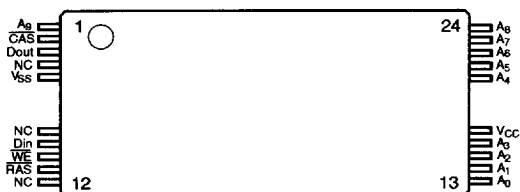
18-pin DIP ( 300mil )  
P18DP-1A0



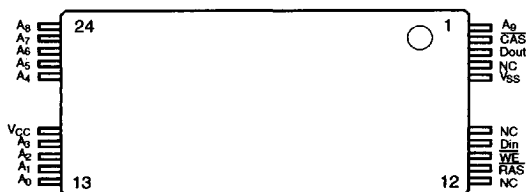
26/20-pin SOJ ( 300mil )  
P26SJ-2A6



20-pin ZIP ( 400mil )  
P20ZP-2B0



20/24-pin TSOP TYPE ( I )  
Normal Bend ( 6 × 16mm )  
P24TV-5B4

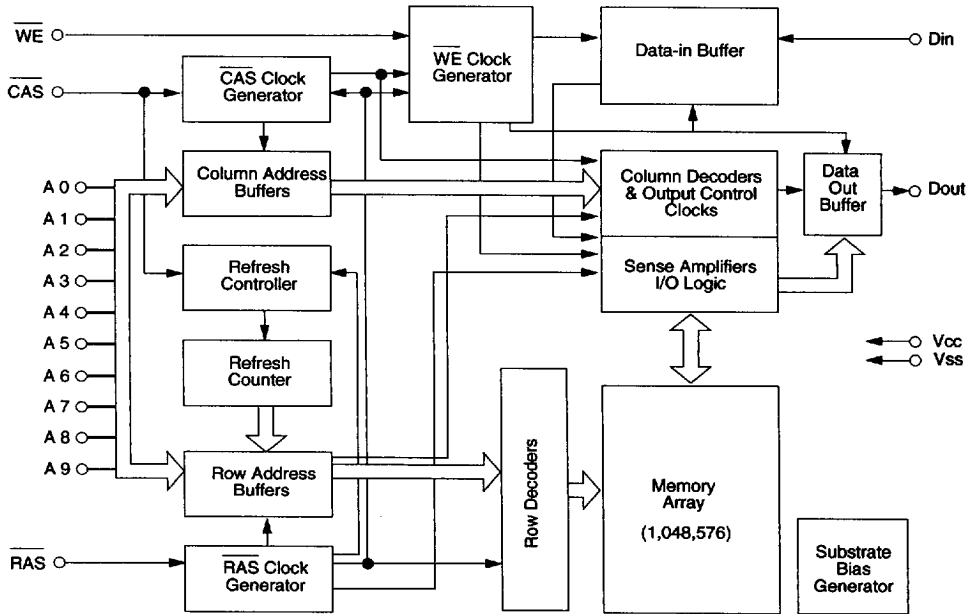


20/24-pin TSOP TYPE ( I )  
Reverse Bend ( 6 × 16mm )  
P24TV-5B4-R

**PIN NAMES**

A0-A9	Address Inputs
RAS	Row Address Strobe
CAS	Column Address Strobe
Din	Data-in
Dout	Data-out
WE	Write Enable
V <sub>CC</sub>	+5V Supply
V <sub>SS</sub>	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
Voltage on Any Pin Relative to V <sub>SS</sub>	V <sub>in</sub> , V <sub>out</sub>	-1 to 7	V
Voltage on V <sub>CC</sub> Relative to V <sub>SS</sub>	V <sub>CC</sub>	-1 to 7	V
Storage Temperature (Plastic)	T <sub>stg</sub>	-55 to +125	°C
Power Dissipation	P <sub>d</sub>	1.0	W
Ambient Operating Temperature	T <sub>a</sub>	0 to +70	°C
Short Circuit Output Current	I <sub>out</sub>	50	mA

Permanent device damage can occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
V <sub>SS</sub>	Supply Voltage	0	0	0	V
V <sub>IH</sub>	Input High Voltage, All Inputs	2.4	—	6.5	V
V <sub>IL</sub>	Input Low Voltage, All Inputs	-1.0	—	0.8	V

Note: All voltage values in this data sheet are with respect to V<sub>SS</sub> unless otherwise specified.

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**DC ELECTRICAL CHARACTERISTICS (0°C ≤ Ta ≤ 70°C, V<sub>CC</sub> = 5.0V ±10%)**

SYMBOL	PARAMETER	SPEED	MIN.	MAX.	UNIT	TEST CONDITIONS	NOTES
I <sub>CC1</sub>	Operating Current	-40		110	mA	t <sub>RC</sub> = t <sub>RC</sub> (min.) RAS, CAS, Address cycling	1, 2
		-45		100	mA		
		-50		90	mA		
		-60		80	mA		
		-70		70	mA		
I <sub>CC2</sub>	Standby Current			1.0	mA	RAS = CAS ≥ (V <sub>CC</sub> - 0.2V)	
				2.0	mA	RAS = CAS ≥ V <sub>IH</sub>	
I <sub>CC3</sub>	Refresh Current (RAS only refresh)	-40		110	mA	t <sub>RC</sub> = t <sub>RC</sub> (min.) RAS cycling, CAS = V <sub>IH</sub>	1
		-45		100	mA		
		-50		90	mA		
		-60		80	mA		
		-70		70	mA		
I <sub>CC4</sub>	Fast Page Mode Current	-40		80	mA	t <sub>PC</sub> = t <sub>PC</sub> (min.) RAS = V <sub>IL</sub> CAS, Address cycling	1,2
		-45		80	mA		
		-50		70	mA		
		-60		60	mA		
		-70		50	mA		
I <sub>CC5</sub>	Refresh Current (CAS before RAS refresh)	-40		110	mA	t <sub>RC</sub> = t <sub>RC</sub> (min.) RAS, CAS cycling	1
		-45		100	mA		
		-50		90	mA		
		-60		80	mA		
		-70		70	mA		
I <sub>CC6</sub>	Refresh Current (L version : CAS before RAS refresh)			150	μA	512 cycles / 128ms t <sub>RAS</sub> ≤ 200ns, WE ≥ (V <sub>CC</sub> - 0.2V) All other inputs are stable at (V <sub>CC</sub> - 0.2V) or (V <sub>SS</sub> + 0.2V)	
I <sub>L1</sub>	Input Leakage Current (Any input pin)		-10	10	μA	0V ≤ V <sub>IH</sub> ≤ 5.5V, Others = 0V	
I <sub>L0</sub>	Output Leakage Current (For high impedance state)		-10	10	μA	RAS ≥ V <sub>IH</sub> (min.), CAS ≥ V <sub>IH</sub> (min.) 0V ≤ V <sub>OUT</sub> ≤ 5.5V	
V <sub>OH</sub>	Output High Voltage		2.4		V	I <sub>OH</sub> = -5.0 mA	
V <sub>OL</sub>	Output Low Voltage			0.4	V	I <sub>OL</sub> = 4.2 mA	

- Notes: 1. I<sub>CC1</sub>, I<sub>CC3</sub>, I<sub>CC4</sub> and I<sub>CC5</sub> depend on cycle rate.  
2. I<sub>CC1</sub> and I<sub>CC4</sub> depend on output loading. Specified values are obtained with the outputs open.

**CAPACITANCE (0°C ≤ Ta ≤ 70°C, V<sub>CC</sub> = 5.0V ±10%, f = 1MHz)**

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C <sub>IN1</sub>	Address(A0 ~ A9)	—	5	pF
C <sub>IN2</sub>	RAS, CAS, WE, Din	—	5	pF
C <sub>OUT</sub>	Dout	—	7	pF

**A.C. OPERATING CONDITIONS ( 0 °C ≤ Ta ≤ 70 °C, V<sub>CC</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V) (NOTES 3, 4, 5)**

NO.	NOTES		PARAMETER	-40		-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t <sub>CL1QV</sub>	t <sub>CAC</sub>	Access Time from $\overline{\text{CAS}}$	—	13	—	15	—	15	—	15	—	20	ns	6,13
2	t <sub>CH2QV</sub>	t <sub>CPA</sub>	Access Time from $\overline{\text{CAS}}$ Precharge	—	30	—	30	—	32	—	35	—	40	ns	13,14
3	t <sub>AVQV</sub>	t <sub>AA</sub>	Access Time from Column Address	—	25	—	25	—	27	—	30	—	35	ns	7,13
4	t <sub>RL1QV</sub>	t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}$	—	40	—	45	—	50	—	60	—	70	ns	6,7
5	t <sub>RL1CH1</sub>	t <sub>GSH</sub>	$\overline{\text{CAS}}$ Hold Time	40	—	45	—	50	—	60	—	70	—	ns	
6	t <sub>RL1CH1</sub>	t <sub>CHR</sub>	$\overline{\text{CAS}}$ Hold Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	10	—	10	—	10	—	10	—	10	—	ns	
7	t <sub>CH2CL2</sub>	t <sub>CPN</sub>	$\overline{\text{CAS}}$ Precharge Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	10	—	10	—	10	—	10	—	10	—	ns	
8	t <sub>CH2CL2</sub>	t <sub>CPT</sub>	$\overline{\text{CAS}}$ Precharge Time	10	—	10	—	10	—	10	—	10	—	ns	
9	t <sub>CH2CL2</sub>	t <sub>CP</sub>	$\overline{\text{CAS}}$ Precharge Time (Fast Page Mode)	5	—	5	—	5	—	5	—	5	—	ns	14
10	t <sub>CL1CH1</sub>	t <sub>CAS</sub>	$\overline{\text{CAS}}$ Pulse Width	15	100K	15	100K	15	100K	15	100K	20	100K	ns	
11	t <sub>CL1RL2</sub>	t <sub>CSR</sub>	$\overline{\text{CAS}}$ Setup Time ( $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	5	—	5	—	5	—	5	—	5	—	ns	
12	t <sub>CL1QX</sub>	t <sub>CLZ</sub>	$\overline{\text{CAS}}$ to Output in Low-Z	0	—	0	—	0	—	0	—	0	—	ns	8
13	t <sub>CH2RL2</sub>	t <sub>CRP</sub>	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	—	5	—	5	—	5	—	5	—	ns	
14	t <sub>CL1WL2</sub>	t <sub>CWD</sub>	$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	15	—	15	—	15	—	15	—	20	—	ns	11
15	t <sub>CL1AX</sub>	t <sub>CAH</sub>	Column Address Hold Time	10	—	10	—	10	—	15	—	15	—	ns	
16	t <sub>RL1AX</sub>	t <sub>AR</sub>	Column Address Hold Time Referenced to $\overline{\text{RAS}}$	30	—	30	—	35	—	40	—	40	—	ns	
17	t <sub>AVCL2</sub>	t <sub>ASC</sub>	Column Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns	14
18	t <sub>AVRH1</sub>	t <sub>RAL</sub>	Column Address to $\overline{\text{RAS}}$ Lead Time	25	—	25	—	27	—	30	—	35	—	ns	
19	t <sub>AVWL2</sub>	t <sub>AWD</sub>	Column Address to $\overline{\text{WE}}$ Delay Time	25	—	25	—	27	—	30	—	35	—	ns	11
20	t <sub>CL1DX</sub> t <sub>WL1DX</sub>	t <sub>DH</sub>	Data Hold Time	10	—	10	—	10	—	10	—	10	—	ns	12
21	t <sub>DVCL2</sub> t <sub>DVWL2</sub>	t <sub>DS</sub>	Data Setup Time	0	—	0	—	0	—	0	—	0	—	ns	12
22	t <sub>CH2QZ</sub>	t <sub>OFF</sub>	Output Buffer Turn-off Delay Time	0	13	0	13	0	13	0	15	0	20	ns	10
23	t <sub>CL1RH1</sub>	t <sub>RSH</sub>	$\overline{\text{RAS}}$ Hold Time	15	—	15	—	15	—	15	—	20	—	ns	
24	t <sub>RH2RL2</sub>	t <sub>RP</sub>	$\overline{\text{RAS}}$ Precharge Time	25	—	25	—	25	—	30	—	40	—	ns	
25	t <sub>RL1RH1</sub>	t <sub>RAS</sub>	$\overline{\text{RAS}}$ Pulse Width	40	100K	45	100K	50	100K	60	100K	70	100K	ns	
26	t <sub>RL1RH1</sub>	t <sub>RASP</sub>	$\overline{\text{RAS}}$ Pulse Width (Fast Page Mode)	40	100K	45	100K	50	100K	60	100K	70	100K	ns	
27	t <sub>RL1CL1</sub>	t <sub>RCD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	13	25	13	30	13	35	13	45	13	50	ns	6
28	t <sub>RH2CL2</sub>	t <sub>RPC</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	10	—	10	—	10	—	10	—	10	—	ns	
29	t <sub>RL1AV</sub>	t <sub>RAD</sub>	$\overline{\text{RAS}}$ to Column Address Delay Time	11	15	11	20	11	23	11	30	11	35	ns	7
30	t <sub>RL1WL2</sub>	t <sub>RWD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	40	—	45	—	50	—	60	—	70	—	ns	11
31	t <sub>CH2WL2</sub>	t <sub>RCH</sub>	Read Command Hold Time	0	—	0	—	0	—	0	—	0	—	ns	9
32	t <sub>RH2WL2</sub>	t <sub>RRH</sub>	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	10	—	10	—	10	—	10	—	10	—	ns	9
33	t <sub>WH2CL2</sub>	t <sub>RCS</sub>	Read Command Setup Time	0	—	0	—	0	—	0	—	0	—	ns	

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**NN511000 series**  
**CMOS 1M × 1bit Dynamic RAM**

NO.	SYMBOL		PARAMETER	-40		-45		-50		-60		-70		UNIT	NOTE
	JEDEC	STD.		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
34	t <sub>RL2RL2</sub>	t <sub>RC</sub>	Random Read or Write Cycle Time	80	—	80	—	90	—	110	—	130	—	ns	
35	t <sub>CL2CL2</sub>	t <sub>PC</sub>	Read or Write Cycle Time (Fast Page Mode)	30	—	30	—	33	—	40	—	45	—	ns	13,14
36	t <sub>RL2RL2</sub>	t <sub>RMW</sub>	Read-Modify-Write Cycle Time	105	—	105	—	115	—	135	—	155	—	ns	
37	t <sub>CL2CL2</sub>	t <sub>PRMW</sub>	Read-Modify-Write Cycle Time (Fast Page Mode)	50	—	50	—	62	—	65	—	70	—	ns	13,14
38	t <sub>REF</sub>	t <sub>REF</sub>	Refresh Period	—	8	—	8	—	8	—	8	—	8	ms	15
39	t <sub>RL1AX</sub>	t <sub>RAH</sub>	Row Address Hold Time	8	—	8	—	8	—	8	—	8	—	ns	
40	t <sub>AVRL2</sub>	t <sub>ASR</sub>	Row Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns	
41	t <sub>T</sub>	t <sub>T</sub>	Transition Time (Rise and Fall)	2	50	2	50	2	50	2	50	2	50	ns	4,5
42	t <sub>CL1WH1</sub>	t <sub>WCH</sub>	Write Command Hold Time	10	—	10	—	10	—	10	—	15	—	ns	
43	t <sub>WL1WH1</sub>	t <sub>WCP</sub>	Write Command Pulse Width	10	—	10	—	10	—	10	—	15	—	ns	
44	t <sub>WL1CL2</sub>	t <sub>WCS</sub>	Write Command Setup Time	0	—	0	—	0	—	0	—	0	—	ns	11
45	t <sub>WL1CH1</sub>	t <sub>CWL</sub>	Write Command to $\overline{\text{CAS}}$ Lead Time	10	—	15	—	15	—	15	—	20	—	ns	
46	t <sub>WL1RH1</sub>	t <sub>RWL</sub>	Write Command to $\overline{\text{RAS}}$ Lead Time	10	—	15	—	15	—	15	—	20	—	ns	

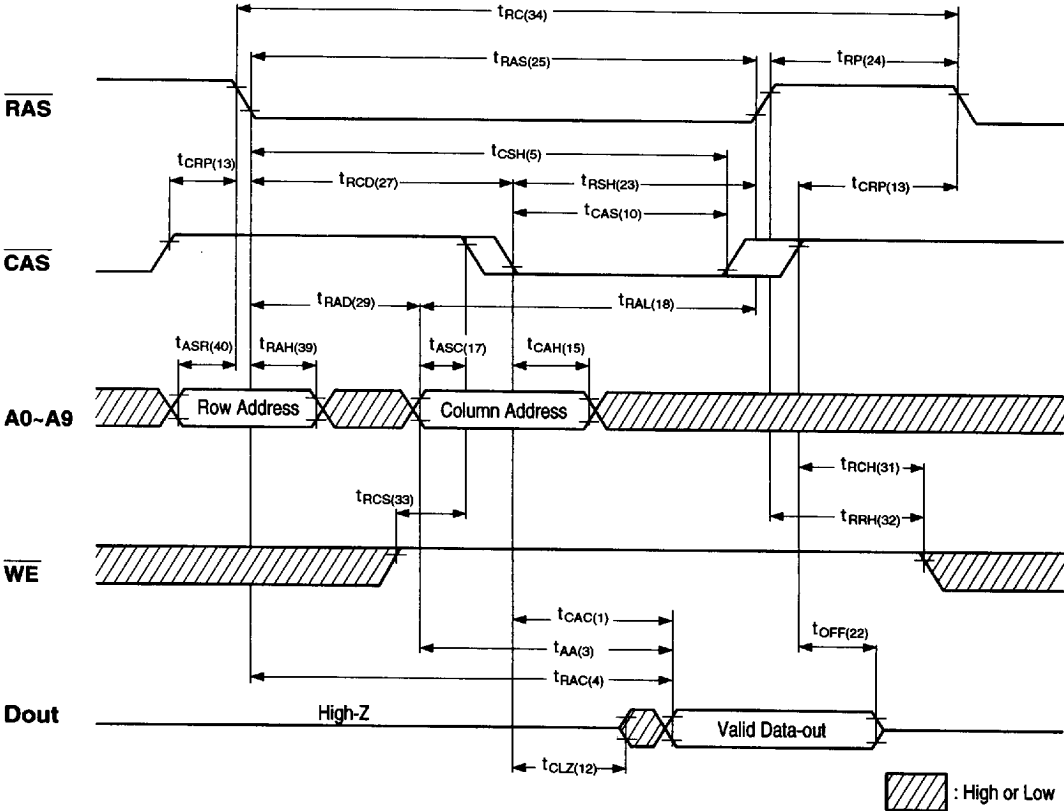
**Notes:**

- Eight Initialization Cycles are required following a 200 $\mu$ s pause after Power Up. These Initialization Cycles may consist of one of the following : RAS only refresh Cycles, Read Cycles, Write Cycles,  $\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  refresh Cycles.
- AC measurements assume  $t_T=3\text{ns}$ . All AC parameters are measured with  $V_{IL}(\text{min.}) \geq V_{SS}$  and  $V_{IH}(\text{max.}) \leq V_{CC}$  and with a load equivalent to two TTL loads and 100pF.
- $V_{IH}(\text{min.})$  and  $V_{IL}(\text{max.})$  are reference levels for measuring timing of input signals. Also, transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- Operation within the  $t_{RCD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RCD}(\text{max.})$  is specified as a reference point only. If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max.})$  limit, then access time is controlled by  $t_{CAC}$ .
- Operation within the  $t_{RAD}(\text{max.})$  limit ensures that  $t_{RAC}(\text{max.})$  can be met.  $t_{RAD}(\text{max.})$  is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max.})$  limit, then access time is controlled by  $t_{AA}$ .
- Assumes three state test load (5pF and a 220 ohm to 1.3V Thevenin equivalent).
- Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a read cycle.
- $t_{OFF}(\text{max.})$  defines the time at which the output achieves an open circuit condition and is not referenced to output voltage levels.
- $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the cycle is an early write cycle and data-out pins will remain open circuit (high impedance) throughout the entire cycle. If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$  and  $t_{AWD} \geq t_{AWD}(\text{min.})$ , the cycle is a read-modify-write cycle and the data-out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data-out (at access time) is indeterminate.
- These parameters are referenced to  $\overline{\text{CAS}}$  leading edge in early write cycles and to  $\overline{\text{WE}}$  leading edge in read-modify-write cycles.
- Access time is determined by the longer of  $t_{AA}$ ,  $t_{CAC}$ , or  $t_{CPA}$ .
- $t_{ASC} \geq t_{CP}$  to achieve  $t_{PC}(\text{min.})$  and  $t_{CPA}(\text{max.})$  values.
- $t_{REF}=128\text{msec}$  for Long Refresh version (L version).

**NPNX**

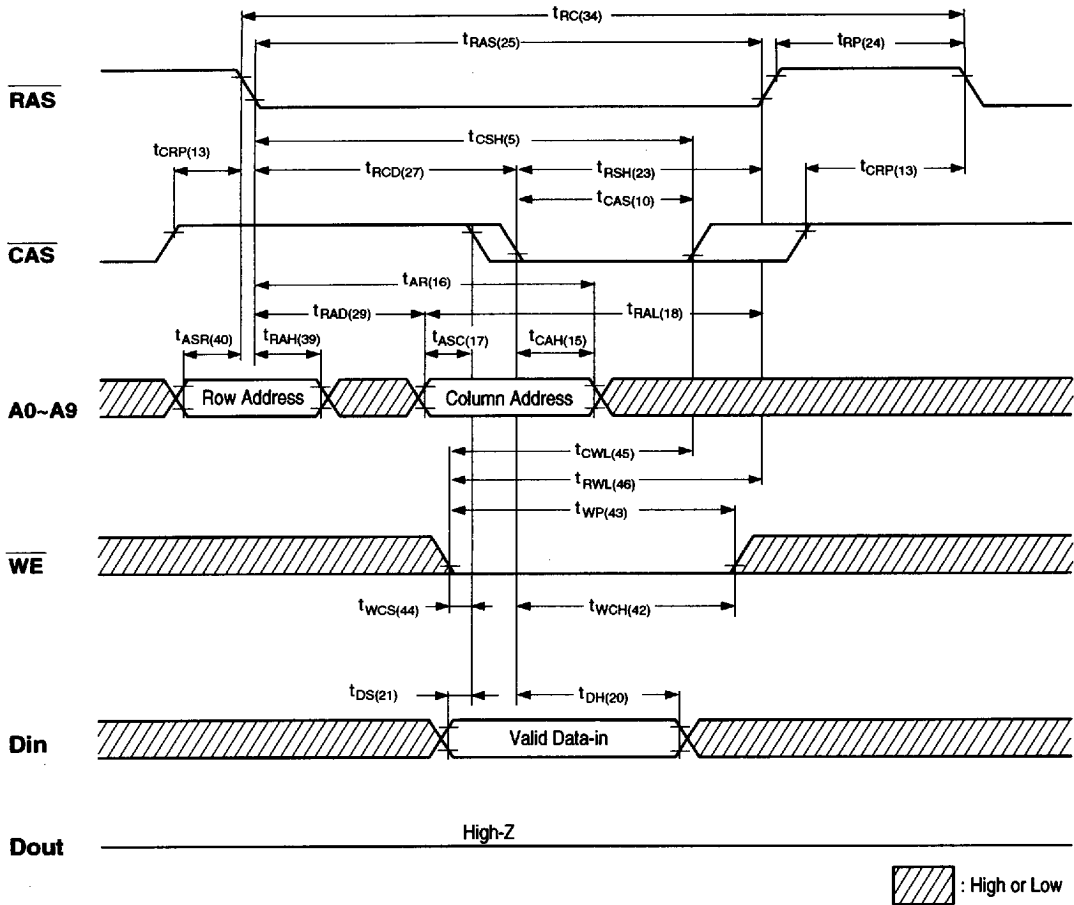
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READ CYCLE



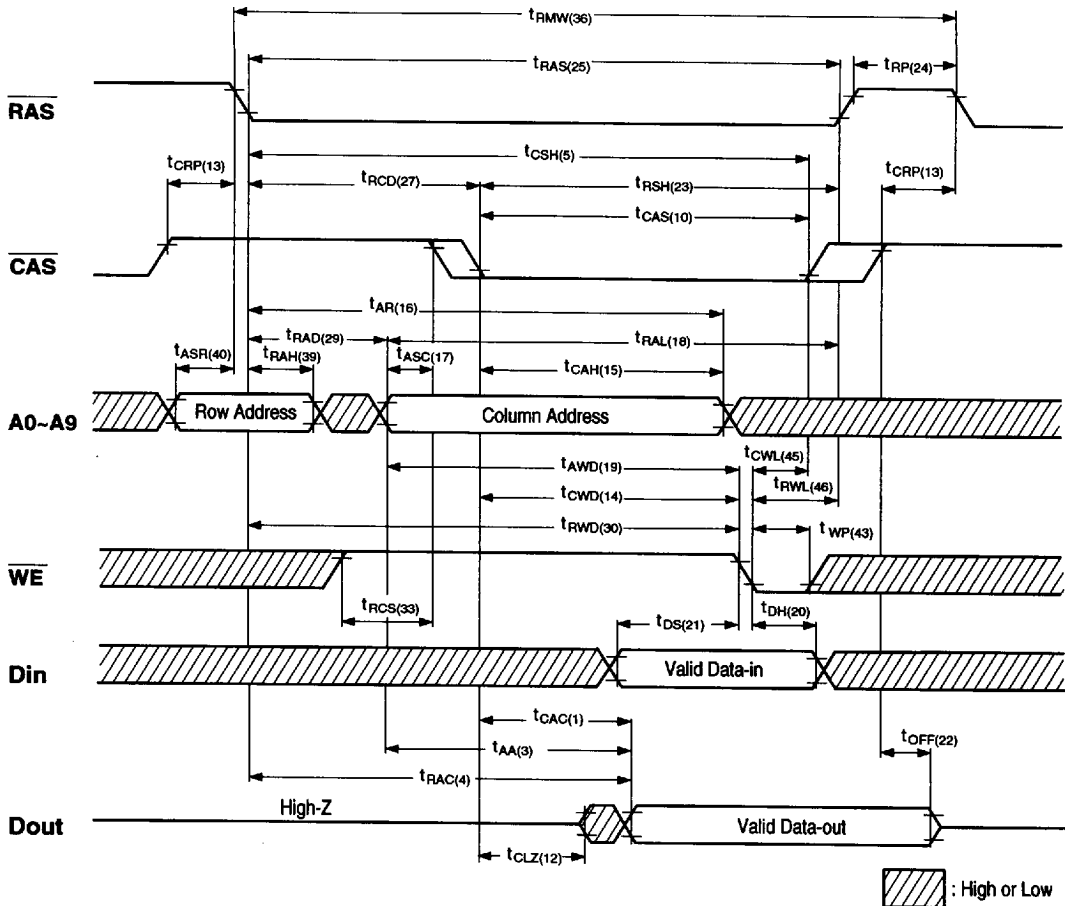
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**WRITE CYCLE (EARLY WRITE)**

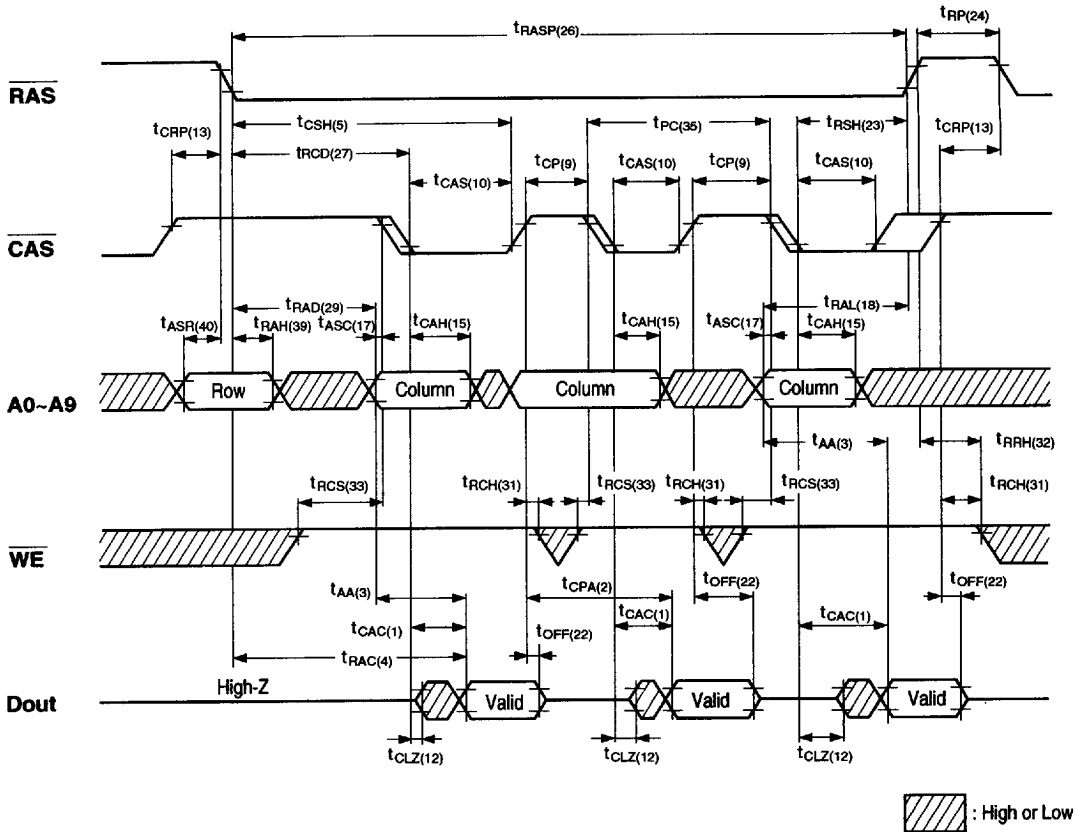




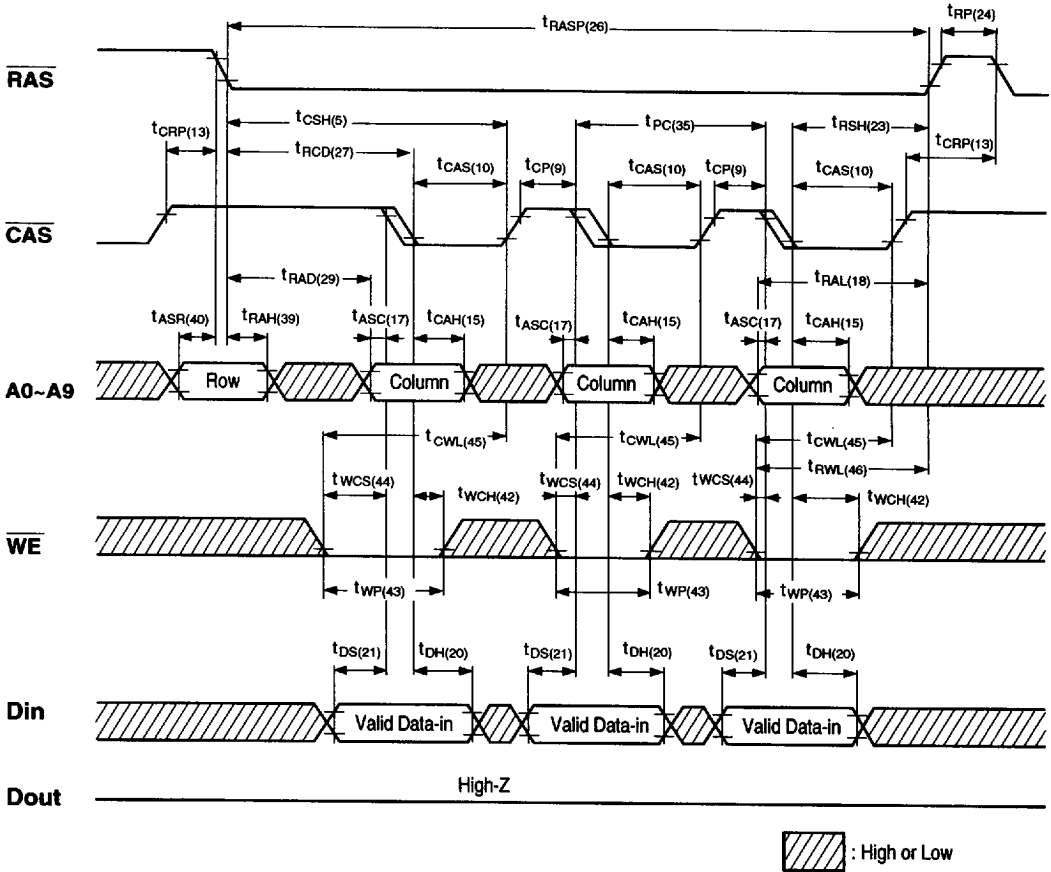
READ-MODIFY-WRITE CYCLE



**FAST PAGE MODE READ CYCLE**

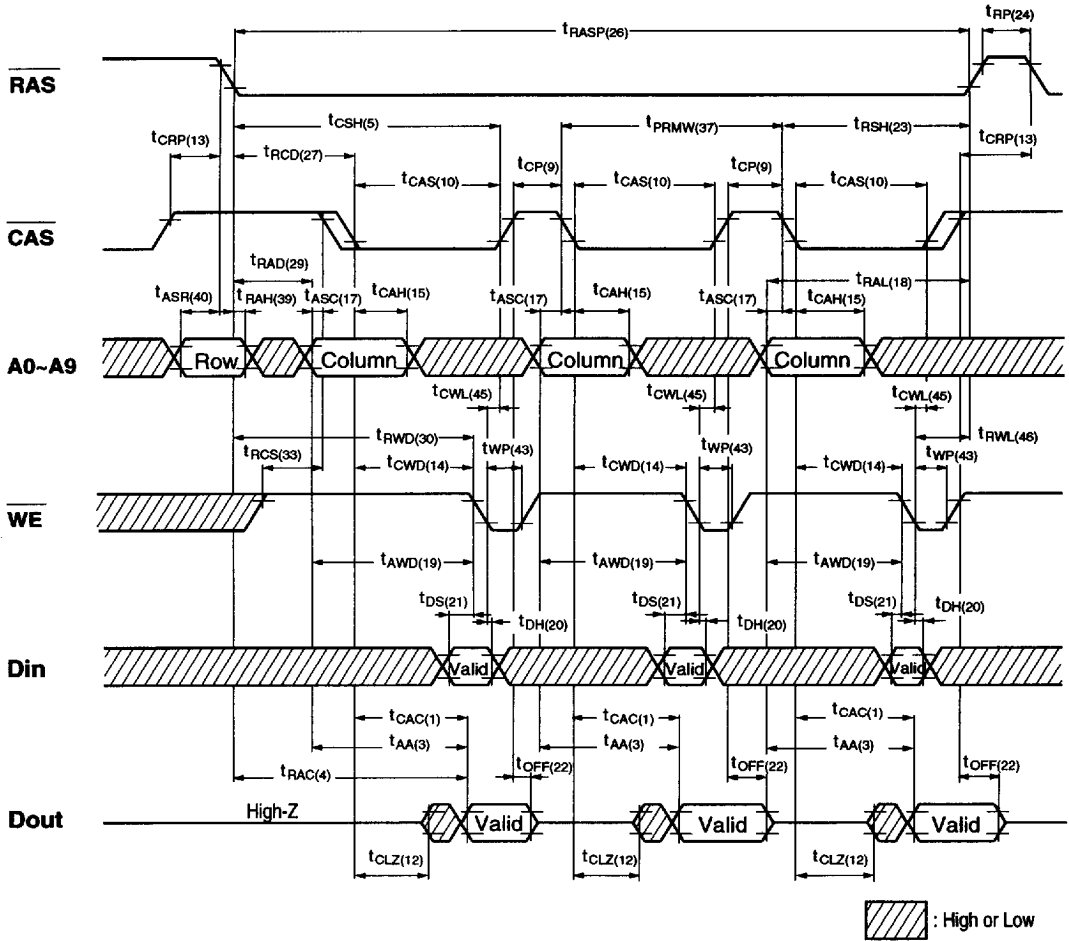


FAST PAGE MODE EARLY WRITE CYCLE

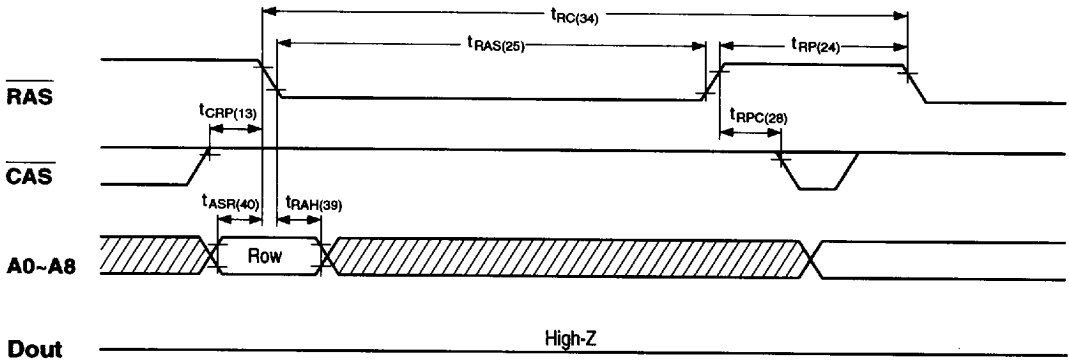


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**FAST PAGE MODE READ-MODIFY-WRITE CYCLE**



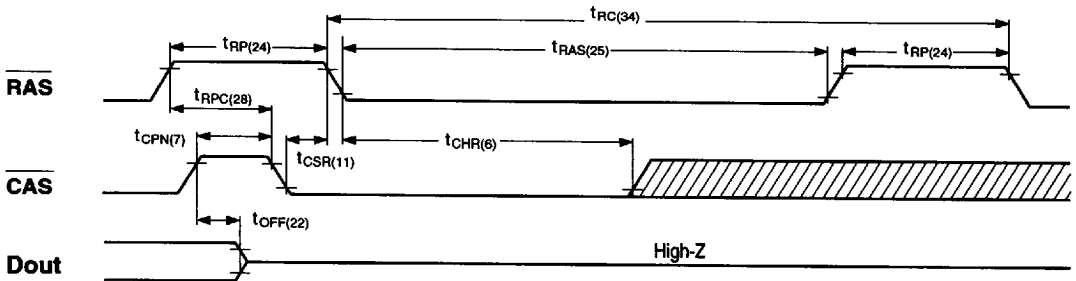
**RAS ONLY REFRESH CYCLE**



Note :  $\overline{WE}$  , A9 = Don't care.

 : High or Low

**CAS BEFORE RAS REFRESH CYCLE**

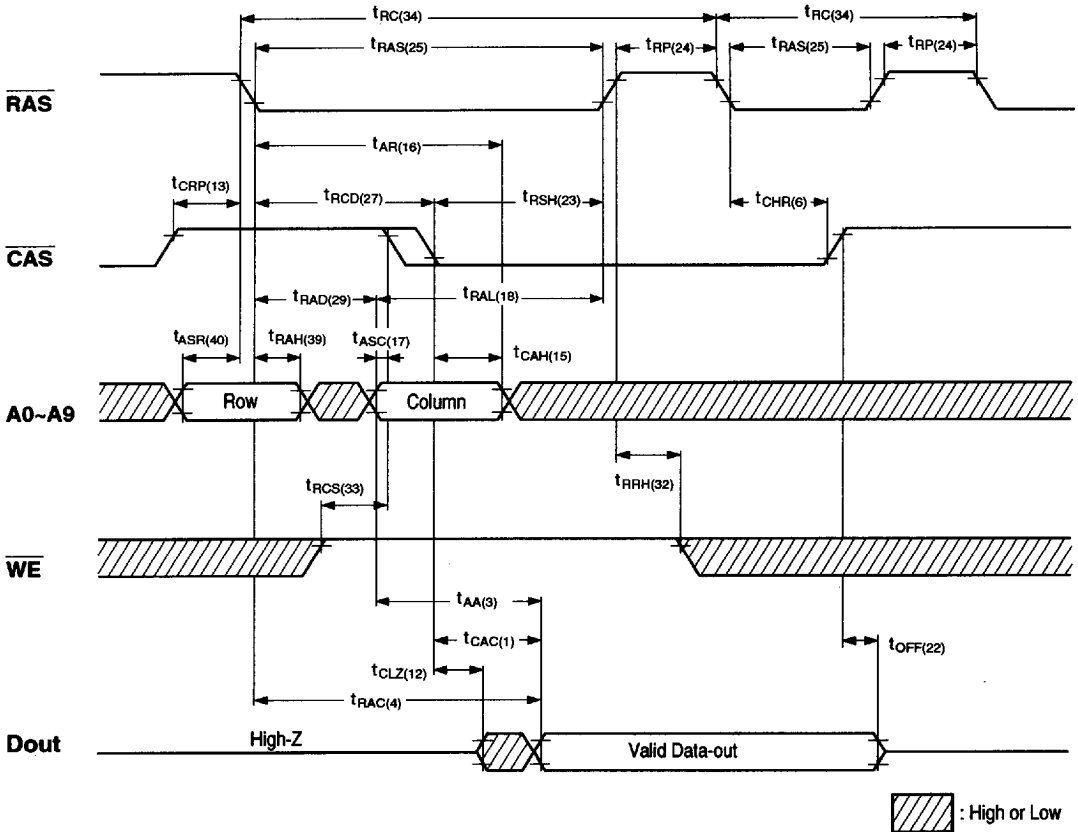


Note :  $\overline{WE}$  , A0~A9 = Don't care.

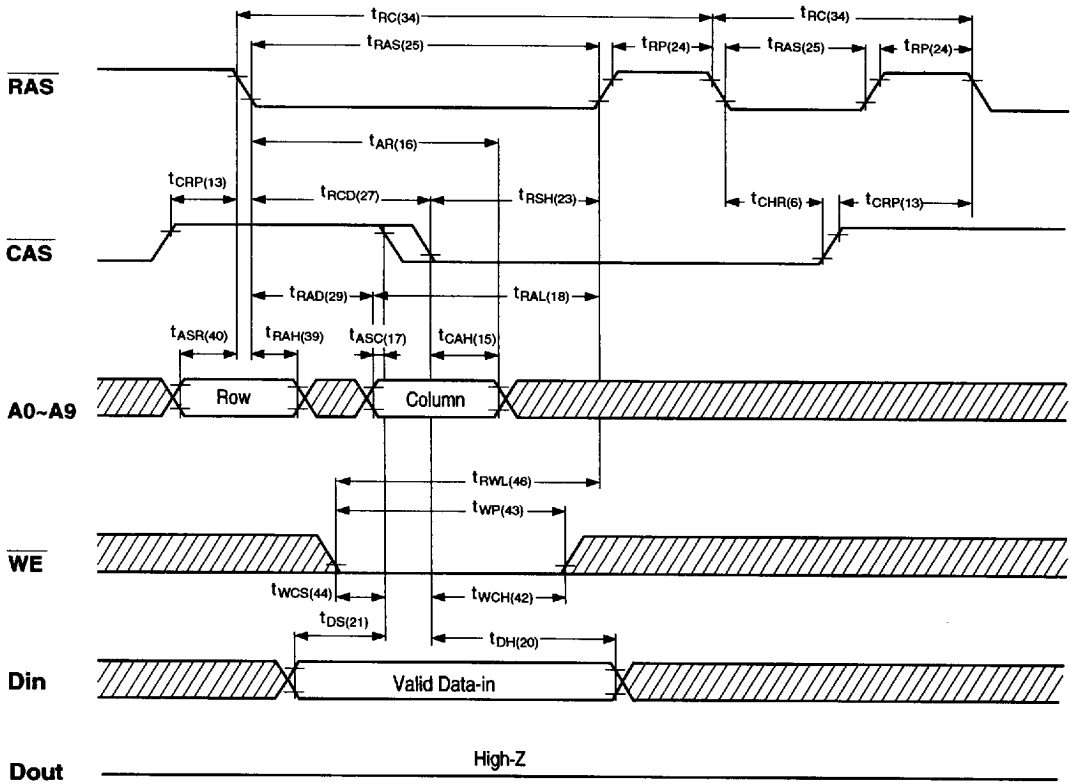
 : High or Low

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**HIDDEN REFRESH CYCLE (READ)**



HIDDEN REFRESH CYCLE (EARLY WRITE)



 : High or Low

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**ORDERING INFORMATION**

**NN511000XX - XX**

