CIRRUS LOGIC®

# CL-SH385

*Preliminary Product Bulletin*

## FEATURES

### General

- **New generation of PCMCIA/ATA disk controller with advanced data integrity capabilities, including:**
  - — Multiple-burst 'on-the-fly' error correction
  - — Header ID on-the-fly error correction
- **Compatible with high-density disk drive technology**
- **Supports both ATA and PCMCIA-ATA standards**
- **Automatic sensing of ATA or PCMCIA-ATA environments**
- **In ATA mode, compatible with industry-standard CL-SH360 disk controller family**

### PCMCIA Features

- **Fully compatible with PCMCIA-ATA Release 2.0 specification**
- **Integrated PCMCIA attribute memory of 256 bytes**
- **Support for all four PCMCIA card configuration registers**
- **Support for all four PCMCIA-ATA command block (task file) addressing modes (I/O and common memory)**
- **Supports 16-bit task file accesses in Common Memory mode**
- **PCMCIA twin-card support**

*(cont.)*

## Advanced Data Integrity PCMCIA-ATA or ATA Mixed-Voltage Disk Controller

## OVERVIEW

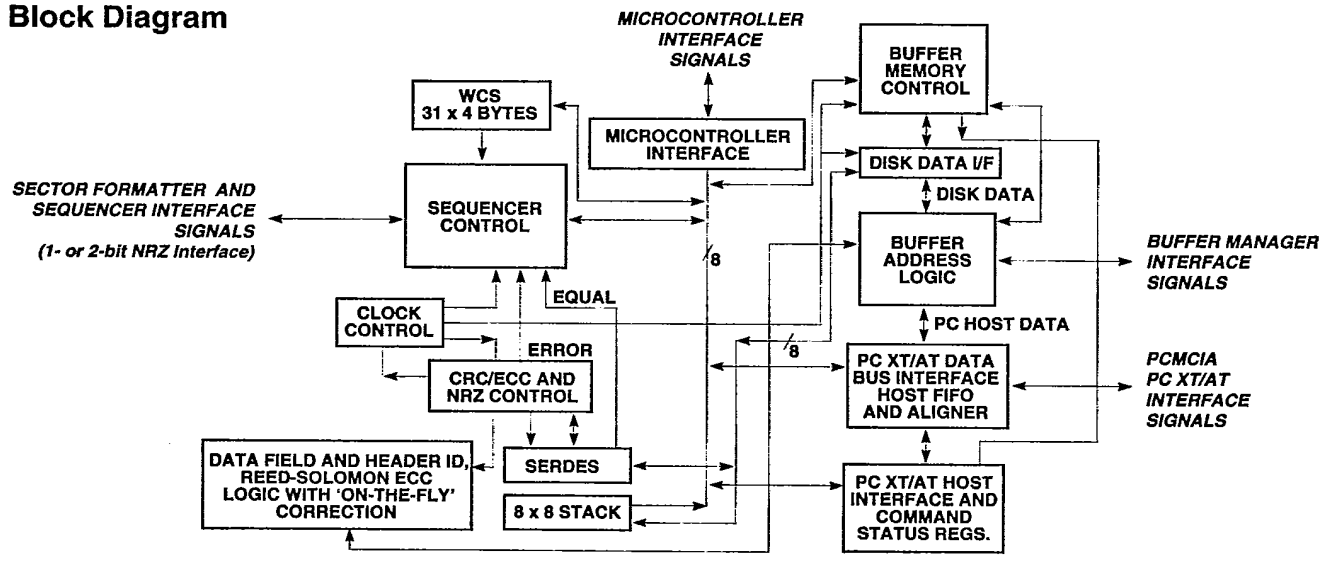
The CL-SH385 is a member of the latest generation of disk controllers from Cirrus Logic. The device offers advanced data integrity features required by the error characteristics of high-density disk drive technology.

The highly integrated CL-SH385 provides a large portion of the hardware necessary to build a Winchester disk controller for PCMCIA or PC XT/AT interfaces. The CL-SH385 is a VLSI chip that combines a complete host interface for both the PCMCIA-ATA and ATA standards with an advanced Winchester disk formatter and a dual-port buffer memory manager. The controller provides the enabling feature set and technology for small, fast, high-capacity, and low-cost drives.

The CL-SH385 supports the full PCMCIA-ATA specification with four card-configuration registers and 256 bytes

*(cont.)*

## Functional Block Diagram



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# CL-SH385

PCMCIA-ATA Disk Controller

## FEATURES (cont.)

### ATA Features

- Host data transfer under programmed I/O, DMA, or Demand mode DMA (EISA Type 'B')
- Supports 8- and 16-bit data transfers on the host bus
- Supports any host speed with programmable and auto-wait-state generation
- AT master/slave protocol

### Disk Controller Features

- Programmable Reed-Solomon error correction code (ECC) allows for on-the-fly correction of up to a single 65-bit error burst or three 17-bit bursts. The code can be programmed for lower ECC overhead and correction capability
- Programmable Reed-Solomon ECC allows on-the-fly correction on the header ID of up to 13-bit error burst
- Fully hardware- and software-compatible with PC XT/AT computers in ATA mode
- Single- and double-bit NRZ rates of 40 and 44 Mbits/second, respectively, at 5.0 volts; 30 and 40 Mbits/second at 3.3 volts
- Multi-level power management capability
- Operates in the range of 3.3 to 5.0 volts VDD (±10%)
- Split-voltage operation enables the host interface to function at a different voltage level than the voltage level for the disk, buffer, and local processor interfaces
- Split-data-field operation for constant density recording formats
- Programmable buffer segments for user-defined caching, read look-ahead, etc.
- Auto-write buffer pointer
- Easy-to-modify, RAM-based disk formatter control store (31 x 4 bytes)
- Full-track, multi-sector transfer capability without local processor intervention
- Support for multiplexed and non-multiplexed address and data bus microcontroller interfaces
- Direct buffer memory addressing of up to 128K bytes of SRAM
- 120-pin VQFP package (1.4mm height)

## OVERVIEW (cont.)

of on-chip attribute memory. The memory is used for the card information structure that describes the PCMCIA disk drive card capabilities and specifications.

The CL-SH385 operates in the range of 3.3 to 5.0 volts. To provide system designers power management flexibility, the controller supports split-voltage operation, that enables the host interface to function at a different voltage than the voltage of the disk, buffer, and local processor interfaces. Multi-levels of hardware- and firmware-controlled power-down modes reduce power consumption to leakage current, making the CL-SH385 ideal for portable and power-sensitive applications.

The CL-SH385 disk formatter consists of a serializer/deserializer, a flexible RAM-based sequencer, and CRC/ECC generation circuitry. A proprietary split-data-field technique optimizes disk capacity, enables faster access times, and increases data rates. The CL-SH385 buffer manager controls up to 128K bytes of SRAM buffer memory as a dual-port circular buffer. It supports a full-track, multi-sector data transfer without microprocessor intervention, allowing creation of low-cost, single-processor disk drive designs. It also allows buffer memory segmentation for user-defined caching algorithms or protected-memory areas.

Several advanced data integrity features are offered by the CL-SH385. The data field error correction code (ECC) consists of a three-way interleaved Reed-Solomon code with programmable redundancy of 4, 5, or 6 bytes-per-interleave, or a total of 12, 15, or 18 bytes of redundancy, respectively. The 'on-the-fly' correction capability can be programmed for 1-, 2-, or up to 3-burst correction. At 6 bytes of redundancy per interleave, the maximum correction capability is for a single error burst of 65 bits, or three error bursts, each of 17-bits length.

The header ID ECC consists of a Reed-Solomon code with programmable redundancy of 6, 7, or 8 bytes, covering up to 12 bytes of header ID data. Correction on the ID is performed on-the-fly for a single burst error and the correction span is programmable for a burst of 5, 9, or 13 bits. The header ID error correction capability offered by the CL-SH385 reduces the 'header not found' error that is the dominant error in many of today's disk drive systems.

The CL-SH385 works with a local microcontroller and supports both multiplexed address and data-bus architecture, similar to the Intel® 8051 or 80196 family and Motorola® 68HC11 microcontrollers, as well as non-multiplexed bus processor architectures. Also provided is a READY signal interface for high-speed microcontrollers. It supports both interrupt and polled processor interfaces. The maskable interrupts include many disk and host interface events. The CL-SH385 also has hardware-to-speed microcontroller access to the buffer memory.

# CL-SH385

*PCMCIA-ATA Disk Controller*

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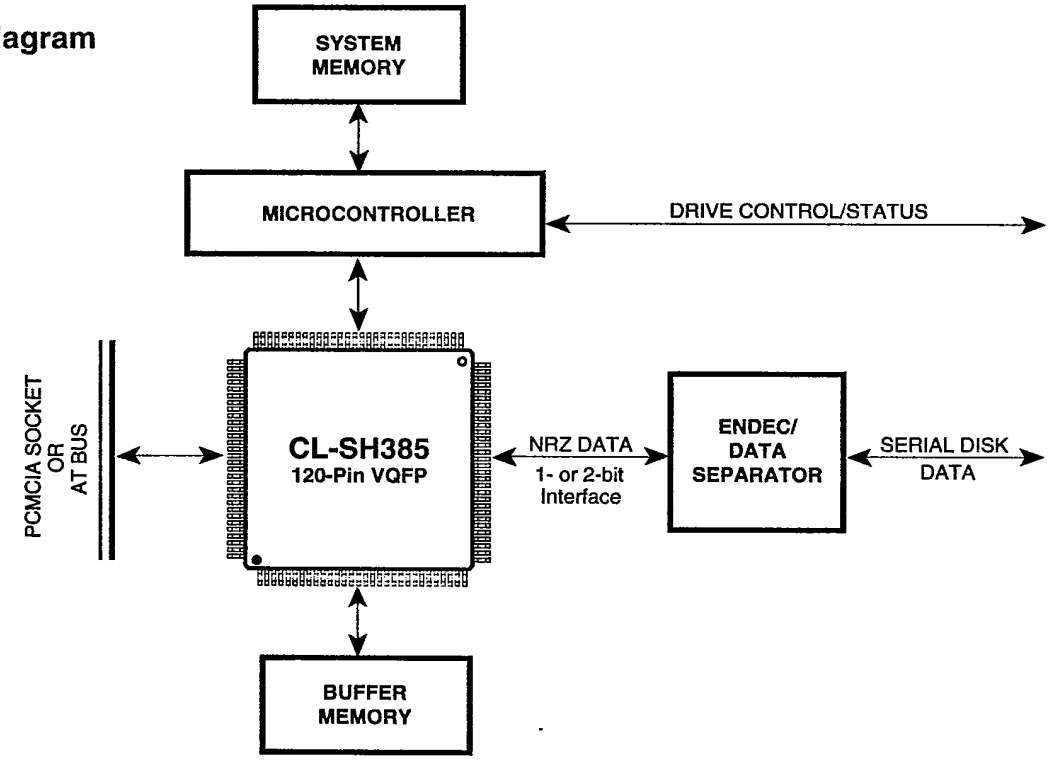
## ADVANTAGES

| Unique Features | Benefits |
|---|---|
| ■ Advanced data integrity features<br>— Multi-burst 'on-the-fly' correction<br>— Header ID ECC with on-the-fly correction | ❒ Compatible with high-density disk drive technology. |
| ■ Full PCMCIA Release 2.0 and PCMCIA-ATA | ❒ Ensures compatibility with software and hardware industry standards for the PCMCIA interface. |
| ■ Supports both ATA and PCMCIA-ATA standards with automatic ATA or PCMCIA environment sensing | ❒ Allows interchange between PCMCIA and ATA systems. |
| ■ 3.3- or 5.0-volt operation with split-voltage capability and dynamic switching between 3.3 and 5.0 volts | ❒ Flexibility in designing systems with single or double voltage requirements as well as conformance to PCMCIA voltage requirements. |
| ■ Multiple levels of power management | ❒ Reduces power consumption to leakage current. |
| ■ Disk data rates of up to 44 Mbits/second | ❒ Ideal for high-performance disk-drive applications. |
| ■ Multi-sector data transfer | ❒ Reduces real-time processing demand on the local disk drive microcontroller, allowing creation of lower-cost, single-processor disk-drive designs. |
| ■ Proprietary split-data-field support | ❒ Optimizes disk capacity, enables faster access times and data rates. |

## System Block Diagram



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