A/D Converters

Type	Resolution (Bits)	Clock Rate (MHz)	Conversion Time (μs)	Power Dissipation Typ. (mW)	Integral Linearity (LSB)	Diff. Linearity (LSB)	Package Number of Pins*
CMOS/SOS Parallel (Flash) Types							
CA3304	4	20	-	30	¼	¼	16 E, D
CA3304A	4	25	-	35	⅛	⅛	16 E, D
CA3306C	6	10	-	55	½	½	18 E, D
CA3306	6	15	-	70	½	½	18 E
CA3306A	6	15	-	70	¼	¼	18 D
CA3318C	8	15	-	150	1.5	+1/-0.8	24 E, D
	Has input bandwidth restriction of 2.5MHz.						
CA3310	10	-	13	-	-	-	-
	½, 1 LSB max. linearity TTL, 3-state output 8mA fm ±5V. Temperature ranges: -40 to +85°C, -55 to +125°C						
HI-7151	10	-	10	150	½	½	28
	TTL, 3-state output						
HI-7152	10	-	5	150	½	½	28
	45mA fm ±5V. Temperature ranges: 0 to +70°C, -40 to +85°C, -55 to +125°C						
I^2L Integrating Types							
CA3162	3 Digits	-	10 (ms)	60	1 (Count)	NMC	16 E
	Part of 2-chip set. To make complete DPM, add CA3161 and 3 PNP transistors.						
CA3162A	3 Digits	-	10 (ms)	60	1 (Count)	NMC	16 E
	-40 to +85°C specified version of CA3162.						

NOTES: 1. A+ 5V supply voltage for all types.
2. Power dissipation is at given sampling rate, at given supply voltage, and does not include reference current.
3. All converters operate from single supply. Specifications are limit values unless noted as typical.
4. All flash and successive approximation A/D converters have three-state CMOS bus driver outputs.
5. Unless noted, all flash and successive approximation A/D converters will accept Nyquist rate input bandwidths.

NMC = No missing codes * See interpretation guide and packaging section

Type	Special Features	Digital Output Format	Input Voltage Range	V_{SUPPLY} / I_{SUPPLY}	Roll Over Error	Package Number of Pins*
4½ Digit						
ICL7135	Under & over range outputs, polarity output	Multiplexed BCD strobes	0 to ±0.2V 0 to ±2V	±5V (typ.) 3mA (max.)	±1 Count	JI, PI
12-Bit						
ICL7109**	Run/hold input, UART handshake. ±12-bit resolution, 1 LSB max. linearity, TTL, 3-state output, 130ms conversion time. Temp. ranges: 0 to +70°C, -25 to +85°C, -55 to +125°C	8/4 bits, separate enables	0 to ±4V 0 to ±3.5V	±5V (typ.) 3mA (max.)	±1 Count	DL, JL, PL
14-Bit						
ICL7104-14 ICL8052	2-chip set, low input leakage, 30pA max. Typical noise (30μV). ±16-bit resolution, 1 LSB max. linearity, TTL, 3-state output, 300ns conversion time. Temp. range: 0 to +70°C	8/6 bits, separate enables	±10V	+5V and ±15V (typ.) 14mA from ±5V	+1 LSB	DL, JL, PL DD, PD
ICL7104-14 ICL8068	2-chip set, low input noise. 2μV typical	8/6 bits, separate enables	±10V	+5V and ±15V (typ.) 1mA (max.)	+1 LSB	DL, JL, PL JD
16-Bit						
ICL7104-16 ICL8052	2-chip set, low input leakage, 30pA max.	8/8 bits, separate enables	±10V	+5V and ±15V (typ.) 1mA (max.)	+1 LSB	DL, JL, PL DD, PD
ICL7104-16 ICL8068	2-chip set, low input noise. 2μV typical.	8/8 bits, separate enables	±10V	+5V and ±15V (typ.) 1mA (max.)	1 LSB	DL, JL, PL JD

Operating temperature range (T_A): 0 to +70°C * See interpretation guide and packaging section
**Operating temperature range also -25 to +85°C, -55 to +125°C