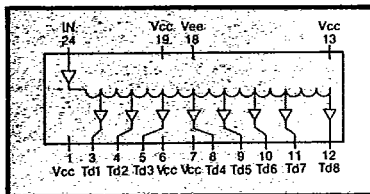


T-47-13

T-47-17

100k ECL DELAY MODULES

- 100k ECL input and output.
- 24-pin transfer-molded DIP package on .400 lead center.
- Available in delays from 5 ns to 200 ns.
- Minimum input pulse width is 25% of total delay.
- 8 equal taps each buffered with 70 ECL fanout capacity.
- Operating temperature range 0 to 85°C.
- Other delays available.
- $V_{ee} = -4.5V \pm 10\%$.
- 500 linear FPM airflow and output terminated with 50 ohm to $-2.0Vdc$.
- Fanout: 70 ECL loads.
- Manufactured to meet Mil-D-23859.
- Commercial with additional testing per customer specification; add suffix "CY" to part number.



Available in these packages:



For dimensions, see drawing 5, page 22.

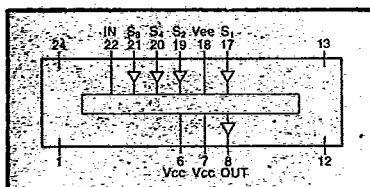
- Contact factory for models with military capability.

Technitrol Part No.	T _{d1} ns	T _{d2} ns	T _{d3} ns	T _{d4} ns	T _{d5} ns	T _{d6} ns	T _{d7} ns	T _{d8} ns	T _d TOL. WIG.	Output Rise Time Max. (ns)
EKLDL005	1.2	2.2	2.5	3.0	3.5	4.0	4.5	5.0	±.25 or 10%	2.0
EKLDL008	1.2	2.2	3.0	4.0	5.0	6.0	7.0	8.0	±.45 or 5%	2.0
EKLDL016	2.0	4.0	6.0	8.0	10.0	12.0	14.0	16.0	±.50 or 5%	2.0
EKLDL025	4.0	7.0	10.0	13.0	16.0	19.0	22.0	25.0	±1.5 or 5%	2.0
EKLDL032	4.0	8.0	12.0	16.0	20.0	24.0	28.0	32.0	±1.5 or 5%	2.0
EKLDL040	5.0	10.0	15.0	20.0	25.0	30.0	35.0	40.0	±1.5 or 5%	2.0
EKLDL048	6.0	12.0	18.0	24.0	30.0	36.0	42.0	48.0	±1.5 or 5%	2.4
EKLDL056	7.0	14.0	21.0	28.0	35.0	42.0	49.0	56.0	±1.5 or 5%	2.8
EKLDL064	8.0	16.0	24.0	32.0	40.0	48.0	56.0	64.0	±1.5 or 5%	3.2
EKLDL072	9.0	18.0	27.0	36.0	45.0	54.0	63.0	72.0	±1.5 or 5%	3.6
EKLDL080	10.0	20.0	30.0	40.0	50.0	60.0	70.0	80.0	±1.5 or 5%	4.0
EKLDL100	12.5	25.0	37.5	50.0	62.5	75.0	87.5	100.0	±1.5 or 5%	5.0
EKLDL120	15.0	30.0	45.0	60.0	75.0	90.0	105.0	120.0	±1.5 or 5%	6.0
EKLDL160	20.0	40.0	60.0	80.0	100.0	120.0	140.0	160.0	±1.5 or 5%	8.0
EKLDL200	25.0	50.0	75.0	100.0	125.0	150.0	175.0	200.0	±1.5 or 5%	10.0

Delay characteristics $V_{ee} = -4.5V \pm .01V$ and $T_a @ 25^\circ C$.
 Delay time measured @ $-1.3V$ level with output pulled-down to $-2.0V$ with 50Ω .
 Rise time measured from 20 to 80% of output pulse.

100k ECL PROGRAMMABLE DELAY MODULES

- 100k ECL input and output.
- 24-pin transfer-molded DIP on .400 lead center.
- 4-bit binary programming gives 15 equal step delays.
- Available in 18 step delays from 0.10 ns to 10 ns; other step delays available.
- Low inherent delay (T_0); $T_0 = 2.0 \pm 1.0$ ns.
- Minimum input pulse width 8 ns or $8 \times$ step delay (W.I.G.).
- Temperature range 0 to $+85^\circ C$.
- $V_{ee} = -4.5V \pm 10\%$.
- 500 linear FPM airflow and output terminated with 50 ohm to $-2.0Vdc$.
- Fanout: 70 ECL loads.
- Manufactured to meet Mil-D-23859.
- For truth table, see page 15.
- Commercial with additional testing, add suffix "CY."



Available in these packages:



For dimensions, see drawing 5, page 22.

- Contact factory for modules with military capability.

Technitrol Part No.	Step Delay			Max. Delay			Output Rise Time Max. (ns)
	ns	±	ns	ns	±	ns	
EKLPGR10	0.10	±	0.075	3.50	±	1.0	2.0
EKLPGR25	0.25	±	0.13	5.75	±	1.0	2.0
EKLPGR50	0.50	±	0.20	9.50	±	1.0	2.0
EKLPGR75	0.75	±	0.25	13.25	±	1.5	2.0
EKLPG010	1.00	±	0.40	17.00	±	1.5	2.0
EKLPG015	1.50	±	0.50	24.50	±	1.5	2.0
EKLPG020	2.00	±	0.50	32.00	±	1.5	2.0
EKLPG025	2.50	±	0.50	39.50	±	2.0	2.0
EKLPG030	3.00	±	0.50	47.00	±	2.5	2.0
EKLPG035	3.50	±	0.50	54.50	±	2.5	2.0
EKLPG040	4.00	±	0.50	62.00	±	3.0	2.0
EKLPG045	4.50	±	0.50	69.50	±	3.0	2.0
EKLPG050	5.00	±	1.00	77.00	±	4.0	2.0
EKLPG060	6.00	±	1.00	92.00	±	5.0	2.0
EKLPG070	7.00	±	1.00	107.00	±	5.0	2.0
EKLPG080	8.00	±	1.00	122.00	±	6.0	2.0
EKLPG090	9.00	±	1.00	137.00	±	7.0	2.0
EKLPG100	10.00	±	1.00	152.00	±	8.0	2.0

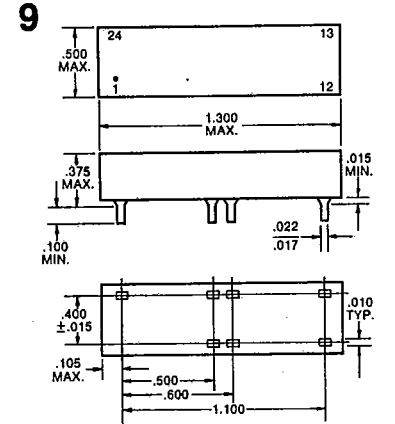
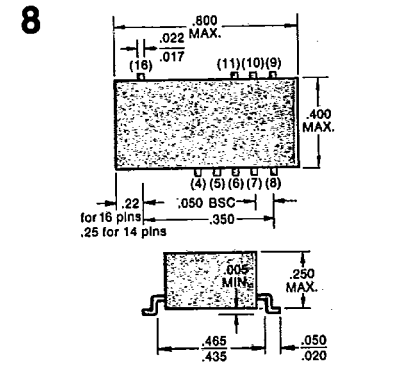
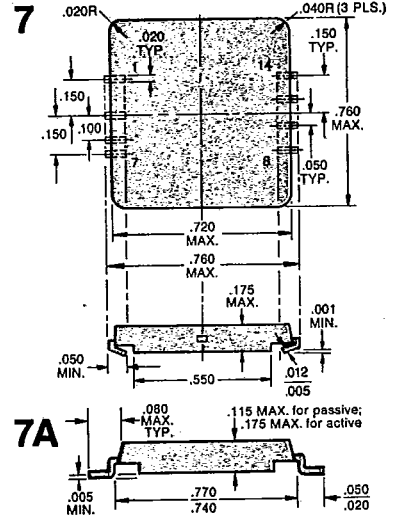
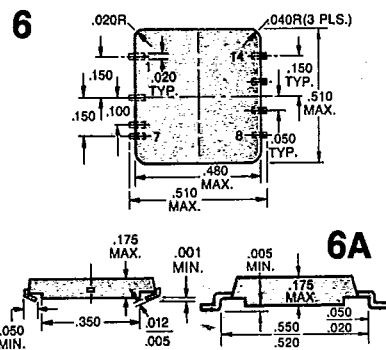
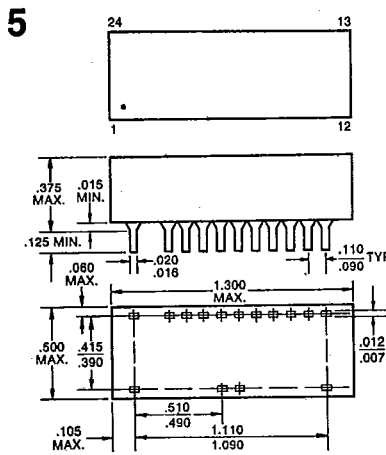
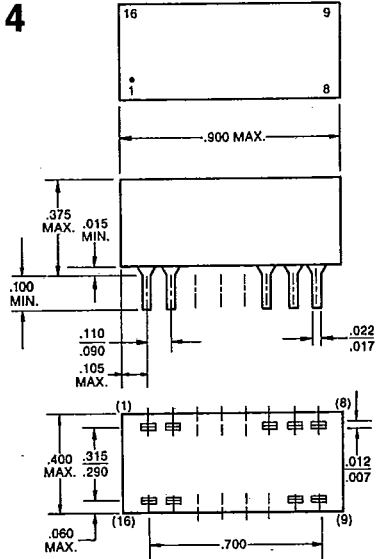
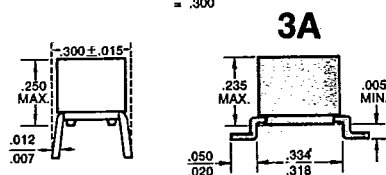
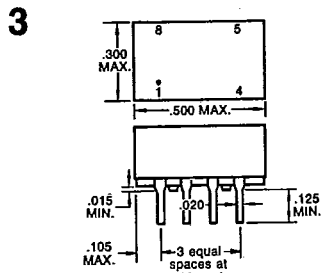
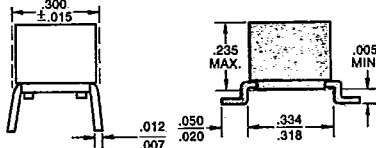
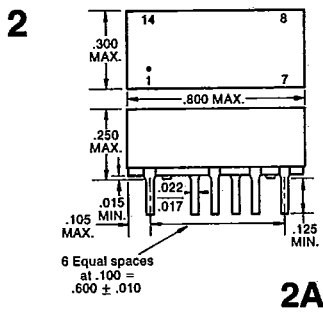
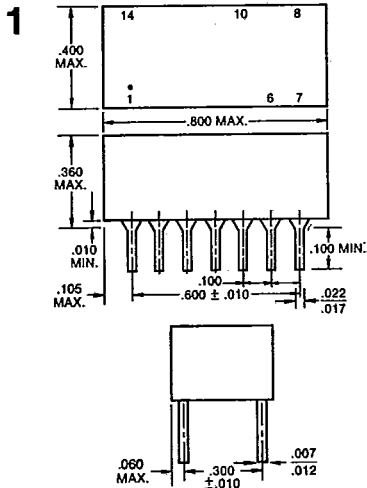
Delay characteristics $V_{ee} = -4.5V \pm .01V$ and $T_a @ 25^\circ C$.
 All delay times measured @ $-1.3V$ level with the output pulled down to $-2.0V$ with 50Ω .
 Rise time measured from 20 to 80% of output pulse.
 For proper operation minimum input pulse width should be 8 ns or 8 times step delay (W.I.G.) and repetition rate should be 2 times input pulse width.
 Input internally terminated; therefore the delay line driver does not require a pull-down resistor.

Numbers of the drawings below are referenced in the catalog at the locations describing specific modules. One drawing may be referenced by two, three, or more modules. Only the pins specified in the applicable schematic are provided with each package.

Pin numbers shown are for identification only, and are not necessarily marked on unit.

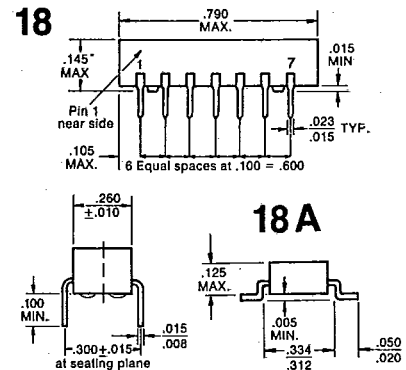
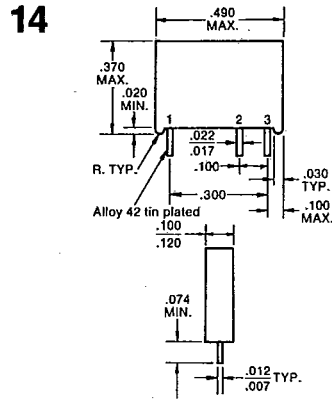
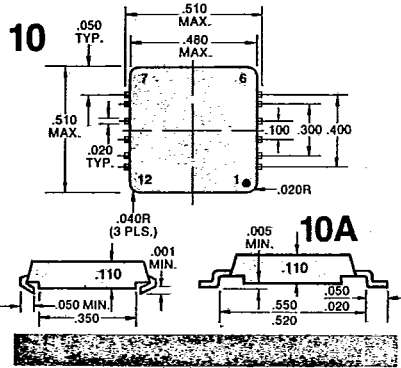
Dimensions

T-50-23

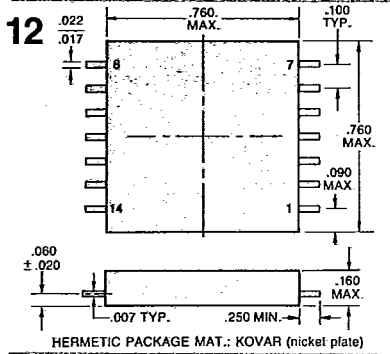
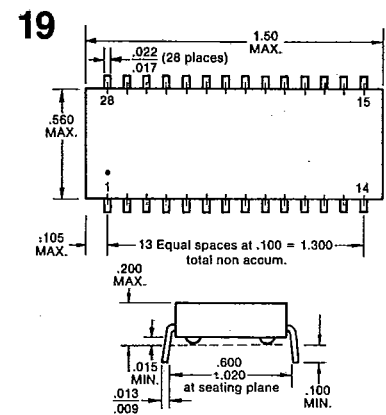
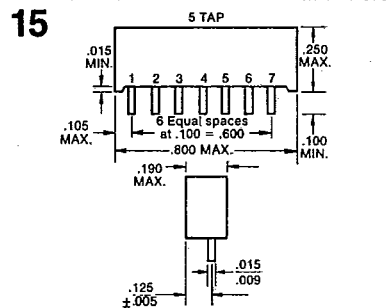
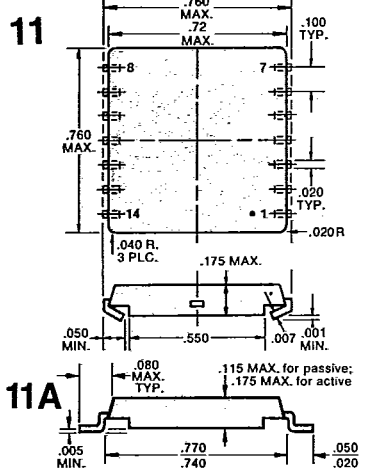


T-50-23

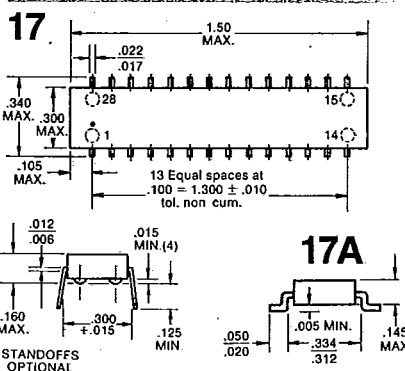
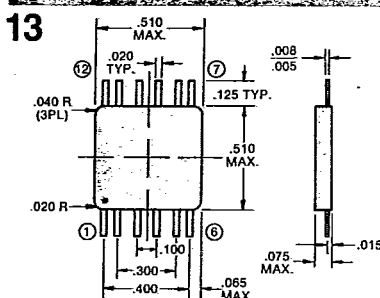
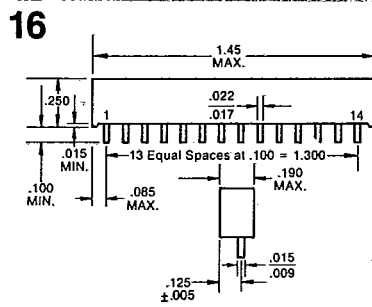
Surface-mount models are shown in shaded color.



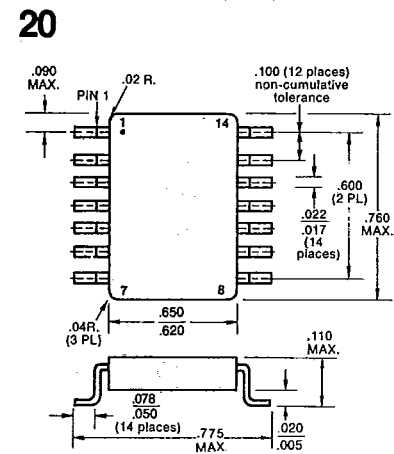
*For delays above 200 ns, height is .200 MAX.



HERMETIC PACKAGE MAT.: KOVAR (nickel plate)



STANDOFFS OPTIONAL



Can be used for ceramic-substrate applications.

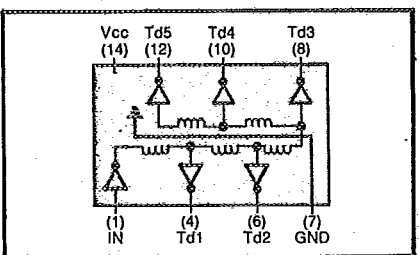
High-Performance 5-Tap TTL Delay Modules— $\frac{3}{4}$ " Sq.

Part No.	NANOSECONDS					All Taps (Max.)	
	T _D 1	T _D 2	T _D 3	T _D 4	T _D 5	T _R +	T _R -
CTTLDL025	5.0	10.0	15.0	20.0	25.0	2.0	2.0
CTTLDL050	10.0	20.0	30.0	40.0	50.0	2.0	2.0
CTTLDL075	15.0	30.0	45.0	60.0	75.0	2.0	2.0
CTTLDL100	20.0	40.0	60.0	80.0	100.0	2.0	5.0
CTTLDL125	25.0	50.0	75.0	100.0	125.0	2.0	5.0
CTTLDL150	30.0	60.0	90.0	120.0	150.0	2.0	6.0
CTTLDL200	40.0	80.0	120.0	160.0	200.0	2.0	7.0

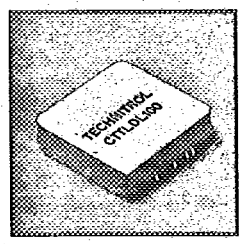
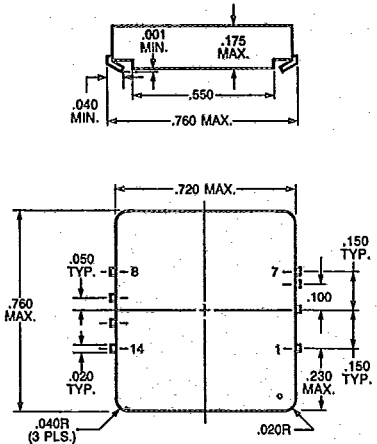
Delay Characteristics measured @ V_{CC} = 5.0V, 25°C no load.
 Delay Tolerance ±2 ns or 5% (whichever is greater).
 Minimum input-pulse width 20% of total delay.

High-Performance Surface-Mount TTL Delay Modules

Schematic and Pin-Out for CTTLDL



C-Lead CTTLDL



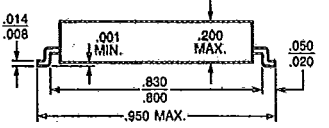
Actual Size

High-Performance Hermetic 5-Tap TTL Delay Modules— $\frac{3}{4}$ " Sq.

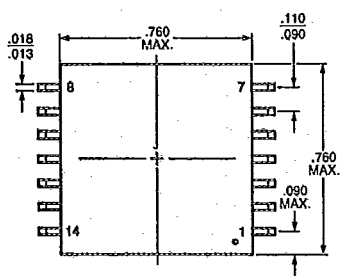
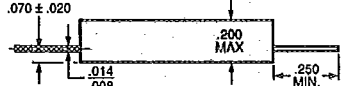
Part No.	Part No.	NANOSECONDS					All Taps (Max.)	
		T _D 1	T _D 2	T _D 3	T _D 4	T _D 5	T _R +	T _R -
GJTTLDL025	JTTLDL025	5.0	10.0	15.0	20.0	25.0	2.0	2.0
GJTTLDL050	JTTLDL050	10.0	20.0	30.0	40.0	50.0	2.0	2.0
GJTTLDL075	JTTLDL075	15.0	30.0	45.0	60.0	75.0	2.0	2.0
GJTTLDL100	JTTLDL100	20.0	40.0	60.0	80.0	100.0	2.0	5.0
GJTTLDL125	JTTLDL125	25.0	50.0	75.0	100.0	125.0	2.0	6.0
GJTTLDL150	JTTLDL150	30.0	60.0	90.0	120.0	150.0	2.0	7.0
GJTTLDL200	JTTLDL200	40.0	80.0	120.0	160.0	200.0	2.0	8.0

Delay Characteristics measured @ V_{CC} = 5.0V, 25°C no load.
 Delay Tolerance ±2 ns or 5% (whichever is greater).
 Minimum input-pulse width 40% of total delay.

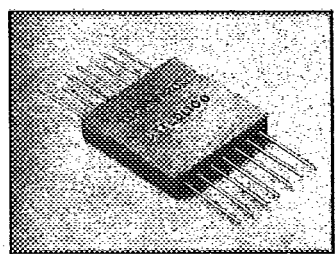
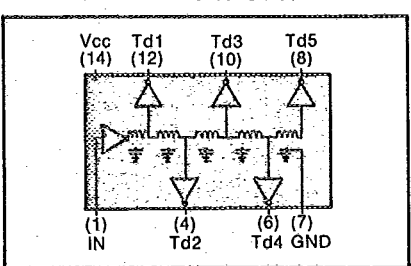
Hermetic Gull Wing GJTTLDL



Hermetic Flat-Pack JTTLDL



Schematic and Pin-Out for GJTTLDL and JTTLDL



Actual Size

Lead material: electro tin plated (alloy 42)
 Note: Pin numbers shown are for reference only and not necessarily marked on unit.

Technitrol

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