High-Performance Processors

AltiVec™ Technology

Overview

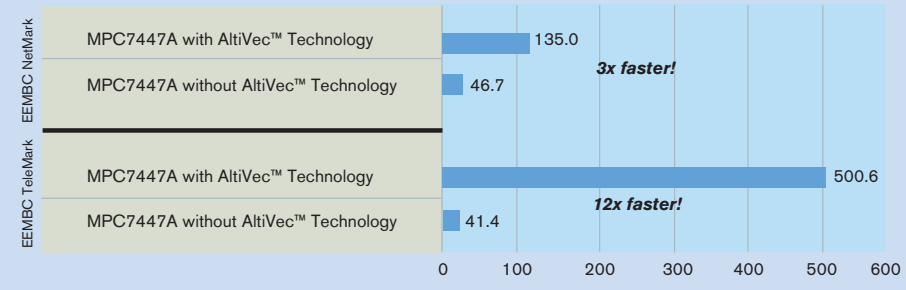
Freescale Semiconductor's advanced AltiVec™ technology is designed to enable exceptional general-purpose processing power for high-performance PowerPC® processors in embedded computing and communications applications. This leading-edge technology is engineered to support high-bandwidth data processing and algorithmic-intensive computations, all in a single-chip solution. AltiVec technology has proven itself to be a leader in enabling high performance, with continued "best-in-class" performance ratings from the Embedded Microprocessor Benchmark Consortium (EEMBC®), an organization of semiconductor, compiler and RTOS vendors.

AltiVec technology offers a programmable solution that can be adapted to changing standards and customer requirements for protecting technology investments.

The preferred programming environment is the C and C++ languages favored by embedded systems developers, and Freescale is working with leading tool providers to develop simulators, assemblers, linkers and compilers to help provide full support for the AltiVec technology. In addition, numerous software libraries are available to help jump-start software development using the AltiVec technology.

AltiVec technology is engineered to bring exceptional power to applications such as telecommunications switches, IP telephony gateways, speech processing systems, image and video processing systems, virtual private network servers, high-resolution 3-D graphics and more. With its DSP-like computing power, AltiVec technology also enables high-performance PowerPC processors to address markets and applications in which performance must be balanced with power consumption, system cost and peripheral integration.

EEMBC® PERFORMANCE BENCHMARKS



The Results Are In: Performance Benchmarks with AltiVec Technology

EEMBC develops meaningful performance benchmarks for the hardware and software used in embedded systems. Through the combined efforts of its members, EEMBC benchmarks have become an industry standard for evaluating the capabilities of embedded processors, compilers, and Java™ language implementations according to objective, clearly defined, application-based criteria.

Freescale Semiconductor's* family of high-performance PowerPC® processors are frequently and rigorously put through EEMBC benchmark certification tests. The graph shows performance improvements when processors are tested out-of-the-box versus when they are tested with AltiVec technology optimizations for telecommunications and networking applications. Telecommunications tests cover autocorrelation, bit allocation, convolutional encoder, Fast Fourier Transform (FFT) and Viterbi decoder. Networking tests cover packet flow, route lookup and Open Shortest Path First (OSPF) protocol.

Launched by Motorola

freescale semiconductor

What Is AltiVec Technology?

Freescale's AltiVec technology is a powerful tool for software developers who want to add efficiency and speed to their applications. Starting with the e600 PowerPC core (also known as the G4), a 128-bit vector execution unit was added to the architecture. This engine operates concurrently with the existing integer and floating-point units and enables highly parallel operations—up to 16 operations in a single clock cycle. By leveraging AltiVec technology, developers can see dramatic acceleration in performance-driven, high-bandwidth computing and communications applications.

AltiVec technology uses a separate register file containing 32 entries—each of which is 128 bits wide. Each value within an AltiVec register is a vector that is made up of elements. AltiVec instructions perform simultaneous operations on all elements within an AltiVec vector register. This is often referred to as SIMD (Single Instruction Multiple Data) parallel processing. Depending on data size, vectors are 4, 8 or 16 elements long. There is virtually no performance penalty for mingling integer, FPU and AltiVec technology operations.

AltiVec technology is an extension to the PowerPC instruction set, adding 162 new "vector" instructions. A set of useful operations such as sum-across (sums all the elements in a vector) and multiply-sum (multiplies and sums elements in three vectors) have been added. In addition, data manipulation instructions have been augmented to include operations such as permute (fills a register with bytes from two other registers), merge (merges two vectors into one), and "splat" (duplicates data across elements in a vector). The AltiVec instructions have one, two or three source operands and are non-destructive in nature.

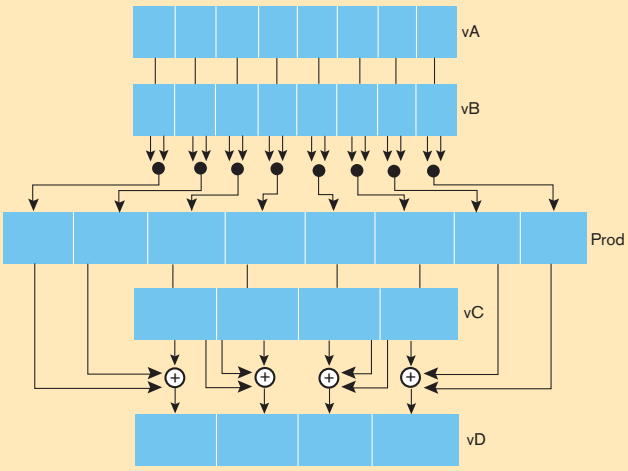
Other advantages provided by the AltiVec instructions include:

> Fully pipelined with single-cycle throughput
- Simple ops: 1 cycle latency
- Compound ops: 3–4 cycle latency
- No restriction on issue with scalar instructions

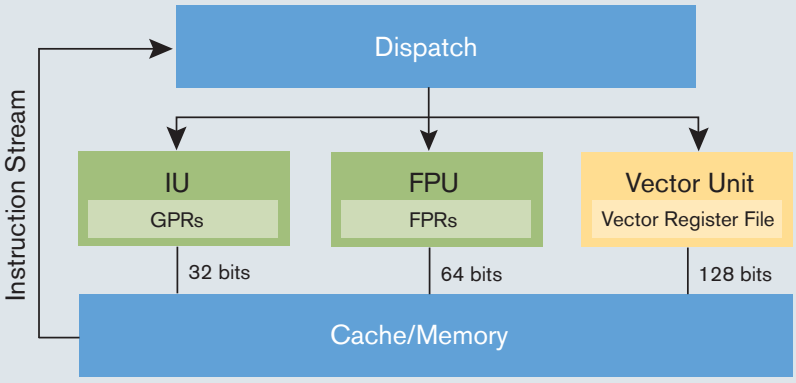
> Enhanced cache/memory interface
- Software hints for data reuse probability
- Prefetch support (stride-N access)

> Simplified load/store architecture
- Simple byte, halfword, word and quadword loads and stores
- Virtually no unaligned accesses—software managed via permute instruction

ALTIVEC EXECUTION OF MULTIPLY-ACCUMULATE



ALTIVEC VECTOR UNIT BLOCK DIAGRAM



Familiar, Supported Programming Environment

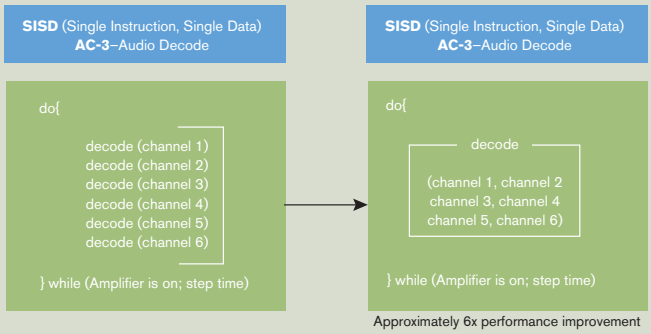
Because AltiVec technology is based on the C programming model, developers may leverage their experience with C, C++ or Obj C to easily take advantage of the benefits that the AltiVec technology has to offer. Standard C programs should compile without modification on C compilers with the AltiVec C Programming Model enabled. New functions and data structures that use the AltiVec technology may be added and used just like other functions and data structures.

Software developers can quickly see performance gains in existing applications by using AltiVec technology. AltiVec technology generally works best for that 10 percent of the application that consumes 80 percent of CPU time; these functions typically have heavy computational and data loads, two areas where AltiVec technology excels.

To identify the functions that are not meeting the performance requirements of the application, software vendors such as Green Hills, Metrowerks and Wind River Systems offer profiling tools designed to enable developers to identify performance bottlenecks that could be alleviated with AltiVec technology.

To help developers more quickly realize the performance benefits of AltiVec technology, Freescale offers downloadable libraries of AltiVec technology-enabled functions. To take advantage of AltiVec technology, an application must be reprogrammed or at least recompiled; however, developers do not need to rewrite the entire application. Application notes and documentation are also provided to help developers start a new application using AltiVec technology.

SAMPLE-BASED PROCESSING



Approximately 6x performance improvement

Without the power of AltiVec technology, the code may have to call a routine six times to perform the same operation on multiple pieces of data. With AltiVec technology, the routine may be run only once on all six sections of data simultaneously.

ALTIVEC LIBRARIES

Application/Category	Libraries Available (Please check the Web site for an updated list of available libraries.)
Telecommunications	> Fixed-Point and Floating Point Fourier Transform (FFT) Megafunction
	> Complex, Real, and Real Delayed Least Mean Squared (LMS) Finite Impulse Response (FIR) Functions
	> Autocorrelation
	> Global System for Mobile Communications (GSM) Convolution Encoder
	> GSM/3G Viterbi Decoder
	> Error Correction Codes (Cyclic Redundancy Check 8,12,16,24)
Networking	> Open Shortest Path First (OSPF)
	> Transmission Control Protocol/Internet Protocol (TCP/IP)
	> Encryption Protocols (AES, DES, 3DES, MD5)
Multimedia	> 2D Discrete Cosine Transform (DCT)
	> 2D Inverse Discrete Cosine Transform (IDCT)
	> MPEG-2 (Moving Picture Experts Group)
	> MPEG-1 Audio Layer-3 (MP3)
	> JPEG (Joint Photographic Experts Group)
	> Quantization
	> Dequantization
	> Sum of Absolute Differences (SAD)
Print/Imaging	> Ghostscript® Library Elements
	> Color Conversion (RGB to YCbCr)
	> FS Dithering
Link-level Libraries (LibC)	> Link-level Support for Standard C Functions (memcpy, strcmp etc.)
Mathematical Primatives	> Log, Exp, Sin, Cos, Log, Sqrt
Operating System Enablement	> Linux (TCP/IP)
	> VxWorks® Elements

Performance Hot Spots for AltiVec Technology

With its high-performance and ease-of-use software environment, AltiVec technology offers a single-chip solution to many common embedded computing challenges. AltiVec technology may be used to improve performance in the following areas:

> High-bandwidth data communications

> Packet data processing

> Image and video processing

> Access concentrators/DSLAMs

- ADSL and digital data concentrators

> Speech recognition

> Voice/sound processing

> Array numeric processing

> Basestation processing

> Real-time continuous speech I/O

- HMM, Viterbi acceleration, neural algorithms

> 3-D graphics

- Games, entertainment
- High-precision CAD

> Virtual reality

> Motion video

- MPEG-2, MPEG-4
- H.234

> High-fidelity audio

- 3-D audio, AC-3, MP3

> Machine intelligence

AltiVec Technology Features

> SIMD functionality for embedded applications with massive data processing needs

- 128-bit vector execution unit with 32-entry,128-bit register file
- Parallel processing with vector permute unit and vector arithmetic logical unit
- 162 additional instructions
- Advanced data types, such as packed byte, halfword and word integers, and packed IEEE® single-precision floats
- Saturation arithmetic

> Simplified architecture

- Virtually no interrupts other than data storage interrupt on loads and stores
- Allows hardware unaligned access support
- Virtually no penalty for running AltiVec and standard PowerPC instructions simultaneously
- Streamlined architecture to facilitate efficient implementation

> Maintains PowerPC ISA's RISC register-to-register programming model

> Supports parallel operation on byte, halfword, word and 128-bit operands

- Intra- and interelement arithmetic instructions
- Intra- and interelement conditional instructions
- Powerful permute, shift and rotate instructions

> Vector integer and floating-point arithmetic

- Data types
- 8-, 16- and 32-bit signed and unsigned integer data types
- 32-bit IEEE single-precision floating-point data type
- 8-, 16- and 32-bit Boolean data types (e.g., OxFFFF = 16-bit TRUE)
- Modulo and saturation integer arithmetic
- 32-bit "IEEE-default" single-precision floating-point arithmetic
- IEEE-default exception handling
- IEEE-default "round-to-nearest"
- Fast non-IEEE mode (e.g., denorms flushed to zero)

> Control flow with highly flexible bit manipulation engine

- Compare creates field mask used by select function
- Compare RC bit enables setting Condition Register
  - › Trivial accept/reject in 3-D graphics
  - › Exception detection via software polling
  - › Available library

Learn More: For more information about Freescale products, please visit **www.freescale.com**.

ALTIVECGLANCE
REV 4

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