# SRAM MODULE

## AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-95595: AS8S128K32
- SMD 5962-93187: AS8S128K32
- SMD 5962-98600: AS7S128K32
- MIL-STD-883

## FEATURES

- Access times of 20, 25, 35, 45 ns
- Built in decoupling caps for low noise operation
- Organized as 128K x32; User configured as 256Kx16 or 512K x8
- Operation with single 5 volt supply
- Low power CMOS
- TTL Compatible Inputs and Outputs
- 2V Data Retention, Low power standby

## OPTIONS MARKINGS

- Timing
  - 20ns -20
  - 25ns -25
  - 35ns -35
  - 45ns -45
- Data Retention, Low power standby L
- Package
  - Ceramic Quad Flatpack No. 704
  - Pin Grid Array -8 Series P No. 802
  - Pin Grid Array -8 Series PN No. 802
  - Pin Grid Array -7 Series P No. 803

**NOTE**: PN indicates a no connect on pins 8, 21, 28, 39

## GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS7S128K32 and AS8S128K32 are 4 Megabit CMOS SRAM Modules organized as 128Kx32-bits and user configurable to 256Kx16 or 512Kx8. The AS7S128K32 and AS8S128K32 achieve high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

The military temperature grade product is suited for military applications.

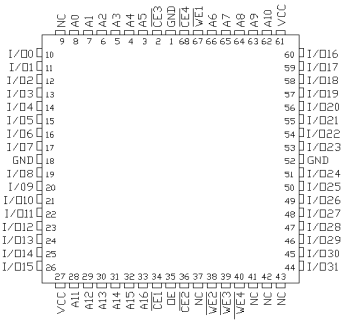
The AS8S128K32 (SMD 5962-95595) module is a single cavity, ceramic quad flatpack. This module makes use of a multi-chip design, has a low profile that reduces height requirements for board assembly.

The AS8S128K32 (SMD 5962-93187) module is a pin grid array substrate with a height of 0.255 inch (max). This module employs a multi-chip design. This compact layout reduces height requirements for board assembly to a minimum, and is pin compatible with SMD 5962-98600.

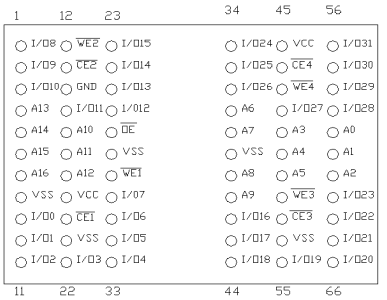
The AS7S128K32 (SMD 5962-98600) module is constructed using a 1.076-inch square ceramic pin grid array substrate. This compact layout reduces space requirements for board assembly to a minimum, and is pin compatible with SMD 5962-93187

## PIN ASSIGNMENT (Top View)

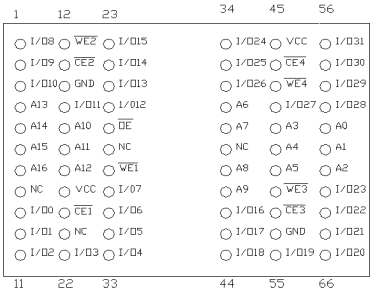
68 Lead CQFP

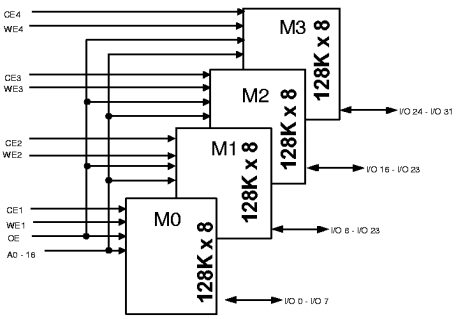



66 Lead PGA- Pins 8, 21, 28, 39 are grounds (P)




66 Lead PGA- Pins 8, 21, 28, 39 are no connects (PN)



## ABSOLUTE MAXIMUM RATINGS*

Voltage of Vcc Supply Relative to Vss.....-1V to +7V
Storage Temperature.....-55°C to +150°C
Short Circuit Output Current(per I/O).....20mA
Voltage on Any Pin Relative to Vss.....-.5V to Vcc+1V
Junction Temperature**.....+175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

This is a stress rating only and functional operation on the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this datasheet for more information.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C≤TA≤125°C; Vcc = 5v ±10%)

| DESCRIPTION | CONDITIONS | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Input High (logic 1) Voltage | | $V_{IH}$ | 2.2 | VCC+.5 | V | 1 |
| Input Low (logic 0) Voltage | | $V_{IL}$ | -0.5 | 0.8 | V | 1,2 |
| Input Leakage Current $_{ADD,OE}$ | $0V < V_{IN} < V_{CC}$ | $I_{L1}$ | -20 | 20 | µA | |
| Input Leakage Current $_{WE, CE}$ | $0V < V_{IN} < V_{CC}$ | $I_{L2}$ | -5 | 5 | µA | |
| Output Leakage Current $_{I/O}$ | Output(s) Disabled $0V < V_{OUT} < V_{CC}$ | $I_{LO}$ | -5 | 5 | µA | |
| Output High Voltage | $I_{OH}$ = -4.0mA | $V_{OH}$ | 2.4 | | V | 1 |
| Output Low Voltage | $I_{OL}$ = 8.0mA | $V_{OL}$ | | 0.4 | V | 1 |
| Supply Voltage | | $V_{CC}$ | 4.5 | 5.5 | V | 1 |

| | | | MAX | | | | | |
|---|---|---|---|---|---|---|---|---|
| DESCRIPTION | CONDITIONS | SYMBOL | -20 | -25 | -35 | -45 | UNITS | NOTES |
| Power Supply Current: Operating | CE\ ≤ $V_{IL}$; $V_{CC}$ = MAX f = MAX = 1/ $t_{RC}$(MIN) OUTPUTS OPEN | $I_{CC}$ | 620 | 560 | 520 | 500 | mA | 3,13 |
| Power Supply Current: Standby | CE\ ≥ $V_{IH}$; $V_{CC}$ = MAX f = MAX = 1/ t RC(MIN) OUTPUTS OPEN | $I_{SBT1}$ | 200 | 180 | 160 | 150 | mA | |
| | CE\ ≥ VIH; All Other Inputs ≤ VIL or ≥ VIH; VCC = MAX f = 0 Hz | $I_{SBT2}$ | 100 | 100 | 100 | 100 | mA | |
| | CE\ ≥ $V_{CC}$ -0.2V; $V_{CC}$ = MAX $V_{IL}$ ≤ $V_{SS}$ +0.2V; $V_{IH}$ ≥ $V_{CC}$ -0.2V; f = 0 Hz | $I_{SBC1}$ | 40 | 40 | 40 | 40 | mA | 13 |
| | "L" Version Only | $I_{SBC2}$ | 24 | 24 | 24 | 24 | mA | 13 |

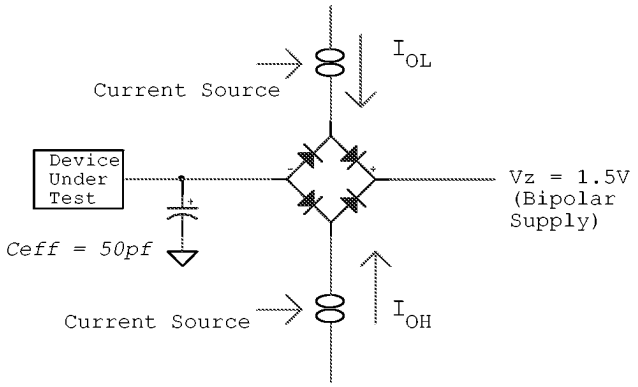
## CAPACITANCE TABLE

$V_{IN}$ = 0V, f = 1MHz, $T_A$ =25ºC

| SYMBOL | PARAMETER | MAXIMUM | UNITS | NOTES |
|---|---|---|---|---|
| $C_{ADD}$ | A0-A18 Capacitance | 40 | pF | 4 |
| $C_{OE}$ | OE\ Capacitance | 40 | pF | 4 |
| $C_{WE}$, $C_{CE}$ | WE\ and CE\ Capactiance | 8 | pF | 4 |
| $C_{IO}$ | I/O 0 - I/O 31 Capactiance | 8 | pF | 4 |

| TRUTH TABLE | | | | | |
|---|---|---|---|---|---|
| MODE | OE\ | CE\ | WE\ | I/O | POWER |
| Read | L | L | H | Q | ACTIVE |
| Write | X | L | L | D | ACTIVE |
| Standby | X | H | X | HIGH Z | STANDBY |
| Not Selected | H | L | H | HIGH Z | ACTIVE |

## AC TEST CONDITIONS




**Test Specifications**

Input pulse levels.....VSS to 3V
Input rise and fall times.....5ns
Input timing reference levels.....1.5V
Output reference levels.....1.5V
Output load.....See Figures 1 and 2

**Notes:**

Vz is programable from -2V to + 7V.
$I_{OL}$ and $I_{OH}$ programmable from 0 to 16 mA.
Vz is typically the midpoint of $V_{OH}$ and $V_{OL}$.
$I_{OL}$ and $I_{OH}$ are adjusted to simulate a typical resistive load circuit.

## ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C≤TA≤125°C; Vcc = 5v ±10%)

| DESCRIPTION | SYMBOL | -20 | | -25 | | -35 | | -45 | | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| READ Cycle | | | | | | | | | | | |
| READ Cycle time | $t_{RC}$ | 20 | | 25 | | 30 | | 45 | | ns | |
| Address access time | $t_{AA}$ | | 20 | | 25 | | 35 | | 45 | ns | |
| Chip Enable access time | $t_{ACE}$ | | 20 | | 25 | | 35 | | 45 | ns | |
| Output hold from address change | $t_{OH}$ | 3 | | 3 | | 3 | | 3 | | ns | |
| Chip Enable to output in Low Z | $t_{LZCE}$ | 3 | | 3 | | 3 | | 3 | | ns | 4,6,7 |
| Chip Disable to output in High Z | $t_{HZCE}$ | | 9 | | 10 | | 14 | | 15 | ns | 4,6,7 |
| Chip Enable to power-up time | $t_{PU}$ | 0 | | 0 | | 0 | | 0 | | ns | 4 |
| Chip Disable to power-down time | $t_{PD}$ | | 20 | | 25 | | 35 | | 45 | ns | 4 |
| Output Enable access time | $t_{AOE}$ | | 7 | | 8 | | 12 | | 12 | ns | |
| Output Enable output in Low Z | $t_{LZOE}$ | 0 | | 0 | | 0 | | 0 | | ns | 4,6 |
| Output Disable to output in High Z | $t_{HZOE}$ | | 7 | | 9 | | 12 | | 12 | ns | 4,6,7 |
| WRITE Cycle | | | | | | | | | | | |
| WRITE Cycle time | $t_{WC}$ | 20 | | 25 | | 35 | | 45 | | ns | |
| Chip Enable to end of write | $t_{CW}$ | 15 | | 17 | | 20 | | 22 | | ns | |
| Address valid to end of write | $t_{AW}$ | 15 | | 17 | | 20 | | 22 | | ns | |
| Address setup time | $t_{AS}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Address hold from end of write | $t_{AH}$ | 0 | | 0 | | 0 | | 0 | | ns | |
| Write Pulse Width | $t_{WP1}$ | 15 | | 17 | | 20 | | 20 | | ns | |
| Write Pulse Width | $t_{WP2}$ | 15 | | 17 | | 20 | | 20 | | ns | |
| Data setup time | $t_{DS}$ | 10 | | 12 | | 15 | | 15 | | ns | |
| Data hold time | $t_{DH}$ | 1 | | 1 | | 1 | | 1 | | ns | |
| Write Disable to output in Low Z | $t_{LZWE}$ | 3 | | 3 | | 3 | | 3 | | ns | 4,6,7 |
| Write Enable to output in High Z | $t_{HZWE}$ | | 10 | | 11 | | 14 | | 15 | ns | 4,6,7 |

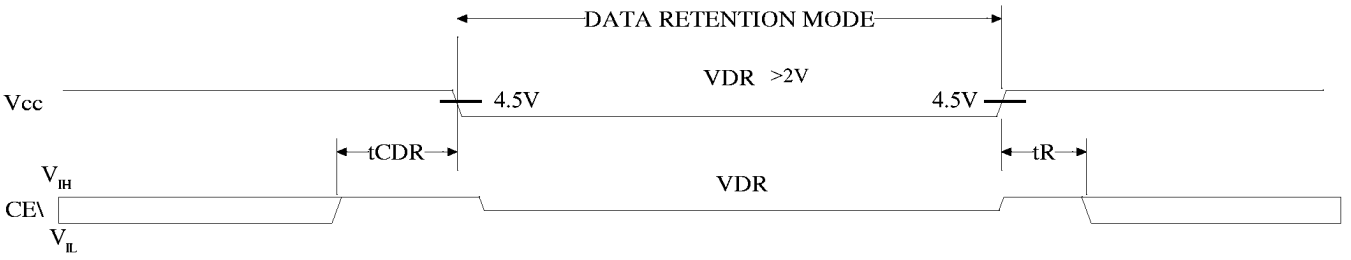
## NOTES

1. All voltages referenced to $V_{SS}$ (GND).
2. -3v for pulse width <20ns.
3. ICC is dependent on output loading and cycle rates. The specified value applies with the outputs open, and f= $\frac{1}{t_{RC(MIN)}}$ Hz.
4. This parameter is sampled.
5. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
6. $t_{HZCE}$, $t_{HZOE}$ and $t_{HZWE}$ are specified with $C_L$= 5pF as in Fig. 2. Transition is measured +/- 500 mV typical from steady state coltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, $t_{HZCE}$, is less than $t_{LZCE}$, and $t_{HZWE}$ is less than $t_{HZWE}$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enable are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. $t_{RC}$ = READ cycle time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.
13. 32 bit operation

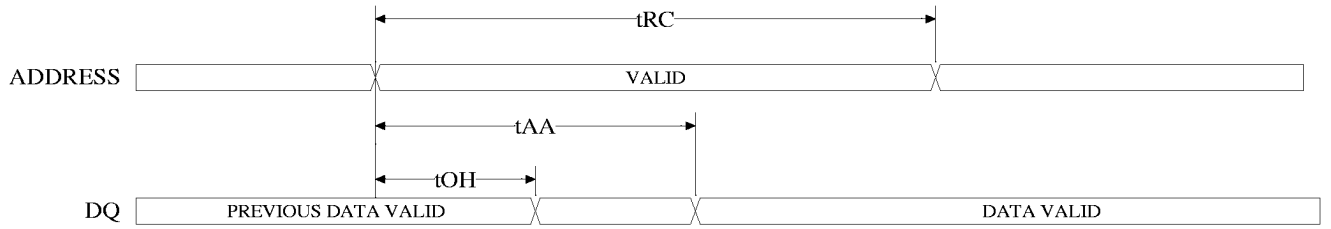
## DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

| DESCRIPTION | CONDITIONS | | SYMBOL | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ for Rerention Data | | | $V_{DR}$ | 2 | | V | |
| Data Retention Current | CE\ ≥ $V_{CC}$ - 0.2 V | $V_{CC}$ = 2.0V | $I_{CCDR}$ | | 5 | mA | |
| | $V_{IN}$ ≥ $V_{CC}$ - 0.2 V | $V_{CC}$ = 3.0V | $I_{CCDR}$ | | 12 | mA | |
| Chip Deselect to Data Retention Time | | | $t_{CDR}$ | 2 | | ns | 4 |
| Operation Recovery Time | | | $t_R$ | $t_{RC}$ | | ns | 4,11 |

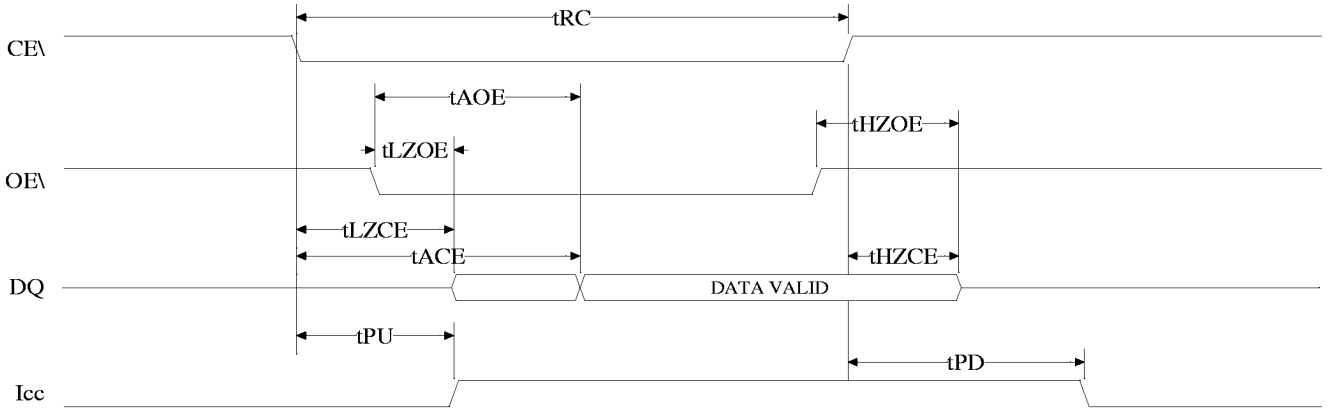
## LOW $V_{CC}$ DATA RETENTION WAVEFORM



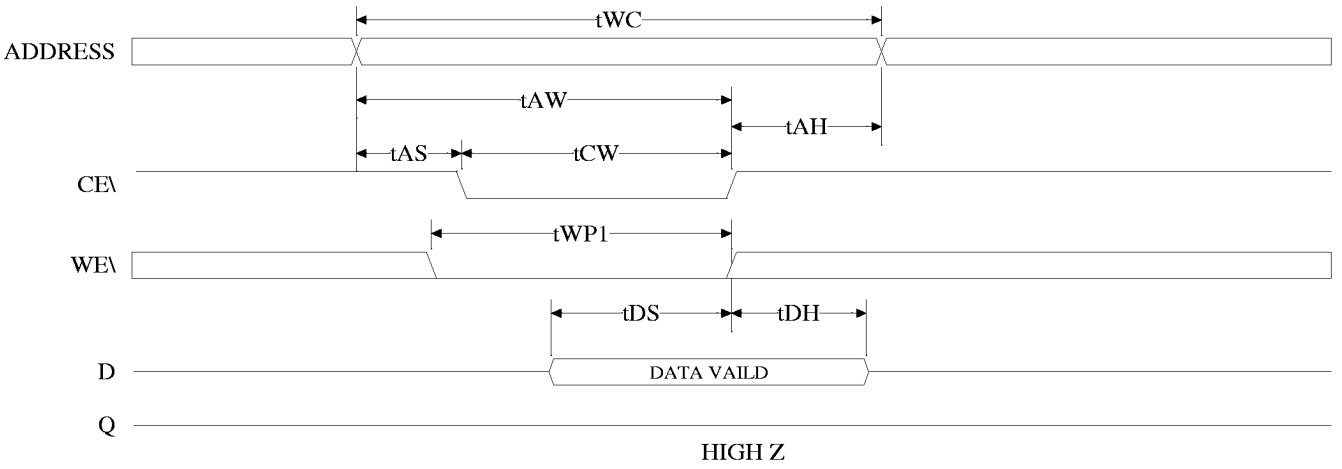
## READ CYCLE NO. 1[8,9]



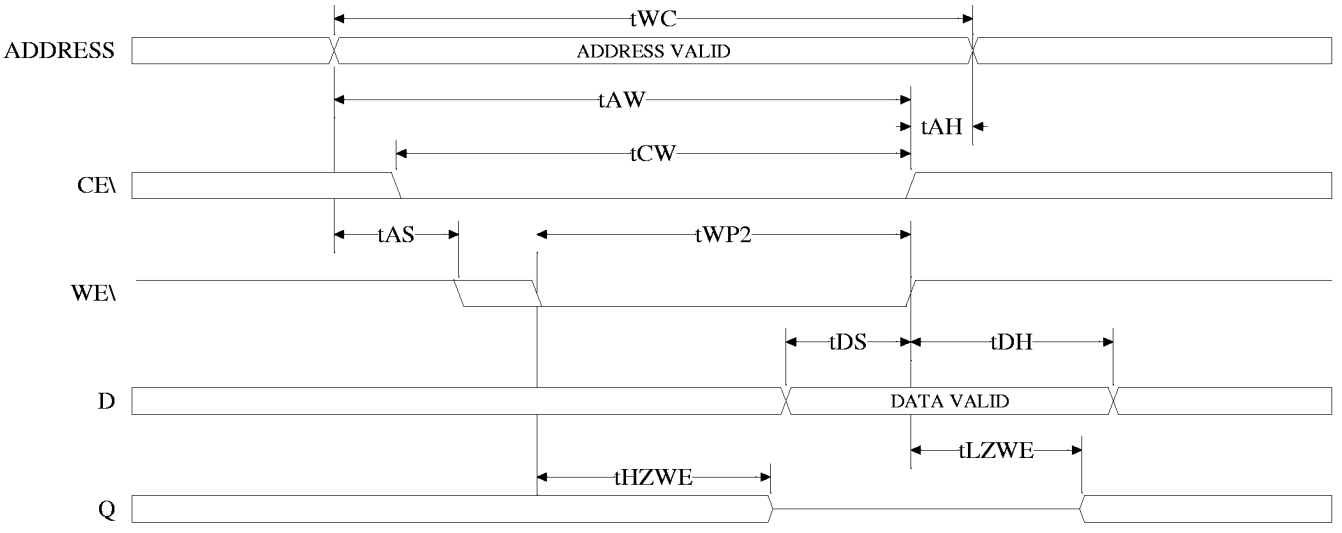

## READ CYCLE NO. 2[7,8,10]



**WRITE CYCLE NO. 1**
(Chip Enable Controlled)

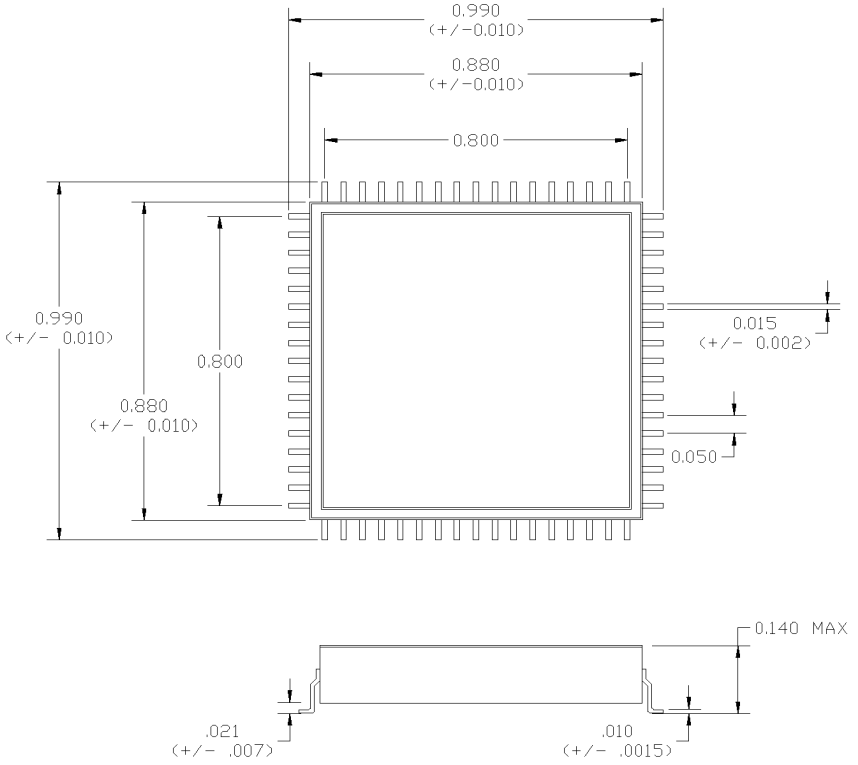



**WRITE CYCLE NO. 2**
(Write Enable Controlled)



## MECHANICAL DEFINITION

AS8S128K32



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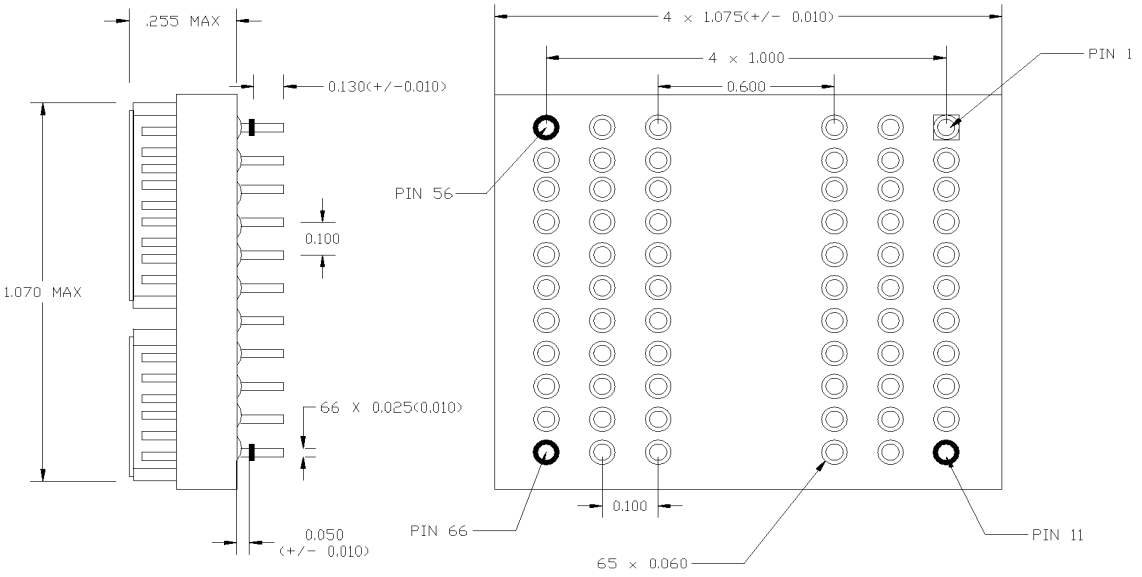


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