SRAM MODULE

AVAILABLE AS MILITARY SPECIFICATIONS

- SMD 5962-94611
- MIL-STD-883

FEATURES

- Operation with single 5V supply
- High speed: 20, 25 and 35ns
- Built in decoupling caps for low noise
- Organized as 512Kx32 , byte selectable
- Low power CMOS
- TTL Compatible Inputs and Outputs
- Theta JC =1.00°C/w
- **Future offerings**
  - 3.3V Power Supply
  - 15, 17 ns Ultra High Speed

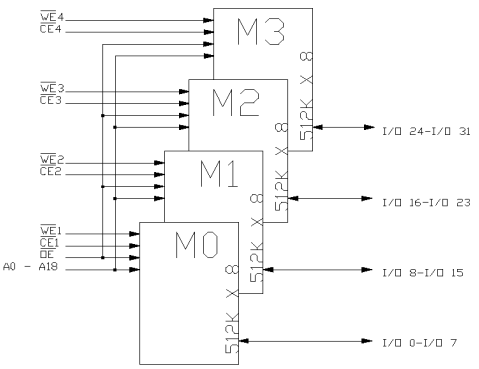
OPTIONS MARKINGS

- Timing
  - 20ns -20
  - 25ns -25
  - 35ns -35
- Package
  - Ceramic Quad Flatpack Q No.702
  - Pin Grid Array P No.802

GENERAL DESCRIPTION

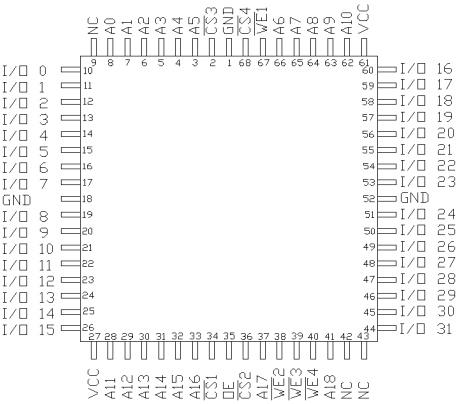
The Austin Semiconductor, Inc. AS8S512K32 is a 16 Megabit CMOS SRAM Module organized as 512Kx32 bits. The AS8S512K32 achieves high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

This military temperature grade product is ideally suited for military and space applications.

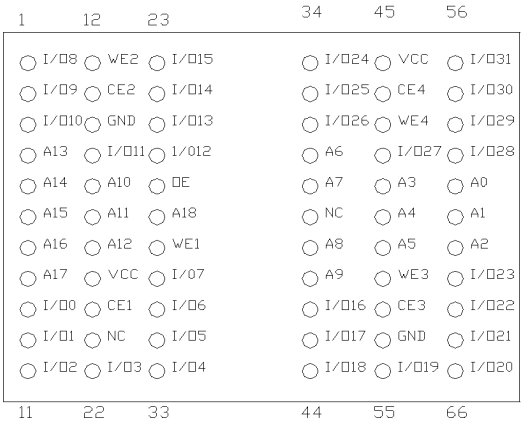


PIN ASSIGNMENT (Top View)

68 Lead CQFP



66 Lead PGA



TRUTH TABLE

MODE	OE\	CE\	WE\	I/O	POWER
Read	L	L	H	D_{OUT}	ACTIVE
Write(2)	X	L	L	D_{IN}	ACTIVE
Standby	X	H	X	High Z	STANDBY

ABSOLUTE MAXIMUM RATINGS*

Voltage of Vcc Supply Relative to Vss.....-.5V to +7V
Storage Temperature.....-55°C to +150°C
Short Circuit Output Current(per I/O).....20mA
Voltage on Any Pin Relative to Vss.....-.5V to Vcc+1V
Junction Temperature**.....+150°C
Power Dissapation.....3.6 W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation on the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this datasheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS
(-55°C ≤ T A ≤ 125°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (logic 1) Voltage		V_{IH}	2.2	V_{CC}+.5	V	1
Input Low (logic 1) Voltage		V_{IL}	-0.5	0.8	V	1,2
Input Leakage Current $_{ADD,OE}$	0V<V_{IN}<V_{CC}	I_{LI1}	-10	10	µA	
Input Leakage Current $_{WE, CE}$		I_{LI2}	-10	10	µA	
Output Leakage Current $_{I/O}$	Output(s) Disabled 0V<V_{OUT}<V_{CC}	ILO	-10	10	µA	
Output High Voltage	I_{OH} = 4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1

			MAX				
DESCRIPTION	CONDITIONS	SYMBOL	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	CE\ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/^{t}RC outputs open	I_{CC}	650	600	570	mA	3,13
Power Supply Current: Standby	CE\ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/^{t}RC outputs open	I_{SBT1}	240	190	190	mA	3,13
CMOS Standby	V_{IN}=V_{CC} - 0.2V, or V_{SS} + 0.2V V_{CC} -5.5V; f = 0Hz	I_{SBC}	80	80	80	mA	

Capacitance Note1,2

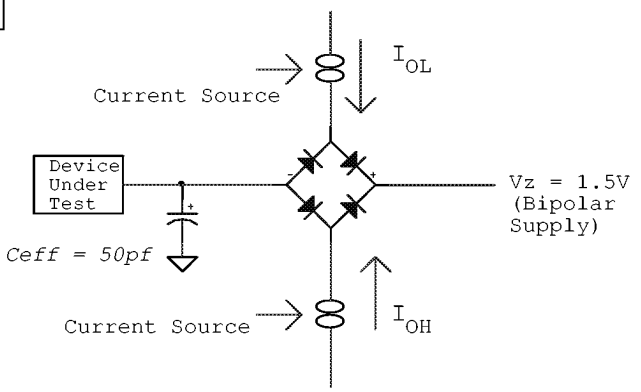
VIN=0V, f=MHz, TA=25 C

SYMBOL	PARAMETER	MAXIMUM	UNITS
C_{ADD}	A0 - A18 Capacitance	40	pF
C_{OE}	OE\ Capactiance	40	pF
C_{WE}, C_{CE}	WE\ and CE\ Capactiance	10	pF
C_{IO}	I/O0 - I/O 31 Capactiance	10	pF

Note:
1. This parameter is sampled.
2. 32 bit configuration.

AC TEST CONDITIONS

Test Specifications	
Input pulse levels	Vss to 3V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2



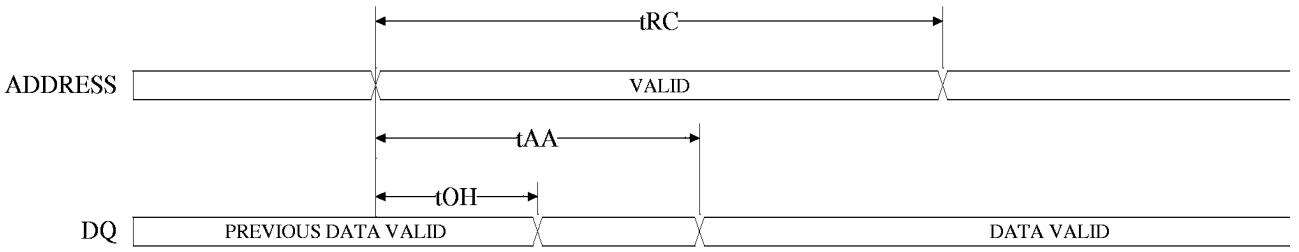
Notes:
Vz is programable from -2V to + 7V.
I_{OL} and I_{OH} programmable from 0 to 16 mA.
Vz is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} and I_{OH} are adjusted to simulate a typical resistive load circuit.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

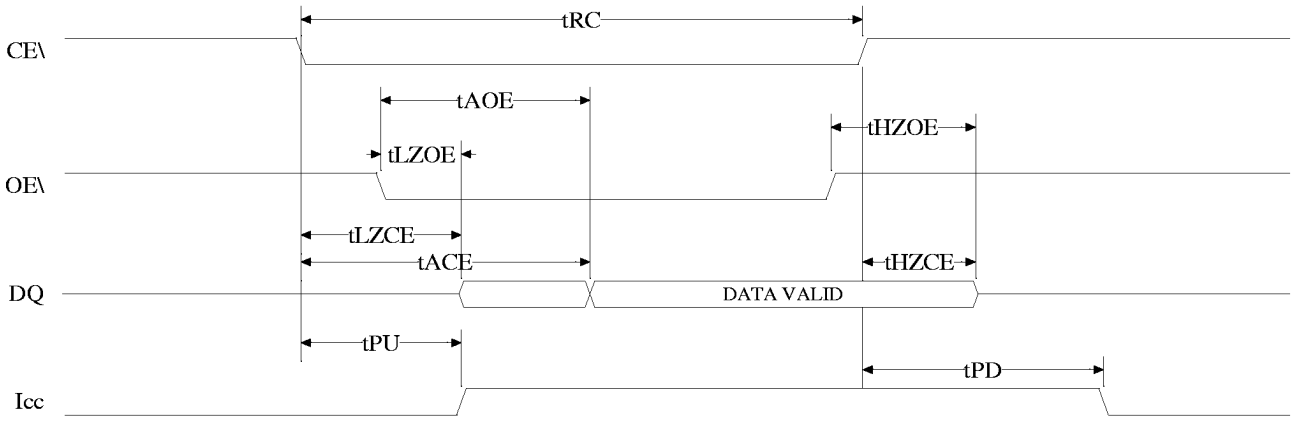
(Notes 5) ($-55°C \leq T_A \leq 125°C$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION		-20		-25		-35			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle									
READ cycle Time	^tRC	20		25		35		ns	
Address access time	^tAA		20		25		35	ns	
Chip Enable access time	^tACE		20		25		35	ns	
Output hold from address change	^tOH	2		2		2		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		ns	4,6,7
Chip disable to output in High-Z	^tHZCE		9		10		12	ns	4,6,7
Output Enable access time	^tAOE		8		10		12	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		ns	4,6
Output disable to output in High-Z	^tHZOE		9		10		12	ns	4,6
WRITE Cycle									
WRITE cycle time	^tWC	20		25		35		ns	
Chip Enable to end of write	^tCW	15		17		20		ns	
Address valid to end of write	^tAW	15		17		20		ns	
Address setup time	^tAS	1		1		1		ns	
Address hold from end of write	^tAH	1		1		1		ns	
WRITE pulse width	$^tWP1$	15		17		20		ns	
WRITE pulse width	$^tWP2$	15		17		20		ns	
Data setup time	^tDS	10		12		15		ns	
Data hold time	^tDH	0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	2		2		2		ns	4,6,7
Write Enable to output in High-Z	^tHZWE		10		12		15	ns	4,6,7

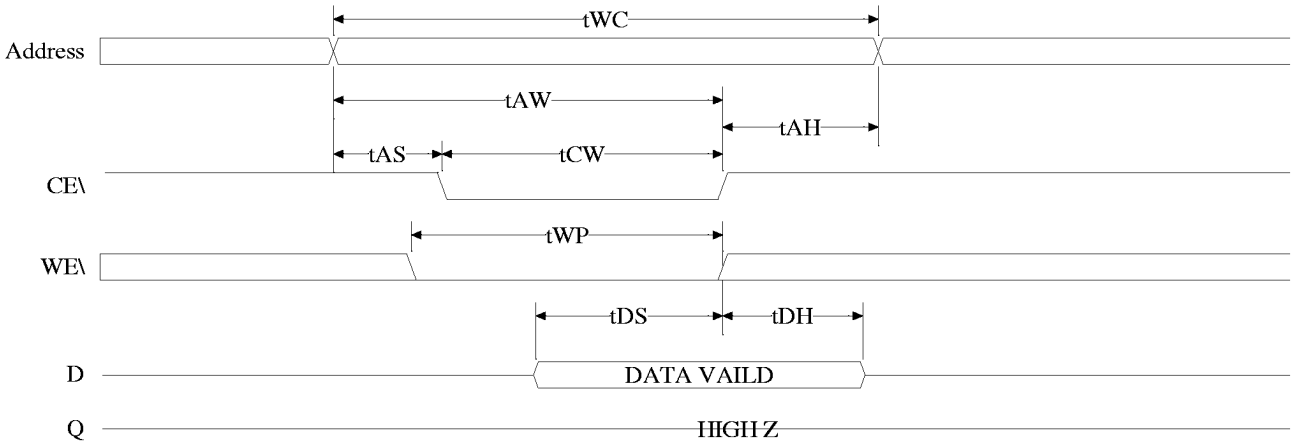
READ CYCLE NO. 1



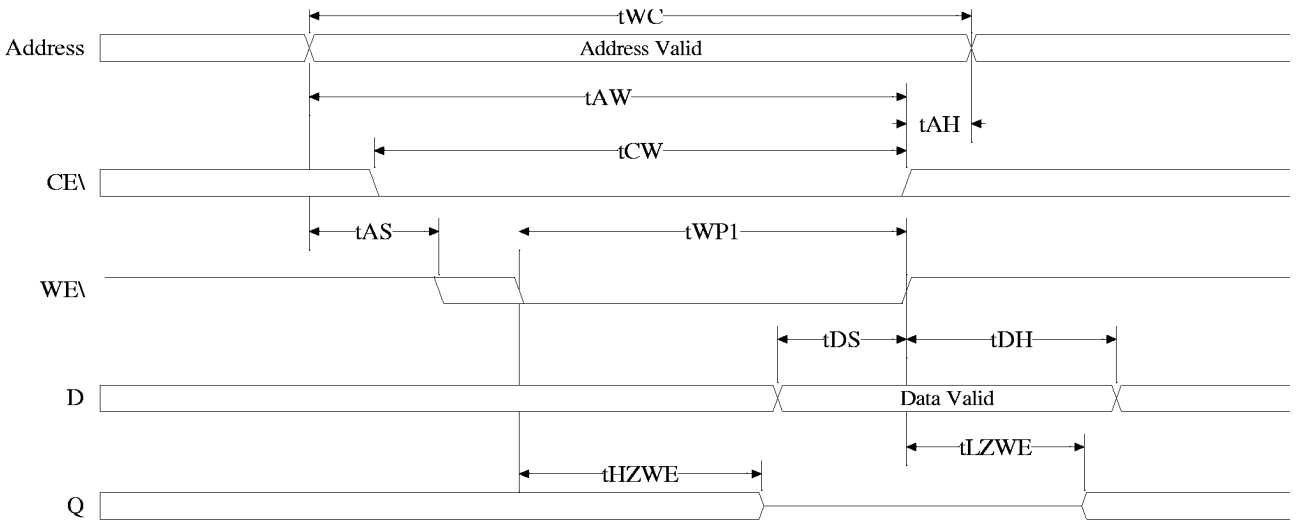
READ CYCLE NO. 2



WRITE CYCLE NO. 1
(Chip Enable Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled)

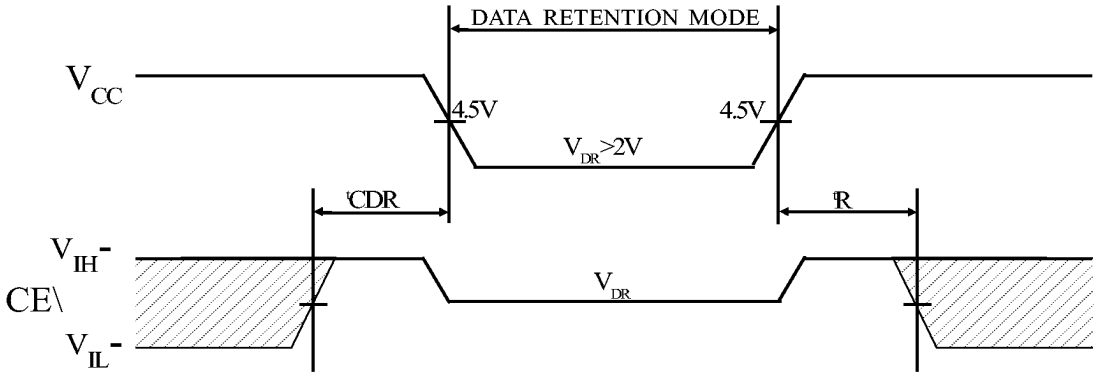


NOTES

1. All voltages referenced to V_{SS} (GND).
2. -2V for pulse width <20ns.
3. ICC is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and f= $\frac{1}{t_{RC(MIN)}}$ Hz.
4. This parameter guaranteedbut not tested.
5. Test conditions as specified with output loading as shown in Fig. 1 unless otherwise noted.
6. t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with C_L= 5pF as in Fig. 2. Transition is measured +/- 200 mV typical from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, t_{HZCE}, is less than t_{LZCE}, and t_{HZWE} is less than t_{HZWE}.
8. WE\ is HIGH for READ cycle.
9. Device is continuously selected. Chip enables and output enable are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. t_{RC}= READ cycle time.
12. Chip enable (CE\) and write enable (WE\) can initiate and terminate a WRITE cycle.
13. I_{CC} is for 32 bit mode.

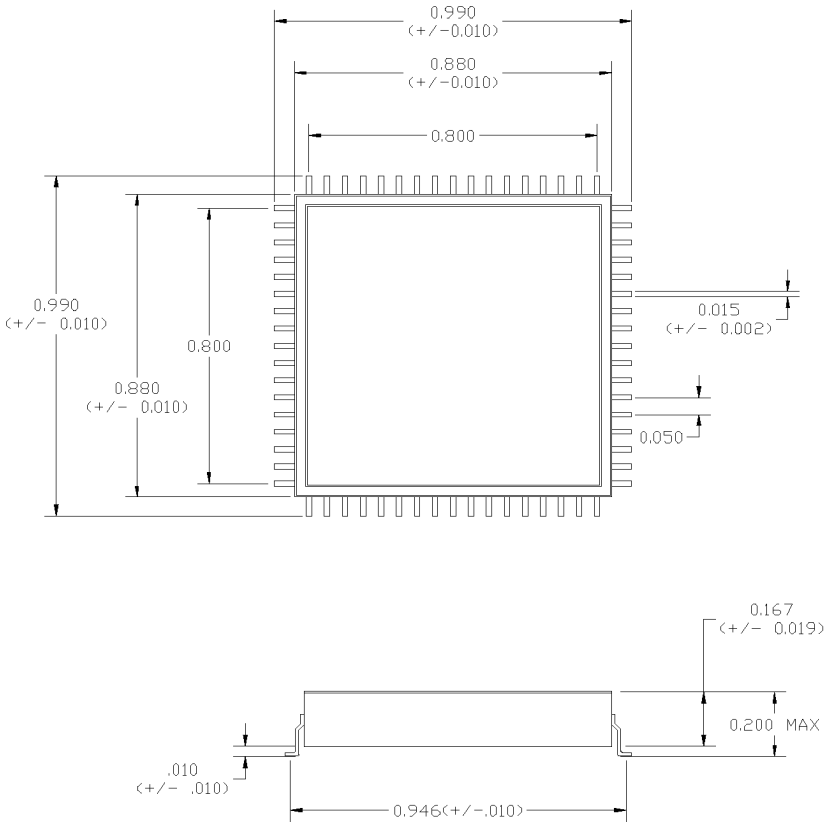
DESCRIPTION	CONDITIONS		SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data			V_{DR}	2		V	
Data Retention Current	CE\ ≥ V_{CC} - 0.2 V	V_{CC} = 2.0V	I_{CCDR}		20	mA	
	V_{IN} ≥ V_{CC} - 0.2 V	V_{CC} = 3.0V	I_{CCDR}		28	mA	
Chip Deselect to Data			t_{CDR}	0		ns	4
Retention Time							
Operation Recovery Time			t_R	t_{RC}		ns	4,11

LOW V_{CC} DATA RETENTION WAVEFORM



MECHANICAL DEFINITION

for the AS8S512K32Q Ceramic Quad Flat Pack



MECHANICAL DEFINITION
for the AS8S512K32P Pin Grid Array