



CTLT3820-M563

**SURFACE MOUNT
VERY LOW V_{CE(SAT)}
NPN SILICON TRANSISTOR**



Top View Bottom View

TLM563 CASE

- Device is *Halogen Free* by design

APPLICATIONS:

- DC/DC Converters
- Voltage Clamping
- Protection Circuits
- Battery powered Cell Phones, Pagers, Digital Cameras, PDAs, Laptops, etc.

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

Collector-Base Voltage	V_{CBO}	80	V
Collector-Emitter Voltage	V_{CEO}	60	V
Emitter-Base Voltage	V_{EBO}	5.0	V
Continuous Collector Current	I_C	1.0	A
Peak Collector Current	I_{CM}	2.0	A
Continuous Base Current	I_B	300	mA
Power Dissipation	P_D	500	mW
Operating and Storage Junction Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$
Thermal Resistance	Θ_{JA}	250	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{CBO}	$V_{CB}=60\text{V}$		100	nA
I_{EBO}	$V_{EB}=5.0\text{V}$		100	nA
BV_{CBO}	$I_C=100\mu\text{A}$	80		V
BV_{CEO}	$I_C=10\text{mA}$	60		V
BV_{EBO}	$I_E=100\mu\text{A}$	5.0		V
$V_{CE(SAT)}$	$I_C=100\text{mA}, I_B=1.0\text{mA}$		0.115	V
$V_{CE(SAT)}$	$I_C=500\text{mA}, I_B=50\text{mA}$		0.15	V
$V_{CE(SAT)}$	$I_C=1.0\text{A}, I_B=100\text{mA}$		0.28	V
$V_{BE(SAT)}$	$I_C=1.0\text{A}, I_B=50\text{mA}$		1.1	V
$V_{BE(ON)}$	$V_{CE}=5.0\text{V}, I_C=1.0\text{A}$		0.9	V
h_{FE}	$V_{CE}=5.0\text{V}, I_C=1.0\text{mA}$	200		
h_{FE}	$V_{CE}=5.0\text{V}, I_C=500\text{mA}$	200		
h_{FE}	$V_{CE}=5.0\text{V}, I_C=1.0\text{A}$	100		
f_T	$V_{CE}=10\text{V}, I_C=50\text{mA}$	150		MHz
C_{ob}	$V_{CB}=10\text{V}, I_E=0, f=1.0\text{MHz}$		10	pF

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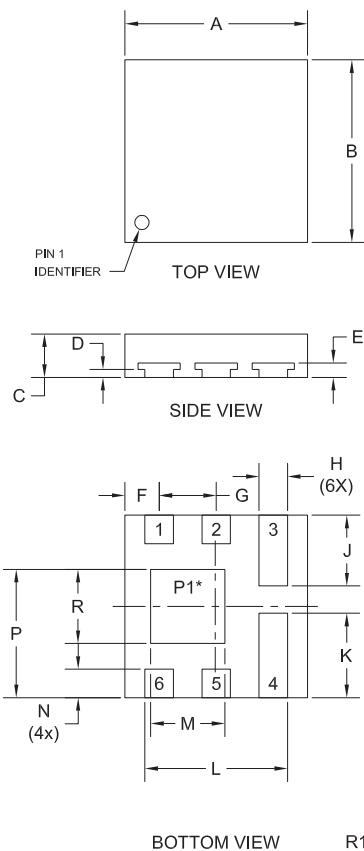
DESCRIPTION:

The CENTRAL SEMICONDUCTOR CTTL3820-M563 is a very low $V_{CE(SAT)}$ NPN Transistor packaged in a space saving 1.6 x 1.6mm TLM™ surface mount package. This device is a TLM™ equivalent of the popular CMLT3820G, SOT-563 device, featuring enhanced thermal characteristics, a package footprint compatible with standard SOT-563 mounting pad geometries, and a height profile of only 0.4mm.

MARKING CODE: CKT**FEATURES:**

- High Current ($I_C=1.0\text{A}$)
- $V_{CE(SAT)}=0.28\text{V MAX} @ I_C=1.0\text{A}$
- Low Profile 0.4mm Package compatible with SOT-563 mounting pad geometries.
- Complementary PNP device **CTLT7820-M563**

TLM563 CASE - MECHANICAL OUTLINE



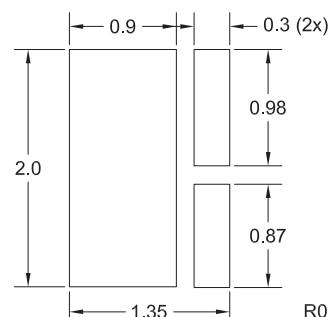
* Exposed pad P1 common to pins 1, 2, 5, and 6.

SYMBOL	DIMENSIONS			
	INCHES	MILLIMETERS	MIN	MAX
A	0.062	0.064	1.57	1.63
B	0.062	0.064	1.57	1.63
C	0.014	0.017	0.36	0.43
D	0.002	0.004	0.04	0.10
E	0.004	0.006	0.10	0.16
F	0.011	0.013	0.27	0.33
G	0.019	0.021	0.47	0.53
H	0.009	0.011	0.22	0.28
J	0.023	0.026	0.59	0.65
K	0.028	0.030	0.71	0.77
L	0.048	0.050	1.22	1.28
M	0.024	0.027	0.62	0.68
N	0.009	0.011	0.22	0.28
P	0.043	0.045	1.09	1.16
R	0.024	0.027	0.62	0.68

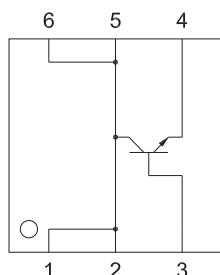
TLM563 (REV:R1)

SUGGESTED MOUNTING PADS

(Dimensions in mm)



PIN CONFIGURATION



LEAD CODE:

- 1) COLLECTOR
- 2) COLLECTOR
- 3) BASE
- 4) Emitter
- 5) COLLECTOR
- 6) COLLECTOR

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R0 (24-September 2009)