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Information

DUAL OPERATION FLASH MEMORY 32M BITS A SERIES

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[MEMO]

SUMMARY OF CONTENTS

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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MAJOR REVISIONS IN THIS EDITION

Edition/ Date	Page		Description	
	This edition	Previous edition	Type of revision	Location
4th edition/ Oct. 2002	p.7	p.6	Addition	INTRODUCTION Object Products
	p.8	p.7		Related Documents
	p.20	p.21	Modification	Table 3-1. Command Sequence Remark
	p.36	p.39		Figure 6-9. Sector / Chip Erase Timing Chart

The mark ★ shows major revised points.

INTRODUCTION

Target Readers This manual is intended for users who wish to design hardware using our dual operation flash memory.

Purpose This manual is intended to give users understanding of the basic functions of dual operation flash memory and how to use them.

Organization This manual explains the operation of our dual operation flash memory. For specifications and addresses, refer to the Data Sheet of each product.

Conventions
Note: Footnote for items marked with Note in the text
Remark: Supplementary information

★ **Object Products** This manual explains our following dual operation flash memory.

Dual Operation Flash Memory

Density (bits)	Organization (words × bits)	Part Number
32M	4M × 8 / 2M × 16	μPD29F032202AL-X μPD29F032203AL-X μPD29F032204AL-X μPD29F032202AL-Y μPD29F032203AL-Y μPD29F032204AL-Y

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Document Name	Document Number
μPD29F032202AL-X DATA SHEET	M14911E
μPD29F032203AL-X DATA SHEET	M14907E
μPD29F032204AL-X DATA SHEET	M14912E
μPD29F032202AL-Y DATA SHEET	M15515E
μPD29F032203AL-Y DATA SHEET	M15504E
μPD29F032204AL-Y DATA SHEET	M15516E
★ MC-222242A-X DATA SHEET	M14908E
MC-222243A-X DATA SHEET	M15029E
MC-222244A-X DATA SHEET	M15318E
★ MC-222252A-X DATA SHEET	M15319E
MC-222253A-X DATA SHEET	M15285E
MC-222254A-X DATA SHEET	M14931E
★ MC-222262-X DATA SHEET	M14923E
MC-222263-X DATA SHEET	M15067E
MC-222264-X DATA SHEET	M15340E
★ MC-222272-X DATA SHEET	M15341E
MC-222273-X DATA SHEET	M15289E
MC-222274-X DATA SHEET	M15342E
MC-242442 DATA SHEET	M15413E
MC-242443 DATA SHEET	M15171E
MC-242444 DATA SHEET	M15411E
MC-242452 DATA SHEET	M15414E
MC-242453 DATA SHEET	M15371E
MC-242454 DATA SHEET	M15372E
MC-2511430 DATA SHEET	M15462E
MC-2621930 DATA SHEET	M15456E
MC-2721930-X DATA SHEET	M15461E

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CHAPTER 1 INPUT / OUTPUT PIN FUNCTION

For specifications, refer to the Data Sheet of each product.

Input / Output Pin Function

Pin name	Input / Output	Function
A0 to A20	Input	Address input pins. A0 to A20 are used differently in the BYTE mode and the WORD mode. BYTE MODE A0 to A20 are used as the upper 21 bits of total 22 bits of address input pin. (The least significant bit (A−1) is combined to I/O15.) WORD MODE A0 to A20 are used as 21 bits address input pin.
I/O0 to I/O14	Input / Output	Data input / output pins. I/O0 to I/O14 are used differently in the BYTE mode and the WORD mode. BYTE MODE I/O0 to I/O7 are used as the 8 bits data input / output pins. I/O8 to I/O14 are High-Z. WORD MODE I/O0 to I/O14 are used as the lower 15 bits of total 16 bits of data input / output pins. (The most significant bit (I/O15) is combined to A−1.)
I/O15, A−1	Input / Output	I/O15, A−1 are used differently in the BYTE mode and the WORD mode. BYTE MODE The least significant address input pin (A−1) WORD MODE The most significant data input / output pin (I/O15)
/CE	Input	This pin inputs the signal that activates the chip. When high level, the chip enters the standby mode.
/OE	Input	This pin inputs the read operation control signal. When high level, output is High-Z.
/WE	Input	This pin inputs the write operation control signal. When low level, command input is accepted.
/BYTE [Note]	Input	The pin for switching BYTE mode and WORD mode. High level : WORD MODE (2M words × 16 bits) Low level : BYTE MODE (4M words × 8 bits)
/RESET	Input	This pin inputs hardware reset. When low level, hardware reset is performed. If 11.5 to 12.5 V is applied to /RESET, the chip enters the temporary sector group unprotect mode.
RY (/BY)	Output	This pin indicates whether automatic program / erase is currently being executed. It uses open drain connection. Low level indicates the busy state during which the device is performing automatic program / erase. High level indicates the device is in the ready state and will accept the next operation. In this case, the device is either in the erase suspend mode or the standby mode.
/WP (ACC)	Input	This pin selects the boot block sector protect mode or accelerated mode. Low level: The boot block (2 sectors) is protected. High level: The boot block is unprotected. V_{ACC} level: Accelerated mode is selected.
V_{CC}	–	Supply Voltage
GND	–	Ground
NC	–	No Connection (Some signals can be applied.)

Note The CIOf pin is used to switch between BYTE mode and WORD mode in the flash memory incorporated in MCP products.

CHAPTER 2 BUS OPERATIONS

The following table shows the operation modes of the dual operation flash memory.

Before turning on power, input GND ± 0.2 V to the /RESET until $V_{CC} \geq V_{CC}$ (MIN.).

For specifications, refer to the Data Sheet of each product.

Table 2-1. Bus Operation

Operation		/CE	/OE	/WE	I/O15, A–1	A6	A1	A0	I/O0 to I/O7	I/O8 to I/O15	/RESET	/WP (ACC)
Read [Note]	BYTE mode	L	L	H	A–1	Address input			Data output	High-Z	H	×
	WORD mode	L	L	H	×	Address input			Data output		H	×
Write	BYTE mode	L	H	L	A–1	Address input			Data input	High-Z	H	×
	WORD mode	L	H	L	×	Address input			Data input		H	×
Standby		H	×	×	×	×	×	×	High-Z	High-Z	H	×
Hardware reset / Standby		×	×	×	×	×	×	×	High-Z	High-Z	L	×
Output Disable		L	H	H	×	×	×	×	High-Z	High-Z	H	×
Temporary Sector Group Unprotect		×	×	×	×	×	×	×	High-Z or Data input / output		V_{ID}	×
Automatic Sleep Mode	BYTE mode	L	L	H	A–1	Address input			Data output	High-Z	H	×
	WORD mode	L	L	H	×	Address input			Data output		H	×
Boot Block Sector Protect		×	×	×	×	×	×	×	High-Z or Data input / output		×	L
Accelerated Mode	BYTE mode	L	H	L	A–1	Address input			Data input	High-Z	H	V_{ACC}
	WORD mode	L	H	L	×	Address input			Data input		H	V_{ACC}

Note When /OE = V_{IL}, V_{IL} can be applied to /WE. When /OE = V_{IH}, a write operation is started.

Remarks 1. H : V_{IH}, L : V_{IL}, × : V_{IH} or V_{IL}, V_{ID} : 11.5 V to 12.5 V, V_{ACC} : 8.5 V to 9.5 V

2. If an address is held longer than the minimum read cycle time (t_{RC}), the automatic sleep mode is set.

2.1 Read

The read operation is controlled by the /CE and /OE. The /CE is used to select a device, and the /OE controls data output. The following three access times are used depending on the condition.

- Address access time (t_{ACC}): Time until valid data is output after an address has been determined (however, after /CE).
- /CE access time (t_{CE}): Time until valid data is output after /CE has been determined (however, after address).
- /OE access time (t_{OE}): Time until valid data is output after /OE has been determined (however, /OE must be input after t_{ACC}–t_{OE}, t_{CE}–t_{OE} after address and /CE have been determined).

On power-up, the device is automatically set in the read mode. To read the device without changing address immediately after power application, either execute hardware reset or briefly lower /CE to V_{IL} from V_{IH}.

For the timing chart, refer to **Figure 6-1. Read Cycle Timing Chart 1**.

2.2 Write

The operation of the device is controlled by writing commands to the registers. The command register is a function that latches the address and data necessary for executing an instruction and does not occupy the memory area.

If an illegal address or data is written or if an address or data is written in the wrong sequence, the device is reset to the read mode.

Refer to **CHAPTER 3 COMMANS** for command details.

2.3 Standby

The standby mode is set when V_{IH} is input to the /CE. The current consumption in the standby mode can be lowered to 5 μA or less in two ways.

One is to use /CE and /RESET. Input $V_{CC} \pm 0.3$ V to /CE and /RESET. However, while automatic programming or erasing is being executed, the operating supply current (I_{CC2}) does not decrease to 5 μA or lower even if /CE = V_{IH}. If a read operation is executed in the standby mode, data is output at /CE access time.

The other is to input GND $\pm$ 0.3 V to the /RESET. At this time, the level of /CE is V_{IH} or V_{IL}. In this case, t_{RH} is required for the device to return to the read mode from the standby mode.

For the timing chart, refer to **Figure 6-2. Read Cycle Timing Chart 2**.

2.4 Hardware Reset

The device is reset to the read mode if V_{IL} is input to the /RESET for the duration of t_{RP} and V_{IH} for the duration of t_{RH}. While V_{IL} is being input to the /RESET, all commands are ignored, and the output pins go into a high impedance state. If the voltage on /RESET is kept to GND $\pm$ 0.2 V at this time, the current consumption can be lowered to 5 μA or less.

Read mode is restored by t_{READY} after V_{IL} is input to the /RESET pin.

For the timing chart, refer to **Figure 6-2. Read Cycle Timing Chart 2**.

2.5 Output Disable

Output from the device is disabled (High impedance state) if V_{IH} is input to the /OE.

2.6 Sector Group Protection

Protect the sector group by using a command. /CE or /WE control is no need. For details, refer to **3.10 Sector Group Protection**.

2.7 Temporary Sector Group Unprotect

Protection of a sector group can be temporarily canceled. When V_{ID} is input to /RESET, the temporary sector group unprotect mode is set. If a protected sector is selected in this mode, it can be programmed or erased. If the mode is canceled, the sector group is protected again.

For the timing chart, refer to **Figure 6-4. Temporary Sector Group Unprotect Timing Chart**.

2.8 Product ID

Read the product ID code by using a command. For details, refer to **3.3 Product ID**.

2.9 Automatic Sleep Mode

The automatic sleep mode is used to reduce the power consumption substantially during a read operation.

If an address is held longer than the minimum read cycle time (t_{RC}), the sleep mode (low power consumption mode) is automatically set. In this mode, the output data is latched and continuously output.

In the automatic sleep mode, /CE, /WE, and /OE do not have to be controlled. At this time, the current consumption decreases to 5 μA or less. During dual operation, however, the current consumption is power supply current (I_{CC6}, I_{CC7}).

If the address is changed, the automatic sleep mode is canceled automatically, the device returns to the read mode, and the data of the newly input address is output.

2.10 Boot Block Sector Protect

The boot block sector protect mode protects the two sectors of the boot block. This mode is set when V_{IL} is input to /WP (ACC). If V_{IL} is input to /WP (ACC) even in the temporary sector group unprotect mode, the boot block remains protected and protection of the other sectors is temporarily canceled.

2.11 Accelerated Mode

This mode is used to program the device at high speed, and the programming time can be shortened to about 60%.

To program the device in the accelerated mode, input V_{ACC} to /WP (ACC) and use an unlock bypass program command. Therefore, ordinary commands can be used for programming or detection of completion of programming. If V_{ACC} is input to /WP (ACC), the device is automatically set in the unlock bypass mode. Therefore, the unlock bypass set command and reset command are not necessary. The accelerated mode is automatically canceled if the input of V_{ACC} to /WP (ACC) is stopped.

In the accelerated mode, protection of the sector group is temporarily canceled. Exercise care in programming the device at this time.

For the timing chart, refer to **Figure 6-5. Accelerated Mode Timing Chart**.

2.12 Dual Operation

This device can execute a program or erase operation and a read operation simultaneously. By selecting bank 1 or 2 by changing the bank address, one bank can execute a read operation while the other bank is executing a program or erase operation. When changing the bank address, no wait cycle is necessary. Note that two or more operations cannot be executed at the same time in the same bank.

The following table shows the combinations of bank operations.

For the timing chart, refer to **Figure 6-6. Dual Operation Timing Chart**.

Table 2-2. Dual Operation

Case	Operation of Bank 1	Operation of Bank 2
1	Read mode	Read mode
2	Read mode	Product ID
3	Read mode	Program Note1
4	Read mode	Erase Note2
5	Product ID	Read mode
6	Program Note1	Read mode
7	Erase Note2	Read mode

Notes 1. The program operation is suspended by the program suspend command, and addresses not being programmed to at this time can only be read.

2. The erase operation is suspended by the erase suspend command. The sector not erased at this time can be read or programmed.

CHAPTER 3 COMMANDS

This chapter explains the commands of the dual operation flash memory and how to write the commands.

3.1 Writing commands

All operations are executed by writing a command.

To write a command, the write cycle of a standard microprocessor is used.

The operation of the device is controlled by writing a command to a register. The command register is a function that latches the address and data necessary for executing an instruction and does not occupy the memory area.

If an illegal address or data is written or if an address or data is written in the wrong sequence, the device is reset to the read mode.

Table 3-1 shows the commands and command sequences.

For specifications, refer to the Data Sheet of each product.

Table 3-1. Command Sequence

Command sequence		Bus cycles	1st bus cycle		2nd bus cycle		3rd bus cycle		4th bus cycle		5th bus cycle		6th bus cycle	
			Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Read / Reset [Note 1]		1	×××H	F0H	RA	RD	–	–	–	–	–	–	–	–
Read / Reset [Note 1]	BYTE mode	3	AAAH	AAH	555H	55H	AAAH	F0H	RA	RD	–	–	–	–
	WORD mode		555H		2AAH		555H							
Program	BYTE mode	4	AAAH	AAH	555H	55H	AAAH	A0H	PA	PD	–	–	–	–
	WORD mode		555H		2AAH		555H							
Program Suspend [Note 2]		1	BA	B0H										
Program Resume [Note 3]		1	BA	30H										
Chip Erase	BYTE mode	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	AAAH	10H
	WORD mode		555H		2AAH		555H		555H		2AAH		555H	
Sector Erase	BYTE mode	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	FSA	30H
	WORD mode		555H		2AAH		555H		555H		2AAH			
Sector Erase Suspend [Note 4]		1	BA	B0H	–	–	–	–	–	–	–	–	–	–
Sector Erase Resume [Note 5]		1	BA	30H	–	–	–	–	–	–	–	–	–	–
Unlock Bypass Set	BYTE mode	3	AAAH	AAH	555H	55H	AAAH	20H	–	–	–	–	–	–
	WORD mode		555H		2AAH		555H							
Unlock Bypass Program [Note 6]		2	×××H	A0H	PA	PD	–	–	–	–	–	–	–	–
Unlock Bypass Reset [Note 6]		2	BA	90H	×××H	00H [Note 11]	–	–	–	–	–	–	–	–
Product ID	BYTE mode	3	AAAH	AAH	555H	55H	(BA) AAAH	90H	IA	ID	–	–	–	–
	WORD mode		555H		2AAH		(BA) 555H							
Sector Group Protection [Note 7]		4	×××H	60H	SPA	60H	SPA	40H	SPA	SD	–	–	–	–
Sector Group Unprotect [Note 8]		4	×××H	60H	SUA	60H	SUA	40H	SUA	SD	–	–	–	–
Query [Note 9]	BYTE mode	1	AAH	98H	–	–	–	–	–	–	–	–	–	–
	WORD mode		55H											
Extra One Time Protect Sector Entry	BYTE mode	3	AAAH	AAH	555H	55H	AAAH	88H	–	–	–	–	–	–
	WORD mode		555H		2AAH		555H							
Extra One Time Protect Sector Program [Note 10]	BYTE mode	4	AAAH	AAH	555H	55H	AAAH	A0H	PA	PD	–	–	–	–
	WORD mode		555H		2AAH		555H							
Extra One Time Protect Sector Erase [Note 10]	BYTE mode	6	AAAH	AAH	555H	55H	AAAH	80H	AAAH	AAH	555H	55H	EOTPSA	30H
	WORD mode		555H		2AAH		555H		555H		2AAH			
Extra One Time Protect Sector Reset [Note 10]	BYTE mode	4	AAAH	AAH	555H	55H	AAAH	90H	×××H	00H	–	–	–	–
	WORD mode		555H		2AAH		555H							
Extra One Time Protect Sector Protection [Note 10]		4	×××H	60H	EOTPSA	60H	EOTPSA	40H	EOTPSA	SD	–	–	–	–

Notes 1. Both these read / reset commands reset the device to the read mode.

2. Programming is suspended if B0H is input to the bank address being programmed to in a program operation.

3. Programming is resumed if 30H is input to the bank address being suspended to in a program-suspend operation.

4. Erasure is suspended if B0H is input to the bank address being erased in a sector erase operation.

5. Erasure is resumed if 30H is input to the bank address being suspended in a sector-erase-suspend operation.

6. Valid only in the Unlock Bypass mode.

7. Valid only in /RESET = V_{ID} (except in the Extra One Time Protect Sector mode).

8. The command sequence that protects a sector group is excluded.

9. Only A0 to A6 are valid as an address.

10. Valid only in the Extra One Time Protect Sector mode.

11. This command can be used even if this data is F0H.

Remarks 1. The system should generate the following address pattern :

WORD mode : 555H or 2AAH (A10 to A0)

BYTE mode : AAAH or 555H (A10 to A0, and A–1)

2. RA : Read address

RD : Read data

IA : Address input as follows

××00H (to read the manufacturer code)

××02H (to read the device code in the BYTE mode)

××01H (to read the device code in the WORD mode)

ID : Code output. For the manufacture code, device code and sector group protection information, refer to the **Product ID code** in each data sheet.

PA : Program address

PD : Program data

★ FSA : Erase sector address. The sector to be erased is selected by the combination of A20 to A12. Refer to the **Sector Organization / Sector Address Table** in each data sheet.

BA : Bank address. Refer to the **Sector Organization / Sector Address Table** in each data sheet.

★ SPA : Sector group address to be protected or protection-verified. Set the sector group address (SGA) and (A6, A1, A0) = (V_{IL}, V_{IH}, V_{IL}).

Sector group protection can be set for each sector group address. For details, refer to **3.10 Sector Group Protection**.

For the sector group address, refer to the **Sector Group Address Table** in each data sheet.

★ SUA : Sector group address to be unprotected or unprotection-verified. Set the sector group address (SGA) and (A6, A1, A0) = (V_{IH}, V_{IH}, V_{IL}).

Sector group unprotect is performed for all sector group using a single command, however, unprotect verification must be performed for each sector group address. For details, refer to **3.11 Sector Group Unprotect**.

For the sector group address, refer to the **Sector Group Address Table** in each data sheet.

EOTPSA : Extra One Time Protect Sector area addresses. These addresses are 3F0000H to 3FFFFFH (BYTE mode) / 1F8000H to 1FFFFFH (WORD mode) for top boot, and 000000H to 00FFFFH (BYTE mode) / 000000H to 007FFFH (WORD mode) for bottom boot.

SD : Data for verifying whether sector groups read from the address specified by SPA, SUA, EOTPSA are protected or unprotected.

3. The sector group address is don't care except when a program / erase address or read address are selected.

4. For the operation of bus, refer **CHAPTER 2 BUS OPERATION**.

5. × of address bit indicates V_{IH} or V_{IL}.

3.2 Read / Reset

This command resets the device to the read mode.

The read mode is maintained until the contents of the command register are changed.

Once the device is in the read mode, no command is necessary for reading data. Data read can be performed using the read cycle of a standard microprocessor.

The read mode is maintained until the contents of the command register are changed.

3.3 Product ID

The manufacturer code and device code can be read without inputting a high voltage to the address pin.

If a bank address is specified in the third bus cycle and a read operation is started from address xx00H in the fourth bus cycle, manufacturer code 0010H is output. If address xx02H (BYTE mode) or xx01H (WORD mode) is read, the device code is output. If a read operation is executed from an address in the bank not specified in the third bus cycle, data of the memory cell is output.

If a read operation is executed starting from address (BA) 02H (WORD mode) or (BA) 04H (BYTE mode), information indicating which sector group is protected can be obtained. If the sector group address is scanned with (A6, A1, A0) = (V_{IL}, V_{IH}, V_{IL}), "1" is output to I/O0 to indicate that the sector group is protected (for details refer to **3.10 Sector Group Protection**).

The product ID can be read only from the specified bank. To read the manufacturer code, device code, and information on protection of sector group from a bank not specified, write the read / reset command, specify the bank address to be read, and then write the product ID command again. To end the product ID mode, writes the read / reset command. To write the product ID command in the product ID mode, execute the read / reset command once.

3.4 Program

This command is used to program data.

Program is performed in 1 byte or 1 word units. Program can be performed regardless of the address sequence, even if the sector limit is exceeded. However, "0" cannot be changed back into "1" through the program operation. If overwriting "1" to "0" is attempted, the program operation is interrupted and "1" is output to I/O5, or successful program is indicated in data polling, but actually the data is "0" as before.

Following write by command sequence, the pulse required for program is automatically generated inside the device and program verification is automatically performed, so that control from external is not required.

During automatic program, any command other than the program suspend is ignored. However, automatic program is interrupted when hardware reset is performed. Since the programmed data is not guaranteed in this case, reexecute the program command following completion of reset.

Upon completion of automatic program, the device returns to the read mode.

The operation status of automatic program can be determined by using the hardware sequence flags (I/O7, I/O6, RY (/BY) pins).

See sections **4.2 I/O7 (Data Polling)**, **4.3 I/O6 (Toggle Bit)**, and **4.7 RY (/BY) (Ready / Busy)**.

For the timing chart and flow chart, refer to **Figure 6-7. Write Cycle Timing Chart (/WE Controlled), Figure 6-8. Write Cycle Timing Chart (/CE Controlled)** and **Figure 7-2. Program Flow Chart**.

3.5 Program Suspend / Resume

This command is used to suspend automatic programming. Addresses not being programmed to while programming is suspended can be read.

Sector erase (including the timeout period) and data program operations can be both suspended. Chip erase operations cannot be suspended.

1 μs is required between when the command sequence is programmed and when the automatic program operation is suspended.

The execution status of an automatic program operation can be determined using a hardware sequence flag (I/O7, I/O6 pins.) refer to **4.2 I/O7 (Data polling)** and **4.3 I/O6 (Toggle Bit)**.

To resume an automatic program operation, write the resume command (30H) while the operation is suspended.

3.5.1 Caution about Program Suspend / Resume

If automatic program resume and suspend are repeated at intervals of less than 5 μs, the program operation may not be correctly completed.

3.6 Chip Erase

This command is used to erase the entire chip.

Following command sequence write, erase is performed after "0" is written to all memory cells and verification is performed, using the automatic erase function. Program before erase and control from external are not required.

During automatic erase, all commands that have been written are ignored. However, automatic erase is interrupted by hardware reset. Since erase is not guaranteed in this case, execute the chip erase command again after reset is completed.

Upon completion of automatic erase, the device returns to read mode.

The automatic erase operation status can be determined with the hardware sequence flags (I/O7, I/O6, RY (/BY) pins). See sections **4.2 I/O7 (Data Polling), 4.3 I/O6 (Toggle Bit)**, and **4.7 RY (/BY) (Ready / Busy)**.

For the timing chart and flow chart, refer to **Figure 6-9. Sector / Chip Erase Timing Chart** and **Figure 7-3. Sector / Chip Erase Flow Chart**.

3.7 Sector Erase

This command is used to erase data in sector units.

"0" is written to the entire sector whose data is to be erased by the automatic erase function after the command sequence has been written, and erase is executed after verification has been performed. Programming before erase and external control are not necessary.

The timeout period of sector erase starts when erase command 30H and the address of the sector to be erased are written at the sixth bus cycle. When this timeout period (50 μs) has elapsed, the device automatically starts erasing.

Two or more sectors can be selected and erased at the same time by additionally writing erase command 30H and the address of the sector whose data is to be erased during the timeout period. In this case, the timeout period starts again after the last erase command has been written.

If a protected sector and a sector that is not protected are included in the selected sectors, only the sector that is not protected is erased and the protected sector is ignored.

If a command other than the sector erase or erase suspend command is input during the timeout period, the device is reset to the read mode. If the timeout period has elapsed and erase has started, any command other than the erase suspend command is ignored. However, erase is stopped if hardware reset is executed. In this case, sector erase is not guaranteed. Execute the sector erase command again after completion of reset.

When automatic erasure has been completed, the device returns to the read mode.

Completion of automatic sector erase can be reported to the host system by using the data polling function of I/O7, toggle bit function of I/O6, and RY (/BY) pin. Sector erase is started after the lapse of the timeout period that is started from the rising of the /WE or /CE pulse, whichever earlier, of the last sector erase command and is completed when the data of I/O7 is set to "1" (refer to **CHAPTER 4 HARDWARE SEQUENCE FLAGS**). The device returns to the read mode. Data polling and toggle bit function in any address of the sector that is to be erased. The time require to erase two or more sectors is "(sector programming time + sector erase time) x number of sectors". If two or more sectors of different banks are erased, a read operation from a bank (i.e., dual operation) cannot be executed.

For the timing chart and flow chart, refer to **Figure 6-9. Sector / Chip Erase Timing Chart** and **Figure 7-3. Sector / Chip Erase Flow Chart**.

3.8 Sector Erase Suspend / Resume

This command suspends automatic erase. During erase suspend, sectors for which erase is not performed can be read and programmed.

Sector erase (including the timeout period) and data program operations can be both be suspended. Chip erase operations cannot be suspended. Suspend can be performed for all sectors for which erase is being performed.

Following command sequence write, 20 μs are required until automatic erase is suspended.

While automatic erase is suspended, any sector for which erase is not being performed can be read and programmed.

Whether automatic erase is suspended can be determined with the hardware sequence flags (I/O7, I/O6, I/O2 pins). See sections **4.2 I/O7 (Data Polling)**, **4.3 I/O6 (Toggle Bit)**, and **4.4 I/O2 (Toggle Bit II)**.

If resume automatic erase that has been suspended, write the resume command (30H) while sector erase is suspended. At this time, input a bank address of the sector for which erasure is suspended.

3.8.1 Caution about Sector Erase Suspend / Resume

If automatic erase resume and suspend are repeated at intervals of less than 100 μs, the erasure operation may not be correctly completed.

3.9 Unlock Bypass

This device provides an unlock bypass mode to shorten the program time.

Normally, 4 write cycle included with 2 unlock cycles are required during program. In contrast, with the unlock bypass mode, it is possible to perform program without unlock cycles.

In the unlock bypass mode, all commands except unlock bypass program and unlock bypass reset are ignored.

To end the unlock bypass mode, the unlock bypass reset command must be written. Note, however, that the unlock bypass reset command must be written to an address of the bank that is not being read in dual operation. If the unlock bypass reset command is written, the device returns to the normal read mode.

In the unlock bypass mode, the operating current is necessary even if /CE = V_{IH}.

For the flowchart, refer to **Figure 7-4. Unlock Bypass Flow Chart (WORD Mode)**.

3.9.1 Unlock Bypass Set

This command sets the device to the unlock bypass mode.

3.9.2 Unlock Bypass Program

This command is used to perform program in the unlock bypass mode.

3.9.3 Unlock Bypass Reset

This command is used to quit the unlock bypass mode.

When this command is executed, the device returns to the read mode.

3.10 Sector Group Protection

This command performs sector group protection.

By applying V_{ID} to /RESET and writing 60H to any address, the device enters the sector group protection mode.

Sector group protection is started by inputting the sector group address of the sector group to be protected to A12 to A20, inputting (A6, A1, A0) = (V_{IL}, V_{IH}, V_{IL}), and writing 60H. After a timeout of 250 μs, sector group protection is completed.

Next, with the sector group address input to A12 to A20, the device enters the sector group protection verify mode by inputting (A6, A1, A0) = (V_{IL}, V_{IH}, V_{IL}), and writing 40H. When read is performed in this state, the sector group protection verify result is output to I/O0. If "1" is output to I/O0, the verified sector group is protected. If "1" was not output to I/O0, sector group protection failed, so perform sector group protection again.

For the timing chart and flow chart, refer to **Figure 6-3. Sector Group Protection Timing Chart** and **Figure 7-1. Sector Group Protection Flow Chart**.

3.11 Sector Group Unprotect

This command performs sector group unprotect.

Sector group unprotect is performed for all sector group. Unprotect cannot be performed for specific sector group. Moreover, all sector groups must be protected priors to unprotect.

The device enters the sector group unprotect mode by applying V_{ID} to /RESET and writing 60H to any address.

If unprotected sector group exist, first perform sector group protection for these sector groups. To protect a sector group, input the sector group address of the sector group to be protected to the sector group address input pin, input (A6, A1, A0) = (V_{IL}, V_{IH}, V_{IL}), and write 60H (refer to **3.10 Sector Group Protection**).

Sector group unprotect is started by inputting (A6, A1, A0) = (V_{IH}, V_{IH}, V_{IL}), and writing 60H to any address. Following a timeout of 15 ms, sector group unprotect is completed.

Unprotect verification must be performed for each sector group.

The device enters the sector group unprotect verification mode by inputting the sector group address to input pin of sector group address and writing 40H, with input (A6, A1, A0) = (V_{IH}, V_{IH}, V_{IL}).

If reading is performed in this state, the sector group unprotect verification result is output to I/O0. If the verified sector group is unprotected, "0" is output to I/O0. If "0" is not output to I/O0, this means that unprotect failed, so perform sector group unprotect again.

For the flow chart, refer to **Figure 7-5. Sector Group Unprotect Flow Chart**.

3.12 Query

The dual operation flash memory conforms to CFI (Common Flash memory Interface). CFI enables information about a device such as the device specifications, memory density, and supply voltage to be read. Therefore, the software of the host system can support the software algorithm of a specific vendor used by a device by using the CFI. For details, refer to the CFI specifications.

By writing the Query command (98H) and giving an address, the device information corresponding to that address can be read (refer to the **CFI Code List** in each Data Sheet). If the device information is read in the WORD mode (16 bits), the upper bytes of data (I/O15 to I/O8) are "0".

To end the Query mode, writes the read / reset command.

3.13 Extra One Time Protect Sector Entry

The dual operation flash memory has a sector area that has One Time Protect function. This area does not allow code that has been written to the area to be changed. This area can be programmed or erased until it is protected. Once it has been protected, however, protection can never be canceled. Therefore, care must be exercised when using this area.

The Extra One Time Protect Sector area has a density of 64 Kbytes and exits at the same addresses as the 8K bytes sector. These addresses are 3F0000H to 3FFFFFH for top boot in the BYTE mode (1F8000H to 1FFFFFH in the WORD mode), and 000000H to 00FFFFH for bottom boot in the BYTE mode (000000H to 007FFFH in the WORD mode). Because boot block areas (8K bytes x 8 sectors) usually appear in the areas of these addresses, the Extra One Time Protect Sector entry command sequence must be written to enter them as the Extra One Time Protect Sector area. The status in which the Extra One Time Protect Sector area appears is the Extra One Time Protect Sector mode.

In the Extra One Time Protect Sector mode, the other sectors, except the boot block area, can be read. In addition, the Extra One Time Protect Sector area can be read, programmed, or erased in this mode. To exit from the Extra One Time Protect Sector mode, the Extra One Time Protect Sector Reset command sequence must be written.

3.14 Extra One Time Protect Sector Program

To program data to the Extra One Time Protect Sector area, write the Extra One Time Protect Sector Program command sequence in the Extra One Time Protect Sector mode. This command is no different from the conventional program command except that it must be written in the Extra One Time Protect Sector mode. Therefore, completion of execution of this command is detected in the same manner as the conventional detection method of using I/O7 data polling, I/O6 toggle bit, and RY(/BY). Care must be exercised in selecting a program destination address. If a program destination address other than the one in the Extra One Time Protect Sector area is selected, the data of that address is changed.

3.15 Extra One Time Protect Sector Erase

To erase the Extra One Time Protect Sector area, write the Extra One Time Protect Sector erase command sequence in the Extra One Time Protect Sector mode. This command is the same as the conventional sector erase command except that it must be written in the Extra One Time Protect Sector mode. Therefore, completion of execution of this command is detected in the same manner as the conventional detection method of using I/O7 data polling, I/O6 toggle bit, and RY(/BY). Care must be exercised in selecting a sector address to erase. If a sector address other than the one in the Extra One Time Protect Sector area is selected, the data of that sector is changed.

3.16 Extra One Time Protect Sector Protection

The following write operations are used to protect the Extra One Time Protect area during the Extra One Time Protect Sector mode.

- Write the sector group protection setup command (60H) in the Extra One Time Protect Sector mode.
- Set (A6, A1, A0) = (V_{IL}, V_{IH}, V_{IL}), and set the sector address that selects the Extra One Time Protect Sector.
- Write the sector group protection command (60H).

Because the sequence is the same as the conventional command sequence to protect a sector group except that the Extra One Time Protect Sector mode must be set and that V_{ID} is not input to the /RESET, the same command sequence can be used.

For details of how to protect a sector group, refer to **3.10 Sector Group Protection**.

If an address other than the one of the Extra One Time Protect Sector area is specified as a sector address, the other sectors are affected. Once the sector has been protected, protection can never be canceled. Exercise utmost care when protecting a sector.

CHAPTER 4 HARDWARE SEQUENCE FLAGS

The status of automatic program / erase operations can be determined from the status of the I/O2, I/O3, I/O5, I/O6, I/O7, and RY (/BY) pins.

Table 4-1. Hardware Sequence Flags

Status			I/O7[Note1]	I/O6[Note2]	I/O5[Note3]	I/O3	I/O2[Note1]	RY (/BY)
Progress	Program		/I/O7	Toggle	0	0	1	0
	Erase		0	Toggle	0	1	Toggle	0
	Program suspend	Program sector	Data	Data	Data	Data	Data	1
		Other than program sector	Data	Data	Data	Data	Data	1
	Erase suspend	Erase suspended sector	1	1	0	0	Toggle	1
		Other than erase suspended sector	Data	Data	Data	Data	Data	1
		Erase suspend program	/I/O7	Toggle	0	0	1	0
Exceeding time Limits	Program		/I/O7	Toggle	1	0	1	0
	Erase		0	Toggle	1	1	N/A	0
	Erase suspend	Erase suspend program	/I/O7	Toggle	1	0	N/A	0

Notes 1. To read I/O7 or I/O2, a valid address must be input.

2. To read I/O6, any address can be used.

3. For I/O5, "1" is output if the automatic program / erase time exceeds the prescribed number of internal pulses.

4.1 Caution When Reading Flags

When checking the completion or suspension status of an automatic program / erase operation by reading different sector data within the same bank, be sure to either clock the /CE or change the address before reading the data.

If the /CE is fixed to V_{IL} or data is read from the same address without the address being changed, the output data may not be output correctly.

4.2 I/O7 (Data Polling)

Data polling is a function to determine the status of automatic program / erase is currently being performed by using I/O7.

Data polling is valid from the rise of the last /WE in the program / erase command sequence.

The status of automatic program is currently being executed can be determined by reading from the program destination addresses. While automatic programming is being executed or while automatic programming is being executed during erasure suspension, the complement of the final data programmed will be output to I/O7. Upon completion of automatic program, the true value of the programmed data, not the complement, is output.

The status of automatic erase is in progress can be determined by reading from the addresses of the sector being erased. If erase is in progress, "0" is output to I/O7. If the automatic erase operation is complete or if it is suspend, "1" will be output to I/O7 when a sector for which erasure is suspended is read.

During automatic erase, if all the selected sectors are protected, data polling is valid for approximately 400 μs. The device is then reset to the read mode. If the selected sectors include protected and unprotected sectors, only unprotected sectors are erased, and protected sectors are ignored.

Upon completion of automatic program / erase, after the data output to I/O7 changes from the complement to the true value, I/O7 changes asynchronously like I/O0 to I/O6 while /OE is maintained at low level.

For the timing chart and flow chart, refer to **Figure 6-10. Data Polling Timing Chart** and **Figure 7-6. Data Polling Flow Chart**.

4.3 I/O6 (Toggle Bit)

The toggle bit is a function that uses I/O6 to determine the status of automatic program / erase is in progress.

The toggle bit is valid from the rise of the last /WE in the program / erase command sequence.

If a continuous read is performed from any address of a bank that is undergoing automatic program or erase, I/O6 will be toggled. If a sector other than the erased sector is read after automatic program / erase is complete or when it is suspended, the I/O6 toggle operation is stopped, and valid data for the read is output. If a sector for which erasure is suspended is read, “1” will be output to I/O6. Continuous read control is performed with the /OE or /CE.

If program is performed for an address inside a protected sector, I/O6 is toggled approximately 1 μs, and then the device is reset to the read mode.

Moreover, if all the sectors selected at the time of automatic erase are protected, I/O6 is toggled approximately 400 μs, and then the device is reset to the read mode.

In this way, by using I/O6, it is possible to determine the status of automatic erase is in progress (or suspended), but to determine which sector is being erased, I/O2 (toggle bit II) is used. See section **4.4 I/O2 (Toggle Bit II)**.

For the timing chart and flow chart, refer to **Figure 6-11. Toggle Bit Timing Chart**, **Figure 6-12. I/O2 vs. I/O6 Timing Chart** and **Figure 7-7. Toggle Bit Flow Chart**.

4.4 I/O2 (Toggle Bit II)

Toggle bit II is a function that determines the status of automatic erase (or erase suspend) is in progress for a particular sector by using I/O2.

I/O2 is toggled when continuous read is performed from addresses in a sector during automatic erase (or erase suspend). Either /OE or /CE is used to control continuous read.

When program to a sector that is not subject to erase suspend is attempted during erase suspend, read from sectors that are not subject to erase suspend cannot be performed until program is completed. In this case, "1" will be output to I/O2 if a continuous read is performed from an address in a sector other than an erased sector.

In this way, it is possible to determine the status of automatic erase (including erase suspend) is in progress for sectors specified using I/O2, but whether the state is erase in progress or erase suspend cannot be determined with I/O2. To determine this, I/O6 (toggle bit) must be used. See section **4.3 I/O6 (Toggle Bit)**.

For the timing chart, refer to **Figure 6-12. I/O2 vs. I/O6 Timing Chart**.

4.5 I/O5 (Exceeding Timing Limits)

If the program / erase time exceeds the prescribed number of pulses during automatic program / erase (exceeding timing limit), "1" is output to I/O5 and automatic program / erase failure is indicated.

Moreover, if overwriting "0" to "1" is attempted, the device judges data overwrite to be impossible, and "1" is output to I/O5 when the timing limit is exceeded.

When this happens, execute command reset.

4.6 I/O3 (Sector Erase Timer)

A 50 μs timeout period occurs following write with the sector erase command sequence before automatic erase starts.

During this timeout period, "0" is output to I/O3. When automatic erase starts upon completion of the timeout period, "1" is output to I/O3.

If sector erase is performed, first confirm whether the device has received a command by using I/O7 (data polling) or I/O6 (toggle bit). Then, using I/O3, check whether automatic erase has started. If I/O3 is "0", the timeout period is not over, and so it is possible to add sectors to erase. If I/O3 is "1", automatic erase starts and other commands (except erase suspend) are ignored until erase is completed.

If a sector to erase is added during the sector erase timeout period, it is recommended to check I/O3 prior to and following the addition. If I/O3 is "1" following the addition, that addition may not be accepted.

4.7 RY (/BY) (Ready / Busy)

The RY (/BY) is a dedicated output pin used to check the status of automatic program / erase is in progress.

During automatic program / erase, "0" is output to the RY (/BY). If "1" is output, this signifies that the device is either in the read mode (including erase suspend) or standby mode.

Since the RY (/BY) is an open-drain output pin, it is possible to connect several RY (/BY) in series by connecting a pull-up resistor to V_{CC}.

For the timing chart, refer to **Figure 6-13. RY (/BY) (Ready / Busy) Timing Chart**.

CHAPTER 5 HARDWARE DATA PROTECTION

This device requires two unlock cycles for program / erase command sequence to prevent illegal program / erase. Moreover, a hardware data protect function is provided as follows.

For specifications, refer to the Data Sheet of each product.

5.1 Low V_{CC} Write Inhibit

To prevent an illegal write cycle during V_{CC} transition, the command register and program / erase circuit is disabled and all write cycles are ignored while V_{CC} is V_{LKO} or lower. Write commands are ignored until V_{CC} becomes equal to or greater than V_{LKO}.

5.2 Logical Inhibit

The write cycle is inhibited under any of the following conditions : /OE = V_{IL}, /CE = V_{IH}, or /WE = V_{IH}. To start a write cycle, /CE = V_{IL} and /WE = V_{IL} must be set while /OE = V_{IH}.

5.3 Power-Up Write Inhibit

Even if /WE = /CE = V_{IL} and /OE = V_{IH} are satisfied at power-up, no commands are accepted at the rising edge of /WE. The device is automatically reset to the read mode at power ON.

5.4 Write Pulse "Glitch" Protection

Because /OE, /CE, and /WE reject a noise pulse of 5 ns (typical) or less as an invalid pulse, a write operation is not started.

5.5 Sector Group Protection

The dual operation flash memory can be protected by the user in sector group units. For details, refer to **3.10 Sector Group Protection**.

CHAPTER 6 TIMING CHARTS

For specifications, refer to the Data Sheet of each product.

The CIOf pin is used to switch between BYTE mode and WORD mode in the flash memory incorporated in MCP products.

Figure 6-1. Read Cycle Timing Chart 1

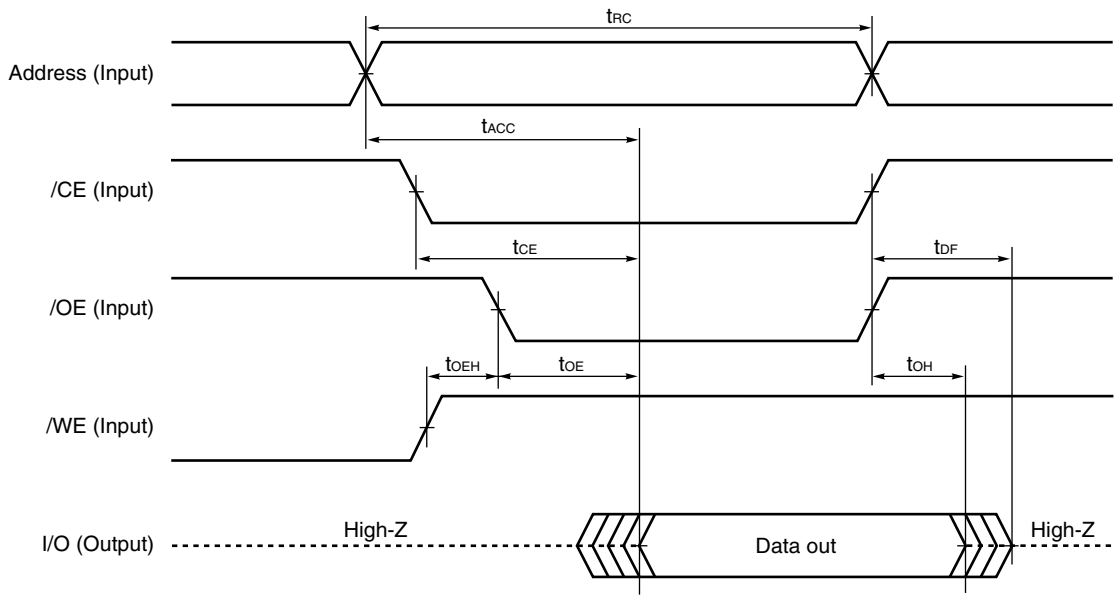


Figure 6-2. Read Cycle Timing Chart 2

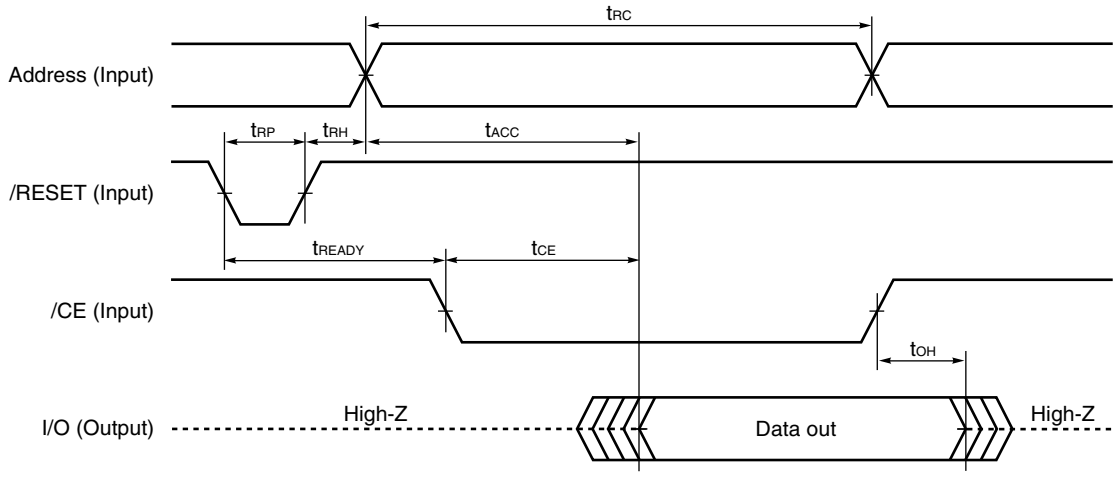
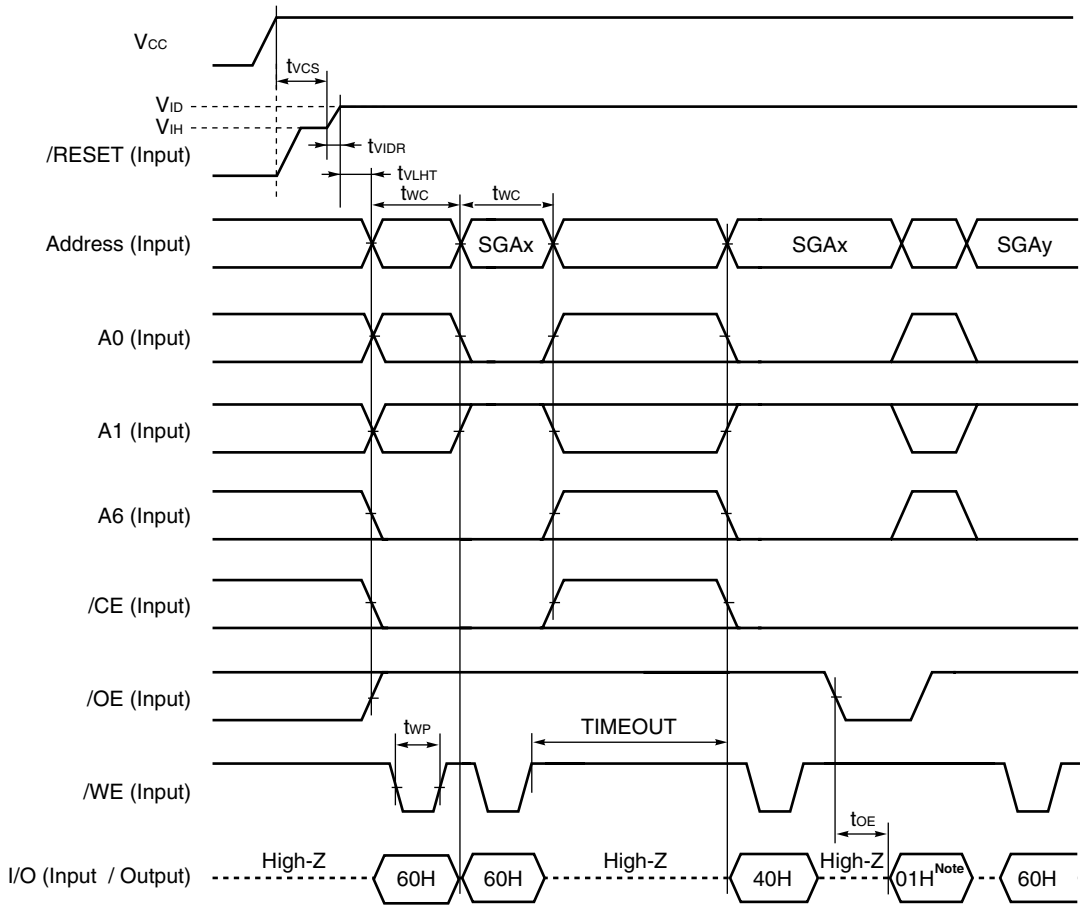


Figure 6-3. Sector Group Protection Timing Chart



Note The sector group protection verification result is output.

01H : The sector group is protected.

00H : The sector group is not protected.

Figure 6-4. Temporary Sector Group Unprotect Timing Chart

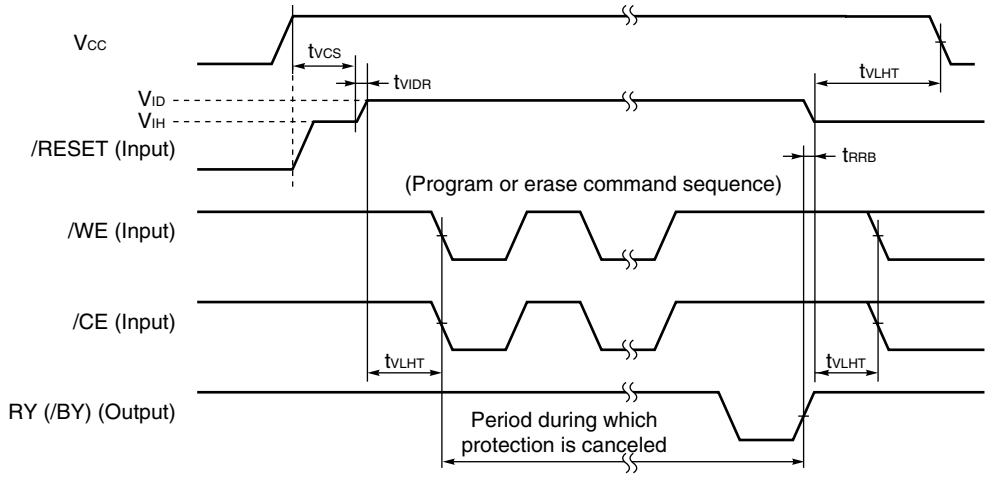


Figure 6-5. Accelerated Mode Timing Chart

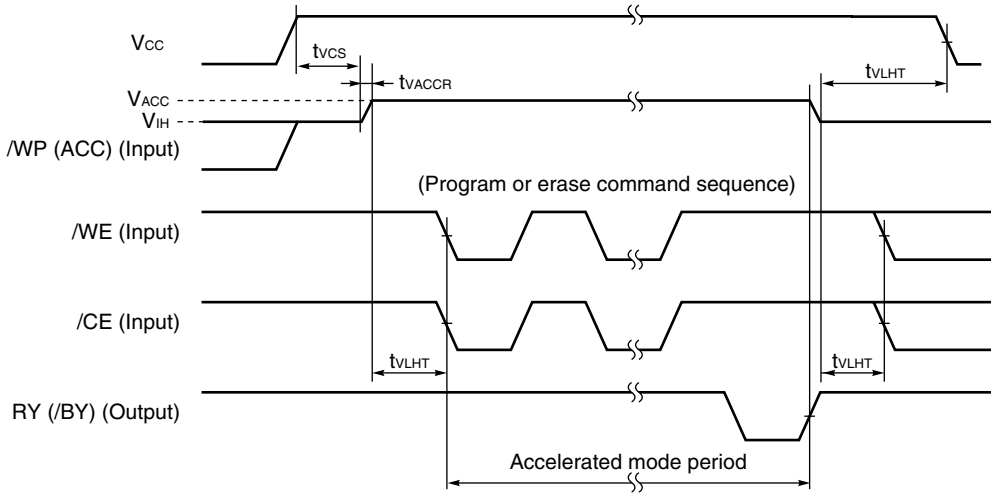


Figure 6-6. Dual Operation Timing Chart

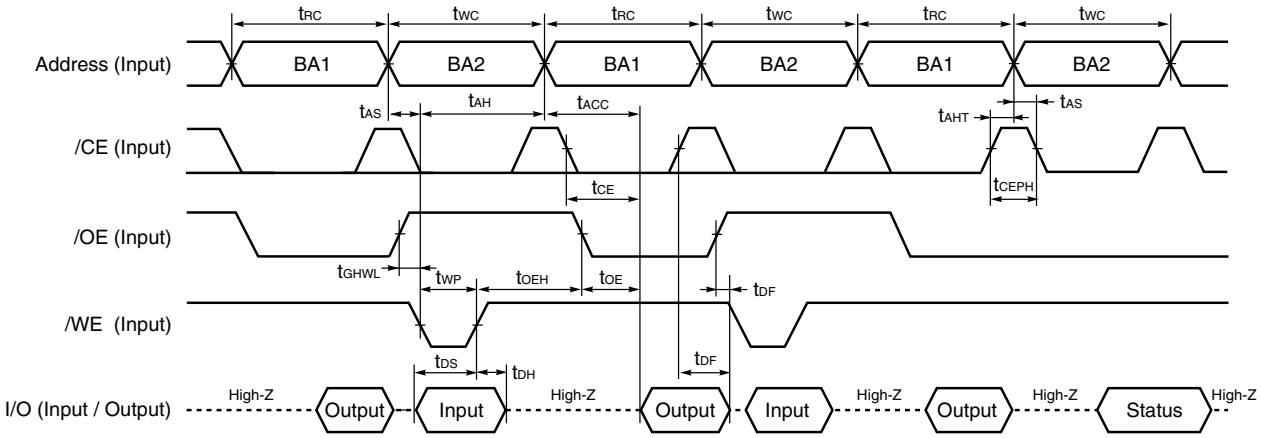
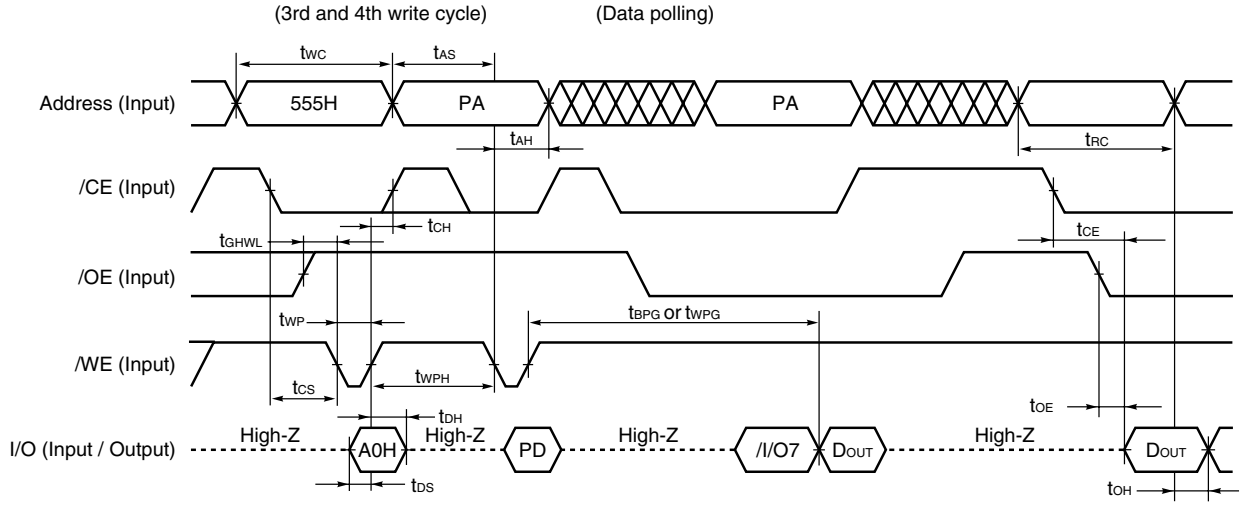


Figure 6-7. Write Cycle Timing Chart (/WE Controlled)

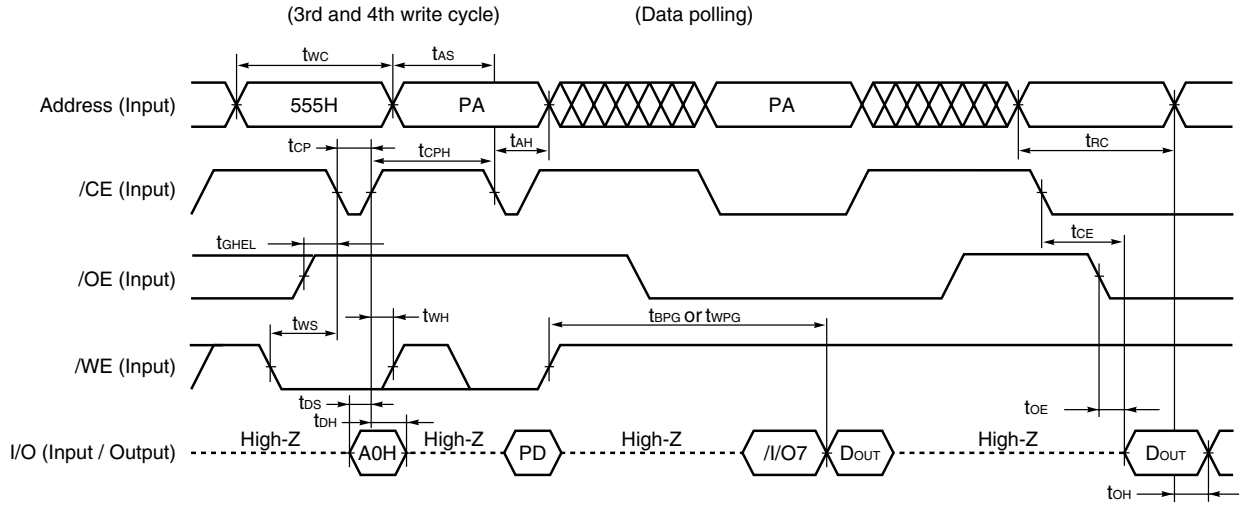


Remarks 1. This timing chart shows the last two write cycles among the program command sequence's four write cycles, and data polling.

2. This timing chart shows the WORD mode’s case. In the BYTE mode, address to be input is different from the WORD mode. See **Table 3-1. Command Sequence**.

3. PA : Program address
PD : Program data
/I/O7 : The output of the complement of the data written to the device.
DOUT : The output of the data written to the device.

Figure 6-8. Write Cycle Timing Chart (/CE Controlled)

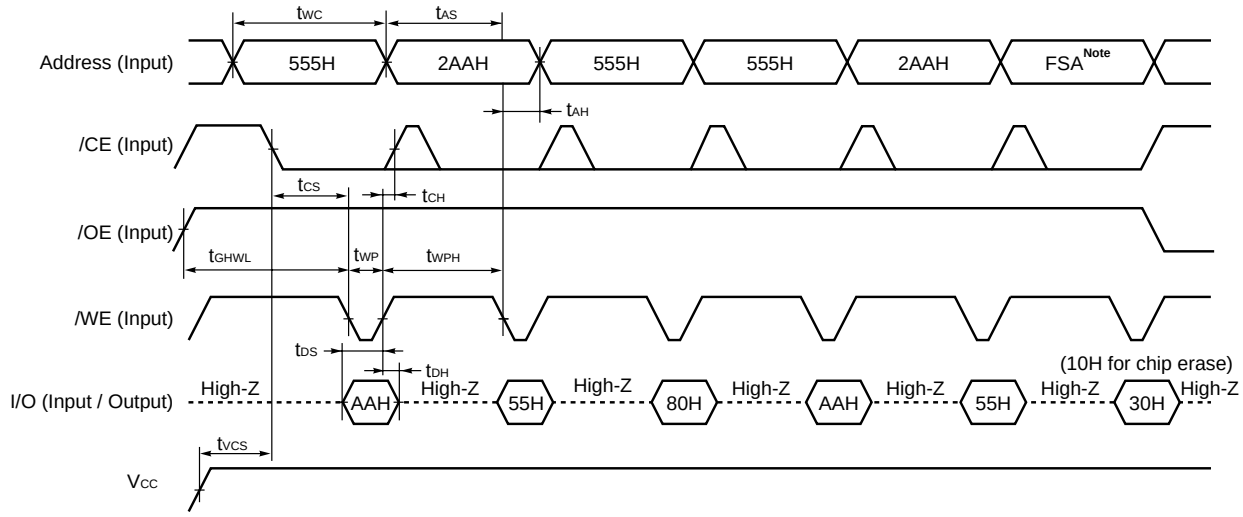


Remarks 1. This timing chart shows the last two write cycles among the program command sequence's four write cycles, and data polling.

2. This timing chart shows the WORD mode’s case. In the BYTE mode, address to be input is different from the WORD mode. See **Table 3-1. Command Sequence**.

3. PA : Program address
PD : Program data
/I/O7 : The output of the complement of the data written to the device.
DOUT : The output of the data written to the device.

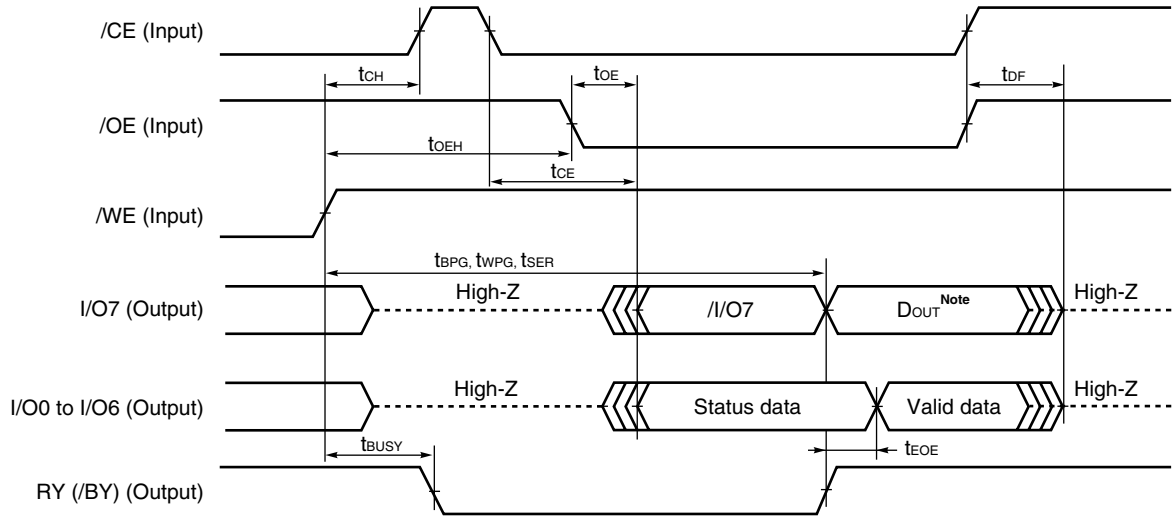
Figure 6-9. Sector / Chip Erase Timing Chart



★ **Note** FSA is the sector address to be erased. In the case of chip erase, input 555H.

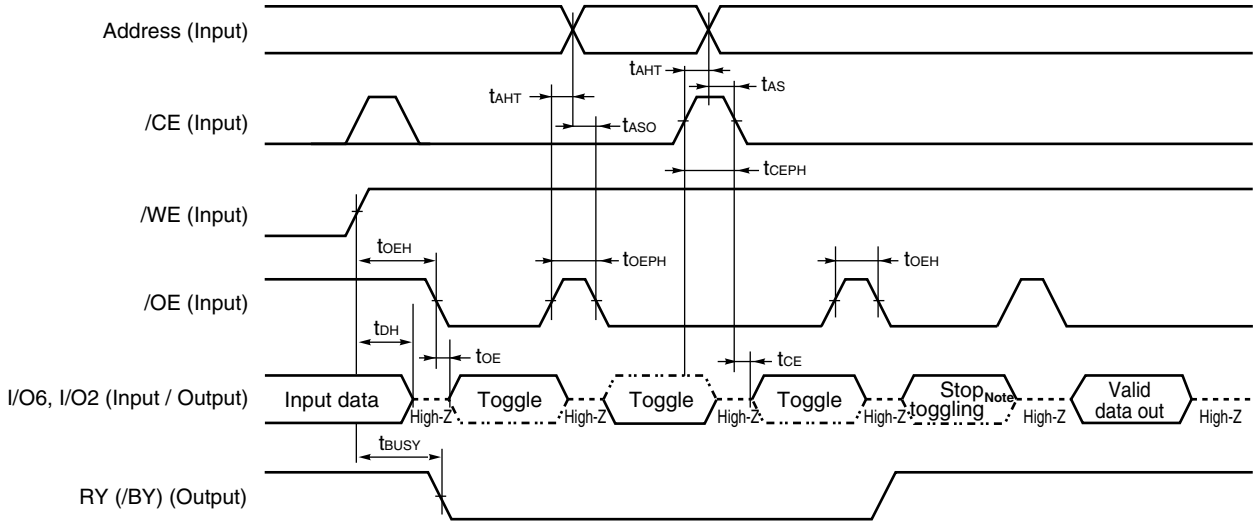
Remark This timing chart shows the WORD mode's case. In the BYTE mode, address to be input is different from the WORD mode. See **Table 3-1. Command Sequence**.

Figure 6-10. Data Polling Timing Chart



Note I/O7 = D_{OUT} : True value of program data (indicates completion of automatic program / erase)

Figure 6-11. Toggle Bit Timing Chart



Note I/O6 stops the toggle (indicates automatic program / erase completion).

Figure 6-12. I/O2 vs. I/O6 Timing Chart

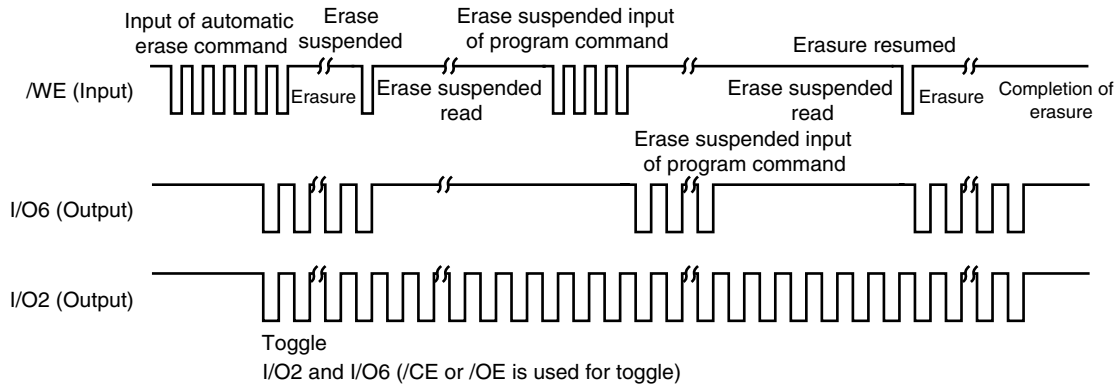


Figure 6-13. RY (/BY) (Ready / Busy) Timing Chart

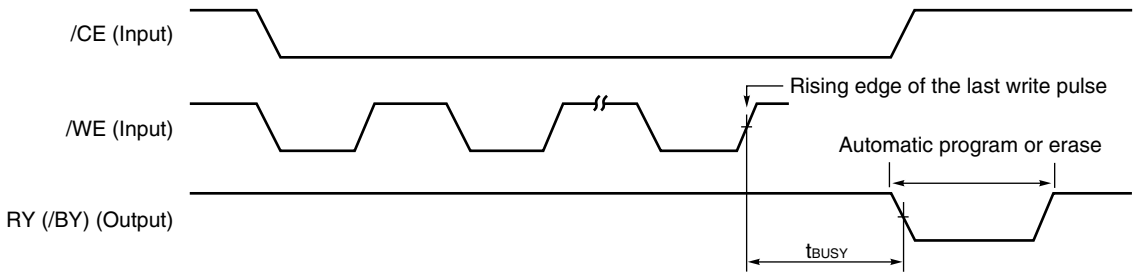


Figure 6-14. (/RESET) / RY (/BY) Timing Chart

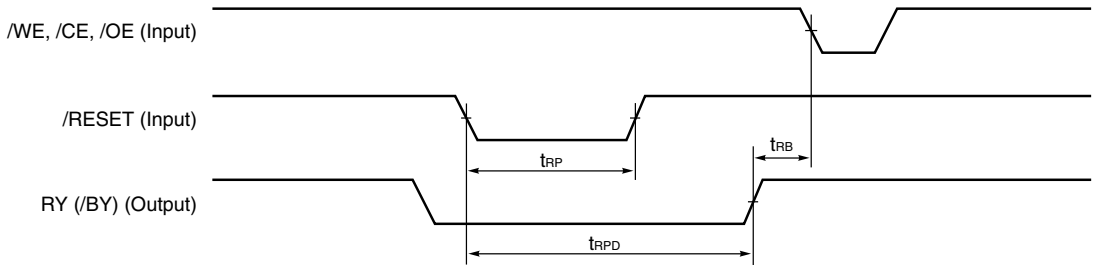


Figure 6-15. Write /BYTE Timing Chart

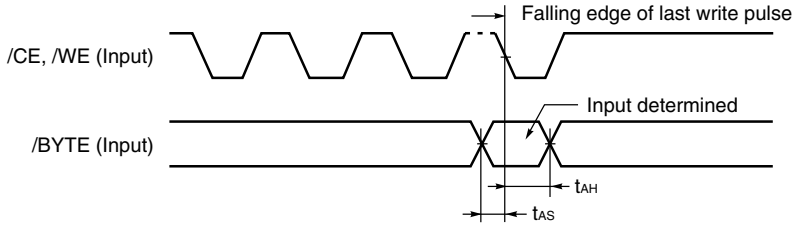


Figure 6-16. BYTE Mode Switching Timing Chart

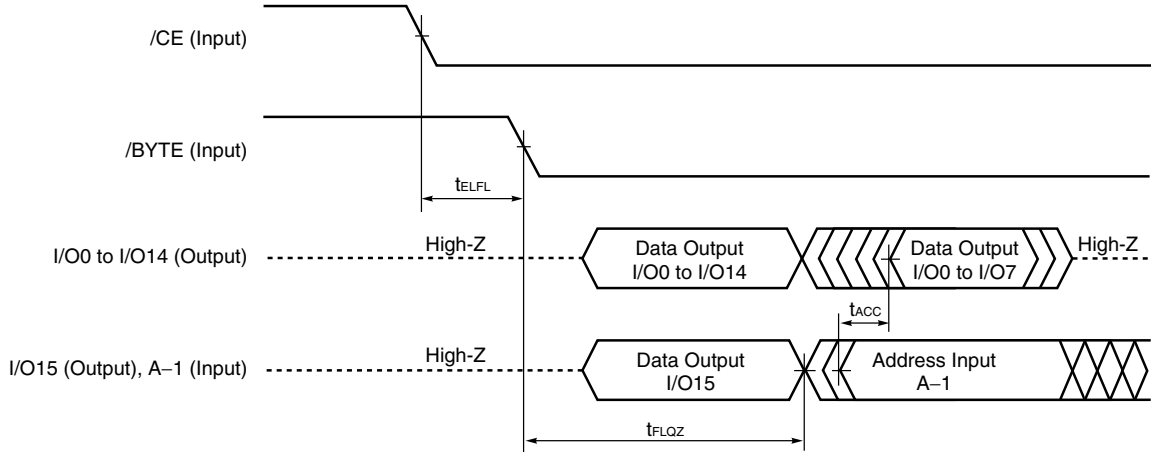
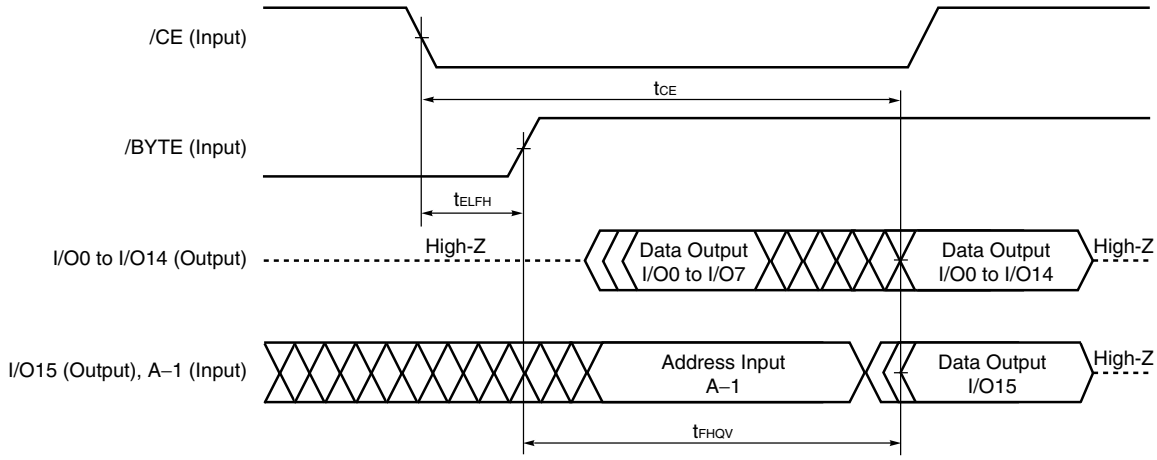


Figure 6-17. WORD Mode Switching Timing Chart



CHAPTER 7 FLOW CHARTS

For specifications, refer to the Data Sheet of each product.

Figure 7-1. Sector Group Protection Flow Chart

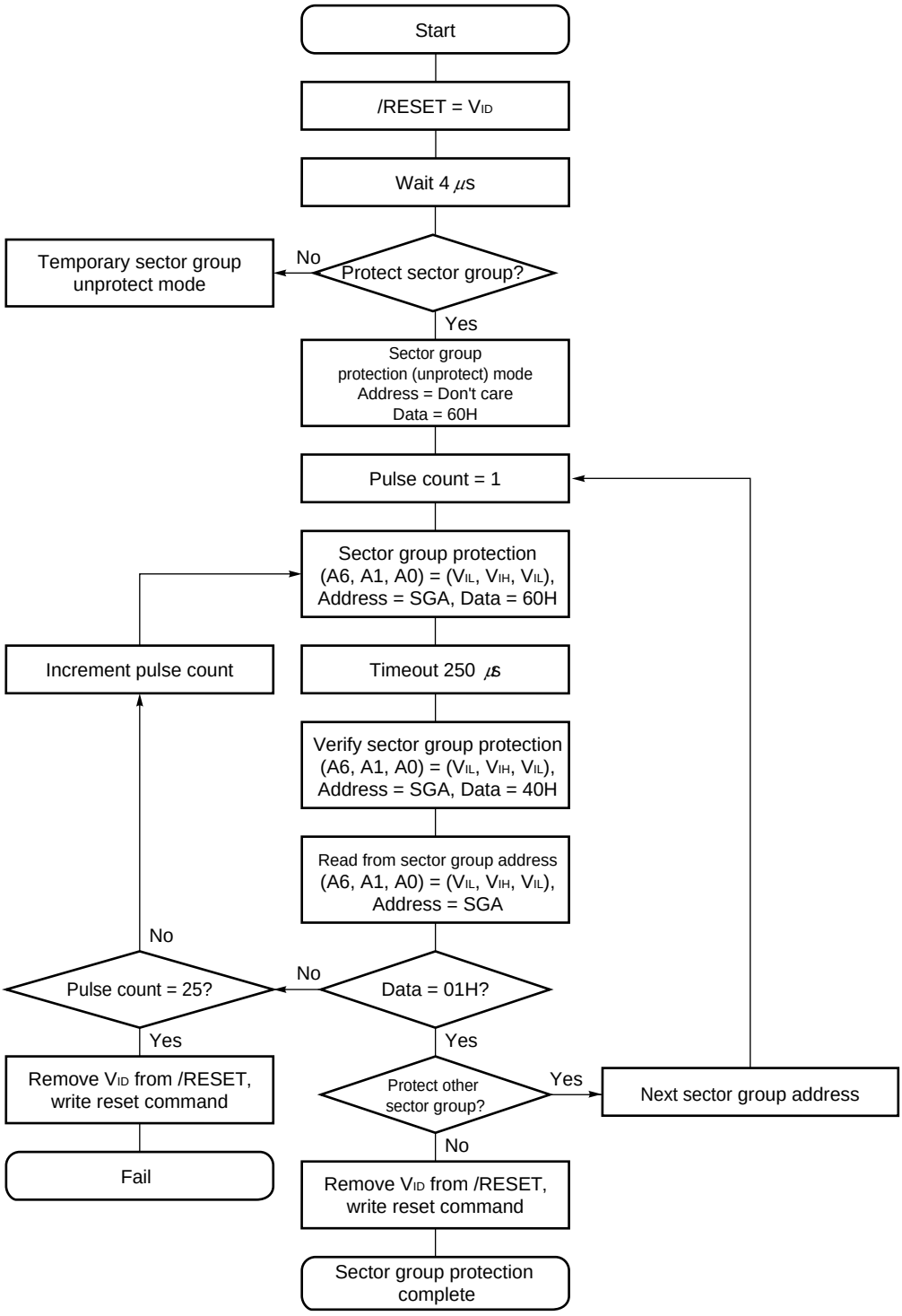


Figure 7-2. Program Flow Chart

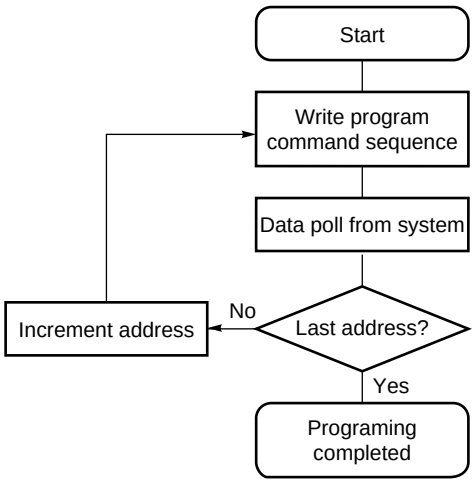


Figure 7-3. Sector / Chip Erase Flow Chart

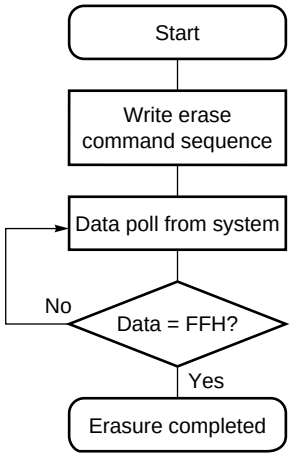
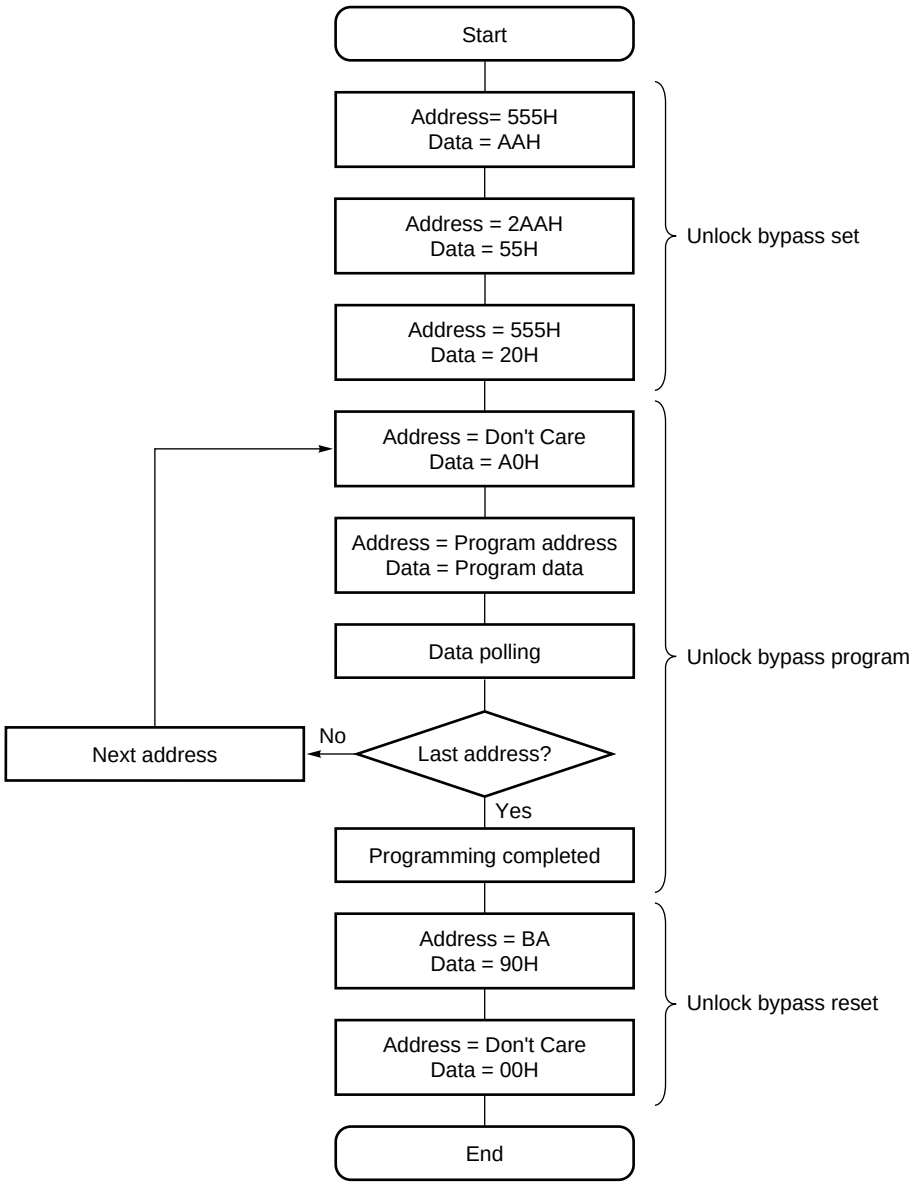


Figure 7-4. Unlock Bypass Flow Chart (WORD Mode)



Remark This flow chart shows the WORD mode's case. In the BYTE mode, address to be input is different from the WORD mode. See **Table 3-1. Command Sequence**.

Figure 7-5. Sector Group Unprotect Flow Chart

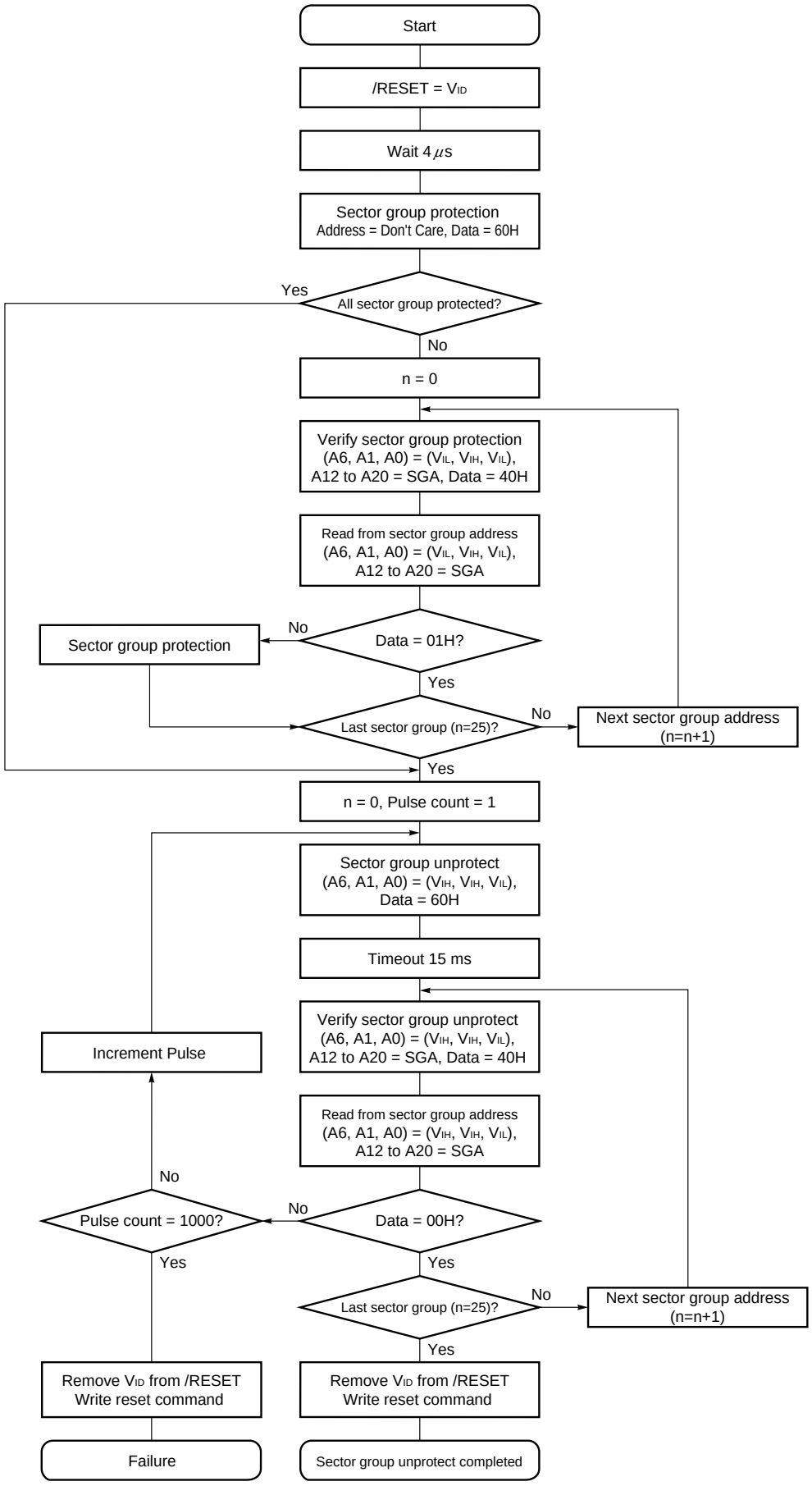


Figure 7-6. Data Polling Flow Chart

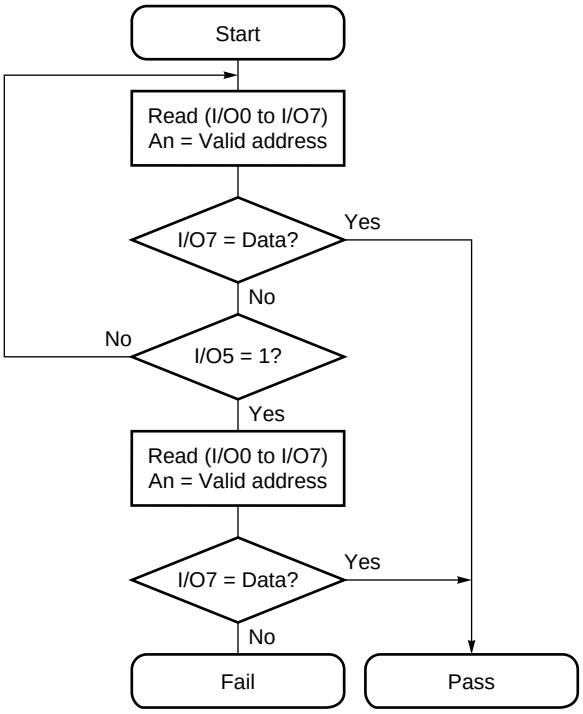
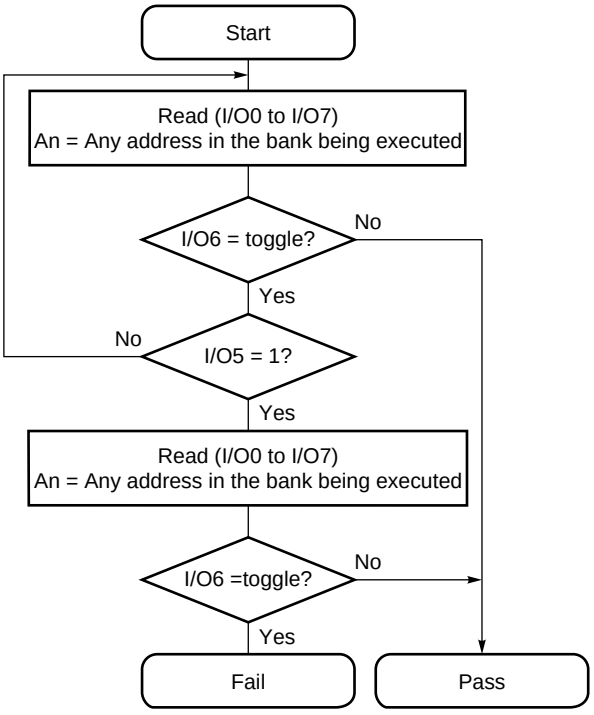


Figure 7-7. Toggle Bit Flow Chart



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