



Preliminary

UNIVERSAL SEMICONDUCTOR, INC.

USH5022

HIGH VOLTAGE

8-CHANNEL

ANALOG SWITCH

T-51-11

8-Channel High Voltage Analog Switch**Ordering Information**

Rev NR Sept 15, 92

$V_{PP} - V_{NN}$	28-lead Ceramic LCC*	28-lead Ceramic Side-braze	28-lead Plastic- Dip	28-lead J-leaded PLCC	Operating Temperature
270 V	USH5022-1L28	USH5022-1C28	USH5022-1P28	USH5022-1K28	0 to 70° C
220 V	USH5022-2L28	USH5022-2C28	USH5022-2P28	USH5022-2K28	0 to 70° C
160 V	USH5022-3L28	USH5022-3C28	USH5022-3P28	USH5022-3K28	0 to 70° C

Consult factory for industrial temp tested and Mil-Std processed parts

* Consult factory for cerdip and ceramic LCC availability

Features

- o Full Dielectric Isolation for High Reliability
- o 60 dB typical Output Off Isolation at 10 Mhz
- o Typical on resistance, R_{on} , is of 28 Ohms
- o CMOS Logic Circuitry for Low Power
- o Excellent Noise Immunity & Extremely Low I_{SOL}
- o On-chip Shift Register, and Latch Logic Circuitry
- o Fully Flexible High Voltage Supply Combinations
- o DC to 10 Mhz Analog Signal Frequency

General Description

This USH5022 is an 8-channel high voltage analog switch utilize Universal's Proprietary full oxide isolation process for switching high voltage analog signals. This device can be used in ultrasound imaging systems and other high voltage applications that requires flexible high voltage switching controlled by internal CMOS logic signals.

The USH5022 combines high voltage bidirectional DMOS switches with low power CMOS logic to provide efficient control of high voltage analog signals. Input data is shifted into an 8-bit register which can then be retained in an 8-bit latch. To minimize any clock feedthrough noise, Latch Enable Bar should be left high until all bits are clock in.

The USH5022-1, for example, is suitable for various combinations of high voltage supplies, e.g. +40V / -230V, or +135V / -135V, or +260V / -10V applications.

Absolute Maximum Ratings*

V_{DD} Logic Power Supply Voltage	0.5V to 18 V	Peak Analog Pulser Current/channel	3.0A
$V_{PP}-V_{NN}$ Supply Voltage	300 V	Storage Temperature	65°C to +150°C
V_{PP} Positive High Voltage Supply	0.5V to $V_{NN}+265$ V	Analog Pulser Range	$V_{AP}-V_{NN} = 0V$ to 240V
V_{NN} Negative High Voltage Supply	+0.5V to -235 V	Power Dissipation	Plastic Package 0.8W Ceramic Package 2.0W
Logic Input Voltage	0.5V to $V_{DD}+0.3V$		

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation under these conditions is not implied.

Continued operation to absolute maximum ratings may affect device reliability.

Electrical Characteristics(over recommended operating conditions, $V_{PP} = +110V$, $V_{NN} = -110V$, and $V_{DD} = 15V$ unless otherwise noted)***DC Characteristics**

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Parameters	Sym	0 °C min	0 °C max	25 °C min	25 °C typ	25 °C max	70 °C min	70 °C max	Units	Test Conditions
Small Signal Ron	R_{ONS}		30		26	30		32	ohms	$I_{SW} = 5mA$
Small Signal Ron	R_{ONS}		20		15	20		20		$I_{SW} = 200mA$
Delta Ron	ΔR_{ONS}		25		10	20		20	%	$I_{SW} = 5mA$
Large Signal Ron	R_{ONL}		100		70	100		100	ohms	$V_{AP} = V_{PP} - 10V$, $I_{SW} = 5mA$
Switch Off Leakage/SW	I_{SOL}		1		0.5	1		1	uA	$V_{AP} = V_{PP} - 10V/V_{NN} - 10V$
DC Offset Switch Off	I_{DCOFF}		200		100	200		200	mV	$R_L = 100K$
DC Offset Switch On	I_{DCON}		300		100	300		300	mV	$R_L = 100K$
Pos. HV Supply Current	I_{PPOFF}				10	50			uA	ALL SWS OFF
Neg. HV Supply Current	I_{NNOFF}				-10	-50			uA	ALL SWS OFF
Pos. HV Supply Current	I_{PPOON}				10	50			uA	ALL SW ON $I_{SW} = 5ma$
Neg. HV Supply Current	I_{NNON}				-10	-50			uA	ALL SW ON $I_{SW} = 5ma$
Analog Pulse Pk Current	I_{PAP}		2		1.5	2		2	A	V_{AP} Duty Cycle < 0.1 %
Output Switch Frequency	f_{SW}		50			50		50	Khz	Duty Cycle = 50 %
I_{PP} Ave. Supply Current	I_{PPAV}				TBD					$f_{SW} = 50$ Khz
I_{NN} Ave. Supply Current	I_{NNAV}				TBD					$f_{SW} = 50$ Khz
V_{DD} Ave. Current	I_{DDAV}		6			6		6	mA	$f_{CLK} = 3$ Mhz
V_{DD} Quiescent Current	I_{DDQ}		10			10		10	uA	
Data Out Source Current	I_{SOR}	1.8		1.8			1.8		mA	$V_{out} = V_{DD} - 0.7V$
Data Out Sink Current	I_{SINK}	-1.8		-1.8			-1.8		mA	$V_{out} = 0.7V$

AC Characteristics

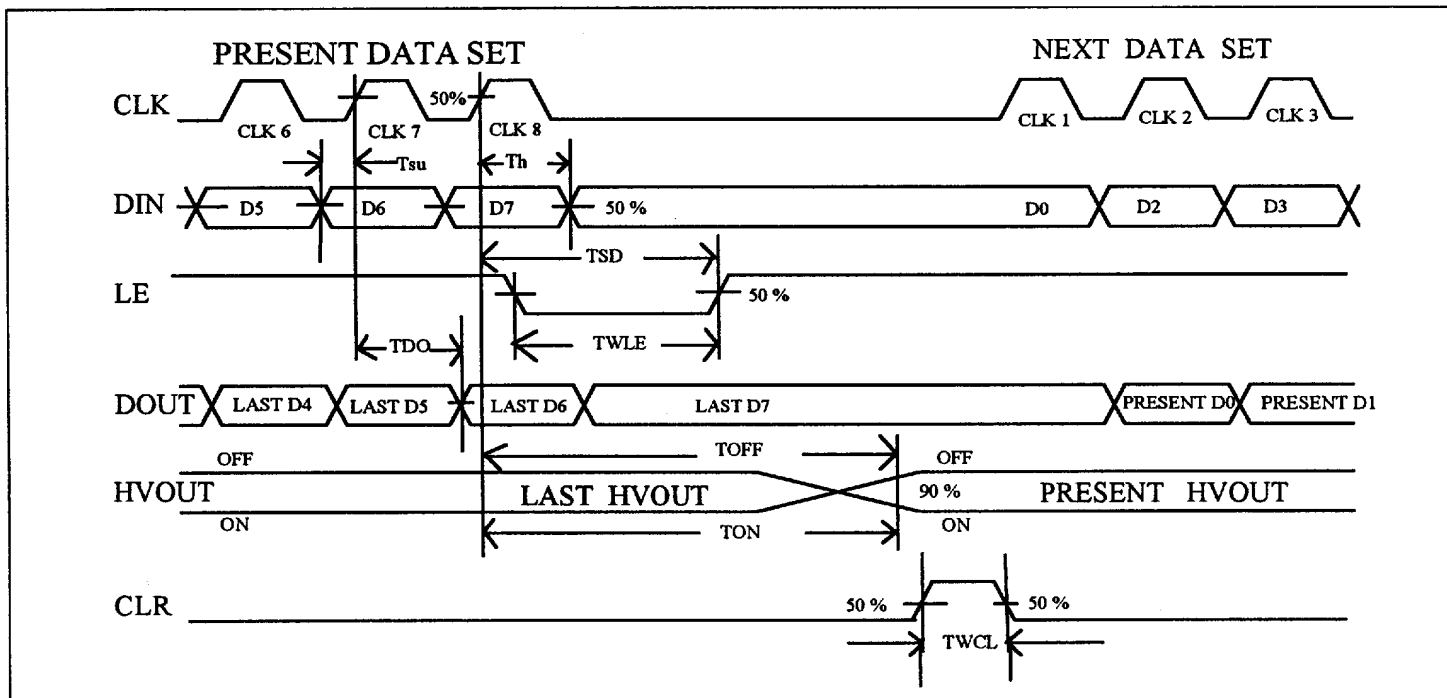
Parameters	Sym	0 °C min	0 °C max	25 °C min	25 °C typ	25 °C max	70 °C min	70 °C max	Units	Test Conditions
Set Up Time Before LE Rises	t_{SD}	150		150			150		ns	
LE Pulse Width	t_{WLE}	50		50			50		ns	
Clock to Dout Delay Time	t_{DO}		300			300		300	ns	
Din to Clock Set Up Time	t_{SU}	30		30			30		ns	
Din to Clock Hold Time	t_H	30		30			30		ns	
Minimum CL Pulse Width	t_{WCL}	5		5			5		us	
Logic Input Rise and Fall Time	t_R / t_F	10	200	10	10	200	10	200	ns	
Max. Logic Clock Frequency	f_{CLK}		5			5		5	Mhz	
CLK to HVout Turn On Time	t_{ON}		5		2	5		5	us	$R_L = 10K$ ohm
CLK to HVout Turn Off Time	t_{OFF}		5		3	5		5	us	$R_L = 10K$ ohm
Channel to Channel Cross-talk	K_{CR}	-60		-60			-60		dB	$f_{VIN} = 5Mhz / 50$ ohm load
Individual Channel Off-Isolation	K_O	-45		-45			-45		dB	$f_{VIN} = 5Mhz / 50$ ohm load
Maximum Positive Noise Glitch	V_{GP}		500			500		500	mV	680 ohms // 220 pf load
Maximum Negative Noise Glitch	V_{GN}		-1.2			-1.2		-1.2	V	680 ohms // 220 pf load
Analog Pulser Rise and Fall Time	V_{APDVT}				12				V/ns	$ V_{AP} = 180V$ in 15 ns
Analog Pulser Max Bandwidth	f_{VAP}		10			10		10	Mhz	
Logic Input Capacitance	C_A				3				pF	0V, 1 Mhz
Switch Off Capacitance to GND	$C_{SG(OFF)}$				20				pF	0V, 1 Mhz
Switch On Capacitance to GND	$C_{SG(ON)}$				50				pF	0V, 1 Mhz
Input to HVout Capacitance	$C_{DS(OFF)}$				T.B.D.				pF	0V, 1 Mhz

Recommended Operating Conditions

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Symbol	Parameters	USH5022-1	USH5022-2	USH5022-3	Other conditions
V_{DD}	Logic Power Supply Voltage	10V to 15.5V	10V to 15.5V	10V to 15.5V	
V_{PP} -Mode A	Positive High Voltage Supply	40V	40V	40V	
V_{NN} -Mode A	Negative High Voltage Supply	-230V	-180V	-120V	
V_{AP} -Mode A	Analog Pulser Voltage Range	$-220 < V_{AP} < 30V$	$-170 < V_{AP} < 30V$	$-110 < V_{AP} < 30V$	$V_{AP} = V_{PP} - 10V / V_{NN} + 10V$
V_{PP} -Mode B	Positive High Voltage Supply	135V	110V	80V	
V_{NN} -Mode B	Negative High Voltage Supply	-135V	-110V	-80V	
V_{AP} - Mode B	Analog Pulser Voltage Range	$-125V < V_{AP} < 125V$	$-100V < V_{AP} < 100V$	$-70V < V_{AP} < 70V$	$V_{AP} = V_{PP} - 10V / V_{NN} + 10V$
V_{PP} -Mode C	Positive High Voltage Supply	260V	210V	150V	
V_{NN} -Mode C	Negative High Voltage Supply	-10V	-10V	-10V	
V_{AP} -Mode C	Analog Pulser Voltage Range	$0V < V_{AP} < 250V$	$0V < V_{AP} < 200V$	$0V < V_{AP} < 140V$	$V_{AP} = V_{PP} - 10V / V_{NN} + 10V$
V_{IH}	Logic Input High Level				
V_{IL}	Logic Input Low Level				
Power Sequence	GND, V_{DD} , CLKS, V_{NN} , V_{PP}	SAME	SAME	SAME	$V_{NN} > -10V$

Timing Diagram



LOGIC TRUTH TABLE

D0	D1	D2	D3	D4	D5	D6	D7	LE	CL	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	OFF							
H								L	L	ON							
	L							L	L		OFF						
	H							L	L		ON						
		L						L	L			OFF					
		H						L	L			ON					
			L					L	L				OFF				
			H					L	L				ON				
				L				L	L					OFF			
				H				L	L					ON			
					L			L	L						OFF		
					H			L	L						ON		
						L		L	L							OFF	
						H		L	L							ON	
							L	L	L								OFF
							H	L	L								ON
X	X	X	X	X	X	X	X	H	L	HOLDS PREVIOUS STATE							
X	X	X	X	X	X	X	X	X	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF

Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L → H transition CLK.
3. The Switches go to a state retaining their present condition at the rising edge of LE. When LE is low the shift register data flows through the latch.
4. Dout is high when switch 7 is on.
5. Shift register clocking has no effect on the switch states if LE is H.
6. The clear input overrides all other inputs.

Description of Operation

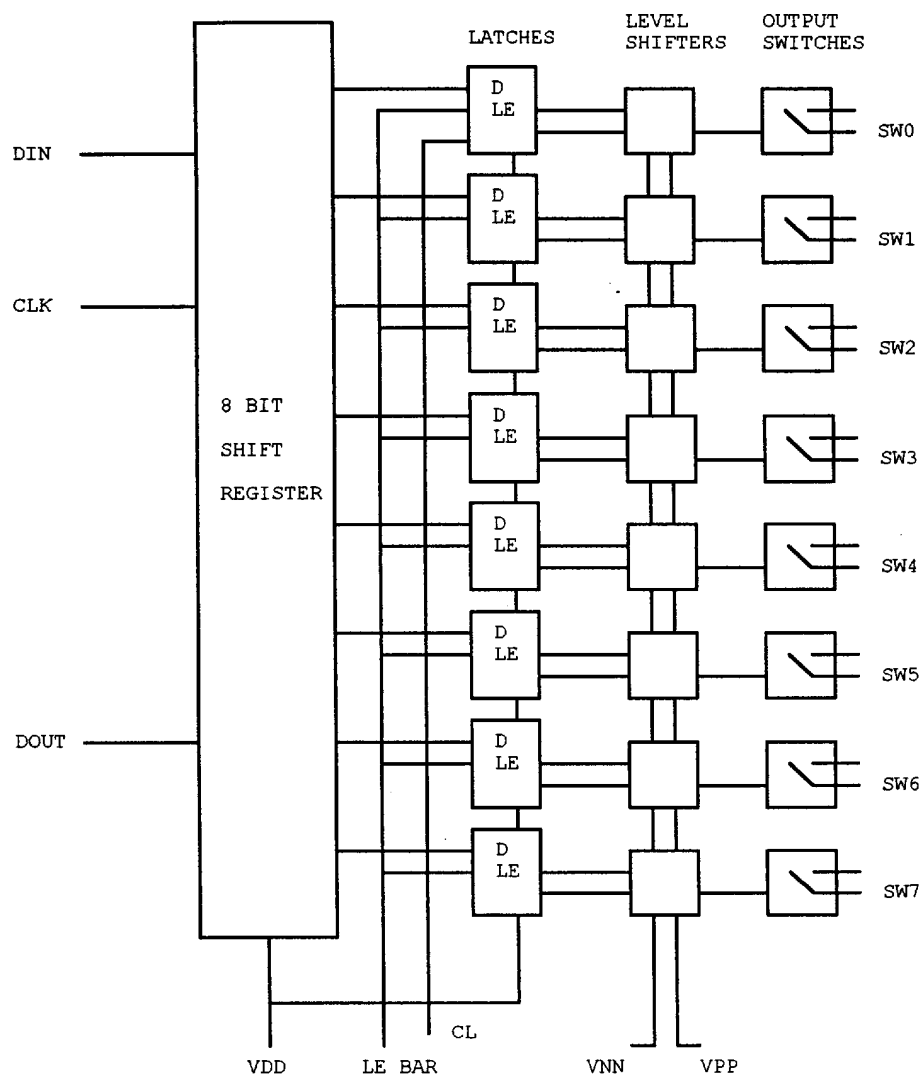
The USH5022 is a High Voltage Integrated Circuit (HIVIC) that contains eight independent high voltage bi-directional switches and the CMOS logic necessary to interface them to a CMOS environment. This HIVIC is designed to switch various analog signals into capacitive loads, and it is designed to conduct current pulses of 2A with 0.1% duty cycle.

The switches (SW0-SW7) are controlled by the serial data on DIN, the shift register clock input (CLK), and the data transfer enable (LE). (See timing diagram and logic truth table). Serial data on line DIN is clocked into the eight-staged static shift registers.

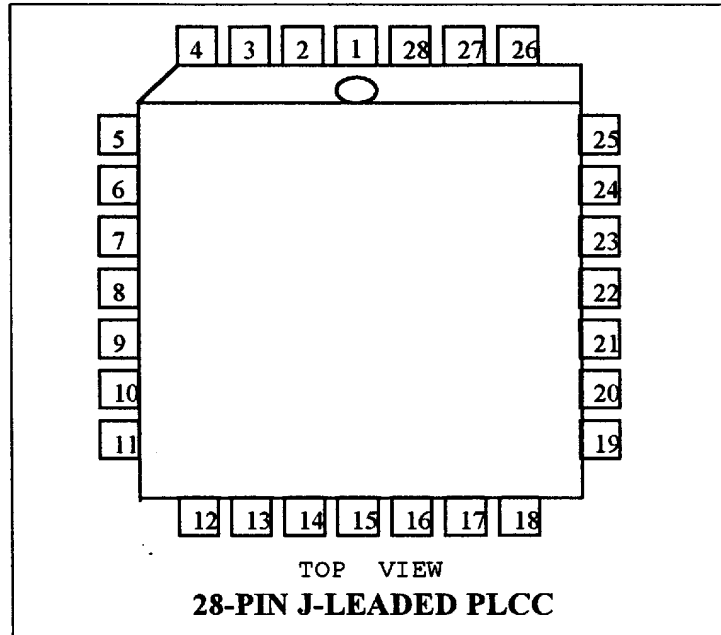
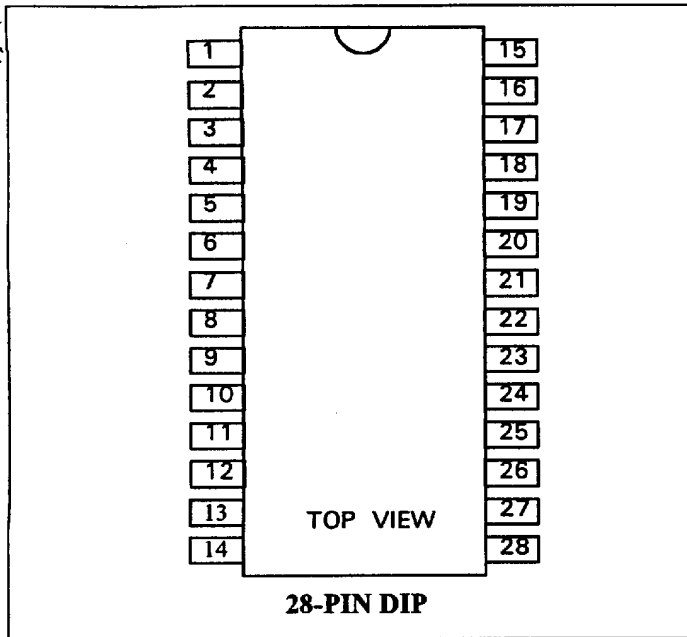
The data in the shift register is transferred to the latches by latch enable LE. When LE is low, the shift register data flows through the latch and controls the state of the switch. When CL is high, it turns all high voltage outputs off.

Pin Definitions

Din	Serial Data Input to Shift Register
CLK	Serial Shift Clock
LE	Parallel Transfer Enable from Shift Register to Latches
Dout	Serial Data Out of Eighth Stage of S.R.
SW0-7	Eight Pairs of High Voltage Lines for Analog Signal Switching
VPP	Positive High Voltage Supply for the Level Shift Circuits
VNN	Negative High Voltage Supply for the Level Shift Circuits
VCC	+ 15 V Logic Supply Pin
CL	Logic control that shuts all HVOUTS all 'OFF'

Logic Diagram

Package and Pin Configurations



28-Pin Dips

<u>Pin</u>	<u>Function</u>	<u>Pin</u>	<u>Function</u>
1	SW3A	15	N/C
2	SW3B	16	DIN
3	SW2A	17	CLK
4	SW2B	18	LE BAR
5	SW1A	19	CL
6	SW1B	20	DOUT
7	SW0A	21	SW7B
8	SW0B	22	SW7A
9	VPP	23	SW6B
10	VNN	24	SW6A
11	N/C	25	SW5B
12	GND	26	SW5A
13	VDD	27	SW4B
14	N/C	28	SW4A

28-Pin J-leaded PLCC

<u>Pin</u>	<u>Function</u>	<u>Pin</u>	<u>Function</u>
1	SW3A	15	N/C
2	SW3B	16	DIN
3	SW2A	17	CLK
4	SW2B	18	LE BAR
5	SW1A	19	CL
6	SW1B	20	DOUT
7	SW0A	21	SW7B
8	SW0B	22	SW7A
9	VPP	23	SW6B
10	VNN	24	SW6A
11	N/C	25	SW5B
12	GND	26	SW5A
13	VDD	27	SW4B
14	N/C	28	SW4A