9-BIT, 8-CELL DIGITAL FILTER PROCESSOR

FEATURES

- 8 filter cells
- Up to 30 MHz sample rate
- 9-bit two's complement coefficients and signal data
- 26-bit accumulator per stage
- Filter lengths over 500 taps
- Expandable coefficient size, data size and filter length
- Decimation by 2, 3, or 4
- Low power, high-speed CMOS

APPLICATIONS

- 1-D and 2-D FIR filters
- Correlation/convolution
- Adaptive filters
- Matrix multiplication
- Complex multiply-add
- Butterfly computation
- Sample rate converters
- Digital video and audio
- Radar/Sonar
- Echo cancellation

FUNCTIONAL DESCRIPTION

The ZR33891 (Figure 1) is a video-speed Digital Filter Processor (DFP) designed to efficiently implement vector operations such as FIR digital filters. It is comprised of eight filter cells cascaded internally, all in a single integrated circuit. Each filter cell contains a 9 x 9 bit two's complement multiplier, three decimation registers and a 26-bit accumulator. The ZR33891 has a maximum sample rate of 30 MHz. The effective multiply-accumulate (MAC) rate is 240 MHz.

Several ZR33891 DFP's can be configured to process expanded coefficient and data size. Multiple DFP's can be cascaded for larger filter lengths without degrading the sample rate, or, a single DFP can process larger filter lengths at less than 30 MHz with multiple passes. The architecture permits processing filter lengths of over 500 taps with the guarantee of no overflows. In practice, with typical coefficients, even larger filter lengths are possible. The DFP "provides" for 8-bit unsigned or 9-bit two's complement arithmetic, for coefficients and signal data.

Each DFP filter cell contains three resampling or decimation registers which permit output sample rate reduction by 2, 3 or 4. These registers also provide the capability to perform 2-D operations such as matrix multiplication and spatial correlations /convolutions for image processing applications.

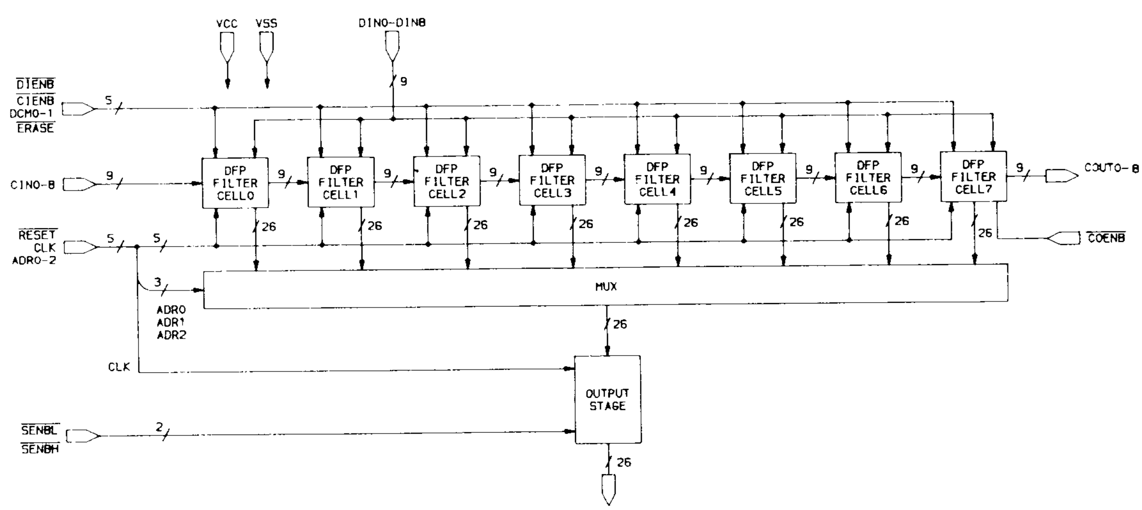


FIGURE 1. ZR33891 BLOCK DIAGRAM

INTERFACE SIGNAL DESCRIPTION

Name	Function
Vcc	+5V power supply input
Vss	Power supply ground input.
CLK	The CLK input provides the DFP system sample clock.
DIN0-8	These nine lines are the data sample input bus. Nine-bit data samples are synchronously loaded through these pins to the data input register (X-REG) of each filter cell of the DFP simultaneously. The $\overline{\text{DIENB}}$ signal enables loading, which is synchronous on the rising edge of the clock signal. The data samples can be either 9-bit two's complement or 8-bit unsigned values. For 9-bit two's complement values, DIN8 is the sign bit. For 8-bit unsigned values, DIN8 must be held at logical zero.
$\overline{\text{DIENB}}$	A low on this input enables the data sample input bus (DIN0-8) to all the filter cells. A rising edge of the CLK signal occurring while $\overline{\text{DIENB}}$ is low will load the X register of every filter cell with the 9-bit value present on DIN0-8. A high on this input forces all the bits of the data sample input bus to zero; a rising CLK edge when $\overline{\text{DIENB}}$ is high will load the X register of every filter cell with all zeros. This signal is latched inside the device, delaying its effect by one clock internal to the device. Therefore it must go low during the clock cycle immediately preceding presentation of the desired data on the DIN0-8 inputs.
CIN0-8	These nine lines are used to input the coefficients. The coefficients are synchronously loaded into the coefficient register (C-REG) of filter CELL0, if a rising edge of CLK occurs while $\overline{\text{CIENB}}$ is low. The coefficients can be either 9-bit 2's complement or 8-bit unsigned values. For 9-bit 2's complement values, CIN8 is the sign bit. For 8-bit unsigned values, CIN8 must be held at logical zero.
$\overline{\text{CIENB}}$	A low on this input enables the C-REG and the decimation registers (D_1 D_2 D_3-REG) of every filter cell according to the state of the DCM0-1 inputs. A rising edge of the CLK signal occurring while $\overline{\text{CIENB}}$ is low will load the C register and

Name	Function
$\overline{\text{CIENB}}$ (cont.)	appropriate D registers with the coefficient data present at their inputs. This provides the mechanism for shifting the coefficients from cell to cell through the device. A high on this input freezes the contents of the C register and the D registers, ignoring the CLK signal. This signal is latched internal to the DFP. Therefore it must go low during the clock cycle immediately preceding presentation of the desired coefficient on the CIN0-8 inputs.
COUT0-8	These nine three-state outputs are used to output the coefficients from filter CELL7. These outputs are enabled by the $\overline{\text{COENB}}$ signal low. These outputs may be tied to the CIN0-8 inputs of another DFP to cascade DFP's for longer filter lengths.
$\overline{\text{COENB}}$	A low on the $\overline{\text{COENB}}$ input enables the COUT0-8 outputs. A high on this input places all these outputs in their high impedance state.
DCM0-1	These two inputs determine the use of the internal decimation registers as follows: DCM1 DCM0 Decimation Function 0 0 Decimation registers not used 0 1 One decimation register is used 1 0 Two decimation registers are used 1 1 Three decimation registers are used The coefficients pass from cell to cell with a delay determined by the number of decimation registers used. When no decimation registers are used, coefficients move from cell to cell with no added delay. When one decimation register is used, coefficients move from cell to cell with a delay of one clock, etc. These signals are latched internal to the device.
SUM0-25 (SUM0-24 in LCC)	These 26 three-state outputs are used to output the results of the internal filter cell computations selected by ADR0-2. The signals $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ enable the most significant and least significant bits of the SUM0-25 result respectively. Both $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ may be enabled simultaneously if the system has a 26-bit or larger bus.

INTERFACE SIGNAL DESCRIPTION

Name	Function
SUMO-25 (cont)	However, individual enables are provided to facilitate use with a 16-bit bus. **NOTE:** The ZR33891 in a leadless chip carrier (LCC) package has only 25 SUM outputs, SUM0-24.
$\overline{\text{SENBH}}$	A low on this input enables result bits SUM16-25. A high on this input places these outputs in their high impedance state.
$\overline{\text{SENBL}}$	A low on this input enables result bits SUM0-15. A high on this input places these outputs in their high-impedance state.
ADR0-2	These three inputs select the one cell whose accumulator will be read through the output bus (SUM0-25). They also determine which accumulator will be cleared when $\overline{\text{ERASE}}$ is low. If the ADR0-2 lines remain at the same address for more than one clock, the output at SUM0-25 will not change to reflect any subsequent accumulator updates in the addressed cell. Only the result available during the first clock, when ADR0-2 selects the cell, will be output. This does not hinder normal operation since the ADR0-2 lines are changed sequentially. This feature facilitates the interface with slow memories where the output is required to be fixed for more than one clock.

Name	Function
Vss (SHADD)	Constant low for proper function, as the SHADD operation is no longer supported.
$\overline{\text{RESET}}$	A low on this input synchronously clears all the internal registers, except the cell accumulators. It can also be used with $\overline{\text{ERASE}}$ to simultaneously clear all the accumulators. This signal is latched in the DFP.
$\overline{\text{ERASE}}$	A low on this input synchronously clears the cell accumulator selected by the ADR0-2 signals. If $\overline{\text{RESET}}$ is also low simultaneously, all cell accumulators are cleared. This signal is latched in the DFP.

ZR33891 FILTER CELL

A 9-bit coefficient (CIN0-8) enters each cell through the C register on the left and exits the cell on the right as signals COUT0-8 (Figure 2). The coefficients may move directly from the C register to the output, exiting the cell on the clock following its entrance. When decimation is selected, the coefficient exit is delayed by 1, 2 or 3 clocks by passing through one or more decimation registers (D1, D2 or D3).

The combination of D registers through which the coefficient passes is determined by the state of DCM0 and DCM1. The output signals (COUT0-8) are connected to the CIN0-8 inputs of the next cell to its right. The COENB input signal enables the COUT0-8 outputs of the right-most cell to the COUT0-8 pins of the device.

The C and D registers are enabled for loading by CIENB. Loading is synchronous with CLK when CIENB is low. Note that CIENB is latched internally. It enables the register for loading after the next CLK following the onset of CIENB low. Actual loading occurs on the second CLK following the onset of CIENB low. Therefore CIENB must go low during the clock cycle immediately preceding presentation of the coefficient on the CIN0-8 inputs. In most basic FIR operations, CIENB will be low throughout the process, so this latching and delay sequence is only important during the initialization phase. When CIENB is high, the coefficients are frozen.

These registers are cleared synchronously under control of RESET, which is latched and delayed exactly like CIENB.

The output of the C register (C<0:8>) is one input to the 9x9 multiplier.

The other input to the 9x9 multiplier comes from the output of the X register. This register is loaded with a data sample from the device input signals DIN0-8.

The X register is enabled for loading by DIENB. Loading is synchronous with CLK when DIENB is low. Note that DIENB is latched internally. It enables the register for loading after the next CLK following the onset of DIENB low. Actual loading occurs on the second CLK following the onset of DIENB low. Therefore DIENB must go low during the clock cycle immediately preceding presentation of the data sample on the DIN0-8 inputs. In most basic FIR operations, DIENB will be low throughout the process, so this latching and delay sequence is only important during the initialization phase. When DIENB is high, the X register is loaded with all zeros.

The multiplier is pipelined and is modeled in Figure 2 as a multiplier core followed by two pipeline registers, M0-REG and M1-REG. The multiplier output is sign extended and input as one operand of the 26-bit adder. The other adder operand is the output of the 26-bit accumulator. The adder output is loaded synchronously into both the accumulator and the output register, T-REG.

The T-REG loading is disabled by the cell select signal, CELLn, where n is the cell number. The cell select is decoded from the ADR0-2 signals to generate the T-REG load enable. The cell select is inverted, delayed and applied as the load enable to the T-REG, so that the T-REG is loaded whenever the cell is not selected. The purpose of the T-REG is to hold the result of a sum-of-products calculation during the clock when the accumulator is cleared to prepare for the next sum-of-products calculation. This allows continuous accumulation without wasting clocks.

The accumulator is loaded with the adder output every clock unless it is cleared. It is cleared synchronously in two ways. When RESET and ERASE are both low, the accumulator is cleared along with all other registers on the device. Since ERASE and RESET are latched internally, clearing occurs on the second CLK following the onset of both ERASE and RESET low.

The second accumulator clearing mechanism clears a single accumulator in a selected cell. The cell select signal, CELLn, decoded from ARD0-2 and the ERASE signal, enable clearing of the accumulator on the next CLK.

The ERASE and RESET signals clear the DFP internal registers and states as follows:

ERASE	RESET	CLEARING EFFECT
1	1	No clearing occurs, internal state remains the same
1	0	Only Reset active. All registers except accumulators are cleared, including the internal pipeline registers.
0	1	Only Erase active. The accumulator whose address is given by the ADR0-2 inputs is cleared.
0	0	Both Reset and Erase active. All accumulators as well as all other registers are cleared.

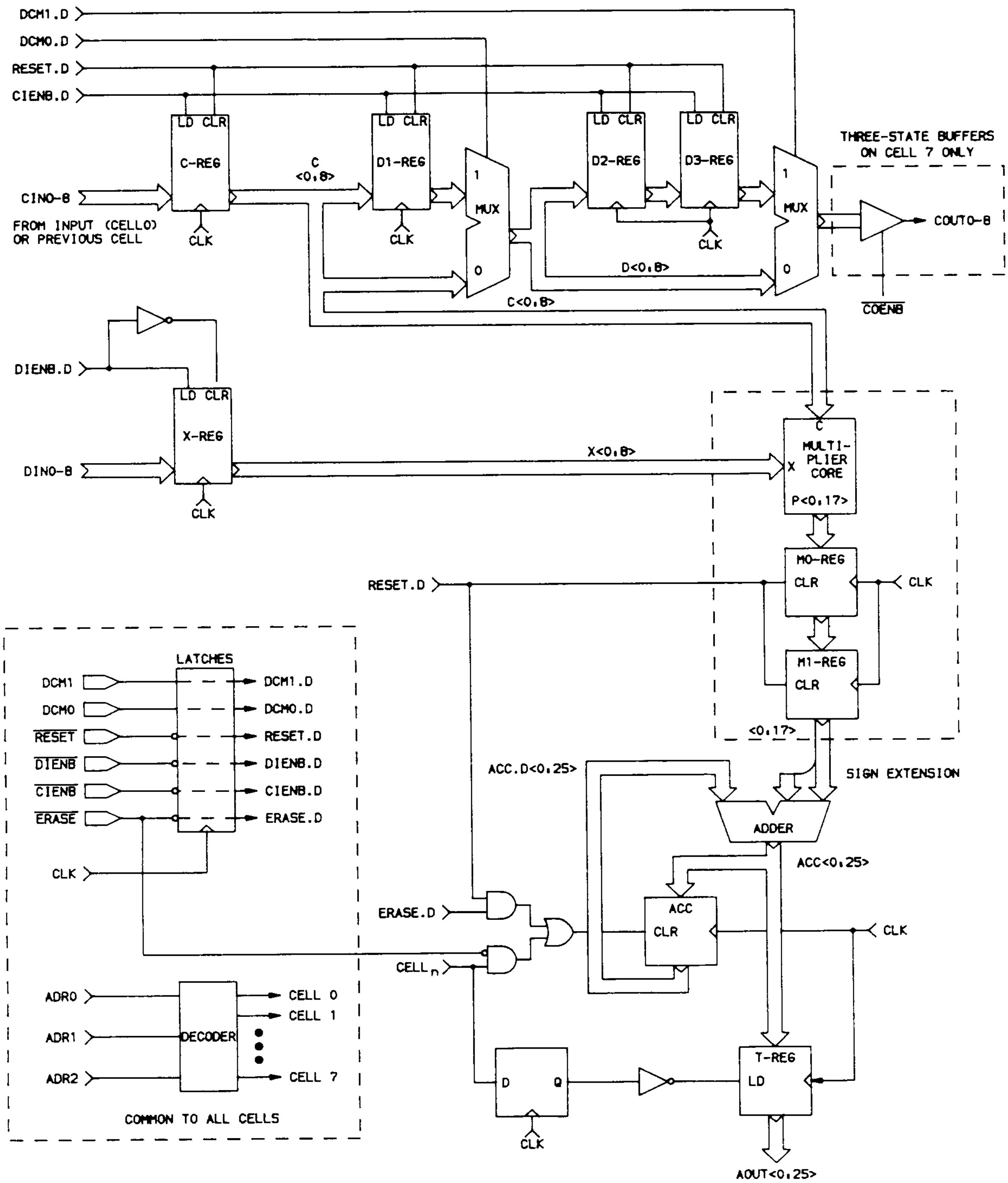


FIGURE 2. ZR33891 FILTER CELL

ZR33891 OUTPUT STAGE

The output stage consists of a cell result multiplexer and a 26-bit three-state driver stage. (Figure 3)

The cell result mux selects the contents of the filter cell accumulator addressed by ADR0-2. If the ADR0-2 lines remain at the same address for more than one clock, the output at SUM0-25 will not change to reflect any subsequent accumulator updates in the addressed cell. Only the result available during the first clock when ADR0-2 selects the cell will be output. This does not hinder normal FIR operation since the ADR0-2 lines are changed sequentially. This feature facilitates the interface with slow memories where the output is required to be fixed for more than one clock.

The clock input to the cell result mux is used for synchronization and does not introduce an extra delay.

The SUM0-25 output bus is controlled by the $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ signals. A low on $\overline{\text{SENBL}}$ enables bits SUM0-15. A low on $\overline{\text{SENBH}}$ enables bits SUM16-25. Thus all 26 bits can be output simultaneously if the external system has a 26-bit or larger bus. If the external system bus is only 16 bits, the bits can be enabled in two groups of 16 and 10 bits.

Also, the output may be arbitrarily scaled and truncated by connecting the proper output bits to output bus lines. For example, assume a filter kernel that with expected input signals, will produce only 22-bit results. Those may be scaled and truncated for a 16-bit output bus by connecting bits SUM6-21 to output bus lines 0-15 respectively. Both the $\overline{\text{SENBH}}$ and $\overline{\text{SENBL}}$ should be active in this case.

Note that this technique is much preferable to scaling down the coefficients (or the input data) to produce only 16-bit results directly, since this would require truncating the coefficients (or the data) to only 3 bits (!), introducing extreme degradation of the frequency response characteristics (or high levels of quantization-noise/distortion).

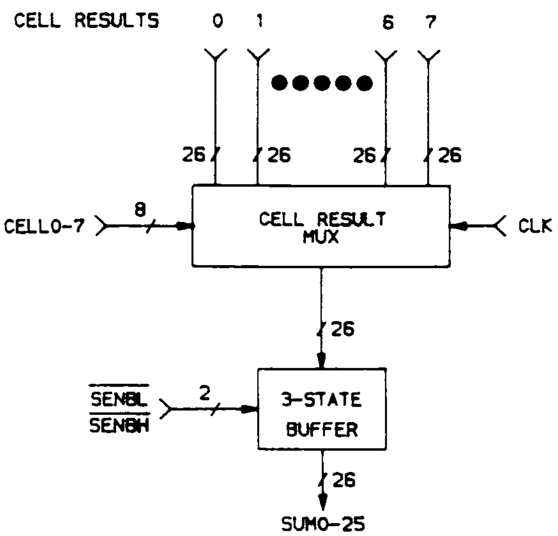


FIGURE 3. ZR33891 OUTPUT STAGE.

ZR33891 ARITHMETIC

Both data samples and coefficients can be represented as either 8-bit unsigned or 9-bit two's complement numbers. The 9x9 bit multiplier in each cell expects 9-bit two's complement operands. The binary format of 9-bit two's complement is shown below. Note that if the most significant or sign bit is held at logical zero, the 9-bit two's complement multiplier can multiply 8-bit unsigned operands. Only the upper (positive) half of the two's complement binary range is used.

The multiplier output is 18 bits and the accumulator is 26 bits. The accumulator width determines the maximum possible number of terms in the sum of products without overflow. The maximum number of terms depends also on the representation and the distribution of the coefficient and data values. As a worst case, assume the coefficients and data samples are always at their maximum absolute values. Then the maximum numbers of terms in the sum of products are:

	Maximum number of terms
Data and coefficients all positive (or 8 bits unsigned)	516
Data (or coefficients) all positive (or 8 bits unsigned), and the other all negative	514
Data and coefficients all negative	511

Note: For the 68-pin package, which has only 25-bit output, the number will be approximately half of the above.

For practical FIR filters, the coefficients are never all near maximum value, so even more terms are possible.

	Two's Complement, 9-bit									**Unsigned, 8-bit (with sign bit at logical 0)**								
	8	7	6	5	4	3	2	1	0	8	7	6	5	4	3	2	1	0
255 (Max +)	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
					•									•				
					•									•				
					•									•				
+1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
-1	1	1	1	1	1	1	1	1	1					Unused				
					•													
					•													
					•													
-256 (Max -)	1	0	0	0	0	0	0	0	0									

BASIC FIR OPERATION

Detailed operation of the ZR33891 DFP to perform a basic 8-tap, 9-bit coefficient, 9-bit data, 30 MHz FIR filter is best understood by observing the schematic (Figure 4), timing diagram (Figure 5) and sequence table (Table 1). The internal pipeline length of the DFP is four (4) clock cycles, corresponding to the registers C-REG (or X-REG), M0-REG, M1-REG, and T-REG (Figures 2 and 3). Therefore the delay from first presentation of data and coefficients at the DIN0-8 and CIN0-8 inputs to a sum appearing at the SUM0-25 output is 12 clock cycles.

After the pipeline has filled, a new output sample is available every clock. The delay to last sample output from last sample input is 4 clocks.

The output sums, Yn, shown in the timing diagram and the sequence table are derived from the sum-of-products equation:

$$Y(n) = C(0) \bullet X(n) + C(1) \bullet X(n\text{-}1) + C(2) \bullet X(n\text{-}2) + C(3) \bullet X(n\text{-}3) + C(4) \bullet X(n\text{-}4) + C(5) \bullet X(n\text{-}5) + C(6) \bullet X(n\text{-}6) + C(7) \bullet X(n\text{-}7)$$

where n refers to an index.

The sequence table (Table 1) shows the results of the adder in each cell and the chip output at each clock.

Filter lengths of less than 8 can be realized by resetting the 3-bit counter after the required number of taps.

EXTENDED FIR FILTER LENGTH

Filter lengths greater than eight taps can be implemented by either cascading together multiple DFP devices or "reusing" a single device. Using multiple devices, an FIR filter of over 500 taps can be constructed to operate at a 30 MHz sample rate. Using a single device clocked at 30 MHz, an FIR filter of over 500 taps can be constructed to operate at lower sample rates. Combinations of these two techniques are also possible.

CLK	CELL0	CELL1	CELL2	CELL3	CELL4	CELL5	CELL6	CELL7	OUTPUT
4	$C_7 \bullet X_0$	0	0	0					–
5	$+C_6 \bullet X_1$	$C_7 \bullet X_1$	0	0					–
6	$+C_5 \bullet X_2$	$+C_6 \bullet X_2$	$C_7 \bullet X_2$	0					–
7	$+C_4 \bullet X_3$	$+C_5 \bullet X_3$	$+C_6 \bullet X_3$	$C_7 \bullet X_3$					–
8	$+C_3 \bullet X_4$	$+C_4 \bullet X_4$	$+C_5 \bullet X_4$	$+C_6 \bullet X_4$	$C_7 \bullet X_4$				–
9	$+C_2 \bullet X_5$	$+C_3 \bullet X_5$	$+C_4 \bullet X_5$	$+C_5 \bullet X_5$	$+C_6 \bullet X_5$	$C_7 \bullet X_5$			–
10	$+C_1 \bullet X_6$	$+C_2 \bullet X_6$	$+C_3 \bullet X_6$	$+C_4 \bullet X_6$	$+C_5 \bullet X_6$	$+C_6 \bullet X_6$	$C_7 \bullet X_6$		–
11	$+C_0 \bullet X_7$	$+C_1 \bullet X_7$	$+C_2 \bullet X_7$	$+C_3 \bullet X_7$	$+C_4 \bullet X_7$	$+C_5 \bullet X_7$	$+C_6 \bullet X_7$	$C_7 \bullet X_7$	–
12	$C_7 \bullet X_8$	$+C_0 \bullet X_8$	$+C_1 \bullet X_8$	$+C_2 \bullet X_8$	$+C_3 \bullet X_8$	$+C_4 \bullet X_8$	$+C_5 \bullet X_8$	$+C_6 \bullet X_8$	–
13	$+C_6 \bullet X_9$	$C_7 \bullet X_9$	$+C_0 \bullet X_9$	$+C_1 \bullet X_9$	$+C_2 \bullet X_9$	$+C_3 \bullet X_9$	$+C_4 \bullet X_9$	$+C_5 \bullet X_9$	CELL0(Y7)
14	$+C_5 \bullet X_{10}$	$+C_6 \bullet X_{10}$	$C_7 \bullet X_{10}$	$+C_0 \bullet X_{10}$	$+C_1 \bullet X_{10}$	$+C_2 \bullet X_{10}$	$+C_3 \bullet X_{10}$	$+C_4 \bullet X_{10}$	CELL1(Y8)
15	$+C_4 \bullet X_{11}$	$+C_5 \bullet X_{11}$	$+C_6 \bullet X_{11}$	$C_7 \bullet X_{11}$	$+C_0 \bullet X_{11}$	$+C_1 \bullet X_{11}$	$+C_2 \bullet X_{11}$	$+C_3 \bullet X_{11}$	CELL2(Y9)
16	$+C_3 \bullet X_{12}$	$+C_4 \bullet X_{12}$	$+C_5 \bullet X_{12}$	$+C_6 \bullet X_{12}$	$C_7 \bullet X_{12}$	$+C_0 \bullet X_{12}$	$+C_1 \bullet X_{12}$	$+C_2 \bullet X_{12}$	CELL3(Y10)
17	$+C_2 \bullet X_{13}$	$+C_3 \bullet X_{13}$	$+C_4 \bullet X_{13}$	$+C_5 \bullet X_{13}$	$+C_6 \bullet X_{13}$	$C_7 \bullet X_{13}$	$+C_0 \bullet X_{13}$	$+C_1 \bullet X_{13}$	CELL4(Y11)
18	$+C_1 \bullet X_{14}$	$+C_2 \bullet X_{14}$	$+C_3 \bullet X_{14}$	$+C_4 \bullet X_{14}$	$+C_5 \bullet X_{14}$	$+C_6 \bullet X_{14}$	$C_7 \bullet X_{14}$	$+C_0 \bullet X_{14}$	CELL5(Y12)
19	$+C_0 \bullet X_{15}$	$+C_1 \bullet X_{15}$	$+C_2 \bullet X_{15}$	$+C_3 \bullet X_{15}$	$+C_4 \bullet X_{15}$	$+C_5 \bullet X_{15}$	$+C_6 \bullet X_{15}$	$C_7 \bullet X_{15}$	CELL6(Y13)
20	$C_7 \bullet X_{16}$	$+C_0 \bullet X_{16}$	$+C_1 \bullet X_{16}$	$+C_2 \bullet X_{16}$	$+C_3 \bullet X_{16}$	$+C_4 \bullet X_{16}$	$+C_5 \bullet X_{16}$	$+C_6 \bullet X_{16}$	CELL7(Y14)
21	$+C_6 \bullet X_{17}$	$C_7 \bullet X_{17}$	$+C_0 \bullet X_{17}$	$+C_1 \bullet X_{17}$	$+C_2 \bullet X_{17}$	$+C_3 \bullet X_{17}$	$+C_4 \bullet X_{17}$	$+C_5 \bullet X_{17}$	CELL0(Y15)

TABLE 1. ZR33891 30 MHZ, 8-TAP FIR FILTER SEQUENCE

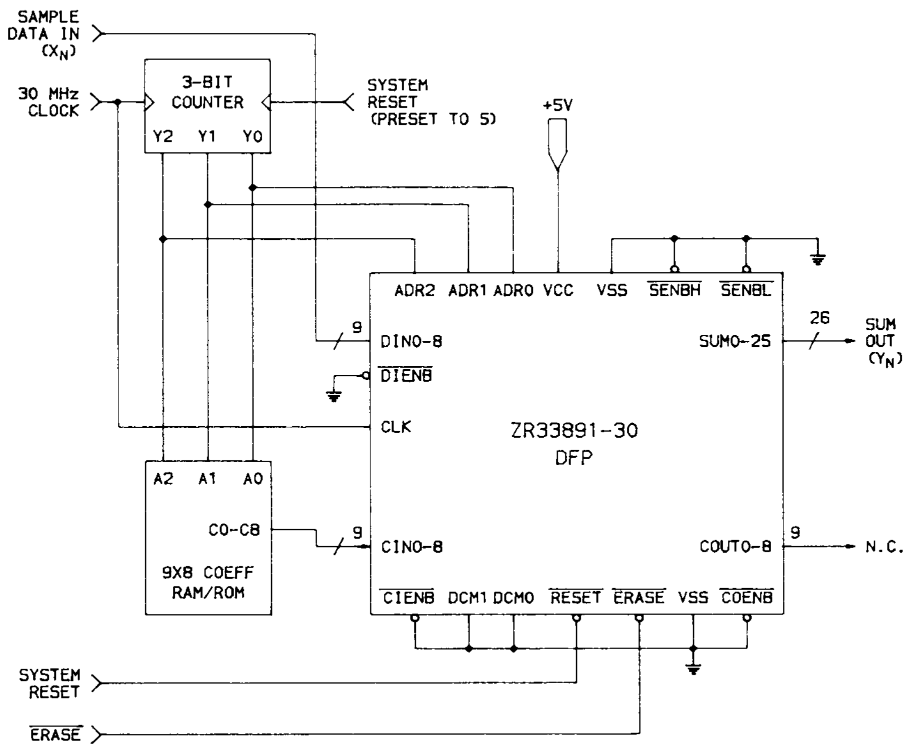
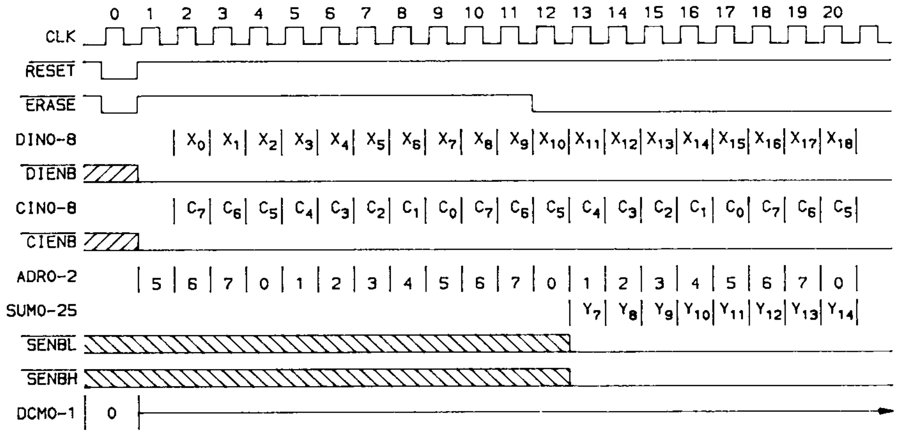


FIGURE 4. ZR33891 30 MHZ, 8-TAP FIR FILTER APPLICATION SCHEMATIC



$$Y_N = \sum_{K=0}^{7} C_K \cdot X_{N-K}$$

FIGURE 5. ZR33891 30 MHZ, 8-TAP FIR FILTER TIMING

A. CASCADE CONFIGURATION

To design a filter length L>8, L/8 ZR33891 DFP's are cascaded by connecting the COUT0-8 outputs of the (i)th DFP to the CIN0-8 inputs of the (i+1)th DFP. The DIN0-8 inputs and SUM0-25 outputs of all the DFP's are tied together. A specific example of two cascaded DFP's illustrates the technique (Figure 6). Timing (Figure 7) is similar to the simple 8-tap FIR, except the $\overline{\text{ERASE}}$ and $\overline{\text{SENBL}}/\overline{\text{SENBH}}$ signals must be enabled independently for the two DFPs in order to clear the correct accumulators and enable the SUM0-25 output signals at the proper times.

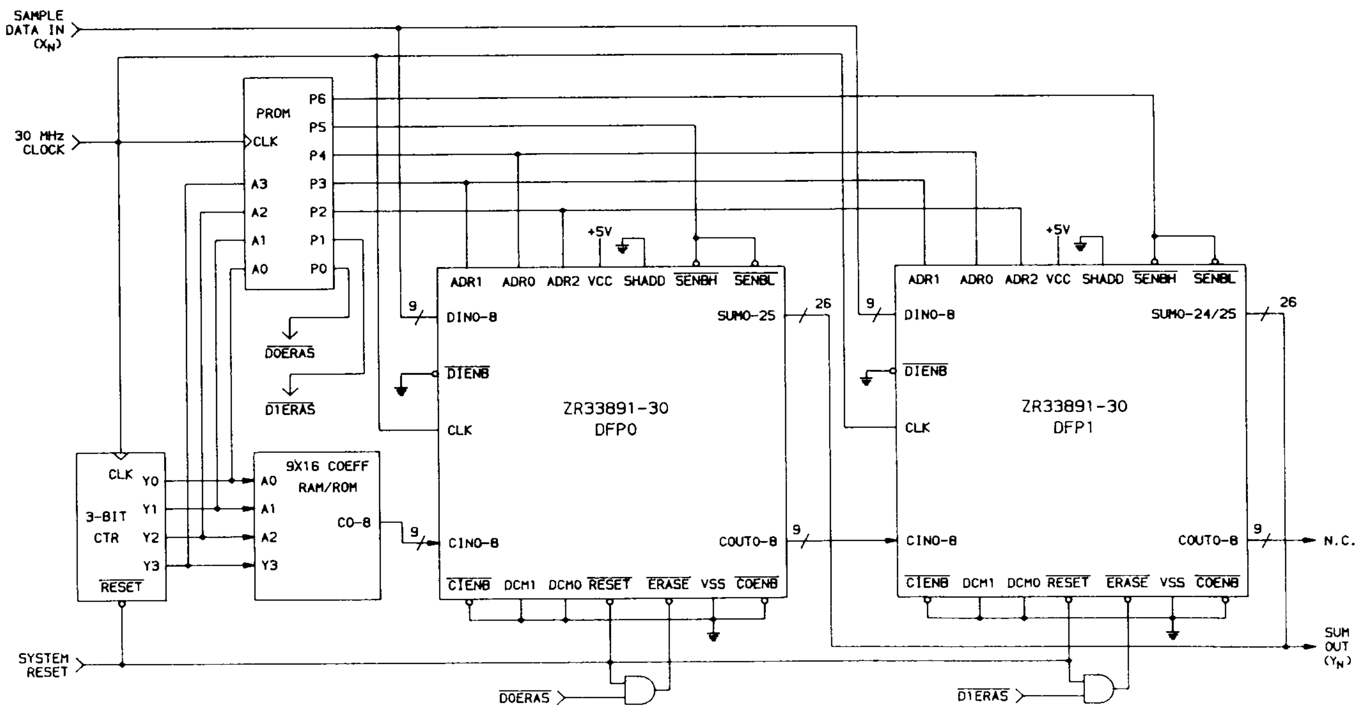
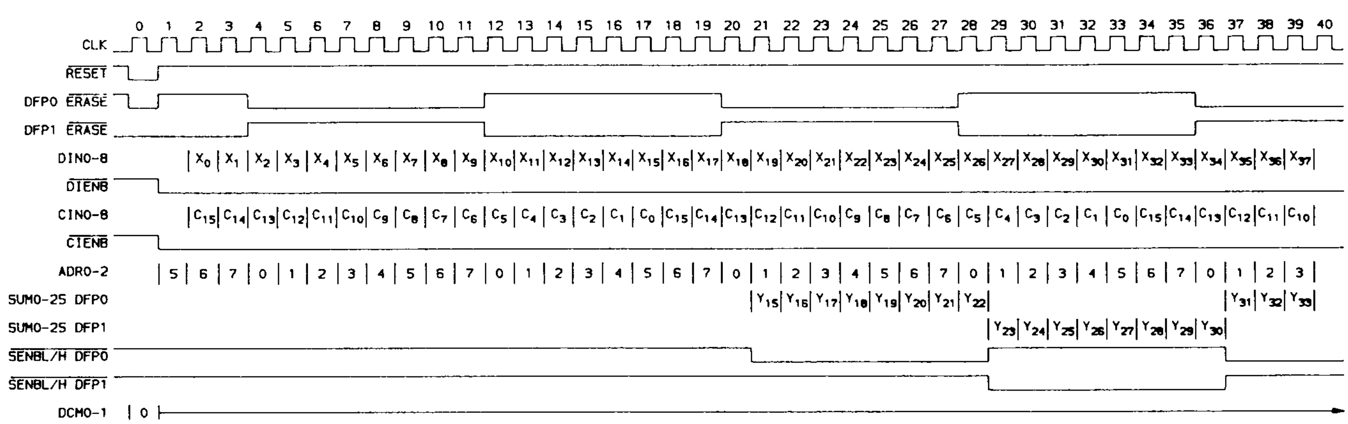


FIGURE 6. ZR33891 30 MHz 16-TAP FIR FILTER CASCADE APPLICATION SCHEMATIC.

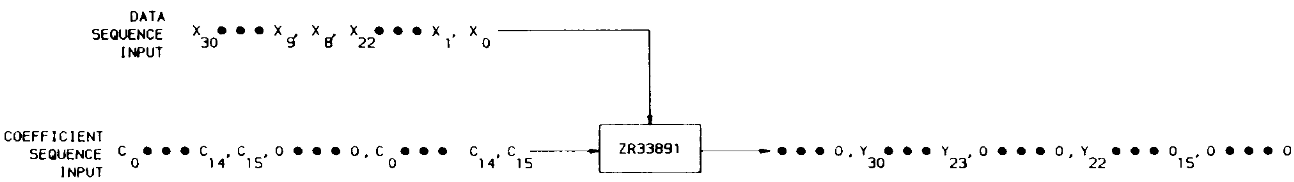


$$Y_N = \sum_{K=0}^{15} C_K \cdot X_{N-K}$$

FIGURE 7. ZR33891 16-TAP 30 MHz FILTER TIMING USING TWO CASCADED DFP's.

B. SINGLE ZR33891 CONFIGURATION

Using a single ZR33891 DFP, a filter of length L>8 can be constructed by processing in L/8 passes as illustrated in the following table (Table 2) for a 16-tap FIR. Each pass is composed of 7 + L cycles and computes eight output samples. In pass i, the samples with indices i*8 to i*8 +(L+6) enter the DIN0-8 inputs. The coefficients C_0 - C_{L-1} enter the CIN0-8 inputs, followed by seven zeros. As these zeros are entered, the result samples are output and the accumulators reset. Filter outputs can be put through a FIFO to even out the sample rate.



CLK	CELL0	CELL1	CELL2	CELL3	CELL4	CELL5	CELL6	CELL7	OUTPUT
4	$C_{15} \cdot X_0$	0	0	0					–
5	$+C_{14} \cdot X_1$	$C_{15} \cdot X_1$	0	0					–
6	$+C_{13} \cdot X_2$		$C_{15} \cdot X_2$	0					–
7	$+C_{12} \cdot X_3$			$C_{15} \cdot X_3$					–
8	$+C_{11} \cdot X_4$			$+C_{14} \cdot X_4$	$C_{15} \cdot X_4$				–
9	$+C_{10} \cdot X_5$			$+C_{13} \cdot X_5$		$C_{15} \cdot X_5$			–
10	$+C_9 \cdot X_6$			$+C_{12} \cdot X_6$			$C_{15} \cdot X_6$		–
11	$+C_8 \cdot X_7$			$+C_{11} \cdot X_7$				$C_{15} \cdot X_7$	–
12	$+C_7 \cdot X_8$			$+C_{10} \cdot X_8$				$+C_{14} \cdot X_8$	–
13	$+C_6 \cdot X_9$			$+C_9 \cdot X_9$				$+C_{13} \cdot X_9$	–
14	$+C_5 \cdot X_{10}$			$+C_8 \cdot X_{10}$				$+C_{12} \cdot X_{10}$	–
15	$+C_4 \cdot X_{11}$			$+C_7 \cdot X_{11}$				$+C_{11} \cdot X_{11}$	–
16	$+C_3 \cdot X_{12}$			$+C_6 \cdot X_{12}$				$+C_{10} \cdot X_{12}$	–
17	$+C_2 \cdot X_{13}$			$+C_5 \cdot X_{13}$				$+C_9 \cdot X_{13}$	–
18	$+C_1 \cdot X_{14}$			$+C_4 \cdot X_{14}$				$+C_8 \cdot X_{14}$	–
19	$+C_0 \cdot X_{15}$			$+C_3 \cdot X_{15}$				$+C_7 \cdot X_{15}$	–
20	0	$+C_0 \cdot X_{16}$		$+C_2 \cdot X_{16}$				$+C_6 \cdot X_{16}$	–
21	0	0	$+C_0 \cdot X_{17}$	$+C_1 \cdot X_{17}$				$+C_5 \cdot X_{17}$	CELL0(Y15)
22	0	0	0	$+C_0 \cdot X_{18}$				$+C_4 \cdot X_{18}$	CELL1(Y16)
23	0	0	0	0	$+C_0 \cdot X_{19}$			$+C_3 \cdot X_{19}$	CELL2(Y17)
24	0	0	0	0	0	$+C_0 \cdot X_{20}$		$+C_2 \cdot X_{20}$	CELL3(Y18)
25	0	0	0	0	0	0	$+C_0 \cdot X_{21}$	$+C_1 \cdot X_{21}$	CELL4(Y19)
26	0	0	0	0	0	0	0	$+C_0 \cdot X_{22}$	CELL5(Y20)
27	$C_{15} \cdot X_8$	0	0	0	0	0	0	0	CELL6(Y21)
28	$+C_{14} \cdot X_9$	$C_{15} \cdot X_9$	0	0	0	0	0	0	CELL7(Y22)
29	$+C_{13} \cdot X_{10}$		$C_{15} \cdot X_{10}$	0	0	0	0	0	–
30	$+C_{12} \cdot X_{11}$			$C_{15} \cdot X_{11}$	0	0	0	0	–
31	$+C_{11} \cdot X_{12}$				$C_{15} \cdot X_{12}$	0	0	0	–
32	$+C_{10} \cdot X_{13}$					$C_{15} \cdot X_{13}$	0	0	–
33	$+C_9 \cdot X_{14}$						$C_{15} \cdot X_{14}$	0	–
34	$+C_8 \cdot X_{15}$							$C_{15} \cdot X_{15}$	–
35	$+C_7 \cdot X_{16}$							$+C_{14} \cdot X_{16}$	–
36	$+C_6 \cdot X_{17}$							$+C_{13} \cdot X_{17}$	–
37	$+C_5 \cdot X_{18}$							$+C_{12} \cdot X_{18}$	–
38	$+C_4 \cdot X_{19}$							$+C_{11} \cdot X_{19}$	–
39	$+C_3 \cdot X_{20}$							$+C_{10} \cdot X_{20}$	–
40	$+C_2 \cdot X_{21}$							$+C_9 \cdot X_{21}$	–
41	$+C_1 \cdot X_{22}$							$+C_8 \cdot X_{22}$	–
42	$+C_0 \cdot X_{23}$							$+C_7 \cdot X_{23}$	–
43	0	$+C_0 \cdot X_{24}$						$+C_6 \cdot X_{24}$	–
44	0	0	$+C_0 \cdot X_{25}$					$+C_5 \cdot X_{25}$	CELL0(Y23)
45	0	0	0	$+C_0 \cdot X_{26}$				$+C_4 \cdot X_{26}$	CELL1(Y24)
46	0	0	0	0	$+C_0 \cdot X_{27}$			$+C_3 \cdot X_{27}$	CELL2(Y25)

TABLE 2. ZR33891-30 10.43 MHZ, 16-TAP FIR FILTER SEQUENCE

EXTENDED COEFFICIENT AND DATA SAMPLE WORD SIZE

The data and coefficient word size can be extended by utilizing several ZR33891 DFP's in parallel to get the maximum sample rate, or a single DFP with resulting lower sample rates. The technique is to compute partial products of 9 x 9 and combine these partial products by shifting and adding to obtain the final result. The shifting and adding can be accomplished with external adders. (Note that the least significant parts of the data and/or coefficients are unsigned.)

DECIMATION/RESAMPLING

The ZR33891 provides a mechanism for decimating by factors of 2, 3, or 4, using the three D registers and two multiplexers in the coefficient path through the cell (Figure 2). The sequence table (Table 3) and the timing diagrams (Figure 8) illustrate the technique for a 16-tap, decimate-by-two, FIR filter with 30MHz input sample rate and 15MHz output sample rate.

OTHER ZR33891 APPLICATIONS

The ZR33891 is a versatile device with many applications beyond simple FIR filtering. The following list is a small sample of some applications possible with the DFP. Implementations of these applications are discussed in greater detail in the various ZR33891 Zoran Application Notes.

- Higher bandwidth (60 MHz and up)
- 2-D FIR Spatial Filtering/ Convolution/Correlation
- Matrix multiplication
- Complex multiply
- Butterfly computation
- DFT
- Adaptive filters
  - -Echo cancellation
  - -Adaptive equalization
- Reverberation generators
- Beam former
- Video Decoders

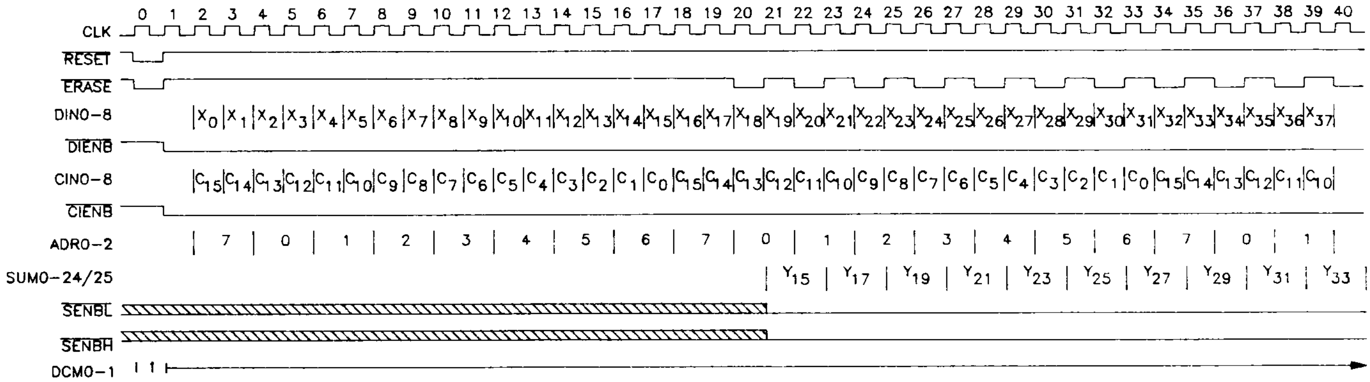
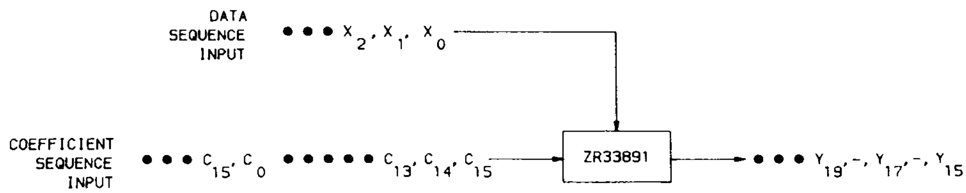


FIGURE 8. ZR33891-30 16-TAP DECIMATE-BY-TWO FIR FILTER TIMING, 30-MHZ IN, 15 MHZ OUT.



CLK	CELL0	CELL1	CELL2	CELL3	CELL4	CELL5	CELL6	CELL7	OUTPUT
4	$C_{15} \cdot X_0$	0	0	0	0	0		0	
5	$+C_{14} \cdot X_1$	0	0	0	0	0	0	0	
6	$+C_{13} \cdot X_2$	$C_{15} \cdot X_2$	0	0	0	0	0	0	
7	$+C_{12} \cdot X_3$		0	0	0	0	0	0	
8	$+C_{11} \cdot X_4$		$C_{15} \cdot X_4$	0	0	0	0	0	
9	$+C_{10} \cdot X_5$			0	0	0	0	0	
10	$+C_9 \cdot X_6$			$C_{15} \cdot X_6$	0	0	0	0	
11	$+C_8 \cdot X_7$				0	0	0	0	
12	$+C_7 \cdot X_8$				$C_{15} \cdot X_8$	0	0	0	
13	$+C_6 \cdot X_9$					0	0	0	
14	$+C_5 \cdot X_{10}$					$C_{15} \cdot X_{10}$	0	0	
15	$+C_4 \cdot X_{11}$						0	0	
16	$+C_3 \cdot X_{12}$						$C_{15} \cdot X_{12}$	0	
17	$+C_2 \cdot X_{13}$							0	
18	$+C_1 \cdot X_{14}$							$C_{15} \cdot X_{14}$	
19	$+C_0 \cdot X_{15}$							$+C_{14} \cdot X_{15}$	
20	$C_{15} \cdot X_{16}$							$+C_{13} \cdot X_{16}$	
21	$+C_{14} \cdot X_{17}$							$+C_{12} \cdot X_{17}$	CELL0(Y15)
22	$+C_{13} \cdot X_{18}$							$+C_{11} \cdot X_{18}$	–
23	$+C_{12} \cdot X_{19}$							$+C_{10} \cdot X_{19}$	CELL1(Y17)
24	$+C_{11} \cdot X_{20}$							$+C_9 \cdot X_{20}$	–
25	$+C_{10} \cdot X_{21}$							$+C_8 \cdot X_{21}$	CELL2(Y19)
26	$+C_9 \cdot X_{22}$							$+C_7 \cdot X_{22}$	–
27	$+C_8 \cdot X_{23}$							$+C_6 \cdot X_{23}$	CELL3(Y21)
28	$+C_7 \cdot X_{24}$							$+C_5 \cdot X_{24}$	–
29	$+C_6 \cdot X_{25}$							$+C_4 \cdot X_{25}$	CELL4(Y23)
30	$+C_5 \cdot X_{26}$							$+C_3 \cdot X_{26}$	–
31	$+C_4 \cdot X_{27}$							$+C_2 \cdot X_{27}$	CELL5(Y25)
32	$+C_3 \cdot X_{28}$							$+C_1 \cdot X_{28}$	–
33	$+C_2 \cdot X_{29}$							$+C_0 \cdot X_{29}$	CELL6(Y27)
34	$+C_1 \cdot X_{30}$							$+C_{15} \cdot X_{30}$	–
35	$+C_0 \cdot X_{31}$	$+C_2 \cdot X_{31}$	$+C_4 \cdot X_{31}$	$+C_6 \cdot X_{31}$	$+C_8 \cdot X_{31}$	$+C_{10} \cdot X_{31}$	$+C_{12} \cdot X_{31}$	$+C_{14} \cdot X_{31}$	CELL7(Y29)
36	$+C_{15} \cdot X_{32}$	$+C_1 \cdot X_{32}$	$+C_3 \cdot X_{32}$	$+C_5 \cdot X_{32}$	$+C_7 \cdot X_{32}$	$+C_9 \cdot X_{32}$	$+C_{11} \cdot X_{32}$	$+C_{13} \cdot X_{32}$	–
37	$+C_{14} \cdot X_{33}$	$+C_0 \cdot X_{33}$	$+C_2 \cdot X_{33}$	$+C_4 \cdot X_{33}$	$+C_6 \cdot X_{33}$	$+C_8 \cdot X_{33}$	$+C_{10} \cdot X_{33}$	$+C_{12} \cdot X_{33}$	CELL8(Y31)

TABLE 3. ZR33891-30 16-TAP DECIMATE-BY-TWO FIR FILTER SEQUENCE, 30MHZ IN, 15 MHZ OUT

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias .... -55°C to +125°C
Storage Temperature .... -65°C to +150°C
Supply Voltage to Ground Potential
Continuous .... -0.5V to +7.0V
DC Voltage Applied to Outputs
for High Output State .... -0.5V to +7.0V

DC Input Voltage .... -0.5V to +5.5V
DC Output Current, into Outputs
(not to exceed 200 mA total) ... 20mA/output
DC Input Current .... -30 to +5.0 mA

NOTE: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGE

Commercial Devices

Temperature .... $0°C \leq T_A \leq +70°C$
Supply Voltage .... $4.75V \leq V_{CC} \leq 5.25V$

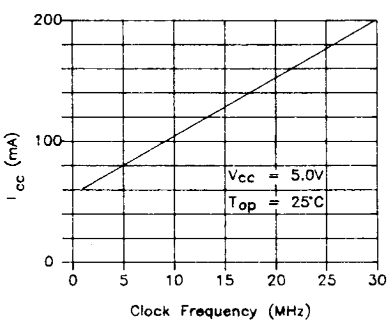
Military Devices

Temperature .... $-55°C < T_A \leq +125°C$
Supply Voltage .... $4.50V \leq V_{CC} \leq 5.50V$

DC CHARACTERISTICS

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL}=2mA
V_{OH}	Output High Voltage	2.4		V	I_{OH}=-400μA
I_{CC}	Power Supply Current @20MHz		190*	mA	T_A=0°C, $V_{CC}=V_{CCmax}$
I_{LI}	Input Leakage Current		±10	μA	$0<Vin<V_{CCmax}$
I_{LO}	Output Leakage Current		±10	μA	$0.45<Vout<V_{CCmax}$
V_{CL}	Clock-In Low Voltage	-0.5	0.6	V	
V_{CH}	Clock-In High Voltage	4.0	V_{CC}+0.5	V	
C_{IN}	Input Capacitance		10	pF	f_C=1MHz
C_{IO}	I/O, Clock, & Output Capacitance		10	pF	f_C=1MHz

*100mA for plastic quad flat pack (PQ) version only.



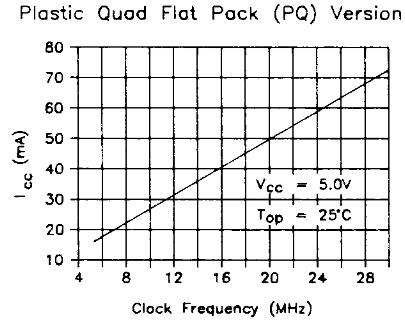


FIGURE 9. TYPICAL I_{CC} VS. FREQUENCY

AC CHARACTERISTICS

See Figures 10 to 14 for definitions and following tables for data.

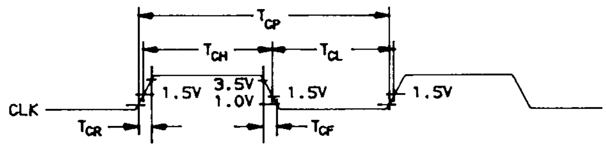


FIGURE 10. CLOCK AC PARAMETERS

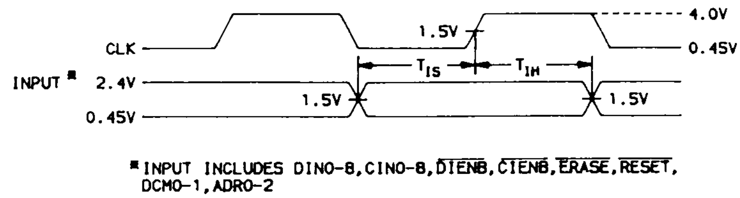


FIGURE 11. INPUT SETUP AND HOLD

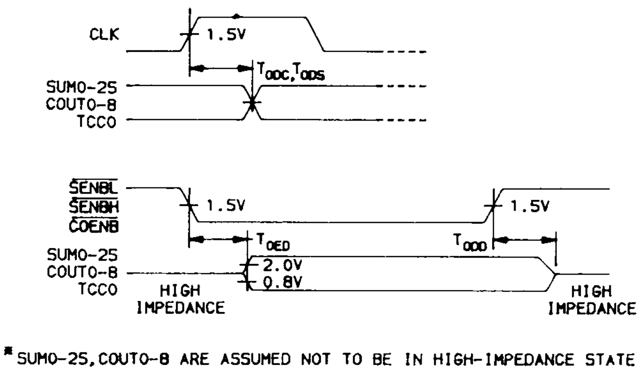
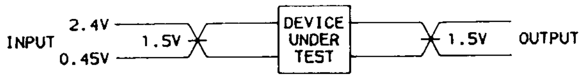
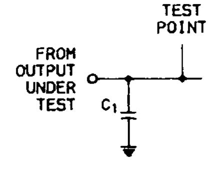


FIGURE 12. SUM0-25, COUT0-8, OUTPUT DELAYS



A.C. TESTING, INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". INPUT AND OUTPUT TIMING MEASUREMENTS ARE MADE AT 1.5V FOR BOTH A LOGIC "1" AND "0"

FIGURE 13. A.C. TESTING INPUT, OUTPUT WAVEFORM



NOTE: C_1=50pF INCLUDING STRAY AND WIRING CAPACITANCE

FIGURE 14. NORMAL A. C. TEST LOAD

AC CHARACTERISTICS OVER OPERATING RANGE ZR33891-30 (all packages)

Symbol	Parameter	ZR33891-30 Min	ZR33891-30 Max	Units	Test Conditions
T_{CP}	Clock Period	33.3	5000	ns	
T_{CL}	Clock Low	15		ns	
T_{CH}	Clock High	15		ns	
T_{CR}	Clock Input Rise		5	ns	1.0V to 3.5V
T_{CF}	Clock Input Fall		5	ns	1.0V to 3.5V
T_{IS}	Input Setup	6		ns	
T_{IH}	Input Hold	5		ns	
T_{ODC}	CLK to Coefficient Output Delay		27	ns	
T_{OED}	Output Enable Delay*		15	ns	
T_{ODD}	Output Disable Delay*		15	ns	
T_{ODS}	CLK to SUM Output Delay		24	ns	

*Not tested in production. Guaranteed by characterization.

AC CHARACTERISTICS OVER OPERATING RANGE ZR33891-25

Symbol	Parameter	ZR33891-25 Min	ZR33891-25 Max	Units	Test Conditions
T_{CP}	Clock Period	40	5000	ns	
T_{CL}	Clock Low	18		ns	
T_{CH}	Clock High	18		ns	
T_{CR}	Clock Input Rise		5	ns	1.0V to 3.5V
T_{CF}	Clock Input Fall		5	ns	1.0V to 3.5V
T_{IS}	Input Setup	8		ns	
T_{IH}	Input Hold	5		ns	
T_{ODC}	CLK to Coefficient Output Delay		28	ns	
T_{OED}	Output Enable Delay*		15	ns	
T_{ODD}	Output Disable Delay*		15	ns	
T_{ODS}	CLK to SUM Output Delay		28	ns ns	

*Not tested in production. Guaranteed by characterization.

AC CHARACTERISTICS OVER OPERATING RANGE ZR33891-20

Symbol	Parameter	ZR33891-20 Min	Max	Units	Test Conditions
T_{CP}	Clock Period	50	5000	ns	
T_{CL}	Clock Low	22		ns	
T_{CH}	Clock High	22		ns	
T_{CR}	Clock Input Rise		5	ns	1.0V to 3.5V
T_{CF}	Clock Input Fall		5	ns	1.0V to 3.5V
T_{IS}	Input Setup	10		ns	
T_{IH}	Input Hold	5		ns	
T_{ODC}	CLK to Coefficient Output Delay		40	ns	
T_{OED}	Output Enable Delay*		20	ns	
T_{ODD}	Output Disable Delay*		20	ns	
T_{ODS}	CLK to SUM Output Delay		40	ns ns	

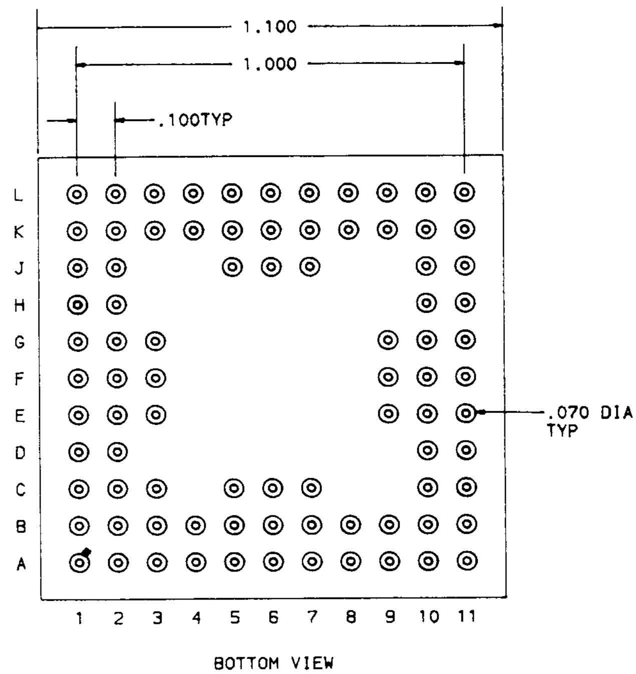
*Not tested in production. Guaranteed by characterization.

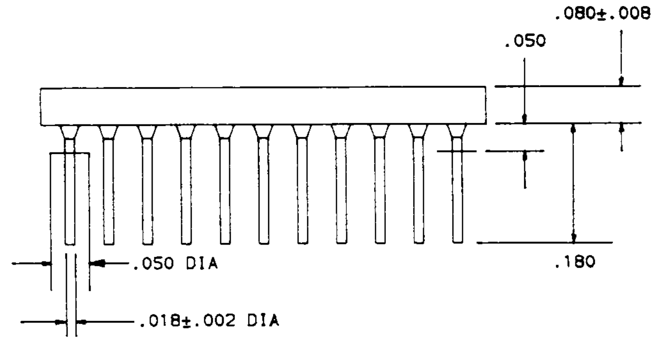
AC CHARACTERISTICS OVER OPERATING RANGE ZR33891-15

Symbol	Parameter	ZR33891-15 Min	Max	Units	Test Conditions
T_{CP}	Clock Period	67	5000	ns	
T_{CL}	Clock Low	30		ns	
T_{CH}	Clock High	30		ns	
T_{CR}	Clock Input Rise		5	ns	1.0V to 3.5V
T_{CF}	Clock Input Fall		5	ns	1.0V to 3.5V
T_{IS}	Input Setup	14		ns	
T_{IH}	Input Hold	5		ns	
T_{ODC}	CLK to Coefficient Output Delay		50	ns	
T_{OED}	Output Enable Delay*		25	ns	
T_{ODD}	Output Disable Delay*		25	ns	
T_{ODS}	CLK to SUM Output Delay		50	ns ns	

*Not tested in production. Guaranteed by characterization.

PACKAGE INFORMATION





PIN L1 — PIN L11

DCM1	SUM23	SUM22	SUM21	SUM18	SUM14	VCC	SUM13	VSS	SUM11	SUM9
SENBH	SUM24	VSS	VCC	SUM19	VSS	SUM15	SUM12	SUM10	SUM8	SUM6
VCC	SUM25			SUM20	SUM17	SUM16			SUM7	VSS
ADR1	ADR0								SUM5	SUM4
ADR2	DCM0	CLK						SUM1	SUM3	SUM2
VSS	COUT0	VSS (SHADOW)			ZR33891G			SUM0	VCC	VSS
COUT1	VSS	COUT2						CIN1	CIN0	SENBL
COUT3	COUT4								CIN2	VCC
COUT5	COUT6	ALIGN PIN		DIENB	DIN5	DIN4			CIN5	CIN3
VCC	COUT7	COUT8	ERASE	DIN8	DIN1	DIN2	CIENB	CIN7	CIN6	CIN4
VSS	COENB	VCC	RESET	DIN7	DIN6	DIN3	DIN0	CIN8	VCC	VSS

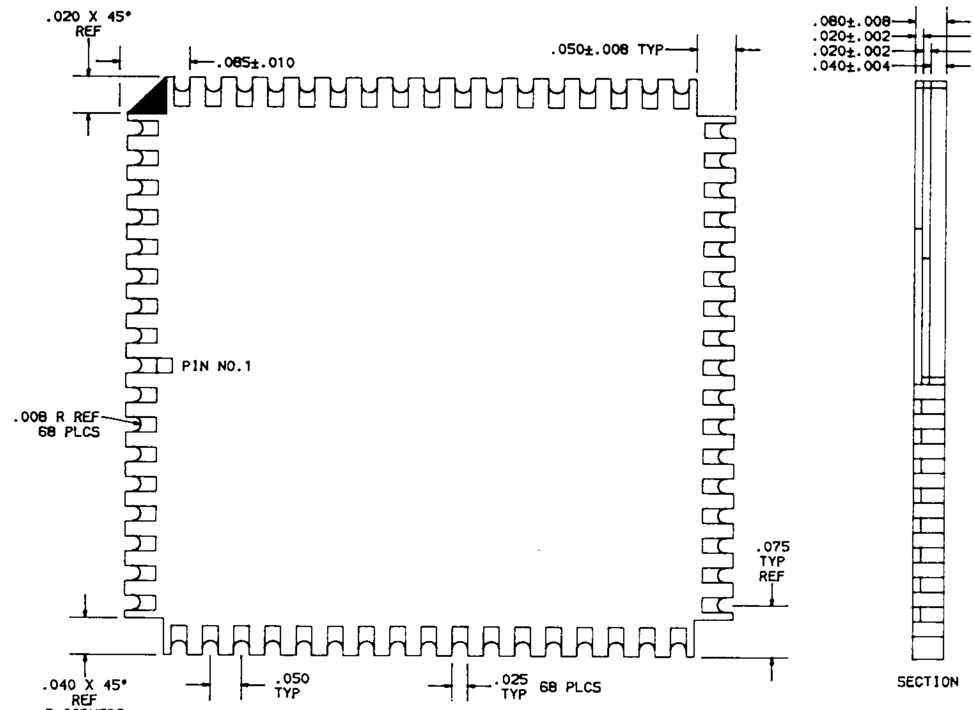
PIN A1 — PIN A11

BOTTOM VIEW

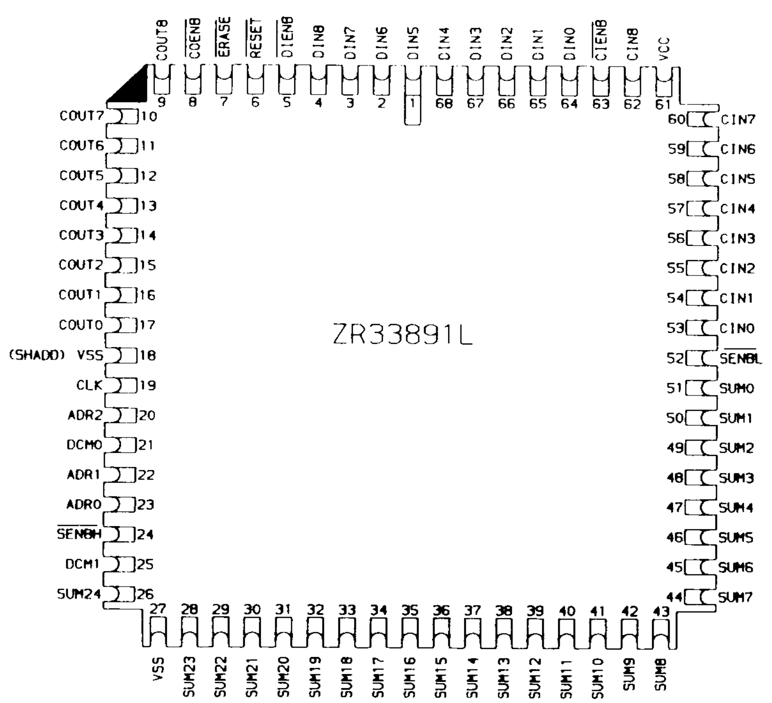
"NOTE:

The align pin (C3) is electrically connected to pin C2 (COUT6)."

ZR33891 84-PIN GRID ARRAY (PGA)

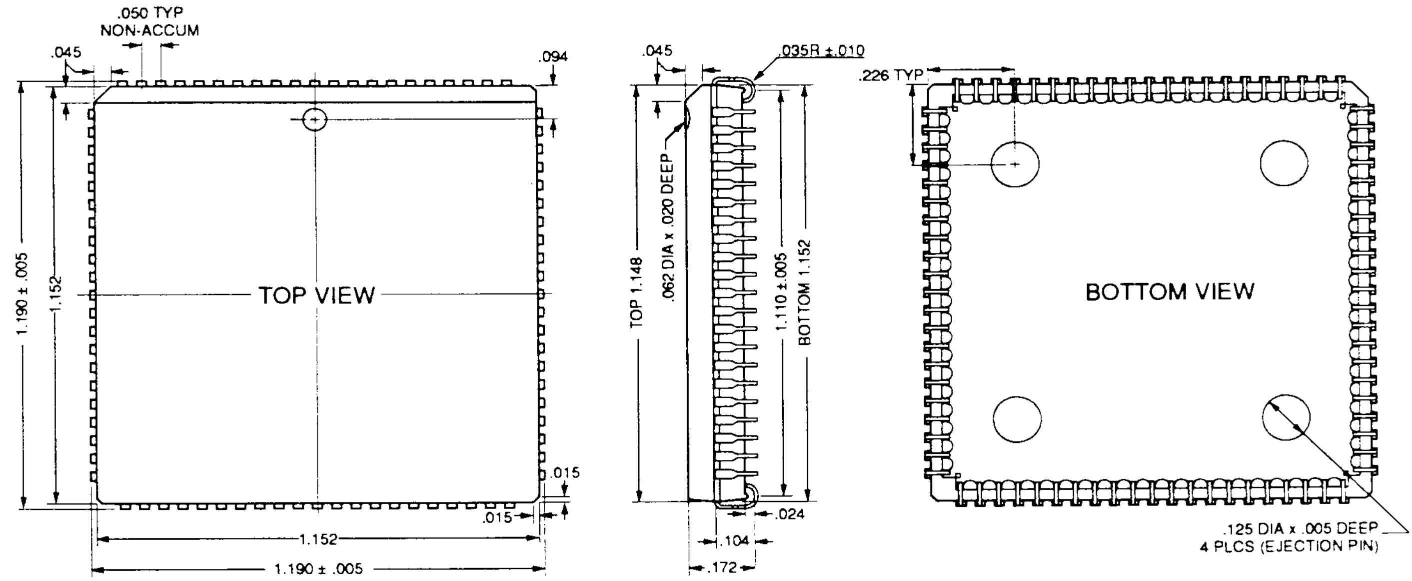


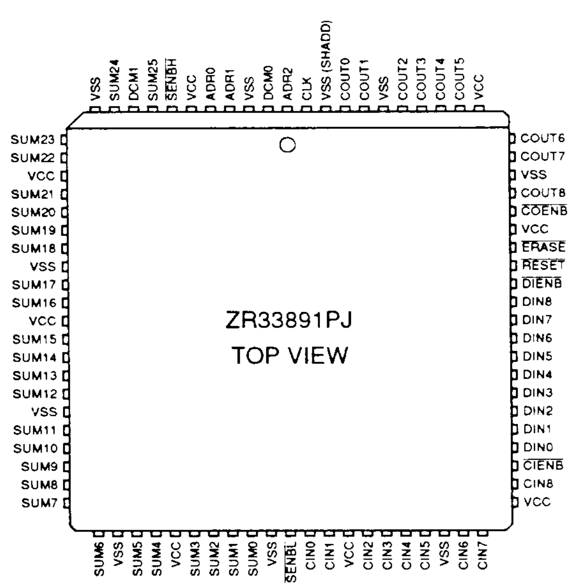
BOTTOM VIEW



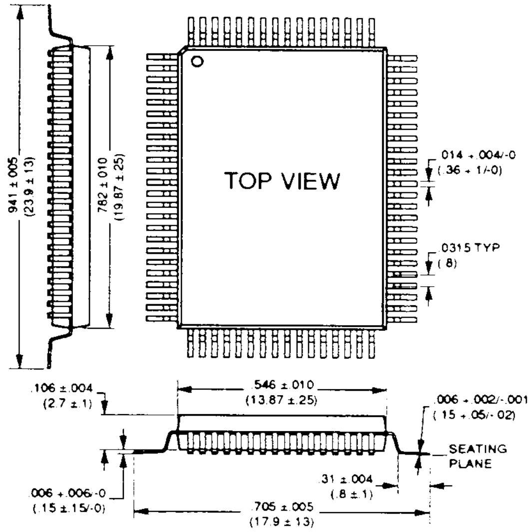
TOP VIEW

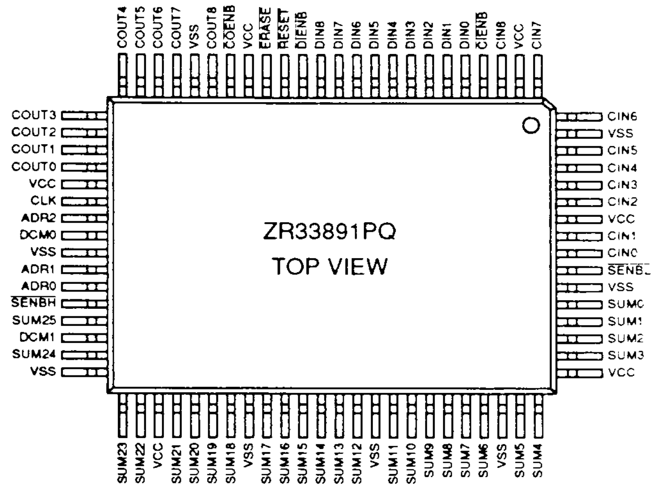
ZR33891 68-PIN LEADLESS CHIP CARRIER (LCC)





ZR33891 84-PIN J-BEND PLASTIC LEADED CHIP CARRIER





NOTE: PRINCIPAL DIMENSIONS IN INCHES, DIMENSIONS IN BRACKETS (IN MM).

ZR33891 80-PIN PLASTIC QUAD FLAT PACK

ORDERING INFORMATION

ZR 33891 G C -30

- -30 — Clock Rate
- C — Screening key
- G — Package
- 33891 — Part Number
- ZR — Prefix

Package

G - 84 pin grid array
L - 68 pin leadless chip carrier
PJ - 84 pin J-bend plastic leaded chip carrier
PQ - 80 pin plastic quad flat pack

Screen Key

C - Commerical temperatures (0° C. to 70° C.)
Vcc = 4.75 to 5.25v
T - Extended temperature (-55° C. to +125° C.)
M - Assembly and test to Zoran's Mil. (883)
B - Full Mil. 883C qualified*

Clock Rate

15,20,25,or 30 MHz

Availability

	G	L	PJ	PQ
C	15,20, 25,30	15,20, 25	20,25, 30	25,30
T	15,20			
M	15,20			
B	15,20	15,20		

*Contact factory for availability

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