DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD78011B(A),78012B(A),78013(A),78014(A)

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

μPD78011B(A),78012B(A), 78013(A) and 78014(A) incorporate various peripheral hardwares such as 8-bit resolution A/D converter, timer, serial interface, interrupt control, etc.

A one-time PROM or EPROM product capable of operating in the same power supply voltage range as of the mask ROM product and other development tools are also provided.

Functions are described in detail in the following User's Manual, which should be read when carrying out design work.

μPD78014, 78014Y Series User's Manual : IEU-780

FEATURES

- High reliability compared with μPD78011B/78012B/78013/78014
- On-chip large ROM/RAM capacity

Item / Product Name	Program Memory (ROM)	Data Memory		Package
		Internal High-Speed RAM	Buffer RAM	
μPD78011B(A)	8K bytes	512 bytes	32 bytes	• 64-pin Plastic Shrink DIP (750 mil) • 64-pin Plastic QFP (□14 mil)
μPD78012B(A)	16K bytes			
μPD78013(A)	24K bytes	1024 bytes		
μPD78014(A)	32K bytes			

- External memory expansion space: 64K bytes
- Instruction execution time can be varied from high-speed (0.4 μs) to ultra-low-speed (122 μs)
- I/O ports: 53
- 8-bit resolution A/D converter : 8 channels
- Serial interface: 2 channels
- Timer: 5 channels
- Operating voltage range : 2.7 to 6.0 V

APPLICATION

Transportation machinery control equipment, gas detection breakers, various kinds of safety equipments, etc.

Document No. IC-3411
(O. D. No. IP-8874)
Date Published May 1994 P

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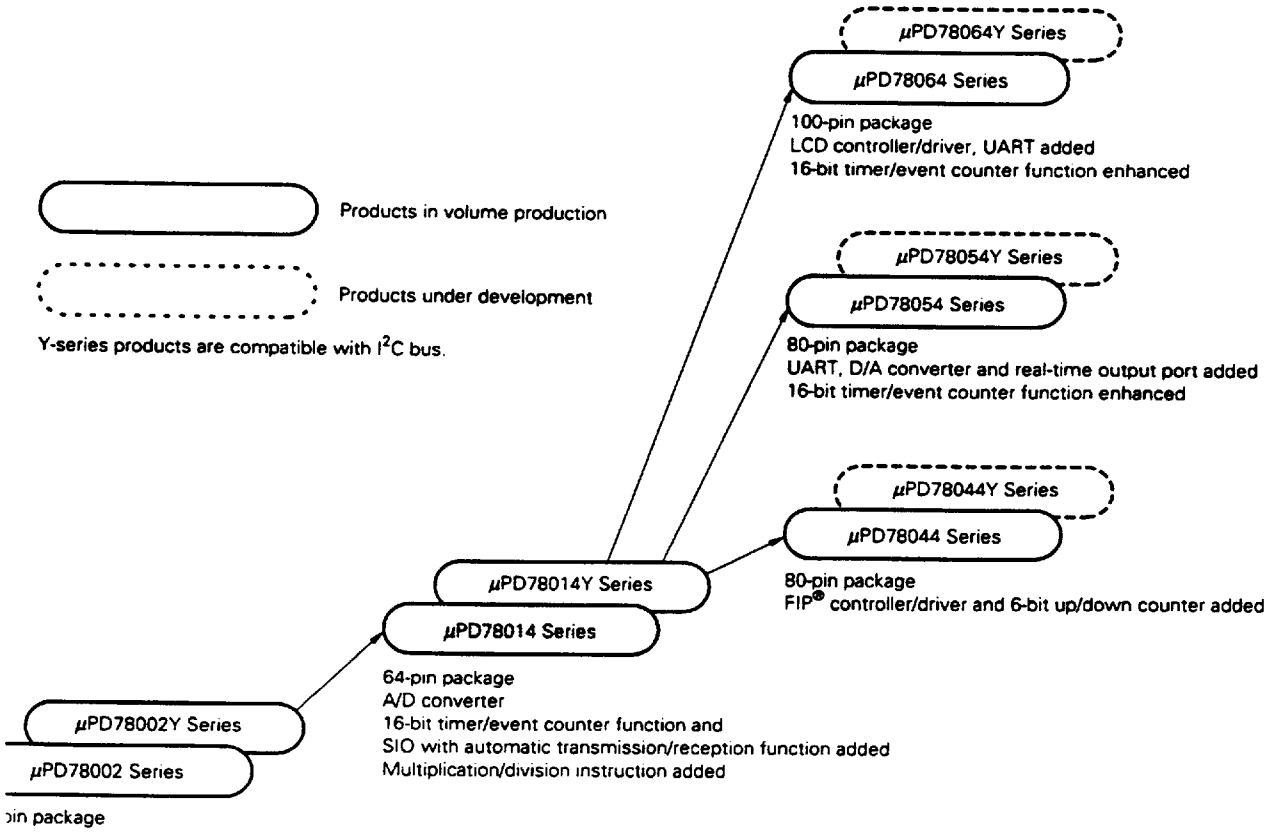
ORDERING INFORMATION

Ordering Code	Package	Quality Grade
μPD78011BCW(A)-xxx	64-pin plastic shrink DIP (750 mil)	Special
μPD78011BGC(A)-xxx-AB8	64-pin plastic QFP (□14 mm)	Special
μPD78012BCW(A)-xxx	64-pin plastic shrink DIP (750 mil)	special
μPD78012BGC(A)-xxx-AB8	64-pin plastic QFP (□14 mm)	Special
μPD78013CW(A)-xxx	64-pin plastic shrink DIP (750 mil)	Special
μPD78013GC(A)-xxx-AB8	64-pin plastic QFP (□14 mm)	Special
μPD78014CW(A)-xxx	64-pin plastic shrink DIP (750 mil)	Special
μPD78014GC(A)-xxx-AB8	64-pin plastic QFP (□14 mm)	Special

Remarks xxx means a ROM code number.

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

78K/0 SERIES DEVELOPMENT



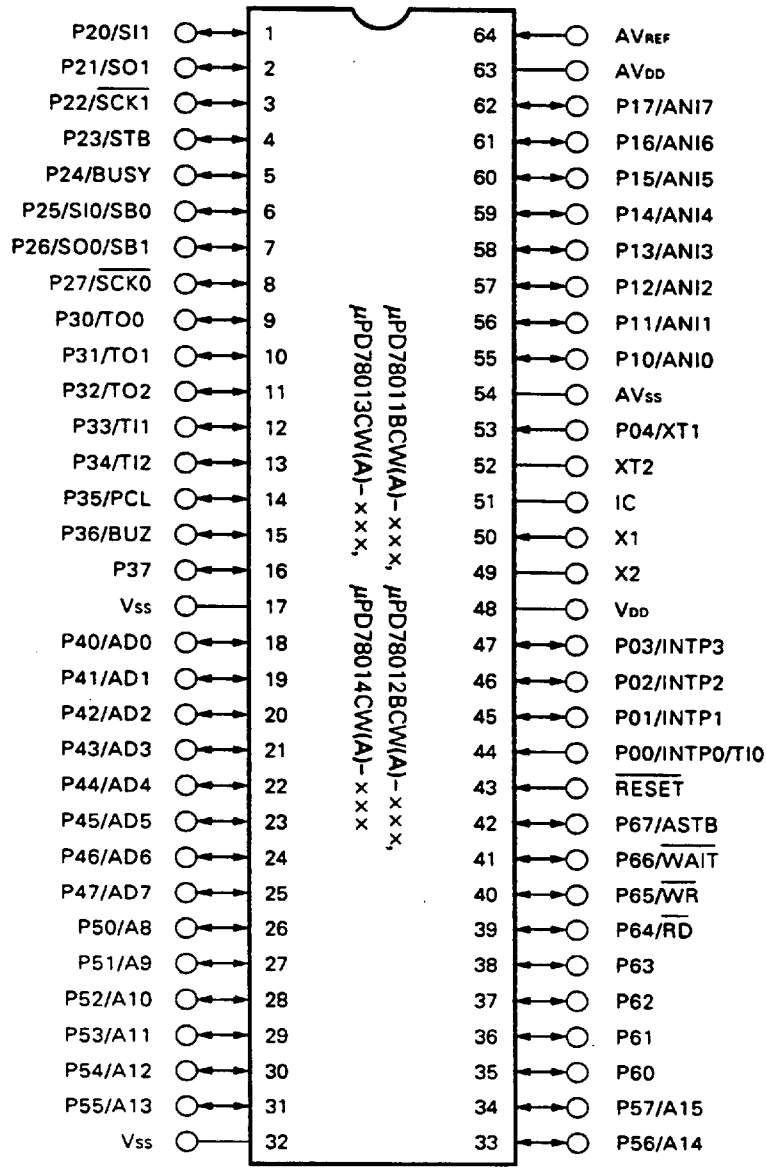
OVERVIEW OF FUNCTION

Item \ Product Name		μPD78011B(A)	μPD78012B(A)	μPD78013(A)	μPD78014(A)
Internal memory	ROM	8K bytes	16K bytes	24K bytes	32K bytes
	Internal high-speed RAM	512 bytes		1024 bytes	
	Buffer RAM	32 bytes			
Memory space		64K bytes			
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Instruction cycle		On-chip instruction execution time cycle modification function			
	When main system clock selected	0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 10.0 MHz operation)			
	When subsystem clock selected	122 μs (at 32.768 kHz operation)			
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.			
I/O ports		Total : 53 • CMOS input : 2 • CMOS I/O : 47 • N-channel open-drain I/O (15 V withstand voltage) : 4			
A/D converter		• 8-bit resolution × 8 channels • Operable over a wide power supply voltage range: V_{DD} = 2.7 to 6.0 V			
Serial interface		• 3-wire/SBI/2-wire/I^2C bus mode selectable: 1 channel • 3-wire mode (on-chip max. 32 bytes automatic data transmit/receive function): 1 channel			
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Watch timer : 1 channel • Watchdog timer : 1 channel			
Timer output		3 (14-bit PWM output × 1)			
Clock output		39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (at main system clock 10.0 MHz operation), 32.768 kHz (at subsystem clock 32.768 kHz operation)			
Buzzer output		2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 10.0 MHz operation)			
Vectored interrupts	Maskable interrupts	Internal : 8 External : 4			
	Non-maskable interrupt	Internal : 1			
	Software interrupt	Internal : 1			
Test input		Internal : 1 External : 1			
Operating voltage range		V_{DD} = 2.7 to 6.0 V			
Operating temperature range		−40 to +85°C			
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (□14 mm)			

CONTENTS

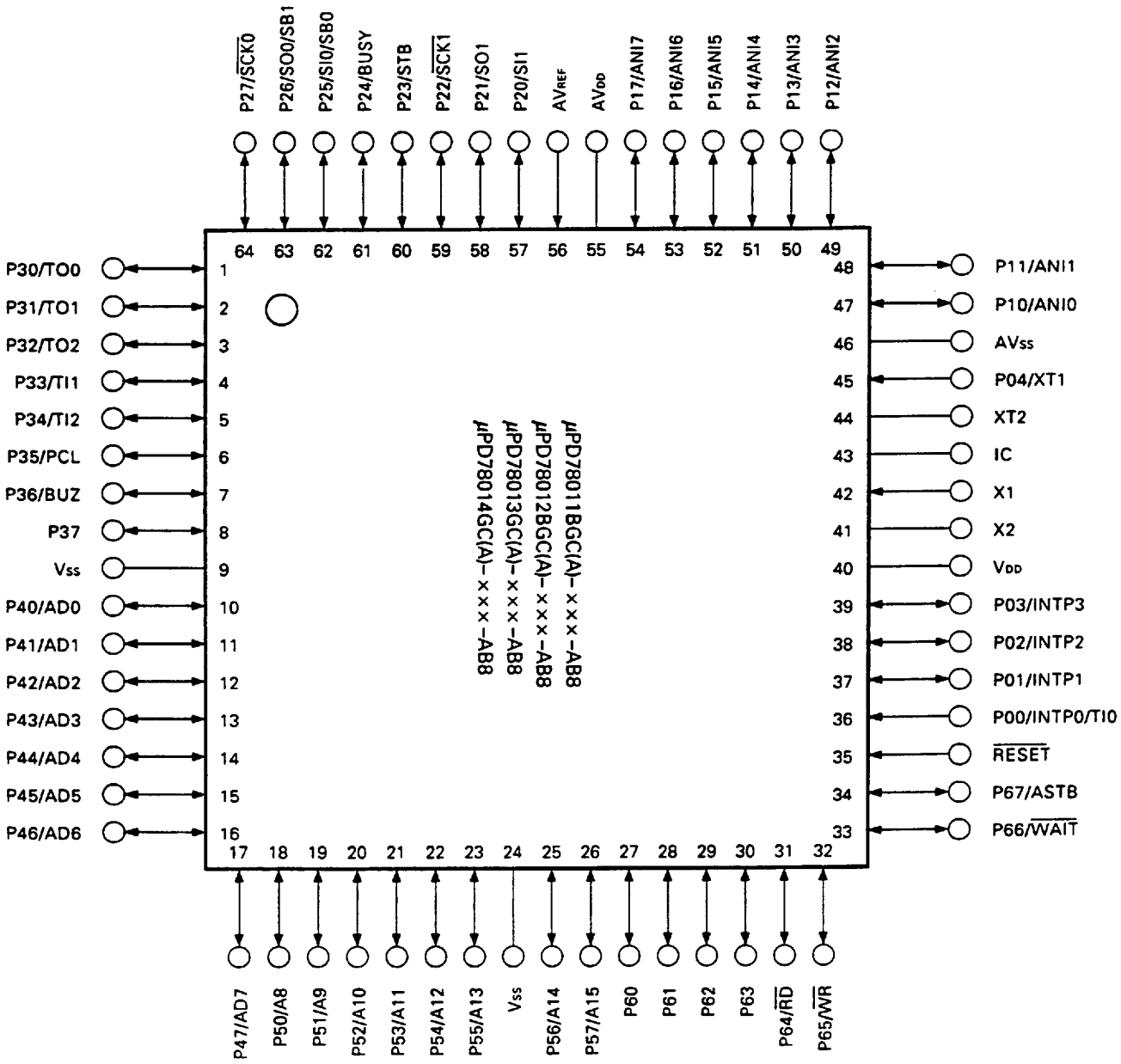
1. PIN CONFIGURATION (TOP VIEW)

64-pin plastic shrink DIP (750 mil)



Note
1. **Always connect the IC (Internally Connected) pin to Vss.**
2. **Always connect the AVDD pin to VDD.**
3. **Always connect the AVss pin to Vss.**

64-pin plastic QFP (□14 mm)

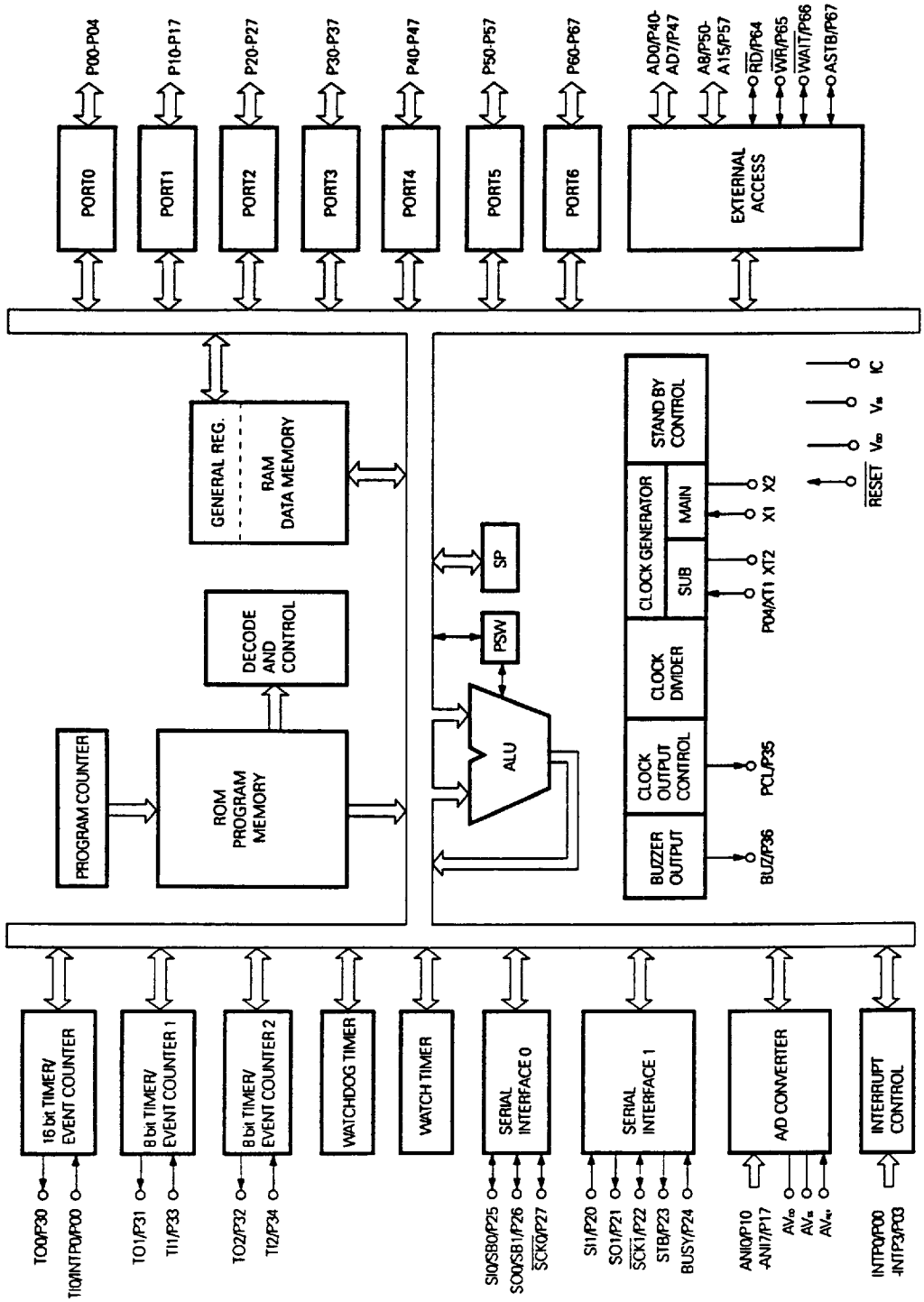


Note
1. **Always connect the IC (Internally Connected) pin to Vss.**
2. **Always connect the AVDD pin to VDD.**
3. **Always connect the AVss pin to Vss.**

P00 to P04	:	Port 0
P10 to P17	:	Port 1
P20 to P27	:	Port 2
P30 to P37	:	Port 3
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P60 to P67	:	Port 6
INTP0 to INTP3	:	Interrupt From Peripherals
TI0 to TI2	:	Timer Input
TO0 to TO2	:	Timer Output
SB0, SB1	:	Serial Bus
SI0, SI1	:	Serial Input
SO0, SO1	:	Serial Output
$\overline{SCK0}$, $\overline{SCK1}$	:	Serial Clock
PCL	:	Programmable Clock
BUZ	:	Buzzer Clock
STB	:	Strobe
BUSY	:	Busy

AD0 to AD7	:	Address/Data Bus
A8 to A15	:	Address Bus
$\overline{RD}$	:	Read Strobe
$\overline{WR}$	:	Write Strobe
$\overline{WAIT}$	:	Wait
ASTB	:	Address Strobe
X1, X2	:	Crystal (Main System Clock)
XT1, XT2	:	Crystal (Subsystem Clock)
$\overline{RESET}$	:	Reset
ANI0 to ANI7	:	Analog Input
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
AV_{REF}	:	Analog Reference Voltage
V_{DD}	:	Power Supply
V_{SS}	:	Ground
IC	:	Internally Connected

2. BLOCK DIAGRAM



Note Internal ROM & RAM capacity varies depending on the product.

3. PIN FUNCTION LIST

3.1 PORT PINS (1/2)

Pin Name	I/O	Function		At Reset	Dual-Function Pin
P00	Input	Port 0 5-bit I/O port	Input only	Input	INTP0/TI0
P01	Input/output		Input/output can be specified in bit-wise. When used as an input port, pull-up resistor can be used by software.	Input	INTP1
P02					INTP2
P03					INTP3
P04*1	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port. Input/output can be specified in bit-wise. When used as an input port, pull-up resistor can be used by software.*2		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port. Input/output can be specified in bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	Input/output	Port 3 8-bit input/output port. Input/output can be specified in bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, pull-up resistor can be used by software. Test flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

* 1. When using the P04/XT1 pins as an input port, do not use the on-chip feedback resistor of the subsystem clock oscillator with bit 6 (FRC) of the processor control register set to 1.

2. When using the P10/ANI0 to P17/ANI7 pins as the A/D converter analog input, pull-up resistor is automatically unused.

3.1 PORT PINS (2/2)

Pin Name	I/O	Function		At Reset	Dual-Function Pin
P50 to P57	Input/output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified in bit-wise. When used as an input port, pull-up resistor can be used by software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port. Input/output can be specified in bit-wise.	N-ch open-drain input/output port. On-chip pull-up resistor can be specified by mask option. LED can be driven directly.	Input	—
P61					
P62					
P63					
P64			When used as an input port, pull-up resistor can be used by software.		$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB

Note **Non-use of internal pull-up resistor (specified by mask option) increases low-level input leakage current in 200 μA (MAX.) in either of the following cases:**

① When the low-level input is performed to the pin using the external device expansion function.

② For 3-clock cycle when the port 6 (P6)/port mode register (PM6) read instruction execution is performed.

3.2 NON-PORT PINS (1/2)

Pin Name	I/O	Function	At Reset	Dual-Function Pin
INTP0	Input	External interrupt input by which the effective edge (rising edge, falling edge, or both rising edge and falling edge) can be specified.	Input	P00/TI0
INTP1				P01
INTP2				P02
INTP3		Falling edge detection external interrupt input.		P03
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SB0	Input /output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input /output	Serial interface serial clock input/output	Input	P27
$\overline{SCK1}$				P22
STB	Output	Serial interface automatic transmit/receive strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmit/receive busy input.	Input	P24
TI0	Input	External count clock input to 16-bit timer (TM0).	Input	P00/INTP0
TI1		External count clock input to 8-bit timer (TM1).		P33
TI2		External count clock input to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer (TM0) output (shared as 14-bit PWM output).	Input	P30
TO1		8-bit timer (TM1) output.		P31
TO2		8-bit timer (TM2) output.		P32
PCL	Output	Clock output (for main system clock, subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
AD0 to AD7	Input /output	Low-order address/data bus at external memory expansion.	Input	P40 to P47
A8 to A15	Output	High-order address bus at external memory expansion.	Input	P50 to P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Strobe output which latches the address information output at ports 4, 5 to access external memory.	Input	P67

3.2 NON-PORT PINS (2/2)

Pin Name	I/O	Function	At Reset	Dual-Function Pin
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AVREF	Input	A/D converter reference voltage input.	—	—
AVDD	—	A/D converter analog power supply. Connected to VDD.	—	—
AVSS	—	A/D converter ground potential. Connected to Vss.	—	—
$\overline{\text{RESET}}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P04
XT2	—		—	—
VDD	—	Positive power supply.	—	—
Vss	—	Ground potential.	—	—
IC	—	Internal connection. Connected directly to Vss.	—	—

3.3 PIN I/O CIRCUITS AND RECOMMENDED CONNECTION OF UNUSED PINS

The input/output circuit type of each pin and recommended connection of unused pins are shown in Table 3-1.

For the input/output circuit configuration of each type, see Fig. 3-1.

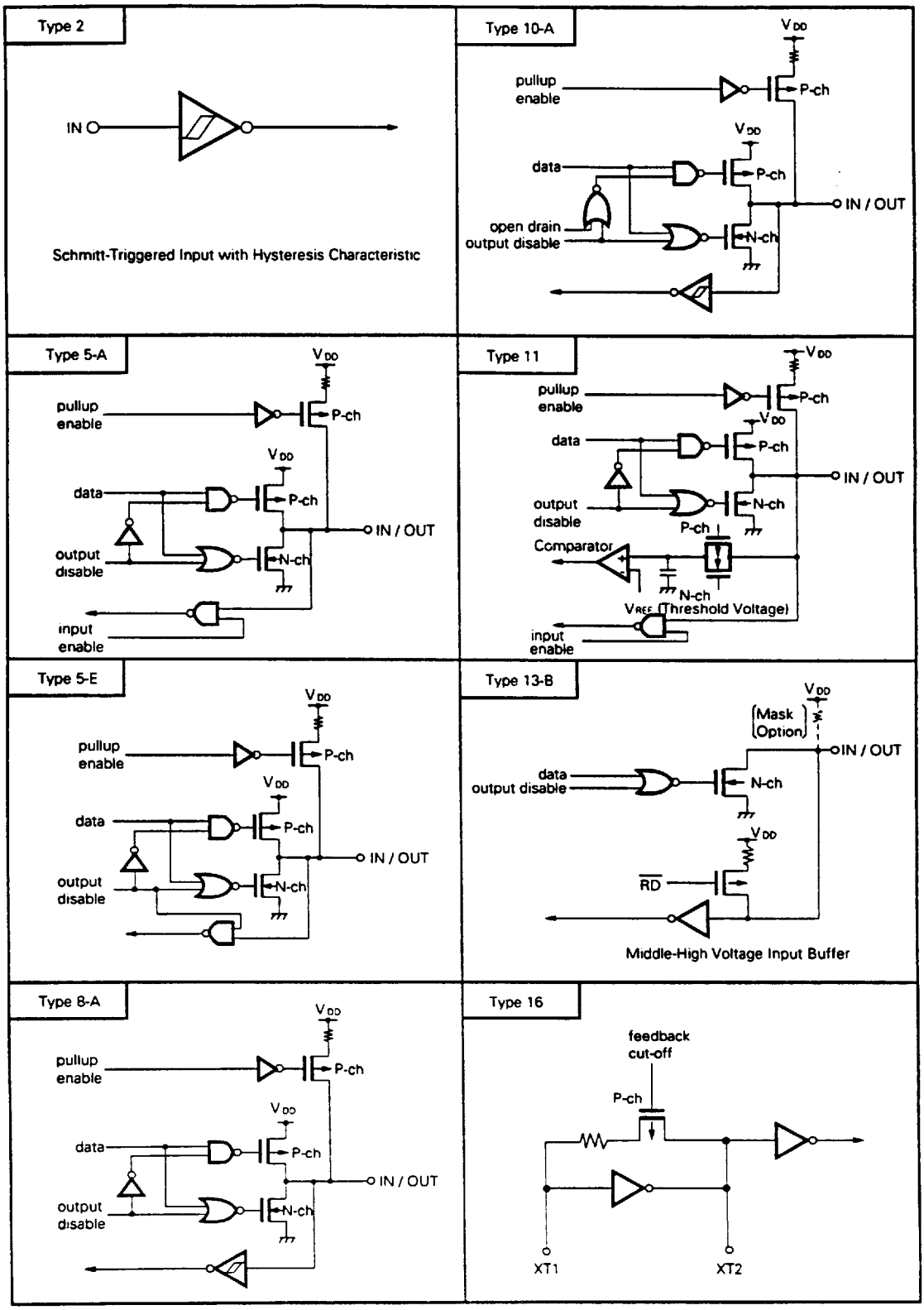
Table 3-1 Input/Output Circuit Type of Each Pin (1/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
P00/INTP0/TI0	2	Input	Connected to Vss.
P01/INTP1	8-A	Input/output	Input : Connected to Vss. Output : Leave open.
P02/INTP2			
P03/INTP3			
P04/XT1	16	Input	Connected to Vss.
P10/ANI0 to P17/ANI7	11	Input/output	Input : Connected to VDD or Vss. Output : Leave open.
P20/SI1	8-A	Input/output	Input : Connected to VDD or Vss. Output : Leave open.
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-A	Input/output	Input : Connected to VDD or Vss. Output : Leave open.
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E	Input/output	Input : Connected to VDD or Vss. Output : Leave open.
P50/A8 to P57/A15	5-A	Input/output	Input : Connected to VDD or Vss. Output : Leave open.
P60 to P63	13-B		
P64/$\overline{RD}$	5-A		
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			

Table 3-1 Input/Output Circuit Type of Each Pin (2/2)

Pin Name	Input/output Circuit Type	I/O	Recommended Connection when not Used
$\overline{\text{RESET}}$	2	Input	—
XT2	16	—	Leave open.
AVREF	—		Connected to Vss.
AVDD			Connected to VDD.
AVSS			Connected to Vss.
IC			Connected directly to Vss.

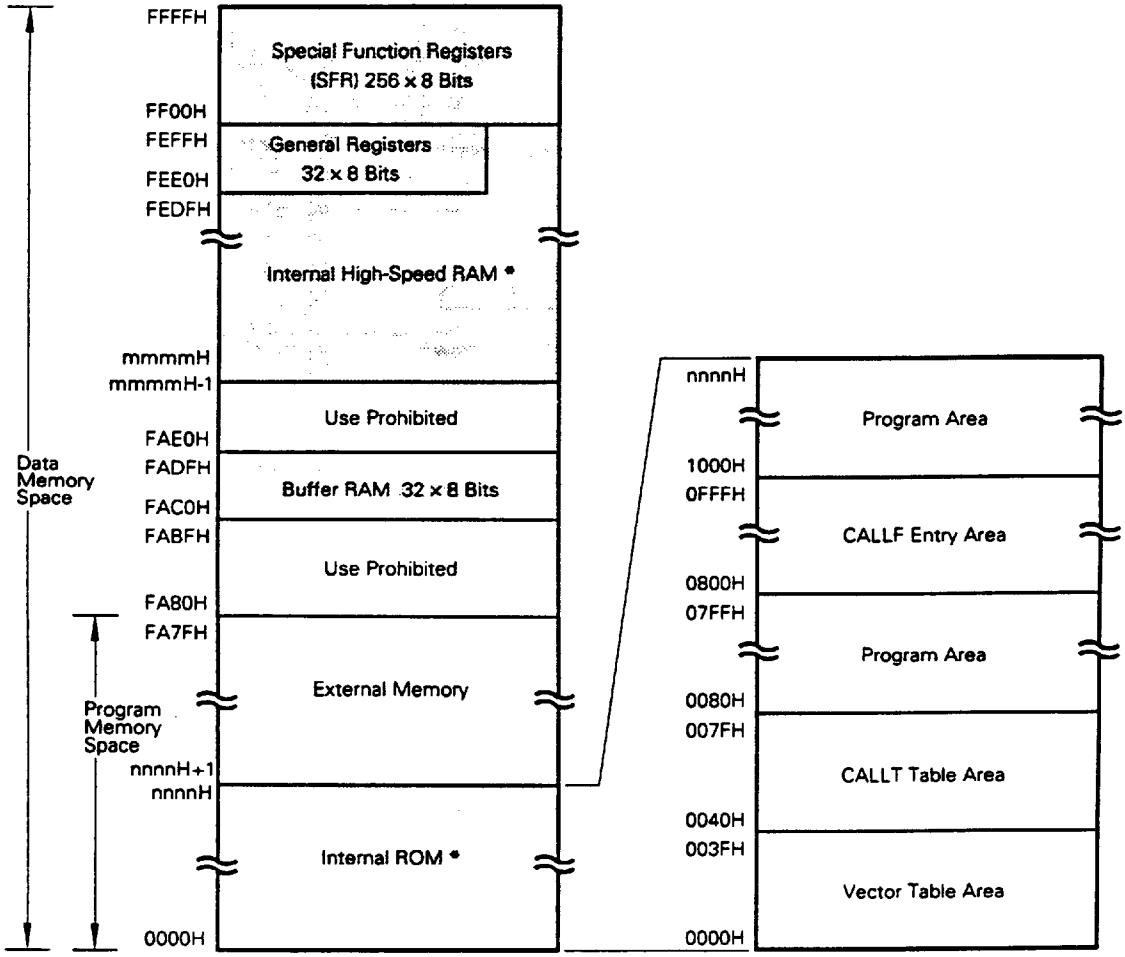
Fig. 3-1 Pin Input/Output Circuits



4. MEMORY SPACE

Memory map of μPD78011B(A), 78012B(A), 78013(A) and 78014(A) is shown in Table 4-1.

Fig. 4-1 Memory Map



* Internal ROM/internal high-speed RAM capacitance depends on product (See the table below)

Product Name	Internal ROM End Address nnnnH	Internal High-Speed RAM Initial Address mmmmH
μPD78011B(A)	1FFFH	FD00H
μPD78012B(A)	3FFFH	
μPD78013(A)	5FFFH	FB00H
μPD78014(A)	7FFFH	

Remarks Shaded area indicates internal memory.

5. CHARACTERISTICS OF PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

The following 3 I/O ports are set:

- CMOS input (P00, P04) : 2
- CMOS input/output (P01 to P03, port 1 to port 5, P64 to P67) : 47
- N-ch open drain input/output (15 V withstand voltage)(P60 to P63) : 4

Total : 53

Table 5-1 Functions of Ports

Name	Pin Name	Function
Port 0	P00, P04	Input only port
	P01 to P03	I/O port. I/O specifiable bit-wise. When used as an input port, internal pull-up resistor can be used by software.
Port 1	P10 to P17	I/O port. I/O specifiable bit-wise. When used as an input port, internal pull-up resistor can be used by software.
Port 2	P20 to P27	I/O port. I/O specifiable bit-wise. When used as an input port, internal pull-up resistor can be used by software.
Port 3	P30 to P37	I/O port. I/O specifiable bit-wise. When used as an input port, internal pull-up resistor can be used by software.
Port 4	P40 to P47	I/O port. I/O specifiable in 8-bit unit. When used as an input port, internal pull-up resistor can be used by software. Test flag (KRIF) is set to 1 by falling edge detection.
Port 5	P50 to P57	I/O port. I/O specifiable bit-wise. When used as an input port, internal pull-up resistor can be used by software. LED can be driven directly.
Port 6	P60 to P63	N-ch open-drain I/O port. I/O specifiable bit-wise. Pull-up resistor can be incorporated by mask option. LED can be driven directly.
	P64 to P67	I/O port. I/O specifiable bit-wise. When used as an input port, internal pull-up resistor can be used by software.

Note **Non-use of internal pull-up resistor (specified by mask option) increases low-level input leakage current in 200μA (MAX.) in either of the following cases:**

① When the low-level input is performed to the pin using the external device expansion function is used.

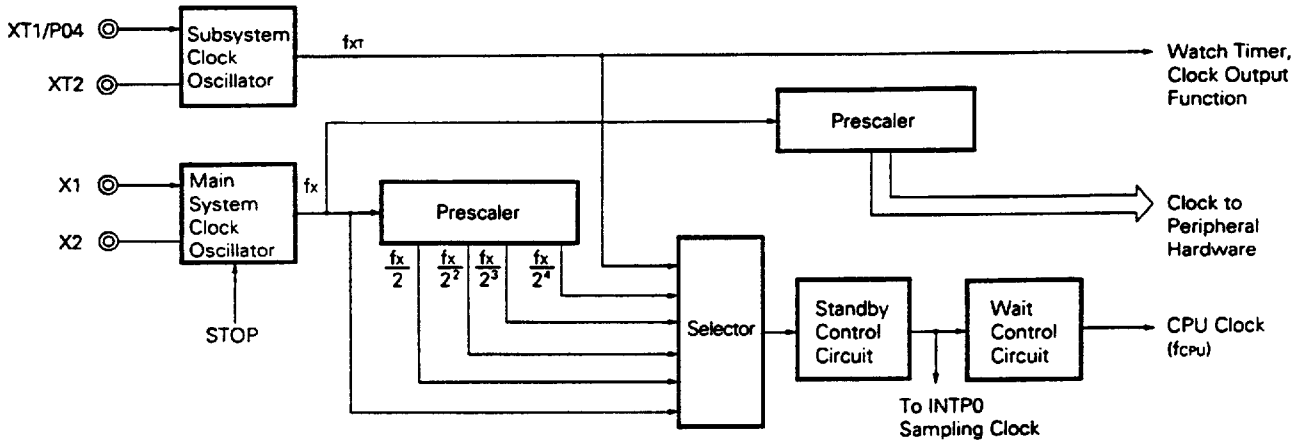
② For 3-clock cycle when the port6 (P6)/port mode register (PM6) read instruction execution is performed.

5.2 CLOCK GENERATOR

Clock generator includes main system clock generator and subsystem clock generator and can also change instruction execution time.

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (Main system clock: operation at 10.0 MHz)
- 122 μs (Subsystem clock: operation at 32.768 kHz)

Fig. 5-1 Clock Generator Block Diagram



5.3 TIMER/EVENT COUNTER

5 channels of timer/event counters are incorporated.

- 16-bit timer/event counter : 1 channel
- 8-bit timer/event counter : 2 channels
- Watch timer : 1 channel
- Watchdog timer : 1 channel

Table 5-2 Type And Function of Timer/Event Counter

		16-bit Timer/ Event Counter	8-bit Timer/ Event Counter	Watch Timer	Watchdog Timer
Type	Interval timer	1 channel	2 channels	1 channel	1 channel
	External event counter	1 channel	2 channels	—	—
Function	Timer output	1 output	2 outputs	—	—
	PWM output	1 output	—	—	—
	Pulse width measurement	1 input	—	—	—
	Square-wave output	1 output	2 outputs	—	—
	Interrupt request	2	2	2	1

Fig. 5-2 16-bit Timer/Event Counter Block Diagram

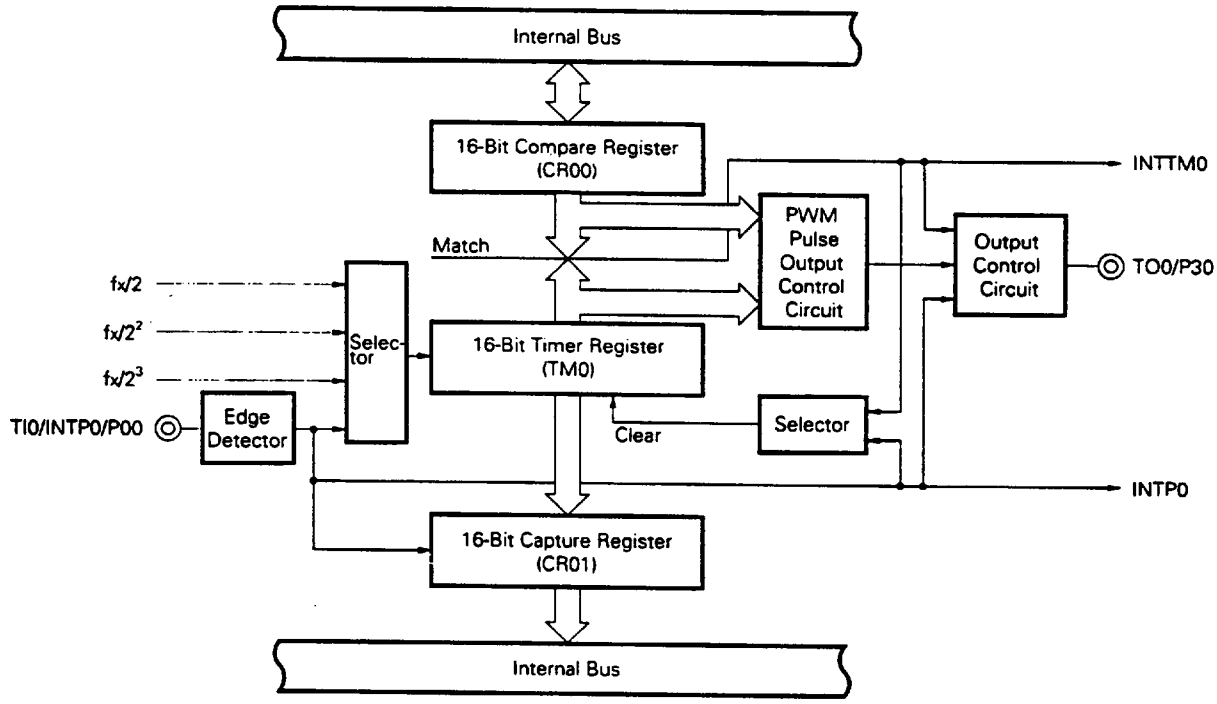


Fig. 5-3 8-Bit Timer/Event Counter Block Diagram

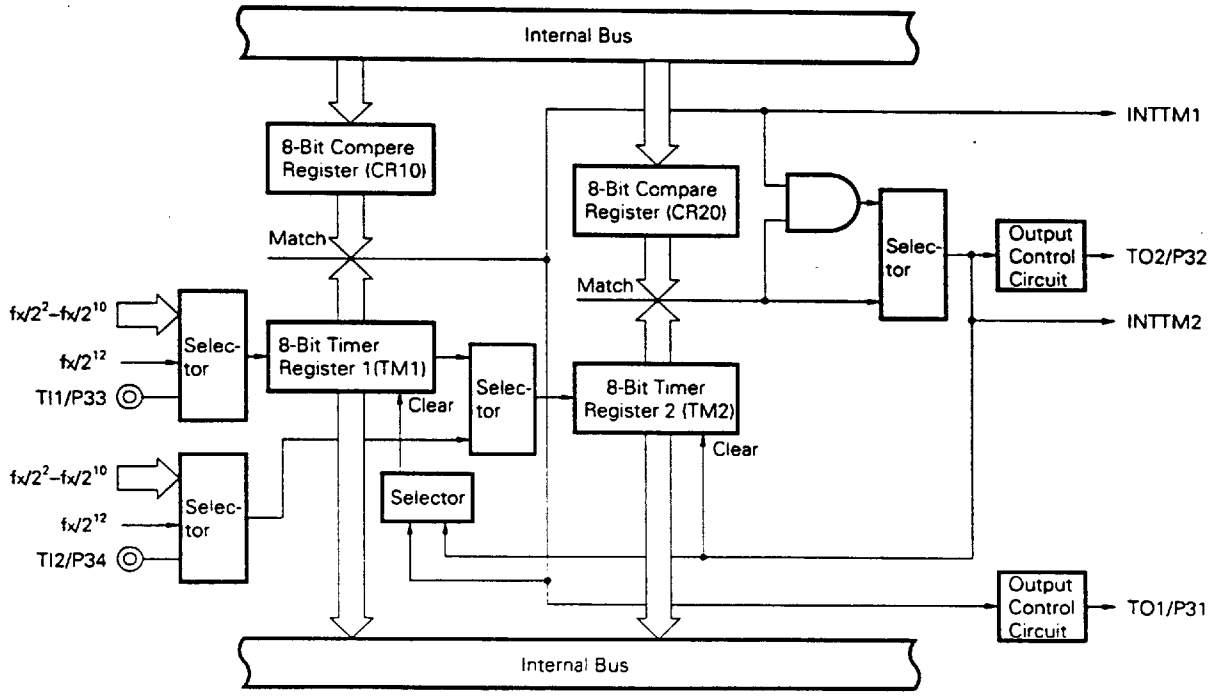


Fig. 5-4 Watch Timer Block Diagram

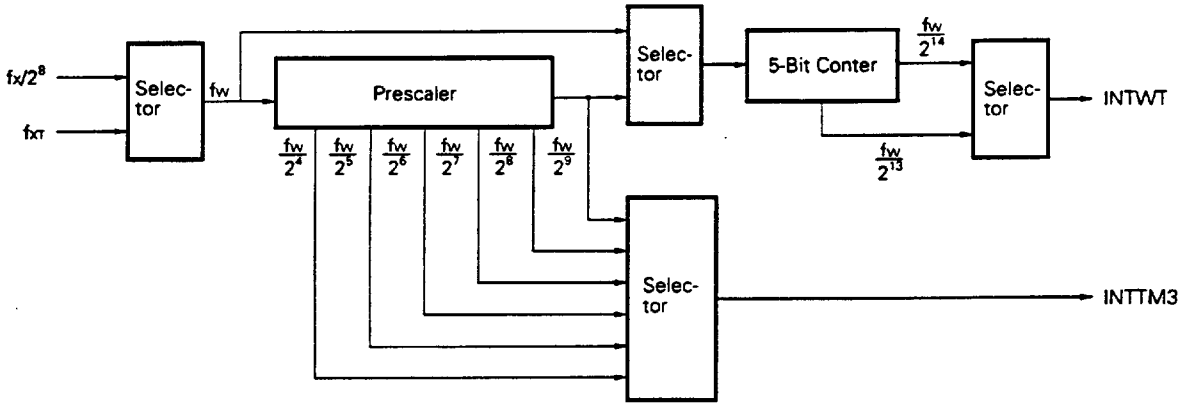
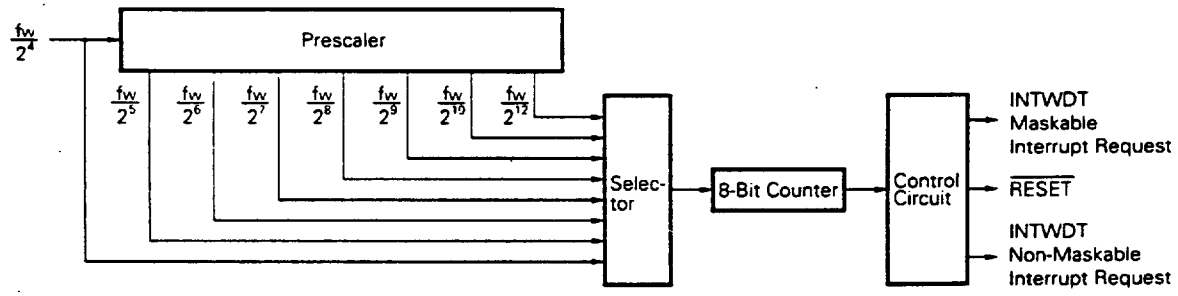


Fig. 5-5 Watchdog Timer Block Diagram

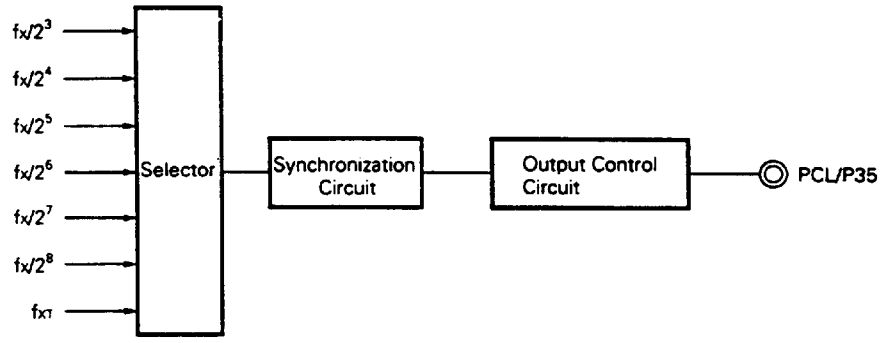


5.4 CLOCK OUTPUT CONTROL CIRCUIT

The following frequency clocks can be output as clock output:

- 1.25 kHz/625 kHz/313 kHz/156 kHz/78.1 kHz/39.1 MHz
  (Main system clock : operation at 10.0 MHz)
- 32.768 kHz
  (Subsystem clock : operation at 32.768 kHz)

Fig. 5-6 Clock Output Control Circuit Block Diagram

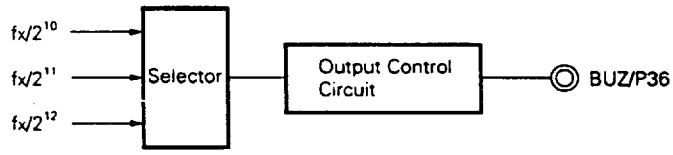


5.5 BUZZER OUTPUT CONTROL CIRCUIT

The following frequency clocks can be output as buzzer output:

- 2.4 kHz/4.9 kHz/9.8 kHz
  (Main system clock : operation at 10.0 MHz)

Figure 5-7 Buzzer Output Control Circuit Block Diagram

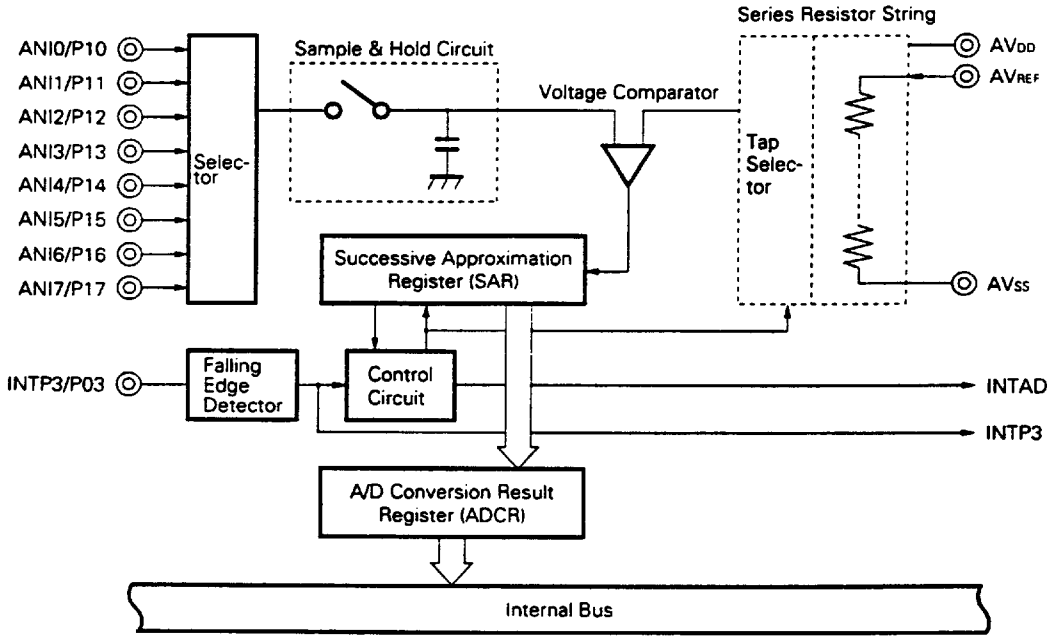


5.6 A/D CONVERTER

8-bit resolution 8-channel A/D converter is incorporated. The following 2 start methods are set for A/D conversion operation.

- Hardware start
- Software start

Fig. 5-8 A/D Converter Block Diagram



5.7 SERIAL INTERFACES

2 channels of clocked serial interface are incorporated.

- Serial interface channel 0
- Serial interface channel 1

Table 5-3 Type And Function of Serial Interface

Function	Serial interface channel 0	Serial interface channel 1
3 wires serial I/O mode	○ (MSB/LSB start switchable)	○ (MSB/LSB start switchable)
3 wires serial I/O mode with automatic transmission /reception function	—	○ (MSB/LSB start switchable)
SBI (Serial bus interface) mode	○ (MSB start)	—
2 wires serial I/O mode	○ (MSB start)	—

Fig. 5-9 Serial Interface Channel 0 Block Diagram

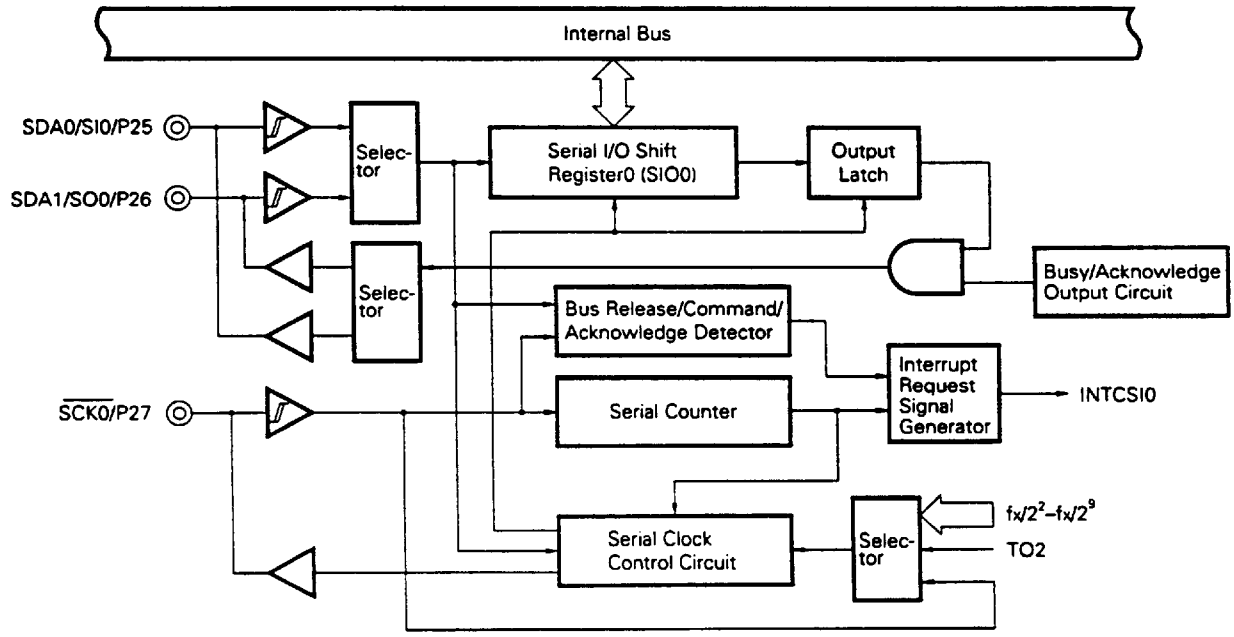
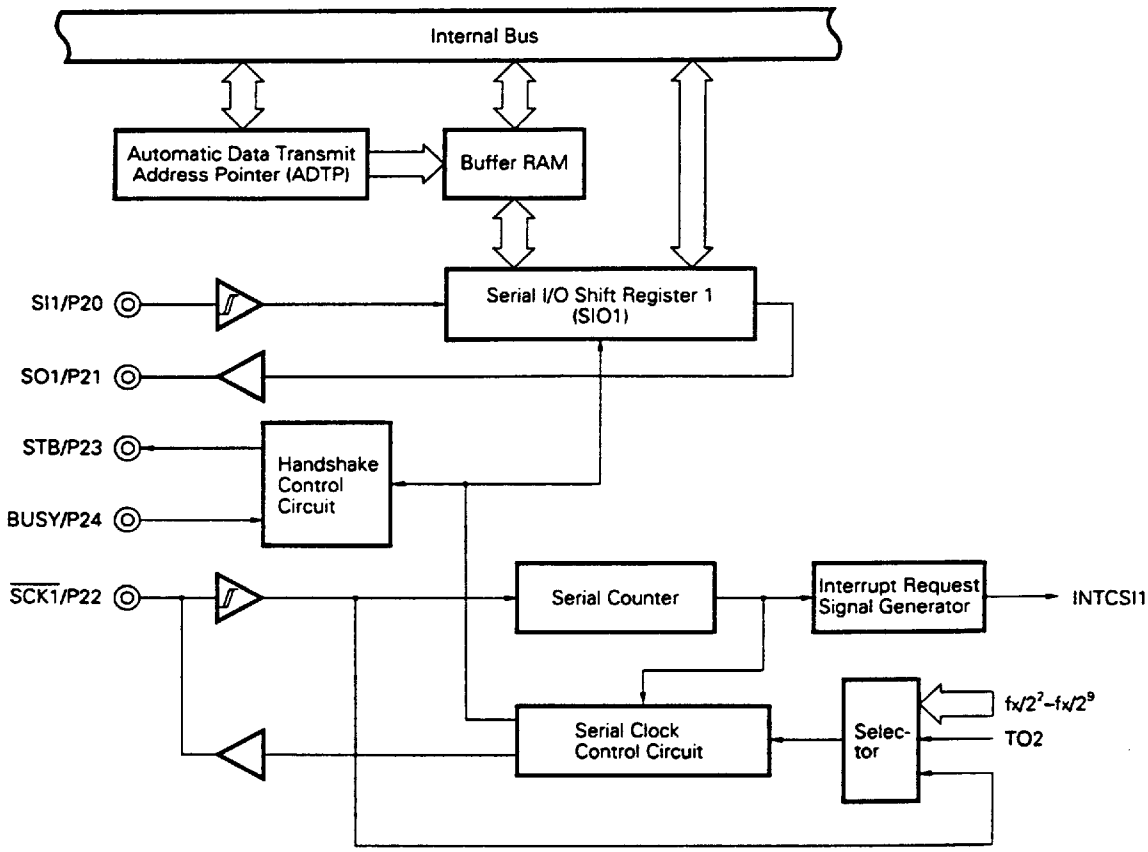


Fig. 5-10 Serial Interface Channel 1 Block Diagram



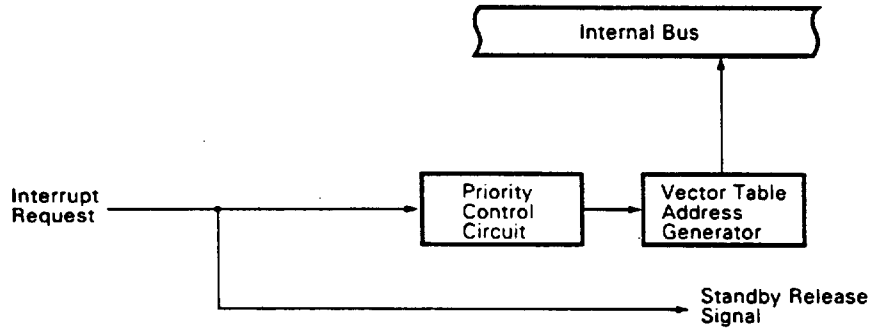
6. INTERRUPT FUNCTIONS AND TEST FUNCTIONS

The following 4 types are available:

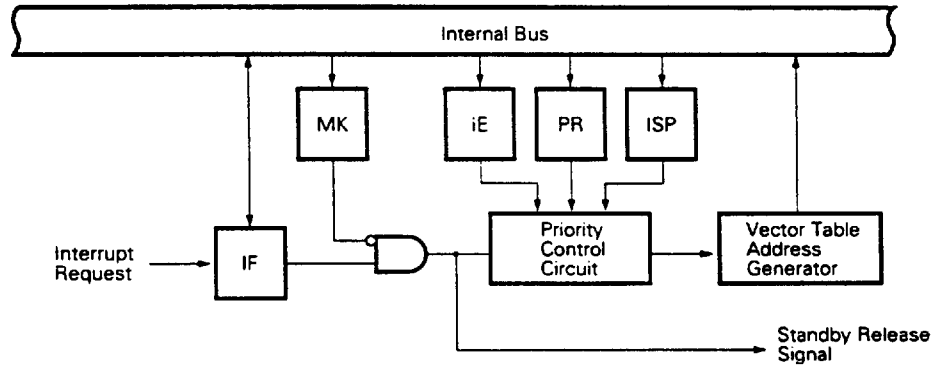
- Non-maskable interrupt : 2
- Maskable interrupt : 12
- Software interrupt : 1
- Test input : 2

Fig. 6-1 Interrupt Function Basic Configuration (1/3)

(A) Internal non-maskable interrupt

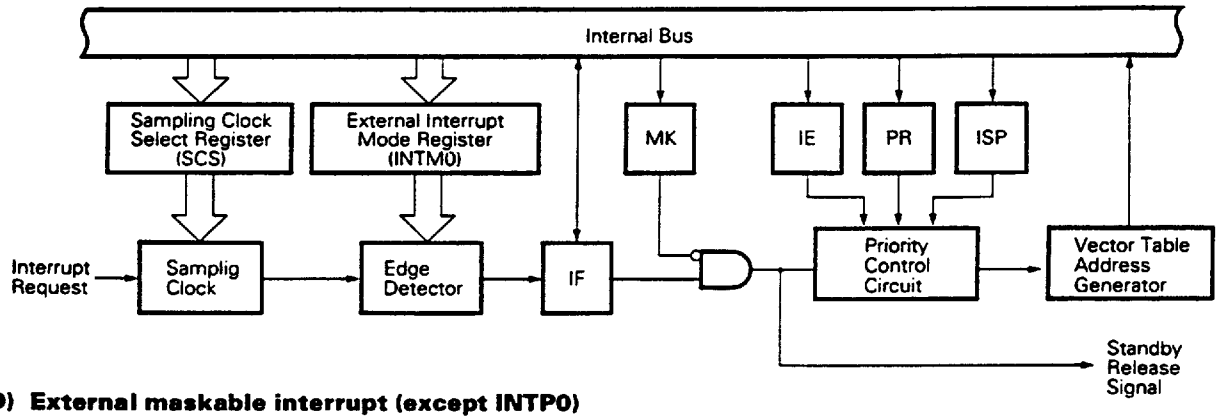


(B) Internal maskable interrupt



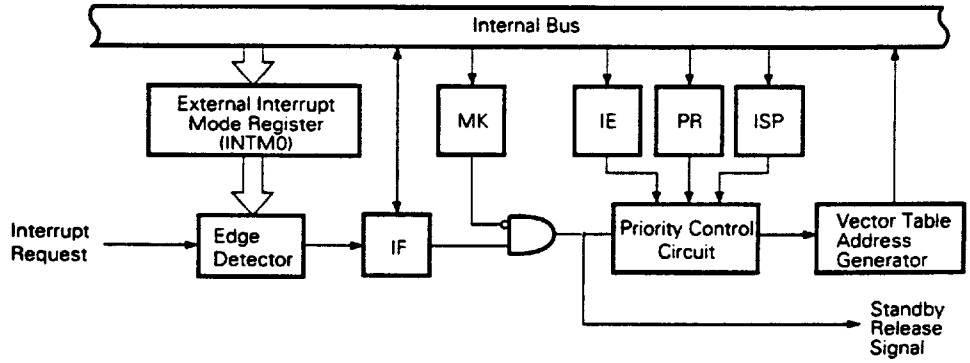
(C) External maskable interrupt (INTP0)

Fig. 6-1 Interrupt Function Basic Configuration (2/3)

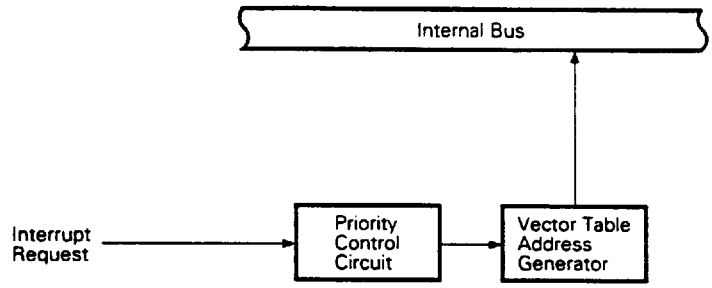


(D) External maskable interrupt (except INTP0)

Fig. 6-1 Interrupt Function Basic Configuration (3/3)

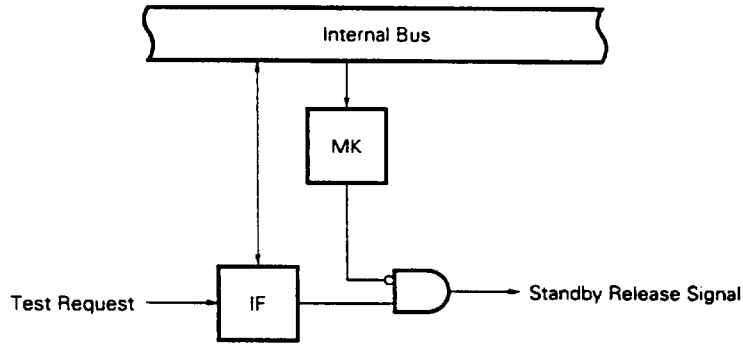


(E) Software interrupt



Remarks
1. IF : Interrupt request flag
2. IE : Interrupt enable flag
3. ISP : In-service priority flag
4. MK : Interrupt mask flag
5. PR : Priority specification flag

(F) Test input



7. EXTERNAL DEVICE EXPANSION FUNCTIONS

The external device expansion functions connect external devices to areas other than the internal ROM, RAM and SFR.

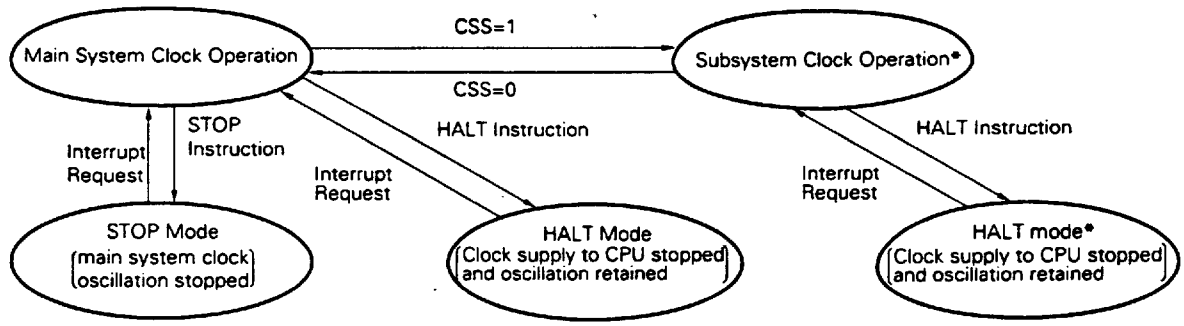
External devices connection uses ports 4 to 6.

8. STANDBY FUNCTION

There are the following two standby functions to reduce the system power cunsumption.

- ○ HALT mode : In this mode, the CPU operation clock is stopped. The average consumption current can be reduced by intermittent operation in combination with the normal operation.
- ○ STOP mode : In this mode, the main system clock oscillator is stopped. The power consumption are greatly reduced to subsystem clock only by stopping the whole main system, clock operations.

Figure 8-1 Standby Function



* Stopping the main system clock enables the consumption current to be reduced. If the CPU is operated by the subsystem clock, the main system clock should be stopped by the MCC set. STOP instruction is not available.

Note If the CPU is operated by the subsystem clock when the main system clock is stopped, reswitching to the main system should be performed after the stable oscillation time has been obtained by the program.

9. RESET FUNCTION

There are the following two reset methods.

- External reset by $\overline{\text{RESET}}$ pin
- Internal reset by watchdog time runaway time detection

10. INSTRUCTION SET

(1) 8-Bit Instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

First Operand \ Second Operand	#byte	A	r*	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL + byte] [HL + B] [HL + C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
r1											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]		MOV											
[HL]		MOV											ROR4 ROL4
[HL + byte] [HL + B] [HL + C]		MOV											
X													MULU
C													DIVUW

* Except r = A

(2) 16-Bit Instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First Operand \ Second Operand	#word	AX	rp*	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW*						INCW, DECW PUSH, POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addrp16		MOVW						
SP	MOVW	MOVW						

* Only in the case of rp = BC, DE, HL

(3) Bit Manipulation Instructions

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

First Operand \ Second Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call Instruction/Branch Instructions

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

First Operand \ Second Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic Instruction	BR	CALL, BR	CALLF	CALLT	BR, BC, BNC, BZ, BNZ
Compound Instruction					BT, BF, BTCLR, DBNZ

(5) Other Instructions

ADJBA, ADJBS, BRK, RET, RET1, RETB, SEL, NOP, EI, DI, HALT, STOP

11. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

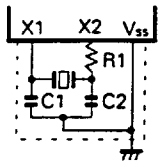
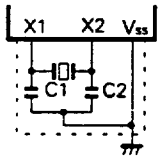
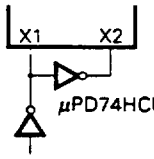
PARAMETER	SYMBOL	TEST CONDITIONS		RATING	UNIT
Supply voltage	V_{DD}			−0.3 to + 7.0	V
	AV_{DD}			−0.3 to V_{DD} + 0.3	V
	AV_{REF}			−0.3 to V_{DD} + 0.3	V
	AV_{SS}			−0.3 to + 0.3	V
Input voltage	V_{I1}	P00 to P04, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, X1, X2, XT2		−0.3 to V_{DD} + 0.3	V
	V_{I2}	P60 to P63	Open-drain	−0.3 to +16	V
Output voltage	V_O			−0.3 to V_{DD} + 0.3	V
Analog input voltage	V_{AN}	P10 to P17	Analog input pin	AV_{SS} −0.3 to AV_{REF} + 0.3	V
Output current high	I_{OH}	1 pin		−10	mA
		P10 to P17, P20 to P27, P30 to P37 total		−15	mA
		P01 to P03, P40 to P47, P50 to P57, P60 to P67 total		−15	mA
Output current low	I_{OL}*	1 pin	Peak value	30	mA
			Effective value	15	mA
		P40 to P47, P50 to P55 total	Peak value	100	mA
			Effective value	70	mA
		P01 to P03, P56, P57, P60 to P67 total	Peak value	100	mA
			Effective value	70	mA
		P01 to P03, P64 to P67 total	Peak value	50	mA
			Effective value	20	mA
		P10 to P17, P20 to P27, P30 to P37 total	Peak value	50	mA
			Effective value	20	mA
Operating temperature	T_{opt}			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

* Effective value should be calculated as follows: [Effective value] = [Peak value] × $\sqrt{\text{duty}}$

Note The product quality may be damaged even if a value of only one of the above parameters exceeds the absolute maximum rating or any value exceeds the absolute maximum rating for an instant. That is, the absolute maximum rating is a rating value which may cause a product to be damaged physically. The absolute maximum rating values must therefore be observed in using the product.

Remarks Unless specified otherwise, the characteristics of dual-function pins are the same as the those of port pins.

MAIN SYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (T_a = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator		Oscillator frequency (fx) *1	V_{DD} = Oscillator voltage range	1		10	MHz
		Oscillation stabilization time *2	After V_{DD} reaches oscillator voltage range MIN.			4	ms
Crystal resonator		Oscillator frequency (fx) *1		1	8.38	10	MHz
		Oscillation stabilization time *2	V_{DD} = 4.5 to 6.0 V			10	ms
						30	
External clock		X1 input frequency (fx) *1		1.0		10.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		50		500	ns

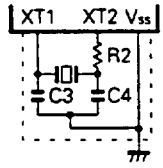
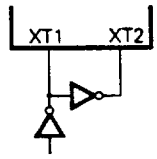
* 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.
2. Time required to stabilize oscillation after reset or STOP mode release.

Note 1. When using the main system clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as Vss.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. If the main system clock oscillation circuit is operated by the subsystem clock when the main system clock is stopped, reswitching to the main system clock should be performed after the stable oscillation time has been obtained by the program.

SUBSYSTEM CLOCK OSCILLATION CIRCUIT CHARACTERISTICS (Ta = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal resonator		Oscillator frequency (f_{XT}) *1		32	32.768	35	kHz
		Oscillation stabilization time *2	V_{DD} = 4.5 to 6.0 V		1.2	2	s
						10	
External clock		XT1 input frequency (f_{XT}) *1		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

* 1. Indicates only oscillation circuit characteristics. Refer to "AC Characteristics" for instruction execution time.

2. Time required to stabilize oscillation after V_{DD} has reached the minimum oscillation voltage range.

Note 1. When using the subsystem clock oscillator, wiring in the area enclosed with the dotted line should be carried out as follows to avoid an adverse effect from wiring capacitance.

- **Wiring should be as short as possible.**
- **Wiring should not cross other signal lines.**
- **Wiring should not be placed close to a varying high current.**
- **The potential of the oscillator capacitor ground should be the same as Vss.**
- **Do not ground it to the ground pattern in which a high current flows.**
- **Do not fetch a signal from the oscillator.**

2. The subsystem clock oscillation circuit is designed as a low amplification circuit to provide low consumption current, causing misoperation to noise more frequently than the main system clock oscillation circuit. Special care should therefore be taken to wiring method when the subsystem clock is used.

RECOMMENDED OSCILATION CIRCUIT CONSTANT

MAIN SYSTEM CLOCK: CERAMIC RESONATOR (Ta = –40 to +85 °C)

In the case of μPD78013(A)/78014(A)

MANU-FACTURER	PRODUCT NAME	FREQUENCY (MHZ)	RECOMMENDED CIRCUIT CONSTANT			OSCILLATOR VOLTAGE RANGE	
			C1 (pF)	C2 (pF)	R1 (kΩ)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSB1000J	1.00	100	100	6.8	2.7	6.0
	CSBxxxxJ	1.01 to 1.25	100	100	4.7	2.7	6.0
	CSAx. xxxMK	1.26 to 1.79	100	100	0	2.7	6.0
	CSAx. xxMG	1.80 to 2.44	100	100	0	2.7	6.0
	CSTx. xxMG		Built-in	Built-in	0	2.7	6.0
	CSAx. xxMG	2.45 to 4.18	30	30	0	2.7	6.0
	CSTx. xxMGW		Built-in	Built-in	0	2.7	6.0
	CSAx. xxMG	4.19 to 6.00	30	30	0	2.7	6.0
	CSTx. xxMGW		Built-in	Built-in	0	2.7	6.0
	CSAx. xxMT	6.01 to 10.0	30	30	0	2.7	6.0
	CSTx. xxMTW		Built-in	Built-in	0	2.7	6.0

Remarks x. xx, xxxx, x. xxx indicates frequency.

SUBSYSTEM CLOCK: CRYSTAL RESONATOR (Ta = –40 to + 60 °C)

In the case of μPD78013(A)/78014(A)

MANU-FACTURER	PRODUCT NAME	FREQUENCY (kHz)	RECOMMENDED CIRCUIT CONSTANT			OSCILLATOR VOLTAGE RANGE	
			C3 (pF)	C4 (pF)	R2 (kΩ)	MIN. (V)	MAX. (V)
Daishinku	DT-38 (1TA252E00, load capacitance 6.3 pF)	32.768	12	12	100	2.7	6.0

Note With the oscillator constants, operation is guaranteed but not reliability. Customers requiring high reliability should contact the resonator manufacturer directly.

CAPACITANCE (Ta = 25 °C, V_{DD} = Vss = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	f = 1M Hz Unmeasured pins returned to 0 V.				15	pF
I/O capacitance	C_{IO}	f = 1 MHz Unmeasured pins returned to 0 V.	P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67			15	pF
			P60 toP63			20	pF

Remarks Unless specified otherwise, the characteristics of dual-function pins are the same as those of port pins.

DC CHARACTERISTICS (Ta = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67		0.7 V_{DD}		V_{DD}	V
	V_{IH2}	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{RESET}$		0.8 V_{DD}		V_{DD}	V
	V_{IH3}	P60 to P63	Open-drain	0.7 V_{DD}		15	V
	V_{IH4}	X1, X2		V_{DD}−0.5		V_{DD}	V
	V_{IH5}	XT1/P04, XT2	V_{DD} = 4.5 to 6.0 V	V_{DD}−0.5		V_{DD}	V
				V_{DD}−0.3		V_{DD}	V
Input voltage low	V_{IL1}	P10 to P17, P21, P23, P30 to P32, P35 to P37, P40 to P47, P50 to P57, P64 to P67		0		0.3 V_{DD}	V
	V_{IL2}	P00 to P03, P20, P22, P24 to P27, P33, P34, $\overline{RESET}$		0		0.2 V_{DD}	V
	V_{IL3}	P60 to P63	V_{DD} = 4.5 to 6.0 V	0		0.3 V_{DD}	V
				0		0.2 V_{DD}	V
	V_{IL4}	X1, X2		0		0.4	V
	V_{IL5}	XT1/P04, XT2	V_{DD} = 4.5 to 6.0 V	0		0.4	V
				0		0.3	V
Output voltage high	V_{OH1}	V_{DD} = 4.5 to 6.0 V, I_{OH} = −1 mA		V_{DD}−1.0			V
		I_{OH} = −100 μA		V_{DD}−0.5			V
Output voltage low	V_{OL1}	P50 to P57, P60 to P63	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.4	2.0	V
		P01 toP03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P64 to P67	V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA			0.4	V
	V_{OL2}	SB0, SB1, $\overline{SCK0}$	V_{DD} = 4.5 to 6.0 V, open-drain pulled-up (R = 1 KΩ)			0.2 V_{DD}	V
	V_{OL3}	I_{OL} = 400 μA				0.5	V
Input leakage current high	I_{LIH1}	V_{IN} = V_{DD}	P00 toP03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, $\overline{RESET}$			3	μA
	I_{LIH2}		X1, X2, XT1/P04, XT2			20	μA
	I_{LIH3}	V_{IN} = 15 V	P60 to P63			80	μA
Input leakage current low	I_{LIL1}	V_{IN} = 0 V	P00 toP03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67, RESET			−3	μA
	I_{LIL2}		X1, X2, XT1/P04, XT2			−20	μA
	I_{LIL3}		P60 to P63 *1			−200	μA
			P60 to P63 Other than above			−3*2	μA

* 1. When memory expansion mode is used by the memory expansion mode register (MM) with no on-chip pull-up resistor by mask option.

2. Non-use of pull-up resistor (specified by mask option) increases low-level input leakage current in 200 μA(MAX.) in either of the following cases:

① When the low-level input is performed to the pin using the external device expansion function is used.

② For 3-clock cycle when the port 6 (P6)/port mode register (PM6) read instruction execution is performed.

Remarks Unless specified otherwise, the characteristics of dual-function pins are the same as the those of port pins.

DC CHARACTERISTICS (Ta = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Output leakage current high	I_{LOH1}	V_{OUT} = V_{DD}				3	μA
Output leakage current low	I_{LOL}	V_{OUT} = 0 V				−3	μA
Mask option pull-up resister	R_1	V_{IN} = 0 V, P60 to P63		20	40	90	kΩ
Software pull-up resister	R_2	V_{IN} = 0 V, P01 to P03, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P64 to P67	4.5 V ≤ V_{DD} ≤ 6.0 V	15	40	90	kΩ
			2.7 V ≤ V_{DD} ≤ 4.5 V	20		500	kΩ
Power supply current*3	I_{DD1}	8.38 MHz, Crystal oscillation operating mode	V_{DD} = 5.0 V ± 10 %*1		7.5	22.5	mA
			V_{DD} = 3.0 V ± 10 %*2		0.8	2.4	mA
	I_{DD2}	8.38 MHz, Crystal oscillation HALT mode	V_{DD} = 5.0 V ± 10 %		1.4	4.2	mA
			V_{DD} = 3.0 V ± 10 %		550	1650	μA
	I_{DD3}	32,768 kHz, Crystal oscilation operating mode	V_{DD} = 5.0 V ± 10 %		60	120	μA
			V_{DD} = 3.0 V ± 10 %		35	70	μA
	I_{DD4}	32,768 kHz, Crystal oscilation HALT mode	V_{DD} = 5.0 V ± 10 %		25	50	μA
			V_{DD} = 3.0 V ± 10 %		5	10	μA
	I_{DD5}	XT1 = 0 V STOP mode When feedback resister is connected	V_{DD} = 5.0 V ± 10 %		1	20	μA
			V_{DD} = 3.0 V ± 10 %		0.5	10	μA
	I_{DD6}	XT1 = 0 V STOP mode When feedback resister is disconnected	V_{DD} = 5.0 V ± 10 %		0.1	20	μA
			V_{DD} = 3.0 V ± 10 %		0.05	10	μA

* 1. Operating in high-speed mode (when set the processor clock control register to 00H).
2. Operating in low-speed mode (when set the processor clock control register to 04H).
3. AV_{REF} current and port current are excluded.

Remarks Unless specified otherwise, the characteristics of dual-function pins are the same as the those of port pins.

AC CHARACTERISTICS (Ta = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

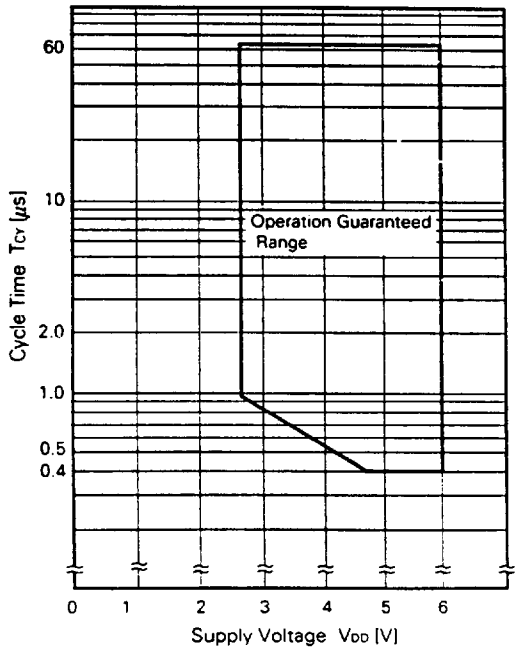
(1) Basic operation

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Cycle time (Min. instruction execution time)	T_{CY}	Operating on main system clock	V_{DD} = 4.5 to 6.0 V	0.4		64	μs
				0.96		64	μs
		Operating on subsystem clock		40	122	125	μs
TI input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		4	MHz
				0		275	kHz
TI input high/low-level width	t_{TIH} t_{TIL}	V_{DD} = 4.5 to 6.0 V		100			ns
				1.8			μs
Interrupt input high/low-level width	t_{INTH} t_{INTL}	INTP0		$8/f_{sam}$*			μs
		INTP1 to INTP3		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ low level width	t_{RST}			10			μs

* In combination with bits 0 (SCS0) and 1 (SCS1) of sampling clock select register, selection of f_{sam} is possible between $f_X/2^{N+1}$, $f_X/64$ and $f_X/128$ (when N = 0 to 4).

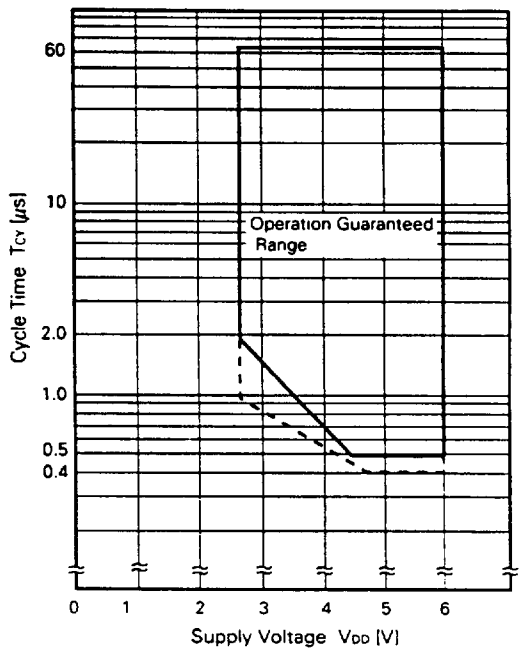
In the case of μPD78011B(A), 78012B(A), 78013(A) and 78014(A)

T_{CY} vs V_{DD} (At main system clock operation)



In the case of μPD78P014(Reference)

T_{CY} vs V_{DD} (At main system clock operation)



Remarks - - - - - - - - indicates Ta = −40 to +40°C

———— indicates Ta = −40 to +85°C

Note **The operating guaranteed range differs between μPD78011B(A), 78012B(A), 78013(A), 78014(A) and μPD78P014.**

(2) Read/write operation (Ta = −40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
ASTB high-level width	t_{ASTH}		0.5t_{CY}		ns
Address setup time	t_{ADS}		0.5t_{CY}−30		ns
Address hold time	t_{ADH}	Load resistor ≥ 5 kΩ	10		ns
Data input time from address	t_{ADD1}			(2+2n)t_{CY}−50	ns
	t_{ADD2}		5	(3+2n)t_{CY}−100	ns
Data input time from $\overline{RD}$↓	t_{RDD1}			(1+2n)t_{CY}−25	ns
	t_{RDD2}			(2.5+2n)t_{CY}−100	ns
Read data hold time	t_{RDH}		0		ns
$\overline{RD}$ low-level width	t_{RDL1}		(1.5+2n)t_{CY}−20		ns
	t_{RDL2}		(2.5+2n)t_{CY}−20		ns
$\overline{WAIT}$↓ input time from $\overline{RD}$↓	t_{RDWT1}			0.5t_{CY}	ns
	t_{RDWT2}			1.5t_{CY}	ns
$\overline{WAIT}$↓ input time from $\overline{WR}$↓	t_{WRWT}			0.5t_{CY}	ns
$\overline{WAIT}$ low-level width	t_{WTL}		(0.5+2n)t_{CY} +10	(2+2n)t_{CY}	ns
Write data setup time	t_{WDS}		100		ns
Write data hold time	t_{WDH}		5		ns
$\overline{WR}$ low-level width	t_{WRL1}		(2.5+2n)t_{CY} −20		ns
$\overline{RD}$↓ delay time from ASTB↓	t_{ASTRD}		0.5t_{CY}−30		ns
$\overline{WR}$↓ delay time from ASTB↓	t_{ASTWR}		1.5t_{CY} −30		ns
ASTB↑ delay time from $\overline{RD}$↑ in external fetch	t_{RDAST}		t_{CY}-10	t_{CY}+40	ns
Address hold time from $\overline{RD}$↑ in external fetch	t_{RDADH}		t_{CY}	t_{CY}+50	ns
Write data output time from $\overline{RD}$↑	t_{RDWD}		10		ns
$\overline{WR}$↓ delay time from write data	t_{WDWR}	V_{DD} = 4.5 to 6.0 V	0.5t_{CY}−120	0.5t_{CY}	ns
			0.5t_{CY}−170	0.5t_{CY}	ns
Address hold time from $\overline{WR}$↑	t_{WRADH}	V_{DD} =4.5 to 6.0 V	t_{CY}	t_{CY}+60	ns
			t_{CY}	t_{CY}+100	ns
$\overline{RD}$↑ delay time from $\overline{WAIT}$↑	t_{WTRD}		0.5t_{CY}	2.5t_{CY}+80	ns
$\overline{WR}$↑ delay time from $\overline{WAIT}$↑	t_{WTWR}		0.5t_{CY}	2.5t_{CY}+80	ns

Remarks 1. $t_{CY} = T_{CY}/4$

2. n indicates number of waits.

3. C_L = 100 pF(C_L indicates load capacitance of P40/AD0 to P47/AD7, P50/A8 to P57/A15, P64/$\overline{RD}$, P65/$\overline{WR}$, P66/$\overline{WAIT}$, P67/ASTB pins)

(3) Serial interface (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

(a) 3-wire serial I/O mode ($\overline{SCK}$... Internal clock output)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low-level width	t_{KH1}	V_{DD} = 4.5 to 6.0 V		t_{KCY1}/2-50			ns
	t_{KL1}			t_{KCY1}/2-150			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK1}			100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI1}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO1}	C = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

* C is the load capacitance of SO output line.

(b) 3-wire serial I/O mode ($\overline{SCK}$...External clock input)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low-level width	t_{KH2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KL2}			1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK2}			100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI2}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO2}	C = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

* C is the load capacitance of SO output line.

(c) SBI mode ($\overline{SCK}$...Internal clock output)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low-level width	t_{KH3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2-50			ns
	t_{KL3}			t_{KCY3}/2-150			ns
SB0, SB1 setup time (to $\overline{SCK}$↑)	t_{SIK3}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK}$↑)	t_{KSI3}			t_{KCY3}/2			ns
SB0, SB1 output delay time from $\overline{SCK}$↓	t_{KSO3}	R = 1 kΩ, C = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY3}			ns
$\overline{SCK}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY3}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY3}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY3}			ns

* R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(d) SBI mode ($\overline{SCK}$...External clock input)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low-level width	t_{KH4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KL4}			1600			ns
SB0, SB1 setup time (to $\overline{SCK}$↑)	t_{SIK4}	V_{DD} = 4.5 to 6.0 V		100			ns
				300			ns
SB0, SB1 hold time (from $\overline{SCK}$↑)	t_{KSI4}			$t_{KCY4}/2$			ns
SB0, SB1 output delay time from $\overline{SCK}$↓	t_{KSO4}	R = 1 kΩ, C = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
SB0, SB1↓ from $\overline{SCK}$↑	t_{KSB}			t_{KCY4}			ns
$\overline{SCK}$↓ from SB0, SB1↓	t_{SBK}			t_{KCY4}			ns
SB0, SB1 high-level width	t_{SBH}			t_{KCY4}			ns
SB0, SB1 low-level width	t_{SBL}			t_{KCY4}			ns

* R and C are the load resistors and load capacitance of the SB0 and SB1 output line.

(e) 2-wire serial I/O mode ($\overline{SCK}$... Internal clock output)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY5}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high-level width	t_{KH5}	R = 1 kΩ, C = 100 pF*		$t_{KCY5}/2-50$			ns
$\overline{SCK}$ low-level width	t_{KL5}			$t_{KCY5}/2-50$			ns
SB0, SB1 setup time (to $\overline{SCK}$↑)	t_{SIK5}			300			ns
SB0, SB1 hold time (from $\overline{SCK}$↑)	t_{KSI5}			600			ns
SB0, SB1 output delay time from $\overline{SCK}$↓	t_{KSO5}	R = 1 kΩ, C = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns

* R and C are the load resistors and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(f) 2-wire serial I/O mode ($\overline{SCK}$... External clock output)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY6}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high-level width	t_{KH6}			650			ns
$\overline{SCK}$ low-level width	t_{KL6}			800			ns
SB0, SB1 setup time (to $\overline{SCK}$↑)	t_{SIK6}			100			ns
SB0, SB1 hold time (from $\overline{SCK}$↑)	t_{KSI6}			$t_{KCY6}/2$			ns
SB0, SB1 output delay time from $\overline{SCK}$↓	t_{KSO6}	R = 1 kΩ, C = 100 pF*	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns

* R and C are the load resistors and load capacitance of the $\overline{SCK0}$, SB0 and SB1 output line.

(g) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK}$...Internal clock output)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY7}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low-level width	t_{KH7}	V_{DD} = 4.5 to 6.0 V		t_{KCY7}/2-50			ns
	t_{KL7}			t_{KCY7}/2-150			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK7}			100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI7}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO7}	C = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns
STB↑ from $\overline{SCK}$↑	t_{SBD}			400		t_{KCY7}	ns
Strobe signal high-level width	t_{SBW}			t_{KCY7}–30		t_{KCY7}+30	ns
Busy signal setup time (to busy signal detection timing)	t_{BYS}			100			ns
Busy signal hold time (from busy signal detection timing)	t_{BYH}			100			ns
$\overline{SCK}$↑ from busy inactive	t_{SPS}					$2t_{KCY7}$	ns

* C is the load capacitance of the SO output line.

(h) 3-wire serial I/O mode with automatic transmit/receive function ($\overline{SCK}$...External clock output)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{KCY8}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low-level width	t_{KH8}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KL8}			1600			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK8}			100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI8}			400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO8}	C = 100 pF*	V_{DD} = 4.5 to 6.0 V			300	ns
						1000	ns

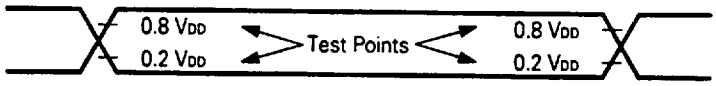
* C is the load capacitance of the SO output line.

(4) A/D converter (Ta = −40 to +85 °C, AV_{DD} = V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

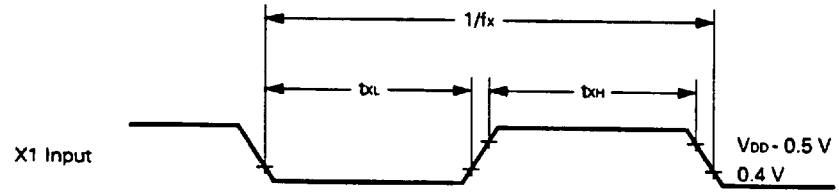
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resolution			8	8	8	bit
Overall error *					0.6	%
Conversion time	t_{CONV}		19.1		200	μs
Sampling time	t_{SAMP}		24/f_X			μs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Reference voltage	AV_{REF}		2.7		AV_{DD}	V
AV_{REF} current	I_{REF}			0.5	1.5	mA

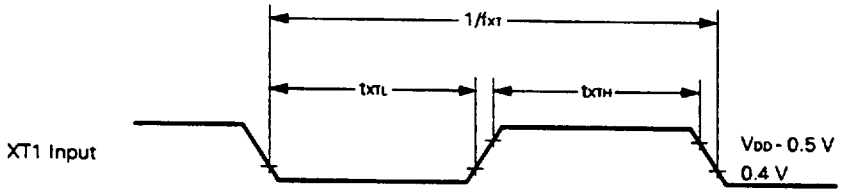
* Quantization error (±1/2 LSB) is not included. This is expressed in proportion to the full-scale value.

AC Timing Test Point (Excluding X1, XT1 Input)

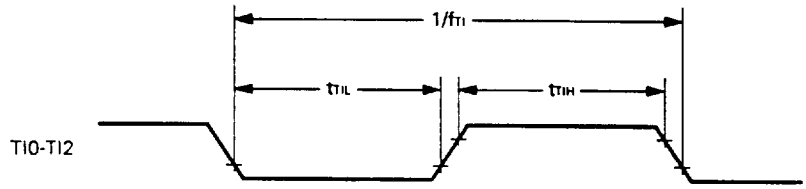


Clock Timing



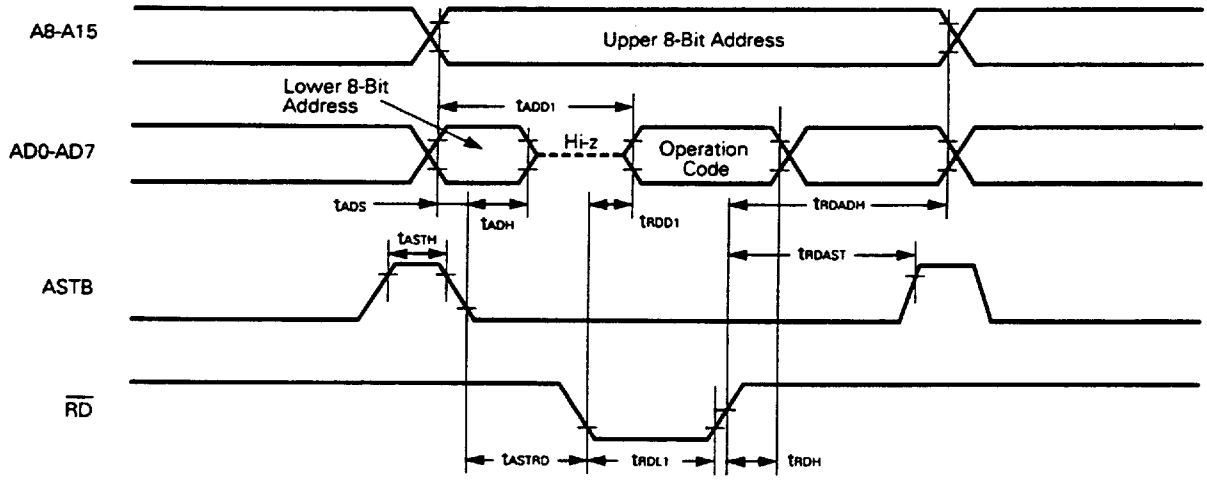


TI Timing

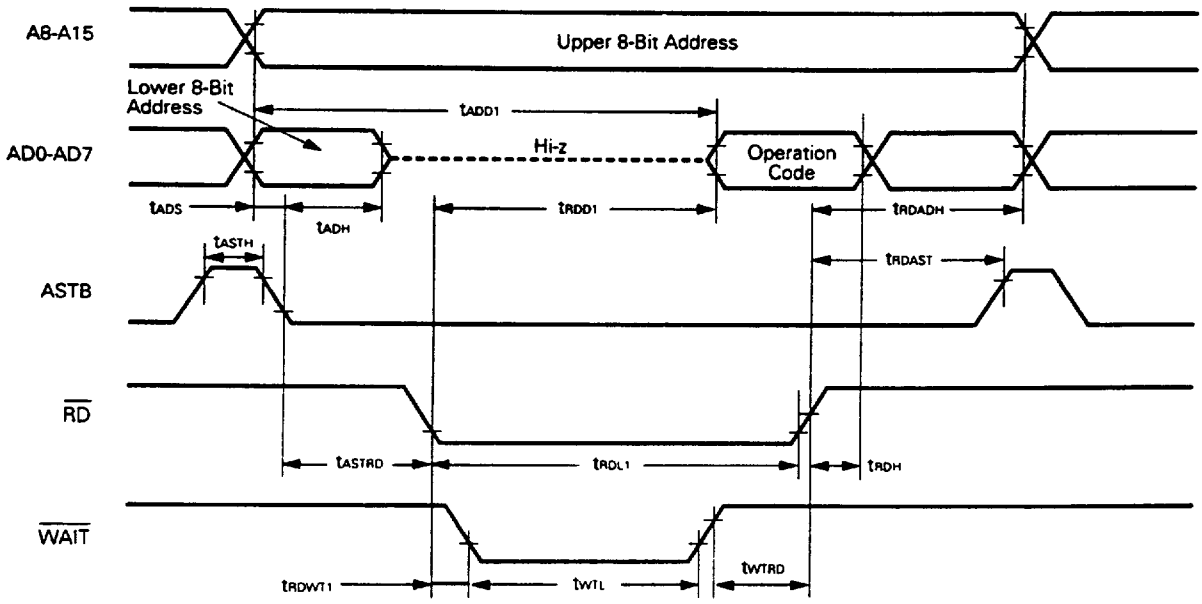


Read/Write Operation

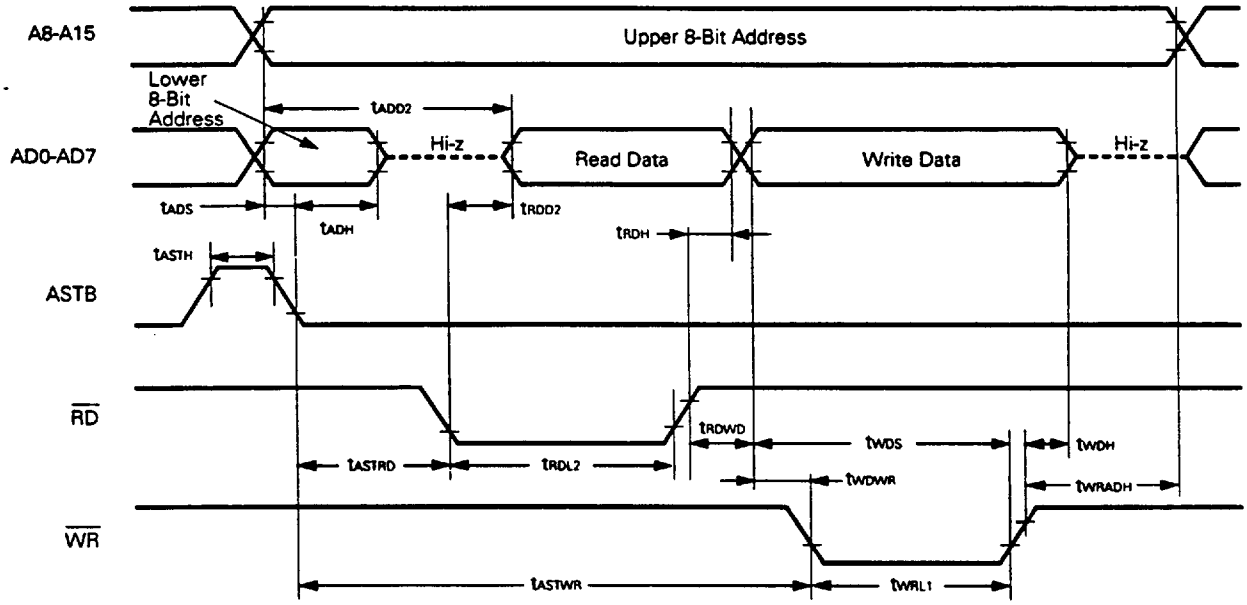
External fetch (no wait):



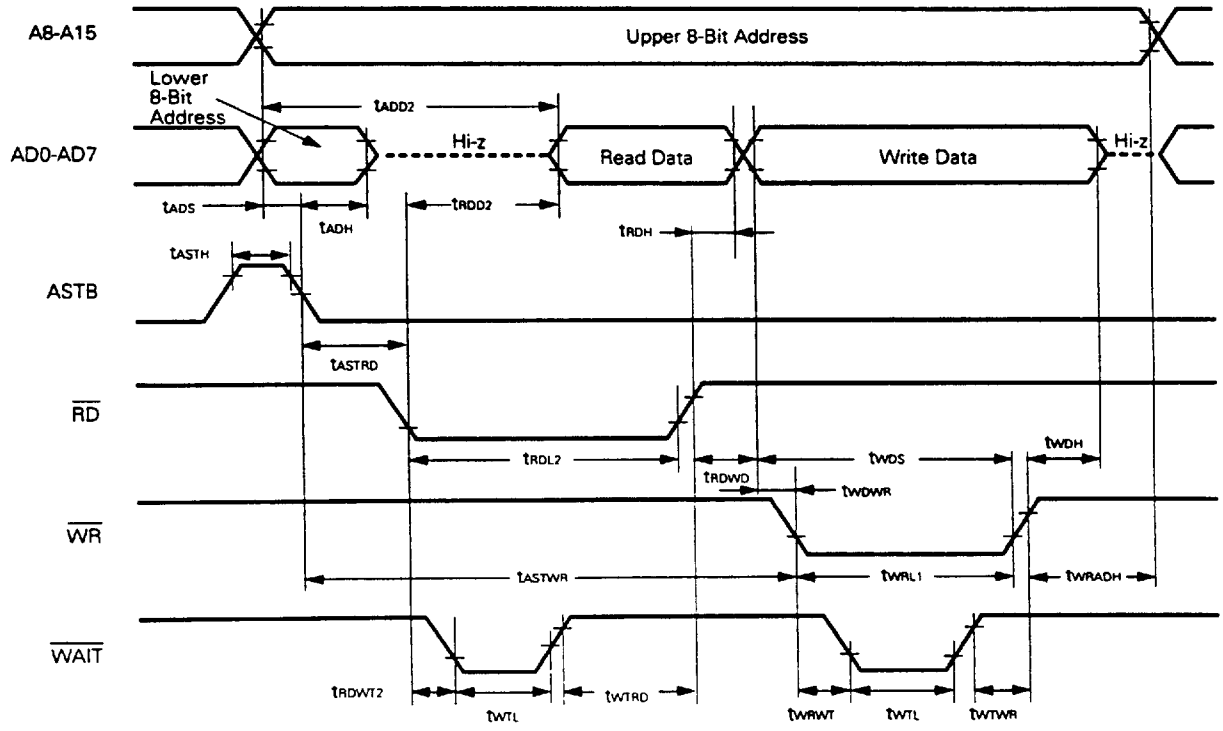
External fetch (wait insertion):



External data access (no wait):

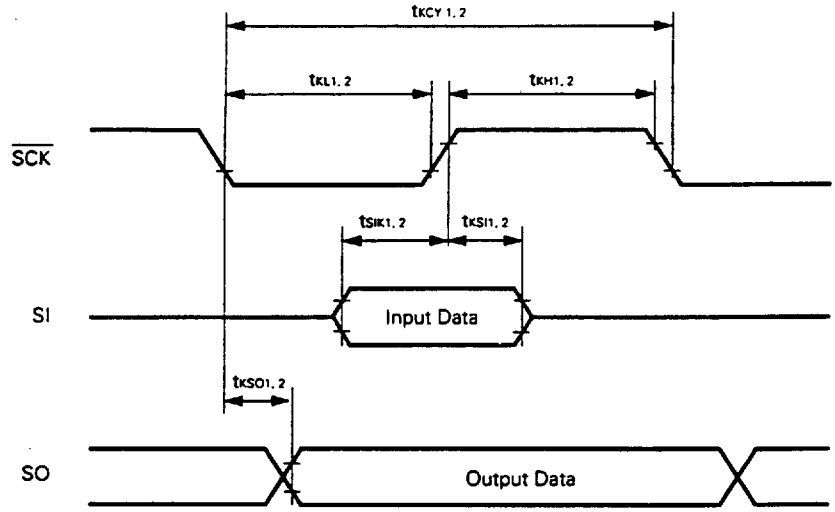


External data access (wait insertion):

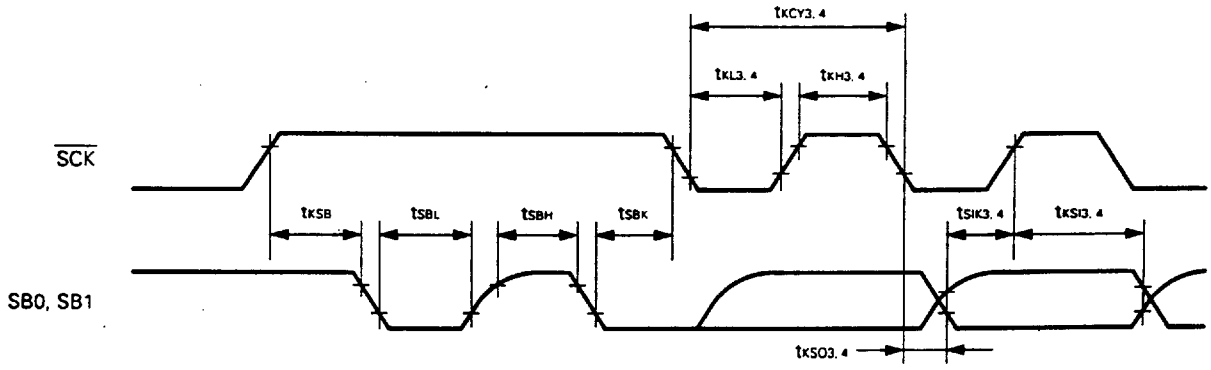


Serial Transfer Timing

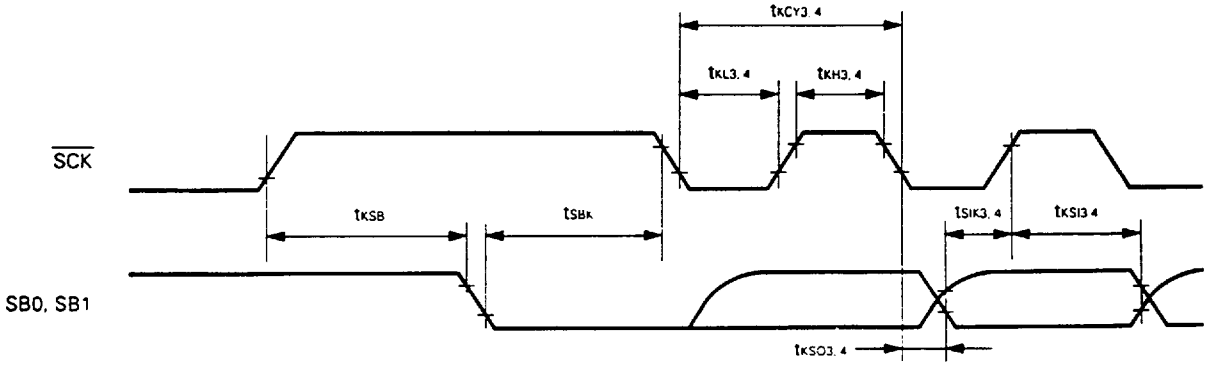
3-wire serial I/O mode:



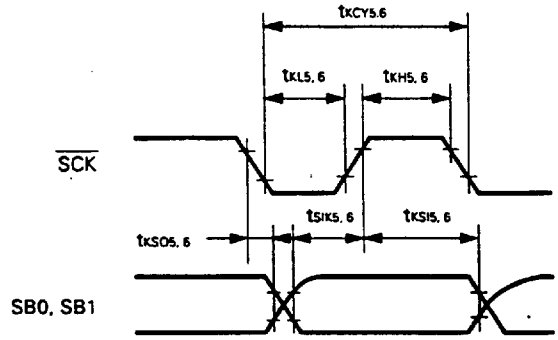
SBI mode (bus release signal transfer):



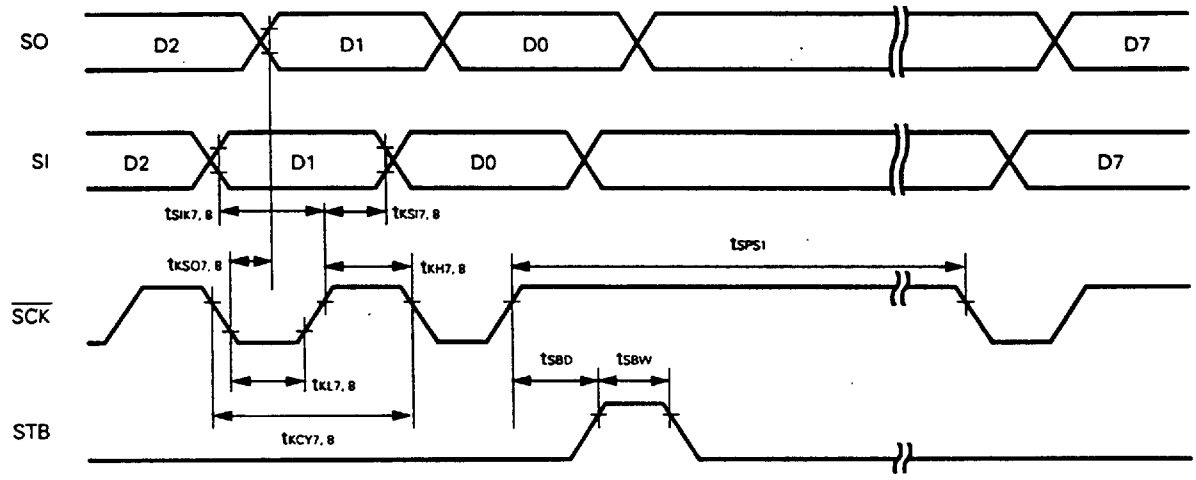
SBI mode (command signal transfer):



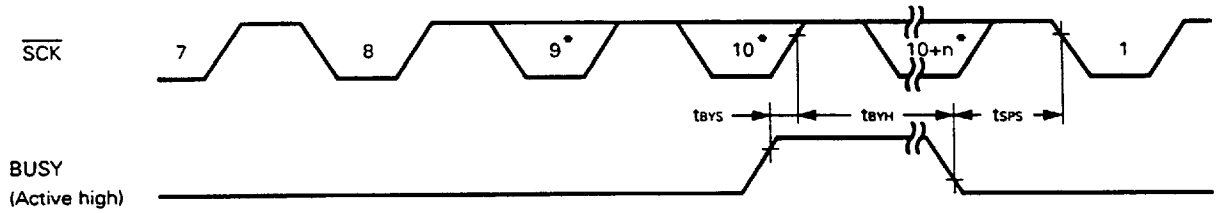
2-wire serial I/O mode:



3-wire serial I/O mode with automatic transmit/receive function:



3-wire serial I/O mode with automatic transmit/receive function (busy processing):



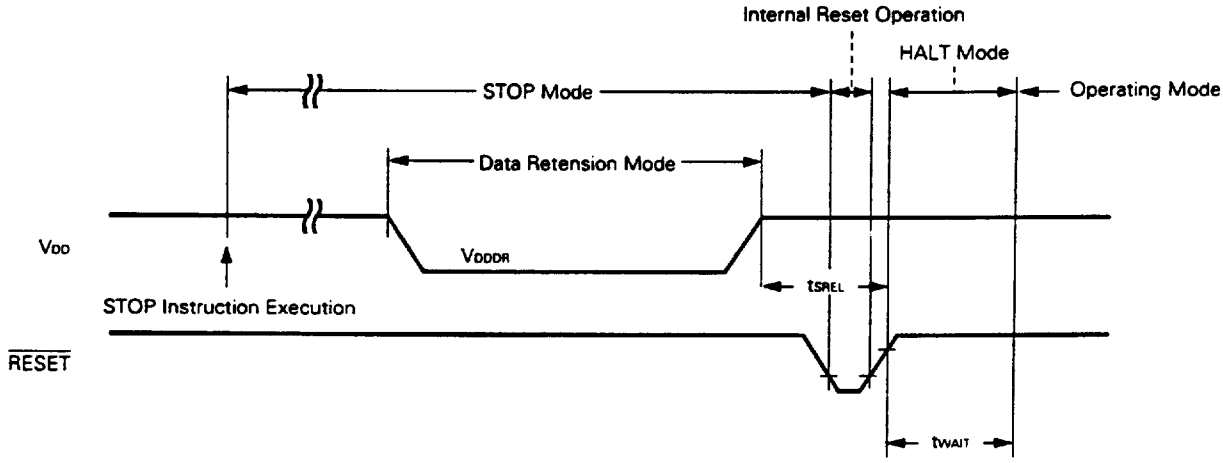
* This signal is not driven low here; it is shown as such to indicate the timing.

DATA MEMORY STOP MODE LOW SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = –40 to +85 °C)

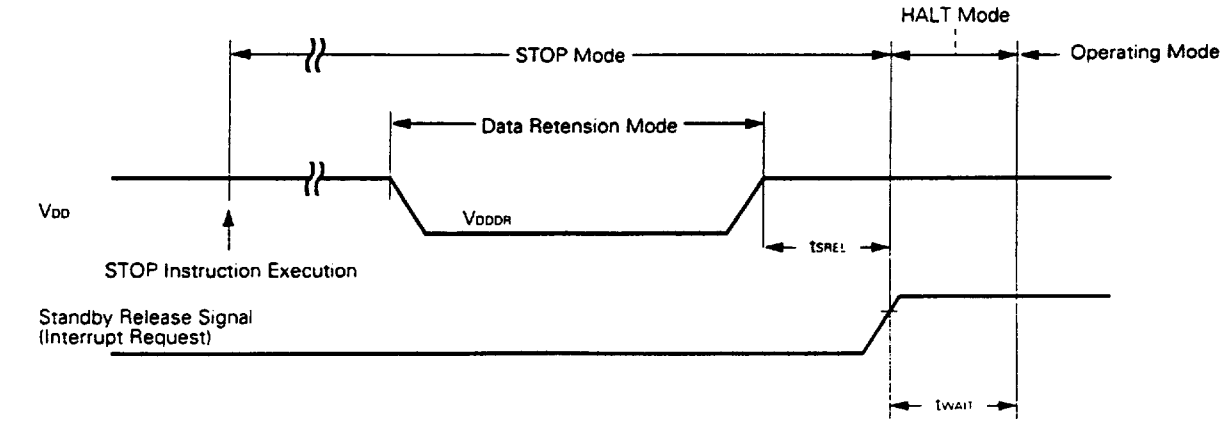
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention supply voltage	V_{DDDR}		2.0		6.0	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.0 V Subsystem clock stop and feed-back resister disconnected		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_x$		ms
		Release by interrupt		*		ms

* In combination with bits 0 to 2 (OSTS0 to OSTS2) of oscillation stabilization time select register, selection of $2^{13}/fx$ and $2^{15}/fx$ to $2^{17}/fx$ is possible.

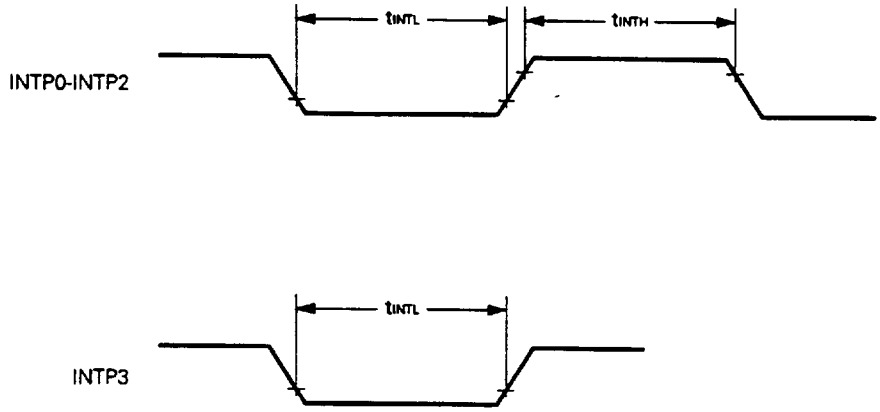
Data Retention Timing (STOP Mode Release by $\overline{RESET}$)



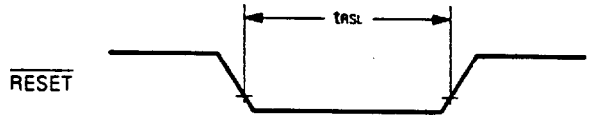
Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



Interrupt Input Timing

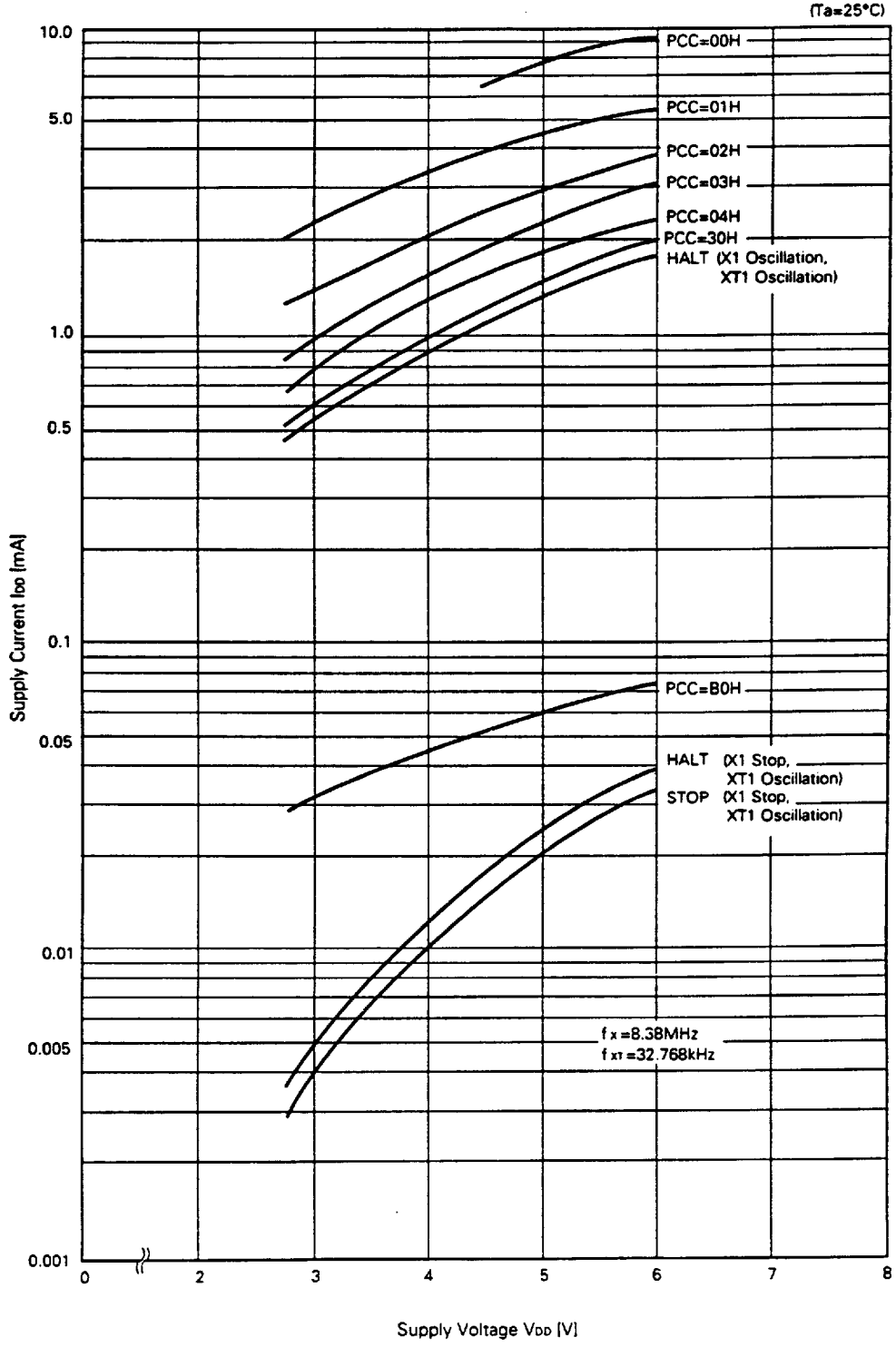


$\overline{\text{RESET}}$ Input Timing

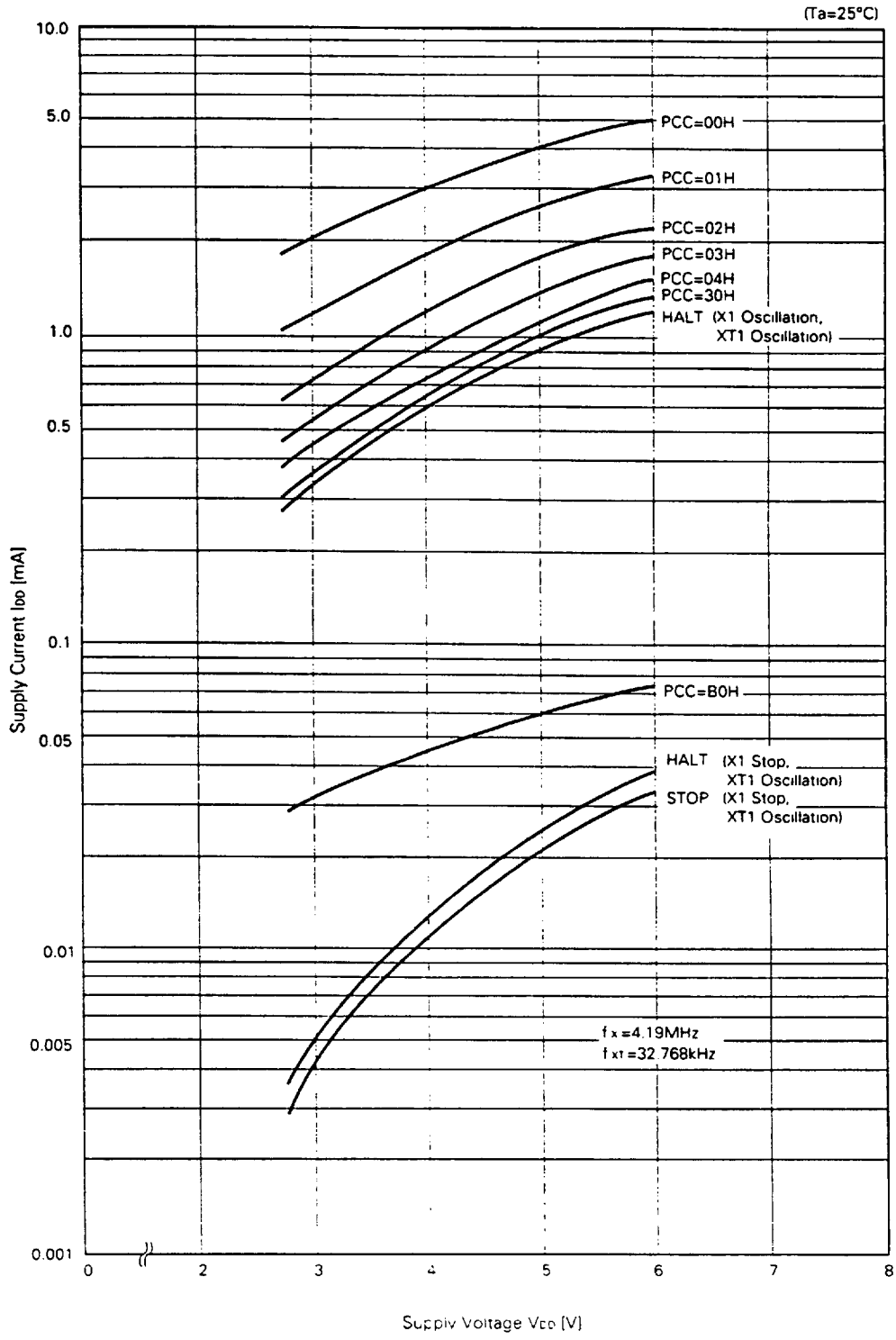


12. CHARACTERISTIC CURVE (REFERENCE VALUES)

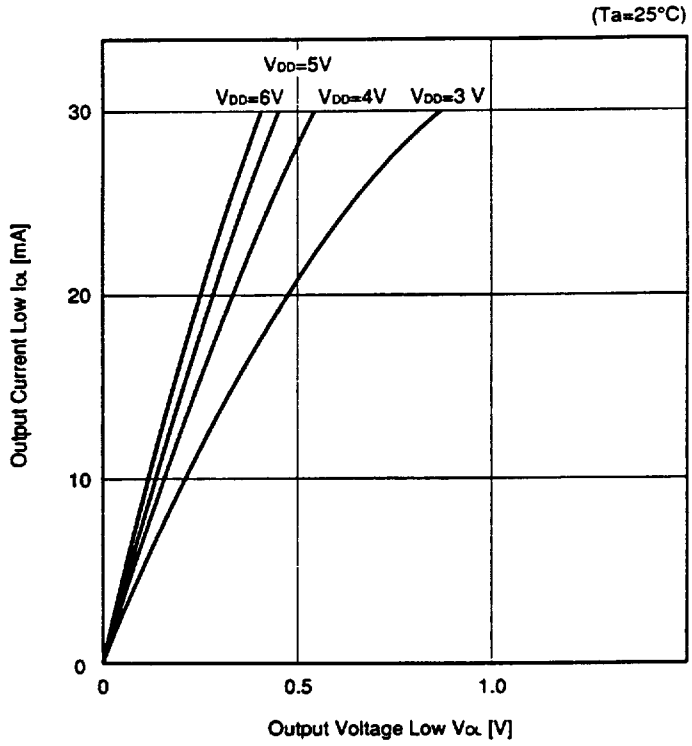
I_{DD} vs V_{DD} (Main System Clock at 8.38 MHz)



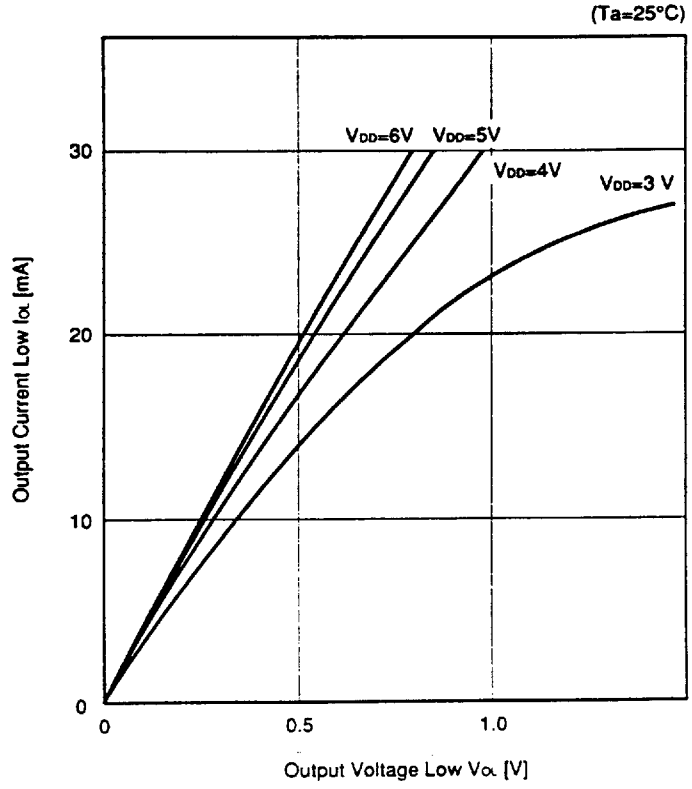
I_{DD} vs V_{DD} (Main System Clock at 4.19 MHz)



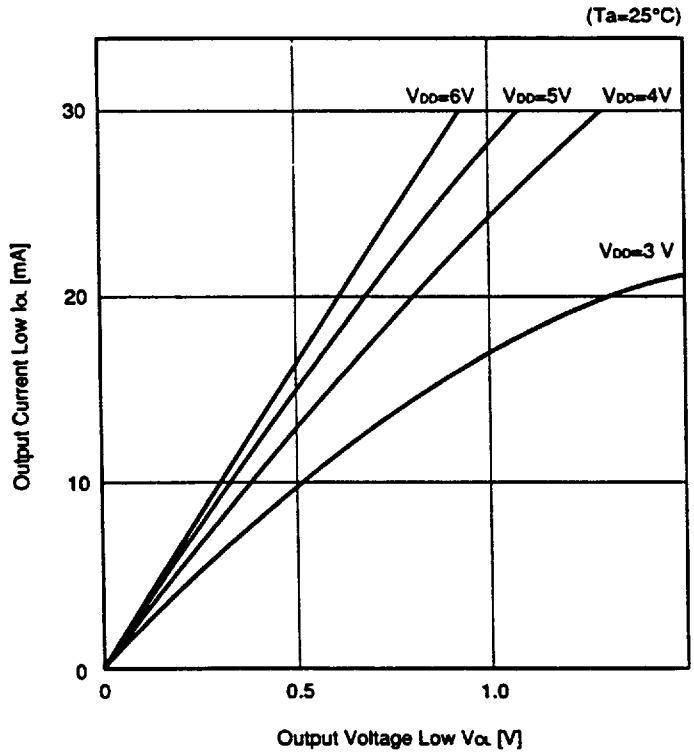
V_{OL} vs I_{OL} (Port 0, 2 to 5, P64 to P67)



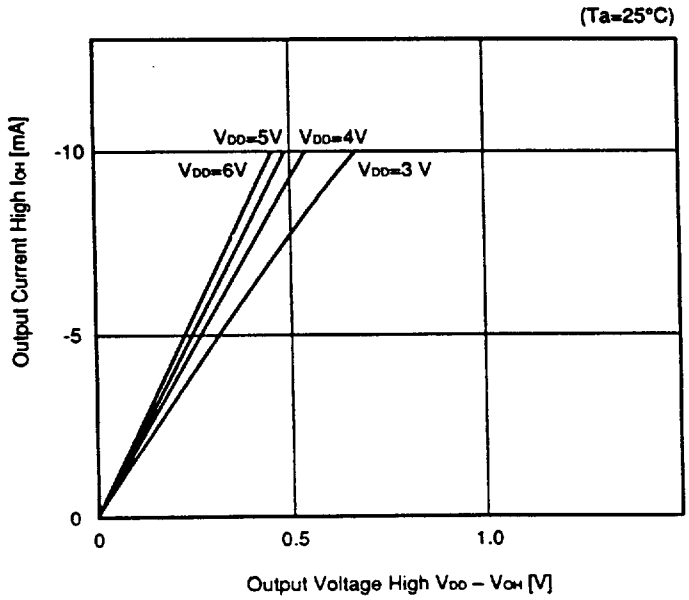
V_{OL} vs I_{OL} (Port 1)



V_{OL} vs I_{OL} (P60 to P63)

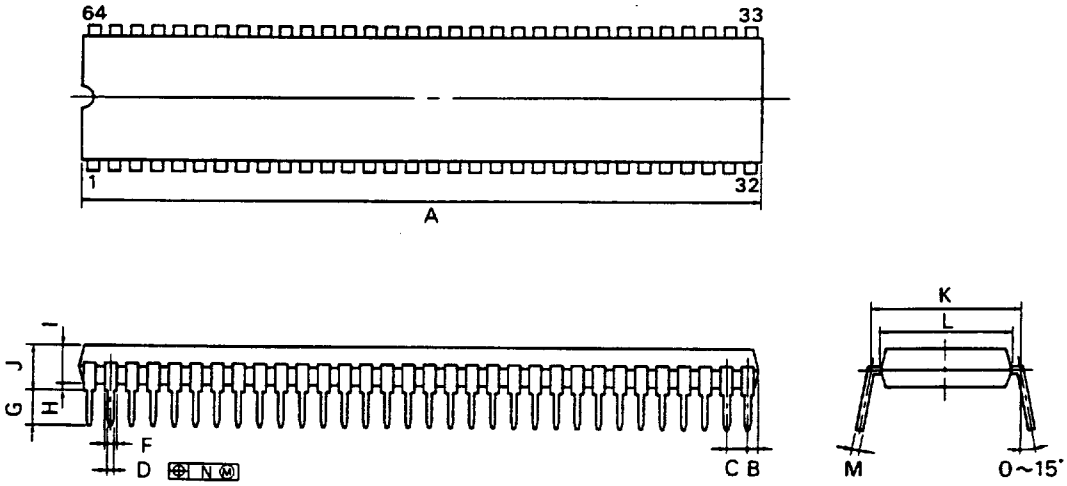


V_{OH} vs I_{OH} (Port 0 to 5, P64 to P67)



13. PACKAGE INFORMATION

64PIN PLASTIC SHRINK DIP (750 mil)



P64C-70-750A,C

NOTES

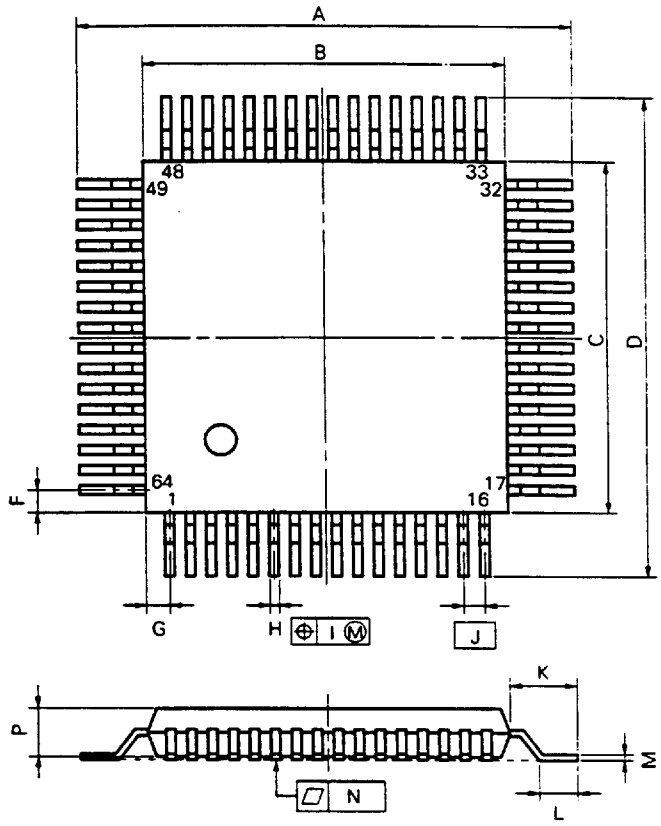
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

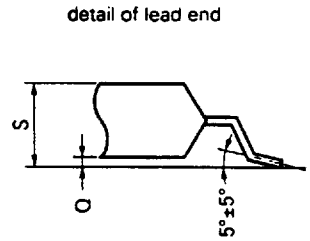
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

Note ES product is 64-pin ceramic shrink DIP (seam weld) (750 mil).

64 PIN PLASTIC QFP (□14)





P64GC-80-AB8-3

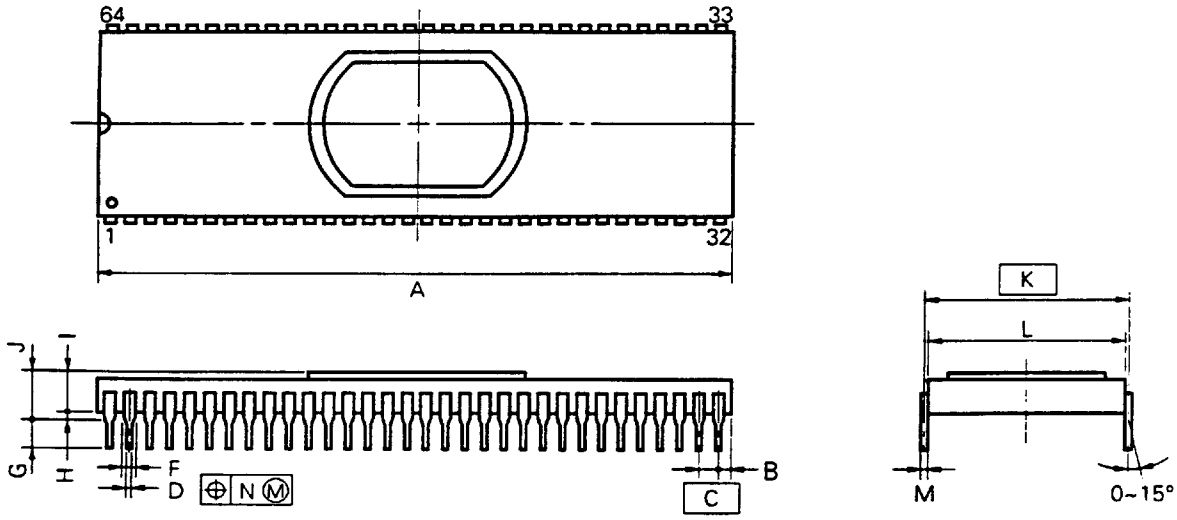
NOTE
Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

Note **ES product is 64-pin ceramic QFP(□14mm).**

ES PACKAGE INFORMATION

64PIN CERAMIC SHRINK DIP (SEAM WELD) (750 mil)



P64D-70-750A1

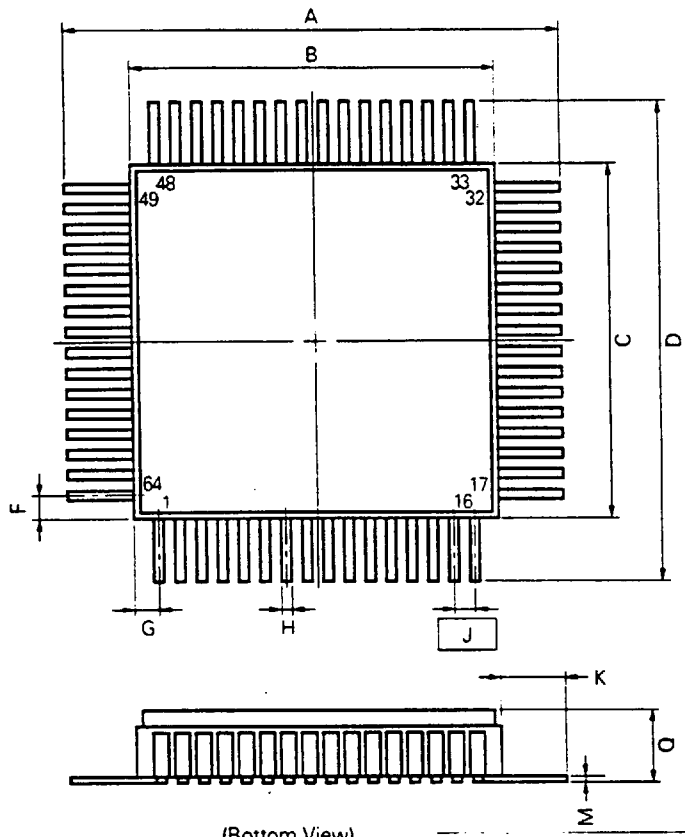
NOTES

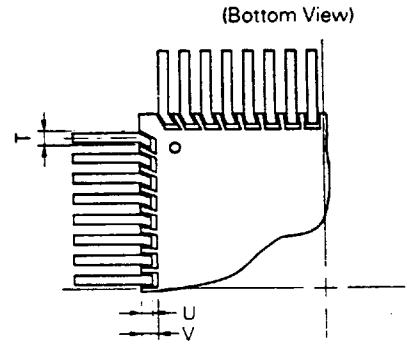
1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.16 MAX.	2.290 MAX.
B	1.521 MAX.	0.060 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.46±0.05	0.018±0.002
F	0.8 MIN.	0.031 MIN.
G	3.5±0.3	0.138±0.012
H	1.02 MIN.	0.040 MIN.
I	3.14	0.124
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	18.8	0.740
M	0.25±0.05	$0.010^{+0.002}_{-0.003}$
N	0.25	0.01

64 PIN CERAMIC QFP (14 × 14) (FOR ES)





X64B-80A-1

ITEM	MILLIMETERS	INCHES
A	22.0±0.4	0.866±0.016
B	14.0	0.551
C	14.0	0.551
D	22.0±0.4	0.866±0.016
F	1.0	0.039
G	1.0	0.039
H	0.32	0.013
J	0.8 (T.P.)	0.031 (T.P.)
K	4.0±0.15	$0.157^{+0.007}_{-0.006}$
M	0.25	0.01
Q	3.0 MAX.	0.119 MAX.
T	0.55	0.022
U	1.0	0.039
V	1.2	0.047

14. RECOMMENDED SOLDERING CONDITIONS

The μPD78011B(A)/78012B(A)/78013(A)/78014(A) should be soldered and mounted under the conditions recommended in the table below.

For detail of recommended soldering conditions, refer to the information document **"Semiconductor Device Mount Manual" (IE-1207)**.

For soldering methods and conditions other than those recommended below, contact our sales personnel.

Table 14-1 Surface Mounting Type Soldering Conditions(1/2)

(1) μPD78011BGC(A)-xxx-AB8 : 64-pin plastic QFP (□14 mm)
μPD78012BGC(A)-xxx-AB8 : 64-pin plastic QFP (□14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C Duration: 30 sec. max. (at 210°C or above) Number of times: Twice max. < precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	IR35-00-2
VPS	Package peak temperature: 215°C Duration: 20 to 40 sec. (at 200°C or above) Number of times: Twice max. <precautions> (1) The second reflow should be started after the first reflow device temperature has returned to the ordinary state. (2) Flux washing must not be performed by the use of water after the first reflow.	VP15-00-2
Pin Part Heating	Pin part temperature: 300°C max. Duration: 3 sec. max. (per device side)	—

Note Use more than one soldering method should be avoided (except in the case of pin part heating).

Table 14-1 Surface Mounting Type Soldering Conditions(2/2)

(2) μPD78013GC(A)-xxx-AB8 : 64-pin plastic QFP (□14 mm)
μPD78014GC(A)-xxx-AB8 : 64-pin plastic QFP (□14 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C Duration: 30 sec. max. (at 210°C or above) Number of times: Once Time limit: 7 days* (thereafter 10 hours prebaking required at 125°C)	IR30-107-1
VPS	Package peak temperature: 215°C Duration: 40 sec. max. (at 200°C or above) Number of times: Once Time limit: 7 days* (thereafter 10 hours prebaking required at 125°C)	VP15-107-1
Wave soldering	Solder bath temperature: 260°C max.Duration: 10 sec. max.Number of times: Once, Preliminary heat temperature: 120°C max. (Package surface temperature), Time limit: 7 days* (thereafter 10 hours prebaking required at 125°C)	WS60-107-1
Pin part heating	Pin part temperature: 300°C max. Duration: 13 sec. max. (per device side)	—

* For the storage period after dry-pack decompression, storage conditions are max. 25°C, 65% RH.

Note Use more than one soldering method should be avoided (except in the case of pin part heating).

Notice

μPD78013(A)/78014(A) with improved recommended soldering conditions is available. For details (imrovement such as infrared reflow peak temperature extension: 235°C, number of times: twice, relaxation of time limit, etc.), contact NEC sales personnel.

Table 14-2 Insertion Type Soldering Conditions

μPD78011BCW(A)-xxx : 64-pin plastic shrink DIP (750mil)
μPD78012BCW(A)-xxx : 64-pin plastic shrink DIP (750mil)
μPD78013CW(A)-xxx : 64-pin plastic shrink DIP (750mil)
μPD78014CW(A)-xxx : 64-pin plastic shrink DIP (750mil)

Soldering Method	Soldering Conditions
Wave soldering (lead part only)	Solder bath temperature: 260°C max., Duration: 10 sec. max.
Pin part heating	Pin part temperature: 260°C max., Duration: 10 sec. max.

Note Wave soldering is only for the lead part in order that jet solder can not contact with the chip directly.

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78011B(A)/78012B(A)/78013(A)/78014(A).

Language Processors Software

RA78K/0 *1,2	78K/0 series common assembler package
CC78K/0 *1,2	78K/0 series common C compiler package
CC78K/0-L *1,2	78K/0 series common C compiler library source file

PROM Write Tools

PG-1500	PROM programmer
PA-78P014CW PA-78P014GC	Programmer adapter connected to PG-1500
PG-1500 controller *1	PG-1500 control program

Debugging Tools

IE-78000-R	78K/0 series common in-circuit emulator
IE-78000-R-BK	78K/0 series common break board
IE-78014-R-EM	μPD78014 series evaluation emulation board
EP-78240CW-R EP-78240GC-R	Emulation probe common with μPD78244 series
EV-9200GC-64	Socket mounted onto user system board for 64-pin plastic QFP
SD78K/0 *1	IE-78000-R screen debugger
DF78014 *1	μPD78014 series device file

Real-Time OS

RX78K/0 *1,2	78K/0 series real-time OS

Fuzzy Inference Development Support System

FE9000 *1	Fuzzy knowledge data creation tool
FT9080 *1	Translator
FI78K0 *1	Fuzzy inference module
FD78K0 *1,3	Fuzzy inference debugger

* 1. PC-9800 series (MS-DOS™) based and IBM PC/AT™ (PC DOS™) based.
2. HP9000 series 300™ (HP-UX™) based, SPARCstation™ (Sun OS™) based and EWS-4800 series™ (EWS-UX/V™) based.
3. Under development.

3rd Party Development Tools

Inquiry to :	Emulator	Assembler	C Compiler	Simulator	Debugger	others
Advanced Data Controls Co., Ltd. (Tel: 03-3576-5351)	—	*	O C cross 78K0 compiler	O (CXDB/S)	O (CXDB/E)	—
Gaio Technology Co., Ltd. (Tel: 03-3662-3041)	—	O (XASS-V)	—	O (XDB-V)	O (XDDI-V)	—
Data I/O Japan Co., Ltd. (Tel: 03-3436-4041)	—	—	—	—	—	O PROM programmer
Life boat Co., Ltd. (Tel: 03-3293-4714)	—	*	O (ICC 78000)	—	—	—
Yokokawa Digital Computer Co., Ltd. (Tel: 0422-56-9101)	O (AD 200)	—	—	—	O (μVIEW)	—

* **Assembler is included in C compiler package.**

APPENDIX B. RELATED DOCUMENTATION

Device Related Documentation (μPD78014 Series)

Document Name		Document No. (Japanese)
μPD78014/78014Y Series User's Manual		IEU-780
78k/0 Series Instruction Application Table		IEM-5522
78k/0 Series Instruction Set		IEM-5521
μPD78014/78014Y Series Special Function Register Application Table		IEM-5527
78k/0 Series Application Note	Introductory Volume I	IEA-715
	Introductory Volume II	IEA-740
	Floating Point Operation Program Volume	IEA-718

Development Tool Documentation (User's Manuals)

Document Name		Document No. (Japanese)
RA78K Series Assembler Package	Operation Volume	EEU-809
	Language Volume	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-817
CC78K Series C Compiler	Operation Volume	EEU-656
	Language Volume	EEU-655
CC78K Series Library Source File		EEU-777
PG-1500 PROM Programmer		EEU-651
PG-1500 Controller		EEU-704
IE-78000-R		EEU-810
IE-78000-R-BK		EEU-867
IE-78014-R-EM		EEU-805
SD78K/0 Screen Debugger	Primer	EEU-852
	Reference Volume	EEU-816

Note **The contents of the above documents are subject to change without notice. The latest documents should be used for design, etc.**

Built-In Software Documents (User's Manuals)

Document Name		Document No. (Japanese)
78K/0 Series Real-Time OS	Introductory Volume	EEU-912
	Installation Volume	EEU-911
	Debugger Volume	EEU-930
	Technical Volume	EEU-913
Fuzzy Knowledge Data Creation Tools		EEU-829
78/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-862
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921

Other Documents

Document Name	Document No. (Japanese)
Package Manual	IEI-635
Surface Mount Technology Manual	IEI-616
Quality Grades on Semiconductor Devices	IEI-620
NEC Semiconductor Device Reliability & Quality Control	IEM-5068
Electrostatic Discharge (ESD) Test	MEM-539
Semiconductor Devices Quality Control Guarantee Guide	MEI-603
Microcomputer Related Products Guide Other Manufacturers Volume	MEI-604

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