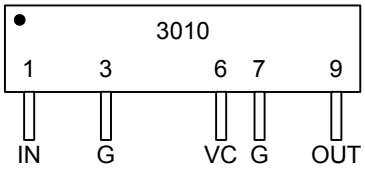
VOLTAGE-VARIABLE DELAY LINE
T_R < 1ns
(SERIES 3010)

FEATURES

- Varactor Technology
- Fast rise time for high frequency applications
- Delay continuously adjustable from 2.4ns to 3.4ns
- Very narrow device (SIP package)
- Stackable for PC board economy
- Epoxy encapsulated
- Meets or exceeds MIL-D-23859C

PACKAGE



3010-P: Positive control voltage
3010-N: Negative control voltage

FUNCTIONAL DESCRIPTION

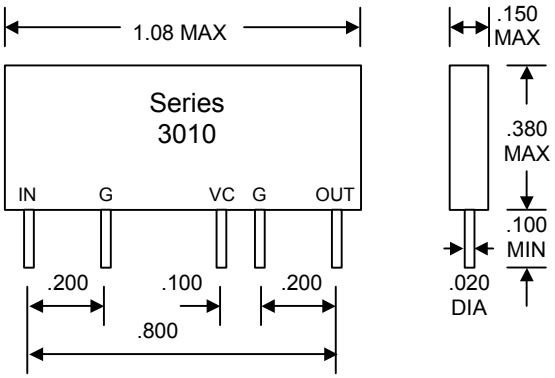
The 3010-series devices are continuously variable, single-input, single-output, passive delay lines. The signal input (IN) is reproduced at the output (OUT), shifted by a time (T_D) which is adjusted via an applied control voltage (VC). This control voltage is positive for the 3010-P and negative for the 3010-N. The characteristic impedance of the line is nominally 50 ohms. The rise time (T_R) of the lines is no more than 1ns, resulting in a 3dB bandwidth of at least 300MHz. The delay resolution is limited only by that of the control voltage.

PIN DESCRIPTIONS

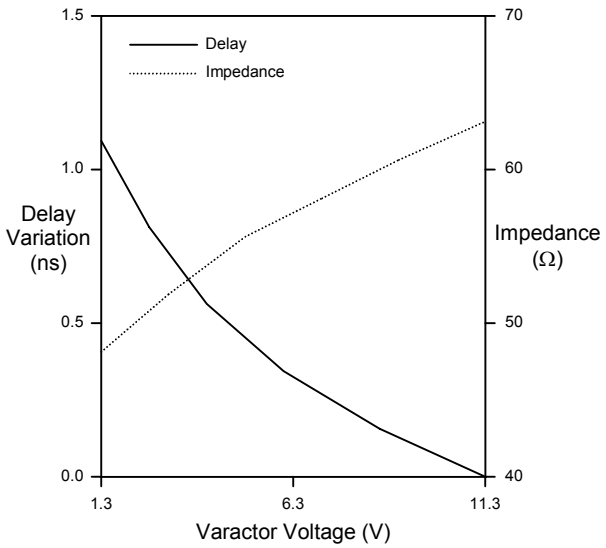
IN	Signal Input
OUT	Signal Output
VC	Control Voltage
G	Ground

SERIES SPECIFICATIONS

- **Varactor voltage range (3010-P):** 1.3V (max T_D) to 11.3V (min T_D)
- **Varactor voltage range (3010-N):** -1.3V (max T_D) to -11.3V (min T_D)
- **Range of delay variation:** 1.0ns ± 0.1ns
- **Minimum delay:** 2.4ns ± 0.25ns
- **Impedance:** 45Ω - 68Ω
- **Output rise time:** 1.0ns max
- **Bandwidth:** 300MHz min
- **Overshoot/preshoot:** ± 20% max
- **Operating temperature:** -10°C to +80°C
- **Temperature coefficient:** 1000 PPM/°C max

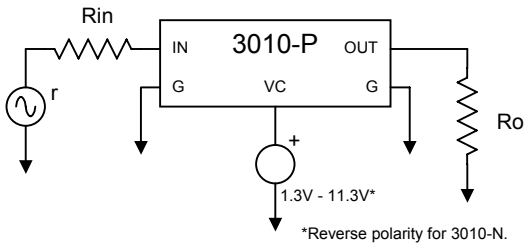


Package Dimensions



Typical Delay/Impedance Variation

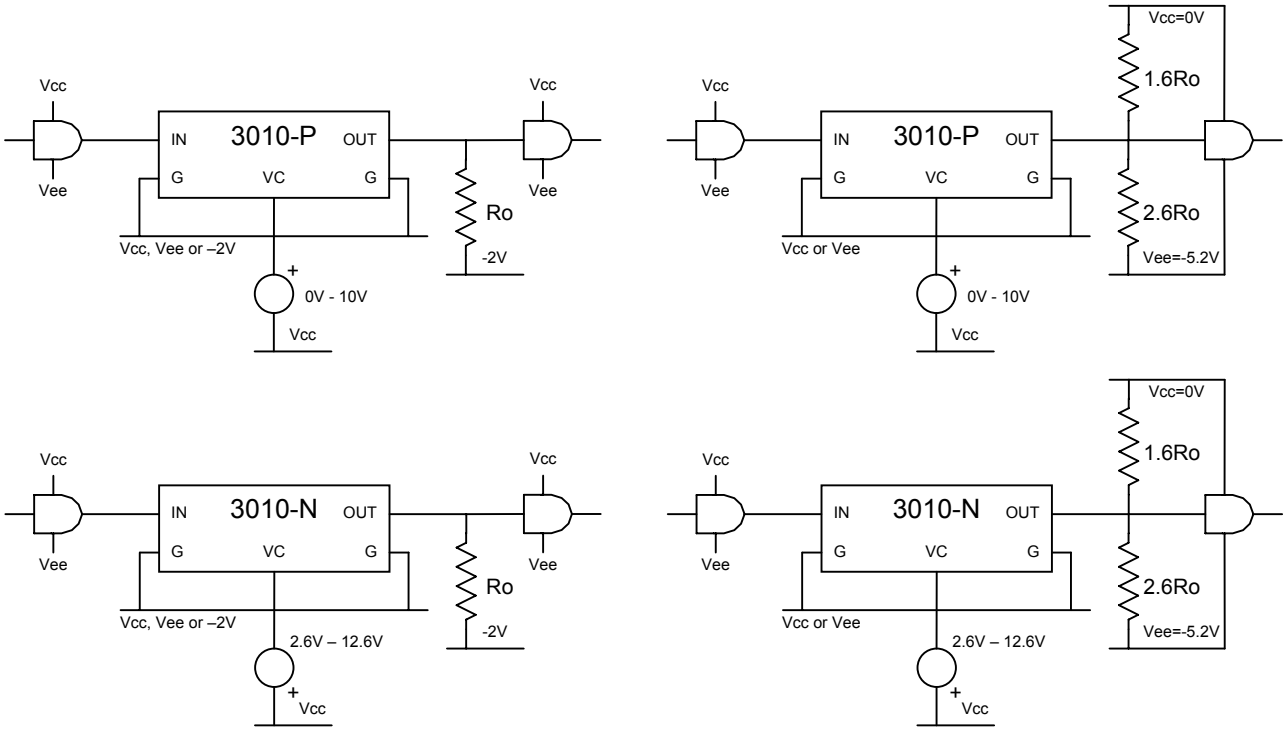
TYPICAL APPLICATIONS



r: Signal source impedance
Rin: Input termination resistor
Ro: Output termination resistor

- Set Ro to the median impedance value within the delay adjustment range (50Ω - 60Ω)
- Set Rin = Rout - r

Analog Interface



ECL with –2V Termination **ECL without –2V Termination**

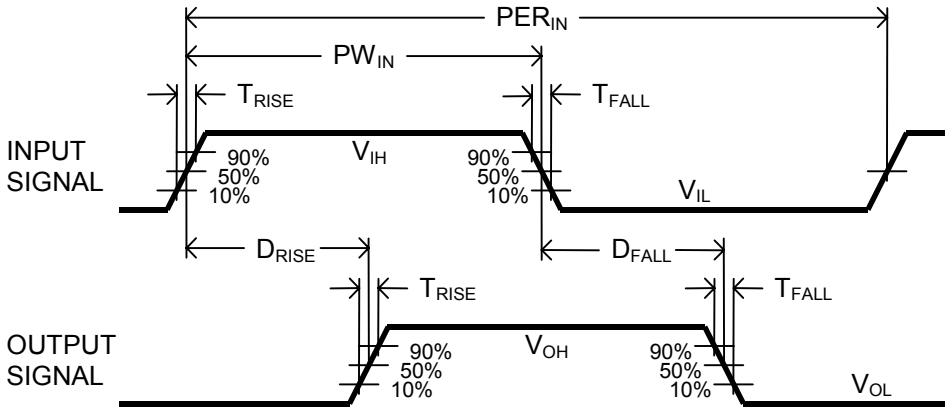
Note: The varicap voltage is referenced to the DC level of the input signal. In the case of ECL applications, a voltage of 0V to 10V (2.6V to 12.6V for the 3010-N) should be applied at pin 6, because the signal line has –1.3V DC level. This assumes the ECL signal has approximately 50% duty cycle.

PASSIVE DELAY LINE TEST SPECIFICATIONS

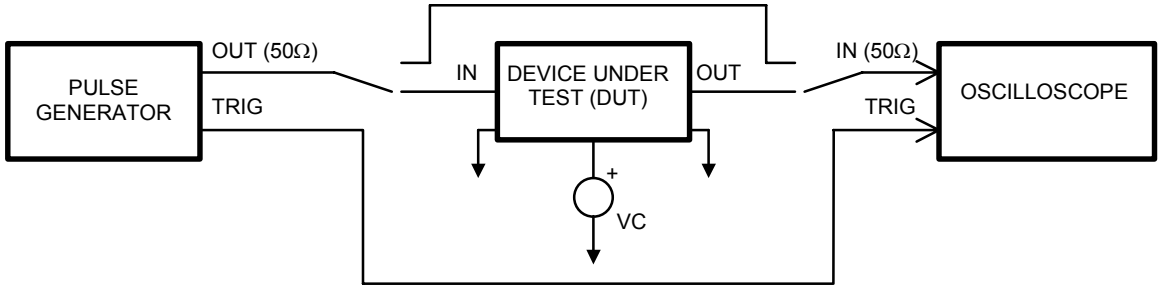
TEST CONDITIONS

INPUT:		**OUTPUT:**	
Ambient Temperature:	25°C ± 3°C	**R_{load}:**	50Ω
Input Pulse:	High = 1.8V typical Low = 0.8V typical	**C_{load}:**	<10pf
		Threshold:	50% (Rising & Falling)
Source Impedance:	50Ω Max.		
Rise/Fall Time:	3.0 ns Max. (measured at 10% and 90% levels)		
Pulse Width:	PW_{IN} = 500ns		
Period:	PER_{IN} = 1000ns		

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Timing Diagram For Testing



Test Setup