PC Clock Generator

Features

- Generates up to 16 preset frequencies and buffers the reference frequency
- External loop filter provides exceptionally smooth frequency transitions
- Synthesizes frequencies from 1 MHz to 130 MHz
- "Green PC" features including:
  - Power down option
  - Slow down CPU clock from any frequency to 8 MHz or 16 MHz
  - Stop clock for the "S" class x86 CPUs
  - Output tristate or disable option
- Meets frequency requirements for Pentium™ and x86 CPUs
- Requires only three external components: one 14.318 MHz crystal, one 0.1 µF capacitor, and one 1 nF capacitor
- CMOS technology in 14-pin PDIP (300 mil) and SOIC (150 mil)
- 5V or 3.3V supply

Description

The Chrontel CH9008 is a PLL clock generator designed for personal computer applications, such as motherboards, graphics, disk drives, modems, and portable/handheld systems.

CH9008 generates the CPU and optional 2XCPU clocks, and buffers the reference frequency. Output is selected by setting frequency select inputs to VDD or GND.

When the power down option is active (logic low), CLK1 and XOUT are tristated and pulled low, while the internal PLL is disabled to minimize power consumption (less than 10 µA). The PLL typically requires 10 milliseconds to reach a preset frequency from power down depending on the capacitor value selected.

Setting the SD* pin to ground enables slow down, which gradually slows CLK1 (CPU clock output) to either 8 MHz or 16 MHz.

CPU clock enable option is for x86 CPUs with stop clock feature. When CLKEN is driven to a low, the CLK1 output is disabled and held at a low state.

The OE1 pin tristates CLK1, placing CLK1 in a high impedance state.

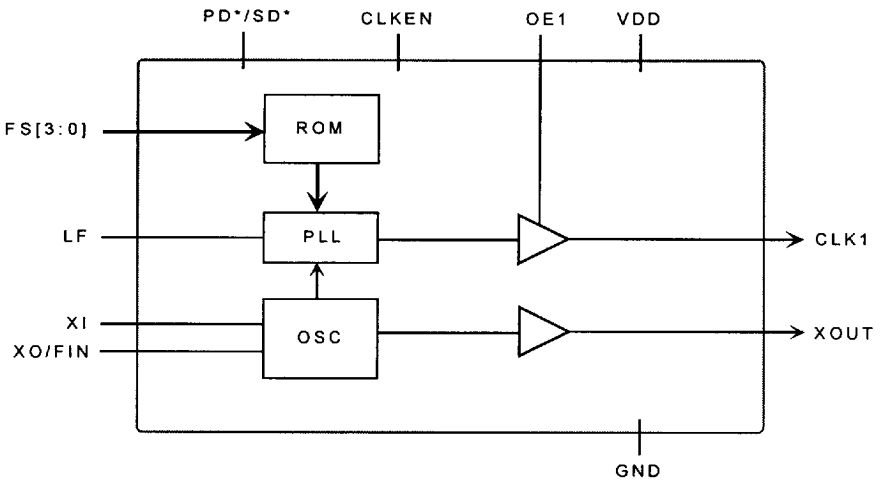

Figure 1: Block Diagram

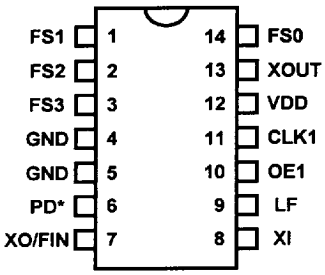

Figure 2: CH9008D

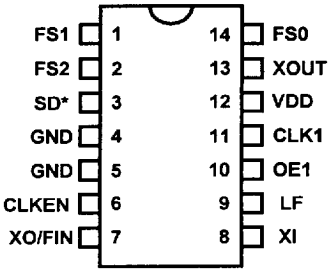

Figure 3: CH9008E

Table 1 • Pin Description CH9008D

Pin	Type	Symbol	Description
1, 2, 3, 14	In	FS1, FS2, FS3, FS0	Frequency select for CLK1 (internal pull-up)
4, 5	Power	GND	Ground
6	In	PD*	Power down input (active low, internal pull-up)
7	Out / In	XO / FIN	Crystal output or external FREF input
8	In	XI	Crystal input
9	In	LF	External loop filter
10	In	OE1	CLK1 output enable (active high, internal pull-up)
11	Out	CLK1	Clock1 output
12	Power	VDD	5V or 3.3V supply
13	Out	XOUT	Buffered reference (14.318 MHz) clock output

Table 2 • Pin Description CH9008E

Pin	Type	Symbol	Description
1, 2, 14	In	FS1, FS2, FS0	Frequency select for CLK1 (internal pull-up)
3	In	SD*	Slow down input (active low, internal pull-up)
4, 5	Power	GND	Ground
6	In	CLKEN	Clock enable input (active high, internal pull-up)
7	Out / In	XO / FIN	Crystal output or external FREF input
8	In	XI	Crystal input
9	In	LF	External loop filter
10	In	OE1	CLK1 output enable (active high, internal pull-up)
11	Out	CLK1	Clock1 output
12	Power	VDD	5V or 3.3V supply
13	Out	XOUT	Buffered reference (14.318 MHz) clock output

Table 3 • Frequencies for CH9008D and E (in MHz)

Frequency Select				Version D	Version E	
3	2	1	0	CLK1	CLK1	Slow Freq
0	0	0	0	16.0	25.0	8.0
0	0	0	1	40.0	33.33	8.0
0	0	1	0	50.0	40.0	8.0
0	0	1	1	80.0	50.0	16.0
0	1	0	0	66.6	66.6	16.0
0	1	0	1	100.0	60.0	16.0
0	1	1	0	8.0	80.0	16.0
0	1	1	1	4.0	50.0	8.0
1	0	0	0	8.0		
1	0	0	1	20.0		
1	0	1	0	25.0		
1	0	1	1	40.0		
1	1	0	0	33.3		
1	1	0	1	50.0		
1	1	1	0	4.0		
1	1	1	1	2.0		
Number of pins				14	14	
Power down option				Yes	No	
Clock enable				No	Yes	
Glitch-free transitions				Yes	Yes	
Slow down option				No	Yes	
Slow down frequency				N/A	See above	
Internal pull-up				Yes	Yes	

Note: Please consult Chrontel for custom frequency patterns

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Table 4 • Absolute Maximum Ratings

Symbol	Description	Value	Unit
VDD	Power supply voltage with respect to GND	–0.5 TO +7.0	V
VIN	Input voltage on any pin with respect to GND	–0.5 TO VDD+0.5	V
TSTOR	Storage temperature	–55 TO +150	°C

Note: Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating conditions is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 5 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 4.75V, IOH = 1mA	2.5			V
VOL	Output low voltage	VDD = 4.75V, IOL = 2mA			0.5	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current			3	10	µA
ILK	Input leakage current		–10		10	µA
CI	Input capacitance	Except XO / FIN, XI			10	pF
CI	Input capacitance	Pins XO / FIN, XI		20		pF
IPD	Power down supply current	PD* = Low		3		µA
ISD	Slow down supply current	SD* = Low, VDD = 5V, No load		3		mA
IDD	Operating current	VDD = 5V CLK1 = 40 MHz, No load CLK1 = 80 MHz, No load		10 20		mA

Table 6 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 5V ±5%)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency		1	14.318	20	MHz
TIR	Input clock rise time				20	ns
TIF	Input clock fall time				20	ns
TR	Output clock rise time	15 pF load, VOUT = 0.8V to 2.0V			3	ns
TF	Output clock fall time	15 pF load, VOUT = 0.8V to 2.0V			3	ns
TDC	Duty cycle	15 pF load	45	48/52	55	%
TJCC	Jitter, cycle to cycle	CLK1 = 50 MHz		50	100	ps
TJLT	Jitter, long term (10,000 cycles)	CLK1 = 50 MHz		200	1000	ps
TFT	Frequency transition time	8 – 80 MHz without 1 nF LF cap		2		ms
		8 – 80 MHz with 1 nF LF cap		10		ms
TPU	Power up time	From OFF to 100 MHz without 1 nF LF cap		3		ms
		From OFF to 100 MHz with 1 nF LF cap		15		ms

Table 7 • DC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
VOH	Output high voltage	VDD = 3.0V, IOH = 1mA	VDD – 0.5			V
VOL	Output low voltage	VDD = 3.0V, IOL = 2mA			0.5	V
VIH	Input high voltage		2.0			V
VIL	Input low voltage				0.8	V
IPU	Input pull-up current			3	10	µA
ILK	Input leakage current		–10		10	µA
CI	Input capacitance	Except XO / FIN, XI			10	pF
CI	Input capacitance	Pins XO / FIN, XI		20		pF
IPD	Power down supply current	PD* = Low		3		µA
ISD	Slow down supply current	SD* = Low, VDD = 3.3V, No load		3		mA
IDD	Operating current	VDD = 3.3V CLK1 = 40 MHz, No load CLK1 = 80 MHz, No load		5 10		mA

Table 8 • AC Specifications (Operating Conditions: T_A = 0°C – 70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Description	Test Condition @TA = 25°C	Min	Typ	Max	Unit
FXTAL	Crystal frequency			14.318		MHz
FIN	Input frequency		1	14.318	20	MHz
TIR	Input clock rise time				20	ns
TIF	Input clock fall time				20	ns
TR	Output clock rise time	15 pF load, VOUT = 0.8V to 2.0V			3	ns
TF	Output clock fall time	15 pF load, VOUT = 0.8V to 2.0V			3	ns
TDC	Duty cycle	15 pF load	45	48/52	55	%
TJCC	Jitter, cycle to cycle	CLK1 = 50 MHz		50	100	ps
TJLT	Jitter, long term (10,000 cycles)	CLK1 = 50 MHz		200	1000	ps
TFT	Frequency transition time	8 – 80 MHz without 1 nF LF cap		2		ms
		8 – 80 MHz with 1 nF LF cap		10		ms
TPU	Power up time	From OFF to 100 MHz without 1 nF LF cap		3		ms
		From OFF to 100 MHz with 1 nF LF cap		15		ms

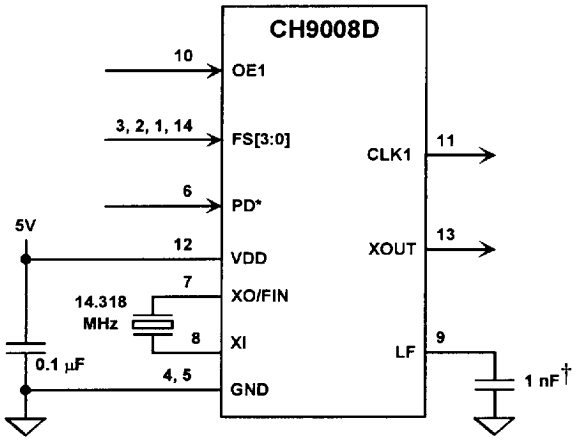

Figure 4: Application Schematic

Note: For other versions, please refer to pin descriptions for exact pin numbers and functions

† Typically a 1 nF capacitor, but may vary depending on application

ORDERING INFORMATION			
Part number	Package type	Number of pins	Voltage supply
CH9008x-N	300 mil PDIP	14	5V
CH9008x-S	150 mil SOIC	14	5V
CH9008x-N-L	300 mil PDIP	14	3.3V
CH9008x-S-L	150 mil SOIC	14	3.3V
Note: x = frequency table version			