Semiconductor Corporation

CS8125/6

T1/PCM-30 Optical Line Interface

Features

- Supports Links at 1.544 MHz or 2.048 MHz up to several km
- Supports both single-mode and multi-mode cable
- Receiver Sensitivities : 1 µA to 30 µA, or 30 nA to 30 µA
- Selectable Transmit Power Level, 10 mA to 100 mA
- Optical Dynamic Ranges: 15 dB, or 30 dB
- Monolithic Clock Recovery
- 3B4B Data Encoding/Decoding

General Description

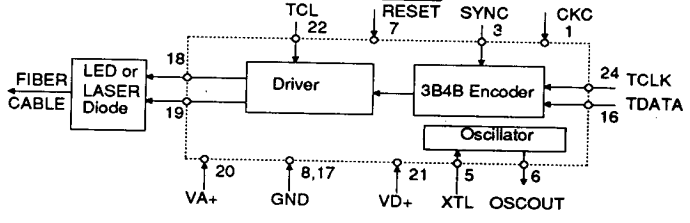
The CS8125 and CS8126 from Crystal Semiconductor Corporation are SMART Analog™ interface devices that receive and transmit serial binary data at T1/PCM-30 rates (up to 2.048 Mbps) over two fiber-optic cables. Combined with an external LED and PIN diode, the CS8125/6 provide a low-cost, easy-to-design optical link. Long transmission distances can be achieved by using a LASER diode and single-mode fiber. Functions included are 3B4B encoding/decoding, clock recovery, PIN diode amplification, and control of transmitter power.

Applications

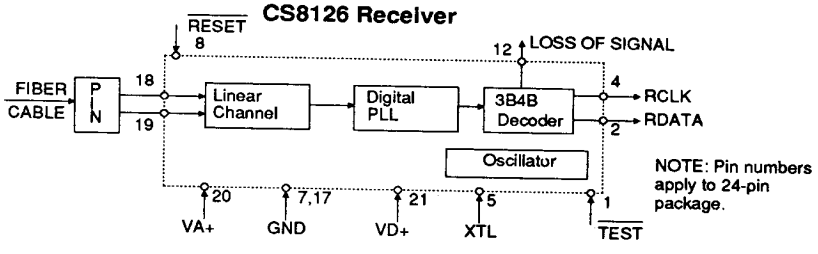
- Campus Networks
- Secure links
- Links in electrically noisy or hazardous environments

ORDERING INFORMATION: Page 8-32

CS8125 Transmitter



CS8126 Receiver



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Preliminary Product Information | This document contains information on a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (VA+, VD+ pins)	V+	-0.3	6.0	V
Input Voltage	V_{in}	GND -0.3	(V+) + 0.3	V
Input Current (Note 1) (Any pin except LDP, LDN, VA+, VD+ & GND)	I_{in}	-	10	mA
Storage Temperature	T_{stg}	-65	150	°C
Power Dissipation	P_D	-	500	mW

WARNING: Operating this device at or beyond these limits may result in permanent damage to the device. Normal operation of the part is not guaranteed at or beyond these extremes.

Note: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Units
DC Supply	V+	4.75	5.0	5.25	V
Ambient Operating Temperature	T_A	-40	25	85	°C
Optical Transmitter Drive Current (Note 2)	I_{out}	90	100	115	mA
Power Consumption, CS8125 (Note 3,4)	P_C	-	375	475	mW
Power Consumption, CS8126 (Note 3,4)	P_C	-	125	150	mW

Note: 2. Measured with TCL floating.
3. Total power dissipated by IC and optical component.
4. Over operating temperature range

DIGITAL CHARACTERISTICS (TA = -40 °C to 85 °C; VA+, VD+ = 5V ± 5%; GND = 0V)

Parameter	Symbol	Min	Typ	Max	Units
High-Level Input Voltage (Note 5)	V_{IH}	2.0	-	-	V
High-Level Input Voltage (XTL only)	V_{IH}	.9 VD+	-	-	V
Low-Level Input Voltage (Note 5)	V_{IL}	-	-	0.8	V
Low-Level Input Voltage (XTL only)	V_{IL}	-	-	.2 VD+	V
High-Level Output Voltage I_{OUT} = -40 uA (Notes 6,7)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage I_{OUT} = 1.6 mA (Notes 6,7)	V_{OL}	-	-	0.4	V
Input Leakage Current	I_{in}	-	± 10.0	-	uA

Notes: 5. Input pins are: TCLK, TDATA, SYNC, $\overline{\text{RESET}}$.
6. Output pins are: RDATA, RCLK, LOS, and OSCOUT (CS8125 only).
7. Output drivers will output CMOS logic levels into a CMOS load.

ANALOG SPECIFICATIONS (TA =-40 °C to 85 °C; VA+, VD+ = 5V ± 5%; GND = OV)

Parameter		Symbol	Min	Typ	Max	Units
CS8126 Receiver Input Current	- IP5, IP6 - IP	I_{IN}	1 30	- -	30 30,000	uA nA
Transmitter Jitter Tolerance	(Note 8)	-	-	12	-	UI p-p

Note: 8. Jitter tolerance increases as jitter frequency decreases.

SWITCHING CHARACTERISTICS (TA = -40 °C to 85 °C; VA+, VD+ = 5V ± 5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
XTL Frequency	T1 PCM-30	f_c	- -	12.352 16.384	- -	MHz MHz
TCLK & Average RCLK Frequency:	(Note 9)	f_{ckc}	-	$f_c/8$	-	kHz
RCLK & TCLK Duty Cycle, and Overdriven Crystal Duty Cycle	(Note 10)		-	50	-	%
Rise Time, All Digital Outputs	(Note 11)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 11)	t_f	-	-	100	ns
TDATA to TCLK Rising Setup Time		t_{su}	200	-	-	ns
TCLK Falling to TDATA Hold Time		t_h	25	-	-	ns
RDATA to RCLK Rising Setup Time		t_{su}	-	$\frac{1}{2 f_{ckc}}$ -100	-	ns
RCLK Rising to RDATA Hold Time		t_h	-	$\frac{1}{2 f_{ckc}}$ +100	-	ns
Frequency Deviation at TCLK Input from f_c /8	(Note 12)		-	-	500	ppm

Notes: 9. Every fourth cycle of RCLK is dropped. The period of those RCLK cycles that are output is $1/6f_c$. See text section on CS8126 optical receiver.
10. Duty cycle is $(t_{pwh}/(t_{pwh} + t_{pwl})) * 100\%$.
11. At maximum load of 1.6 mA and 50 pF.
12. Crystal frequency must be within ± 50 ppm of specified frequency.

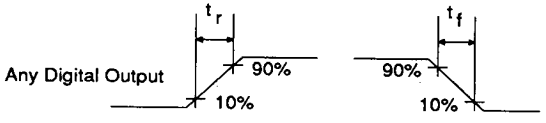


Figure 1. Digital Output Rise and Fall Characteristics

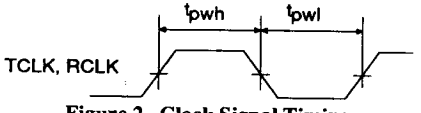


Figure 2. Clock Signal Timing

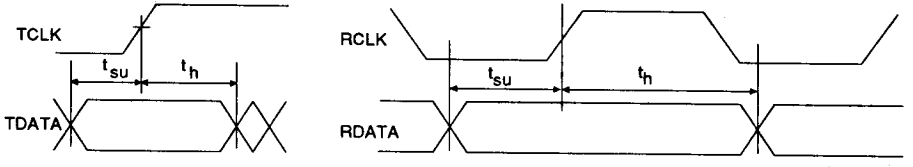


Figure 3. Switching Characteristics

CIRCUIT DESCRIPTION

The CS8125 T1/PCM-30 Optical Transmitter and CS8126 T1/PCM-30 Optical Receiver can be used to transport 1.544 Mbps (or 2.048 Mbps) data over several kilometers of multimode fiber. The only external components required are a quartz crystal, an optical emitter (LED) and an optical receiver (PIN diode with biasing circuit), as shown in Figure 6. Transmission distances can be significantly increased by use of single-mode fiber and a LASER diode as an optical transmitter. The only limitation on transmission distance is that sufficient current must be driven into the CS8126 LDN/LDP inputs.

The CS8125 transmitter accepts NRZ input data, sampled on the rising edge of TCLK, and encodes the user data in a 3B4B line code before transmitting onto the fiber. The 3B4B encoding rules are shown in Table 1. 3B4B encoding transmits four bits for every three input to the CS8125 thereby ensuring sufficient ones density to maintain receiver lock even if all zero data is input for transmission. A synchronization pattern can be generated upon user request. The transmit power level is user selectable.

Input binary	Coded binary
001	0011
010	0101
100	1001
011	0110
101	1010
110	1100
000	0010 alternated with 1101
111	1011 alternated with 0100

Table 1. Translation Rules for the 3B4B

The CS8126 receiver accepts 3B4B encoded information, recovers clock, decodes the 3B4B line code and outputs NRZ data which can be sampled using the rising edge of the receive clock output pin, RCLK. A loss of signal output, LOS, indicates when transmission has been interrupted.

Total transmission delay is generally less than 14 bit periods through the CS8125 and 4 bit periods through the CS8126.

CS8125 T1/PCM-30 OPTICAL TRANSMITTER

The CS8125 accepts data on the TDATA input pin on the rising edge of TCLK. The data is encoded using the 3B4B line code before transmission through the external LED or laser. The CS8125 has a current mode driver with sufficient drive current (up to 100 mA) to drive either an LED (for multi-mode cable) or a laser (for single-mode cable).

The transmit current level is typically 100 mA when TCL is left unconnected. The current level may be adjusted, as shown in Figure 4, by tying the TCL pin to ground through a resistor. Tying TCL directly to ground selects the minimum drive current of 10 mA. The output drive current corresponding to a given resistor can be calculated using the following equation:

$$I_{drive} = 100 \left(\frac{110 + R_{TCL}}{1100 + R_{TCL}} \right) mA$$

Equation 1.

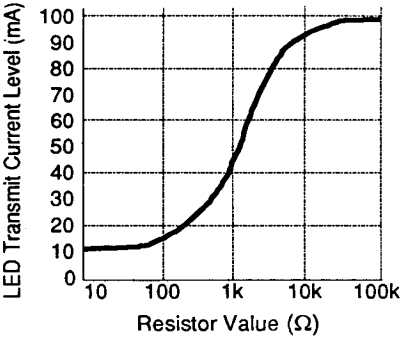


Figure 4. Resistor to Set the Transmit Current Level

The CS8125 requires an 8-times-1.544 MHz external crystal or input clock (12.352 MHz). For 2.048 MHz operation, the XTL pin should be overdriven by a 16.384 MHz clock. This clock must meet the input requirements of the XTL pin: see Digital Characteristics Table. The external crystal or input clock is attached to the XTL pin. The 12.352 MHz output clock is output on pin OSCOUT, which can be used to drive the XTL input of the CS8126, thus allowing one crystal to support both the CS8125 and CS8126. For 2.048 Mbps operation, both the CS8125 and CS8126 should be driven by the external 16.384 MHz clock oscillator. Because of the 3B4B line code used, the actual data rate on the cable is the crystal frequency divided by 6.

TCLK may be internally generated or input from an external source based on the state of the Clock Control pin, CKC. If CKC is high, the TCLK output rate is XTL frequency ÷ 8. When CKC is floated or pulled low, TCLK must be externally generated. Externally generated TCLK may deviate from XTL ÷ 8 by several hundred ppm. Similarly, the transmit FIFO and internal timing mechanisms can tolerate huge amounts of TCLK jitter.

Under the control of the SYNC pin, the CS8125 will generate a repetitive encoded pattern to achieve 3B4B code alignment of the far-end CS8126 prior to the transmission of data. The far-end CS8126 takes no special action in response to this pattern, other than decoder alignment and normal 3B4B decoding. The CS8126 will synchronize to a random data pattern, but the synchronization time is somewhat unpredictable since it is dependent on the data and the corresponding 3B4B code. The SYNC function ensures receive lock in the shortest possible time.

The synchronization code used is a repetitive 110001 pattern which is encoded as 11000011. The user must maintain SYNC high for 50 ms. When the user returns SYNC low, there will be up to 20 bits (typically 12 bits) of undefined data between the end of the synchronization codes and the start of valid user data as the synchronization codes are flushed from the transmit FIFO.

CS8126 T1/PCM-30 OPTICAL RECEIVER

The external PIN diode detects the data from the far-end CS8125. The PIN diode output signal is input to the CS8126 using the biasing circuit shown in the Application Section of this data sheet. A digital phase-lock loop performs the timing recovery. When the CS8126 is sychronized to the incoming signal; LOS, pin 12, goes low. The 3B4B line code is decoded and the recovered signal is output on RDATA, and may be sampled using RCLK. As a result of the 3B4B decoding, RCLK is output at 4/3 the data rate (crystal-divided-by-6 frequency) with every fourth clock dropped as shown in Figure 5. A CS61600 PCM Jitter Attenuator, or a CS61544's or a CS61535A's on-chip transmit jitter attenuator, can be used to eliminate this line code induced jitter.

The CS8126 establishes a machine cycle which is 96 bit periods long. During its machine cycle, the CS8126 determines how to update its digital PLL

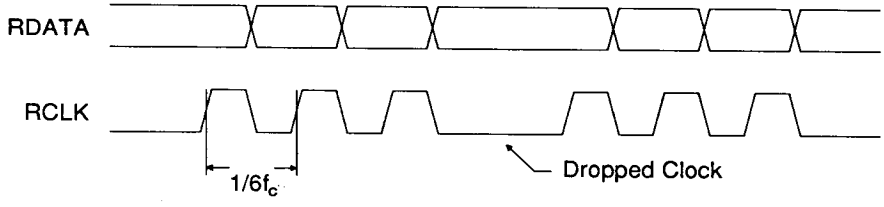


Figure 5. Receiver Output Timing

to maintain lock on the incoming signal, and monitors the 3B4B code. The CS8126 will declare LOS if there are two 3B4B code violations in four (or fewer) machine cycles. When the CS8126 detects loss of signal, the LOS output pin is set high and a device reset automatically occurs. A reset clears all internal logic, and the CS8126 attempts to resynchronize to the incoming signal. Synchronization is declared (LOS goes low) when there are no 3B4B code violations for an entire machine cycle. The machine cycle timing is internally established, and not accessable by the user.

When no signal is presented to the LDP/LDN inputs (for example, when no cable is attached to the PIN diode, or if the PIN diode is not attached to LDP/LDN), the LOS output may wink due to nonrandom noise coupling in the receiver. The noise will occasionally mimic a valid 3B4B input code. The typical duration of a LOS low state due to noise is 250 µs. An RC filter can be used on the LOS output to remove the winks. When LOS returns high, the CS8126 does a reset which temporarily interrupts the RCLK output.

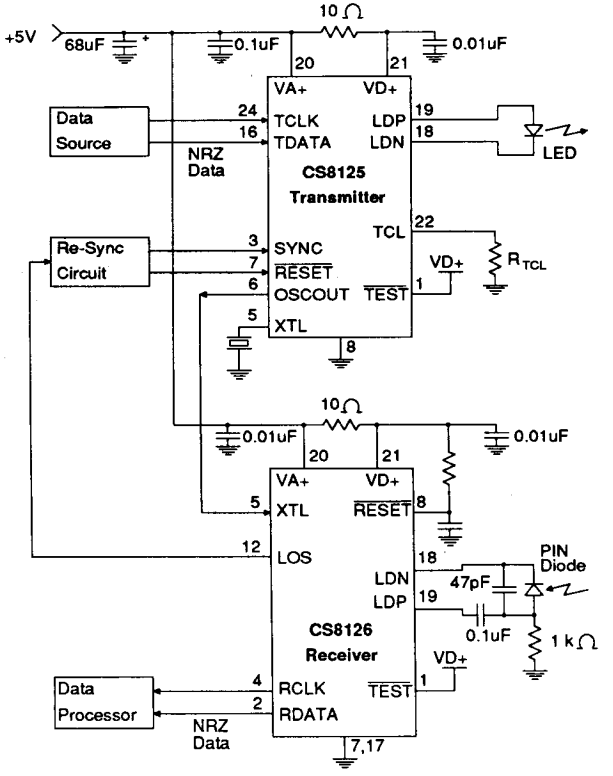
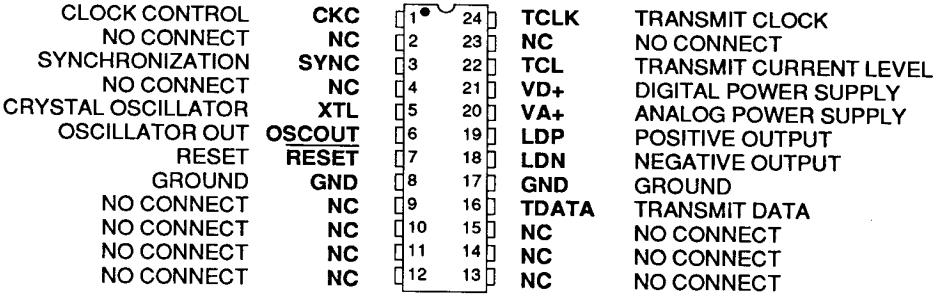


Figure 6. System Connection Diagram For One End of the Communications Link

PIN DESCRIPTIONS

CS8125 T1/PCM-30 Optical Driver



Power Supplies

VA+ - Analog Power Supply, Pin 20.
Typically +5 volts.

VD+ - Digital Power Supply, Pin 21.
Typically +5 volts.

GND - Ground, Pins 8 and 17.
Ground reference.

Oscillator

XTL - Crystal Oscillator, Pin 5.
Crystal or external clock input. When used with a crystal, this pin should be pulled to the VD+ supply with a 1 MΩ resistor. The crystal, if used, should be parallel resonant with one pin connected to XTL with minimal length trace on the printed circuit board; the other pin of the crystal should be tied to ground. T1 operation requires a 12.352 MHz (± 50 ppm at 14 pF) crystal or external oscillator. PCM-30 operation requires a 16.384 MHz external oscillator. Slower frequencies may be used to adjust the data link throughput and data rates. The crystal's series resistance must be below 13Ω to ensure oscillator startup.

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IMPORTANT NOTE: The initial DIP package will be 600-mil wide. Crystal will be introducing a 300-mil DIP package in the future, at which time the 600-mil package wil be discontinued. All through-hole board designs for the 600-mil package should have a dual footprint so that the 300-mil package can be dropped in at a later time.

Inputs

TDATA, TCLK - Transmit Data, Pin 16; Transmit Clock, Pin 24.

TDATA is data to be transmitted. Data is clocked into the CS8125 on the rising edge of TCLK. TCLK is either a clock input or output depending on the state of the CKC pin. TDATA is sampled on the rising edge of TCLK.

CKC - Clock Control, Pin 1.

CKC defines the source of the TCLK signal. If CKC is left floating or pulled low, an externally-provided clock should be input on TCLK. A high on CKC will result in the CS8125 outputting TCLK at 1.544 MHz or 2.048 MHz (more precisely, at one-eighth of the XTL rate).

SYNC - Synchronization Request , Pin 3.

A high level causes a synchronization pattern to be transmitted. SYNC has an internal pull down.

TCL - Transmit Current Level, Pin 22.

Defines the current driven into LDP/LDN. When left unconnected, the current level is typically 100 mA. When tied to ground, output current level is at a minimum of about 10 mA. Current can be set at an intermediate level, (as shown in Figure 4 in the Circuit Description section), by tying this pin through a resistor to ground.

$\overline{\text{RESET}}$ - Reset, Pin 7.

A level sensitive input which causes the CS8125 to reset all of its internal logic when the pin is pulled low. Reset has precedence over every other operational state.

Outputs

LDP; LDN - Laser/LED Positive Output; Laser/LED Negative Output, Pins 19 & 18.

These pins connect directly to the LED or Laser. LDP connects to the optical component anode and LDN connects to the optical component cathode.

OSCOUT - Oscillator Out, Pin 6.

This output signal matches the input frequency of the XTL input. OSCOUT can generally be connected to the XTL pin of a companion CS8126, however this pin may not have sufficient speed or drive capability to drive the CS8126 XTL pin at frequencies approaching 16 MHz.

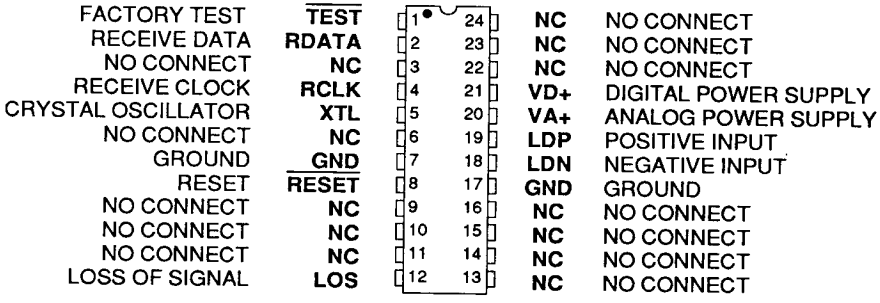
No Connects

NC - No Connect, Pins 2, 4, 9-15, 23.

Must be left floating.

PIN DESCRIPTIONS (Pin Numbers Below Refer To Dip Package)

CS8126 T1/PCM-30 Optical Receiver



Power Supplies

VA+ - Analog Power Supply, Pin 20.
Typically +5 volts.

VD+ - Digital Power Supply, Pin 21.
Typically +5 volts.

GND - Ground, Pins 7 and 17.
Ground reference.

Oscillator

XTL - Crystal Oscillator, Pin 5.
Crystal or external clock input. When used with a crystal, this pin should be pulled up to the VD+ supply with a 1 MΩ resistor. The crystal, if used, should be parallel resonant with one pin connected to XTL with minimal length trace on the printed circuit board; the other pin of the crystal should be tied to ground. T1 operation requires a 12.352 MHz (± 50 ppm at 14 pF) crystal or external oscillator. PCM-30 operation requires a 16.384 MHz external oscillator. Slower frequencies may be used to adjust the data link throughput and data rates.

Inputs

LDP; LDN - PIN Diode Positive Input; PIN Diode Negative Input, Pins 19 & 18.
These pins connect to the PIN diode through the biasing circuit show in the application section.

IMPORTANT NOTE: The initial DIP package will be 600-mil wide. Crystal will be introducing a 300-mil DIP package in the future, at which time the 600-mil package wil be discontinued. All through-hole board designs for the 600-mil package should have a dual footprint so that the 300-mil package can be dropped in at a later time.

$\overline{\text{RESET}}$ - Reset, Pin 8.

A level sensitive input to the CS8126 which resets all of its internal logic when the pin is pulled low. After reset, the data recovery circuit must resynchronize to the incoming data stream. Reset has precedence over every other operational state.

$\overline{\text{TEST}}$ - Factory Test, Pin 1.

Must be tied to logic high for normal operation. This pin should be connected to VD+ or to the supply through a 10kΩ resistor.

Outputs

LOS - Loss of Signal, Pin 12.

A high level indicates that the CS8126 is not synchronized. LOS goes low to indicate that the CS8126 is synchronized to the incoming data.

RDATA, RCLK - Received Data, Pin 2; Received Clock, Pin 4.

RDATA is valid and stable on the rising edge of RCLK.

Ordering Guide

Model	Frequency	Package*	Minimum Receiver Input Current
CS8125-IP5	T1 Only (1.544 Mbps)	24-Pin 0.6" DIP	-
CS8125-IP6	PCM-30 Only (2.048 Mbps)	24-Pin 0.6" DIP	-
CS8125A-IP	T1 & PCM-30	24-Pin 0.3" DIP	-
CS8126-IP5	T1 Only (1.544 Mbps)	24-Pin 0.6" DIP	1 µA
CS8126-IP6	PCM-30 Only (2.048 Mbps)	24-Pin 0.6" DIP	1 µA
CS8126A-IP	T1 & PCM-30	24-Pin 0.3" DIP	30 nA

* The 24-Pin, 0.6" DIP package will be discontinued and replaced by the 24-Pin, 0.3" DIP package. Lay out your PCB for both.

APPLICATION NOTES

The use of a CDB8125/6 Evaluation Board to evaluate an optical link is highly recommended because system performance is highly dependent upon the quality of the board layout.

Power Supply Decoupling

VA+, VD+ and GND should be decoupled using the circuit shown in Figure A1. The 68 µF capacitor is required to filter the power supply, and prevent power supply ripple, and should placed close to the CS8125/6. The 0.1 µF capacitor and 0.01 µF capacitor should be placed as close as possible to the CS8125/6. Any other ICs on the same board or sharing the same power supply should also be decoupled.

Because of the sensitivity of the analog circuitry to power supply noise, evaluation of the CS8125/6 using wire-wrapped boards is not recommended.

Inexpensive Fiber Optic Cables and LED's

Hewlett-Packard's LED's for plastic fibers (the VERSATILE HFBR-152x family) can be used for very low cost links. These LED's are approximately one-third the cost of the glass-fiber compatible LED's. However, the length of the cable is limited by the attenuation characteristics of plastic fiber (about 1dB per meter).

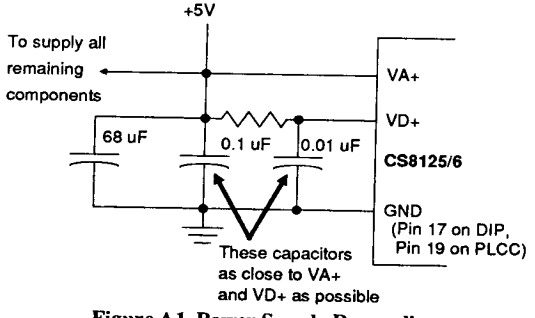


Figure A1. Power Supply Decoupling

Calculating a Link Budget

A link budget is used to determine the range of fiber lengths and operating margin for a CS8125 to CS8126 link. The link budget takes into account: the power coupled to the fiber from the optical transmitter, the loss of the fiber, and the responsivity of the optical receiver. Fiber coupled power and responsivity are significantly affected by temperature. The wavelength of the transmitted light will also change with temperature. Responsivity of the receiver diode will vary with wavelength. Optical transmitters and receivers must be compatible (operate at the same wavelength). Losses due to splices and environmental factors, etc. must be considered when calculating a link budget.

Fiber coupled power depends on the numerical aperture and diameter of the fiber, with larger diameter fiber coupling significantly more light power than small diameter fiber. Fiber coupled power varies in inverse proportion to temperature. The loss of a fiber is generally expressed in dB/km. The larger the diameter of the fiber, the greater the loss of light power. Loss will be slightly greater for short (much less than 1 km) fibers. Responsivity is a measure of the amount of current generated by a diode when light is shined on it and is expressed in amps/watt of light power. Responsivity is dependent on wavelength and varies in proportion to temperature. Table A1 shows some parameters for calculating link budgets for different fiber diameters when using a typical LED transmitter and PIN diode receiver.

To calculate the maximum cable length for 100/140 µm fiber at a fixed temperature, first calculate the amount of light power needed at the PIN diode to generate 1 µA of output current (the minimum required by the CS8126).

$$P_{Rx} = \frac{1\ uA}{0.24\ A/W} = 4.17\ uW$$

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Cable Type	NA	Fiber Loss	LED Launch Power	PIN Responsivity
200 µm	0.37	6 dB/km	640 µW	0.15 A/W
100/140 µm	0.30	4.5 dB/km	116 µW	0.24 A/W
62.5/125 µm	0.275	3.75 dB/km	44 µW	0.27 A/W
50/125 µm	0.20	3.5 dB/km	20 µW	0.30 A/W

Table A1. Typical Link Budget Values

The allowable loss due to cable and splices is:

Power Margin = 10 log(launched power / P_{Rx})
= 10 log(116µW/4.17µW)
= 14.44 dB

Cable loss is 4.5 dB/km which would allow a transmision distance of 3.21 km, max. Selecting an LED with more output power and a PIN with more responsivity will allow longer transmission distances. It is wise to allow about 3 dB of operating margin, and transmission media loss due to splices or other factors should also be accounted for.

If the ends of the link are expected to be at different temperatures, additional margin should be provided to compensate for loss in performance of the LED and PIN. If the temperature increases or decreases at both ends of the link such that the two ends remain within a few degrees of each other, the link budget will remain essentially the same. Loss in performance at one end is compensated for by improved performance at the other end.

CS8126 PIN Diode Biasing Circuit

The object of the circuit is to provide a 2.5 V reverse bias on the PIN diode, and approximately a 47 pF load to LDP/LDN. In addition, the 47 pF capacitor shunting the LDN & LDP pins ensures the stability of the receiver. With a noisy ground environment, an optional 20 pF capacitor from LDN to ground may be required. This capacitor couples noise into LDN that is equal to noise coupled into LDP by the 10 MΩ resistor.

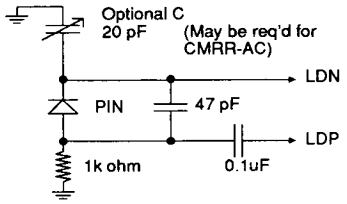

Figure A2. PIN Diode Biasing

Oscillator Considerations

T1 applications can input either a 12.352 quartz crystal or clock signal to XTL. PCM-30 applications must input a 16.384 MHz signal to XTL.

When using a crystal, the following considerations are important. A 1 MΩ pull-up resistor is required between the XTL pin and V+. The crystal should be located as close as possible to the XTL pin. One end of the resistor should also be physically close to the XTL pin. The other end of the resistor (which is tied to V+) should be located away from the IC. The resistor should not be on the back of the PCB directly underneath the IC. The total capacitance on the XTL input (including capacitance resulting from adjacent traces, power supplies, socket, etc.) should be ≤ 4pF. The crystal requirements are: $C_O \leq 5.5$ pF; 12.352 MHz at C_L = 14pF; R_S=9Ω (typically). In

all cases, $R_S < 13\Omega$. The lower the resistance, the more reliable the oscillator start-up will be.

Layout Considerations

It is recommended that a healthy amount of ground plane be used around LDP and LDN, and the LED pins (on both sides of the board in case of two-layer boards); and also around the quartz crystal.

Resynchronization Considerations

The RESET-SYNC circuit shown in Figure A3 is intended to ensure minimum synchronization time upon power-up or after a Loss of Signal, LOS, condition occurs. If transmission of a normally functioning link is interrupted, the LOS pin on the CS8126 will go high. The RESET portion of the circuit will cause a short reset of the CS8125. This reset interrupts transmission, thereby causing a LOS condition to occur at the far end of the link, which in turn resets the far end CS8125. Both CS8125s will transition from the RESET condition to the SYNC state, which will ensure minimum synchronization time. The CS8125 will stay in the SYNC state until after the CS8126 has established synchronization.

Repeating

For recovery and retransmission of the signal, simply connect a CS8126 RCLK and RDATA outputs to the TCLK and TDATA inputs of a CS8125. It is not necessary to clean up the CS8126 RCLK output.

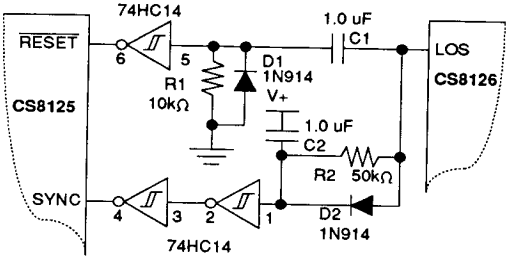

Figure A3. RESET-SYNC Circuit.

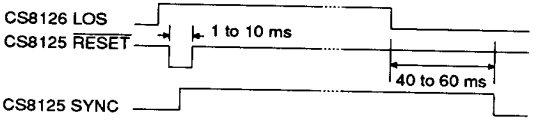

Figure A4. Resynchronization Timing

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