FERRANTI semiconductors®

D-A/A-D CONVERTER

ZN425 Series

8 Bit Monolithic D to A/A to D Converter

FEATURES

- **8, 7 and 6 bit Accuracy**
- **0°C to +70°C (ZN425E Series)**
- **–55°C to +125°C (ZN425J-8)**
- **TTL and 5V CMOS Compatible**
- **Single +5V Supply**
- **Settling Time (D to A) 1 μsec Typical**
- **Conversion Time (A to D) 1 msec typical, using ramp and compare.**
- **Extra Components Required**
  - **D-A : Reference capacitor (direct voltage output through 10 kΩ typ.)**
  - **A-D : Comparator, gate, clock and reference capacitor**

DESCRIPTION

The ZN425 is a monolithic 8-bit digital to analogue converter containing an R-2R ladder network of diffused resistors with precision bipolar switches, and in addition a counter and a 2.5V precision voltage reference. The counter is a powerful addition which allows a precision staircase to be generated very simply merely by clocking the counter.

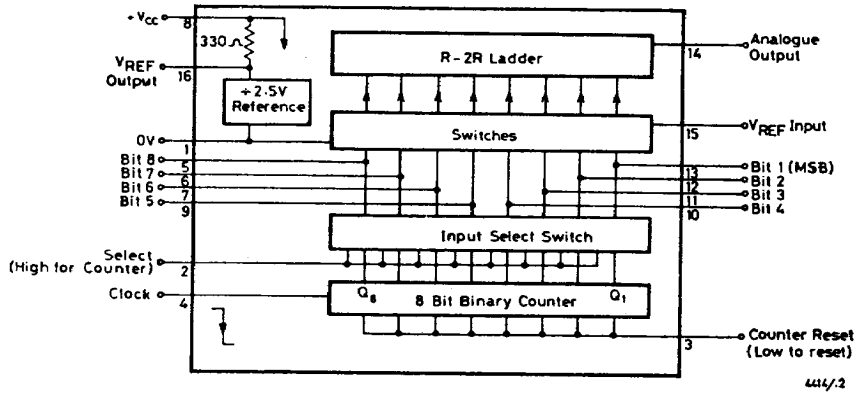


Fig. 1 – System Diagram

ZN425 Series

INTRODUCTION

The ZN425 is an 8-bit dual mode digital to analogue/analogue to digital converter. It contains an 8-bit D to A converter using an advanced design of R-2R ladder network and an array of precision bipolar switches plus an 8-bit binary counter and a 2.5 volt precision voltage reference all on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

By including on the chip an 8-bit binary counter, analogue to digital conversion can be obtained simply by adding an external comparator (ZN424P) and clock inhibit gating (ZN7400E).

By simply clocking the counter the ZN425 can be used as a self-contained precision ramp generator.

A logic input select switch is incorporated which determines whether the precision switches accept the outputs from the binary counter or external digital inputs depending upon whether the control signal is respectively high or low.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

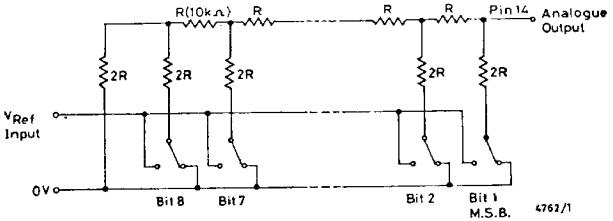


Fig. 2 – The R-2R Ladder Network

Each 2R element is connected either to 0V or V_{REF} by transistor switches specially designed for low offset voltage (typically 1 millivolt).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

ORDERING INFORMATION

Operating Temperature	8-bit Accuracy	7-bit Accuracy	6-bit Accuracy	Package
0°C to +70°C	ZN425E-8	ZN425E-7	ZN425E-6	Plastic
–55°C to +125°C	ZN425J-8	—	—	Ceramic

ABSOLUTE MAXIMUM RATINGS

Supply voltage V_{CC} .. .. +7·0 volts
Max. voltage, logic and V_{REF} inputs .. .. +5·5 volts *See note 3*
Operating temperature range .. .. .. 0°C to +70°C (ZN425E Series)
–55°C to +125°C (ZN425J-8)
Storage temperature range .. .. –55°C to +125°C

CHARACTERISTICS (at T_{amb} = 25°C and V_{CC} = +5 volts unless otherwise specified).

Internal voltage reference

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Output voltage	V_{REF}	2·4	2·55	2·7	volts	I = 7·5 mA (internal)
Slope resistance	R_s	—	2	4	ohms	I = 7·5 mA (internal)
V_{REF} Temperature coefficient		—	40	—	ppm/°C	I = 7·5 mA (internal)

Note: The internal reference requires a 0·22 μF stabilising capacitor between pins 1 and 16.

8-Bit D to A Converter and Counter

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Resolution		8	—	—	bits	
Accuracy (useful resolution) ZN425J-8		8	—	—	bits	V_{REF} Input = 2 to 3V
ZN425E-8		8	—	—	bits	
ZN425E-7		7	—	—	bits	
ZN425E-6		6	—	—	bits	
Non-linearity		—	—	±0·5	L.S.B.	*See Note 3*
Differential non-linearity		—	±0·5	—	L.S.B.	*See Note 6*
Settling time		—	1·0	—	μs	1 L.S.B. step
Settling time to 0·5 L.S.B.		—	1·5	2·5	μs	All bits ON to OFF or OFF to ON
Offset voltage ZN425J-8	V_{OS}	—	8	12	mV	All bits OFF *See Note 3*
ZN425E-8, ZN425E-6, ZN425E-7		—	3	8	mV	
Full scale output		2·545	2·550	2·555	volts	All bits ON Ext. V_{REF}=2·56V
Full scale temperature coeff.		—	3	—	ppm/°C	Ext. V_{REF}=2·56V
Non-linearity error temp. coeff.		—	7·5	—	ppm/°C	Relative to F.S.R.
Analogue output resistance	R_o	—	10	—	kΩ	
External reference voltage		0	—	3·0	volts	
Supply voltage	V_{CC}	4·5	—	5·5	volts	*See Note 3*
Supply current	I_s	—	25	35	mA	
High level input voltage	V_{IH}	2·0	—	—	volts	*See Notes 1 and 2*
Low level input voltage	V_{IL}	—	—	0·7	volts	

CHARACTERISTICS *(continued)*.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
High level input current	I_{IH}	—	—	10	μA	V_{CC} = max. V_I = 2·4V
		—	—	100	μA	V_{CC} = max. V_I = 5·5V
Low level input current, bit inputs	I_{IL}	—	—	–0·68	mA	V_{CC} = max. V_I = 0·3V
Low level input current, clock reset and input select	I_L	—	—	–0·18	mA	
High level output current	I_{OH}	—	—	–40	μA	
Low level output current	I_{OL}	—	—	1·6	mA	
High level output voltage	V_{OH}	2·4	—	—	volts	V_{CC} = min. Q = 1 I_{load} = –40 μA
Low level output voltage	V_{OL}	—	—	0·4	volts	V_{CC} = min. Q = 0 I_{load} = 1·6 mA
Maximum counter clock frequency	f_c	3	5	—	MHz	*See Note 5*
Reset pulse width	t_R	200	—	—	ns	*See Note 4*

Notes:

1. The Input Select pin (2) must be held low when the bit pins (5, 6, 7, 9, 10, 11, 12 and 13) are driven externally.
2. To obtain counter outputs on bit pins the Input Select pin (2) should be taken to $+V_{CC}$ via a 1 kΩ resistor.
3. The ZN425J differs from the ZN425E in the following respects:
   (a) For the ZN425J, the maximum linearity error may increase to ±1 LSB over the temperature ranges –55°C to 0°C and +70°C to +125°C.
   (b) Maximum operating voltage. Between 70°C and 125°C the maximum supply voltage is reduced to 5.0V.
   (c) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
4. The device may be reset by gating from its own counter.
5. F_{max} in A/D mode is 300 kHz, see page 6.
6. Monotonic over full operating temperature range at resolution appropriate to accuracy.

If Pin 2 is high then the output equals the Q output of the corresponding counter.

If Pin 2 is low then the output transistor, Tr1 is held off.

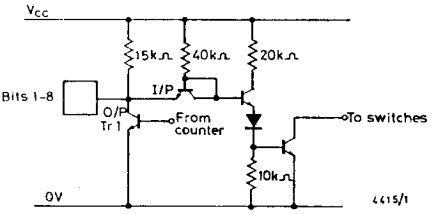


Fig. 3 – Bit Inputs/Outputs

APPLICATIONS

1. 8-bit D to A Converter

The ZN425 gives an analogue voltage output directly from pin 14 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the Analogue Output Resistance R_o, will be less than 0·004% per °C (or 1 L.S.B./100°C) if R_L is chosen to be $\geqslant 650\ k\Omega$.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 4 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6 kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust R_2 until $V_{out} = 0{\cdot}000V$.

ii. Set all bits to ON (high) and adjust R_1 until V_{out} = Nominal full scale reading – 1 L.S.B.

iii. Repeat *i.* and *ii.*

e.g. Set F.S.R. to +3·840 volts – 1 L.S.B.

= 3·825 volts

$$(1\ \text{L.S.B.} = \frac{3{\cdot}84}{256} = 15{\cdot}0\ \text{millivolts.})$$

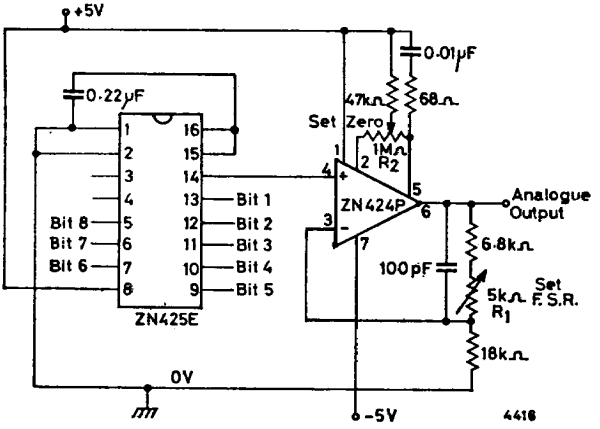


Fig. 4 – 8-bit Digital to Analogue Converter

2. 8-bit Analogue to Digital Converter

A counter type ADC can be constructed by adding a voltage comparator and a latch as in Fig. 5. On the negative edge of the CONVERT COMMAND pulse (15 μs minimum) the counter is set to zero and the STATUS latch to logical 1. On the positive edge the gate is opened, enabling clock pulses to be fed to the counter input of the ZN425. The minimum negative clock pulse width to the ZN425 is 100 ns. The analogue output of the ZN425 ramps until it equals the voltage on the other input of the comparator. At this point the comparator output goes low and resets the STATUS latch to inhibit further clock pulses. The logical 0 from the status latch indicates that the 8 bit digital output is a valid representation of the analogue input voltage.

A small capacitor of 47 pF is added to the ZN425 output to stop any positive going glitches prematurely resetting the status latch. This capacitance is in parallel with the ZN425 output capacitance (20–30 pF) and they form a time constant with the ZN425 output resistance (10 kΩ). This time constant is the main limit to the maximum clock frequency. With a fast comparator the clock frequency can be up to 300 kHz. Using the ZN424P as a comparator the clock frequency should be restricted to 100 kHz. The conversion time varies with the input, being a maximum for full scale input.

$$\text{Maximum conversion time} = \frac{256}{\text{clock frequency in Hz}} \text{ seconds}$$

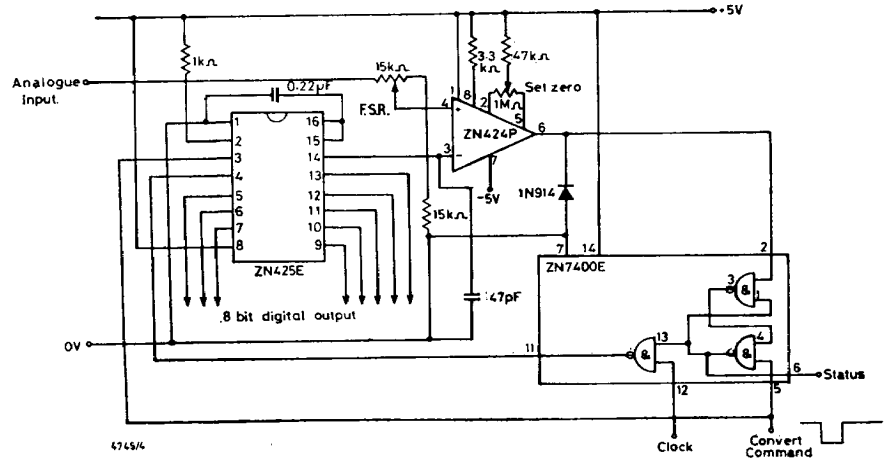


Fig. 5 – 8-bit Analogue to Digital Converter

3. Precision Ramp Generator

The inclusion of an 8-bit binary counter on the chip gives the ZN425 a useful ramp generator function. The circuit, Fig. 6 uses the same buffer stages as the D to A converter. The calibration procedure is also the same. Holding pin 2 low will set all bits to ON and if RESET is taken low with pin 2 high all the bits are turned OFF. If the end voltages of the ramp are not required to be set accurately then the buffer stage could be omitted and the voltage ramp will appear directly at pin 14.

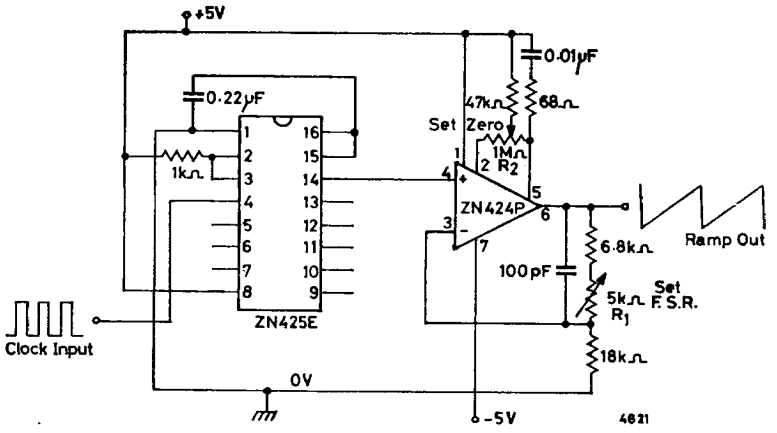


Fig. 6 – Precision Ramp Generator

4. Alternative Output Buffer using the ZLD741

The following circuit, employing the ZLD741 operational amplifier, may be used as the output buffer for both the 8-bit Digital to Analogue Converter (Fig. 4) and the Precision Ramp Generator (Fig. 6).

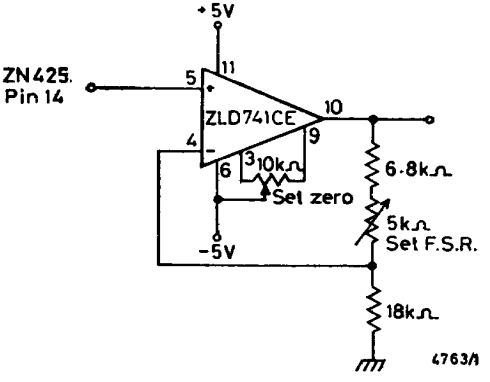
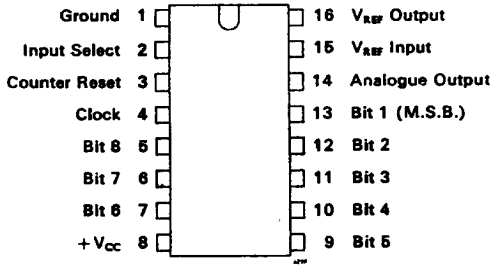


Fig. 7 – The ZLD741 as Output Buffer

5. Further Applications

Details of a wide range of additional applications, described in the Ferranti publication 'Application Report–ZN425 8-bit A-D/D-A Converter', are also available.

PIN CONNECTIONS



CHIP DIMENSIONS AND LAYOUT