Read/Write Identification IC with 1 Kbit Memory

Functional Description

The e5552 is a two terminal, contactless R/W-**ID**entification **IC** (IDIC)* for tag applications in the 125 kHz (± 25 kHz) range. The IC uses the external RF signal to generate it's own power supply and internal clock reference.

The IC contains a total of 1056 bits of EEPROM memory grouped into 32 individually addressable data blocks. Each block is made up of 32 bits of data plus an associated lock bit for block write protection. Blocks 1 to 31 are provided for user related data and block 0 for system configuration.

Data is transmitted from the IC (uplink) using reflective load (backscatter) modulation. This is achieved by damping the external RF field by switching a resistive load between the two terminals Clock–A/Clock–B as shown in figure 14 (downlink). The IC receives and decodes amplitude modulated data from the base station.

As soon as the tag included the e5552 is exposed to an RF field and the field is strong enough to derive enough energy to operate, the tag will respond by continuously transmitting stored data (uplink mode). The base station can at any time switch the tag into downlink mode to write new user or configuration data. Generally the tag will automatically return to the default uplink mode when the downlink transfer is complete or interrupted or if an error condition occurs.

Features

- Low power, low voltage operation
- ESD protection: > 8 kV (HBM)
- Optimized for flipchip die attach processes
- Contactless power supply
- Contactless read/write data transmission
- Radio Frequency (RF): 100 kHz to 150 kHz
- 1056 bits of EEPROM memory
- 992 bits (31 x 32 bits) of user memory
- Defined start of data transmission
- Auto-verify after EEPROM programming
- Block write protection for each block
- Configurable options include:
  - Modulation type: PSK | Manchester
  - Bit rate [bit/s]: RF/16 | RF/32
  - Number of readable blocks
  - Modulation defeat
  - POR start-up delay: ≈ 1 ms | ≈ 65 ms

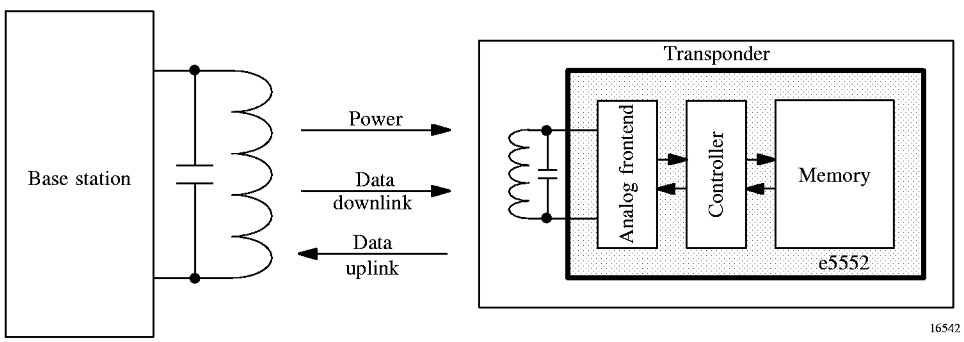


Figure 1. Transponder system example using e5552

* IDIC stands for IDentification Integrated Circuit and is a trademark of TEMIC Semiconductors

Functional Modules

Analog Front End (AFE)

The analog front end (AFE) includes all circuits which are directly connected to the coil. It generates the IC's power supply and handles the bidirectional data communication with the basestation. It consists of the following blocks:

- Rectifier to generate a DC supply voltage from the AC coil voltage.
- ESD protection
- Clock extractor
- Switchable load between Clock-A/ Clock-B for data transmission from the IC to the reader electronics (uplink mode).
- Field gap detector for data transmission from the base station to the IC (downlink mode).

Controller

The control logic is responsible for the following:

- Initializing and refresh configuration register from EEPROM block 0.
- Controlling read and write memory accesses.
- Handling data transmission and opcode decoding.
- Error detection and error handling.

Clock Extraction

The clock extraction circuit generates the internal clock source out of the external RF signal.

Data Rate Generator

The data rate in uplink mode can be selected to operate at either RF/16 (nominally 7.81 kHz, default) or RF/32 (nominally 3.91 kHz).

Bit Decoder

This function block decodes the field gaps and verifies the validity of the incoming data stream.

Charge Pump

This circuit generates the high voltage required for programming the EEPROM.

Power-On Reset (POR)

This circuit delays the IC's functionality until an acceptable voltage threshold has been reached.

Mode Register

This register holds the configuration data bits stored in EEPROM block 0. It is refreshed at the start of every block read operation.

Modulator

The modulator encodes the serial data stream shifted out of the selected EEPROM data block and controls the damping circuit in the AFE. The e5552 frontend supports PSK and Manchester encoding.

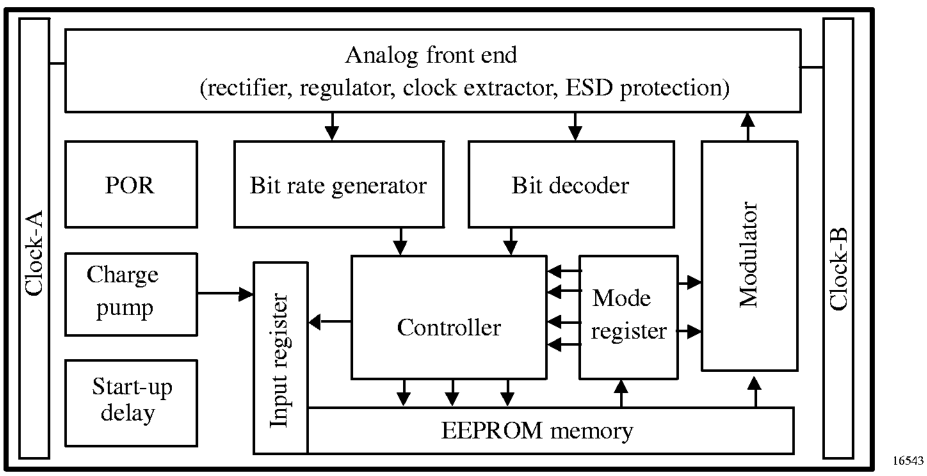


Figure 2. Functional block diagram

Operating the e5552

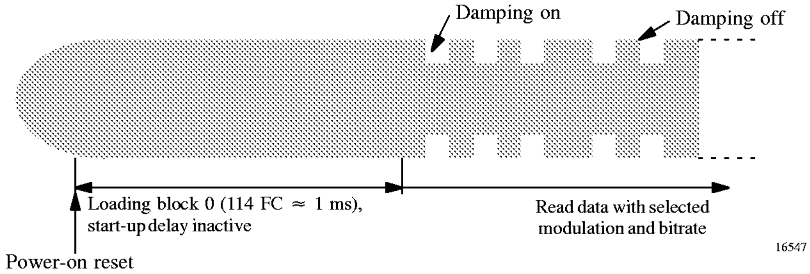


Figure 3. Voltage at Clock-A/ Clock-B after power on

General

The basic functions of the e5552 are to supply the IC from the RF field, read data out of the EEPROM and shift them to the modulator, receive data and program these data bits into the EEPROM. An error detecting circuit prevents the EEPROM from being written with wrong data.

Power Supply

The IC is supplied via a tuned LC circuit which is connected to the Clock-A/Clock-B pads. The incoming RF induces a current in the coil. The on-chip rectifier generates the DC supply voltage. Overvoltage protection prevents the IC from damage due to high field strengths. Depending on the coil, the open-circuit voltage across the LC circuit can reach more than 100 V.

Initialization

The occurrence of a RF field triggers a power–on reset pulse, ensuring a defined start-up. The Power-On-Reset circuit (POR) remains active until an adequate voltage threshold has been reached. This in turn triggers the default start-up delay sequence. During this period of 114 field clock cycles (FC) the e5552 is initialized with the configuration data stored in EEPROM block 0. This is followed by an additional delay time which is defined by the ”Start-up Delay” bit.

If the ”Start-up Delay” bit is set the e5552 remains inactive until 8192 RF clock cycles have occured. If this option is deactivated, no delay is observed after the configuration period of 114 RF clock cycles (≈ 1 ms).

Any field gap occuring during initialization will restart the complete sequence.

$T_{INIT} = (114 + 8{,}192{*}\text{delay bit})/125\text{ kHz} \approx 65\text{ ms}$

After this initialization time the e5552 enters uplink mode and modulation starts automatically using the parameters defined in the configuration block.

Uplink Operation

All transmissions from the IC to the base station utilizes amplitude modulation (ASK) of the RF carrier. This takes place by switching a resistive load between the coil pads (Clock-A and Clock-B) which in turn modulates the RF field generated by the base station (reflective backscatter modulation).

MaxBlock

Data from the memory is serially transmitted, starting with block 1, bit 1, up to the last block (MAXBLK), bit 32. The last block which will be transmitted is defined by the mode parameter field MAXBLK is stored in EEPROM block 0. When the MAXBLK address has been reached, data transmission restarts with block 1.

The user defines the cyclic datastream by setting the MAXBLK between 0 and 31 (representing each of the 32 data blocks). If set to 1, only block 1 is transmitted. If set to 31, blocks 1 to 31 will be sequentially transmitted. If set to 0, only the contents of the configuration block (normally not accessible) will be transmitted (see figure 4).

On the other hand it is also possible to access a single data block selectively, independant of the MAXBLK value, with the direct access command (Opcode ‘11’). The thus addressed data block is transmitted repeatedly.

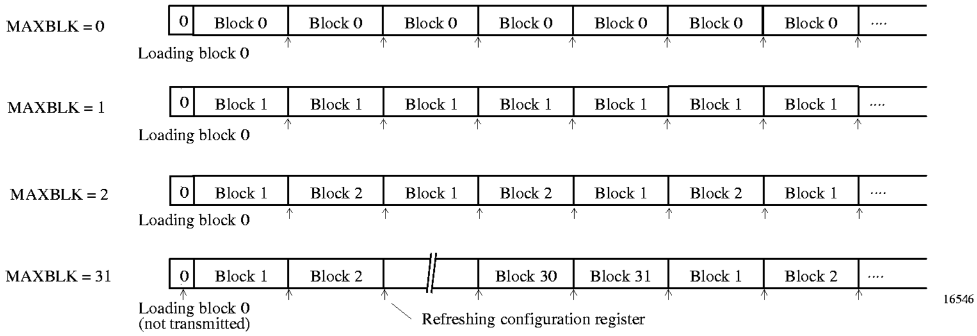


Figure 4. Datastream pattern depending on MAXBLK

Data Encoding

Everytime when entering uplink mode, the data stream is preceeded by a single start bit (always '0'). Then the data stream continues with block 1, bit 1, and continues through MAXBLK, bit 32. This data stream pattern cycles continuously.

The modulator is configurable for

- MANCHESTER

Manchester encoded data represent a logical '1' with a rising edge and a logical '0' with a falling edge.

- PSK using sub-carrier frequency RF/2

The PSK modulator changes phase with each change of data. The first phase shift represents a data change from '0' —> '1'.

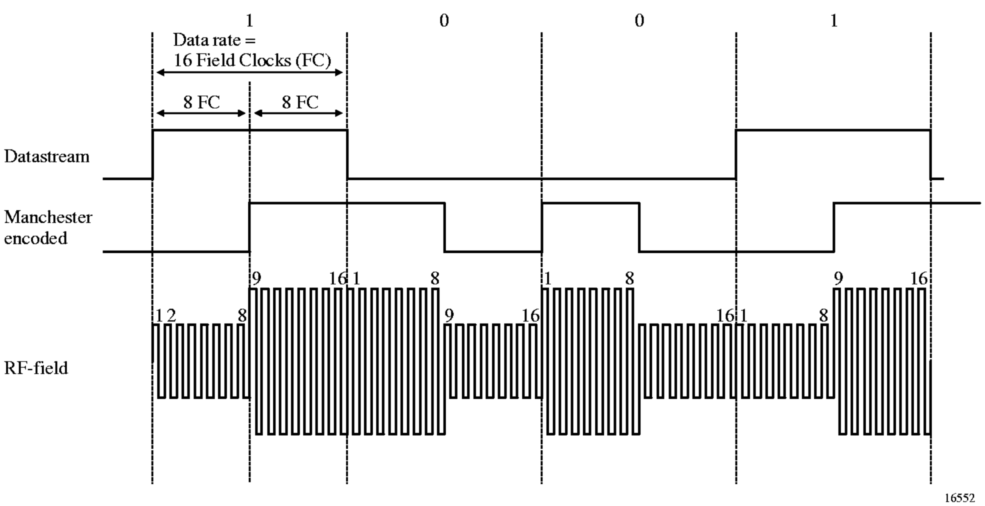


Figure 5. Example of Manchester encoding with data rate RF/16

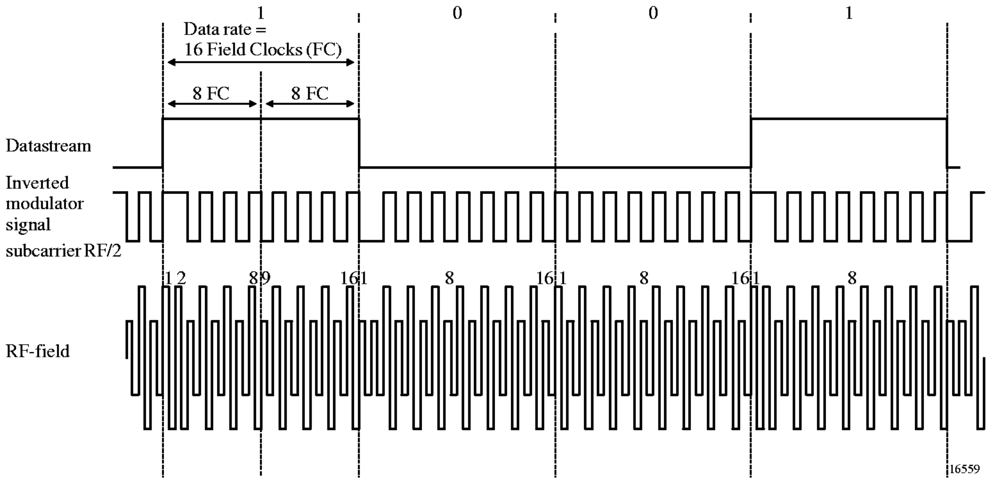


Figure 6. Example of PSK encoding with data rate RF/16

Downlink Operation

Data is transmitted from the base station by amplitude modulation of the field (m = 1) using a series of so called gaps. With the exception of the initial synchronisation gap (start gap), all field gaps have the same duration, the logical data being encoded in the length of the unmodulated phases (see figure 7)

A valid data stream is always preceeded by a start gap which is approximately twice as long as a normal field gap. Detection of this first gap causes the e5552 to switch immediately into the downlink mode where it can receive and decode the following data stream. This stream consists of two opcode bits, followed by (0, 3 or 5) address bits and finally (0 or 33) data bits (including the lock bit). In downlink mode the transponder damping is permanently enabled. This loads the resonant transponder coil circuit so that it comes quickly to rest when field gaps occur – thus allowing fast gap detection.

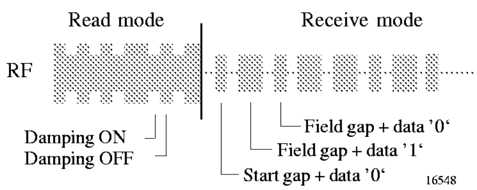


Figure 7. Entering the downlink mode

A start gap will be accepted at any time after start–up initialization has been finished (RF field ON plus ≈ 1 ms, startup delay inactive) and the IC is not in downlink operation.

Downlink Data Coding

The duration of a field gap is typically between 80 and 250 µs. After the start gap the data bits are transmitted by the base station whereby each bit is separated by a field gap. The bit decoder interprets 16 to 32 internal field clocks as a logical '0' and 48 to 64 internal field clocks as a logical '1' (see figure 8). Therefore the time between two gaps is typically 24 field clocks for a '0' and 56 field clocks for a '1'.

Whenever the bit decoder detects more than 64 field clocks, the e5552 will abort the downlink mode. The incoming data stream is checked continuously and should an error be detected the corresponding error handling is initiated.

The control logic initiates an EEPROM programming cycle if the correct number of bits had been received (see figure 9).

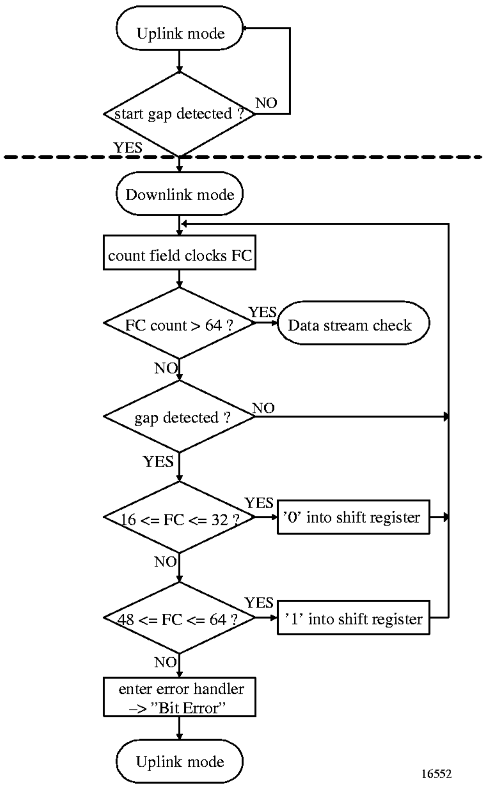


Figure 8. Operation of bit decoder – data stream decoder

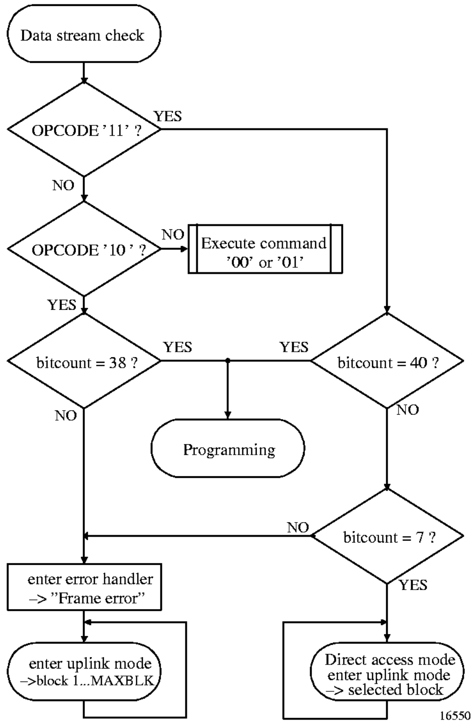


Figure 9. Data stream checking

Opcode definitions

The first two bits of the data stream are decoded by the controller as the opcode bits (see figure 10):

'11': Opcode for a 5-bit address data stream

- To initiate a standard block write cycle the 2 opcode bits are followed by the lock bit, the 32 data bits and the 5-bit block address (40 bits total).
- The direct access command consists of the opcode '11' followed by the 5-bit block address and is a read–only command (7 bits total).

'10': Opcode for a 3-bit address data stream

- e5550 receive mode compatible
  To initiate a block write cycle, the opcode '10' is followed by the lock bit, the 32 data bits and the 3-bit block address (38 bits total).

'01': reserved for production test commands.

'00': Opcode for an internal reset command.

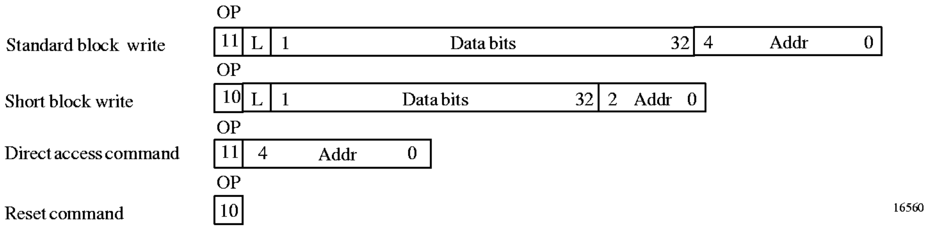


Figure 10. e5552 opcode format definition

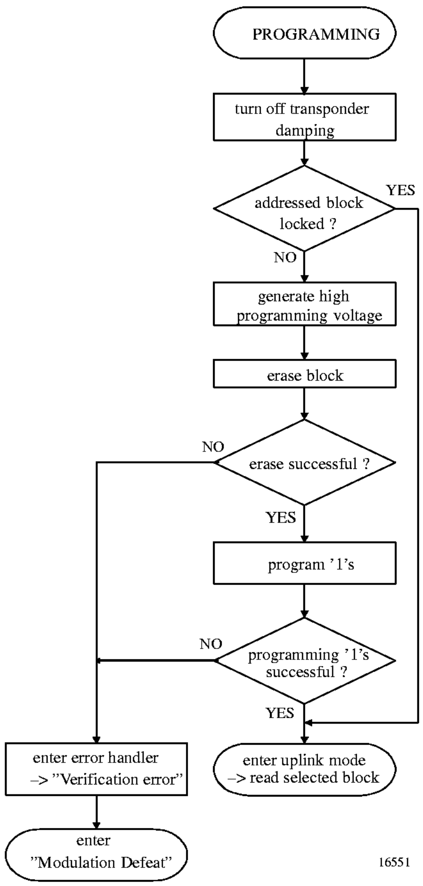


Figure 11. Programming cycle flow chart

Programming

If the bit decoder and controller detect a valid data stream, the e5552 will start an erase and programming cycle if a data write command was decoded (see figure 11).

During the erase and programming cycle downlink damping is turned off. The programming cycle includes a data verification read to check the integrity of the data. After EEPROM programming and verification has been finished successfully, the e5552 enters uplink mode transmitting the block just programmed.

The typical programming time is ≈ 18 ms.

Error Handling

Several error conditions are detected by the e5552 to ensure that only valid information is programmed into the EEPROM.

Errors During EEPROM Programming

There are two error types which will lead to different actions.

- Verification error

  If one of the data verification cycles fails, the e5552 will inhibit modulation and not return to the uplink mode. This "modulation defeat" state is terminated by re-entering the downlink mode with a start gap.

- Block write protection

  If the lock bit of the addressed block is set, programming is disabled. In this case, the programming cycle is not initiated and the e5552 reverts to uplink mode, transmitting the currently addressed (and unmodified) block continuously.

Errors During Data Transmission

The following errors are detected by the decoder:

- Bit error

  Wrong number of field clocks between two gaps (i.e. not a valid ‘0’ or ‘1’ pulse stream).

- Frame error

  The number of data bits received is incorrect:

  – valid bit count for 3-bit address write is 38 bits

  – valid bit count for 5-bit address write is 40 bits or

  – 7 bits for a direct access command.

If any of these conditions is detected, the e5552 enters uplink mode starting with block 1.

EEPROM Memory Organisation

The memory array of the e5552 consists of 1,056 bits of EEPROM, arranged in 32 individually addressable blocks of 33 bits each, consisting of one lock bit and 32 data bits. All 33 bits, including the lock bit, are programmed simultaneously.

The programming voltage is generated on-chip.

Lock bit

Each block has an associated write lock bit with which the entire block can be protected. By default all lock bits **L** are reset (‘0’).

Note: Once set, the lock bit – and the content of the associated block – cannot be altered.

Memory Map

The configuration data of the e5552 is stored in block 0 of the EEPROM.

The remaining thirty-one data blocks (1 .. 31) each consist of one lock bit and 32 user data bits.

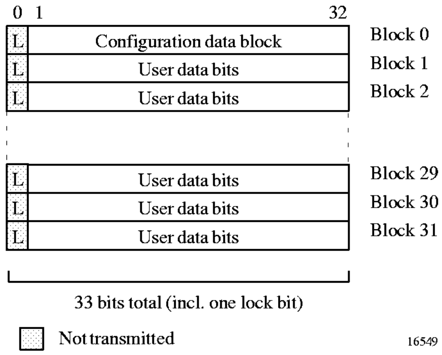


Figure 12. Memory map

Configuration Data Block

This data block contains 9 configuration bits.

The remaining bits of block 0 are reserved for future enhancements and should be set to ‘0’.

- Start-up Delay bit (SD, default: NO delay)
  When set, an additional delay time of 64 ms is added after any internal reset.
- Data Rate bit (DR, default: RF/16)
  Selects data rate of RF/16 or RF/32.
- Modulation Select bit (MS, default is PSK)
  Selects type of data encoding which is either MANCHESTER or PSK.
- Modulation Defeat bit (MD, default is OFF)
  When set (to ‘1’) the modulation output is deactivated, hence no data will be transmitted. The ”modulation defeat” state does not impact the transponder damping function.
- MAXBLK address
  This 5-bit block address is used to define the upper limit of cyclic block reads.

Note: The configuration is changed by re-programming block 0 as long as the corresponding lock bit is not set.

e5552 Configuration Block 0

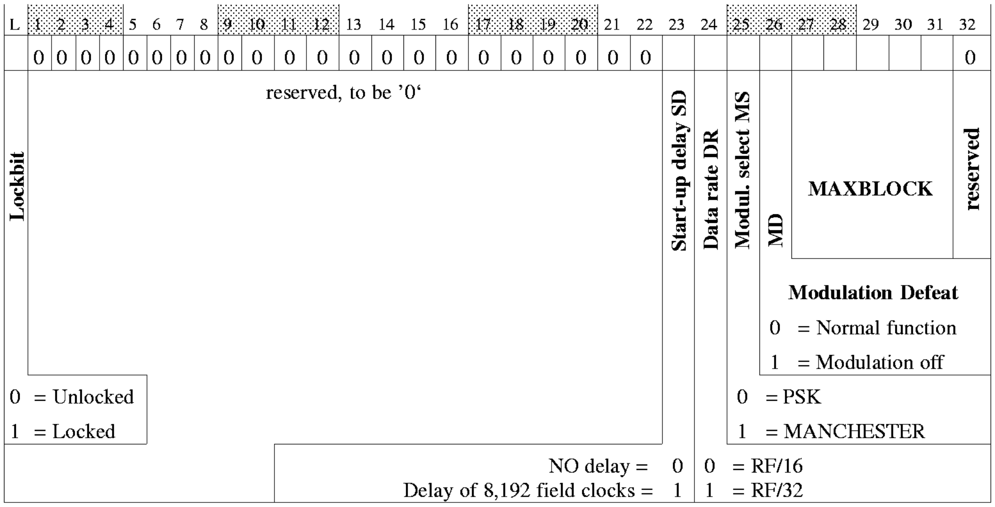


Figure 13. e5552 configuration block 0 bit mapping

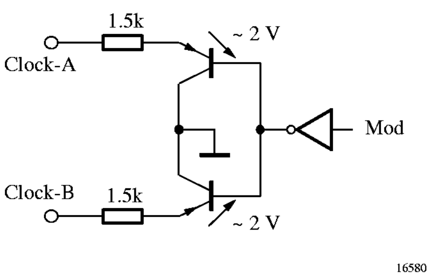


Figure 14. Simplified damping circuit

Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Maximum DC current into Clock-A/Clock-B	I_{coil}	10	mA
Maximum AC current into Clock-A/Clock-B, f = 125 kHz	$I_{coil\,PP}$	20	mA
Power dissipation (dice) 1)	P_{tot}	100	mW
Electrostatic discharge voltage according to MIL-Standard 883D method 3015 (HBM)	V_{max}	8000	V
Operation ambient temperature range	T_{amb}	–40 to +85	°C
Storage temperature range 2)	T_{stg}	–40 to +125	°C
Maximum assembly temperature for less than 5 min 3)	T_{sld}	+150	°C

Notes: 1) Free–air condition, time of application: 1s
2) Data retention reduced
3) Assembly temperature of 150 °C for less then 5 minutes does not affect the data retention

Stresses above those listed under ”Absolute Maximum Ratings” may cause permanent damage to the device.

Operating Charateristics

T_{amb} = 25°C; f_{RF} = 125 kHz reference terminal is V_{SS}

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
RF frequency range		f_{RF}	100	125	150	kHz
Supply current	Uplink & downlink mode – full temperature range	I_{DD}		5	7.5	µA
	Programming – full temperature range	I_{DD}		14	28	µA
Clamp voltage	10 mA current into Clock-A/B	V_{clamp}	7		11	V
Programming time	Per block	t_P		18		ms
Startup time	2)	$t_{startup}$	1		65	ms
Data retention	1)	$t_{retention}$	20			Years
Programming cycles	1)	n_{cycles}	100,000			
Clock-A/B voltage	Uplink & downlink mode	$V_{clockPP}$	6			V
Clock-A/B voltage	Programming, RF field w/o damping	$V_{clockPP}$	12			V
Damping resistor	Each at Clock-A and Clock-B	R_D		1.5		kΩ

Note: 1) Since EEPROM performance is influenced by assembly and packaging, TEMIC Semiconductors confirm the parameters for DOW (= tested dice on wafer) and ICs assembled in standard package.

2) Depends on start-up delay bit in configuration register

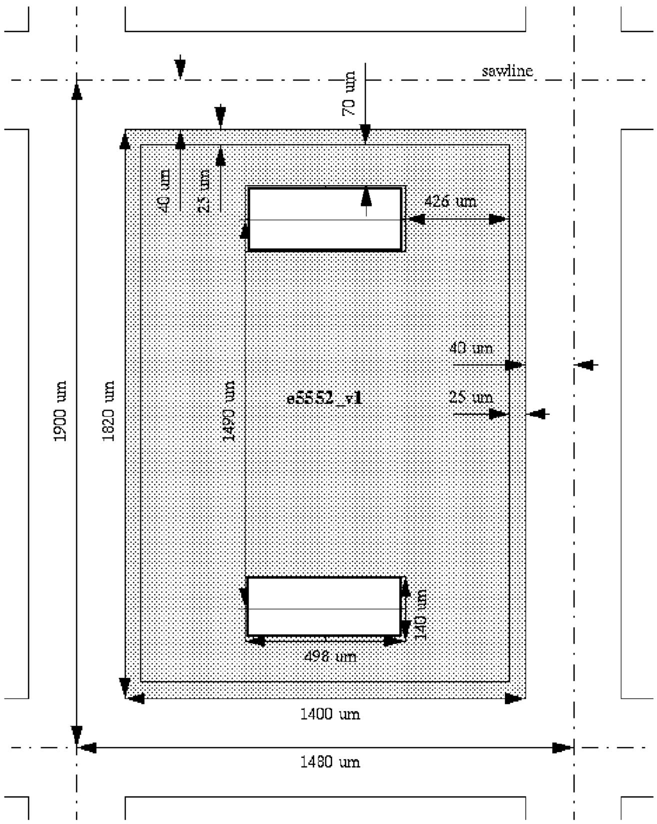
Die Pad Layout

The Clock-A and Clock-B terminals have been geometrically optimized for high volume, mass production flipchip die attach processes. The large pads are located on each extreme end of the longer dimension of the IC. With exception to the pad terminals, all remaining surface area is passivated.

The IC has a rectangular aspect ratio of roughly 1:1.3.

Dimensions

Name	Dimension	Function
e5552	1.48mm x 1.90mm (58 mils x 75 mils)	Overall footprint
Clock-A	0.14mm x .498mm (5.5 mils x 19.6 mils)	Antenna/Coil Connection Pad
Clock-B	0.14mm x .498mm (5.5 mils x 19.6 mils)	Antenna/Coil Connection pad
Clock-A/B pitch	1.49 mm (58.6 mils)	Clock-A to Clock-B pitch



Ozone Depleting Substances Policy Statement

It is the policy of **TEMIC Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

TEMIC Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

TEMIC Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

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