



## Low Power, High Performance CMOS Gate Array and ROM Combo

### Features

- 64K ROM: 8192 words x 8 bits
- 2880 available gates, 2000 usable gates
- 3V or 5V operating supply
- 90ns access time from Address
- Auto low power standby mode in ROM
- Typical gate delay = 300ps, fanout = 2
- Programmable ROM Enable active level
- Output buffers programmable, from 2mA to 24mA
- Low Power ROM: 2mA Operating, 50  $\mu$ A Standby
- Input levels selectable, CMOS, TTL, ECL, hysteresis, Analog Comparator
- 74 pads; each can be assigned as power, GND, Input, Output, or I/O
- Latch-Up immunity on all pins
- Class 3 (4000V) ESD Protection
- Wide range of packaging options  
Plastic or Ceramic DIP  
PQFP and TQFP  
PLCC, TSOP

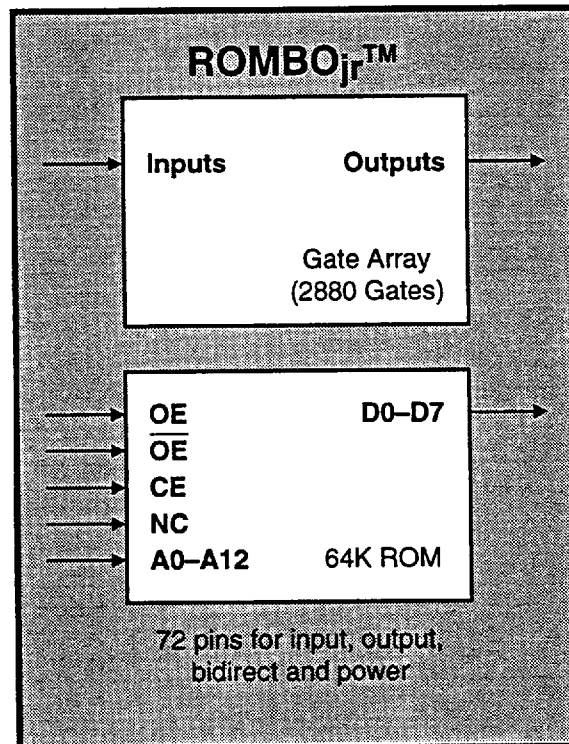


Figure 1. ROMBO Block Diagram

**Absolute Maximum Ratings:** Voltages with respect to ground ( $V_{SS}$ ) unless otherwise noted.

Parameter	Symbol	Min.	Max.	Units
Supply Voltage	$V_{DD}$		7.0	V
Input Voltage	$V_I$	-0.5	$V_{DD} + 0.5$	V
Output Voltage	$V_O$	-0.5	$V_{DD} + 0.5$	V
Operating Temperature	$T_{OP}$	0°	85°	C
Storage temperature	$T_{STG}$	-25°	125°	C

**NOTE:** Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Functional operation should be restricted to the conditions described under Recommended Operating Conditions.

**Recommended Operating Conditions:** Voltages with respect to ground ( $V_{SS}$ ) unless otherwise noted.

Characteristics	Symbol	Test Conditions	Min.	Max.	Units
Supply Voltage	$V_{DD}$		4.75	5.25	V
Supply current (static) <sup>(1, 2)</sup>	$I_{DD1}$	No D.C. loads on pads		50	$\mu$ A
Supply current (static) <sup>(1, 3)</sup>	$I_{DD2}$	No D.C. loads on pads		2	mA
Ambient Temperature	$T_A$		0°	70°	C

**NOTE 1:** All other inputs are connected to  $V_{DD}$  or  $V_{SS}$  while measuring  $I_{DD}$ .

**NOTE 2:**  $I_{DD1}$  is measured with the internal ROM inactive.

**NOTE 3:**  $I_{DD2}$  is measured with the internal ROM inactive, CS, OE, and CE in active state.

**DC Characteristics:** Voltages with respect to ground ( $V_{SS}$ ) unless otherwise noted.  
Specified at  $V_{DD} = 5V \pm 5\%$ , ambient temperature 0 to 70°C.

Input Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Units
Input voltage range	$V_{IN}$		$V_{SS}-0.5$		$V_{DD}+0.5$	V
Hysteresis, High Threshold	$V_{T+}$		2.35		2.90	V
Hysteresis, Low Threshold	$V_{T-}$		1.85		2.45	V
Hysteresis, $V_{T+} - V_{T-}$	$DV_T$		0.35	0.50	0.60	V
TTL, Input high	$V_{IH}$		2.0			V
TTL, Input low	$V_{IL}$				0.8	V
ECL, Diff. input range	$V_{IDR}$		350			mV
ECL, Common mode range	$V_{ICR}$		2.5		$V_{DD}-1.0$	V
CMOS, Input high	$V_{IH}$		3.5			V
CMOS, Input low	$V_{IL}$				1.5	V
Comparator Input Common Mode	$V_{ICR}$		1.0		$V_{DD}-1.5$	V
Comparator input offset	VOS				10	mV
Comparator gain	AV			750		V/V
Pull down current	$I_{ID}$	$V_{IN} = V_{DD}$	3	12	50	$\mu A$
Pull up current	$I_{IU}$	$V_{IN} = V_{SS}$	-50	-12	-3	$\mu A$
Input leakage	$I_{IL}$	$V_{IN} = V_{DD}$ to $V_{SS}$	-10		+10	$\mu A$
Output Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS Output Low	$V_{OL}$	$I_{OL} = 2.0$ to 24 mA			0.4	V
CMOS Output High	$V_{OH}$	$I_{OH} = -2.0$ to 24 mA	$V_{DD}-1.0$			V
TTL Output Low	$V_{OL}$	$I_{OL} = 2.0$ to 24 mA			0.4	V
TTL Output High	$V_{OH}$	$I_{OL} = -2.0$ to -24 mA	2.4			V
Leakage current (no pullup-down)	$I_{IL}$	$V_{IN} = V_{DD}$ to $V_{SS}$	-10		10	$\mu A$

**AC Electrical Characteristics:** Voltages with respect to ground ( $V_{SS}$ ) unless otherwise stated, also see timing diagram.

Timing Parameter	Definition	Min.	Typ.	Max.	Units
$t_{ACE}$	Chip enable access time, from $\overline{CE}$		100		nsec
$t_{AA}$	Address access time		90		nsec
$t_{HZ}$	Output high Z delay from $\overline{CE}$			40	nsec
$t_{LZ}$	Output Low Z delay from $\overline{CE}$	5			nsec
$t_{PU}$	Power up Time from $\overline{CE}$	0			nsec
$t_{PD}$	Power down time from $\overline{CE}$			40	nsec

NOTE 1: Load capacitance on all outputs is assumed to be 50pf, unless otherwise specified.

NOTE 2: Rise and fall times of all inputs are assumed to be 5ns or less.

## Timing Diagram

