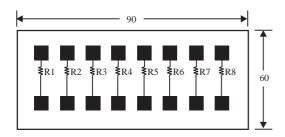
CALIFORNIA MICRO DEVICES ▶▶▶▶

ISOLATED RESISTOR NETWORK

California Micro Devices' resistor arrays are the hybrid equivalent to the isolated resistor networks available in surface mount packages. The resistors are spaced on ten mil centers resulting in reduced real estate. These chips are manufactured using advanced thin film processing techniques and are 100% electrically tested and visually inspected.

ELECTRICAL SPECIFICATIONS						
Parameter	Test Condition					
TCR	-55°C to +125°	±100ppm/°C	Max			
Operating Voltage	-55°C to +125°	50Vdc	Max			
Power Rating (per resistor)	@ 70°C (Derate linearly to zero @ 150°C)	50mw	Max			
Thermal Shock	Method 107 MIL-STD-202F	±0.25%@ΔR	Max			
High Temperature Exposure	100 Hrs @ 150°C Ambient	±0.25%∆R	Max			
Moisture Resistance	Method 106 MIL-STD-202F	±0.5%ΔR	Max			
Life	Method 108 MIL-STD-202F (125°C/1000hr)	±0.5%ΔR	Max			
Noise	Method 308 MIL-STD-202F	-35 dB	Max			
	≥250kΩ	-30 dB	Max			
Short Time Overload	MIL-R-83401	0.25%	Max			
Insulation Resistance	@25°C	1 X 10 ¹² Ω	Min			



Formats

Die Size: $90\pm3 \times 60\pm3$ mils Bonding Pads: 5x7 mils typical

VALUES

8 resistors from 100Ω to 346Ω

MECHANICAL SPECIFICATIONS				
Substrate	Silicon 10±2 mils thick			
Isolation Layer	SiO2 10,000Å thick, min			
Backing	Lapped (gold optional)			
Metalization	Aluminum 10,000Å thick, min			
	(15,000Å gold optional)			
Passivation	Silicon nitride			

PACKAGING

Two inch square trays of 196 chips maximum.

NOTES

1. Resistor pattern may vary from one value to another.

	PART NUMBER DESIGNATION N							
CC	5003	F	Α	G	W	Р		
Series	Value First 3 digits are significant value. Last digit represents number of zeroes. R indicates decimal point.	Tolerance $D = \pm 0.5\%$ $F = \pm 1\%$ $G = \pm 2\%$ $J = \pm 5\%$ $K = \pm 10\%$ $M = \pm 20\%$	TCR No Letter = ± 100 ppm A = $\pm 50\%$ B = $\pm 25\%$	Bond Pads G = Gold No Letter=Aluminum	Backing W = Gold L = Lapped No Letter=Either	Ratio Tolerance No Letter=±1% P = ±0.5%		