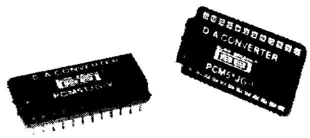
BURR-BROWN®

PCM51JG
DESIGNED FOR AUDIO



039092

16-Bit DIGITAL-TO-ANALOG CONVERTER

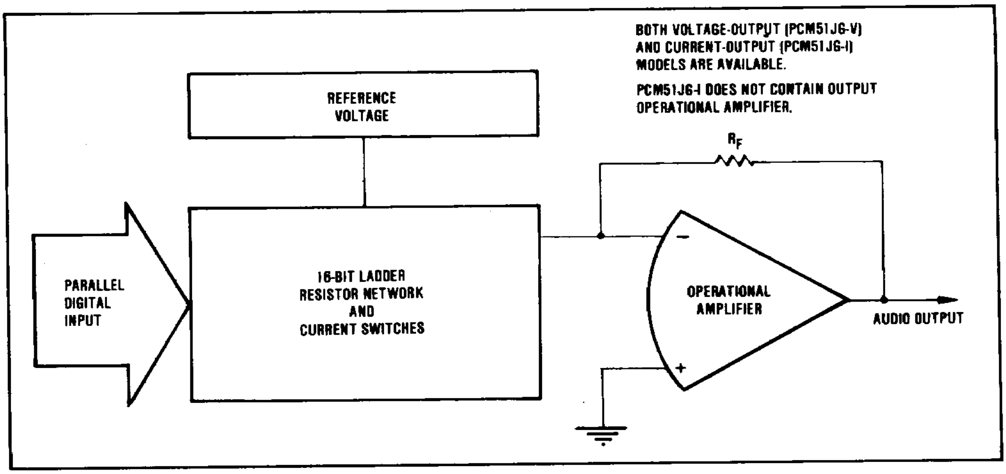
FEATURES

- 16-BIT RESOLUTION
- 350nsec SETTLING TIME, typ (I Model)
- 5μsec SETTLING TIME, typ (V Model)
- 0.006% OF FSR MAX DIFFERENTIAL LINEARITY ERROR (0.0025% typ)
- 0.0025% THD (FS Input, 16 Bits), typ
- 0.012% THD (-15dB, 16 Bits), typ
- 96dB DYNAMIC RANGE
- EIAJ STC-007 COMPATIBLE
- PIN COMPATIBLE - DAC71 & PCM50
- LOW COST

DESCRIPTION

The PCM51 is designed for PCM audio applications and is compatible with EIAJ STC-007 specifications. The PCM51 may be operated as either a 16-bit or a 14-bit converter. It features wide dynamic range, low differential linearity error, low distortion, and has a very-fast settling time.

The PCM51 contains an internal voltage reference. It uses state-of-the-art IC and laser-trimmed thin-film components. The converter combines high quality and high performance with low cost.



International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

T_A = +25°C and rated power supplies unless otherwise noted.

MODEL	PCM51JG MIN	PCM51JG TYP	PCM51JG MAX	UNITS
INPUT				
DIGITAL INPUT				
Resolution		16		Bits
Dynamic Range		96		dB
Logic Levels (TTL-Compatible)(1)				
Logic "1" at +40μA	+2.4		+5.5	VDC
Logic "0" at -1.6mA	0		+0.4	VDC
TRANSFER CHARACTERISTICS				
Gain Error		±0.1	±0.5	%
Bipolar Zero Error(2)		±10	±100	mV
Differential Linearity Error at Bipolar Zero		0.0025	0.006	% of FSR(3)
TOTAL HARMONIC DISTORTION(4)				
V_O = ±FS at f = 400Hz				
14-Bit Resolution		0.004		%
16-Bit Resolution		0.0025	0.005	%
V_O = -15dB at f = 400Hz				
14-Bit Resolution		0.023	0.06	%
16-Bit Resolution		0.012	0.04	%
V_O = -20dB at f = 400Hz				
14-Bit Resolution		0.04		%
16-Bit Resolution		0.025		%
V_O = -60dB at f = 400Hz				
14-Bit Resolution		4.2		%
16-Bit Resolution		1.9		%
DRIFT (Over Specified Temperature Range)				
Total Bipolar Drift (includes gain, offset, and linearity drift)		±25	±50	ppm of FSR/°C
SETTLING TIME (To ±0.006% of FSR)				
Voltage Model, PCM51JG-V				
Output: 20V Step		5		μsec
1LSB Step(5)		3		μsec
Slew Rate		20		V/μsec
Current Model, PCM51JG-I				
Output: 1mA Step				
10Ω to 100Ω load		350		nsec
1kΩ Load(6)		350		nsec
WARM-UP TIME	1			Min
OUTPUT				
ANALOG OUTPUT				
Voltage Model, PCM51JG-V				
Ranges		±10		V
		±5(7)		V
Output Current		±5		mA
Output Impedance (DC)		0.1		Ω
Short-Circuit Duration		Indefinite To Common		
Current Model, PCM51JG-I				
Range		±1		mA
Output Impedance		3		kΩ
POWER SUPPLY				
SENSITIVITY				
-15VDC		±0.02		% of FSR/% Vs
+15VDC		±0.002		% of FSR/% Vs
POWER SUPPLY REQUIRMENTS				
Voltage, Vs	±14.5	±15	±15.5	VDC
Supply Drain, +15VDC (no load)		±25		mA
-15VDC		-40		mA
TEMPERATURE RANGE				
Specification	0		+70	°C
Operating (derated specs)	-25		+85	°C
Storage	-55		+85	°C

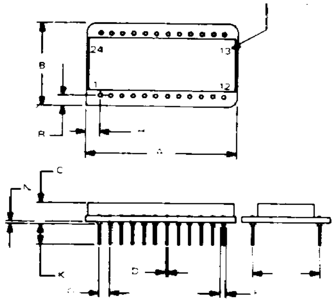
NOTES:

1. Adding external CMOS hex buffers CD4009A will provide 15VDC CMOS input compatibility. The percent change in output (V_O) as logic 0 varies from 0.0V to +0.4V and logic 1 changes from +2.4V to +5.0V on all inputs is less than 0.006% of FSR.
2. Adjustable to zero with external trim potentiometer.
3. FSR means Full Scale Range and is 20V for ±10V range and 10V for ±5V range.
4. The measurement of total harmonic distortion is highly dependent on the characteristics of the measurement circuit. A block diagram of a measurement circuit is shown in Figure 3. Burr-Brown calculates THD from the measured linearity errors using equation (2) in the section on "Total Harmonic Distortion", and specifies that the maximum THD measured with the circuit shown in Figure 3 will be less than the limits indicated.
5. LSB is for 14-bit resolution.
6. Measured with an active clamp, as shown in Figure 10, to provide a low impedance for approximately 200nsec.
7. Connect pin 24 to pin 17 to obtain ±5V range.

MECHANICAL

NOTE: Leads in true position. Within 0.10" (0.25mm) R at MMC at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.



CASE: Black Ceramic

MATING CONNECTOR: 245MC

WEIGHT: 8.4 grams (0.3 oz.)

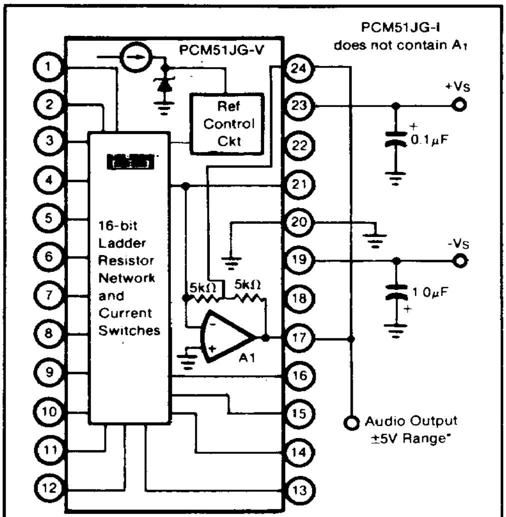
HERMETICITY: Conforms to method 1014 condition C step 1 fluorocarbon of MIL-STD-883 gross leak.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1 310	1 360	33 27	34 54
B	770	810	19 56	20 57
C	150	210	3 81	5 33
D	018	021	0 46	0 53
F	035	050	0 89	1 27
G	100 BASIC		2 54 BASIC	
H	110	130	2 79	3 30
K	150	250	3 81	6 35
L	600 BASIC		15 24 BASIC	
N	002	010	0 05	0 25
R	085	105	2 16	2 67

#2

PCM51

CONNECTION DIAGRAM



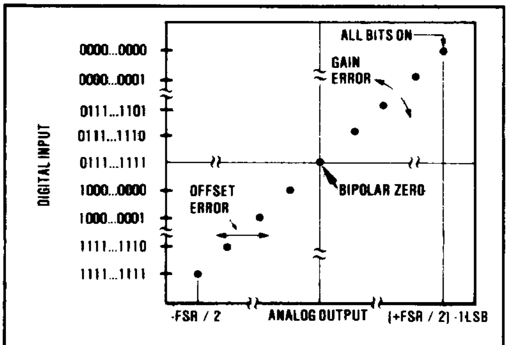
*Note: Leave Pin 24 open for ±10V Range.

PIN ASSIGNMENTS

Pin No.	PCM51JG-I	Pin No.	PCM51JG-V
1	Bit 1 (MSB)	1	Bit 1 (MSB)
2	Bit 2	2	Bit 2
3	Bit 3	3	Bit 3
4	Bit 4	4	Bit 4
5	Bit 5	5	Bit 5
6	Bit 6	6	Bit 6
7	Bit 7	7	Bit 7
8	Bit 8	8	Bit 8
9	Bit 9	9	Bit 9
10	Bit 10	10	Bit 10
11	Bit 11	11	Bit 11
12	Bit 12	12	Bit 12
13	Bit 13	13	Bit 13
14	Bit 14	14	Bit 14
15	Bit 15	15	Bit 15
16	Bit 16 (LSB)	16	Bit 16 (LSB)
17	±10V RANGE SELECT	17	AUDIO OUT
18	TEST POINT	18	TEST POINT
19	-15VDC	19	-15VDC
20	COMMON	20	COMMON
21	I_{OUT}	21	SUMMING JUNCTION
22	TEST POINT	22	TEST POINT
23	+15VDC	23	+15VDC
24	±5V RANGE SELECT	24	±5V RANGE SELECT

THEORY OF OPERATION

The accuracy of a D/A converter is described by the transfer function shown in Figure 1. The errors in the D/A converter are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity, and Power Supply Sensitivity. Initial Offset or Bipolar zero errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the minus full scale point (all bits Off), and Offset drift shifts the line left or right over the operating temperature range. Most of the offset and gain drift with temperature or time is due to the drift of the internal reference zener diode. The converter is designed so that these drifts are in opposite directions. This way the bipolar zero voltage is virtually unaffected by variations in the reference voltage. Total Harmonic Distortion (THD) is useful in audio applications and is a measure of the magnitude and distribution of the Linearity Error, Differential Linearity Error, and Noise, as well as Quantization Error. To be useful, THD should be specified for both high level and low level input signals. This error is unadjustable and is the most meaningful indicator of D/A converter accuracy for audio applications. The resolution of a D/A converter can be expressed in terms of Dynamic Range. The Dynamic Range is a measure of the ratio of the smallest signals the converter can produce to the full scale range and is usually expressed in decibels (dB). The theoretical dynamic range of a converter is approximately 6 x n, where n is the number of bits of resolution, or 96dB for a 16-bit converter. The actual or useful dynamic range is limited by noise and linearity errors and is therefore somewhat less than the theoretical limit.



*SEE TABLE I FOR DIGITAL CODE DEFINITIONS.

FIGURE 1. Input vs Output for an Ideal Bipolar D/A Converter.

DIGITAL INPUT CODES

The PCM51 accepts complementary digital input codes in binary format. It may be connected by the user for

TABLE I. Digital Input Codes.

DIGITAL INPUT CODES			
		COB	CTC*
	MSB LSB	Complementary Offset Binary	Complementary Two's Complement
All bits ON	0000...000	+Full Scale	-1LSB
Mid Scale	0111...111	Zero	-Full Scale
All bits OFF	1111...111	-Full Scale	Zero
	1000...000	-1LSB	+Full Scale

*A TTL inverter must be connected between the MSB input signal and bit 1 (pin 1) to obtain CTC input code.

either complementary offset binary (COB) or complementary two's complement (CTC) codes. See Table I.

DISCUSSION OF SPECIFICATIONS

The PCM51 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for a D/A converter in audio applications are total harmonic distortion, differential linearity error, bipolar zero error, parameter shifts with time and temperature, and settling-time effects on accuracy. This DAC is factory-trimmed and tested for all critical key specifications.

BIPOLAR ZERO ERROR

Initial bipolar zero error (Bit 1 "ON" and all other bits "OFF") is factory-trimmed to typically ±10mV (±100mV maximum) at +25°C. This error may be trimmed to zero by connecting the external trim potentiometer shown in Figure 6.

DIFFERENTIAL LINEARITY ERROR

Differential Linearity Error (DLE) is the deviation from an ideal 1LSB change from one adjacent output state to the next. DLE is important in audio applications because excessive DLE at bipolar zero (at the "major carry") can result in audible crossover distortion for low level output signals. Initial DLE on the PCM51 is factory-trimmed to typically ±0.0025% of FSR (±0.006% of FSR, maximum).

STABILITY WITH TIME AND TEMPERATURE

The parameters of a D/A converter designed for audio applications should be stable over a relatively wide temperature range and over long periods of time to avoid undesirable periodic readjustment. The most important parameters are Bipolar Zero Error, Differential Linearity Error, and Total Harmonic Distortion. Most of the offset and gain drift with temperature or time is due to the drift of the internal reference zener diode. The PCM51 is designed so that these drifts are in opposite directions so that the bipolar zero voltage is virtually unaffected by variations in the reference voltage. Both DLE and THD are dependent upon the matching and tracking of resistor ratios and upon the matching and tracking of V_{BE} and h_{FE} of the current-source transistors. The PCM51 was designed so that any absolute shift in these components has virtually no effect on DLE or THD. The resistors are made of identical links of ultra-stable nichrome thin-film. The current density in these resistors is very-low to further enhance their stability.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect accuracy. The PCM51 power supply sensitivity is specified for ±0.02% of FSR/% V_S, for -15VDC supplies and ±0.002% of FSR/% V_S, for +15VDC supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with this DAC. See also Power Supply Connections paragraph in the Installation and Operating Instructions section.

SETTLING TIME (PCM51JG-V)

Settling time is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 2).

Settling times are specified to ±0.006% of FSR; one for maximum full scale range changes of 20V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst-case settling time occurs.

SETTLING TIME (PCM51JG-I)

Two settling times are specified to a ±0.006% of FSR. Each is given for current model connected with two different resistive loads: 10Ω to 200Ω and 1000Ω. Current-output model settling time is particularly important if the PCM51JG-I is going to be used to build a successive-approximation A/D converter. See Figure 11.

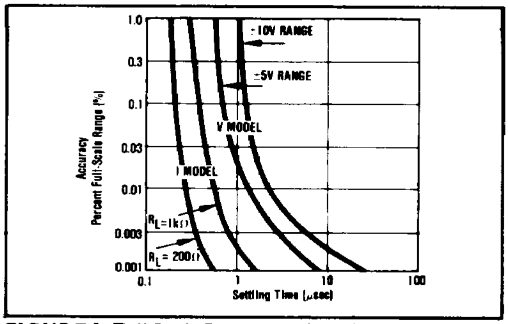


FIGURE 2. Full Scale Range Settling Time vs Accuracy.

TOTAL HARMONIC DISTORTION

The Total Harmonic Distortion (THD) is defined as the ratio of the square root of the sum of the squares of the value of the rms harmonics to the value of the rms fundamental and is expressed in percent or dB. A block diagram of the test circuit used to measure the THD of the PCM51 is shown in Figure 3. A timing diagram for the control logic is shown in Figure 4. The digital input code stored in the PROM as well as the output obtained from an ideal PCM51, the value of an ideal sine wave, and the inherent quantization error are given in Tables III and IV. If we assume that the error due to the test circuit is negligible, then the rms value of the PCM51 error referred to the input can be shown to be

$$\epsilon_{rms} = \sqrt{1/N \sum_{i=1}^{N} [E_L(i) + E_Q(i)]^2} \qquad (1)$$

where N is the number of samples, $E_L(i)$ is the linearity error of the PCM51 at each sampling point, and $E_Q(i)$ is the quantization error at each sampling point. The THD can then be expressed as

$$THD = \epsilon_{rms}/E_{rms} = \frac{\sqrt{1/N \sum_{i=1}^{N} [E_L(i) + E_Q(i)]^2}}{E_{rms}} \times 100\% \qquad (2)$$

This expression indicates that, in general, there is a correlation between the THD and the square root of the

PCM51

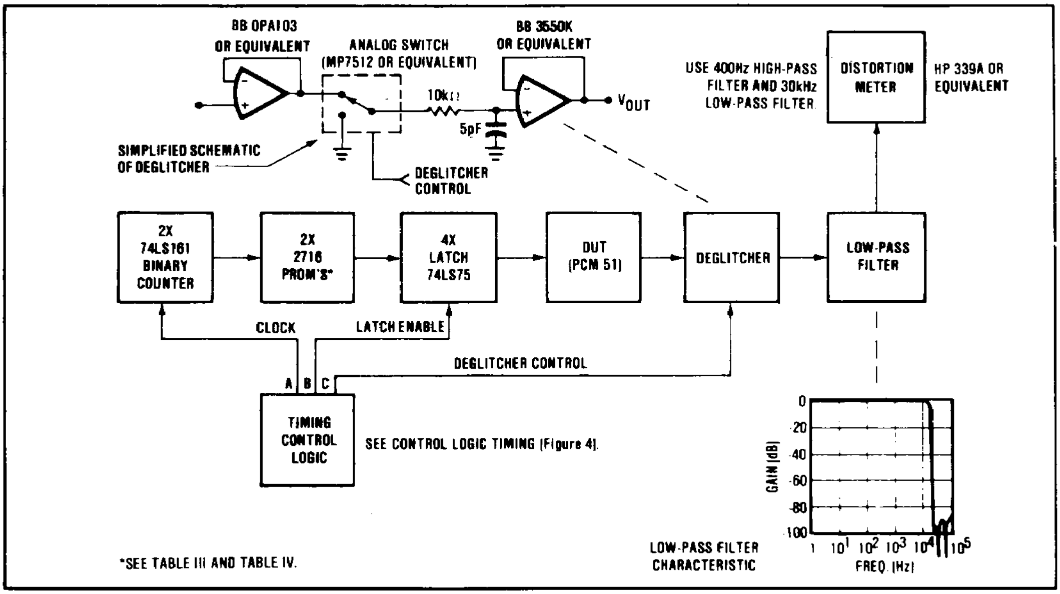


FIGURE 3. Block Diagram of Distortion Test Circuit.

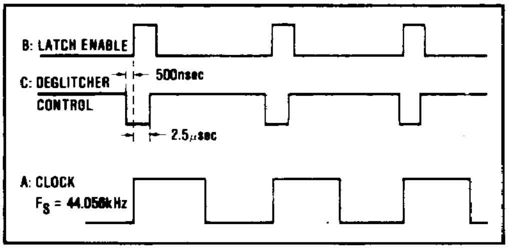


FIGURE 4. Control Logic Timing for PCM51 Distortion Test Circuit.

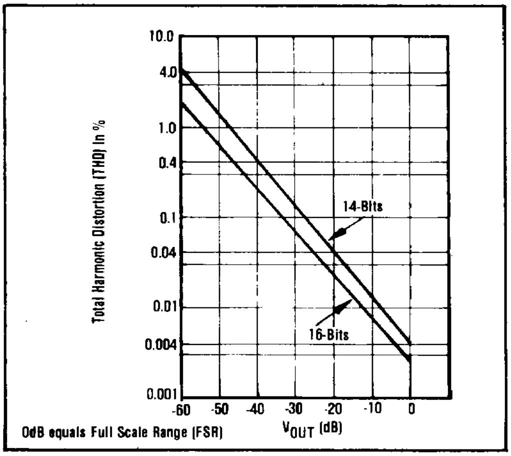


FIGURE 5. Total Harmonic Distortion (THD) vs V_{OUT}.

sum of the squares of the linearity errors at each digital word of interest. However, this expression does not mean that the worst-case linearity error of the D/A is directly correlated to the THD.

For the PCM51 the test period was chosen to be 22.7μsec (44.056kHz) which is compatible with the EIAJ STC-007 specification for PCM audio. The test frequency is 400Hz and the amplitude of the input signal is -15dB down from full scale.

Figure 5 shows the typical THD as a function of output voltage.

INSTALLATION AND OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the PCM51.

EXTERNAL BIPOLAR ZERO ADJUST (OPTIONAL)

In some applications the bipolar zero error may require adjustment. This error may be adjusted to zero by installing an external potentiometer as shown in Figure 6.

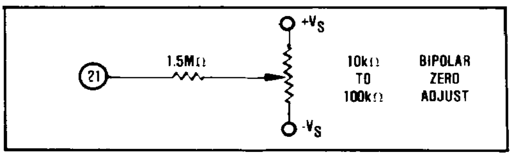


FIGURE 6. Optional External Bipolar Zero Adjust.

The TCR of the potentiometer should be 100ppm/°C or less. The 1.5MΩ resistor (20% carbon or better) should be located close to the PCM51 to prevent noise pickup. Refer to Figure 7 for the relationship of bipolar zero adjust on the D/A converter transfer function.

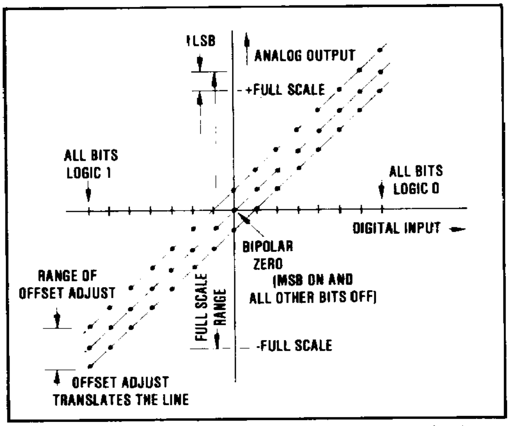


FIGURE 7. Affect of Offset Adjustment on a Bipolar D/A Converter Transfer Function.

ADJUSTMENT PROCEDURE

Apply the digital input code that should produce zero volts output (bit 1 or MSB "ON" and all other bits "OFF"). Adjust the offset potentiometer until zero volts is obtained.

Table II shows the ideal plus and minus full scale voltages and LSB values for both 14- and 16-bit resolution and ±10V, ±5V, and ±1mA output ranges.

TABLE II. Digital Input and Analog Output Relationships.

DIGITAL INPUT CODE	OUTPUT CODE: VOLTAGE, 16-Bit Resolution	VOLTAGE, 14-Bit Resolution	CURRENT, 16-Bit Resolution	CURRENT, 14-Bit Resolution
Complementary Bipolar Offset Binary COB				
±10V or ±1mA				
One LSB	+305μV	+1.22mV	0.031μA	0.122μA
All Bits On (00..00)	+9.99969V	+9.99878V	-0.99997mA	-0.99968mA
All Bits Off (11..11)	-10.0000V	-10.0000V	+1.0000mA	+1.0000mA
±5V or ±1mA				
One LSB	+152μV	+610μV	0.031μA	0.122μA
All Bits On (00..00)	+4.999848V	+4.99939V	-0.99997mA	-0.99968mA
All Bits Off (11..11)	-5.0000V	-5.0000V	+1.0000mA	+1.0000mA

*Connect pin 24 to pin 17 to obtain ±5V Range.

INSTALLATION CONSIDERATIONS

If 16-bit resolution is not required, bit 15 (pin 15) and bit 16 (pin 16) should be connected to +5VDC through a 1kΩ resistor.

Figure 8 shows the connection diagram for a PCM51. Lead and contact resistances are represented by R_1 through R_3. As long as the load resistance (R_L) is constant, R_1 simply introduces a gain error. R_2 is part of R_L if the output voltage is sensed at Common (pin 20) and therefore introduces no error. If R_L is variable, then R_1 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_1 should be less than 0.08Ω. R_L should be located as close as possible to the PCM51 for optimum performance.

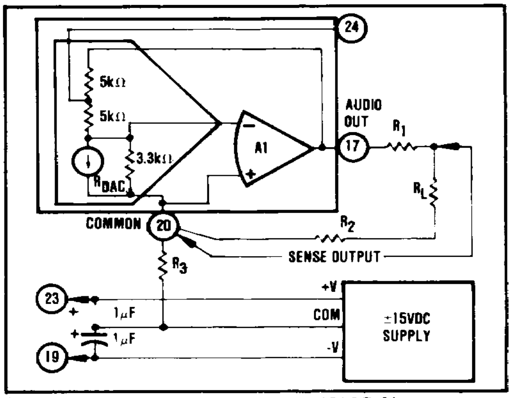


FIGURE 8. Output Circuit for PCM51JG-V.

The PCM51 and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key word in elimination of RF radiation or pickup is loop area; therefore, signal leads and their return conductors should be kept close together. This reduces the external magnetic field along with any radiation. Also, if a signal lead and its return conductor are wired close together they present a small flux-capture cross section for any external field. This reduces radiation pickup in the circuit.

See Figure 9 for the connection diagram of a PCM51JG-I current-to-voltage converter. R_1 through R_4 represent lead and contact resistances.

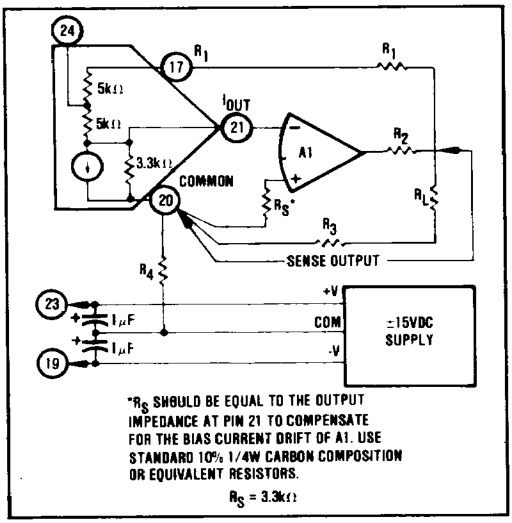


FIGURE 9. Preferred External Op Amp Configuration for PCM51JG-I

APPLICATIONS

A single PCM51 can be used for both the left and right channel as shown in Figure 10. Note that a Sample/Hold is not required.

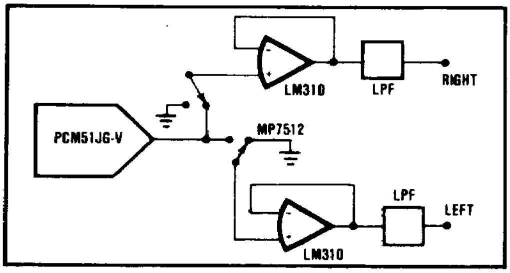


FIGURE 10. PCM51 Used for Stereo.

An A/D converter can be constructed using the PCM51JG-I shown in Figure 11.

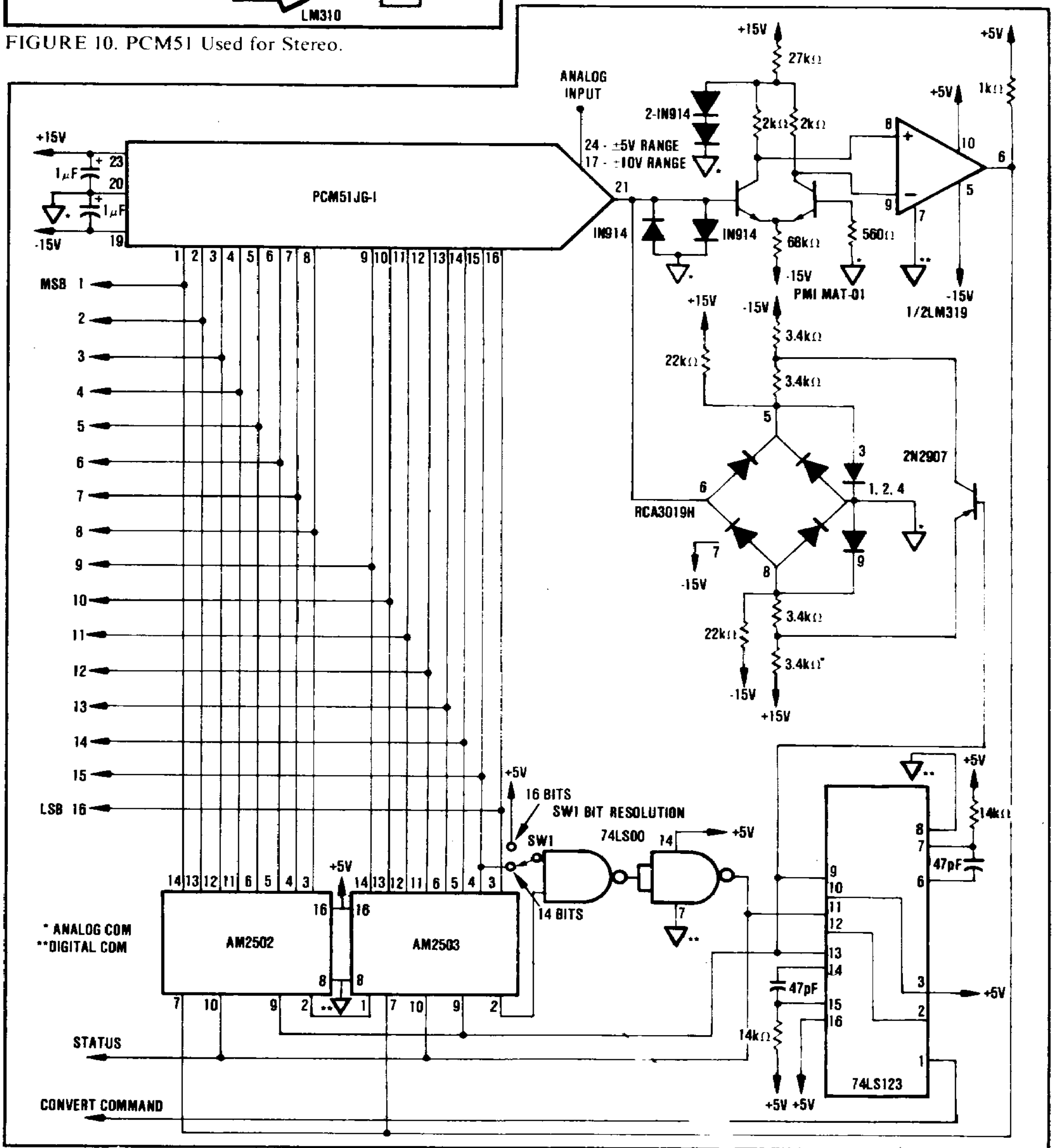


FIGURE 11. A/D Converter Using PCM51JG-I.

Table III shows the hex code loaded into the PROM's of the Distortion Test Circuit, Figure 3, for 14-bit values and Table IV shows the hex code for 16-bit values. Values are for a 400Hz sine wave (-15dB of full scale); all values are in volts.

TABLE III. Hex Code for 14-Bit Values (-15dB Output in 20V Full Scale Range).

CODE#	HEX CODE	IDEAL DAC OUT Volts	IDEAL SINE VALUE Volts	QUANTIZING ERROR Volts
1	7FFF	0.000000	0.000000	0.000000
2	7EB3	.101318	.101520	.000201
3	7D67	.202637	.202709	.000072
4	7C1F	.302734	.303236	.000502
5	7AD7	.402832	.402775	-.000057
6	7997	.500488	.500999	.000511
7	7857	.598145	.597590	-.000555
8	7723	.692139	.692231	.000092
9	75F3	.784912	.784614	-.000298
10	74CF	.874023	.874439	.000415
11	73AF	.961914	.961410	-.000504
12	729F	1.044922	1.045246	.000325
13	7197	1.125488	1.125673	.000185
14	709B	1.202393	1.202428	.000035
15	6FAB	1.275635	1.275261	-.000374
16	6ECB	1.343994	1.343934	-.000060
17	6DF7	1.408691	1.408223	-.000468
18	6D33	1.468506	1.467920	-.000586
19	6C7F	1.523438	1.522828	-.000610
20	6BDF	1.572266	1.572769	.000503
21	6B4B	1.617432	1.617580	.000148
22	6AC7	1.657715	1.657115	-.000600
23	6A5B	1.690674	1.691244	.000570
24	69FB	1.719971	1.719857	-.000113
25	69AF	1.743164	1.742861	-.000303
26	6977	1.760254	1.760179	-.000075
27	6953	1.771240	1.771756	.000516
28	693F	1.777344	1.777554	.000210
29	693F	1.777344	1.777554	.000210
30	6953	1.771240	1.771756	.000516
31	6977	1.760254	1.760179	-.000075
32	69AF	1.743164	1.742861	-.000303
33	69FB	1.719971	1.719857	-.000113
34	6A5B	1.690674	1.691244	.000570
35	6AC7	1.657715	1.657115	-.000600
36	6B4B	1.617432	1.617580	.000148
37	6BDF	1.572266	1.572769	.000503
38	6C7F	1.523438	1.522828	-.000610
39	6D33	1.468506	1.467920	-.000586
40	6DF7	1.408691	1.408223	-.000468
41	6ECB	1.343994	1.343934	-.000060
42	6FAB	1.275635	1.275261	-.000374
43	709B	1.202393	1.202428	.000035
44	7197	1.125488	1.125673	.000185
45	729F	1.044922	1.045246	.000325
46	73AF	.961914	.961410	-.000504
47	74CF	.874023	.874439	.000415
48	75F3	.784912	.784614	-.000298
49	7723	.692139	.692231	.000092
50	7857	.598145	.597590	-.000555
51	7997	.500488	.500999	.000511
52	7AD7	.402832	.402775	-.000057
53	7C1F	.302734	.303236	.000502
54	7D67	.202637	.202709	.000072
55	7EB3	.101318	.101520	.000201
56	7FFF	0.000000	0.000000	0.000000
57	814B	-.101318	-.101520	-.000201
58	8297	-.202637	-.202709	-.000072
59	83DF	-.302734	-.303236	-.000502
60	8527	-.402832	-.402775	.000057
61	8667	-.500488	-.500999	-.000511
62	87A7	-.598145	-.597590	.000555
63	88DB	-.692139	-.692231	-.000092
64	8A0B	-.784912	-.784614	.000298
65	8B2F	-.874023	-.874439	-.000415
66	8C4F	-.961914	-.961410	.000504
67	8D5F	-1.044922	-1.045246	-.000325
68	8E67	-1.125488	-1.125673	-.000185
69	8F63	-1.202393	-1.202428	-.000035
70	9053	-1.275635	-1.275261	.000374
71	9133	-1.343994	-1.343934	.000060
72	9207	-1.408691	-1.408223	.000468
73	92CB	-1.468506	-1.467920	.000586
74	937F	-1.523438	-1.522828	.000610
75	941F	-1.572266	-1.572769	-.000503
76	94B3	-1.617432	-1.617580	-.000148
77	9537	-1.657715	-1.657115	.000600
78	95A3	-1.690674	-1.691244	-.000570
79	9603	-1.719971	-1.719857	.000113
80	964F	-1.743164	-1.742861	.000303
81	9687	-1.760254	-1.760179	.000075
82	96AB	-1.771240	-1.771756	-.000516
83	96BF	-1.777344	-1.777554	-.000210
84	96BF	-1.777344	-1.777554	-.000210
85	96AB	-1.771240	-1.771756	-.000516
86	9687	-1.760254	-1.760179	.000075
87	964F	-1.743164	-1.742861	.000303
88	9603	-1.719971	-1.719857	.000113
89	95A3	-1.690674	-1.691244	-.000570
90	9537	-1.657715	-1.657115	.000600
91	94B3	-1.617432	-1.617580	-.000148
92	941F	-1.572266	-1.572769	-.000503
93	937F	-1.523438	-1.522828	.000610
94	92CB	-1.468506	-1.467920	.000586
95	9207	-1.408691	-1.408223	.000468
96	9133	-1.343994	-1.343934	.000060
97	9053	-1.275635	-1.275261	.000374
98	8F63	-1.202393	-1.202428	-.000035
99	8E67	-1.125488	-1.125673	-.000185
100	8D5F	-1.044922	-1.045246	-.000325
101	8C4F	-.961914	-.961410	.000504
102	8B2F	-.874023	-.874439	-.000415
103	8A0B	-.784912	-.784614	.000298
104	88DB	-.692139	-.692231	-.000092
105	87A7	-.598145	-.597590	.000555
106	8667	-.500488	-.500999	-.000511
107	8527	-.402832	-.402775	.000057
108	83DF	-.302734	-.303236	-.000502
109	8297	-.202637	-.202709	-.000072
110	814B	-.101318	-.101520	-.000201

TABLE IV. Hex Code for 16-Bit Values (-15dB Output in 20V Full Scale Range).

CODE#	HEX CODE	IDEAL DAC OUT Volts	IDEAL SINE VALUE Volts	QUANTIZING ERROR Volts
1	7FFF	0.000000	0.000000	0.000000
2	7EB2	.101624	.101520	-.000104
3	7D67	.202637	.202709	.000072
4	7C1D	.303345	.303236	-.000109
5	7AD7	.402832	.402775	-.000057
6	7995	.501099	.500999	-.000099
7	7859	.597534	.597590	.000056
8	7723	.692139	.692231	.000092
9	75F4	.784607	.784614	.000007
10	74CE	.874329	.874439	.000110
11	73B1	.961304	.961410	.000107
12	729E	1.045227	1.045246	.000019
13	7196	1.125793	1.125673	-.000120
14	709B	1.202393	1.202428	.000035
15	6FAC	1.275330	1.275261	-.000069
16	6ECB	1.343994	1.343934	-.000060
17	6DF9	1.408081	1.408223	.000142
18	6D35	1.467896	1.467920	.000024
19	6C81	1.522827	1.522828	.000001
20	6BDD	1.572876	1.572769	-.000107
21	6B4B	1.617432	1.617580	.000148
22	6AC9	1.657104	1.657115	.000010
23	6A59	1.691284	1.691244	-.000040
24	69FB	1.719971	1.719857	-.000113
25	69B0	1.742859	1.742861	.000002
26	6977	1.760254	1.760179	-.000075
27	6951	1.771851	1.771756	-.000094
28	693E	1.777649	1.777554	-.000095
29	693E	1.777649	1.777554	-.000095
30	6951	1.771851	1.771756	-.000094
31	6977	1.760254	1.760179	-.000075
32	69B0	1.742859	1.742861	.000002
33	69FB	1.719971	1.719857	-.000113
34	6A59	1.691284	1.691244	-.000040
35	6AC9	1.657104	1.657115	.000010
36	6B4B	1.617432	1.617580	.000148
37	6BDD	1.572876	1.572769	-.000107
38	6C81	1.522827	1.522828	.000001
39	6D35	1.467896	1.467920	.000024
40	6DF9	1.408081	1.408223	.000142
41	6ECB	1.343994	1.343934	-.000060
42	6FAC	1.275330	1.275261	-.000069
43	709B	1.202393	1.202428	.000035
44	7196	1.125793	1.125673	-.000120
45	729E	1.045227	1.045246	.000019
46	73B1	.961304	.961410	.000107
47	74CE	.874329	.874439	.000110
48	75F4	.784607	.784614	.000007
49	7723	.692139	.692231	.000092
50	7859	.597534	.597590	.000056
51	7995	.501099	.500999	-.000099
52	7AD7	.402832	.402775	-.000057
53	7C1D	.303345	.303236	-.000109
54	7D67	.202637	.202709	.000072
55	7EB2	.101624	.101520	-.000104
56	7FFF	0.000000	0.000000	0.000000
57	814C	-.101624	-.101520	.000104
58	8297	-.202637	-.202709	-.000072
59	83E1	-.303345	-.303236	.000109
60	8527	-.402832	-.402775	.000057
61	8669	-.501099	-.500999	.000099
62	87A5	-.597534	-.597590	-.000056
63	88DB	-.692139	-.692231	-.000092
64	8A0A	-.784607	-.784614	-.000007
65	8B30	-.874329	-.874439	-.000110
66	8C4D	-.961304	-.961410	-.000107
67	8D60	-1.045227	-1.045246	-.000019
68	8E68	-1.125793	-1.125673	.000120
69	8F63	-1.202393	-1.202428	-.000035
70	9052	-1.275330	-1.275261	.000069
71	9133	-1.343994	-1.343934	.000060
72	9205	-1.408081	-1.408223	-.000142
73	92C9	-1.467896	-1.467920	-.000024
74	937D	-1.522827	-1.522828	-.000001
75	9421	-1.572876	-1.572769	.000107
76	94B3	-1.617432	-1.617580	-.000148
77	9535	-1.657104	-1.657115	-.000010
78	95A5	-1.691284	-1.691244	.000040
79	9603	-1.719971	-1.719857	.000113
80	964E	-1.742859	-1.742861	-.000002
81	9687	-1.760254	-1.760179	.000075
82	96AD	-1.771851	-1.771756	.000094
83	96C0	-1.777649	-1.777554	.000095
84	96C0	-1.777649	-1.777554	.000095
85	96AD	-1.771851	-1.771756	.000094
86	9687	-1.760254	-1.760179	.000075
87	964E	-1.742859	-1.742861	-.000002
88	9603	-1.719971	-1.719857	.000113
89	95A5	-1.691284	-1.691244	.000040
90	9535	-1.657104	-1.657115	-.000010
91	94B3	-1.617432	-1.617580	-.000148
92	9421	-1.572876	-1.572769	.000107
93	937D	-1.522827	-1.522828	-.000001
94	92C9	-1.467896	-1.467920	-.000024
95	9205	-1.408081	-1.408223	-.000142
96	9133	-1.343994	-1.343934	.000060
97	9052	-1.275330	-1.275261	.000069
98	8F63	-1.202393	-1.202428	-.000035
99	8E68	-1.125793	-1.125673	.000120
100	8D60	-1.045227	-1.045246	-.000019
101	8C4D	-.961304	-.961410	-.000107
102	8B30	-.874329	-.874439	-.000110
103	8A0A	-.784607	-.784614	-.000007
104	88DB	-.692139	-.692231	-.000092
105	87A5	-.597534	-.597590	-.000056
106	8669	-.501099	-.500999	.000099
107	8527	-.402832	-.402775	.000057
108	83E1	-.303345	-.303236	.000109
109	8297	-.202637	-.202709	-.000072
110	814C	-.101624	-.101520	.000104