CPL20
(CPL16L8, CPL16R4, CPL16R6 and CPL16R8)

CMOS Programmable Logic Array
20-Pin Series

FEATURES/BENEFITS

- High-speed CMOS equivalent to Bipolar PAL devices
- CMOS UV-erasable EPROM cell to allow reprogrammability
- Low power (35mA Max. I_{CC}) and standard (70mA Max. I_{CC}) versions
- Four speed grades (t_{PD} = 15ns Max, t_{PD} = 20ns Max, t_{PD}=25ns Max, and t_{PD} = 35ns Max)
- Available over both commercial and industrial temperature ranges
- >2000V ESD input and output protection
- 100% functional and AC tested
- 100% programming tested
- Programmable security bit to prevent pattern duplication
- Register Preload for register configuration
- Programmable three-state outputs

DESCRIPTION

The CPL20 Series devices are high-speed, UV-erasable, electrically programmable CMOS logic replacements of the Bipolar 20-pin PAL16R8 family. They utilize the familiar sum-of-products form (AND array followed by an OR array) allowing the user to customize logic to his/her needs.

Four devices are offered in the CPL20 Series. They are: the CPL16L8, the CPL16R4, the CPL16R6, and the CPL16R8. Each of these devices has 16 array inputs and 8 outputs. All the outputs to the CPL16L8 are combinatorial, while all the outputs to the CPL16R8 are registered. In contrast, the CPL16R4 has 4 registered and 4 combinatorial outputs, and the CPL16R6 has 6 registered and 2 combinatorial outputs. Each combinatorial output in the CPL16R6 and CPL16R4 devices serves as an I/O pin. The CPL16L8 device has 6 I/O pins.

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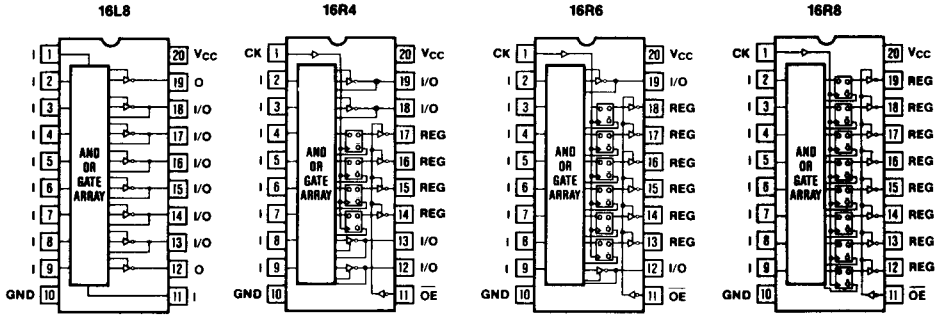
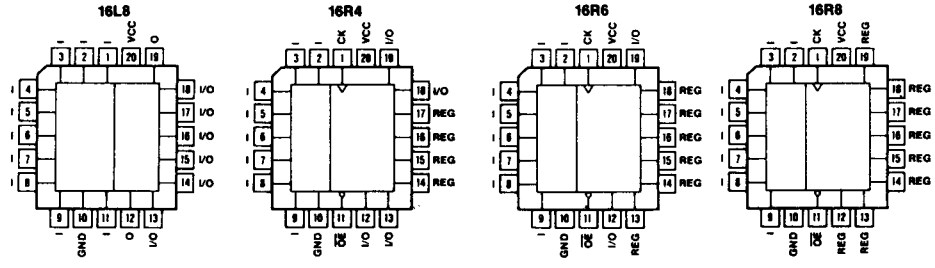
LOGIC SYMBOLS AND PINOUTS



DIP PACKAGES



PLCC PACKAGES

DESCRIPTION (Continued)

The CPL devices are manufactured using a 1.2 micron EPROM technology which offers low power dissipation (45/70 mA maximum I_{CC}) combined with high performance 15ns maximum propagation delay). Because the CPL devices are erasable, they can be thoroughly tested for programming, functional and AC integrity, resulting in high-reliability and 100% programming yields.

The CPL20 devices are housed in 20-pin plastic DIP, PLCC, and windowed CERDIP packages. The windowed CERDIP package allows the user to erase the CPL device using UV light, and later to reprogram it with a different pattern. The plastic DIP and PLCC devices are one-time-programmable (OTP) and may not be erased.

Register Preload

The register preload feature of the CPL20 Series allows output pins to be loaded with arbitrary states, making functional testing easier than ever.

Security Bit

All CPL20 devices feature a security bit. The security bit allows the user to protect his/her design against unauthorized duplication. When the security bit is set, the contents of the programmable-cell array may not be accessed in Read or Verify modes. Since the CPL devices do not have visible fuses, they offer enhanced security over what is available in bipolar PAL devices.

Test Array

Another feature of the devices in the CPL20 Series is the on-chip test array. It is programmed for final functional and AC testing of the devices after they have been packaged (even if the security bits have been programmed). In the normal operation of the device, the test arrays are not accessed. In the test mode of operation, only the input terms in the shaded portion of the functional block diagram are accessed. The test array facilitates high-reliability as well as simple and short testing.

ERASURE (windowed-CERDIP only)

The CPL devices will erase by light at wavelengths of under 4000 Angstroms. The window must be covered by an opaque label to prevent erasure by exposure to sunlight or fluorescent lighting.

Recommended dose of ultraviolet light for erasure:
Wavelength of 2537 Angstroms
(minimum dose -- 25 Wsec/cm^2)

If an ultraviolet lamp with a 12mW/cm^2 power rating is used, 30 to 35 minutes of erasure time will suffice. The lamp must be closer than 1 inch from the window to guarantee optimal erasing conditions. Exposure to high intensity UV light for an extended period of time may cause permanent damage to the CPL devices. The maximum dosage recommended is 7250 Wsec/cm^2.

CPL20 ABSOLUTE MAXIMUM RATINGS (Note 1)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
DC Input Voltage	V_{IN} ($\|I_{IN}\| \leqq 20mA$)	-3.0 to +7.0	V
Off-State DC Output Voltage	V_O	-0.5 to V_{CC} + 0.5	V
DC Programming Voltage		14.0	V
Storage Temperature	T_{STG}	-65 to +150	°C
Power Dissipation per Package	P_D (Note 2)	500	mW

Note 1: Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only, and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

Note 2: Power dissipation temperature derating:
Plastic Package (N): -12mW/°C from 65°C to 85°C
Ceramic Package (J): -12mW/°C from 100°C to 125°C

RECOMMENDED OPERATING CONDITIONS For CPL20-20, -25, and -35

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.5 to 5.5	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C
Operating Temperature Range, Industrial	T_A	-40 to +105	°C

RECOMMENDED OPERATING CONDITIONS For CPL20-15 (Preliminary)

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	4.75 to 5.25	V
DC Input and Output (Off-State) Voltages	V_{IN}, V_O (Note 3)	0 to V_{CC}	V
Operating Temperature Range, Commercial	T_A	0 to +70	°C
Operating Temperature Range, Industrial	T_A	-40 to +105	°C

Note 3: Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND).

CPL20 DC ELECTRICAL CHARACTERISTICS

Over Recommended Operating Conditions

Parameter	Symbol	Test Conditions		Min	Max	Unit
Low Level Input Voltage	V_{IL}				0.8	V
High Level Input Voltage	V_{IH}			2.0		V
Input Current	I_{IN}	$0 < V_{IN} < V_{CC}$		-10	10	μA
Low Level Output Voltage	V_{OL}	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OL} = 24mA		0.5	V
High Level Output Voltage	V_{OH}	V_{CC} = Min $V_{IN} = V_{IH}$ or V_{IL}	I_{OH} = -3.2mA	2.4		V
Off-State Output Leakage Current	I_{OZL}	V_{CC} = Max, $V_{IN} = V_{IH}$ or V_{IL}	V_O = 0.4V		-100	μA
	I_{OZH}		V_O = 2.4V		100	
Power Supply Current	I_{CC}	All inputs = GND V_{CC} = Max I_{OUT} = 0mA	"L" STD "L-15"		35 70 45	mA mA mA

Note 4: These are absolute values with respect to device ground. The applied voltage plus overshoots due to system and/or tester noise must not exceed these worst-case values.

CPL20 AC ELECTRICAL CHARACTERISTICS

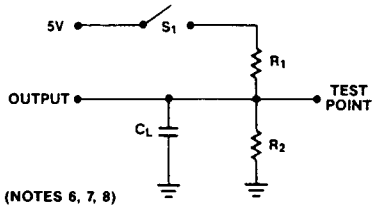
Over Recommended Operating Conditions (Note 5)

		Commercial (0 to +70°C)								Industrial (-40 to +105°C)								
		-15*		-20		-25		-35		-15*		-20		-25		-35		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input or Feedback to Non-Registered Output, 16R6, 16R4, 16L8	t_{PD}		15		20		25		35		15		20		25		35	ns
Clock to Registered Output or Feedback, 16R8, 16R6, 16R4	t_{CO}		12		15		15		25		12		15		15		25	ns
Pin 11 to Output Enabled, 16R8, 16R6, 16R4	t_{PZX11}		12		15		20		25		12		15		20		25	ns
Pin 11 to Output Disabled, 16R8, 16R6, 16R4	t_{PXZ11}		12		15		20		25		12		15		20		25	ns
Input to Output Enabled, 16R6, 16R4, 16L8	t_{PZX}		15		20		25		35		15		20		25		35	ns
Input to Output Disabled, 16R6, 16R4, 16L8	t_{PXZ}		15		20		25		35		15		20		25		35	ns
Setup Time from Input or Feedback to Clock, 16R8, 16R6, 16R4	t_{SU}	12		15		20		30		12		15		20		30		ns
Hold Time, 16R8, 16R6, 16R4	t_H	0		0		0		0		0		0		0		0		ns
Clock Width (High or Low)	t_W	10		15		15		20		10		15		15		20		ns
Clock Period	t_P	24		30		35		55		24		30		35		55		ns
Maximum Frequency	f_{MAX}	41.6		33.3		28.5		18		41.6		33.3		28.5		18		MHz

* Preliminary

Note 5: Input rise and fall times (10% to 90% of V_{CC}): $t_r = t_f \leqq 6$ns.

AC Test Circuit



Resistor Values (Ω)

R1	R2
200	390

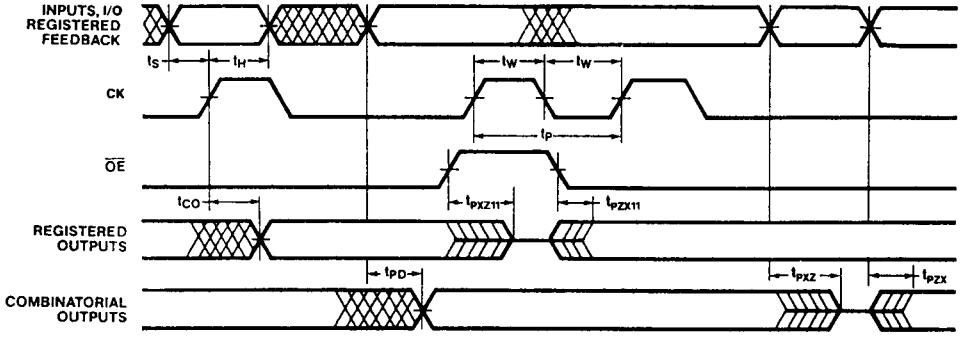
Note 6: C_L includes load and test jig capacitance.

Note 7: t_{PD} is tested with switch S_1 closed and C_L = 50pF.

Note 8: For 3-State outputs, output enable times are tested with C_L = 50pF to the 1.5V level; S_1 is open for high impedance to HIGH tests and closed for high impedance to LOW tests. Output disable times are tested with C_L = 5pF. HIGH to high impedance tests are made to an output voltage of V_{OH} - 0.5V with S_1 open; LOW to high impedance tests are made to the V_{OL} = 0.5V level with S_1 closed.

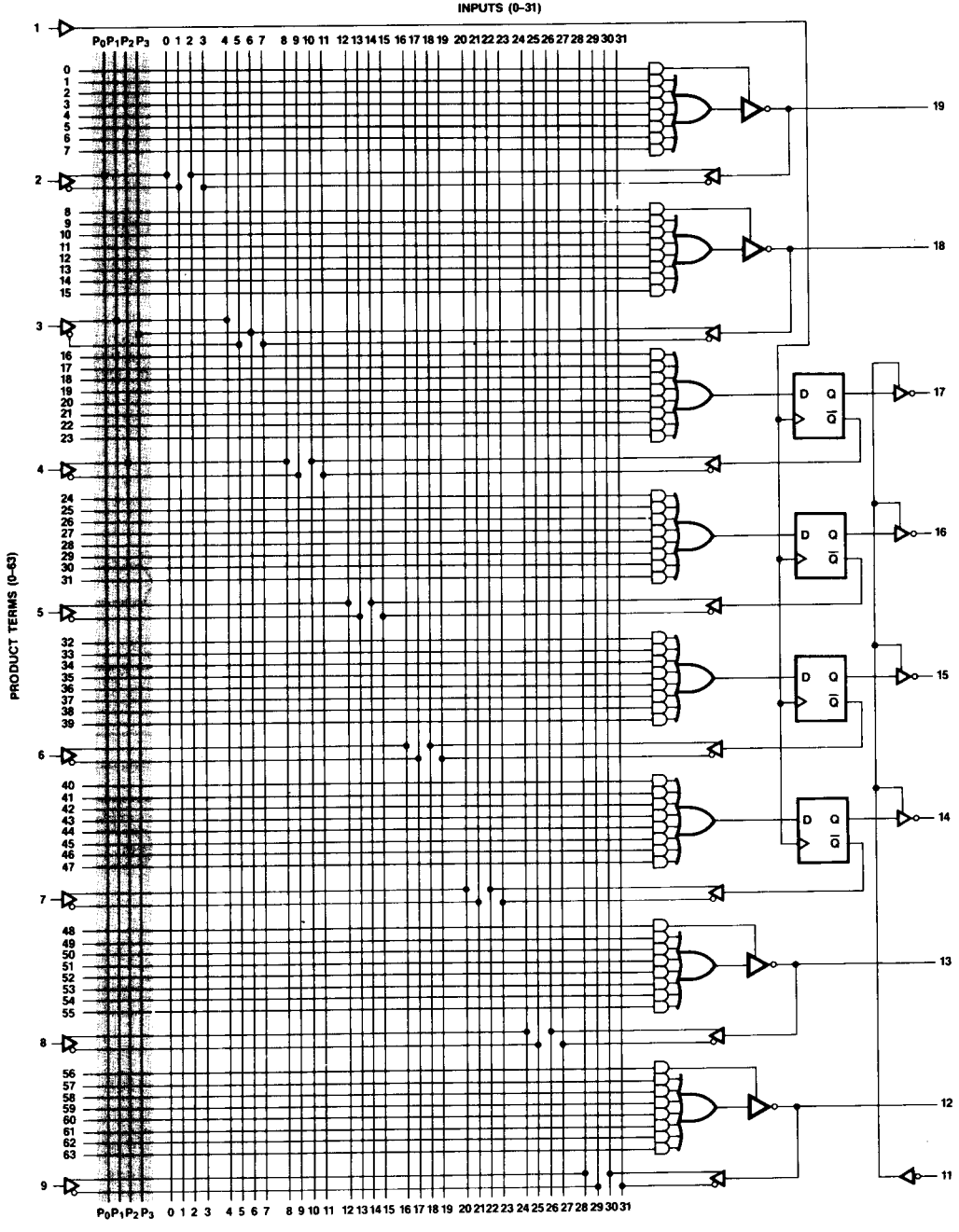
3

CPL20 SWITCHING WAVEFORMS



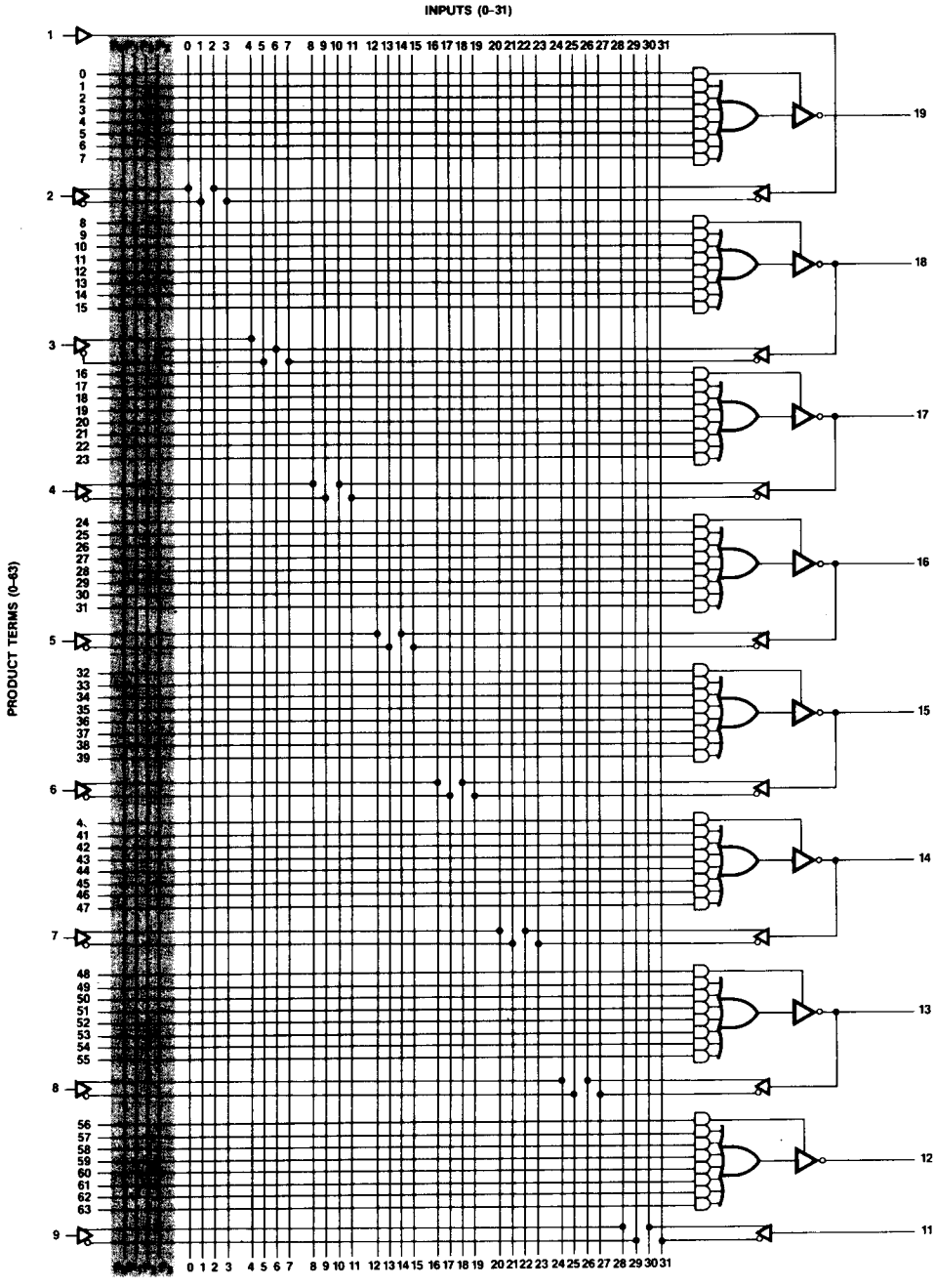
CPL20 FUNCTIONAL LOGIC DIAGRAMS (Continued)

CPL16R4



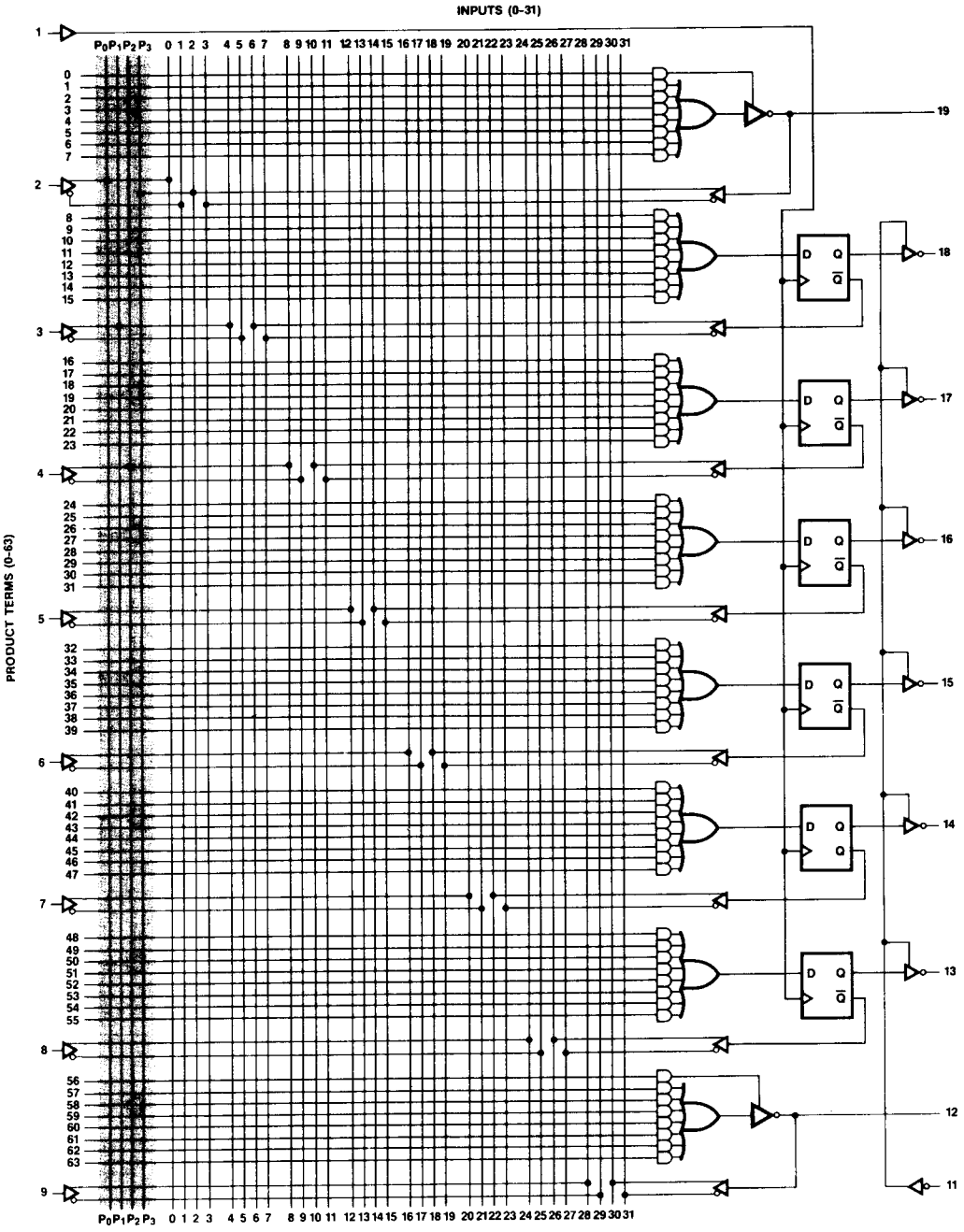
CPL20 FUNCTIONAL LOGIC DIAGRAMS

CPL16L8

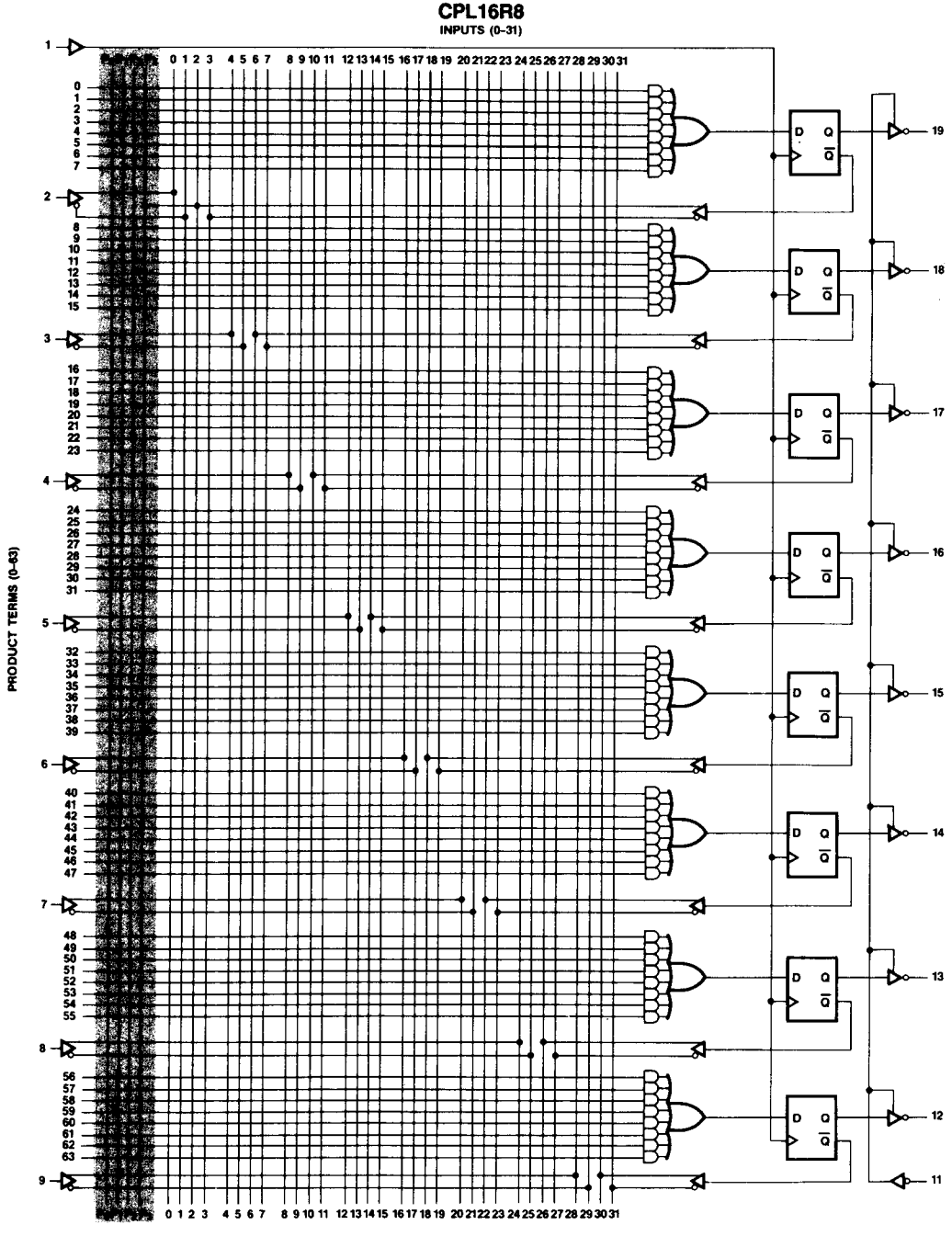


CPL20 FUNCTIONAL LOGIC DIAGRAMS (Continued)

CPL16R6

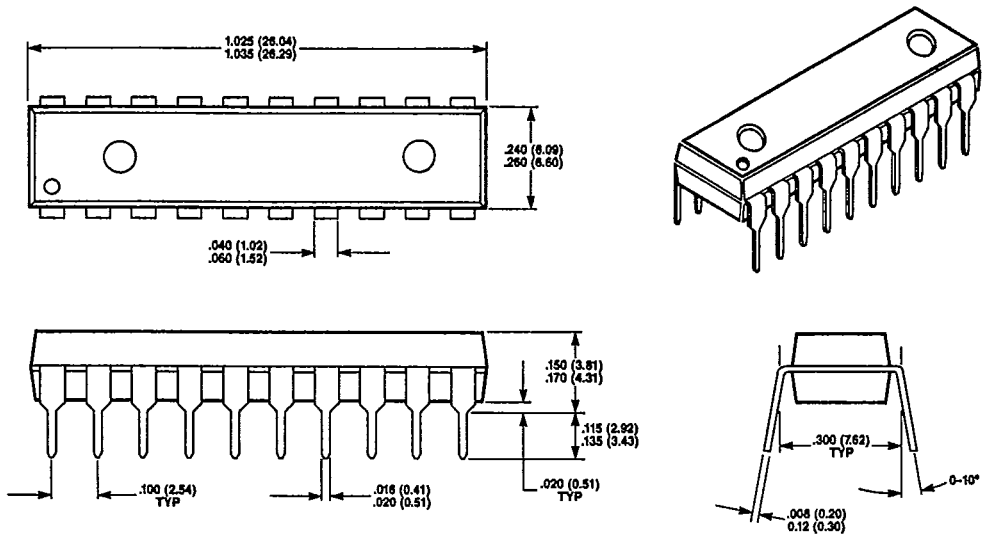


CPL16R8


INPUTS (0–31)
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
PRODUCT TERMS (0–63)
1
2
3
4
5
6
7
8
9
0 1 2 3 4 5 6 7
8 9 10 11 12 13 14 15
16 17 18 19 20 21 22 23
24 25 26 27 28 29 30 31
32 33 34 35 36 37 38 39
40 41 42 43 44 45 46 47
48 49 50 51 52 53 54 55
56 57 58 59 60 61 62 63
D Q
19
18
17
16
15
14
13
12
11

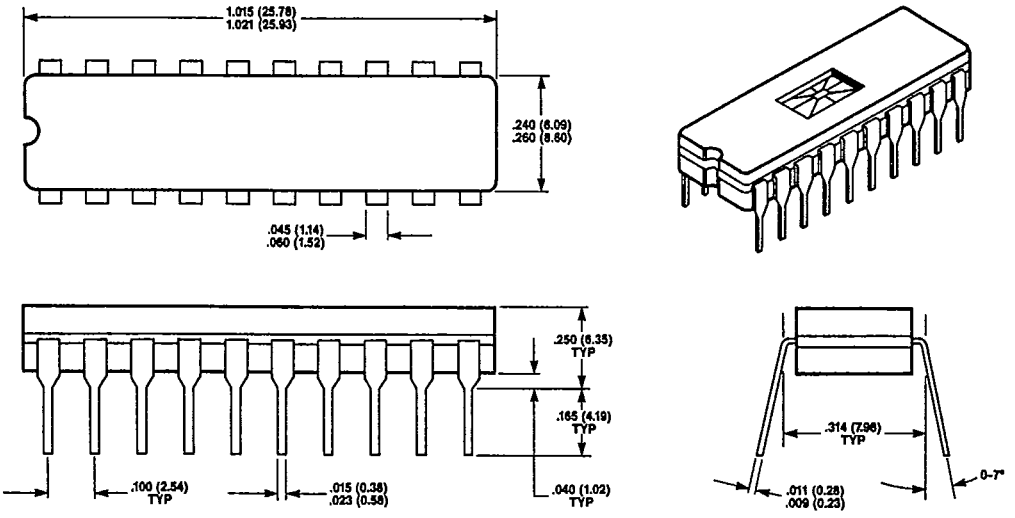
T-90-20

20 PIN PLASTIC DIP



DIMENSIONS IN INCHES
AND (MILLIMETERS)
MIN.
MAX.

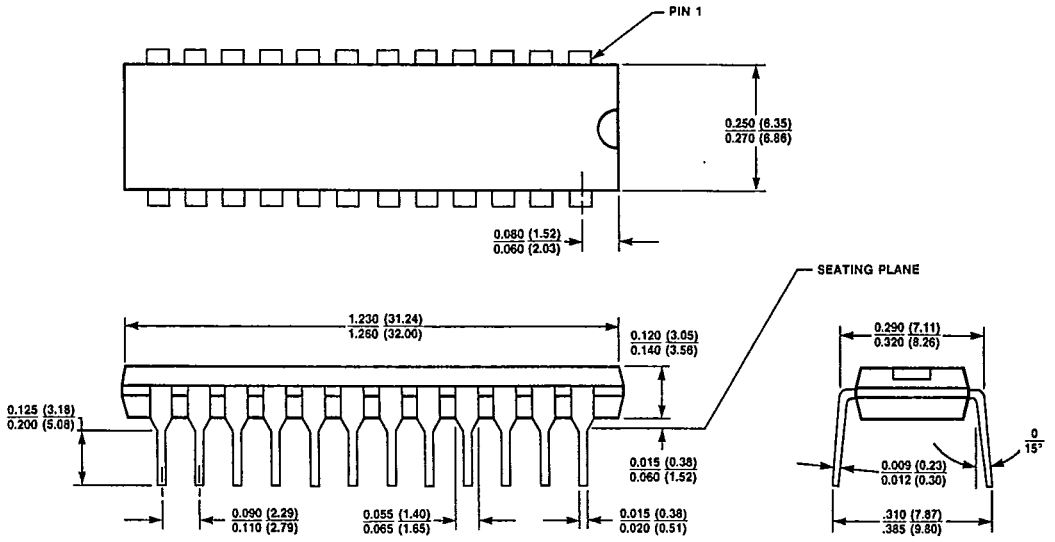
20 PIN WINDOWED CERDIP



DIMENSIONS IN INCHES
AND (MILLIMETERS)
MIN.
MAX.

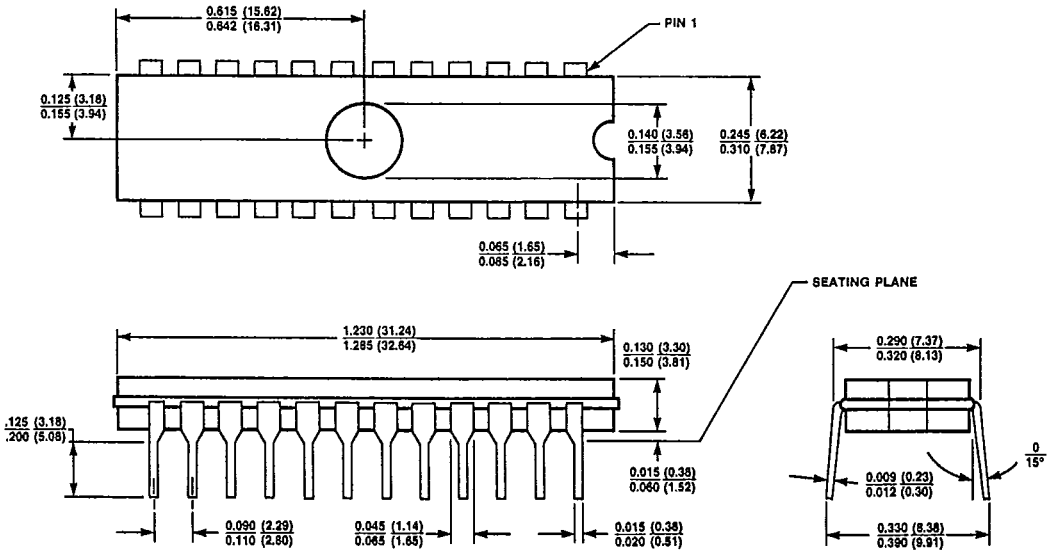
7

24 PIN PLASTIC DIP



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

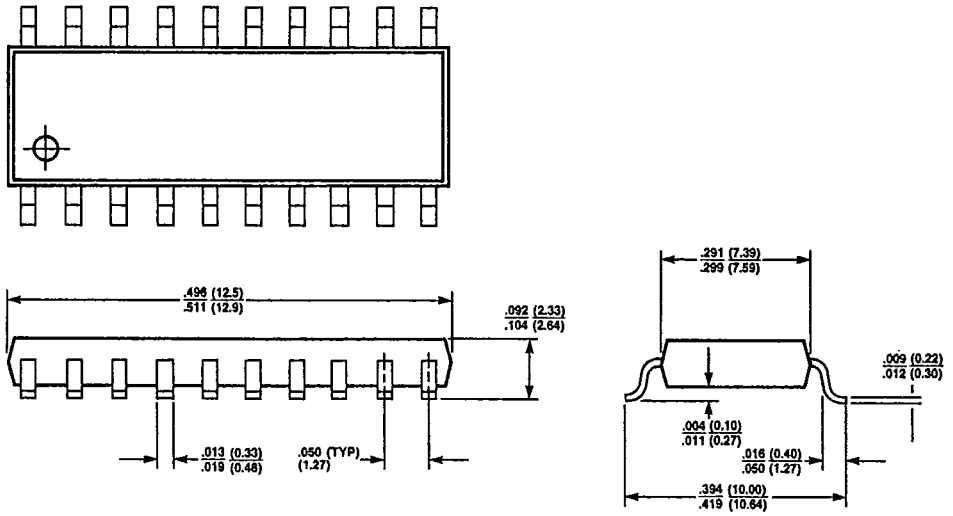
24 PIN WINDOWED CERDIP



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

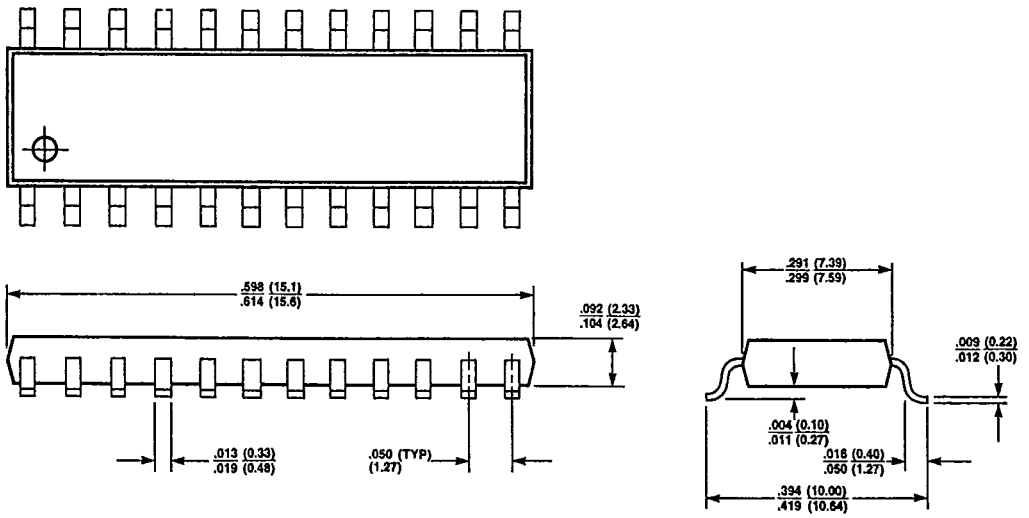
T-90-20

20 PIN SOIC



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

24 PIN SOIC

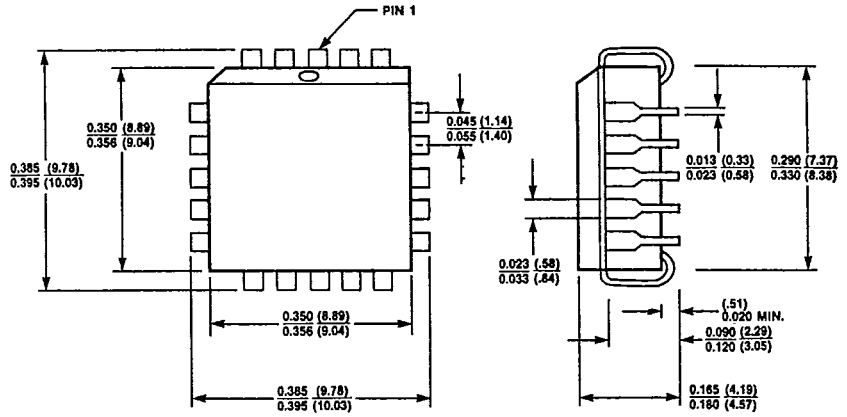


DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

7

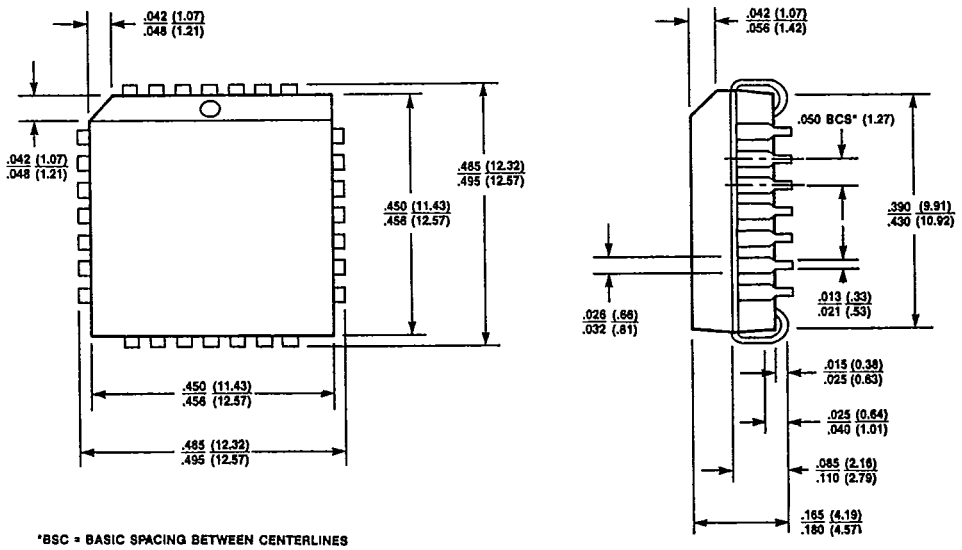
T-90-20

20 PIN PLCC



DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.

28 PIN PLCC



*BSC = BASIC SPACING BETWEEN CENTERLINES

DIMENSIONS IN INCHES AND (MILLIMETERS)
MIN.
MAX.